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General Standards Corporation

High Performance Bus Interface Solutions

Rev: 090412

PMC-16AO12

16-BIT, 12-CHANNEL, PMC HIGH SPEED ANALOG OUTPUT BOARD

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC-16AO12 board is a single-width PCI mezzanine card (PMC) that provides precision high-speed analog output capability for the PCI bus. Twelve 16-bit analog output channels provide output ranges of ±2.5V, ±5V or ±10V, and can be clocked either simultaneously or sequentially at rates up to 400 KSPS (Kilosamples per second) per channel. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.1, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification. A PCI interface adapter supports the "plug-n-play" initialization concept.

Power requirements consist of +5 VDC from the PCI bus in accordance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling. Specific details of physical characteristics and power requirements are contained in the PMC-16AO12 product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

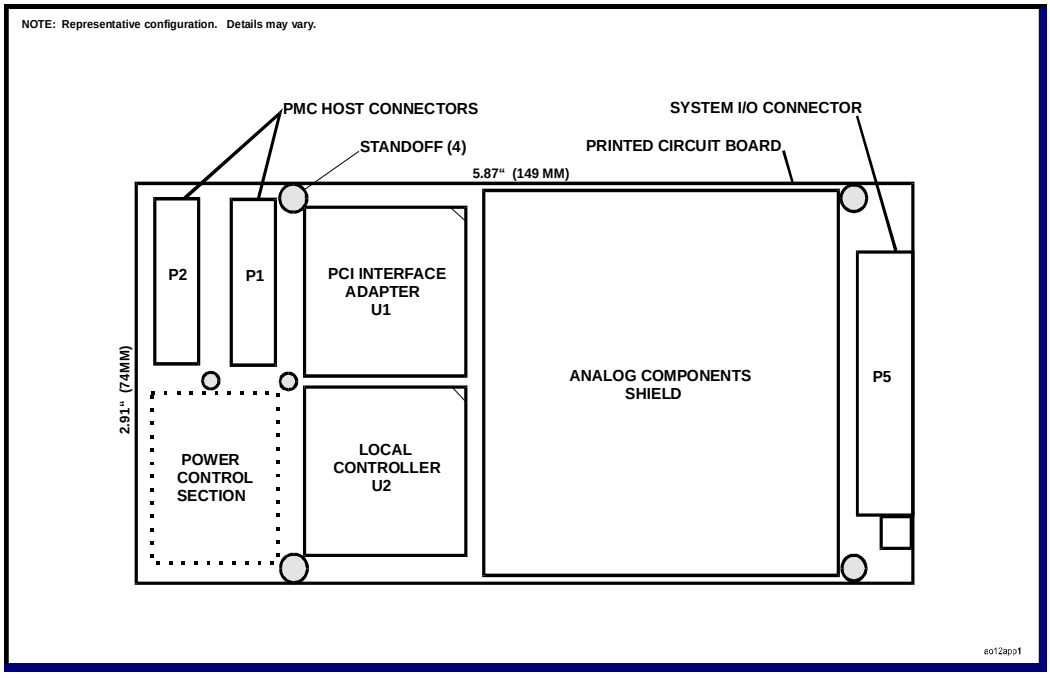


Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made through a single 50-pin, dual-ribbon front-access I/O connector. The analog outputs are set to zero-level (midrange) during initialization.

1.2 Functional Overview

Principal capabilities of the PMC-16AO12 board are summarized in the following list of features.

- 12 Precision High-Speed Analog Output Channels
- 16-Bit Resolution; D/A Converter per Channel
- Data Rates to 400K Samples per Second per Channel; 4.8 MSPS Aggregate Rate
- Outputs Updated Simultaneously or Sequentially; Software-Selectable
- Output Ranges of ±10V, ±5V or ±2.5V
- 32K, 64K or 128K-Sample Analog Output FIFO Buffer Configurable as Circular or Open
- Continuous and Triggered-Burst (One-Shot) Output Modes
- Data Rate Controlled by Adjustable Internal Clock or by Externally Supplied Clock
- Supports Multiboard Synchronization.
- Internal Autocalibration of all Channels
- Differential Sync I/O Available for Synchronizing GSC's Sigma-Delta ADC Boards
- Active Buffer Size Adjustable from 1 Sample to 32K Samples
- Fast Settling; 5 us to 0.1%; 8 us to 0.01%;with No-filter Option
- Integral Shield Assures Minimum Susceptibility to Radiated Noise in PMC Environment
- Single-width PMC Form Factor.

Figure 1.2-1 outlines the internal functional organization of the board. The twelve analog output channels are controlled through an analog output buffer, and can be updated either simultaneously or sequentially. The output sample rate can be controlled by an internal rate generator, or by an external clock source. Internal selftest networks permit all channels to be calibrated automatically to a single internal voltage reference.

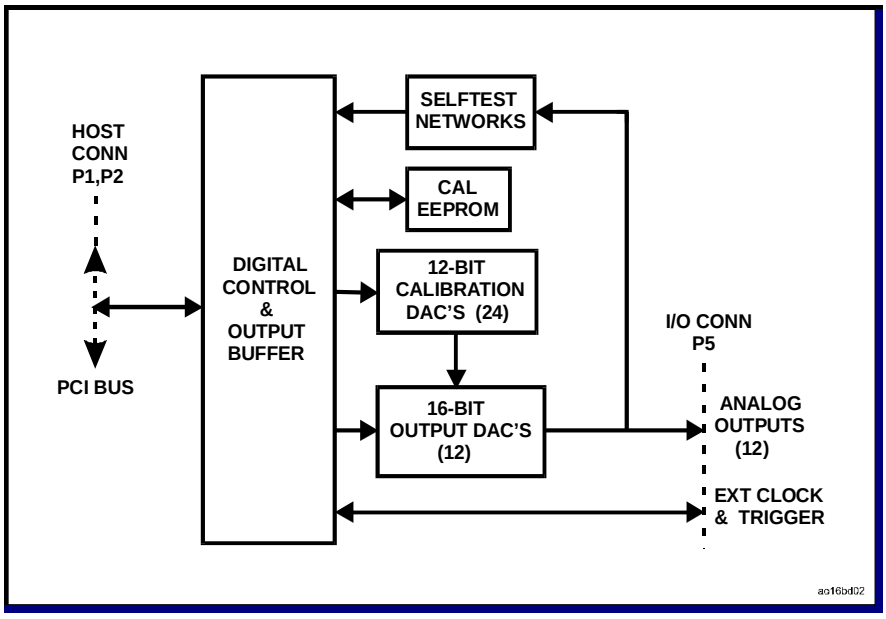


Figure 1.2-1. Functional Organization

Offset and gain trimming of the output D/A converters (DAC's) are performed by 12-bit calibration DAC's. Correction values for the calibration DAC's are determined during autocalibration, and are stored in nonvolatile EEprom for subsequent transfer to the calibration DAC's during board initialization. Autocalibration can be invoked at any time from the PCI bus.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector with the mating connectors on the host board, and carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the four standoffs are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2.2-1. I/O connector P5 is designed to mate with a 50-pin dual-ribbon connector, equivalent to 3M# P50E-050S-EA. This insulation displacement (IDC) cable connector accepts two 25-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2.2-1 and in Figure 2.2.2-1. Contact the factory if preassembled cables are required.

Table 2.2.2-1. System Connector Pin Functions

P5A	
PIN	SIGNAL
1	OUTPUT RETURN
2	OUTPUT CHANNEL 00
3	OUTPUT RETURN
4	OUTPUT CHANNEL 01
5	OUTPUT RETURN
6	OUTPUT CHANNEL 02
7	OUTPUT RETURN
8	OUTPUT CHANNEL 03
9	OUTPUT RETURN
10	OUTPUT CHANNEL 04
11	OUTPUT RETURN
12	OUTPUT CHANNEL 05
13	OUTPUT RETURN
14	OUTPUT CHANNEL 06
15	OUTPUT RETURN
16	OUTPUT CHANNEL 07
17	OUTPUT RETURN
18	OUTPUT CHANNEL 08
19	OUTPUT RETURN
20	OUTPUT CHANNEL 09
21	OUTPUT RETURN
22	OUTPUT CHANNEL 10
23	OUTPUT RETURN
24	OUTPUT CHANNEL 11
25	OUTPUT RETURN

P5B		
PIN	SIGNAL	
1	OUTPUT RETURN	
2	REMOTE GROUND SENSE	
3	OUTPUT RETURN	
4	OUTPUT RETURN	
5	VRANGE RETURN	
6	VRANGE OUTPUT	
7	VRANGE RETURN	
8	OUTPUT RETURN	
9	OUTPUT RETURN	
10	OUTPUT RETURN	
11	OUTPUT RETURN	
12	OUTPUT RETURN	
13	OUTPUT RETURN	
14	OUTPUT RETURN	
15	OUTPUT RETURN	
16	OUTPUT RETURN	
17	DIGITAL RETURN	
18	TRIGGER INPUT	(TRIG INPUT HI)
19	DIGITAL RETURN	(TRIG INPUT LO)
20	TRIGGER OUTPUT	(TRIG OUTPUT HI)
21	DIGITAL RETURN	(TRIG OUTPUT LO)
22	CLOCK INPUT	(CLOCK IO HI)
23	DIGITAL RETURN	(CLOCK IO LO)
24	CLOCK OUTPUT	(CLOCK OUTPUT HI)
25	DIGITAL RETURN	(CLOCK OUTPUT LO)

(Signal names in parentheses () apply only is the differential sync I/O option is present.)

2.3 System Configuration

2.3.1 Output Considerations

The twelve analog output channels are single-ended and have a common signal return that is referred to in Table 2.2.2-1 as OUTPUT RETURN. In general, single-ended outputs should drive only loads that are isolated from system ground. The best results are obtained when the loads also are isolated from each other.

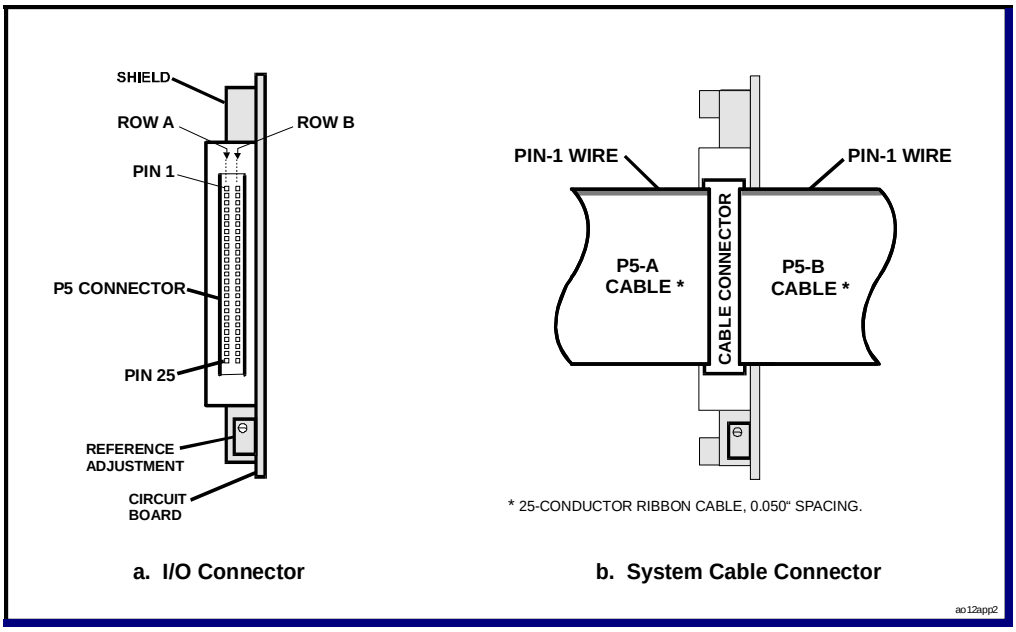


Figure 2.2.2-1. Input/Output Connector and Cables

2.3.1.1 Line Losses

The voltage drop in ribbon cable can be a significant source of error in 16-bit systems, even with relatively short cables driving low-current loads. Figure 2.3.1-1 shows the effect of load current on the voltage drop in copper wire of various sizes. A 2.0 milliamp load for example, will insert a voltage drop of approximately 130 microvolts *per foot* in conventional #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors in a 16-bit system, in which 1 LSB may represent only 76 microvolts (±2.5 Volt range). High impedance loads, however, generally will not produce significant DC line loss errors.

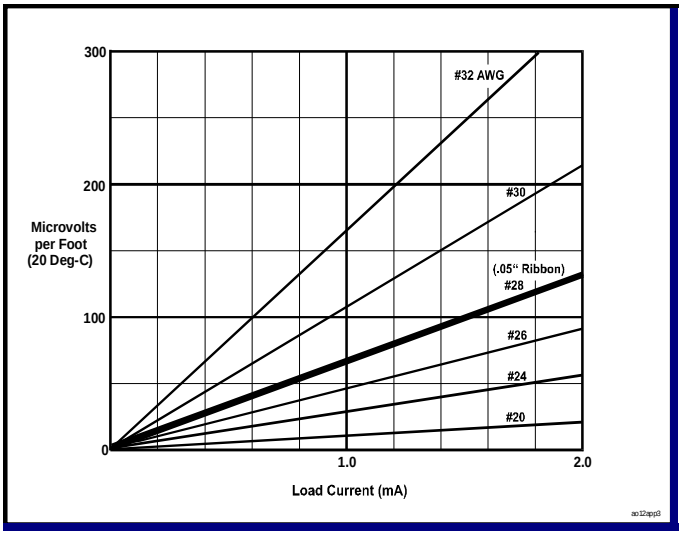


Figure 2.3.1-1. Line Loss Versus Load Current

2.3.1.2 Output Configurations

Figure 2.3.1-2 shows the primary sources of error in both isolated and nonisolated system configurations. For loads that are isolated from each other (Figure 2.3.1-2a), the total line-loss error is twice the loss produced in a single line, assuming equal wire size and length for output and return lines. For loads with a common return that is isolated from system ground, line loss in the common return appears as crosstalk between channels.

If the load return is inadvertently connected to a remote system ground (Figure 2.3.1-2b), the potential difference Vgnd between the system ground and the internal signal return will introduce an error into the signal delivered to the load. The ground current Ignd developed in the return line is limited essentially only by Rgnd, and may damage the cable or the board if not controlled.

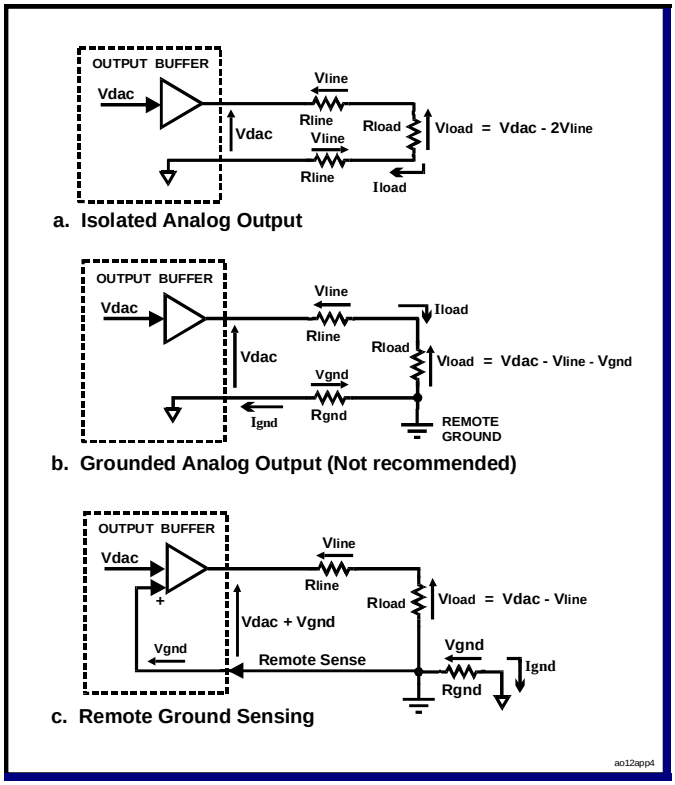


Figure 2.3.1-2. Output Configurations

2.3.1.3 Remote Ground Sensing

If a significant potential difference is expected between the ground connection at the load and the output return from the board, remote ground sensing should be considered. When remote ground sensing is enabled, the input signal at the REMOTE GROUND SENSE pin in the I/O connector is used to adjust the output voltages of all channels to produce the desired voltage levels at the load. As Figure 2.3.1-2c indicates, external connection of the remote ground to the local system ground prevents potentially damaging ground current Ignd from passing through the board and I/O cable.

To provide correction for the potential difference between the analog output return and the remote system ground, the REMOTE GROUND SENSE input must be connected to the remote system ground, and remote sensing must be enabled by the control software. If remote ground sensing is not implemented, the REMOTE GROUND SENSE input should be connected to OUTPUT RETURN.

The remote sensing input affects all analog output channels, and consequently can be a significant source of noise if not adequately protected from external sources of radiated interference.

2.3.2 Sample Clock Input

When external clocking is selected by the control software, the analog outputs are updated at the rate present at the CLOCK INPUT pin in the I/O connector. The clock input is TTL compatible, and is active on a HIGH-to-LOW transition. The external clock frequency should not exceed the maximum sample rate that is specified for the board.

NOTE: If the differential sync I/O option is present, the trigger and clock inputs and outputs are Low Voltage Differential Signaling (LVDS) levels. The CLOCK IO pin is a 16-32MHZ output when the board is operating as an Initiator, or a sample-clock pulse input when in the Target mode. Pins designated as "HI" in Table 2.2.2-1 are noninverted signals, and the "LO" inputs are the inverted returns.

NOTE: To use the TRIGGER OUT as the SYNC input to an SDI-series sigma-delta board, the TRIGGER OUT HI and LO outputs must be connected to the SYNC LO and HI inputs, respectively, at the SDI board.

2.3.3 Burst Trigger Input

If burst triggering is enabled by the control software, an external TTL signal can initiate a data burst by applying a HIGH-to-LOW transition on the TRIGGER INPUT pin of the I/O connector. In order for the trigger input to be acknowledged by the board, the TRIGGER OUTPUT signal must be HIGH. TRIGGER OUTPUT is LOW during a burst, and is HIGH when the burst is completed.

2.3.4 Multiboard Synchronization

2.3.4.1 Synchronized Bursts

If multiple boards are to be burst-synchronized together, the TRIGGER OUTPUT from one board, the *burst-initiator*, is connected to the TRIGGER INPUT pins of a group *of burst-target* (Figure 2.3.4-1). Each burst-target, when operated in the triggered-burst mode, will initiate a single burst from its buffer each time the burst-initiator initiates a burst. The initiator can be configured for either continuous or burst operation.

2.3.4.2 Synchronized Clocks

To clock-synchronize multiple boards together, the CLOCK OUTPUT from one board, designated the *clock-initiator*, is connected to the CLOCK INPUT of one or *more clock-target* boards. The clock-targets are software-configured for external clocking, and the initiator can be configured for either external or internal clocking.

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference calibration. The optimum calibration interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended.

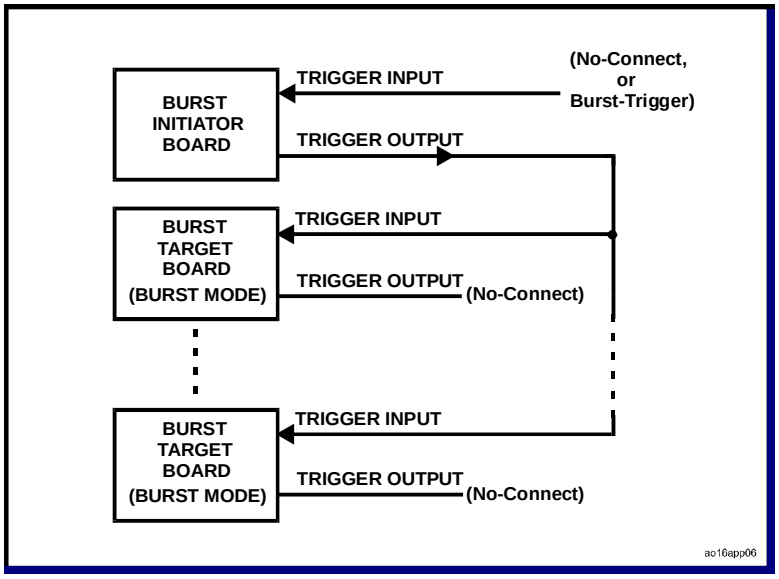


Figure 2.3.4-1. Multiboard Burst Synchronization

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and input signal levels, should be evaluated before troubleshooting of the board itself is attempted. If surface-mount repair capability is not available, a board that is suspected to be defective should be returned to the factory for problem analysis and repair.

2.5 Calibration

All output channels are software-calibrated to an internal voltage reference (Vrange) by an embedded autocalibration software utility. The calibration procedure presented here describes the adjustment of the reference. For applications in which the system must not be powered down, the board can be calibrated under normal operating conditions while installed on the existing host board.

To eliminate the requirement for a special test connector, the two test points required for calibration, VRANGE OUTPUT and VRANGE RETURN, can be made available at a system breakout connector or test panel. This arrangement also eliminates the necessity of disconnecting the system input/output cable for reference calibration.

2.5.1 Equipment Required

Table 2.5.1-1 lists the minimum equipment requirements for calibrating the PMC-16AO12 board. Alternative equivalent equipment may be used.

Table 2.5.1-1. Calibration Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Standard 50-Pin, 0.05", dual-ribbon cable connector, with test leads. (Not required if calibration test points are made permanently available at a system connection point)	Robinson Nugent	P50E-050-S-TG

2.5.2 Calibration Procedure

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification.

Adjustment of the internal reference (Vrange) is performed with an internal trimpot that is accessible from the front of the board, as shown in Figure 2.2.2-1. The adjustment seal on the trimmer should be removed before beginning the procedure, and the trimmer should then be resealed with a suitable sealing agent after calibration has been completed.

This procedure assumes that the board to be calibrated is installed on a host board, and that the host is installed in an operating system. The board can be operating in any mode when the adjustment is performed.

1. Connect the digital multimeter between the VRANGE OUTPUT (+) and VRANGE RETURN (-) pins in the system I/O connector. Refer to Table 2.2.2-1 for pin assignments.
2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding..
3. Adjust the REFERENCE ADJUSTMENT trimmer until the digital multimeter indication is within the appropriate range listed in the following table:

OUTPUT VOLTAGE RANGE	MULTIMETER INDICATION (DC Volts)
±10 Volts	+9.9902 ±0.0009
± 5 Volts	+4.9951 ±0.0005
±2.5 Volts	+2.4976 ±0.0003.

4. Calibration is complete. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC-16AO12 board is compatible with the PCI Local Bus specification, and supports auto configuration at the time of power-up. The PCI interface is controlled by a PLX™ PCI-9080 I/O accelerator device. Configuration-space registers are initialized internally to support the location of the board on any eight-longword boundary in memory space. After initialization has been completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers to the analog output buffer.

Table 3.1-1. Control and Data Registers

OFFSET	REGISTER	ACCESS MODE*	ACTIVE BITS	PRIMARY FUNCTION
00	BOARD CONTROL (BCR)	R/W	16	Board Control Register (BCR)
04	CHANNEL SELECTION	R/W	12	Channel-enabling
08	SAMPLE RATE	R/W	16	Analog output clocking rate selection
0C	BUFFER OPERATIONS	R/W	16	Buffer size selection and status flags
10	(Reserved)	---	---	---
14	(Reserved)	---	---	---
18	OUTPUT DATA BUFFER	WO	17	Analog output FIFO buffer
1C	ADJUSTABLE CLOCK	R/W	10	Control of the adjustable clock (Optional)

* Access mode is D32. R/W = Read/Write; WO = Write-only

3.2 Board Control Register

As Table 3.2-1 indicates, the BCR consists of 16 control bits and status flags. Specific control bits are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section. The BCR initializes to the value 0010h (0810h if the interrupt request is asserted).

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3.1-1.

Table 3.2-1. Board Control Register

Offset: 0000h **Default: 0810h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	BURST ENABLED	0	Selects burst-mode if HIGH, continuous-mode if LOW. Default is LOW; i.e. continuous-mode.
D01	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.
D02	R/W	*BURST TRIGGER	0	Software burst trigger, asserted HIGH. Active only when BURST ENABLED control bit is asserted. Initialized LOW.
D03	R/W	REMOTE GROUND SENSE	0	Correction is made for remote ground potentials when this bit is HIGH.
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.
D05	R/W	(Reserved)	0	
D06	R/W	(Reserved)	0	
D07	R/W	SIMULTANEOUS OUTPUTS	0	When HIGH, selects simultaneous output clocking. When LOW, selects sequential clocking. Default is LOW; i.e.: sequential clocking.
D08	R/W	INTERRUPT A0	0	Interrupt source selection.
D09	R/W	INTERRUPT A1	0	
D10	R/W	INTERRUPT A2	0	
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board asserts an interrupt request. Clears the request when cleared LOW by the bus.
D12	R/W	*CM0	0	Calibration mode. Defaults to normal operation.
D13	R/W	*CM1	0	Completion available as an interrupt condition.
D14	RO	BIT STATUS FLAG	0	Records the status of autocalibration; LOW for pass, HIGH for fail. Initializes LOW.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all defaults for all registers.

* Cleared automatically when operation is completed. R/W = Read/Write; RO=Read-Only.

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted as described in Section 3.6.

Table 3.3.1-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Loading of the PCI configuration registers is completed within 3 milliseconds or less after the assertion of a PCI bus reset, and should be required only once after the initial application of power. During this interval, the response to PCI target accesses is RETRYs. PCI register configuration terminates with the PCI interrupts disabled (Paragraph 3.6).

3.3.2 Initialization

Internal control logic is initialized, without invoking configuration, by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- Calibration D/A converters are initialized with correction values from internal EEprom
- The analog output buffer is reset to empty
- All analog output levels are set to zero (midrange)
- Data coding format is offset binary
- All channels are active
- Internal clocking is selected
- Clocking is disabled
- Clocking mode is continuous and sequential
- Buffer configuration is open, with maximum size selected
- The local interrupt request is asserted (ignored unless PCI interrupts are enabled)
- The BCR is initialized; all defaults are invoked
- If present, the optional adjustable clock frequency is not initialized.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Output Control

Section 3.4 describes those operations that control the movement of data from the PCI bus through the analog output buffer. These functions include the selection of active channels, the organization of data within the buffer, and the clocking of data from the buffer to the analog outputs. The principal parameters associated with controlling the analog output channels are summarized below in Table 3.4-1. Section 3.8 provides detailed examples of analog output operations.

Table 3.4-1. Summary of Output Control Parameters

Parameter	Mode	Description
Data Control	Active Channels	A single set of all active output channels constitutes an *Active Channel Group.* Active channels are selected under a channel mask.
	Data Frame	All data values in the buffer comprise a *Data Fr*ame.
	Data Coding	Output data can be coded either in offset-binary format or in two's complement format.
Active Buffer	Size Selection	The active buffer is a subset of the physical output data buffer. Active buffer size is determined by the SIZE[3..0] control-bit field in the buffer operations register.
	Status Flags	Status flags buffer-empty, buffer-low-quarter, buffer-high-quarter and buffer-full are provided for the active buffer.
Buffer Configuration	Open	Data read from the buffer is used and then discarded, until the buffer is empty.
	Circular (closed)	Data within the buffer is recirculated. Each value read from the output of the buffer FIFO is written back to the input of the FIFO. An end-of-frame (EOF) flag tracks the movement of data through the buffer.
Clock Source	External	External hardware provides the sample clock.
	Internal	The sample clock is provided by an internal rate generator, at a rate determined by the sample rate control register.
Clocking Mode	Simultaneous	At each clock occurrence, the next channel group (i.e.: a single group of all active channel values) in the output buffer is transferred to the respective analog output channels. All outputs are updated simultaneously.
	Sequential	At each clock occurrence, the next active channel value in the output buffer is transferred to the associated analog output channel, which is updated immediately.
Sampling Mode	Continuous	The contents of the output buffer are sampled continuously at the selected clock rate.
	Triggered Burst	A single data frame in the buffer is clocked to the outputs.

3.4.1 Data Organization

3.4.1.1 Active Channels

Analog output data is loaded into the output buffer in discrete groups of channel data. An active *channel group* consists of a single set of output values for all active channels.

Only active output channels receive data from the output buffer. A channel that is deselected to the inactive state retains the last value that was received while the channel was still active. During initialization, all channels are selected as active.

3.4.1.1.1 Selection

An output channel is selected as *active* by setting the corresponding selection bit HIGH in the Channel Selection Register, as shown in Table 3.4.1-1. A channel is deselected to the *inactive* state by clearing the corresponding selection bit. To select Channels 3, 6, 7 and 10 as active, for example, the selection bits in the selection register would have the value 4C8h.

Table 3.4.1-1. Channel Selection Register

Offset: 0004h **Default: 0FFFh**

BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	CHANNEL 00 ENABLED	Channel-Enable mask. A channel is enabled if the associated mask bit is HIGH, or is disabled if the bit is LOW. May be truncated for 8-channel and 4-channel boards.
D01	R/W	CHANNEL 01 ENABLED	
D02	R/W	CHANNEL 02 ENABLED	
D03	R/W	CHANNEL 03 ENABLED	
D04	R/W	CHANNEL 04 ENABLED *	
D05	R/W	CHANNEL 05 ENABLED *	
D06	R/W	CHANNEL 06 ENABLED *	
D07	R/W	CHANNEL 07 ENABLED *	
D08	R/W	CHANNEL 08 ENABLED **	
D09	R/W	CHANNEL 09 ENABLED **	
D10	R/W	CHANNEL 10 ENABLED **	
D11	R/W	CHANNEL 11 ENABLED **	
D12	---	(Reserved)	---
D13	---	(Reserved)	---
D14	---	(Reserved)	---
D15	---	(Reserved)	---

R/W = Read/Write. * 8-Channel and 12-Channel boards only. ** 12-Channel boards only.

3.4.1.1.2 Loading

Channel data values are loaded into the output buffer in ascending order of the active channels. The channel groups are loaded contiguously, beginning with the first group to be transferred to the outputs, and proceeding sequentially to the last group. Figure 3.4.1-1 illustrates a loading example that represents three active channels, with 100 values per channel. Each channel group consists of active channels 3, 6 and 8. Consequently the value in the channel selection register is 0148h.

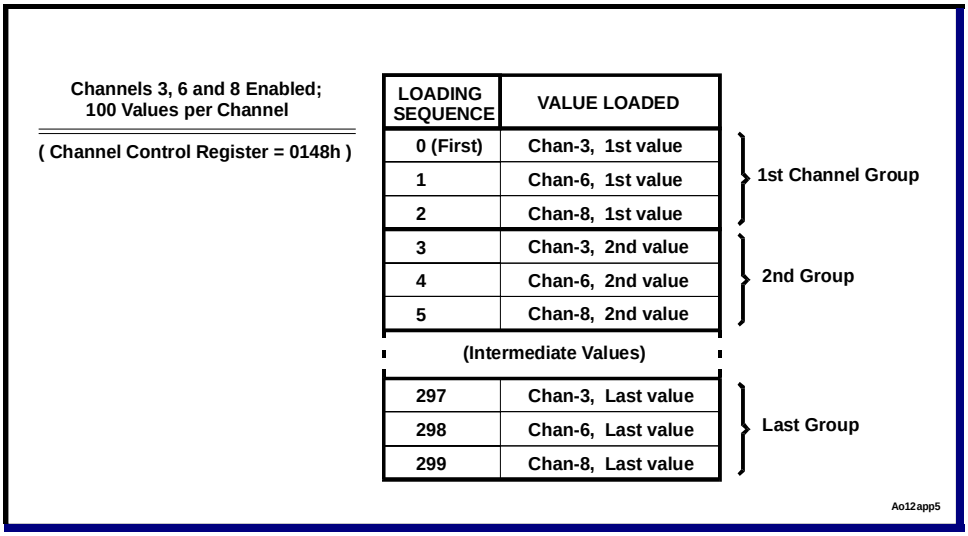


Figure 3.4.1-1. Typical Buffer Loading Sequence

3.4.1.2 Data Frame

A *data frame* consists of an integral number of contiguous channel groups.

For triggered bursts, or for function concatenation, the last active channel in the last channel group is designated as the *end-of-frame* (EOF). The EOF designation is applied by setting the EOF flag (D16) HIGH when loading the last channel value into the buffer. Thereafter, the EOF flag follows the last channel value through the buffer.

3.4.1.3 Output Data Format

3.4.1.3.1 Output Data Buffer

Analog output data values are written in word-serial sequence from the PCI bus to the Output Data Buffer register shown in Table 3.4.1-2. Bits D15..0 represent the output data value. Bit D16 is set HIGH to indicate the last value in a data frame, and is the end-of-frame (EOF) flag. Bits D31..17 are inactive and have no effect. Access to the output buffer is supported for both single-longword transfers and single-address multiple-longword DMA transfers.

Table 3.4.1-2. Output Data Buffer

Offset: 0018h **Default: N/A (Write-Only)**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	**DATA 00**	Least significant data bit
D01-D14	WO	**DATA 01 - DATA 14**	Intermediate data bits
D15	WO	**DATA 15**	Most significant data bit
D16	WO	**EOF FLAG**	End-of-frame (EOF) flag.
D17-D31	WO	**---**	(Inactive)

* WO indicates write-only access. Read-access produces all-zero value.

3.4.1.3.2 Output Data Coding

Analog output data can be coded either in 16-bit offset binary format by asserting the OFFSET BINARY control bit HIGH in the BCR, or in two's complement format by clearing the control bit LOW (Table 3.4.1-3). Analog output data transactions are D32 (32 bits), but the data significance is 16 bits.

Table 3.4.1-3. Output Data Coding; D15..0

ANALOG OUTPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	XXXX FFFF	XXXX 7FFF
Zero plus 1 LSB	XXXX 8001	XXXX 0001
Zero	XXXX 8000	XXXX 0000
Zero minus 1 LSB	XXXX 7FFF	XXXX FFFF
Negative Full Scale plus 1 LSB	XXXX 0001	XXXX 8001
Negative Full Scale	XXXX 0000	XXXX 8000

Positive Full Scale is a positive level that equals the range option defined for the board (e.g.: +5.000 Volts for the ±5V option). *Negative Full Scale* is the negative equivalent of positive full-scale. *Full-scale Range* (FSR) is the total voltage range for the output channel . One LSB equals the full-scale range divided by 65,536. (e.g.: 152.59 microvolts for the ±5V option).

3.4.2 Output Buffer

The *physical output buffer* consists of a 17-bit wide FIFO that has a capacity of 32K, 64K, or 128K output values, depending on the factory configuration ordered. Each output value is 16 bits wide and occupies a single location within the FIFO. The 17th bit is an end-of-frame flag that is attached to the last value in a data frame. Data values are transferred from the PCI bus to the analog output channels through an *active buffer*, which is a subset of the physical buffer.

3.4.2.1 Buffer Operations Register

The *buffer operations register* (BOR) controls the configuration of the output buffer, as well as related functions such as clocking and loading. The BOR (Table 3.4.2-1) is 16 bits wide and resides at relative offset 0Ch.

3.4.2.2 Active Buffer

The *active buffer* is a virtual buffer that represents a subset of the physical buffer, and which is the working buffer through which all output data flows. The size of the active buffer is adjustable from a single value up to the full size of the physical buffer. The buffer can be cleared to the empty state by setting the CLEAR BUFFER control bit HIGH in the buffer operations register. CLEAR BUFFER clears automatically after the reset operation has been completed.

Note: Data loss may occur if the buffer is allowed to fill completely.

The active buffer performs exactly like a physical buffer of the same size. That is, a full buffer will accept no further data from the bus, and an empty buffer indicates that all outputs are idle. Buffer status flags (empty, low-quarter, high-quarter and full) respond to the size of the *active buffer*, not to the size of the physical buffer.

Table 3.4.2-1. Buffer Operations Register

Offset: 000Ch **Default: 340Dh**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	SIZE0	1	Size-selection bit field for the active buffer.
D01	R/W	SIZE1	0	Defaults to Dh (32K Samples).
D02	R/W	SIZE2	1	
D03	R/W	SIZE3	1	
D04	R/W	EXTERNAL CLOCK	0	Selects hardware or software clock source when HIGH, or the internal rate generator when LOW. Default is LOW (internal rate generator).
D05	R/W	ENABLE CLOCK	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).
D06	RO	CLOCK READY	0	If external clocking is selected, indicates when HIGH that a hardware or software clock will be accepted. If LOW, indicates that the output is not ready to accept a clock. Active only when external clocking is selected.
D07	R/W	*SW CLOCK	0	If external clocking is selected, produces a single output clock event when asserted. Clears LOW automatically when the clock event is completed. Active only when external clocking is selected.
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.
D09	R/W	*LOAD REQUEST	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available as an interrupt condition. Defaults HIGH.
D11	R/W	*CLEAR BUFFER	0	Resets the buffer to empty.
D12	R/W	BUFFER EMPTY	1	Status flags for the active buffer. Empty, lo-quarter and
D13	RO	BUFFER LOW QUARTER	1	hi-quarter flags are available as conditions for an interrupt
D14	RO	BUFFER HIGH QUARTER	0	request.
D15	RO	BUFFER FULL	0	

R/W = Read/Write, RO = Read-only. * Clears LOW automatically when operation is completed.

Buffer size is determined by the SIZE[3..0] control bit field in the buffer operations register. Available active buffer sizes are listed in Table 3.4.2-2.

Table 3.4.2-2. Active Buffer Size

SIZE[3:0]	BUFFER SIZE (Total Channel Values)	SIZE[3:0]	BUFFER SIZE (Total Channel Values)
0	4	8	1024
1	8	9	2048
2	16	A	4096
3	32	B	8192
4	64	C	16384
5	128	D	32768
6	256	E	*65536
7	512	F	**131072

* With 64K-Sample buffer option, or ** with 128K-Sample buffer option.

3.4.2.3 Status Flags

Status flags for the buffer operate with respect to the active buffer, and can provide an interrupt request if the active buffer becomes empty, 3/4-full, or less than 1/4-full. The status flags are located in the buffer operations shown in Table 3.4.2-1. A bit field in the BCR controls interrupt request selection.

3.4.2.4 Open Buffer

Data in an open buffer is discarded as it is used. Consequently, the buffer is self-flushing, and will empty itself unless it is replenished from the bus. This mode of operation permits the continuous flow of data from the PCI bus to the analog outputs. The buffer status flags are useful in this situation, and provide an indication of whether the buffer is empty, less than 1/4 full (low-quarter), equal to or greater than 3/4 full (high-quarter), or full. A full buffer will discard additional data from the bus, while an empty buffer indicates that the outputs are idle. The low-quarter and high-quarter flags are used to control data flow through the buffer when generating continuous functions.

NOTE: Data loss may occur if the buffer is allowed to fill completely.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.4.2-1 illustrates the movement of a single data frame through an open buffer.

3.4.2.5 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While closed, the buffer is not accessible from the bus. (Example 3.8.4).

In Figure 3.4.2-2, a single data frame is loaded into the buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

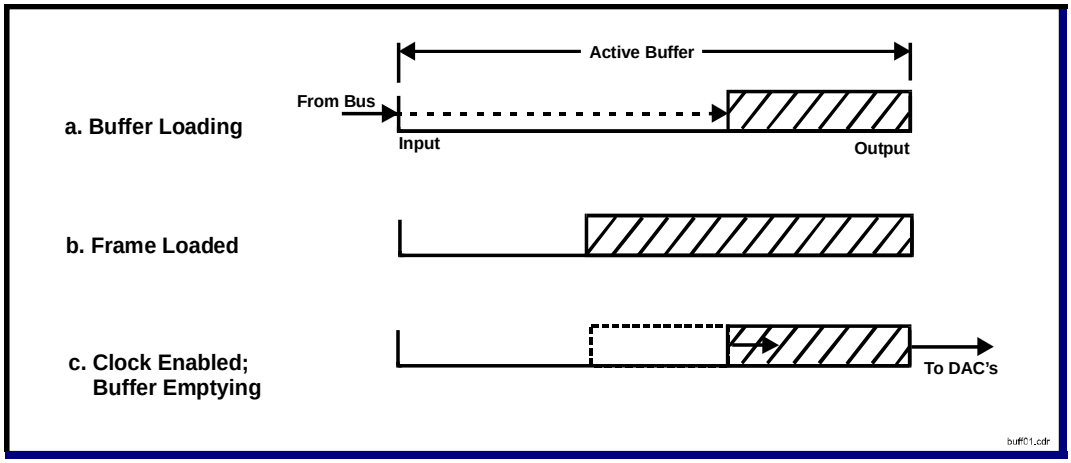


Figure 3.4.2-1. Open Buffer Data Flow

An end-of-frame (EOF) flag accompanies the end-point, or last value in a data frame. The EOF flag is D16 in the buffer, and is set HIGH when the last value in a data frame is loaded. The EOF flag is used during a triggered burst to define the last value in the burst. Multiple burst functions can reside in the buffer simultaneously.

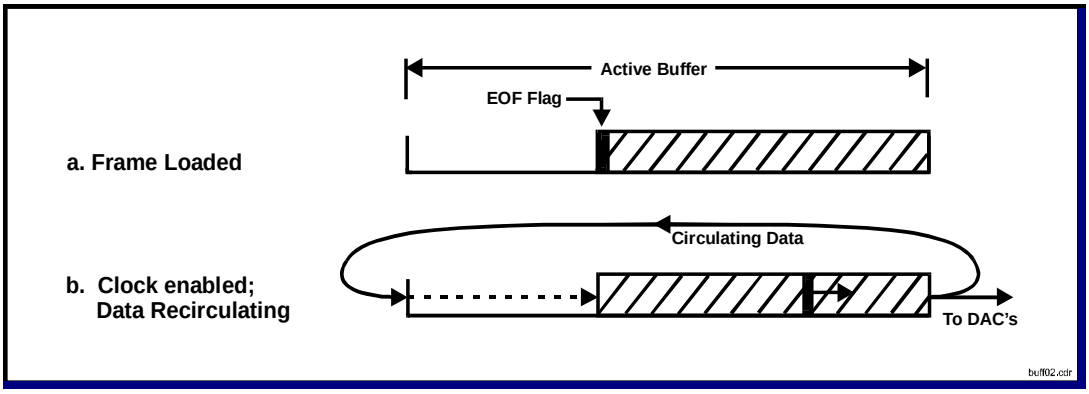


Figure 3.4.2-2. Circular Buffer Data Flow

3.4.3 Output Clocking

When the ENABLE CLOCK control bit in the buffer operations register is asserted HIGH, the active analog outputs are updated at each occurrence of the sample clock. The sample clock can be generated internally by the rate generator, or can be supplied externally through the I/O connector.

NOTE: If the differential sync I/O option is present, refer to Section 3.10 for information pertaining to differential sync inputs and outputs, and to the operation of the adjustable clock generator.

Hardware output signal CLOCK OUTPUT goes HIGH momentarily when a sample clock occurs, Connecting this signal to the CLOCK INPUT pins of other boards permits synchronous clocking of multiple boards.

3.4.3.1 Clock Source

When buffer operations register bit EXTERNAL CLOCK is HIGH, the sample clock is supplied externally through the I/O connector as CLOCK INPUT. If the EXTERNAL CLOCK control bit is LOW, the sample clock is derived from the internal rate generator.

3.4.3.1.1 External Clock

The external clock source can have any frequency up to the maximum value specified for the sampling rate. When the external clock source is selected, sampling occurs on a HIGH-to-LOW transition of the CLOCK INPUT pin in the I/O connector.

Hardware output signal CLOCK OUTPUT goes HIGH momentarily when a sample clock occurs, Connecting this signal to the CLOCK INPUT pins of other boards permits synchronous clocking of multiple boards.

3.4.3.1.2 Internal Rate Generator

The internal rate generator provides a sample clock that is adjustable by the RATE[15..0] control bits in the SAMPLE RATE control register (Table 3.4.3-1).

Table 3.4.3-1. Sample Rate Control Register

Offset: 0008h **Default: 004Bh**

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	**RATE00**	Least significant rate bit
D01-D14	R/W	**RATE01 - RATE14**	Intermediate rate bits
D15	R/W	**RATE15**	Most significant rate bit
D16-D31	*R/W	**---**	(Inactive)

* Active in write-mode only. Read-access retrieves all-zero.

The sample rate Rs is calculated from the relationship:

Rs (Hz) = 30,000,000 / Nrate ,

where Nrate is the decimal equivalent of the value in the SAMPLE RATE control register. Table 3.4.3-2 illustrates the effect of Nrate on the sample rate. Values less than 75 (4Bh) for Nrate may produce unpredictable results, and are not recommended.

NOTE: If the differential sync I/O option is present, refer to Section 3.10 for information pertaining to differential sync inputs and outputs, and to the operation of the adjustable clock generator.

3.4.3.2 Simultaneous Clocking

Simultaneous sampling is selected by setting the SIMULTANEOUS OUTPUTS control bit in the board control register HIGH. If simultaneous sampling is selected, the analog values in each successive channel group appear simultaneously at the outputs, with minimum time-skew between channels. Upon each occurrence of the sampling clock, an entire active channel group is transferred from the output buffer, and all outputs are updated simultaneously. In this mode, the effective sample rate for each channel equals the sample rate **Rs**.

Table 3.4.3-2. Sample Rate Selection

Nrate (RATE[15..0])		SAMPLE RATE Rs *
(Dec)	(Hex)	(Samples per Second)
75	004B	400,000
76	004C	394,747
77	004D	389,610
---	---	Rs (Hz) = 30,000,000 / Nrate
---	---	
---	---	
65534	FFFE	457.78
65535	FFFF	457.77

* ±0.015 percent.

3.4.3.3 Sequential Operation

Sequential sampling is selected when the SIMULTANEOUS OUTPUTS control bit in the board control register is LOW. At each clock occurrence in sequential operation, a single channel value is transferred from the buffer to the associated output channel, and the channel is updated immediately. Channel values are read from the buffer beginning with the lowest-numbered active channel in a channel group, and proceeding upward through the highest-numbered active channel. (Example 3.8.1). When operating in this mode, the sample rate for each channel equals the sample rate **Rs** divided by the number of active channels.

3.4.4 Sampling Mode

3.4.4.1 Continuous Sampling

When the *continuous sampling* mode is selected, data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that a sample clock is present. In order for a sample clock to be present, the ENABLE CLOCK control bit in the buffer control register must be HIGH. Continuous sampling is selected when the BURST ENABLED control bit in the board control register is LOW. (Examples 3.8.2 and 3.8.3).

3.4.4.2 Data Bursts

During a *triggered burs*t, data is transferred continuously from the buffer to the analog outputs until either the buffer is empty, or the end-of-frame (EOF) flag is encountered. In the triggered-burst sampling mode, a software or hardware trigger initiates the transfer of data from the output buffer to the output channels. A software trigger occurs when the BURST TRIGGER control bit in the board control register is set HIGH. The BURST TRIGGER bit is cleared automatically when the burst is completed.

A hardware burst trigger occurs upon a HIGH-to-LOW transition of the TRIGGER INPUT pin of the I/O connector, *if* the BURST ENABLED control bit in the BCR is HIGH, *and* if the BURST READY flag in the BCR is also HIGH. The BURST READY flag is LOW during a burst, and is HIGH if no burst is in progress.

Hardware output signal TRIGGER OUTPUT is LOW during a burst, and is HIGH when the burst is completed. Connecting this signal to the TRIGGER INPUT pins of other boards permits synchronous burst triggering of multiple boards.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used (Paragraph 3.4.1.2). The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected sample rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

3.4.5 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal. Multiple boards can be arranged to operate with:

a. Independent clocking and burst triggering
b. Synchronous burst triggering
c. Synchronous clocking
d. Synchronous clocking and burst triggering.

As many as four boards can be synchronized together.

3.4.5.1 Synchronous Bursts

To burst-synchronize a group of boards, the TRIGGER OUTPUT from one board, the *burst-initiator*, is connected to the TRIGGER INPUT pins of a group *of burst-target* boards. Each burst-target, when operated in the triggered-burst mode (BURST ENABLED set HIGH in the board control register), initiates a single burst from its buffer each time the burst-initiator initiates a burst. The initiator can be configured for either continuous or burst operation.

3.4.5.2 Synchronous Clocking

To clock-synchronize multiple boards together, the CLOCK OUTPUT from one board, designated the *clock-initiator*, is connected to the CLOCK INPUT of one or *more clock-target* boards. The clock-targets are configured for external clocking (EXTERNAL CLOCK set HIGH in the buffer control register), and the initiator can be configured for either external or internal clocking.

NOTE: If the differential sync I/O option is present, refer to Section 3.10 for information pertaining to differential sync inputs and outputs, and to the operation of the adjustable clock generator.

3.4.6 Function Generation

3.4.6.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous sampling and circular operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly. Clocking is enabled when the ENABLE CLOCK control bit in the buffer operations register is HIGH. (Example 3.8.4).

If triggered-burst sampling is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a software or hardware trigger, and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform values are retained in the buffer, and the waveform can be produced again by a subsequent trigger. (Example 3.8.5).

3.4.6.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst sampling is selected, the functions will be generated sequentially in response to a series of burst triggers. If the buffer is open, the functions will be flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions will be retained in the buffer, and the series of functions will be repeated indefinitely. (Example 3.8.5).

3.4.6.3 Function Sequencing

A new function (data frame) can be concatenated to the end of an existing function in a circular buffer, while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes and the new function seamlessly begins circulating in the buffer and producing an output. (Example 3.8.6).

The introduction of the new function commences by setting the LOAD REQUEST flag HIGH in the buffer operations register, and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has been opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame. The board's interrupt request will respond to the assertion of LOAD READY, if Load Ready is selected in the INT[] control field of the board control register.

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag (D16 set HIGH). The EOF flag causes the buffer to close, and clears both the LOAD READY flag and the LOAD REQUEST control bit. Notice that the loading of the new function into the buffer must be completed before the existing function terminates. The board's interrupt request will respond to the HIGH-to-LOW transition of LOAD READY if End Load Ready is selected in the INT[] control field of the board control register.

In Figure 3.4.6-1, An existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

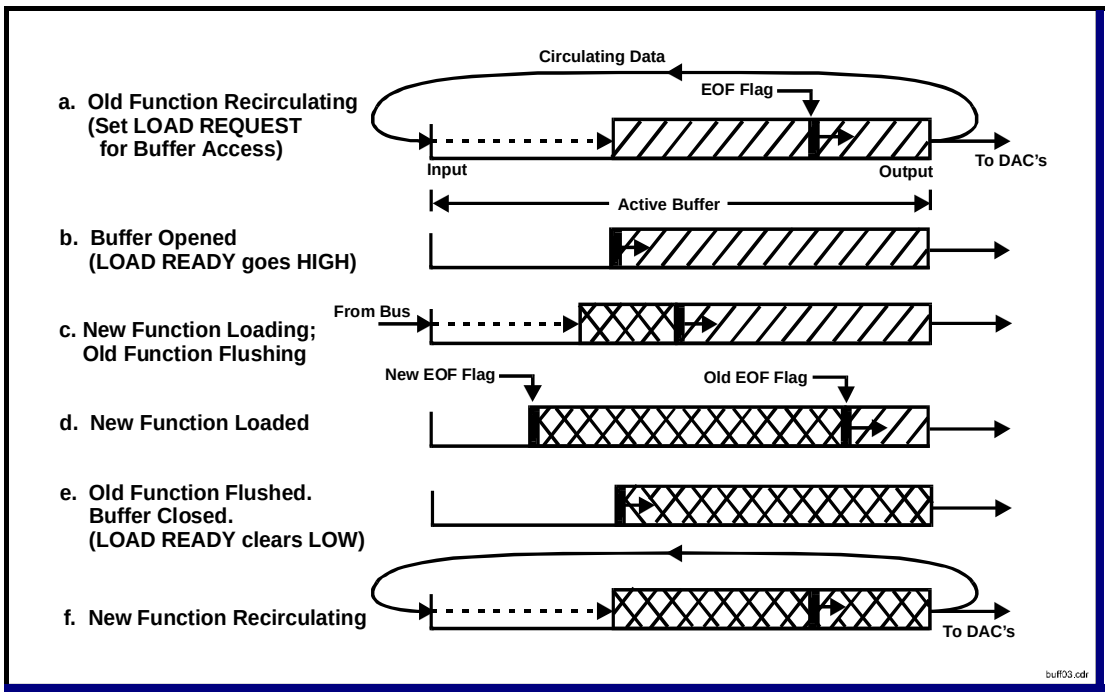


Figure 3.4.6-1. Function Sequencing

3.5 Autocalibration

Autocalibration is invoked by control bits CM[1..0] in the BCR. If both bits are LOW, the board is in the normal operating mode. Autocalibration is initiated by setting CM[1] HIGH (CM[1..0]=2), as shown in Table 3.5-1. CM[1..0] returns to zero (normal operation) automatically at the end of autocalibration. During initialization, CM[1..0] is set to Normal Operation as the default state.

Table 3.5-1. Calibration Mode Selection

BCR Bits D13..12 **Default: 0h**

CM[1:0]	FUNCTION
0	Normal operation. No calibration activity. Default state.
1	(Reserved).
2	Invoke Autocalibration
3	(Reserved)

Autocalibration has a duration of approximately 3-5 seconds. Completion of the operation can be detected either by polling cm[1..0] for a zero-state, or by selecting the 'Calibration-mode operation complete' interrupt condition (paragraph 3.6) and waiting for the interrupt request. Write-accesses from the PCI bus should be avoided during autocalibration, and the board should be initialized after autocalibration is completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the new values in both the EEprom and the calibration DAC's. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major

environmental transition such as that which usually occurs directly after power is applied. The analog outputs are active during autocalibration.

Calibration correction values for analog output channels are stored in nonvolatile EEprom, which retains the correction values when power is removed. The calibration values are transferred automatically from the EEprom to the calibration DAC's during board initialization.

If a board is defective, the autocalibration process may be unable to successfully calibrate all output channels. If this situation occurs, the BIT STATUS FLAG bit in the BCR will be set HIGH at the end of the autocalibration interval, and will remain HIGH until a subsequent initialization or autocalibration occurs. BIT STATUS FLAG remains LOW unless an autocalibration failure occurs.

3.6 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.6.2.

3.6.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The source condition for the request is selected as shown in Table 3.6.1-1. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until either (a) the PCI bus clears the BCR request flag, or (b) the associated interrupt condition is deasserted. A local interrupt request is generated automatically at the end of initialization.

Table 3.6.1-1. Interrupt Source Selection

BCR Bits D10..D08 **Default: 0h**

INTERRUPT A[2:0]	INTERRUPT CONDITION
0	Idle. Interrupt disabled unless initializing. Default state.
1	Calibration-mode operation completed
2	Output buffer empty
3	Output buffer low-quarter (buffer less than 1/4-full)
4	Output buffer high-quarter (buffer 3/4-full)
5	Burst Trigger Ready
6	Load Ready (LOW-to-HIGH transition)
7	End Load Ready (HIGH-to-LOW transition of Load Ready)

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.6.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX™ PCI-9080 reference manual..

3.7 Remote Ground Sensing

Remote ground sensing is enabled when the REMOTE GROUND SENSE control bit in the BCR is HIGH, and is disabled when the control bit is LOW. Unless specific wiring provisions have been made to implement remote sensing, the remote sense control bit should be left in the default (LOW) disabled state.

3.8 Application Examples

Specific operating modes and procedures will vary widely according to the unique requirements of each application. The examples presented in this section (Table 3.8-1) illustrate several basic operating modes, and can be modified or combined for more complex operations.

References to *functions* in these examples generally apply to a single output channel, for simplicity of explanation. However, it must be remembered that each active channel represents an independent set of functional values and that all channels share a common sample clock.

Table 3.8-1. Summary of Operation Examples

Operation Example	Description
Sequential Direct Outputs	Each value written to the output data buffer appears immediately at the associated analog output channel.
Simultaneous Direct Outputs	Data values accumulate in the buffer until an entire channel group has been loaded. When the last channel is loaded, all active output channels update simultaneously.
Continuous Function	Identical to Simultaneous Direct Outputs, except: a. A clocking rate other than the maximum rate may be selected. b. The buffer is not allowed to become either empty or full.
Periodic Function	A single function is generated repeatedly in each active channel.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

Each of the examples in this section assumes that the initial operations listed in Table 3.8-2 have already been performed.

Table 3.8-2. Initial Operations

Operation	Default Value	Applicable Paragraph
The board has been reset or initialized.	---	3.3
The active channel group has been defined .	All channels active	3.4.1.1
The required output coding has been selected.	Offset binary	3.4.1.3.2
Active buffer size has been selected.	Maximum buffer size	3.4.2.2
Remote ground sensing has been selected or deselected.	Deselected	3.7

The remaining operational parameters are assumed to be in the following *default* states:

Buffer mode:	Open	Sample rate:	Maximum
Buffer status:	Empty	Sampling mode:	Sequential
Clock source:	Internal	Interrupt selected:	0 (Idle)
Clock status:	Disabled		

3.8.1 Sequential Direct Outputs

Table 3.8.1-1. Sequential Direct Outputs Example

Operation	PCI Bus Action	Board Response
Enable clocking	Set ENABLE CLOCK (D05) HIGH in the buffer operations register at location 0Ch.	Clocking is enabled at the maximum rate.
Load the output value for the first active channel.	Write the first value to the output data buffer at 18h.	Output value appears immediately at the analog output.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining active analog outputs are updated in ascending sequence.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	Each value written to the buffer is transferred immediately (within 2.5us) to the associated analog output

Notes:
1. End-of-frame (EOF) flags are ignored when operating in the open-buffer mode. Only D15..0 are active in the output buffer.
2. Data written to the buffer at rates above 400KSPS will accumulate in the buffer.
3. Access to an individual output channel is accomplished by first selecting the channel, and by then writing the output value to the buffer.

3.8.2 Simultaneous Direct Outputs

Table 3.8.2-1. Simultaneous Direct (Single Group) Outputs Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS (D07) HIGH in the board control register located at 00h.	Simultaneous clocking is enabled.
Enable clocking	Set ENABLE CLOCK (D05) HIGH in the buffer operations register located at 0Ch.	Clocking is enabled at the maximum rate.
Load the output value for the first active channel.	Write the first value to the output data buffer at 18h.	First value is retained in the buffer.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining values are accumulated in the buffer. When the last value is loaded, all values are extracted from the buffer and appear simultaneously at the associated output channels.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	All active channels are updated simultaneously when the last value in each group is written to the buffer.

Notes:
1. End-of-frame (EOF) flags are ignored when operating with in the open-buffer mode. Only D15..0 are active in the output buffer.
2. Data written to the buffer at rates above 4800KSPS will accumulate in the buffer.

3.8.3 Continuous Function

Table 3.8.3-1. Continuous Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS (D07) HIGH in the board control register located at 00h.	Simultaneous clocking is enabled.
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking will be used).	Write the required sample clocking rate to the sample rate control register at 08h.	The frequency of the internal rate generator is selected, if internal clocking is required.
Note: The following two operations may be performed simultaneously with a single write-transaction to the buffer operations register:	---	---
If external clocking is required, select external clocking.	To select external clocking, set EXTERNAL CLOCK (D04) HIGH in the buffer operations register at 0Ch.	External clocking is selected, if required.
Enable clocking	Set ENABLE CLOCK (D05) HIGH in the buffer operations register.	Clocking is enabled.
Select the buffer lo-quarter interrupt.	Set the INT[] bit field to 3 in the board control register.	The interrupt will respond when the buffer becomes less than 1/4 full.
Write an block of values to all active channels. Total block size should be between 1/4 and 3/4 of the buffer size. (Note 1). To avoid discontinuities in the output functions, the loading rate for channel groups must be greater than the sample (clocking) rate times the number of active channels. Maximum loading rate is 15MSPS during DMA transfers.	Write function values for all active channels to the output data buffer at 18h.	All active channels produce their respective output functions.
Wait for the lo-quarter interrupt. (Note 2).	Other, nonrelated activities can occur on the PCI bus until the lo-quarter interrupt request occurs.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		All output functions proceed continuously.

Notes:

1. The size of a data block must be at least 1/4 the size of the buffer to ensure that the lo-quarter interrupt will occur. Also, the block size must be no greater than 3/4 the size of the buffer to avoid data loss by forcing the buffer to full-status.
2. Response to the interrupt must be fast enough to prevent the buffer from going empty.

3.8.4 Periodic Function

Table 3.8.4-1. Periodic Function Example

Operation	PCI Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS (D07) HIGH in the board control register located at 00h.	Simultaneous clocking is enabled.
Load the first function value for each active channel.	Write the values for the first active group to the output data buffer at 18h.	Initial values for all active channels accumulate in the buffer.
Load the remaining function values for all active channels. Set the end-of-frame (EOF) flag.	Write all remaining function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	All function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking is required).	Write the required sample rate to the sample rate control register at 08h.	The frequency of the internal rate generator is selected if internal clocking is required.
Note: The remaining operations may be performed simultaneously with a single write-transaction to the buffer operations register:	---	---
Select the circular buffer mode.	Set CIRCULAR BUFFER (D08) HIGH in the buffer operations register at 0Ch.	The output buffer is closed (circular).
If external clocking is required, select external clocking.	To select external clocking, set EXTERNAL CLOCK (D04) HIGH in the buffer operations register.	External clocking is selected, if required.
Enable the sample clock.	Set ENABLE CLOCK (D05) HIGH in the buffer operations register.	Clocking is enabled. All active channels produce their respective functions repeatedly until the clock is disabled or the operating mode is changed. All outputs update simultaneously at the sample clock rate.

Notes:

1. To generate periodic functions simultaneously in multiple channels, all functions must be commensurate. That is, the functions in all channels must have frequencies that are exact integer multiples of the frequency of the lowest-frequency channel. Conversely, the period of the lowest-frequency channel must be an exact integer multiple of the period of each of the other channels.

3.8.5 Function Burst

Table 3.8.5-1. Function Burst Example

Operation	PCI Bus Action	Board Response
Clear the data buffer and disable clocking.	Set the CLEAR BUFFER bit (D11) and clear the ENABLE CLOCK bit (D05) in the buffer operations Register at 0Ch.	The buffer is cleared and clocking is disabled.
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS (D07) HIGH in the board control register located at 00h.	Simultaneous clocking is selected.
Load the first function value for each active channel.	Write the values for the first active group to the output data buffer at 18h.	Initial values for all active channels accumulate in the buffer.
Load the remaining function values for all active channels.	Write all remaining function values for all active channels to the output buffer.	All function values for all active channels accumulate in the buffer.
Set the end-of-frame (EOF) flag.	Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If more than one burst-function is required, repeat the previous operations for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
If the internal rate generator is to be used, select the sample rate.	Write the required sample rate to the sample rate control register at 08h.	The frequency of the internal rate generator is selected if internal clocking is required.
Select triggered-burst mode.	Set BURST ENABLED (D00) HIGH in the board control register at 00h.	The triggered-burst sampling mode is selected.
Prepare the buffer operations register for burst mode:	Write a single value to the buffer operations register at 0Ch:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER (D08) HIGH.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
If external clocking is required, select external clocking.	To select external clocking, set EXTERNAL CLOCK (D04) HIGH.	External clocking is selected, if required.
Enable the sample clock.	Set ENABLE CLOCK (D05) HIGH.	Clocking is enabled. The board is awaiting a burst trigger.
For software burst triggering, generate a software trigger to produce a single burst on all active output channels.	Set BURST TRIGGER (D02) HIGH in the board control register. (BURST TRIGGER is cleared automatically when the burst is completed).	All active output channels produce a single burst in response to a software trigger. (Use Interrupt-5 to detect the burst-ready condition).
For external burst triggering, no further bus activity is required.	---	All active output channels produce a single burst in response to each HIGH-to-LOW transition of TRIGGER INPUT at the I/O connector.

3.8.6 Function Concatenation

Table 3.8.6-1. Function Sequencing Example

Operation	PCI Bus Action	Board Response
Establish a periodic function as described in Paragraph 3.8.4. The following operations will replace the original ('old') function in each channel with a new function.	---	Each active output is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request access to the output data buffer.	Select the load-ready interrupt by setting INT[]=6 in the board control register at 00h. Set LOAD REQUEST (D09) HIGH in the buffer operations register at 0Ch.	The load-ready interrupt is selected. The board will assert the LOAD READY flag when the EOF flag in the original function occurs.
Wait for the buffer to open.	Wait for the load-ready interrupt request. Then clear D11..08 in the board control register.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. A load-ready interrupt request is generated. The buffer is now open, and the original functions are being flushed from the buffer.
Load the new function for each active channel into the buffer. Set the end-of-frame (EOF) flag.	Write the function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	New function values for all active channels reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group. The original functions are still active, and the remaining values are flushed from the buffer as they are sent to the output channels.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode when the last data value in the original function set moves out of the buffer. The new functions then commences seamlessly and circulate within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes. The End Load Ready interrupt condition can be used to detect completion of the flushing sequence.

3.9 DMA Operation

DMA transfers to the analog output FIFO buffer are supported with the board operating as bus master. Table 3.9-1 illustrates a typical PCI register configuration that would control a non-chaining, non-incrementing DMA transfer, in which a PCI interrupt is generated when the transfer has been completed. Bit 02 in the PCI Command register (04h) must be set HIGH to select the bus mastering mode. Refer to the PCI-9080 data manual for a detailed description of these registers.

Table 3.9-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status Register (A8h) should be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

3.10 Differential External Synchronization

An optional configuration provides a high frequency external clock signal that can be used for synchronizing sigma-delta analog input boards, such as the PMC-6SDI or PCI-16SDI, to a PMC-16AO12 board.

The clocking rate for a sigma-delta A/D converter usually is an integer multiple of the data sampling frequency. The integer multiplier, or *oversampling factor*, has a value of 64 for the PMC-6SDI and PCI-16SDI boards. An internal division by 2 (to ensure a 50 percent duty cycle) increases the effective oversampling factor to 128. For example, the maximum sample rate of 220KSPS for the PMC-6SDI requires an external clocking frequency of 28.16MHz.

The differential clocking option provides an adjustable clock source that is adjustable from 16MHz to 32MHz, with 0.2 percent resolution. The sigma delta boards divide the adjustable clock frequency to produce data sampling rates from 3.9KSPS to 250KSPS, with specified performance guaranteed from 5KSPS to 220KSPS.

Note: When operating in Initiator Mode, the adjustable clock replaces the 30MHz master clock used to determine the internal rate generator frequency described in Section 3.4.3. Consequently, the formula for the sample rate **Rs** shown in Section 3.4.3.1.2 becomes:

Rs (Hz) = Fclock / Nrate,

where Fclock is the frequency of the adjustable clock, in Hertz, and Nrate is a 16-bit integer in the Sample Rate control register.

Note: The adjustable clock is not initialized.

3.10.1 Adjustable Clock Frequency Control

The frequency of the adjustable clock is controlled by a 9-bit field D08:00 in the Adjustable Clock control register located at offset 0000 001Ch, as shown in Table 3.10.1-1. Control bit D09 selects the direction of the clock signal at the CLOCK I/O interface pins.

Table 3.10.1-1. Adjustable Clock Control Register

Offset: 0000 001Ch **Default: 0000 0000h**

REGISTER BITS	ACCESS MODE	DESIGNATION	DESCRIPTION
D[08:00]	R/W	CLOCK RATE (**Nclk**)	Controls the frequency of the adjustable clock. This field is not initialized.
D[09]	R/W	CLOCK INITIATOR	Configures the CLOCK IO pin as an input if LOW, or as an output if HIGH. Defaults LOW.
D[31:10]	RO	(Reserved, read-only)	(Reserved)

The frequency **Fclock** of the adjustable clock is controlled by the 9-bit value **Nclk** according to the relationship:

$$\mathbf{Fclock = 16 * (1 + Nclk / 511),}$$

where **Fclock** is in Megahertz, and **Nclk** is an integer with a value from zero to 511. For example, a value of 100 for **Nclk** would produce a clock frequency of 19.131MHz.

3.10.2 Initiator/Target Operation

Control bit D09 in the Adjustable Clock control register configures the board as a clock *initiator* if HIGH, or as a *target* board if LOW. When the board is configured as an initiator, the CLOCK I/O differential pair at the I/O connector provides a differential clock output signal at the frequency of the adjustable clock, and the clock output frequency replaces the master clock frequency of 30MHz referred to in Section 3.4.3.1.2. The CLOCK INITIATOR control bit initializes LOW, to target status.

In the target board configuration, the CLOCK I/O pair is an input clock that can be selected as the local output sampling clock by the EXTERNAL CLOCK control bit in the Buffer Operations Control register, as described in Section 3.4.3.

In *all* configurations, the CLOCK OUTPUT signal at the I/O connector is the analog output sampling clock for the board, and produces a single clock pulse each time the local outputs are updated.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PMC-16AO12 board contains twelve 16-bit D/A converters (DAC's), and all supporting functions necessary for adding precision high-speed analog output capability to a PMC host. As Figure 4.1-1 illustrates, a PCI interface adapter provides an interface between the controlling PCI bus and an internal local controller through a 16-bit local bus. A 17th local bit (not shown) provides a path for an end-of-frame (EOF) flag that is used for triggered-burst and other related buffer operations. The local controller performs all internal configuration and data manipulation functions, including autocalibration.

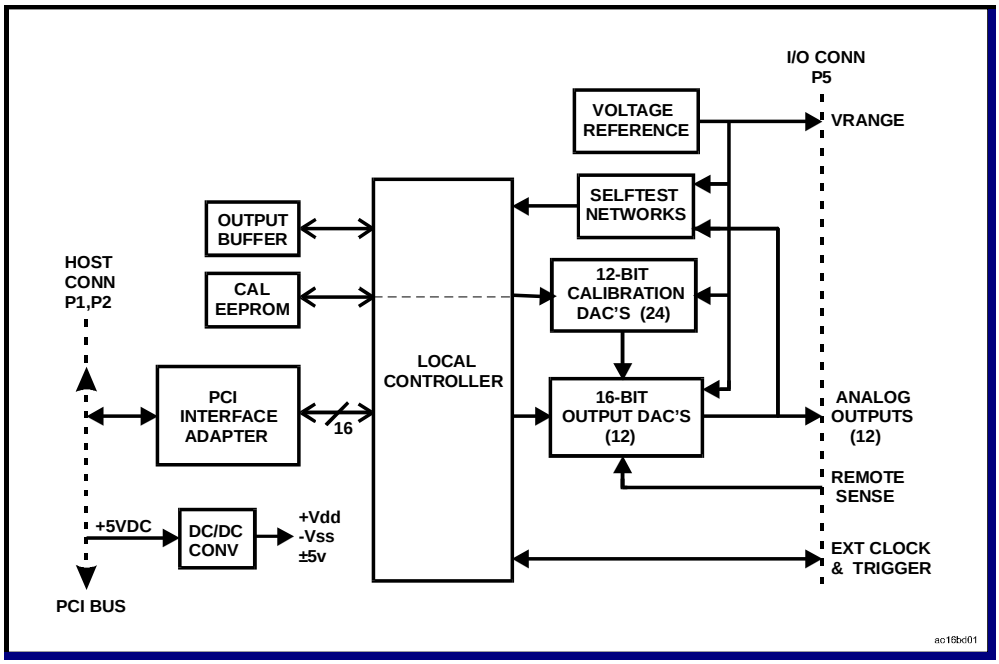


Figure 4.1-1. Functional Block Diagram

During normal operation, analog output data values are written from the PCI bus to an output buffer. The data values subsequently are serialized and transferred to the respective analog output DAC's. Each analog output channel consists of one 16-bit output DAC and two 12-bit calibration DAC's. Remote sensing of remote ground potentials is software selectable and affects all outputs simultaneously.

External control inputs and outputs accept burst-trigger and sample-clock inputs, and provide the digital signals necessary for multiboard synchronization.

Selftest networks allow the controller to compare the analog levels from all output channels against the internal voltage reference, and are used to establish the internal connections necessary during autocalibration. All channels are calibrated with respect to the single precision voltage reference.

The offset and gain corrections for each output channel are adjusted with a pair of 12-bit Calibration DAC's, the values for which are stored in nonvolatile electrically erasable programmable read-only memory (EEprom). The calibration EEprom and calibration DAC's provide the adjustment functions that otherwise would be associated with 24 trimpots in conventional analog configurations. Calibration control values are determined and stored in EEprom during autocalibration.

4.2 Analog Outputs

Each of the twelve analog output channels consists of a 16-bit output DAC and two 12-bit calibration DAC's. The local controller reads the 16-bit channel data value for each channel from the analog output buffer, and sends the value serially to the associated output DAC. The output DAC deserializes the data to obtain the original 16-bit data word, and holds that word in an internal buffer until commanded to transfer the data to the output register that drives the DAC output. All output registers are updated simultaneously if the controlling software has selected simultaneous sampling, or in ascending channel sequence if sequential sampling is selected.

The two calibration DAC's in each output channel provide offset and gain trimming of the associated 16-bit output DAC, using trim values that are determined during autocalibration.

4.3 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

An internal voltage reference is adjusted during the calibration procedure described in Section 2 to equal approximately 99.9 percent of the output voltage range. This voltage reference is compared with actual channel output values to calibrate the gain of each analog output channel. Calibration values for channels offsets are determined by comparing channel outputs with the potential on the internal analog ground bus.

Each of the 24 calibration DAC's is adjusted in a successive approximation sequence that commences with the DAC in an all-zero state. The most significant bit initially is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response, the bit either is cleared or is left in the "1" state. The next lower significant bit is then tested in the same manner, and this process continues until all 12 bits have been tested and adjusted. The final value in the calibration DAC is stored in the nonvolatile calibration EEprom for subsequent retrieval by the local controller during initialization.

4.4 Power Control

Regulated supply voltages of ±5 Volts and ±13 Volts are required by the analog networks, and are derived from the +5-Volt input from the PCI bus through a DC/DC converter. To obtain optimum performance from the internal supplies, all analog power voltages are produced by series regulation.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes all local registers and principal control-bit fields that appear in Section 3.

Table 3.1-1. Control and Data Registers

OFFSET	REGISTER	ACCESS MODE*	ACTIVE BITS	PRIMARY FUNCTION
00	BOARD CONTROL (BCR)	R/W	16	Board Control Register (BCR)
04	CHANNEL SELECTION	R/W	12	Channel-enabling
08	SAMPLE RATE	R/W	16	Analog output clocking rate selection
0C	BUFFER OPERATIONS	R/W	16	Buffer size selection and status flags
10	(Reserved)	---	---	---
14	(Reserved)	---	---	---
18	OUTPUT DATA BUFFER	WO	17	Analog output FIFO buffer
1C	ADJUSTABLE CLOCK	R/W	10	Control of the adjustable clock (Optional)

* Access mode is D32. R/W = Read/Write; WO = Write-only

Offset: 0000h **Table 3.2-1. Board Control Register** **Default: 0810h**

BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	BURST ENABLED	0	Selects burst-mode if HIGH, continuous-mode if LOW. Default is LOW; i.e. continuous-mode.
D01	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that a burst is in progress, and that a trigger will not be accepted. Available as an interrupt condition.
D02	R/W	*BURST TRIGGER	0	Software burst trigger, asserted HIGH. Active only when BURST ENABLED control bit is asserted. Initialized LOW.
D03	R/W	REMOTE GROUND SENSE	0	Correction is made for remote ground potentials when this bit is HIGH.
D04	R/W	OFFSET BINARY	1	Selects offset-binary data format when asserted HIGH, or two's complement when LOW.
D05	R/W	(Reserved)	0	
D06	R/W	(Reserved)	0	
D07	R/W	SIMULTANEOUS OUTPUTS	0	When HIGH, selects simultaneous output clocking. When LOW, selects sequential clocking. Default is LOW; i.e.: sequential clocking.
D08	R/W	INTERRUPT A0	0	Interrupt source selection.
D09	R/W	INTERRUPT A1	0	
D10	R/W	INTERRUPT A2	0	
D11	R/W	INTERRUPT REQUEST FLAG	1	Set HIGH when the board asserts an interrupt request. Clears the request when cleared LOW by the bus.
D12	R/W	*CM0	0	Calibration mode. Defaults to normal operation.
D13	R/W	*CM1	0	Completion available as an interrupt condition.
D14	RO	BIT STATUS FLAG	0	Records the status of autocalibration; LOW for pass, HIGH for fail. Initializes LOW.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets all defaults for all registers.

Table 3.4.1-1. Channel Selection Register

Offset: 0004h **Default: 0FFFh**

BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	CHANNEL 00 ENABLED	Channel-Enable mask. A channel is enabled if the associated mask bit is HIGH, or is disabled if the bit is LOW. May be truncated for 8-channel and 4-channel boards.
D01	R/W	CHANNEL 01 ENABLED	
D02	R/W	CHANNEL 02 ENABLED	
D03	R/W	CHANNEL 03 ENABLED	
D04	R/W	CHANNEL 04 ENABLED *	
D05	R/W	CHANNEL 05 ENABLED *	
D06	R/W	CHANNEL 06 ENABLED *	
D07	R/W	CHANNEL 07 ENABLED *	
D08	R/W	CHANNEL 08 ENABLED **	
D09	R/W	CHANNEL 09 ENABLED **	
D10	R/W	CHANNEL 10 ENABLED **	
D11	R/W	CHANNEL 11 ENABLED **	
D12	---	(Reserved)	---
D13	---	(Reserved)	---
D14	---	(Reserved)	---
D15	---	(Reserved)	---

R/W = Read/Write. * 8-Channel and 12-Channel boards only. ** 12-Channel boards only.

Table 3.4.1-2. Output Data Buffer

Offset: 0018h **Default: N/A (Write-Only)**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	WO	**DATA 00**	Least significant data bit
D01-D14	WO	**DATA 01 - DATA 14**	Intermediate data bits
D15	WO	**DATA 15**	Most significant data bit
D16	WO	**EOF FLAG**	End-of-frame (EOF) flag.
D17-D31	WO	**---**	(Inactive)

* WO indicates write-only access. Read-access produces all-zero value.

Table 3.4.2-1. Buffer Operations Register

Offset: 000Ch **Default: 340Dh**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	SIZE0	1	Size-selection bit field for the active buffer.
D01	R/W	SIZE1	0	Defaults to Dh (32K Samples).
D02	R/W	SIZE2	1	
D03	R/W	SIZE3	1	
D04	R/W	EXTERNAL CLOCK	0	Selects hardware or software clock source when HIGH, or the internal rate generator when LOW. Default is LOW (internal rate generator).
D05	R/W	ENABLE CLOCK	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).
D06	RO	CLOCK READY	0	If external clocking is selected, indicates when HIGH that a hardware or software clock will be accepted. If LOW, indicates that the output is not ready to accept a clock. Active only when external clocking is selected.
D07	R/W	*SW CLOCK	0	If external clocking is selected, produces a single output clock event when asserted. Clears LOW automatically when the clock event is completed. Active only when external clocking is selected.
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.
D09	R/W	*LOAD REQUEST	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.
D10	RO	LOAD READY	1	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available as an interrupt condition. Defaults HIGH.
D11	R/W	*CLEAR BUFFER	0	Resets the buffer to empty.
D12	R/W	BUFFER EMPTY	1	Status flags for the active buffer. Empty, lo-quarter and
D13	RO	BUFFER LOW QUARTER	1	hi-quarter flags are available as conditions for an interrupt
D14	RO	BUFFER HIGH QUARTER	0	request.
D15	RO	BUFFER FULL	0	

R/W = Read/Write, RO = Read-only. * Clears LOW automatically when operation is completed.

Table 3.4.2-2. Active Buffer Size

SIZE[3:0]	BUFFER SIZE (Total Channel Values)	SIZE[3:0]	BUFFER SIZE (Total Channel Values)
0	4	8	1024
1	8	9	2048
2	16	A	4096
3	32	B	8192
4	64	C	16384
5	128	D	32768
6	256	E	*65536
7	512	F	**131072

* With 64K-Sample buffer option, or ** with 128K-Sample buffer option.

Table 3.4.3-1. Sample Rate Control Register

Offset: 0008h **Default: 004Bh**

DATA BIT	MODE	DESIGNATION	DESCRIPTION
D00	R/W	**RATE00**	Least significant rate bit
D01-D14	R/W	**RATE01 - RATE14**	Intermediate rate bits
D15	R/W	**RATE15**	Most significant rate bit
D16-D31	*R/W	**---**	(Inactive)

* Active in write-mode only. Read-access retrieves all-zero.

Table 3.4.3-2. Sample Rate Selection

Nrate (RATE[15..0])		SAMPLE RATE Rs *
(Dec)	(Hex)	(Samples per Second)
75	004B	400,000
76	004C	394,747
77	004D	389,610
---	---	Rs (Hz) = 30,000,000 / Nrate
---	---	
---	---	
65534	FFFE	457.78
65535	FFFF	457.77

* ±0.015 percent.

Table 3.5-1. Calibration Mode Selection

BCR Bits D13..12 **Default: 0h**

CM[1:0]	FUNCTION
0	Normal operation. No calibration activity. Default state.
1	(Reserved).
2	Invoke Autocalibration
3	(Reserved)

Table 3.6.1-1. Interrupt Source Selection

BCR Bits D10..D08 **Default: 0h**

INTERRUPT A[2:0]	INTERRUPT CONDITION
0	Idle. Interrupt disabled unless initializing. Default state.
1	Calibration-mode operation completed
2	Output buffer empty
3	Output buffer low-quarter (buffer less than 1/4-full)
4	Output buffer high-quarter (buffer 3/4-full)
5	Burst Trigger Ready
6	Load Ready (LOW-to-HIGH transition)
7	End Load Ready (HIGH-to-LOW transition of Load Ready)

Table 3.9-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3.10.1-1. Adjustable Clock Control Register

Offset: 0000 001Ch **Default: 0000 0000h**

REGISTER BITS	ACCESS MODE	DESIGNATION	DESCRIPTION
D[08:00]	R/W	CLOCK RATE (**Nclk**)	Controls the frequency of the adjustable clock. This field is not initialized.
D[09]	R/W	CLOCK INITIATOR	Configures the CLOCK IO pin as an input if LOW, or as an output if HIGH. Defaults LOW.
D[31:10]	RO	(Reserved, read-only)	(Reserved)

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