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High Performance Bus Interface Solutions

Rev: 082718

PMC66-16AISS2AO2A2M

4-Channel 16-Bit PMC Analog Input/Output Board

With Two Simultaneously-Sampled Inputs at 2.0 MSPS per Channel,
Two Analog Outputs at 2.0 MSPS per Channel,
And 8-Bit Buffered Digital Output Port

REFERENCE MANUAL

---- PRELIMINARY ----

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SECTION 1.0

INTRODUCTION

The single-width PCI mezzanine card PMC66-16AISS2AO2A2M provides 16-bit analog input and output capability for PMC applications. Two analog input channels (Figure 1.1-1) are digitized simultaneously at rates up to 2,000,000 conversions per second per channel, with software-controlled voltage ranges of ±10V, ±5V or ±2.5V. Digitized input data is buffered through a 2Megasample FIFO.

Two 16-bit analog output channels provide software-selected output ranges of ±10V, ±5V or ±2.5V, and are accessed either directly through dedicated control registers, or through a 2 Megasample FIFO buffer. The analog output buffer can be clocked at rates up to 2,000,000 output samples per second per channel.

A Digital output port provides 8 TTL output lines through a 256Kx8 FIFO buffer, and an 8-bit bidirectional port provides eight direct-accessed TTL lines.

The board is designed for minimum off-line maintenance. All functional parameters are under software control, thereby eliminating field-configuration jumpers. A selftest switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host.

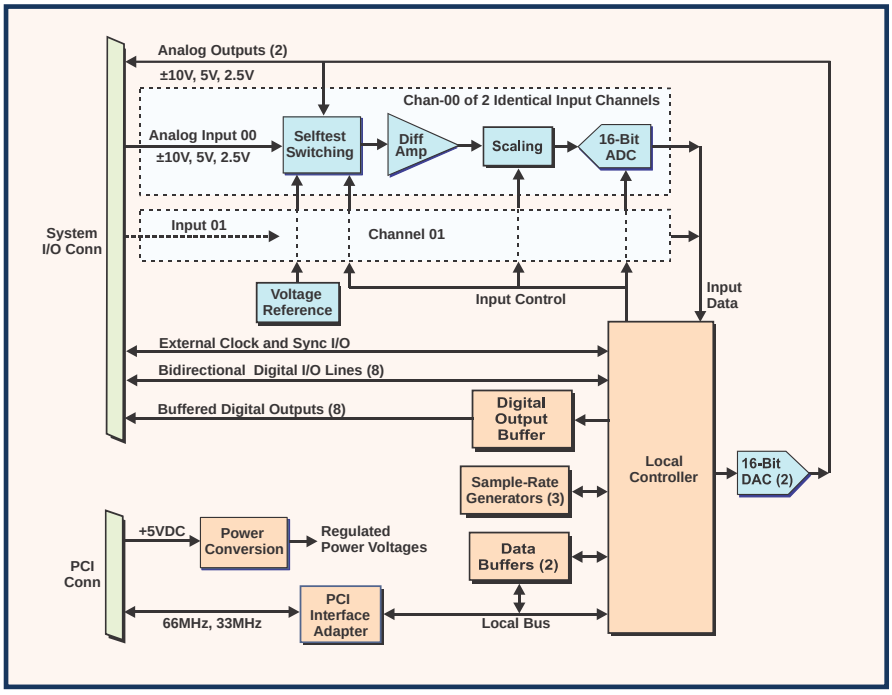


Figure 1.1-1. Functional Organization

This product is compatible with the IEEE PCI local bus specification Revision 2.3. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector, and +5VDC supplied by the PCI bus is converted to analog power voltages. Universal signaling is supported, and all operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional convection cooling.

SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel (Figure 2.2-1). Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the standoffs are seated against the host board.

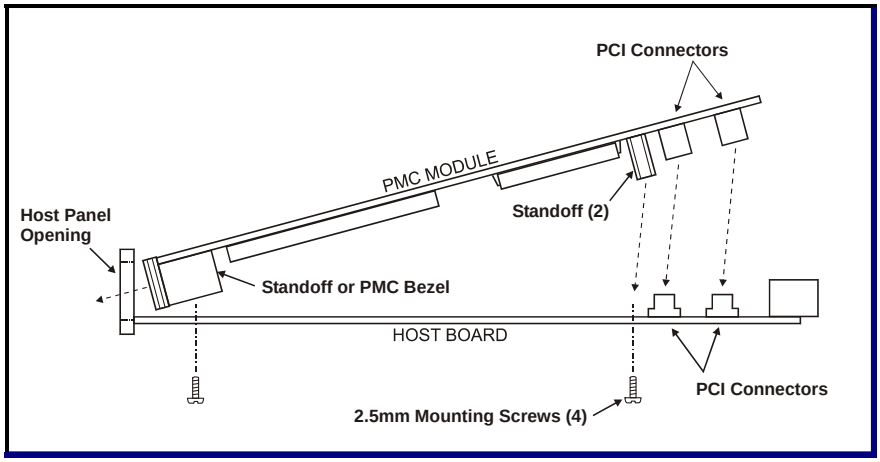


Figure 2.2-1: PMC Physical Installation

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

Standard system cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with an 80-pin dual-ribbon connector, equivalent to Robinson Nugent #P50E-080S-TG. The Robinson Nugent insulation displacement connector accepts two 40-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-2. Contact the factory if preassembled cables are required.

Table 2.2-1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	OUTPUT RTN
2	ANA OUT 00
3	OUTPUT RTN
4	ANA OUT 01
5	OUTPUT RTN
6	INPUT RTN
7	INPUT RTN
8	INPUT RTN
9	INP00 LO
10	INP00 HI
11	INPUT RTN
12	INPUT RTN
13	INP01 LO
14	INP01 HI
15	INPUT RTN
16	INPUT RTN
17	VTEST RTN
18	VTEST
19	INPUT RTN
20	INPUT RTN
21	DIGITAL RTN
22	DIG OUT 00 *
23	DIGITAL RTN
24	DIG OUT 01 *
25	DIGITAL RTN
26	DIG OUT 02 *
27	DIGITAL RTN
28	DIG OUT 03 *
29	DIGITAL RTN
30	DIG OUT 04 *
31	DIGITAL RTN
32	DIG OUT 05 *
33	DIGITAL RTN
34	DIG OUT 06 *
35	DIGITAL RTN
36	DIG OUT 07 *
37	DIGITAL RTN
38	DIG OUT CLK INP *
39	DIGITAL RTN
40	DIGITAL RTN

ROW-B	
PIN	SIGNAL
1	INPUT RTN
2	INPUT RTN
3	INPUT RTN
4	INPUT RTN
5	INPUT RTN
6	INPUT RTN
7	INPUT RTN
8	INPUT RTN
9	INPUT RTN
10	INPUT RTN
11	INPUT RTN
12	INPUT RTN
13	INPUT RTN
14	INPUT RTN
15	INPUT RTN
16	INPUT RTN
17	INPUT RTN
18	INPUT RTN
19	DIGITAL RTN
20	DIO 00 **
21	DIGITAL RTN
22	DIO 01 **
23	DIGITAL RTN
24	DIO 02 **
25	DIGITAL RTN
26	DIO 03 **
27	DIGITAL RTN
28	DIO 04 **
29	DIGITAL RTN
30	DIO 05 **
31	DIGITAL RTN
32	DIO 06 **
33	DIGITAL RTN
34	DIO 07 **
35	DIGITAL RTN
36	OUTPUT CLK I/O
37	DIGITAL RTN
38	TRIGGER I/O
39	DIGITAL RTN
40	INPUT CLK I/O

* Buffered digital output port.

** Bidirectional digital I/O port.

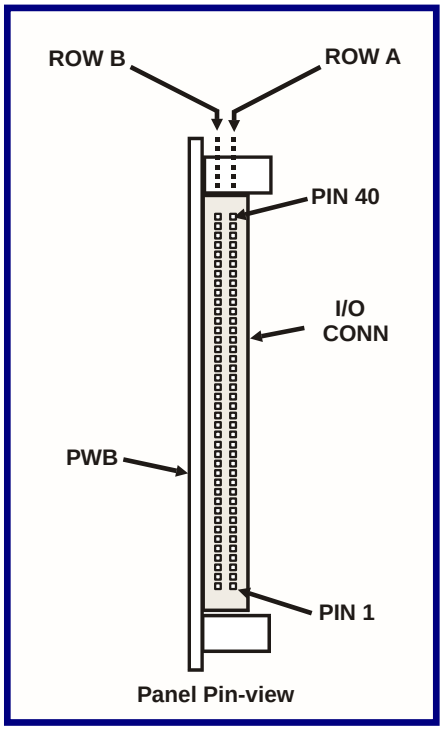


Figure 2.2-2. System I/O Connector

2.3 System Configuration

2.3.1 Analog Inputs

The two analog input channels can be configured for either differential or single-ended operation. The hardware input configuration must be acknowledged by the control software.

2.3.1.1 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other or have returns that are at significantly different potentials. A potential difference between grounds is significant if it is larger than the maximum tolerable measurement error.

This operating mode also offers the highest rejection of the common mode noise, which is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode, shown in Figure 2.3-1a, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a ground point which ensures that the sum of the signal level **(Vsig)** and the common mode voltage **(Vcm)** remains within the range specified for the board. Ground current through the INPUT RTN pins must be limited in order to avoid damage to the cable or the input board.

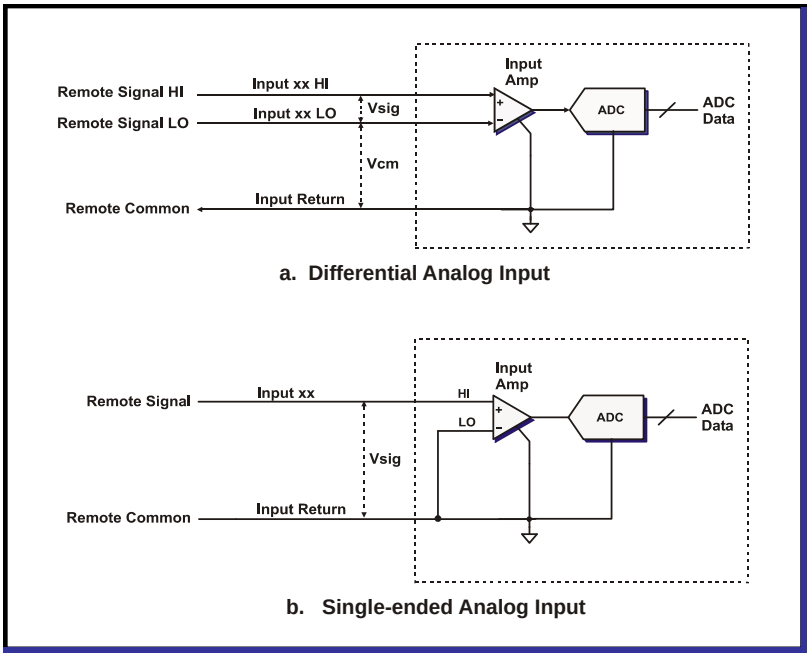


Figure 2.3-1. Analog Input Configurations

2.3.1.2 Single-Ended Inputs

Single-ended operation (Figure 2.3-1b) generally provides acceptable performance only when the input signal sources either are isolated from each other, or are common to a single isolated signal return. A single-ended configuration usually is more susceptible to system interference than a differential configuration.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or could generate potentially destructive ground current.

For applications in which multiple signal sources share a single ground, the differential configuration is recommended, with all "LO" inputs connected together at the common remote return.

2.3.2 Analog Outputs

2.3.2.1 Output Configurations

The two analog output channels are single-ended and have a common signal return that is referred to in Table 2.2-1 as OUTPUT RTN. Single-ended outputs should drive only loads that have high impedances to system ground. The best results are obtained when the loads are isolated also from each other.

Figure 2.3-2 shows the primary sources of error in both isolated and nonisolated system configurations. For loads that are isolated from each other (Figure 2.3-2a), the total line-loss error is twice the loss produced in a single line, assuming equal wire size and length for output and return lines. For loads with a common return that is isolated from system ground, line loss in the common return appears as crosstalk between channels.

If the load return is connected to a remote system ground (Figure 2.3-2b), the potential difference **Vgnd** between the remote ground and the internal signal return will introduce an error into the signal delivered to the load. The ground current **Ignd** developed in the return line is limited essentially only by **Rgnd**, and can damage the cable or the board if not controlled.

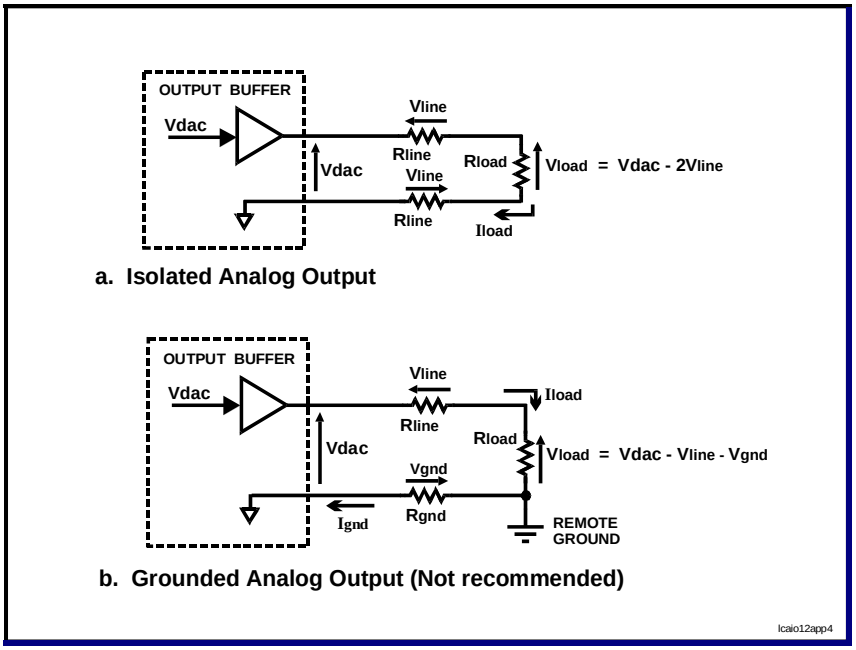


Figure 2.3-2. Output Configurations

2.3.2.2 Loading Considerations

The voltage drop in the system I/O cable can be a significant source of error, especially with relatively long cables driving moderate or heavy loads. Figure 2.3-3 shows the effect of load current on the voltage drop in copper wire of various sizes. A 4.0 milliamp load for example, inserts a voltage drop of more than 0.25 millivolt *per foot* in #28 AWG ribbon cable; twice that if the return line also is considered. Several feet of ribbon cable therefore can produce significant errors, especially in a 16-bit system, in which 1 LSB can represent only 76 microvolts on a ±2.5 Volt range. High impedance loads generally do not produce significant DC errors.

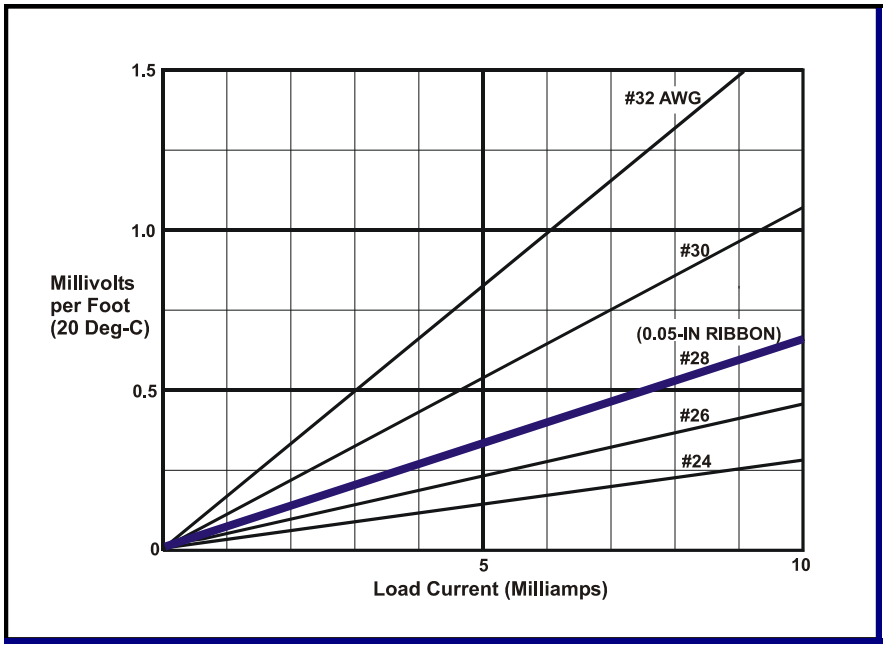


Figure 2.3-3. Line Loss versus Load Current

2.3.3 External Sync I/O

The INPUT CLK I/O and OUTPUT CLK I/O pins in the system connector are bidirectional TTL synchronization signals that provide external control of analog input sampling and analog output clocking, respectively. The TRIGGER I/O pin also is bidirectional, and is shared by the analog inputs and outputs. Specific input/output configurations are determined by individual system requirements, and must be acknowledged by the control software.

When a board is software-configured as an ***Initiator***, these I/O signals are outputs that can be used to control multiple *Target* boards. Each clock or trigger event output consists of a 70-100 nanosecond TTL pulse, asserted LOW. Output loading in the Initiator configuration should be limited to 8 milliamps or less. The analog inputs, analog outputs and triggering all can be configured independently as either initiators or targets.

For ***Target*** boards, the I/O signals become inputs and can synchronize input and output operations to an Initiator board. Clock and trigger inputs are edge-detected on the negative (falling) edge, and must be asserted for at least 60 nanoseconds in order to be acknowledged. All three inputs are asserted LOW, and are pulled up internally to +3.3V through approximately 33 KOhms.

2.3.4 Multiboard Synchronization

If multiple boards are to be synchronized together, the INPUT CLK I/O, TRIGGER I/O and OUTPUT CLK I/O pins from one board, the ***initiator***, are connected to the corresponding pins of as many as four ***target*** boards in the same backplane (Figure 2.3-4). The controlling software determines specific synchronization functions.

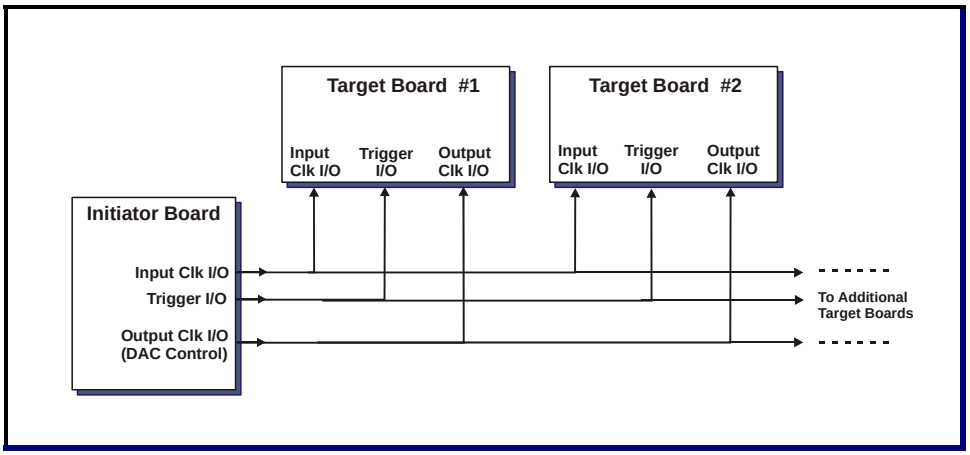


Figure 2.3-4. Multiboard Synchronization

2.4 Digital I/O Ports

2.4.1 Bidirectional Digital I/O Port.

Eight bidirectional digital I/O lines provide Register-Direct TTL signaling through DIO 00 to DIO 07. These eight lines can be software-configured as either all inputs or all outputs, and are controlled through a single register. When configured as outputs, the DIO lines can source or sink up to 10mA. When configured as inputs the eight lines are pulled up to +3.3V through 33K.

2.4.2 Buffered Digital Output Port.

Eight TTL output lines DIGITAL OUT 00 through DIGITAL OUT 07 I/O are driven by a 256Kx8-Bit FIFO buffer, and support pattern generation and byte-wide digital streaming. The buffer is loaded by the host through a single register, and can be clocked either internally or from an external source (DIG OUT-CLK-INP). Each output can source or sink up to 10mA.

2.5 Maintenance

This product requires no scheduled maintenance other than periodic verification and possible adjustment of the internal voltage reference. The optimum verification interval will vary with upon the specific application, but in most instances an interval of one year should be sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that has been determined to be defective should be returned to the factory for detailed problem analysis and repair.

2.6 Reference Verification

All analog channels are software-calibrated to a single internal voltage reference by an embedded autocalibration utility. The procedure presented here describes the verification and adjustment of the reference.

2.6.1 Equipment Required

Table 2.6-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.6-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts. Input impedance 10 Megohms or greater.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to the system I/O connector.	---	---

2.6.2 Verification and Adjustment

The following procedure describes the verification of the internal voltage reference. Adjustment of the internal reference, if necessary, is performed with an internal trimmer that is accessible as shown in Figure 2.5-1.

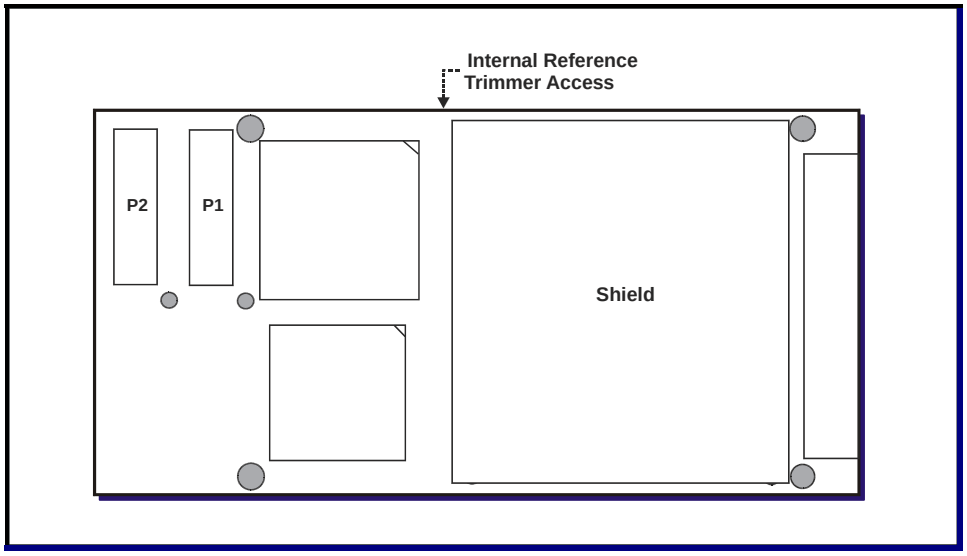


Figure 2.6-1. Reference Adjustment Access

This procedure assumes that the PMC is installed on a host board, and that the host is installed in a system.

1. Connect the digital multimeter between the VTEST pin (+), and the VTEST RTN pin (-) in the System I/O connector.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Verify that the digital multimeter indication is +9.9000 VDC ±0.0015 VDC. If the indication is not within this range, adjust the internal reference trimmer for an in-range digital multimeter indication.
4. Verification and adjustment is completed. Remove all test connections.

SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC66-16AISS2AO2A2M is compatible with the PCI Local Bus specification Revision 2.3, and a PLX™ PCI-9056 adapter controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 32-longword boundary in memory space. After initialization is completed, communication between the PCI bus and the local bus takes place through the control and data registers listed in Table 3.1-1. All data transfers are long-word D32. DMA access is supported for data transfers from the analog input buffer and to the analog output data buffers. To ensure compatibility with subsequent controller revisions, reserved control bits should be written LOW (zero), and maintenance registers should not be modified.

Table 3.1-1. Control and Status Registers

Offset (Hex)	Register	Mode	Default	Primary Function	Ref
0000	BOARD CONTROL	RW	2202 00A0h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	0000 00XXh	8-Bit Bidirectional Digital I/O port	3.9
0008	ANALOG OUTPUT CHAN 00	RW	0000 8000h	Output Channel 00 data.	3.12
000C	ANALOG OUTPUT CHAN 01	RW	0000 8000h	Output Channel 01 data.	
0010-0014	(Reserved)	RO	0000 0000h	---	---
0018	ANALOG INPUT BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0000 007Eh	Rate-A generator divider; 24 bits.	3.7
0020	RATE GENERATOR B	RW	0000 2760h	Rate-B generator divider; 24 bits.	
0024	INPUT CONFIGURATION	RW	0300 0400h	Analog inputs channel-mask and burst-size.	3.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the input buffer.	3.4.5.2
002C	INPUT BUFFER THRESHOLD	RW	001F FFFEh	Input buffer status flag threshold.	
0030	PRIMARY STATUS	RW	0000 0X00h	Principal status-flag register	3.11
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.16
0038	Autocal Values [2]	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1043h	Buffered Analog Outputs Control	3.13.2.3
0040	OUTPUT BUFFER THRESHOLD	RW	001F FFFEh	Output buffer status flag threshold.	
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.13.2
004C	RATE GENERATOR C	RW	0000 007Eh	Rate-C generator divider; 24 bits.	3.13.4.1.2
0050	BDO BUFFER SIZE	RO	0000 0000h	Buffered Digital Outputs (BDO) Size (Number of bytes)	3.19
0054	BDO BUFFER CONTROL	RW	0001 FFFEh	BDO buffer controls and threshold	
0058	BDO OUTPUT BUFFER	WO	0000 0000h	BDO FIFO buffer.	
005C	BDO BUFFER RATE GENERATOR	RW	0000 0D20h	BDO clocking rate generator.	
0060	ANCILLARY CONTROL REGISTER	R/W	0000 0000h	Isolates clock and sync I/O lines.	3.18
0064-007C	(Reserved)	---	---	---	---

Notes: 1. RW = Read/Write, RO = Read-Only, WO = Write-Only.
2. Maintenance register; Shown for reference only.

3.2 Board Control Register (BCR)

Basic board functions such as initialization, autocalibration and input/output range selection are controlled through the board control register (BCR) shown in Table 3.2-1. Specific control bits are cleared automatically after the associated operations have been completed. Read-only status flags indicate the states of specific operational functions.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY'**s. Configuration operations are executed in the sequence shown in Table 3.3-1. Loading of the PCI configuration registers is completed within 3 milliseconds after the assertion of a PCI bus reset.

3.3.2 Initialization

Internal control logic can be initialized without invoking a full reconfiguration by setting the INITIALIZE control bit HIGH in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all register defaults are invoked. (Paragraph 3.3).
- Analog input and output data coding is offset binary. (3.6).
- All analog input and output channels are active. (3.4.2, 3.13.1.1.1).
- Analog input and output ranges are ±10V. (3.4.3, 3.13.1.3).
- External clock and trigger signals are in the target (Input) mode. (3.8, 3.13.6).
- The input and output buffers are reset to empty. (3.4.5.1, 3.13.2.3).
- Analog Inputs:
  - Input channels are differential. (3.4.1.1).
  - Sample clocking is from the Rate-A generator; Bursting is disabled. (3.4.4.2, 3.7).
  - The ADC (Rate-A) generator is adjusted to 320 kHz, and is disabled. (3.7),
  - The analog input buffer is reset to empty; buffer threshold is 3FFFEh. (3.4.5).
  - Burst block size is 1024 (0400h). (3.4.4.2).
- Analog Outputs:
  - Analog outputs are at midrange (zero), and are disconnected (3.6, 3.12.1.1).
  - Direct-Register access is selected. (3.12).
  - The DAC (Rate-C) generator is adjusted to 320 kHz, and is disabled. (3.13.4.1.2).
- The burst-trigger (Rate-B) generator is adjusted to 4 kHz, and is disabled. (3.7)
- The bidirectional Digital I/O port is configured as one input byte. (3.9).
- The Buffered Digital Output (BDO) buffer is cleared and disabled. (3.19)
- The BDO Rate generator is adjusted to 12 kHz, and is disabled. (3.19)

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2202 00A0h**

Bit	Mode [1]	Designation	Def	Description	Ref
D00-D02	RW	ANALOG INPUT MODE	0	Analog input mode: 0 => Differential system inputs 1 => Single-ended system inputs 2 => Zero selftest 3 => VREF selftest 4 => Output Channel 00 5 => Output Channel 01 6 => Output Channel 02 7 => Output Channel 03	3.4.1
D03	RW	ANALOG INPUTS AUTOCAL [2]	0	Initiates an analog-inputs autocalibration operation.	3.10
D04-D05	RW	INPUT CHANNEL 00 RANGE	2	Analog Input Channel-00 Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.4.3
D06-D07	RW	INPUT CHANNEL 01 RANGE	2	Analog Input Channel-01 Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16-D17	RW	OUTPUT RANGE	2	Analog Output Voltage Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.12.1 3.13.1.3
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, data is clocked to the outputs one channel at a time. Affects only buffered outputs.	3.12.2.2 3.13.4.2
D19	RW	ENABLE BUFFERED OUTPUTS	0	When HIGH, enables the analog output FIFO buffer, and disables the analog output registers ANALOG OUTPUT CHAN xx.	3.13
D20	RW	OUTPUT S/W CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.13.4.1
D21	RW	TRIGGER INITIATOR	0	Configures the shared analog input/output hardware trigger pin as an output if HIGH, or as an input if LOW.	3.4.4.2
D22	R/W	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.13.4.1.2
D23	R/W	INPUT BUFFER UNDERFLOW	0	Set HIGH if the input buffer underflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D24	RW	ANALOG INPUT CLK INITIATOR	0	Configures the analog input I/O clock as an *output* if HIGH, or as an *input* if LOW.	3.4.4
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.6
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog inputs.	3.7
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for triggered bursts.	
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.10
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	
D30	R/W	SWAP DEMAND MODE CHANNELS	0	Reverses the default demand-mode DMA channels for analog inputs and outputs	3.5 3.15
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

3.4 Analog Inputs

Each of two analog input channels can be digitized simultaneously with 16-bit resolution at rates from DC to 2 Megasamples per second. Data from any combination of inputs can be acquired in a 2 Megasample buffer, and a tag-bit is attached to the first (lowest-numbered) active channel data values. Three voltage ranges are available, and any two of these ranges can be used simultaneously on different channels. Each input channel contains a dedicated 16-Bit ADC.

All active inputs are sampled simultaneously, and the sample clock can be derived: (a) from an internal rate generator, (b) from an external hardware clock input, or (c) directly from the bus.

To illustrate the requirements for initiating analog input acquisition directly after board initialization, setting the following control bits HIGH simultaneously in the BCR would start two-channel acquisition using the Rate-A generator at the default sample rate:

- ANALOG INPUT CLK INITIATOR; Selects the analog input clock initiator mode,
- ENABLE INPUT BUFFER; Enables the analog input buffer,
- ENABLE RATE-A GENERATOR: Enables the Rate-A generator.

3.4.1 Input Modes

An input switching network routes either the system input signals or internal test signals through the input channels, and is controlled by the ANALOG INPUT MODE control field in the BCR. The system inputs are disconnected when internal signals are monitored, and have no effect on test results.

3.4.1.1 System Inputs

Of the eight possible input modes available through the ANALOG INPUT MODE field, two are dedicated to system inputs. In the differential configuration, the signal present between the HI and LO inputs in each channel is acquired. For a single-ended input, the input signal is measured between the HI input and the input return, and the LO input is ignored. The selected system input configuration must agree with the system wiring configuration (Paragraph 2.3).

3.4.1.2 Test Modes

Internal analog nodes can be monitored to verify the functional integrity of the board. The selected input ranges apply in all input modes, including test modes. The following signals are present in *all input channels* when the indicated test modes are selected:

Zero Selftest: Midscale value, ideally equal to 0.000 VDC,

VREF Selftest: Internal voltage reference, ideally equal to +99.00 percent of the ***selected analog output range*** *,

Output Channels: Either of the two analog output channels.

* The VREF Selftest source and the Output DAC's share a common reference.

3.4.2 Active Channel Selection

Input channels are designated as active by setting the corresponding ENABLE CHANNEL XX control bit HIGH in the Input Configuration register (Table 3.4-1), or as inactive by clearing the bit LOW. Both active inputs are sampled simultaneously when a sample clock occurs. Inactive channels produce no data in the input buffer.

Table 3.4-1. Input Configuration Register

Offset: 0024h **Default: 0300 0400h**

Bit	Mode	Designation	Def	Description
D00-D23	RW	BURST BLOCK SIZE	0400h	Number of active channel sets acquired during a triggered burst.
D24	RW	ENABLE INPUT 00	1	Analog input channel selection mask.
D25	RW	ENABLE INPUT 01	1	
D26-D31	RW	(Reserved)	0	

* RW = Read/Write, RO = Read-Only.

3.4.3 Input Ranges

Input voltage ranges of ±10V, ±5V and ±2.5V are assigned independently to the two input channels by the INPUT CHANNEL 00 RANGE and INPUT CHANNEL 01 RANGE control fields in the BCR:

Note: Voltage levels outside the selected ranges will produce saturation codes of plus or minus fullscale, but will not damage the inputs if they are within the range indicated in the product specification for overvoltage protection.

3.4.4 Sampling Modes

All active channels are sampled at each occurrence of the analog input sample clock. If the ANALOG INPUT CLK INITIATOR control bit is HIGH in the BCR, input sample clocks are supplied by either the Rate-A generator or by the INPUT S/W CLOCK control bit in the BCR. The INPUT S/W CLOCK control bit always produces an input clock, regardless of the state of the Rate-A generator or the INITIATOR control bit. In the ***Initiator*** mode, each sample clock produces a 100 nanosecond LOW output pulse at the bidirectional INPUT CLK I/O pin in the system I/O connector.

If the INITIATOR control bit is LOW, designating the board as a ***Target***, the INPUT CLK I/O pin becomes an input, and a sample clock is generated for each HIGH-to-LOW transition received at the pin. The Rate-A generator is ignored in the target clocking mode.

To avoid contention among multiple boards interconnected for multiboard synchronous operation, the INITIATOR control but defaults LOW for target mode.

3.4.4.1 Continuous

During continuous sampling, all active input channels are sampled continuously as long as a clock source is present. Continuous sampling is selected when the ENABLE INPUT BURST control bit is LOW in the BCR.

3.4.4.2 Burst Sampling

If burst sampling is enabled by setting the ENABLE INPUT BURST control bit HIGH in the BCR, an input trigger initiates the acquisition of a specific number of samples for each active channel. During a burst, sampling proceeds at the selected input sample rate until the specified number of samples has been acquired, and then terminates until a subsequent trigger occurs. The number of samples acquired during a triggered burst is specified by the 24-Bit BURST BLOCK SIZE control field in the Input Configuration register (Table 3.4-1). The value in this field is the number of samples acquired *for each active channe*l, and the total number of samples acquired equals this value *times* the number of active channels.

Note: If a BURST BLOCK SIZE of zero is selected while bursting is enabled, a burst trigger initiates a nonterminating burst that continues until: (a) the sample clock is disabled, (b) input bursting is disabled, or (c) BURST BLOCK SIZE becomes nonzero.

The END OF BURST status bit in the input buffer (Paragraph 3.4.5) is set HIGH for the last input value acquired in a burst. The INPUT BURST BUSY status flag in the BCR is HIGH during each triggered burst, and is LOW otherwise. *Input triggering cannot occur when INPUT BURST READY is LOW.*

If the TRIGGER INITIATOR control bit in the BCR is HIGH, the board is a trigger ***initiator***, and a burst trigger is provided either by the Rate-B generator or by the INPUT S/W TRIGGER control bit in the BCR. The INPUT S/W TRIGGER bit always produces a burst trigger, regardless of the state of the Rate-B generator or the INITIATOR control bit. In the ***Initiator*** mode, each burst trigger produces a 100 nanosecond LOW output pulse at the bidirectional TRIGGER I/O pin in the system I/O connector.

If the TRIGGER INITIATOR control bit is LOW (default), indicating *Target Mode*, the TRIGGER I/O pin becomes an input, and a trigger is generated for each HIGH-to-LOW transition received at the pin. The Rate-B generator is ignored in the target clocking mode, but the INPUT S/W TRIGGER control bit remains active.

NOTE: If TRIGGER INITIATOR is HIGH (initiator mode), the TRIGGER I/O pin is an output and produces a trigger pulse in response to either an input trigger or an output trigger (3.13.5.2). If the control bit is LOW (target mode), an input HIGH-to-LOW transition at the TRIGGER I/O pin produces either an input or output trigger if either is enabled individually, or inputs and outputs simultaneously if both are enabled.

3.4.5 Input Data Buffer

3.4.5.1 Organization

Analog input data accumulates in the input data FIFO buffer until extracted by the PCI bus. The buffer has a capacity of 2.0 Megasamples, and contains a 16-bit data field, a 1-bit tag field, and an END OF BURST status bit (Table 3.4-2). Analog input data is right-justified to the LSB, and occupies bit positions D00 through D15.

NOTE: The input buffer capacity of 2 Megasamples is distributed among both input channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 2097152/ Number of active channels.

The channel tag identifies the first (lowest-numbered) active channel in each active channel-set. Reserved bits are always returned as zeros. The END OF BURST (EOB) status bit identifies the last data value in an input burst or function.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

Bit Field	Designation	Description
D00	DATA00	Data value least significant bit (LSB)
D01-D14	DATA01 - DATA14	Data value intermediate bits
D15	DATA15	Data value most significant bit (MSB)
D16	FIRST-CHANNEL TAG	Tag assigned to first (lowest-numbered) active channel.
D17	END OF BURST (EOB)	Identifies the last input value in a burst.
D18-D31	(Reserved)	Always zero.

In order for the input buffer to acquire input data, the ENABLE INPUT BUFFER control bit must be set HIGH in the BCR. The buffer can be cleared, or emptied, by writing a "one" to the CLEAR INPUT BUFFER control bit in the BCR. The CLEAR INPUT BUFFER bit clears automatically. An empty buffer returns an indeterminate value.

The INPUT BUFFER OVERFLOW status bit in the BCR is set HIGH if the buffer overflows, thereby indicating data loss. The INPUT BUFFER UNDERFLOW bit is set HIGH if the buffer underflows (underruns), indicating that indeterminate data was acquired from an empty buffer. Each status bit remains HIGH until cleared, either directly from the bus, by the CLEAR INPUT BUFFER control bit, or by a board reset.

3.4.5.2 Buffer Size and Threshold Registers

The Input Buffer Size control register listed in Table 3.1-1 contains the total number of data values present in the input buffer. The Input Buffer Threshold register (Table 3.4-3) specifies the buffer size value above which the INPUT BUFFER THRESHOLD FLAG is asserted HIGH. The threshold flag is duplicated in the BCR.

Table 3.4-3. Analog Input Buffer Threshold Register

Offset: 002Ch **Default: 001F FFFEh**

Bit	Mode	Designation	Default	Description
D00-D21	RW	ANALOG INPUT BUFFER THRESHOLD	1F_FFFEh	Specifies the number of values in the analog input buffer above which the threshold flag is asserted HIGH.
D22-23	RO	(Reserved)	0	---
D24	RO	ANALOG INPUT BUFFER THRESH FLAG	0	HIGH when the number of values in the analog input buffer exceeds the specified buffer thre0shold.
D25-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

3.5 Analog Input Buffer DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as a bus master. Set Bit 02 in the PCI Command register HIGH to select the bus mastering mode. Refer to the PCI-9056 reference manual for a description of DMA configuration registers.

3.5.1 Block Mode

Table 3.5-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 00, in which a PCI interrupt is generated when the transfer has been completed. For most applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Table 3.5-1. Typical Input DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

3.5.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.5-2 shows a *typical* PCI register configuration for DMA Channel 00 demand mode operation.

Table 3.5-2. Typical Input DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The PCI-9056 adapter extracts data from the 32-Bit (Lword) local bus in 64-Bit (quad-word) increments. Consequently, *if the buffer runs empty or nearly empty*, the situation can arise in which the last one or two samples in an active channel group are retained until subsequent data is acquired. If this occurs, the next sample set flushes the retained data through the PCI-9056 adapter to the PCI bus, and no samples are lost.

NOTE: The default analog input DMA channel for demand-mode operation is Channel 00. To operate in DMA Channel 01, set the SWAP DEMAND MODE CHANNELS control bit HIGH in the BCR and use the Channel 01 PCI registers.

3.6 Data Coding Formats

Analog input and output data is arranged as 16 active right-justified data bits with the coding conventions shown in Figure 3.6-1. The default format is offset binary. Two's complement format is selected by clearing the OFFSET BINARY control bit LOW in the BCR. Unless indicated otherwise, offset binary coding is assumed throughout this document.

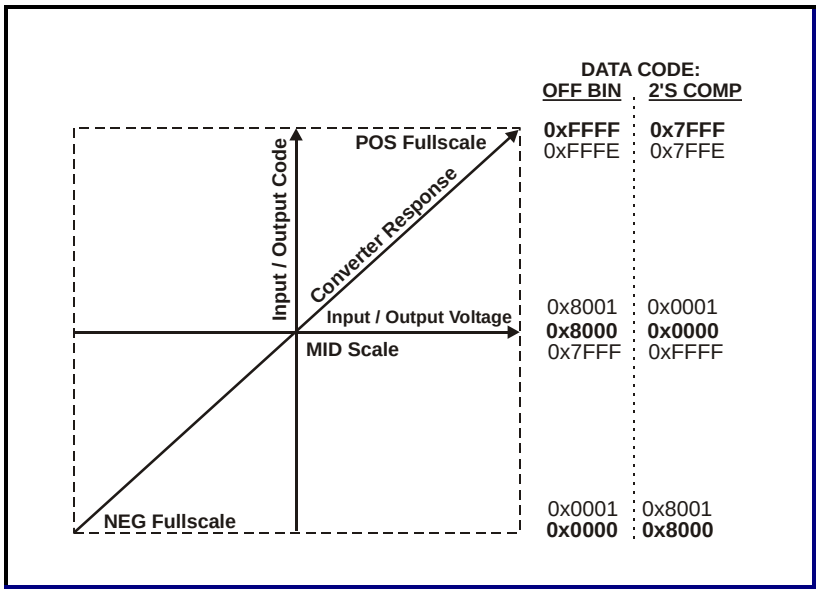


Figure 3.6-1. Analog Data Coding Formats; 16 Bit Data

3.7 Rate-A/B Generators

Two rate generators supply independent clocking frequencies from 3 Hz to 2.000 MHz. The Rate-A Generator shown in Table 3.7-1 generates an internal sample clock for the analog inputs. The Rate-B generator output can be used as a trigger source for input burst acquisition.

Each generator is enabled by the associated ENABLE RATE-A/B GENERATOR control bit in the BCR. The generators are disabled when these bits are LOW.

Table 3.7-1. Analog Input and Trigger Rate Generator Registers (A,B)

Offset: 001Ch (Rate-A), 0020h (Rate-B) **Default: 0000 007E (Rate-A), 0000 2760h (Rate-B)**

Data Field	Mode	Designation	Default	Description
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

The frequency **Fgen** (Table 3.7-2) of each generator is calculated as:

Fgen = Fclk / Ndiv,

where **Fclk** is the master clock frequency for the board, and **Ndiv** is the value written to the Rate-A/B Generator register. **Fgen** and **Fclk** are both expressed in the same frequency units. For simplicity, **Fclk** is assumed here to be 40.000 MHz, but is an ordering option and can have any value close to this frequency. The actual value for **Fclk** is identified in the Assembly Configuration register shown in Section 3.16.

Table 3.7-2. Input Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (40 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
20	0014	2000.00
21	0015	1904.76
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv

* ±0.003 percent.

3.8 Multiboard Synchronization

Analog input and output clocking and triggering can be synchronized among multiple boards by designating one of the boards as an ***initiator***, and the remaining boards as ***targets***. In order to implement this function, the boards must be connected together as described in Paragraph 2.3.4.

When multiple boards are configured as an initiator and multiple targets, the analog input clock, the analog input trigger, and the analog output clock generated in the initiator board are duplicated in the target boards with delays of less than 100 nanoseconds.

All boards default to the target mode, with the ANALOG INPUT CLK INITIATOR and TRIGGER INITIATOR control bits cleared LOW in the BCR. To designate a board as a clock or trigger initiator, set the associated control bit HIGH.

NOTE: To avoid contention among boards that are wired in an initiator/target configuration, ensure that all target boards have been designated before initiating clocking operations.

3.9 Digital I/O Port

The 8-Bit bidirectional digital I/O port consists of eight bidirectional TTL lines, as shown in Table 3.9-1. Data field DIO PORT DATA[7..0] represents the eight digital I/O pins in the system I/O connector. Logic polarities are retained, with a HIGH level at a connector pin associated with a HIGH level for the corresponding bit in the Digital I/O Port register. DIO PORT DATA[0] corresponds to register Bit D00.

Each data byte is an *input field* from the system I/O connector if the corresponding DIO PORT OUTPUT control bit is LOW, or is an *output field* to the connector if the control bit is HIGH. The DIO PORT DATA field defaults to inputs.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 0000 00XXh**

Data Field	Mode	Designation	Default	Description
D00-D07	RW	DIO PORT DATA[7..0]	XXh	System connector pins DIO 00 through DIO 07.
D08	RW	DIO PORT OUTPUT	0	Direction control for DIO BYTE 00. When LOW, DIO PORT DATA[] is an input field. When HIGH, DIO PORT DATA[] is an output field.
D09-D31	RO	(Reserved)	0h	Read back as all-zero.

3.10 Autocalibration

To obtain maximum measurement accuracy, autocalibration should be performed after:

- Power warmup,
- PCI bus reset,
- Analog input or output range change.

The analog inputs are always calibrated on all input ranges during autocal, but the analog outputs are calibrated only on the selected output range.

Note: Analog outputs ***are not active*** during standard autocalibration,

Autocalibration is invoked by setting the AUTOCAL control bit HIGH in the BCR. The control bit returns LOW automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of less than 5 seconds. Completion of the operation can be detected either by monitoring the "Autocal Busy" status flag in the primary status register (Table 3.11-1), or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in internal volatile memory. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR is cleared LOW at the end of the autocalibration interval, and remains LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs. This status flag responds to both general and analog-inputs Autocal.

Inputs-Only Autocalibration:

The ANALOG INPUTS AUTOCAL control bit in the BCR initiates an autocal sequence that calibrates only the analog inputs. This control bit remains HIGH during the autocal sequence, and clears automatically at autocal completion. *The analog outputs are forced to midrange (zero) during the calibration sequence, and retain this value after autocalibration.*

3.11 Primary Status Register

Critical status flags are consolidated into a single Primary Status register (Table 3.11-1), which is organized into a selection field and a response field. A response status bit is asserted if the selected event occurs after it has been selected. The response bit remains high until it is cleared from the PCI bus, either by clearing the response bit, *or by clearing the associated selection bit*.

NOTE: Response status bits can *only* be cleared LOW from the PCI bus. A "one" written to a response bit is ignored.

A selected event is edge-detected on a transition of the event from false to true. Once asserted, a response bit remains in that state until cleared from the bus, regardless of subsequent changes in the associated event state.

NOTE: Any PSR event will generate a local interrupt (LINT#), which can in turn can generate an interrupt (INT-A) on the PCI bus. Refer to the PLX™ PCI-9056 adapter reference manual for a description of interrupts.

Table 3.11-1 Primary Status Register

Offset 0x0030 **Default 0x0000 0000**

Selection Bit [1]	Critical Event	Response Bit [2]	Reference Paragraph
D00	Autocal completed	D16	3.10
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18	
D03	Input Buffer Overflow or Underflow	D19	3.4.5.1
D04	Analog Input Burst initiated (BURST BUSY LO-HI)	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO)	D21	
D06	BDO [3] Buffer threshold flag HIGH-to-LOW transition	D22	3.19
D07	BDO [3] Buffer threshold flag LOW-to-HIGH transition	D23	
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition	D24	3.9
D09	Output Buffer threshold flag HIGH-to-LOW transition	D25	3.13.2.3
D10	Output Buffer threshold flag LOW-to-HIGH transition	D26	
D11	Output Load-Ready Flag HIGH-to-LOW transition	D27	3.13.3.3
D12	Output Load-Ready Flag LOW-to-HIGH transition	D28	
D13	Analog Output Burst Ready	D29	3.13.5.2
D14	Output Buffer Overflow or Frame Overflow	D30	3.13.2.3 3.13.3.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Remains HIGH until cleared LOW.
3. BDO = "Buffered Digital Outputs".

3.12 Analog Outputs

The two analog output channels can be accessed either directly through two control registers, or through a 2.0 Megasample data buffer. The output voltage range is selectable independently of the analog input ranges, and the outputs can be disconnected from the system I/O connector.

3.12.1 Output Ranges

An output voltage range of ±10V, ±5V or ±2.5V is assigned by the OUTPUT RANGE control field in the BCR. The default output range is ±10V.

3.12.1.1 Connecting/Disconnecting the Analog Outputs

The analog outputs are enabled (connected to the system I/O connector pins ANA_OUT_xx) when the ENABLE ANALOG OUTPUTS control bit is HIGH in the BOR, or are disconnected (disabled) when this bit is LOW. The outputs are disconnected also during power-up and during autocalibration, and are disconnected by default. When disconnected, the output impedance is greater than 10 K-Ohms.

3.12.2 Registered (Direct) Analog Output Control

If the ENABLE BUFFERED OUTPUTS control bit is LOW in the BCR, the analog outputs are controlled in Direct-Register mode through the two ANALOG OUTPUT CHAN xx registers listed in Table 3.1-1. If the control bit is HIGH, then the outputs are controlled in the Buffered Outputs mode through the output buffer described in Section 3.13.

Each analog output channel is controlled directly through the associated ANALOG OUTPUT CHAN xx register. Output data is written to a 16-bit field that is right-justified in the data registers (Table 3.12-1). The outputs are self-clocking in this mode, and each channel updates immediately after receiving new data from the host.

Table 3.12-1. Analog Output Channel Data Register

Offset: 0008h - 0014h **Default: 0000 8000h**

Data Field	Designation	Description
D00	DATA00	Data value least significant data bit
D01-D14	DATA01 - DATA14	Data value intermediate data bits
D15	DATA15	Data value most significant data bit
D16-D31	(Reserved)	Data in this field is ignored.

3.13 Buffered Analog Output Control

If the ENABLE BUFFERED OUTPUTS control bit is set HIGH in the BCR, the analog outputs are controlled through the output buffer in the *Buffered Outputs* mode described in this section.

This section describes those operations that control the movement of data from the PCI bus through the analog output buffer. These functions include the selection of active channels, the organization of data within the buffer, and the clocking of data from the buffer to the analog outputs. The principal parameters associated with controlling the analog output channels are summarized below in Table 3.13-1.

Table 3.13-1. Summary of Output Control Parameters

Parameter	Mode	Description
Data Control	Active Channels; **Channel Group**	A single set of all active output channels constitutes an ***Active Channel Group***. Active channels are selected under a channel mask.
	Data Frame	All data values in the buffer comprise a *Data Fr*ame.
	Data Coding	Output data can be coded either in offset-binary format or in two's complement format.
Buffer Configuration	Open	Data read from the buffer is used and then discarded, until the buffer is empty.
	Circular (closed)	Data within the buffer is recirculated. Each value read from the output of the buffer FIFO is written back to the input of the FIFO. An end-of-frame (EOF) flag tracks the movement of data through the buffer.
Clock Source	External	External hardware provides the sample clock.
	Internal	The sample clock is provided by an internal rate generator, at a rate determined by the sample rate control register, or directly by a control bit in the BCR
Clocking Mode	Simultaneous	At each clock occurrence, the next channel group (i.e.: a single group of all active channel values) in the output buffer is transferred to the respective analog output channels. Both outputs are updated simultaneously.
	Sequential (Legacy)	At each clock occurrence, the next active channel value in the output buffer is transferred to the associated analog output channel, which is updated immediately.
Sampling Mode	Continuous	The contents of the output buffer are sampled continuously at the selected clock rate.
	Triggered Burst	A single data frame in the buffer is clocked to the outputs.

3.13.1 Data Organization

3.13.1.1 Active Channels

Analog output data is loaded into the output buffer in discrete groups or frames of channel data. An active *channel group* consists of a single set of output values for all active channels.

Only active output channels receive data from the output buffer. A channel that is deselected to the inactive state retains the last value that was received while the channel was still active. During initialization, all channels are designated as active and are set to midrange (zero output level).

3.13.1.1.1 Selection

An output channel is selected as *active* by setting the corresponding AO CHANNEL-xx-ACTIVE selection bit HIGH in the Buffered Output Operations register shown in Table 3.13-2. A channel is deselected to the *inactive* state by clearing the corresponding selection bit.

3.13.1.1.2 Loading

Channel data values are loaded into the output buffer in ascending order of active channels. The channel groups are loaded contiguously, beginning with the first group to be transferred to the outputs, and proceeding sequentially to the last group. Figure 3.13-1 illustrates a loading example that represents two active channels, with 100 values per channel. Each channel group consists of active channels 0, 1 and 3.

NOTE: Data can be loaded from the PCI bus to the output buffer only if the buffer is open; that is, not circular or closed (3.13.2.4).

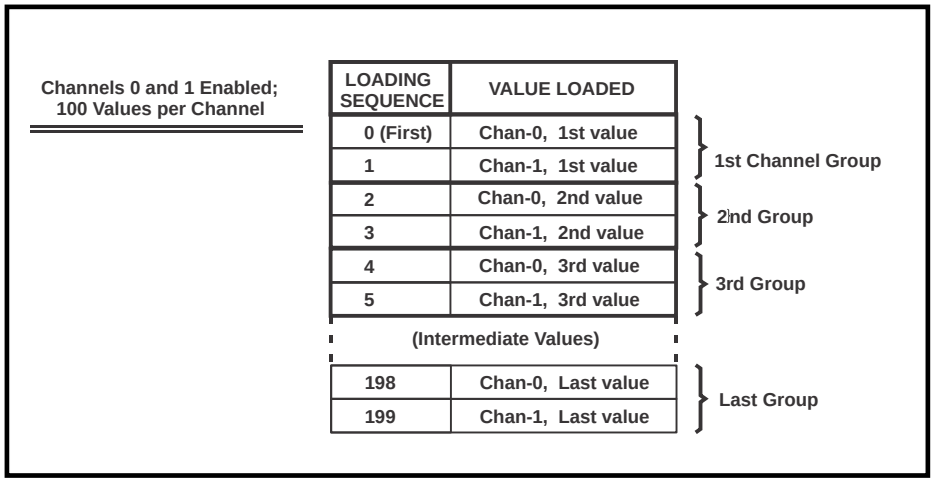


Figure 3.13-1. Typical Analog Output Buffer Loading Sequence

Table 3.13-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_1043h**

Bit	Mode	Designation	Def	Description	Ref
D00	R/W	AO CHAN 00 ACTIVE	1	Active-channel mask for analog output channels. HIGH => Active; LOW => Inactive.	3.13.1.1
D01	R/W	AO CHAN 01 ACTIVE	1		
D02-D03	R/W	(Reserved)	0		
D04	R/W	ANALOG OUTPUT CLK INITIATOR	0	Selects the internal Rate-C generator for output clocking if HIGH, or the Output Clock I/O hardware input if LOW.	3.13.4.1
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.13.4
D06	RO	OUTPUT CLOCK READY	1	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	
D07	R/W	OUTPUT SW CLOCK *	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.13.4.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.13.2.5
D09	R/W	LOAD REQUEST *	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.13.3.3
D10	RO	LOAD READY	0	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	
D11	R/W	CLEAR OUTPUT BUFFER *	0	Resets the output buffer to empty.	3.13.2.3
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	
D13	RO	AO BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	
D14	R/W	ENABLE ANALOG OUTPUTS	0	Enables the analog output drivers when HIGH. When LOW, the analog outputs are in a high-impedance state at zero-level.	3.12.1.1
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.13.2.3
D16	R/W	AO BUFFER OVERFLOW	0	Set HIGH when data is written to a full buffer. **	
D17	R/W	FRAME OVERFLOW	0	Set HIGH when data is written to a closed buffer. **	
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.13.5
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.13.5.2
D20	R/W	OUTPUT SW TRIGGER *	0	Produces a single output trigger event when asserted. Clears LOW automatically when the clock event is completed. Independent of triggering mode.	
D21	R/W	TRIG AI BURST ON AO	0	Synchronizes triggering of analog input bursts to analog output bursts.	3.17
D22-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

* Clears LOW automatically when operation is completed.

** Remains HIGH until cleared by a direct write as LOW, or by initialization.

3.13.1.2 Data Frame

A *data frame* consists of an integral number of channel groups.

For triggered bursts, or for function concatenation, the last active channel in the last channel group is designated as the *end-of-frame* (EOF). The EOF designation is applied by setting the EOF flag (D16) HIGH when loading the last channel value into the buffer. Thereafter, the EOF flag follows the last channel value through the buffer.

3.13.1.3 Voltage Range Selection

An output voltage range of ±10V, ±5V or ±2.5V is assigned by the OUTPUT RANGE control field in the BCR. The default output range is ±10V.

For maximum accuracy, autocalibration should be performed after a new input or output range is selected.

3.13.2 Output Buffer

Analog output data from the PCI bus is first corrected for offset and gain errors, and then flows directly into the 256K-sample analog output FIFO data buffer (Table 3.13.1). From the buffer, the corrected data is routed to the analog output DAC channels.

NOTE: The output buffer capacity of 2.0 Megasamples is distributed among all active output channels. The capacity in samples-per-channel is:

Sample Capacity per Channel = 2097152 / Number of active channels.

3.13.2.1 Output Data Format

Analog output data values are written in Lword-serial sequence from the PCI bus to the Analog Output Buffer register shown in Table 3.13-3. Bits D15..0 represent the output data value. Bit D16 is set HIGH to indicate the last value in a data frame, and is the end-of-frame (EOF) flag. Bits D31..17 are inactive. Access to the output buffer is supported for both single-longword transfers and single-address multiple-longword DMA transfers. The output buffer appears to the PCI bus as a single register, and a read-access to this register returns an all-zero value.

Table 3.13-3. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only)**

Bit	Mode *	Designation	Description
D00	WO	DATA 00	Least significant data bit
D01-D14	WO	DATA 01 - DATA 14	Intermediate data bits
D15	WO	DATA 15	Most significant data bit
D16	WO	EOF FLAG	End-of-frame (EOF) flag.
D17-D31	WO	---	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

3.13.2.2 Output Data Coding

Analog output data coding is described in Paragraph 3.6.

3.13.2.3 Output Buffer Control

The Buffered Output Operations register in Table 3.13-2 controls and monitors the flow of data through the analog output data buffer. Asserting the CLEAR OUTPUT BUFFER control bit HIGH clears, or empties, the buffer.

The AO BUFFER OVERFLOW flag is set HIGH if data is written to a full buffer, and the FRAME OVERFLOW flag indicates that an attempt was made to write data to a closed buffer. Both flags indicate data loss. Once set, each of these flags remains HIGH until written LOW directly from the bus, or by initialization .

The AO BUFFER EMPTY flag indicates that the buffer contains no output data. The AO BUFFER FULL flag is asserted when the buffer is full. Data written to a full output buffer is discarded.

The Output Buffer Size register shown in Table 3.13-4 contains the number of output data values present in the buffer, and is updated continuously.

Table 3.13-4. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-D21	RO	BUFFER SIZE	00 0000h	Number of values in the analog output buffer
D22-D31	RO	(Inactive)	0	---

The Output Buffer Threshold register in Table 3.13-5 specifies the buffer size value above which the OUTPUT BUFFER THRESHOLD FLAG is asserted HIGH.

Table 3.13-5. Output Buffer Threshold Register

Offset: 0040h **Default: 001F FFFEh**

Bit	Mode	Designation	Default	Description
D00-D21	RW	OUTPUT BUFFER THRESHOLD	1F FFFEh	Specifies the number of values in the analog output buffer above which the threshold flag is asserted HIGH.
D22-23	RO	(Reserved)	0	---.
D24	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the analog output buffer *exceeds* the specified buffer threshold.
D25-D31	RO	(Reserved)	0	---

3.13.2.4 Open Buffer

If the CIRCULAR BUFFER control bit is LOW in the buffer operations register, the output buffer operates in the open mode. Data in an open buffer is discarded as it is used. Consequently, the buffer is self-flushing, and will empty itself unless it is replenished from the PCI bus. This mode of operation permits the continuous flow of data from the PCI bus to the analog outputs.

The open-buffer configuration also can be used to produce a one-shot waveform, provided the particular waveform is to be used only once. Figure 3.13-2 illustrates the movement of a single data frame through an open buffer.

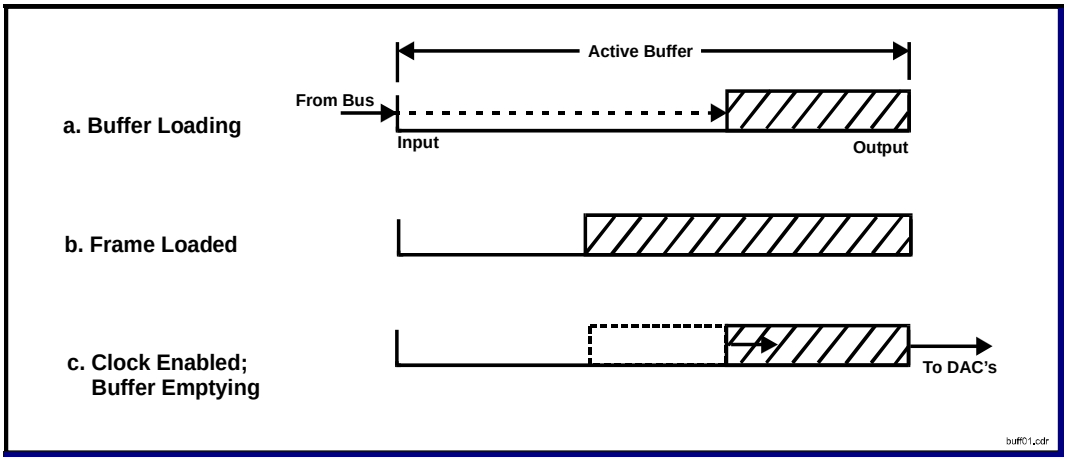


Figure 3.13-2. Open Buffer Data Flow

3.13.2.5 Circular Buffer

Data in a circular (closed) buffer is retained indefinitely. This configuration generally is implemented to produce either periodic waveforms of constant frequency, or one-shot transient waveforms that will be used repeatedly but not necessarily periodically. While closed, the buffer is not accessible from the PCI bus.

In Figure 3.13-3 a single data frame is loaded into the buffer. The buffer is then closed (CIRCULAR BUFFER set HIGH) and clocking is enabled. The data frame subsequently circulates in the buffer while passing data values to the output channels.

An end-of-frame (EOF) flag accompanies the end-point, or last value in a data frame. The EOF flag is D16 in the buffer, and is set HIGH when the last value in a data frame is loaded. This flag is used at the end of a function or triggered burst to define the last value. Multiple contiguous burst functions, or frames, can reside in the buffer simultaneously.

NOTE: Disable output clocking before loading the output buffer for circular operation.

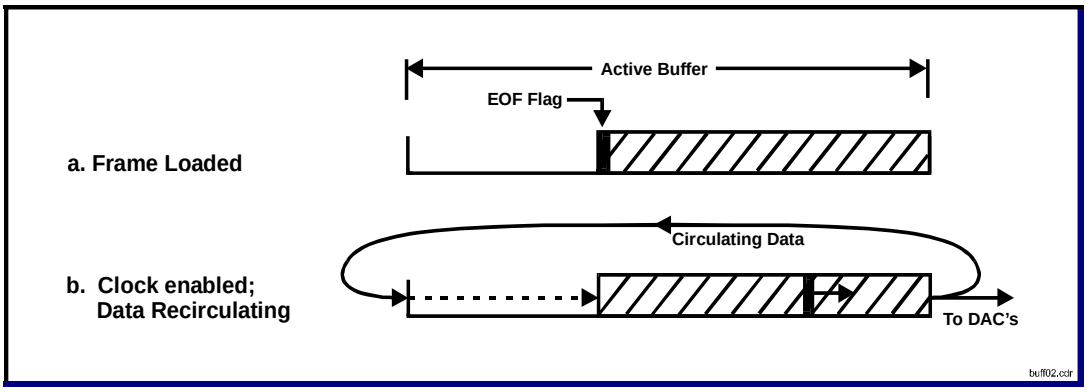


Figure 3.13-3. Circular Buffer Data Flow

3.13.3 Function Generation

3.13.3.1 Periodic and One-Shot Functions

Periodic waveforms are produced when the buffer is configured for continuous sampling and circular operation. In this mode, the contents of the buffer are scanned continuously as long as clocking is enabled and a clock is present. The data frame is recirculated through the buffer repeatedly. Clocking is enabled when the ENABLE OUTPUT CLOCKING control bit in the buffer operations register is HIGH.

If triggered-burst sampling is used in conjunction with a circular buffer, a *one-shot waveform* is produced that contains all values within a single data frame. The triggered burst is initiated by a software or hardware trigger, and terminates automatically when the end-of-frame (EOF) flag is encountered. Because the buffer is circular, the waveform is retained in the buffer and can be reproduced repeatedly by subsequent triggers.

3.13.3.2 Multiple Functions

When multiple functions are loaded into the buffer as contiguous data frames, and if triggered-burst sampling is selected, the functions will be generated sequentially in response to a series of burst triggers. If the buffer is open, the functions are flushed from the buffer as they are clocked to the analog outputs. However, if the buffer is closed (circular), the functions are retained in the buffer, and the series of functions is repeated indefinitely. .

3.13.3.3 Function Sequencing (Concatenation)

A new function can be concatenated to the end of an existing function in a circular buffer, while the existing function is being flushed from the buffer. During this operation, the existing function is flushed from the buffer as it is clocked to the outputs, and is replaced by the new function. When the last value of the existing function is clocked out of the buffer, the buffer closes and the new function seamlessly begins circulating in the buffer and producing an output.

Introduction of a new function commences by setting the LOAD REQUEST flag HIGH in the buffered output operations register (Table 3.13-2), and by then waiting for the LOAD READY flag to be asserted. (In effect, LOAD REQUEST is an "interrupt request" to the buffer). The LOAD READY flag indicates that the buffer has opened, and that the existing function is being flushed from the buffer, beginning with the first value in the function's data frame.

After LOAD READY goes HIGH, the new function is written to the buffer and is terminated with an EOF flag (output data bit D16 set HIGH). The EOF flag of the existing function causes the buffer to close, and clears both the LOAD READY flag and the LOAD REQUEST control bit. Notice that the loading of the new function into the buffer must be completed before the existing function terminates.

In Figure 3.13-4, an existing function is replaced by a new function while the existing ('old') function is flushed from the buffer.

NOTE: If the loading of a new function extends beyond the LOAD-READY interval, the FRAME OVERFLOW flag is set HIGH in the Buffer Operations register, indicating data loss. Once set, this flag remains HIGH until written LOW directly from the bus, or by initialization

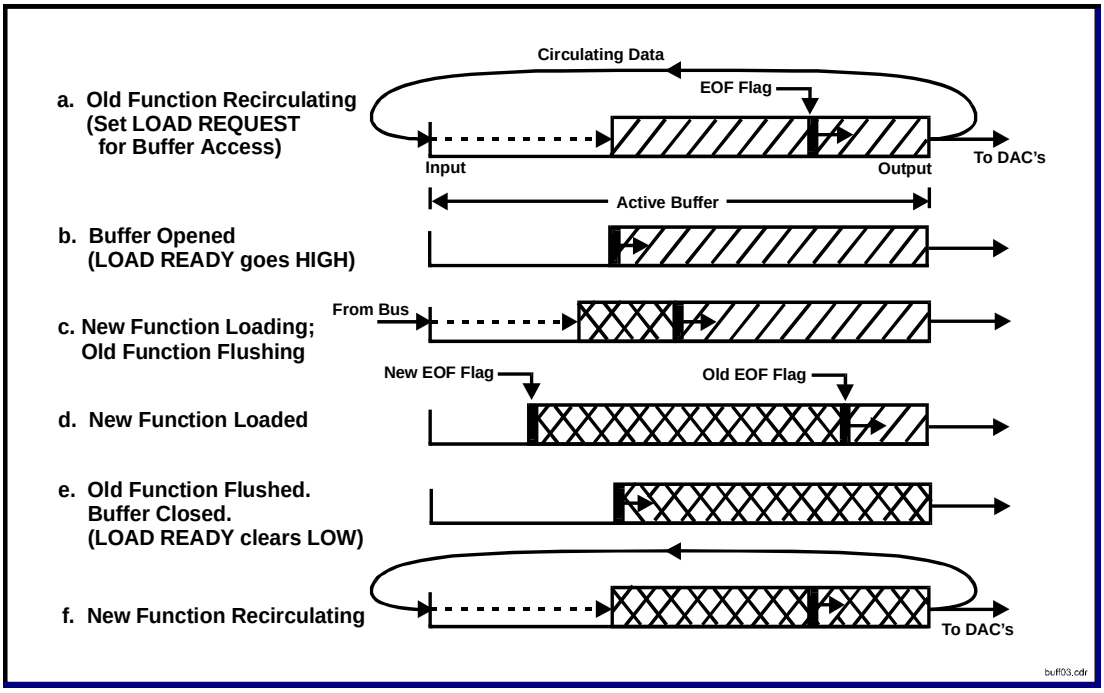


Figure 3.13-4. Function Sequencing

3.13.4 Output Clocking

If the ENABLE OUTPUT CLOCKING control bit in the buffer operations register is asserted HIGH, clocking is enabled and the active analog outputs are updated at each occurrence of the sample clock. The sample clock can be generated internally by the rate generator, or can be supplied externally through the I/O connector. Output clocking is disabled when the ENABLE OUTPUT CLOCKING control bit is LOW. The OUTPUT CLOCK READY flag indicates that data is available to be clocked to the output channels .

Hardware output signal OUTPUT CLK I/O (Table 2.2-1) goes LOW momentarily each time a sample clock occurs, Connecting this signal to the OUTPUT CLK I/O pins of other boards permits synchronous clocking of multiple boards.

3.13.4.1 Clock Source

When buffer operations register bit ANALOG OUTPUT CLK INITIATOR is LOW, the output clock is supplied externally through the I/O connector as OUTPUT CLK I/O and the internal Rate-C generator is ignored. If the control bit is HIGH, the output clock is derived from the internal Rate-C generator. An output clock can also be supplied at any time by asserting the OUTPUT SW CLOCK control bit, which clears automatically.

3.13.4.1.1 External Clock

The external clock source can have any frequency up to the maximum value specified for the sampling rate. When the external clock source is selected, sampling occurs on a HIGH-to-LOW transition of the OUTPUT CLK I/O pin in the I/O connector.

3.13.4.1.2 Internal Output Rate Generator

The internal Rate-C generator provides a sample clock that is adjustable by the RATE[23..0] control bits in the Output Sample Rate control register shown in Table 3.13-6. The Rate-C generator is enabled by setting the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.

Table 3.13-6. Output Sample Rate Control Register (Rate-C)

Offset: 004Ch **Default: 0000_007Eh**

Data Bit	Mode	Designation	Description
D00	R/W	RATE 00	Least significant rate bit
D01-D22	R/W	RATE 01 - RATE 22	Intermediate rate bits
D23	R/W	RATE 23	Most significant rate bit
D24-D31	RO	---	Inactive. Returns all-zero.

The output clocking rate **Fclock** is calculated from the relationship:

$$\textbf{Fclock (Hz) = Fclk / Nrate ,}$$

where **Nrate** is the decimal equivalent of the value in the RATE value in the Sample Rate control register, and **Fclk** is the master clock frequency for the board. For simplicity, **Fclk** is assumed here to be 40.000 MHz, but is an ordering option and can have any value close to this frequency. The actual value for **Fclk** is identified in the Assembly Configuration register shown in Section 3.16.

Table 3.13-7 illustrates the effect of **Nrate** on the sample rate. Clocking rates more than 2-3 percent above **2000 KSPS** can produce unpredictable results and are not recommended. **Nrate** should not be modified during function generation.

Table 3.13-7. Output Sample Rate Selection

Ndiv		FREQUENCY Fgen (40.32MHz Master Clock)*
(Dec)	(Hex)	(kHz)
20	0014	2016.00
21	0015	1919.04
---	---	Fclock (Hz) = Fclk (Hz) / Ndiv

* ±0.003 percent.

3.13.4.2 Simultaneous Clocking

Simultaneous sampling is selected by setting the SIMULTANEOUS OUTPUTS control bit in the board control register HIGH. If simultaneous sampling is selected, the analog values in each successive channel group appear simultaneously at the outputs, with minimum time-skew between channels. Upon each occurrence of the sampling clock, an entire active channel group is transferred from the output buffer, and all outputs are updated simultaneously. In this mode, the effective sample rate for each channel equals the output clocking rate **Fclock**.

3.13.4.3 Sequential Operation

Sequential sampling is selected when the SIMULTANEOUS OUTPUTS control bit in the board control register is LOW. At each clock occurrence, a single channel value is transferred from the buffer to the associated output channel, and the channel is updated immediately.

To implement this mode, follow the general procedure for Simultaneous Buffered Outputs (3.14.2), but clear the SIMULTANEOUS OUTPUTS control bit LOW in the BCR.

3.13.5 Sampling Mode

3.13.5.1 Continuous Sampling

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is LOW (default), the *continuous sampling* mode is selected and data is transferred continuously from the buffer to the analog outputs, assuming that the buffer is not empty and that an output clock is present.

3.13.5.2 Data Bursts

If the ENABLE OUTPUT BURST control bit in the Buffered Output Operations register is HIGH, burst operation is selected. During a *triggered output burs*t, data is transferred continuously from the output buffer to the analog outputs until either the ***buffer goes empty, or the end-of-frame (EOF) flag is encountered***. In the triggered-burst sampling mode, an internal or external output trigger initiates the transfer of data from the output buffer to the output channels.

If the TRIGGER INITIATOR control bit in the BCR is HIGH, *internal triggering* is selected, and either a software or a hardware trigger will initiate a burst. A software trigger is generated by setting the OUTPUT S/W TRIGGER control bit HIGH, and a hardware trigger is provided by the

Rate-B generator, if enabled. These trigger sources are independent of each other, and the occurrence of either or both will initiate a burst. The OUTPUT SW TRIGGER bit remains HIGH during the burst, and clears automatically when the burst is completed.

In the initiator mode, hardware output pin TRIGGER I/O produces a LOW pulse at the beginning of each burst. Connecting this signal to the TRIGGER I/O pins of other boards permits synchronous burst triggering of multiple boards.

If the TRIGGER INITIATOR control bit is LOW in the BCR, indicating *Target Mode or External triggering*, a hardware burst trigger occurs upon a HIGH-to-LOW transition of the TRIGGER I/O pin in the I/O connector, *if* the ENABLE OUTPUT BURST control bit in the operations register is HIGH, *and* if the BURST READY flag also is HIGH. The BURST READY flag is LOW during a burst, and is HIGH if no burst is in progress. The OUTPUT S/W TRIGGER control bit also is active in the target mode.

Multiple burst functions can exist simultaneously within the buffer if the end-of-frame (EOF) flag is used (Paragraph 3.13.2.1). The EOF flag defines the last output value in each data burst. After a burst is triggered, data values from the buffer are clocked to the analog outputs at the selected sample rate until the EOF flag is encountered. The burst then terminates, and clocking of the buffer ceases until a subsequent trigger occurs.

Refer also to the Trigger Initiator note in 3.4.4.2.

3.13.6 Multiboard Synchronization

Boards that are configured for *synchronous clocking* update their outputs simultaneously in response to a common *clock* signal. Boards that are configured for *synchronous burst triggering* initiate data bursts simultaneously in response to a common *trigger* signal. Multiple boards can be arranged to operate with:

a. Independent clocking and burst triggering
b. Synchronous burst triggering (Common burst trigger)
c. Synchronous clocking (Common DAC clock)
d. Synchronous clocking and burst triggering (Common trigger and DAC clock).

As many as four boards can be synchronized together. External clock and trigger I/O signaling uses standard TTL levels.

3.13.6.1 Synchronous Bursts

To ***burst-synchronize*** a group of boards, the TRIGGER I/O signal from one board, the *burst-initiator*, is connected to the TRIGGER I/O pins of a group *of burst-target* boards. Each burst-target, when operated in the triggered-burst mode, initiates a single burst from its buffer each time the burst-initiator initiates a burst.

3.13.6.2 Synchronous Clocking

To ***clock-synchronize*** multiple boards together, the OUTPUT CLK I/O from one board, designated the *clock-initiator*, is connected to the OUTPUT CLK I/O pin of one or *more clock-target* boards. In this case, the clock-targets are configured for external clocking (ANALOG OUTPUT CLK INITIATOR cleared LOW in the operations control register), and the initiator is configured for internal clocking.

3.14 Analog Output Application Examples

Paragraphs 3.14-1 and 3.14-2 illustrate typical register sequences for generating Direct (Registered) and Buffered analog outputs. ***These guidelines are for illustration only.*** The registers involved are the BCR, the BOR, and the analog output buffer itself. Both examples assume default conditions for the associated control bits in the BCR and BOR. Internal clocking is assumed for buffered outputs.

3.14.1 Direct Analog Outputs Typical Sequence

1.

BCR: (Default)	SIMULTANEOUS OUTPUTS	LOW
	ENABLE BUFFERED OUTPUTS	LOW
	ENABLE RATE-C GENERATOR	LOW
BOR: (Default)	ANALOG OUTPUT CLK INITIATOR	LOW
	ENABLE OUTPUT CLOCKING	LOW
	CIRCULAR BUFFER	LOW
	CLEAR OUTPUT BUFFER	LOW

2. Write output values to the A NALOG OUTPUT CHAN 00/01 registers.

3.14.2 Buffered Analog Outputs Typical Sequence

1.

BCR: (Default)	SIMULTANEOUS OUTPUTS	HIGH [1]
	ENABLE BUFFERED OUTPUTS	HIGH [1]
	ENABLE RATE-C GENERATOR	LOW
BOR: (Default)	ANALOG OUTPUT CLK INITIATOR	LOW
	ENABLE OUTPUT CLOCKING	LOW
	CIRCULAR BUFFER	LOW

2.

BOR:	ANALOG OUTPUT CLK INITIATOR	HIGH [1]	
	CLEAR OUTPUT BUFFER	HIGH	(Clears automatically)

[1] Hold this state throughout the sequence.

3. Load data into the AO Buffer

4.

BOR:	ENABLE OUTPUT CLOCKING	HIGH	
	CIRCULAR BUFFER	HIGH	(Nonstreamimg functions)

5.

BCR:	ENABLE RATE-C GENERATOR	HIGH	Initiates output function(s)

To halt the buffer and initiate a new sequence:

6.

BCR:	ENABLE RATE-C GENERATOR	LOW	Halts output function(s)

7.

BOR:	ENABLE OUTPUT CLOCKING	LOW	
	CIRCULAR BUFFER	LOW	
	CLEAR OUTPUT BUFFER	HIGH	(Clears automatically)

8. Return to Step-3; Load AO buffer.

Specific operating modes and procedures can vary widely. The examples in this section illustrate basic operating modes, and can be modified or combined for more complex operations.

References to *functions* in these examples generally refer to a single output channel; However, each active channel represents an independent set of function values, and both channels share a common output clock.

Table 3.14-1. Summary of Operation Examples

Operation Example	Description
Simultaneous Direct Outputs	Data values accumulate in the output data buffer until an entire channel group has been loaded. When the last channel is loaded, all active output channels update simultaneously when clocked.
Continuous Function	An extension of Simultaneous Direct Outputs, in which the buffer is not allowed to become either empty or full.
Periodic Function	A single function is generated repeatedly in each active channel.
Function Burst	One or more functions are generated as discrete data bursts. The burst cycle is repeated indefinitely if the circular-buffer mode is selected.
Function Sequencing	An existing active function is replaced seamlessly by a new function.

3.14.3 Simultaneous Direct Outputs

Table 3.14-2. Simultaneous Direct (Single Group) Outputs Example

Operation	Host Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the BCR.	Simultaneous clocking is selected.
Select Internal Clocking	Set the ANALOG OUTPUT CLK INITIATOR control bit HIGH in the buffer operations register.	The internal Rate-C generator is selected as the output clocking source.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the default rate.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the output value for the first active channel.	Write the first value to the output data buffer.	First value is retained in the buffer.
Load the output values for the remaining active channels.	Write the remaining active channel values to the output data buffer.	Remaining values are accumulated in the buffer. When the last value is loaded, all values are extracted from the buffer and appear simultaneously at the associated output channels.
Repeat the above operations for subsequent channel groups.	Continue to write output values to the output data buffer.	All active channels are updated simultaneously when the last value in each group is written to the buffer.

Notes: 1. Data written to the buffer at rates above 2000KSPS will accumulate in the buffer.

3.14.4 Continuous Function

Table 3.14-3. Continuous Function Example

Operation	Host Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Set the buffer threshold flag to 1/4 of the expected block size.	Write 1/4 block size to the threshold register (Table 3.13-5).	The threshold flag will go LOW when the buffer contents drop below the threshold.
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking will be used).	Write the required sample clocking rate to the Rate-C generator control register.	The frequency of the internal rate generator is selected, if internal clocking is required.
If internal clocking is required, select internal clocking.	To select internal clocking, set the ANALOG OUTPUT CLK INITIATOR bit HIGH in the buffer operations register.	Internal clocking is selected, if required.
Enable clocking	Set the ENABLE OUTPUT CLOCKING control bit HIGH in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled at the selected rate. The internal rate generator is enabled, if internal clocking is required.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Write a block of values to all active channels. To avoid discontinuities in the output functions, the effective loading rate for channel groups must be greater than the sample (clocking) rate times the number of active channels. Maximum loading rate is 40MSPS during DMA transfers.	Write function values for all active channels to the output data buffer.	All active channels produce their respective output functions.
Wait for the buffer threshold flag to go LOW. (See Note 1).	Monitor the analog output buffer threshold flag until LOW.	The output buffer empties to less than 1/4-full status.
Repeat the previous two steps to sustain function generation.		All output functions proceed continuously.

Notes:
1. Response to the flag must be fast enough to prevent the buffer from going empty.

3.14.5 Periodic Function

Table 3.14-4. Periodic Function Example

Operation	Host Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUTPUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the first function value for each active channel.	Write the values for the first active group to the output data buffer.	Initial values for all active channels accumulate in the buffer.
Load the remaining function values for all active channels. (Note 1) Set the end-of-frame (EOF) flag.	Write all remaining function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	Remaining function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If the internal rate generator is to be used, select the sample rate. (Skip this step if external clocking will be used).	Write the required sample clocking rate to the Rate-C generator control register.	The frequency of the internal rate generator is selected, if internal clocking is required.
Note: The remaining operations may be performed simultaneously with a single write-transaction to the buffer operations register:	---	---
Select the circular buffer mode.	Set CIRCULAR BUFFER in the buffer operations register.	The output buffer is closed (circular).
If the internal rate generator is to be used, select internal clocking.	To select internal clocking, set the ANALOG OUTPUT CLK INITIATOR bit HIGH in the buffer operations register.	The internal Rate-C generator is selected, if required.
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING in the buffer operations register. Set the ENABLE RATE-C GENERATOR control bit HIGH in the BCR.	Clocking is enabled. All active channels produce their respective functions repeatedly until the clock is disabled or the operating mode is changed. All outputs update simultaneously at the sample clock rate.

Notes:

1. To generate periodic functions simultaneously in multiple channels, all functions must be commensurate. That is, the functions in all channels must have frequencies that are exact integer multiples of the frequency of the lowest-frequency channel. Conversely, the period of the lowest-frequency channel must be an exact integer multiple of the period of each of the other channels.

3.14.6 Function Burst

Table 3.14-5. Function Burst Example

Operation	Host Bus Action	Board Response
Select simultaneous clocking.	Set SIMULTANEOUS OUTPUTS in the board control register.	Simultaneous clocking is selected.
Clear the output buffer.	Set the CLEAR OUT BUFFER bit in the output operations register.	The output buffer clears to empty.
Load the first function value for each active channel.	Write the values for the first active group to the output data buffer.	Initial values for all active channels accumulate in the buffer.
Load the remaining function values for all active channels. Set the end-of-frame (EOF) flag.	Write all remaining function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	All function values for all active channels accumulate in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group.
If more than one burst-function is required, repeat the previous operations for each additional function.	---	If required, additional burst functions accumulate in the output buffer.
Select the trigger source.	For internal triggering, set the TRIGGER INITIATOR bit HIGH in the BCR. For external triggering, clear the bit LOW (default).	The frequency of the internal rate generator is selected, if internal clocking is required.
If the internal rate generator is to be used for ***clocking***, select the clocking rate.	Write the required clocking rate to the Rate-C generator control register.	The frequency of the internal rate generator is selected, if internal clocking is required.
If the internal rate generator is to be used for ***triggering***, select the triggering rate.	Write the required triggering rate to the Rate-B generator control register.	The frequency of the internal rate generator is selected, if internal triggering is required.
Select triggered-burst mode.	Set ENABLE OUTPUT BURST in the buffer operations register.	The triggered-burst operating mode is selected.
Prepare the buffer operations register for burst mode:	Write to the buffer operations register:	---
If the burst functions will be used repeatedly, select the circular buffer mode.	To select the circular buffer mode, set CIRCULAR BUFFER.	If required, the output buffer is closed (circular), and all functions will be retained in the buffer indefinitely.
If internal clocking is required, select internal clocking.	To select internal clocking, set ANALOG OUTPUT CLK INITIATOR.	Internal clocking is selected, if required.
Enable the sample clock.	Set ENABLE OUTPUT CLOCKING.	Output clocking is enabled.
Enable the internal rate generators, if required.	Set the ENABLE RATE-B and RATE-C GENERATOR control bits in the BCR.	Required internal rate generators are enabled.

3.14.6 Function Burst (Continued)

Table 3.14-6. Function Burst Example (Continued)

Operation	Host Bus Action	Board Response
For software burst triggering, generate a software trigger to produce a single burst on all active output channels.	Set OUTPUT SW TRIGGER in the buffer operations register..	All active output channels produce a single burst in response to each software trigger, if software triggering is used.
For external burst triggering, or internal rate-generator triggering, no further bus activity is required.	---	All active output channels produce a single burst in response to each internal or external trigger.

3.14.7 Function Sequencing (Concatenation)

Table 3.14-7. Function Sequencing Example

Operation	Host Bus Action	Board Response
Establish a periodic function as described in Paragraph 3.14.4. The following operations will replace the original ('old') function in each channel with a new function.	---	Each active output is producing a specific output function or waveform. The output buffer is circular (closed), and is not accessible from the bus.
Request buffer access	Set LOAD REQUEST in the buffer operations register.	The board will assert the LOAD READY flag when the EOF flag in the original function occurs.
Wait for the buffer to open.	Monitor the LOAD READY status flag. The buffer is open when this flag goes HIGH.	The EOF flag in the existing function set causes the LOAD READY bit in the buffer operations register to be asserted. The buffer is now open, and the original functions are being flushed from the buffer.
Load the new function for each active channel into the buffer. Set the end-of-frame (EOF) flag.	Write the function values for all active channels to the output buffer. Set the EOF flag (D16 in the output buffer) HIGH when writing the data value for the last channel in the last group.	New function values for all active channels reside in the buffer. The EOF flag is set HIGH in the buffer location that contains the last channel value in the last channel group. The original functions are still active, and the remaining values are flushed from the buffer as they are sent to the output channels.
(None required)	No further attention is required from the PCI bus.	The buffer returns to circular (closed) mode after the last data value in the original function set leaves the buffer. The new function then commences seamlessly and circulates within the buffer. Both the Load Request control bit and the Load Ready flag are cleared automatically when the buffer closes.

3.15 Analog Output Buffer DMA Operation

DMA transfers to the analog output FIFO buffer are supported in either block-mode or demand-mode, with the board operating as bus master. Bit 02 in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to the PCI-9056 reference manual for a detailed description of the associated DMA configuration registers.

3.15.1 Block Mode

Table 3.15-1 illustrates a *typical* PCI register configuration that would control a non-chaining, non-incrementing ***block-mode*** DMA transfer in DMA Channel 01, in which a PCI interrupt is generated when the transfer has been completed.

Table 3.15-1. Typical Output DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A0h	DMA Transfer Byte Count	Number of bytes in transfer	*
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

For typical applications, the DMA Command Status Register would be initialized to 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

3.15.2 Demand Mode

Demand mode transfers are controlled in a manner similar to block mode transfers, with the addition of ***demand-mode*** operation selected in the DMA mode register (D[12] = HIGH). Demand mode operation also requires the ***slow terminate*** mode (D[15] = LOW), which is the default state for this control bit. Table 3.15-2 shows a *typical* PCI register configuration for DMA Channel 01 demand mode operation.

Table 3.15-2. Typical Output DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32)	0002 1943h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

NOTE: The default analog output DMA channel for demand-mode operation is Channel 1. To operate in DMA Channel-00, set the SWAP DEMAND MODE CHANNELS control bit HIGH in the BCR and use the Channel-00 PCI registers.

3.16 Assembly Configuration Register

The read-only Assembly Configuration register (Table 3.16-1) contains the existing firmware revision and a status field that indicates the availability of optional features.

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12-D15	(Reserved bit field; all-zero)
D16	Number of analog input channels: 0 => 2 Analog input channels. 1 => 1 Analog input channel.
D17	Number of analog output channels: 0 => 2 analog output channels. 1 => No analog outputs.
D18-D19	Master clock frequency: 0 => 40.320MHz 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D20-D31	(Reserved bit field; returns all-zero).

3.17 Synchronizing Analog Input Bursts to Analog Outputs

Analog input and output bursts can be triggered simultaneously either from the Rate-B generator or externally through the Trigger IO pin in the system I/O connector. However, while both input and output bursts can be triggered simultaneously, the first input sample generally will not occur simultaneously with the first output clock. The skew of the first input sample from the first output clock can be as large as the input sample period or the output clocking period, whichever is larger.

The first input sample can be synchronized to the first output clock in simultaneous bursts by setting the TRIG AI BURST ON AO control bit HIGH in the BOR. This *synchronous mode* ensures that the first input sample will occur within 100-125 nanoseconds of the first output clock.

The following setup sequence represents one baseline approach to triggering input and output bursts simultaneously and synchronously, either externally or from the internal Rate-B generator. *It is provided as a general guide only, and is not intended to be a definitive set of requirements.* Input and output burst sizes are independent, and can have any valid values. ('Overlays' are OR'd into the indicated registers' existing contents):

1. Initialize the following control registers to required values:
   Rate Generator-A,B,C: (A=> input sample rate; B=> Internal burst triggering rate; C => Output clocking rate).
   Input Configuration.

2. BCR @00: Assert: (Net overlay = 010C_1000h):
   - D12: Enable Input Buffer.
   - D18: Simultaneous Outputs.
   - D19: Enable Buffered Outputs.
   - D24: Analog Input Clk Initiator.

3. BOR @3C: Assert: (Net overlay = 0000_0800):
   - D11: Clear Output Buffer.

4. Load the required function into the output buffer.

5. BOR @3C: Assert: (Net overlay = 0028_0130h for AO-synchronized bursts):
   (Net overlay = 0008_0130h for nonsynchronous simultaneous bursts):
   - D04: Analog Output Clk Initiator.
   - D05: Enable Output Clocking.
   - D08: Circular Buffer (If periodic function is required).
   - D19: Enable Output Burst.
   - D21: Trigger AI Burst On AO (For AI/AO burst synchronization).
     (BOR D21 has no effect with firmware Revision 202)

6. BCR @00: Assert: (Net overlay = 0D6C_1200):
   - D09: Enable Input Burst.
   - D21: Trigger Initiator (For Rate-B generator triggering; Omit for external triggering)
   - D22: Enable Rate-C Generator.
   - D26: Enable Rate-A Generator.
   - D27: Enable Rate-B Generator (Omit for external triggering).

Simultaneous triggering should commence at this point. Details of the setup will vary, depending upon the requirements of specific applications.

3.18 Isolating the System Bidirectional Control I/O Pins:

To eliminate activity on the bidirectional Input Clk I/O, Output Clk I/O, and Trigger I/O pins when they are not required for system control functions, the Ancillary Control register (Table 3.18-1) can be used to configure these pins as passive grounded outputs.

When each control bit is asserted HIGH, the corresponding I/O pin becomes a logic LOW output, but the associated internal functions otherwise associated with that pin are unaffected. If all three bits are asserted, the board is completely isolated from front-panel external system control functions and operates autonomously.

Table 3.18-1. Ancillary Control Register

Offset: 0060h **Default: 0000 0000**

Data Bit	Access Mode	Designation	Default	Function
D00	R/W	ISOLATE INPUT CLK IO PIN	0	When HIGH, configures the INPUT CLK I/O pin as a logic LOW output.
D01	RO	ISOLATE TRIGGER IO PIN	0	When HIGH, configures the TRIGGER I/O pin as a logic LOW output.
D02	RO	ISOLATE OUTPUT CLK IO PIN	0	When HIGH, configures the OUTPUT CLK I/O pin as a logic LOW output..
D03-D31	RO	(Reserved)	0h	---

3.19 Buffered Digital Outputs (BDO)

The eight buffered digital TTL output lines DIG OUT 00-07 are driven from a 256Kx8 FIFO buffer that is loaded from the Host Bus. ***Host access is by direct register-write, and DMA is not supported.*** Operation of the buffer is controlled through the BDO Buffer Control Register (Table 3.19-1). The output of the buffer is updated by a buffer clock that can be provided by any of three sources:

a. Internal BDO Rate generator.
b. External BDO hardware TTL clock input DIG OUT CLK INP.
c. Control bit BDO BUFFER CLOCK in the BDO Buffer Control register.

Table 3.19-1. BDO Buffer Control Register

Offset: 0054h **Default: 0003 FFFEh**

Bit	Mode	Designation	Default	Description
D00-19	RW	BDO THRESHOLD	3_FFFEh	Specifies the number of values in the Buffered Digital Outputs (BDO) output buffer above which the threshold flag is asserted HIGH.
D20	RW	CLEAR BDO BUFFER [1]	0	Clears (empties) the BDO Buffer.
D21	RW	ENABLE BDO BUFFER INPUTS [2]	0	Enables write-access to the BDO FIFO Buffer.
D22	RW	ENABLE BDO BUFFER CLOCKING [2]	0	Enables output clocking of the Buffer.
D23	RW	BDO SW BUFFER CLOCK [1,2]	0	The BDO buffer output advances one 8-bit value each time this bit is asserted HIGH.
D24	RO	BDO BUFFER THRESH FLAG [2]	0	HIGH when the number of values in the BDO Buffer exceeds the specified buffer threshold.
D25	RW	EXTERNAL BDO BUFFER CLOCK [2]	0	Selects the DIG OUT CLK INP I/O pin as the BDO buffer clock source when HIGH, or the internal BDO Rate generator when LOW.
D26	RW	ENABLE BDO RATE GENERATOR [2]	0	Enables the internal BDO rate generator.
D27	RW	PASSTHRU MODE	0	Selects the passthru (Direct-write) mode.
D28	RW	BUFFER UNDERFLOW	0	Indicates BDO buffer underflow.
D29	RW	BUFFER OVERFLOW	0	Indicates BDO buffer overflow.
D30-D31	RO	(Reserved)	0	---

[1] Clears automatically. [2] Ignored when PASSTHRU MODE is asserted.

3.19.1 Buffer Data Configuration

The BDO buffer is accessed through a single write-only register, with the least eight significant bits active and the remaining bits all-zero (Table 3.19-2). Logic polarity is maintained, in that a "one" written to a specific data bit in the buffer appears as a "one" when that bit is accessed at the output.

Table 3.19-2. BDO Output Buffer

Offset: 0058h **Default: N/A (Write-Only)**

Bit	Mode *	Designation	Description
D00	WO	DATA 00	Least significant data bit
D01-D06	WO	DATA 01 - DATA 06	Intermediate data bits
D07	WO	DATA 07	Most significant data bit
D08-D31	RO	---	Returns all-zero.

* WO indicates write-only access. Read-access returns all-zero value.

3.19.2 BDO Buffer Size Register

The number of occupied buffer locations is reported through the BDO Buffer Size register (Table 3.19-3). Each value in this register represents the number of 8-bit data fields contained in the buffer.

Table 3.19-3. BDO Buffer Size Register

Offset: 0050h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-D17	RO	BUFFER SIZE	0 0000h	Number of 8-bit values in the BDO Buffer
D18-D31	RO	(Inactive)	0	---

3.19.3 BDO Control

If the ENABLE BDO BUFFER CLOCKING control bit is HIGH, the output of the BDO buffer is advanced to the first or the next value by each buffer clock. Clearing this control bit disables output clocking from the buffer, but allows write access by the host. The remainder of this section assumes that this control bit is HIGH (clocking enabled).

NOTE: The first value loaded into an empty BDO buffer does not appear at the output until the first clock occurs. Subsequent values follow subsequent clocks.

If the Passthru mode is disabled (3.19.7), setting the BDO BUFFER CLOCK control bit HIGH in the BDO Buffer Control register advances the buffer output by one byte-wide value. This bit can be applied at any time that clocking is enabled, and overrides all other sources of clocking for the buffer. It is disabled in the Passthru mode.

If the EXTERNAL BDO BUFFER CLOCK control bit is LOW, an internal 24-Bit counter divides the master clock frequency to provide an output rate clock for the buffer. This internal 'BDO Rate' generator provides clocking rates from less than 3SPS up to approximately 5 Megasamples per second (1.0 Megasamples per second with external clocking). The default rate is 12.000KSPS.

Table 3.19-4. BDO Internal Rate Generator (BDO Rate)

Offset: 005Ch **Default: 0000_0D20h**

Data Bit	Mode	Designation	Description
D00	R/W	RATE 00	Least significant rate bit
D01-D22	R/W	RATE 01 - RATE 22	Intermediate rate bits
D23	R/W	RATE 23	Most significant rate bit
D24-D31	RO	---	Inactive. Returns all-zero.

If the EXTERNAL BDO BUFFER CLOCK control bit is HIGH, each TTL High-to-Low transition on the DIG OUT CLK INP I/O pin generates a single output clock. This input is edge-detected, and must have minimum HIGH and LOW durations of at least 100nS.

3.19.4 Buffer Threshold

To support data streaming to the buffer, the BDO THRESHOLD field can be adjusted to produce a status flag at any fill-value within the buffer's capacity of 256K samples. The BDO BUFFER THRESH FLAG is asserted HIGH if the buffer contents ***exceed*** the threshold value, and can be selected as an interrupt event on either the rising or falling edge of the flag.

3.19.5 Buffer Write Access

Host access to the buffer takes place through the BDO output buffer (Table 3.19.2). Transfers to the buffer are Longword single-writes to the buffer location at Offset 0x0058, and DMA is not supported. A buffer-read produces an all-zero value.

3.19.6 Underflow/Overflow Flags

The BUFFER UNDERFLOW flag reports a read from an empty buffer, and BUFFER OVERFLOW reports a write to a full buffer; both indicative of data loss. Once asserted, these flags can be cleared only (a) by initialization, (b) by a direct-write to the LOW state, or (c) by selecting the Passthru mode. They are unaffected by simply clearing the buffer.

3.19.7 Passthru Mode

Selecting the Passthru mode converts the BDO buffer port into a direct-write TTL output port, with each value written to the BDO Buffer appearing immediately at the output. The selection of this mode disables all other BDO control functions except BDO THRESHOLD and CLEAR BDO BUFFER.

NOTE: After initialization, setting the Passthru control bit HIGH makes Passthru access available immediately.

SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

Each of two analog input channels contains a selftest input switching network, a differential amplifier, a scaling network and a 16-Bit ADC (Figure 4.1-1), and provides input ranges of ±10V, ±5V and ±2.5V. A 2-Megasample FIFO buffer accumulates analog input data for subsequent retrieval through the PCI bus. Two 16-bit analog output channels provide software-selected output ranges of ±2.5V, ±5V or ±10V, and are accessed either directly through dedicated control registers, or through a 2-Megasample FIFO buffer. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller, and supports universal signaling. +5 VDC power from the PCI bus is converted into regulated power voltages for the internal analog networks.

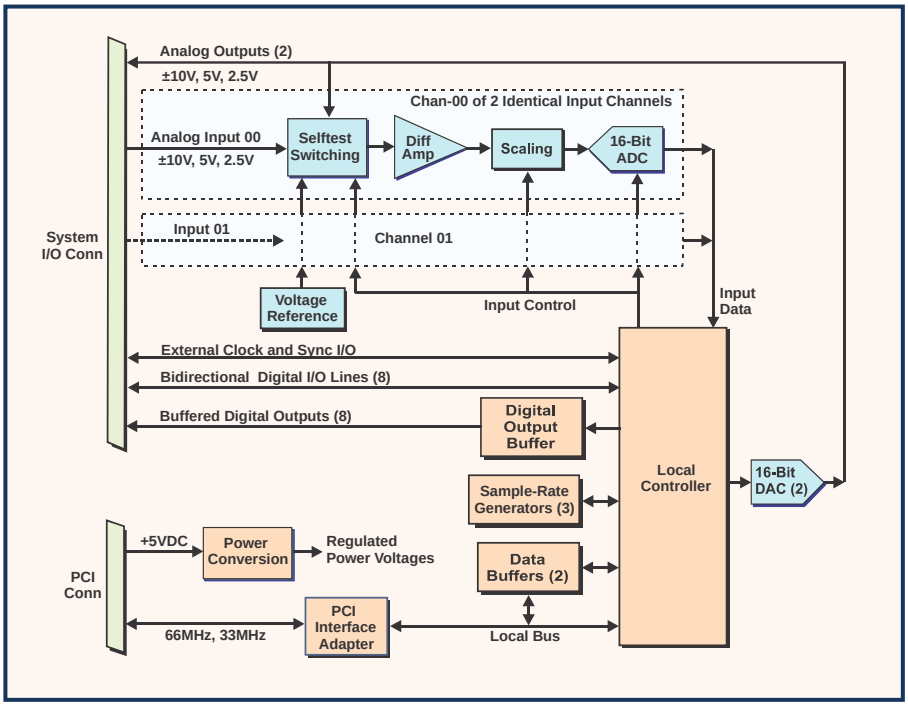


Figure 4.1-1. Functional Block Diagram

Selftest switches at the inputs provide test signals for autocalibration of all input and output channels, and can be configured to accept either differential or single-ended system inputs.

Analog input sampling and output clocking on multiple target boards can be synchronized to a single software-designated initiator board.

Two 8-bit digital I/O ports provide external TTL communication.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches shown in Figure 4.1-1. During normal operation, the 16-bit ADC's receive system analog input signals from the system I/O connector. For integrity testing and autocalibration operations, the internal voltage reference and the analog outputs can be routed through the selftest switches to the ADC's. An attenuator in each channel provides the necessary scaling for software-controlled input ranging.

Parallel data from each ADC is multiplexed into a continuous data stream within the local controller. The output of the data multiplexer passes through a digital processor that applies gain and offset correction values obtained during autocalibration. The corrected data is formatted, and the final processed and formatted data is loaded into the analog input data buffer.

ADC clocking can be supplied either from an internal 24-Bit rate generator, or from an external source. Triggered bursts can be acquired by using a second internal rate generator, or an external input as a trigger source. The burst block-size can be controlled by a 24-Bit counter, or sampling can be configured to operate continuously after a trigger. The ADC external clock and trigger pins can be configured independently as inputs or outputs.

4.3 Input Data Buffer

A 2-Megasample FIFO buffer accumulates analog input data for subsequent retrieval through the PCIbus. The buffer is supported by a 'size' register that tracks the number of values in the buffer, and by an adjustable threshold flag that generates a status flag in response to the number of samples contained within the buffer.

4.4 Analog Outputs

Two independent 16-bit DAC's are controlled either directly through dedicated control registers, or through a 2-Megasample FIFO buffer. The buffer can be operated either open for data streaming, or closed (circular) for periodic function generation. Function concatenation from the PCI bus is supported.

Output clocking can be supplied either from a third internal 24-Bit rate generator, or from an external source. Triggered bursts are supported, and share the triggering function with the analog inputs (4.2). The output burst size is controlled by a tag-bit attached to the last output value in a sequence. If the tag-bit is not attached, a burst will operate continuously after a trigger, or until the buffer goes empty.

4.5 Digital I/O Ports

Eight bidirectional TTL I/O lines provide register-direct communication between external devices and the host.

A second digital port consists of eight TTL output lines that are driven from a 256Kx8 FIFO buffer. The buffer is loaded from the host, and the contents of the buffer are clocked 8 bits wide to the I/O connector. Clocking can originate internally from the board or from an external TTL source.

4.6 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input and output channels to a single internal voltage reference. The utility can be invoked at any time by the control software.

The internal voltage reference is used to calibrate the span of each channel, and a zero-reference is used to calibrate the offset value. Correction values determined during autocalibration are applied to each digitized sample acquired during acquisition, and to each output value written to the DAC channels. Correction values are retained until the autocalibration sequence is repeated, or until power is removed.

4.7 Power Control

Regulated supply voltages of ±5 VDC and ±14 VDC are required for the analog networks, and are derived from the +5-Volt input provided by the PCI bus, both by switching preregulators and by linear postregulators.

APPENDIX A

LOCAL REGISTER QUICK REFERENCE

APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Status Registers

Offset (Hex)	Register	Mode	Default	Primary Function	Ref
0000	BOARD CONTROL	RW	2202 00A0h	Board Control Register (BCR).	3.2
0004	DIGITAL I/O PORT	RW	0000 00XXh	8-Bit Bidirectional Digital I/O port	3.9
0008	ANALOG OUTPUT CHAN 00	RW	0000 8000h	Output Channel 00 data.	3.12
000C	ANALOG OUTPUT CHAN 01	RW	0000 8000h	Output Channel 01 data.	
0010-0014	(Reserved)	RO	0000 0000h	---	---
0018	ANALOG INPUT BUFFER	RO	00XX XXXXh	Analog input buffer data.	3.4.5
001C	RATE GENERATOR A	RW	0000 007Eh	Rate-A generator divider; 24 bits.	3.7
0020	RATE GENERATOR B	RW	0000 2760h	Rate-B generator divider; 24 bits.	
0024	INPUT CONFIGURATION	RW	0300 0400h	Analog inputs channel-mask and burst-size.	3.4.2
0028	INPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the input buffer.	3.4.5.2
002C	INPUT BUFFER THRESHOLD	RW	001F FFFEh	Input buffer status flag threshold.	
0030	PRIMARY STATUS	RW	0000 0X00h	Principal status-flag register	3.11
0034	ASSEMBLY CONFIGURATION	RO	00XX XXXXh	Options and firmware revision.	3.16
0038	Autocal Values [2]	RW	0000 XXXXh	Autocal value readback.	---
003C	BUFFERED OUTPUT OPERATIONS	RW	0000 1043h	Buffered Analog Outputs Control	3.13.2.3
0040	OUTPUT BUFFER THRESHOLD	RW	001F FFFEh	Output buffer status flag threshold.	
0044	OUTPUT BUFFER SIZE	RO	0000 0000h	Number of data values in the output buffer.	
0048	ANALOG OUTPUT BUFFER	WO	0000 0000h	Analog Output Data Buffer.	3.13.2
004C	RATE GENERATOR C	RW	0000 007Eh	Rate-C generator divider; 24 bits.	3.13.4.1.2
0050	BDO BUFFER SIZE	RO	0000 0000h	Buffered Digital Outputs (BDO) Size (Number of bytes)	3.19
0054	BDO BUFFER CONTROL	RW	0001 FFFEh	BDO buffer controls and threshold	
0058	BDO OUTPUT BUFFER	WO	0000 0000h	BDO FIFO buffer.	
005C	BDO BUFFER RATE GENERATOR	RW	0000 0D20h	BDO clocking rate generator.	
0060	ANCILLARY CONTROL REGISTER	R/W	0000 0000h	Isolates clock and sync I/O lines.	3.18
0064-007C	(Reserved)	---	---	---	---

Notes: 1. RW = Read/Write, RO = Read-Only, WO = Write-Only.
2. Maintenance register; Shown for reference only.

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 2202 00A0h**

Bit	Mode [1]	Designation	Def	Description	Ref
D00-D02	RW	ANALOG INPUT MODE	0	Analog input mode: 0 => Differential system inputs 1 => Single-ended system inputs 2 => Zero selftest 3 => VREF selftest 4 => Output Channel 00 5 => Output Channel 01 6 => Output Channel 02 7 => Output Channel 03	3.4.1
D03	RW	ANALOG INPUTS AUTOCAL [2]	0	Initiates an analog-inputs autocalibration operation.	3.10
D04-D05	RW	INPUT CHANNEL 00 RANGE	2	Analog Input Channel-00 Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.4.3
D06-D07	RW	INPUT CHANNEL 01 RANGE	2	Analog Input Channel-01 Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	
D08	RW	INPUT S/W CLOCK [2]	0	Initiates a single sample of active input channels. Overrides existing input clocking source.	3.4.4
D09	RW	ENABLE INPUT BURST	0	Enables triggered burst input acquisition.	3.4.4.2
D10	RO	INPUT BURST BUSY	0	HIGH when a triggered input burst is in progress.	
D11	RW	INPUT S/W TRIGGER [2]	0	Initiates a single input data burst. Overrides existing burst triggering source.	
D12	RW	ENABLE INPUT BUFFER	0	Enables the analog input buffer for accepting data.	3.4.5.1
D13	RW	CLEAR INPUT BUFFER [2]	0	Clears (empties) the analog input data buffer.	
D14	RO	INPUT BUFFER THRESHOLD FLAG [3]	0	HIGH when the number of values in the input buffer exceeds the selected buffer threshold.	3.4.5.2
D15	RW	INPUT BUFFER OVERFLOW	0	Set HIGH if the input buffer overflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D16-D17	RW	OUTPUT RANGE	2	Analog Output Voltage Range: 0 => ±2.5V 2 => ±10V 1 => ±5V 3 => (Reserved)	3.12.1 3.13.1.3
D18	RW	SIMULTANEOUS OUTPUTS	0	When HIGH, all outputs update simultaneously in response to an output clock. When LOW, data is clocked to the outputs one channel at a time. Affects only buffered outputs.	3.12.2.2 3.13.4.2
D19	RW	ENABLE BUFFERED OUTPUTS	0	When HIGH, enables the analog output FIFO buffer, and disables the analog output registers ANALOG OUTPUT CHAN xx.	3.13
D20	RW	OUTPUT S/W CLOCK [2,3]	0	Produces a single analog output clock. Overrides existing output clocking source.	3.13.4.1
D21	RW	TRIGGER INITIATOR	0	Configures the shared analog input/output hardware trigger pin as an output if HIGH, or as an input if LOW.	3.4.4.2
D22	R/W	ENABLE RATE-C GENERATOR	0	Enables the Rate-C generator for analog outputs.	3.13.4.1.2
D23	R/W	INPUT BUFFER UNDERFLOW	0	Set HIGH if the input buffer underflows. Stays HIGH until cleared from the bus or by a board reset.	3.4.5.1
D24	RW	ANALOG INPUT CLK INITIATOR	0	Configures the analog input I/O clock as an *output* if HIGH, or as an *input* if LOW.	3.4.4
D25	RW	OFFSET BINARY	1	Selects offset-binary analog I/O data format when HIGH, or two's complement when LOW.	3.6
D26	RW	ENABLE RATE-A GENERATOR	0	Enables the Rate-A generator for analog inputs.	3.7
D27	RW	ENABLE RATE-B GENERATOR	0	Enables the Rate-B generator for triggered bursts.	
D28	RW	AUTOCAL [2]	0	Initiates an autocalibration operation when asserted. Clears automatically upon completion,	3.10
D29	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.	
D30	R/W	SWAP DEMAND MODE CHANNELS	0	Reverses the default demand-mode DMA channels for analog inputs and outputs	3.5 3.15
D31	RW	INITIALIZE [2]	0	Initializes the board. Sets all register defaults.	3.3.2

Notes: 1. RW = Read/Write, RO = Read-Only. 2. Clears automatically. 3. Duplicated elsewhere

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Table 3.4-1. Input Configuration Register

Offset: 0024h **Default: 0300 0400h**

Bit	Mode	Designation	Def	Description
D00-D23	RW	BURST BLOCK SIZE	0400h	Number of active channel sets acquired during a triggered burst.
D24	RW	ENABLE INPUT 00	1	Analog input channel selection mask.
D25	RW	ENABLE INPUT 01	1	
D26-D31	RW	(Reserved)	0	

* RW = Read/Write, RO = Read-Only.

Table 3.4-2. Input Data Buffer

Offset: 0018h **Default: 00XX XXXXh**

Bit Field	Designation	Description
D00	DATA00	Data value least significant bit (LSB)
D01-D14	DATA01 - DATA14	Data value intermediate bits
D15	DATA15	Data value most significant bit (MSB)
D16	FIRST-CHANNEL TAG	Tag assigned to first (lowest-numbered) active channel.
D17	END OF BURST (EOB)	Identifies the last input value in a burst.
D18-D31	(Reserved)	Always zero.

Table 3.4-3. Analog Input Buffer Threshold Register

Offset: 002Ch **Default: 001F FFFEh**

Bit	Mode	Designation	Default	Description
D00-D21	RW	ANALOG INPUT BUFFER THRESHOLD	1F_FFFEh	Specifies the number of values in the analog input buffer above which the threshold flag is asserted HIGH.
D22-23	RO	(Reserved)	0	---
D24	RO	ANALOG INPUT BUFFER THRESH FLAG	0	HIGH when the number of values in the analog input buffer exceeds the specified buffer threshold.
D25-D31	RO	Reserved	0	---

1. Duplicated in the BCR.

Table 3.5-1. Typical Input DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.5-2. Typical Input DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32)	0002 1943h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial (constant) local address	0000 0018h
90h	DMA Descriptor Counter	Transfer direction (Local bus to PCI bus)	0000 0008h
A8h (D7:0)	DMA Command/Status	Command and Status Register	01h, 03h (See Text)

* Determined by specific transfer requirements.

Table 3.7-1. Analog Input and Trigger Rate Generator Registers (A,B)

Offset: 001Ch (Rate-A), 0020h (Rate-B) Default: 0000 007E (Rate-A), 0000 2760h (Rate-B)

Data Field	Mode	Designation	Default	Description
D00-D23	R/W	Ndiv	---	Rate generator frequency control
D24-D31	RO	(Inactive)	0	---

Table 3.7-2. Input Rate Generator Frequency Selection

Ndiv		FREQUENCY Fgen (40 MHz Master Clock)*
(Dec)	(Hex)	(kHz)
20	0014	2000.00
21	0015	1904.76
---	---	Fgen (Hz) = Fclk (Hz) / Ndiv

* ±0.003 percent.

Table 3.9-1. Digital I/O Port Register

Offset: 0004h **Default: 0000 00XXh**

Data Field	Mode	Designation	Default	Description
D00-D07	RW	DIO PORT DATA[7..0]	XXh	System connector pins DIO 00 through DIO 07.
D08	RW	DIO PORT OUTPUT	0	Direction control for DIO BYTE 00. When LOW, DIO PORT DATA[] is an input field. When HIGH, DIO PORT DATA[] is an output field.
D09-D31	RO	(Reserved)	0h	Read back as all-zero.

Table 3.11-1 Primary Status Register

Offset 0x0030 **Default 0x0000 0X00**

Selection Bit [1]	Critical Event	Response Bit [2]	Reference Paragraph
D00	Autocal completed	D16	3.10
D01	Input Buffer threshold flag HIGH-to-LOW transition	D17	3.4.5.2
D02	Input Buffer threshold flag LOW-to-HIGH transition	D18	
D03	Input Buffer Overflow or Underflow	D19	3.4.5.1
D04	Analog Input Burst initiated (BURST BUSY LO-HI)	D20	3.4.4.2
D05	Analog Input Burst Completed (BURST BUSY HI-LO)	D21	
D06	BDO [3] Buffer threshold flag HIGH-to-LOW transition	D22	
D07	BDO [3] Buffer threshold flag LOW-to-HIGH transition	D23	
D08	Digital I/O Port DIO 00 LOW-to-HIGH transition	D24	3.9
D09	Output Buffer threshold flag HIGH-to-LOW transition	D25	3.13.2.3
D10	Output Buffer threshold flag LOW-to-HIGH transition	D26	
D11	Output Load-Ready Flag HIGH-to-LOW transition	D27	3.13.3.3
D12	Output Load-Ready Flag LOW-to-HIGH transition	D28	
D13	Analog Output Burst Ready	D29	3.13.5.2
D14	Output Buffer Overflow or Frame Overflow	D30	3.13.2.3 3.13.3.3
D15	(Reserved)	D31	---

1. Event selection. Enables assertion of the corresponding response bit when the selected event occurs.
2. Event response. Asserted HIGH when a selected event occurs. Remains HIGH until cleared LOW.
3. BDO = "Buffered Digital Outputs".

Table 3.12-1. Analog Output Channel Data Register

Offset: 0008h - 0014h **Default: 0000 8000h**

Data Field	Designation	Description
D00	DATA00	Data value least significant data bit
D01-D14	DATA01 - DATA14	Data value intermediate data bits
D15	DATA15	Data value most significant data bit
D16-D31	(Reserved)	Data in this field is ignored.

Table 3.12-2 Simultaneous Output Clock Source Selection

Register	Control Bit	S/W Clock (BCR)	Rate-C Gen	External Input
BCR	SIMULTANEOUS OUTPUTS	HIGH	HIGH	HIGH
	ENABLE RATE-C GENERATOR	X	HIGH	X
BOR *	ANALOG OUTPUT CLK INITIATOR	X	HIGH	LOW

* Buffered Outputs Operations register (Table 3.13-2).

Table 3.13-1. Summary of Output Control Parameters

Parameter	Mode	Description
Data Control	Active Channels; **Channel Group**	A single set of all active output channels constitutes an ***Active Channel Group***. Active channels are selected under a channel mask.
	Data Frame	All data values in the buffer comprise a *Data Fr*ame.
	Data Coding	Output data can be coded either in offset-binary format or in two's complement format.
Buffer Configuration	Open	Data read from the buffer is used and then discarded, until the buffer is empty.
	Circular (closed)	Data within the buffer is recirculated. Each value read from the output of the buffer FIFO is written back to the input of the FIFO. An end-of-frame (EOF) flag tracks the movement of data through the buffer.
Clock Source	External	External hardware provides the sample clock.
	Internal	The sample clock is provided by an internal rate generator, at a rate determined by the sample rate control register.
Clocking Mode	Simultaneous	At each clock occurrence, the next channel group (i.e.: a single group of all active channel values) in the output buffer is transferred to the respective analog output channels. All outputs are updated simultaneously.
	Sequential	At each clock occurrence, the next active channel value in the output buffer is transferred to the associated analog output channel, which is updated immediately.
Sampling Mode	Continuous	The contents of the output buffer are sampled continuously at the selected clock rate.
	Triggered Burst	A single data frame in the buffer is clocked to the outputs.

Table 3.13-2. Buffered Output Operations Register

Offset: 003Ch **Default: 0000_1043h**

Bit	Mode	Designation	Def	Description	Ref
D00	R/W	AO CHAN 00 ACTIVE	1	Active-channel mask for analog output channels. HIGH => Active; LOW => Inactive.	3.13.1.1
D01	R/W	AO CHAN 01 ACTIVE	1		
D02-D03	R/W	(Reserved)	0		
D04	R/W	ANALOG OUTPUT CLK INITIATOR	0	Selects the internal Rate-C generator for output clocking if HIGH, or the Output Clock I/O hardware input if LOW.	3.13.4.1
D05	R/W	ENABLE OUTPUT CLOCKING	0	Enables output clocking when HIGH. Disables clocking when LOW. Default is LOW (clocking disabled).	3.13.4
D06	RO	OUTPUT CLOCK READY	1	Indicates when HIGH that an output clock will be accepted. If LOW, indicates that the output will not respond to a clock.	
D07	R/W	OUTPUT SW CLOCK *	0	Produces a single output clock event when asserted. Independent of clocking mode. Duplicated in the BCR.	3.13.4.1
D08	R/W	CIRCULAR BUFFER	0	Selects circular buffer configuration if HIGH, or open self-flushing buffer configuration if LOW. Access for loading new data into the circular buffer must be requested by asserting LOAD REQUEST. Default is LOW; i.e. open buffer.	3.13.2.5
D09	R/W	LOAD REQUEST *	0	When set HIGH, requests loading access to the circular buffer. Initializes LOW.	3.13.3.3
D10	RO	LOAD READY	0	Set HIGH when the frame index passes through zero, if both CIRCULAR BUFFER and LOAD REQUEST are HIGH. When HIGH, indicates that the circular buffer is ready to accept new data. Available also in the PSR. Defaults HIGH.	
D11	R/W	CLEAR OUTPUT BUFFER *	0	Resets the output buffer to empty.	3.13.2.3
D12	RO	AO BUFFER EMPTY	1	Indicates the analog output buffer is empty.	
D13	RO	AO BUFFER THRESHOLD	0	Analog output buffer threshold flag. Duplicated in the AO Buffer Threshold register.	
D14	R/W	ENABLE ANALOG OUTPUTS	0	Enables the analog output drivers when HIGH. When LOW, the analog outputs are in a high-impedance state at zero-level.	3.12.1.1
D15	RO	AO BUFFER FULL	0	Indicates the output buffer is full.	3.13.2.3
D16	R/W	AO BUFFER OVERFLOW	0	Set HIGH when data is written to a full buffer. **	
D17	R/W	FRAME OVERFLOW	0	Set HIGH when data is written to a closed buffer. **	
D18	RO	BURST READY	0	If HIGH, indicates that a burst trigger will be accepted. If LOW, indicates that the output will not respond to a trigger.	3.13.5
D19	R/W	ENABLE OUTPUT BURST	0	Enables analog output burst operation.	3.13.5.2
D20	R/W	OUTPUT SW TRIGGER *	0	Produces a single output trigger event when asserted. Clears LOW automatically when the clock event is completed. Independent of triggering mode.	
D21	R/W	TRIG AI BURST ON AO	0	Synchronizes triggering of analog input bursts to analog output bursts.	3.17
D22-D31	RO	(Reserved)	0	Inactive. Returns all-zero.	---

* Clears LOW automatically when operation is completed.
** Remains HIGH until cleared by a direct write as LOW, or by initialization.

Table 3.13-3. Analog Output Buffer

Offset: 0048h **Default: N/A (Write-Only)**

Bit	Mode *	Designation	Description
D00	WO	DATA 00	Least significant data bit
D01-D14	WO	DATA 01 - DATA 14	Intermediate data bits
D15	WO	DATA 15	Most significant data bit
D16	WO	EOF FLAG	End-of-frame (EOF) flag.
D17-D31	WO	---	(Inactive)

* WO indicates write-only access. Read-access returns all-zero value.

Table 3.13-4. Output Buffer Size Register

Offset: 0044h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-D21	RO	BUFFER SIZE	00 0000h	Number of values in the analog output buffer
D22-D31	RO	(Inactive)	0	---

Table 3.13-5. Output Buffer Threshold Register

Offset: 0040h **Default: 001F FFFEh**

Bit	Mode	Designation	Default	Description
D00-D21	RW	OUTPUT BUFFER THRESHOLD	1F FFFEh	Specifies the number of values in the analog output buffer above which the threshold flag is asserted HIGH.
D22-23	RO	(Reserved)	0	---.
D24	RO	OUTPUT BUFFER THRESHOLD FLAG	0	HIGH when the number of values in the analog output buffer *exceeds* the specified buffer threshold.
D25-D31	RO	(Reserved)	0	---

Table 3.13-6. Output Sample Rate Control Register (Rate-C)

Offset: 004Ch **Default: 0000_007Eh**

Data Bit	Mode	Designation	Description
D00	R/W	RATE 00	Least significant rate bit
D01-D22	R/W	RATE 01 - RATE 22	Intermediate rate bits
D23	R/W	RATE 23	Most significant rate bit
D24-D31	RO	---	Inactive. Returns all-zero.

Table 3.13-7. Output Sample Rate Selection

Ndiv		FREQUENCY Fgen (40.32MHz Master Clock)*
(Dec)	(Hex)	(kHz)
20	0014	2016.00
21	0015	1919.04
---	---	Fclock (Hz) = Fclk (Hz) / Ndiv

* ±0.003 percent.

.

Table 3.15-1. Typical Output DMA Register Configuration; Block Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A0h	DMA Transfer Byte Count	Number of bytes in transfer	*
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

Table 3.15-2. Typical Output DMA Register Configuration; Demand Mode

PCI Offset	PCI Register	Function	Typical Value
94h	DMA Mode	Bus width (32)	0002 1943h
98h	DMA PCI Address	Initial PCI data source address	*
9Ch	DMA Local Address	Initial (constant) local address	0000 0048h
A4h	DMA Descriptor Counter	Transfer direction (PCI bus to Local bus)	0000 0000h
A9h (A8, D15:8)	DMA Command/Status	Command and Status Register	01h 03h (See Text)

* Determined by specific transfer requirements.

Table 3.16-1. Assembly Configuration Register

Offset: 0000 0034h **Default: 00XX XXXXh**

Bit Field	Description
D00-D11	Firmware Revision
D12-D15	(Reserved bit field; all-zero)
D16	Number of analog input channels: 0 => 2 Analog input channels. 1 => 1 Analog input channel.
D17	Number of analog output channels: 0 => 2 analog output channels. 1 => No analog outputs.
D18-D19	Master clock frequency: 0 => 40.320MHz 1 => (Reserved) 2 => (Reserved) 3 => (Reserved)
D20-D31	(Reserved bit field; returns all-zero).

Table 3.18-1. Ancillary Control Register

Offset: 0060h **Default: 0000 0000**

Data Bit	Access Mode	Designation	Default	Function
D00	R/W	ISOLATE INPUT CLK IO PIN	0	When HIGH, configures the INPUT CLK I/O pin as a logic LOW output.
D01	RO	ISOLATE TRIGGER IO PIN	0	When HIGH, configures the TRIGGER I/O pin as a logic LOW output.
D02	RO	ISOLATE OUTPUT CLK IO PIN	0	When HIGH, configures the OUTPUT CLK I/O pin as a logic LOW output..
D03-D31	RO	(Reserved)	0h	---

Table 3.19-1. BDO Buffer Control Register

Offset: 0054h **Default: 0001 FFFEh**

Bit	Mode	Designation	Default	Description
D00-19	RW	BDO THRESHOLD	3_FFFEh	Specifies the number of values in the Buffered Digital Outputs (BDO) output buffer above which the threshold flag is asserted HIGH.
D20	RW	CLEAR BDO BUFFER [1]	0	Clears (empties) the BDO Buffer.
D21	RW	ENABLE BDO BUFFER INPUTS [2]	0	Enables write-access to the BDO FIFO Buffer.
D22	RW	ENABLE BDO BUFFER CLOCKING [2]	0	Enables output clocking of the Buffer.
D23	RW	BDO SW BUFFER CLOCK [1,2]	0	The BDO buffer output advances one 8-bit value each time this bit is asserted HIGH.
D24	RO	BDO BUFFER THRESH FLAG [2]	0	HIGH when the number of values in the BDO Buffer exceeds the specified buffer threshold.
D25	RW	EXTERNAL BDO BUFFER CLOCK [2]	0	Selects the DIG OUT CLK INP I/O pin as the BDO buffer clock source when HIGH, or the internal BDO Rate generator when LOW.
D26	RW	ENABLE BDO RATE GENERATOR [2]	0	Enables the internal BDO rate generator.
D27	RW	PASSTHRU MODE	0	Selects the passthru (Direct-write) mode.
D28	RW	BUFFER UNDERFLOW	0	Indicates BDO buffer underflow.
D29	RW	BUFFER OVERFLOW	0	Indicates BDO buffer overflow.
D30-31	RO	(Reserved)	0	---

[1] Clears automatically. [2] Ignored when PASSTHRU MODE is asserted.

Table 3.19-2. BDO Output Buffer

Offset: 0058h **Default: N/A (Write-Only)**

Bit	Mode *	Designation	Description
D00	WO	DATA 00	Least significant data bit
D01-D06	WO	DATA 01 - DATA 06	Intermediate data bits
D07	WO	DATA 07	Most significant data bit
D08-D31	RO	---	Returns all-zero.

* WO indicates write-only access. Read-access returns all-zero value.

Table 3.19-3. BDO Buffer Size Register

Offset: 0050h **Default: 0000 0000h**

Data Bit	Mode	Designation	Default	Description
D00-D17	RO	BUFFER SIZE	0 0000h	Number of 8-bit values in the BDO Buffer
D18-D31	RO	(Inactive)	0	---

Table 3.19-4. BDO Internal Rate Generator (BDO Rate)

Offset: 005Ch **Default: 0000_0D20h**

Data Bit	Mode	Designation	Description
D00	R/W	RATE 00	Least significant rate bit
D01-D22	R/W	RATE 01 - RATE 22	Intermediate rate bits
D23	R/W	RATE 23	Most significant rate bit
D24-D31	RO	---	Inactive. Returns all-zero.

APPENDIX B

Migration From the PMC66-16AISS8AO4

Appendix B
Migration from PMC66-16AISS8AO4

Operation of the PMC66-16AISS2QAO2A2M is similar to that of the PMC66-16AISS8AO4. This appendix summarizes the principal similarities and differences between the two products, and is provided as a general guide rather than a definitive list of requirements.

B.1. Comparison of Features

Table B.1 provides a brief comparison of PMC66-16AI32SSC and PMC66-16AISS2AO2A2M features.

Table B.1. PMC66-16AISS8AO4, CCVPX-16AISS8AO4C Features Comparison

Feature	PMC66-16AISS8AO4	PMC66-16AISS8AO2A2M
Maximum Clocking Rates	2MSPS *inputs, 1MSPS outputs*	2MSPS *inputs, 2MSPS outputs*
Buffered Digital Outputs	None	8 Bits, 256K-Sample FIFO Buffer
Analog Outputs Disconnect	None	On-demand, and during power-up and Autocalibration
Input Channels	8 Differential	2 Differential
Output Channels	4 Single-ended	2 Single-ended
Conversion Resolution	16 Bits	
Input/Output Ranges	±10V, ±5V, ±2.5V	
Host Interface	PCI 2.3; D32; 33MHz/66MHz	
Master Clock	40.32MHz	

B.2. Migration Issues

General:

1. The system I/O connector pinout has changed.
2. Analog I/O reduced to two input channels and two output channels.
3. Analog Outputs can be clocked up to 2MSPS, and can be disconnected from the I/O connector.
4. The width of the bidirectional digital I/O port has been changed from 16 bits to eight.
5. Eight new TTL digital outputs are buffered through a 256Kx8 FIFO buffer.

Section 2.0. Installation and Maintenance:

Para 2.4.2: New section pertaining to the Buffered Digital Outputs.

Section 3.0. Control Software:

Table 3.1-1: Deleted 2 AO registers. Added 4 buffered DO registers Some defaults have changed.
Para 3.9: Width of DIO port has been reduced to eight.
Para 3.11: PSR: Replaced analog input and output clock events with BDO threshold events.
Para 3.13-2: Added control bit D14 'ENABLE ANALOG OUTPUTS'. (Used for outputs-disconnect).
Para 3.19: New section pertaining to operation of the buffered digital outputs.

The following tables have been modified to accommodate the larger analog I/O buffers and the increased analog output maximum clocking rate:

Table 3.4-1; Input Configuration Register
Table 3.4-3: Analog Input Buffer Threshold Register
Table 3.13-4: Output Buffer Size Register
Table 3.4-1: Output Buffer Threshold Register.

Revision History:

05-08-2017: Originated as Preliminary Draft.

05-18-2017: 3.14: Added Direct AO and Buffered AO typical sequence examples.

05-27-2017: Corrected title page.
3.19: Eliminated BDO DMA access. Reconfigured BDO control reg @ 0054h.
Added Passthru mode and Under/OverFlow flags.

06-06-2017: 3.9: Corrected data field width.
3.12: Reorganized section.
3.14: Revised examples section.

07-27-2017: Table 3.4-1: Updated default value.

8-28-2017: 3.19: Add Demand-mode DMA switch for AO and BDO.

07-31-2018: Para 3.10: Added comment.
Table 3.13-7:Updated.

08-16-2018: Para 1.1: Updated sample rate.
Para 2.3.1, 2.3.2.1, 4.4: Channel-count corrections.

08-27-2018: Removed 'Preliminary' status.
Para 3.19, Table 3.19-1. Removed DMA for buffered digital outputs.

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