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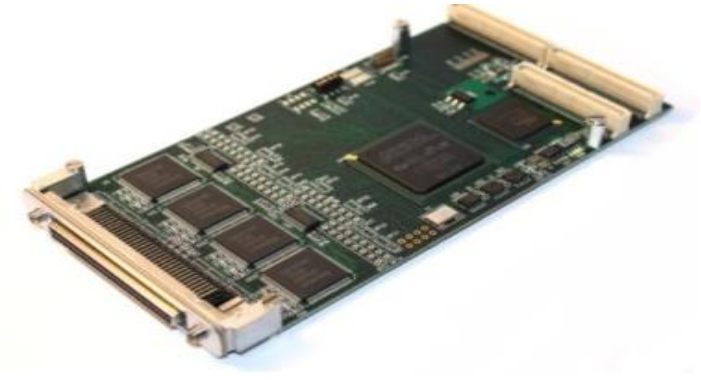
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PMC66-SIO4BXR-SYNC

Hardware User's Manual



HIGH SPEED
QUAD CHANNEL
SYNCHRONOUS SERIAL IO CONTROLLER
WITH DEEP TRANSMIT AND RECEIVE FIFOS
AND MULTIPROTOCOL TRANSCEIVERS

RS-485
RS-422 / V.11
RS-423 / V.10
RS-232 / V.28

General Standards Corporation
8302A Whitesburg Drive
Huntsville, AL 35802
Phone: (256) 880-8787
Fax: (256) 880-8788
URL: www.generalstandards.com
E-mail: techsupport@generalstandards.com

Revision 3

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PREFACE

Revision History

1. Rev NR – Mar 2011 – Original rev from PMC66-SIO4BXR-SYNC manual.
2. Rev 1 – Mar 2013
3. Rev 2 – Jun 2014 – Add PinSrc B (Pulse/Delay)
4. Rev 3 – Aug 2014 – Add Rx Bit Size and Timestamp

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8302A Whitesburg Drive
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(EIA order number EIA-RS-422A)

EIA-485 – Standard for Electrical Characteristics of Generators and Receivers for Use in Balanced Digital Multipoint Systems
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PCI Local Bus Specification Revision 2.2 December 18, 1998.

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TABLE OF CONTENTS

CHAPTER 1: INTRODUCTION 1

1.0 General Description 1
1.1 Serial Interface 2
1.1.1 Three Signal Serial Interface 2
1.1.2 Two Signal Serial Interface 3
1.2 Deep Transmit/Receive FIFOs 3
1.3 Multiprotocol Transceivers 3
1.4 PMC/PCI Interface 4
1.5 General Purpose IO 4
1.6 Connector Interface 4
1.7 Timestamp 4
1.8 Standard Channels 4

CHAPTER 2: LOCAL SPACE REGISTERS 5

2.0 GSC Firmware (Local Space) Registers 5
2.1 Firmware Revision: Local Offset 0x0000 6
2.2 Board Control: Local Offset 0x0004 6
2.3 Board Status: Local Offset 0x0008 7
2.4 TimeStamp: Local Offset 0x000C 8
2.5 Channel TX Almost Flags: Local Offset 0x0010 / 0x0020 / 0x0030 / 0x0040 8
2.6 Channel Rx Almost Flags: Local Offset 0x0014 / 0x0024 / 0x0034 / 0x0044 8
2.7 Channel FIFO: Local Offset 0x0018 / 0x0028 / 0x0038 / 0x0048 9
2.8 Channel Control/Status: Local Offset 0x001C / 0x002C / 0x003C / 0x004C 9
2.9 Interrupt Registers 11
2.8.1 Interrupt Control: Local Offset 0x0060 12
2.8.2 Interrupt Status/Clear: Local Offset 0x0064 12
2.8.3 Interrupt Edge/Level: Local Offset 0x0068 12
2.8.4 Interrupt Hi/Lo: Local Offset 0x006C 12
2.10 Channel Pin Source B: Local Offset 0x0070 / 0x0074 / 0x0078 / 0x007C 12
2.11 Channel Pin Source: Local Offset 0x0080 / 0x0084 / 0x0088 / 0x008C 13
2.12 Channel Pin Status: Local Offset 0x0090 / 0x0094 / 0x0098 / 0x009C 15
2.13 Programmable Clock Registers: Local Offset 0x00A0 / 0x00A4 / 0x00A8 15
2.14 Tx Bit Register: Local Offset 0x00B0 / 0x00B4 / 0x00B8 / 0xBC 15
2.15 Rx Bit Register: Local Offset 0x00C0 / 0x00C4 / 0x00C8 / 0xCC 15
2.16 FIFO Count Register: Local Offset 0x00D0 / 0x00D4 / 0x00D8 / 0x00DC 16
2.17 FIFO Size Register: Local Offset 0x00E0 / 0x00E4 / 0x00E8 / 0x00EC 16
2.18 FW Type ID Register: Local Offset 0x00F8 16
2.19 Features Register: Local Offset 0x00FC 17

CHAPTER 3: PROGRAMMING 18

3.1 Serial Interface 18
3.1.1 Serial Interface Definition 18
3.1.2 Two Signal Interface 18
3.1.3 Tx Word Bit Size / Tx Gap 18
3.1.4 Rx Word Bit Size / Rx Bit Count 19
3.2 FIFOs 19
3.2.1 FIFO Flags 19

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3.2.2 FIFO COUNTERS 20
3.2.3 FIFO SIZE 20
3.3 BOARD VS. CHANNEL REGISTERS 20
3.4 PROGRAMMABLE OSCILLATOR / PROGRAMMABLE CLOCKS 21
3.5 MULTIPROTOCOL TRANSCEIVER CONTROL 21
3.6 DCE/DTE MODE 21
3.7 LOOPBACK MODES 21
3.8 TIMESTAMP 22
3.9 FRAME VALID PULSE / DELAY MODE 22
3.10 GENERAL PURPOSE IO 22
3.11 INTERRUPTS 23
3.10 PCI DMA 23

CHAPTER 4: PCI INTERFACE 24

4.0 PCI INTERFACE REGISTERS 24
4.1 PCI REGISTERS 24
4.1.1 PCI CONFIGURATION REGISTERS 24
4.1.2 LOCAL CONFIGURATION REGISTERS 25
4.1.3 RUNTIME REGISTERS 25
4.1.4 DMA REGISTERS 25
4.1.4.1 DMA CHANNEL MODE REGISTER: (PCI 0X80 / 0X94) 25

CHAPTER 5: HARDWARE CONFIGURATION 26

5.0 BOARD LAYOUT 26
5.1 BOARD ID JUMPER J5 27
5.2 TERMINATION RESISTORS 27
5.3 LEDS 27
5.4 INTERFACE CONNECTOR 28

CHAPTER 6: ORDERING OPTIONS 30

6.0 ORDERING INFORMATION 30
6.1 INTERFACE CABLE 30
6.2 DEVICE DRIVERS 30
6.3 CUSTOM APPLICATIONS 30

APPENDIX A: PROGRAMMABLE OSCILLATOR PROGRAMMING 31

APPENDIX B: FIRMWARE REVISIONS / FEATURES REGISTER 34

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CHAPTER 1: INTRODUCTION

1.0 General Description

The General Standards PMC66-SI04BXR-SYNC board provides four, high-speed synchronous serial interface channels for PMC applications. The SIO4BXR-SYNC combines a flexible serial/parallel converter, deep FIFO data buffers, and multiprotocol transceivers in four fully independent synchronous serial IO channels. These features, along with four programmable baud rate generators and a high performance PMC/PCI interface engine, give the PMC66-SIO4BXR-SYNC unsurpassed performance in a synchronous serial interface card.

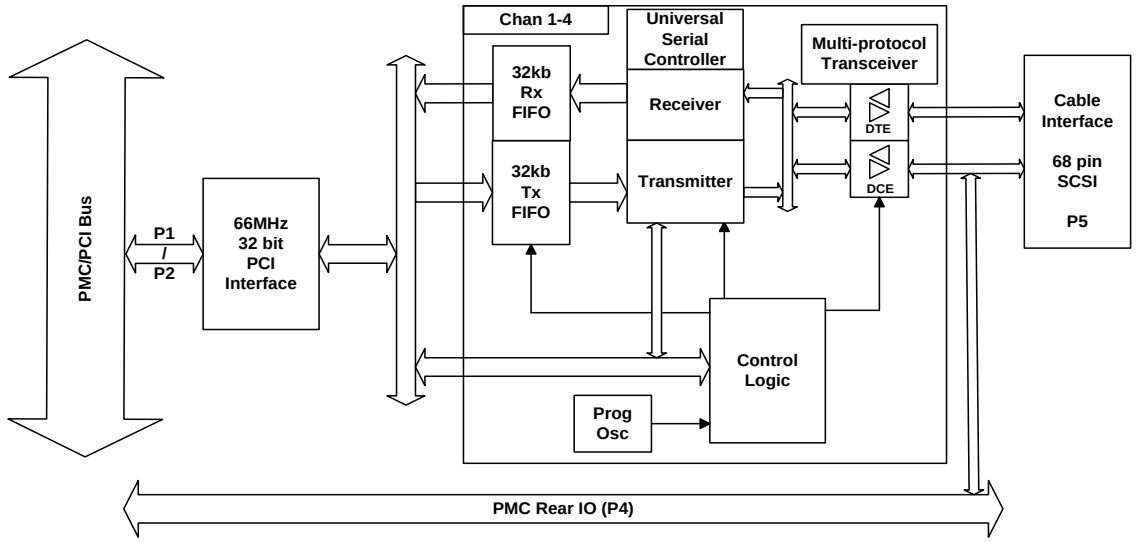


Figure 1-1 Block Diagram of PMC66-SIO4BXR-SYNC

- Four Independent Multi-Protocol Serial Channels
- Independent Transmit and Receive FIFOs for each Serial Channel – 32K byte each
- Multi-protocol Transceivers support RS422/RS485, RS232, RS423
- Fast RS422/RS485 Differential Cable Transceivers Provide Data Rates up to 10Mbps
- RS423 and RS232 Cable Transceivers Provide Data Rates up to 230kbps
- Two Signal (Clock/Data) or Three Signal modes (Clock/Data/Data Valid)
- Each Channel may be configured as standard PMC66-SIO4BXR channel
- Programmable Oscillators provide increased flexibility for Baud Rate Clock generation
- Programmable Transmit Bit Counts allow for various transmit word lengths
- Programmable Transmit Gap Bit Counts allow for variable gap between words
- Fully Programmable Polarity on all signals
- Eight signals per channel, configurable as either DTE or DCE:
  3 Serial Clocks (TxC,RxC,AuxC), 2 Serial Data (TxD,RxD), 2 Data Valid (TxE,RxE), plus Spare
- Unused signals may be reconfigured as General Purpose IO
- SCSI type 68 pin front edge I/O Connector
- Standard Cable to four DB25 connectors and Custom Cables available
- Interchangeable 120Ω Termination Resistors (RS422/RS485 Mode)
- Available drivers include VxWorks, WinNT, Win2k, WinXP, Linux, and Labview
- Industrial Temperature Option Available
- May be mounted on various adapters to fit PCI, PCIe, PXI, and cPCI form factors

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1.1 Serial Interface

The simple synchronous interface may be configured as a three signal interface - Clock, Data, and Envelope (Data Valid), or an even simpler two signal interface – Clock and Data. The SIO4BXR-SYNC allows the serial interface to be further customized with the following user configurable options:

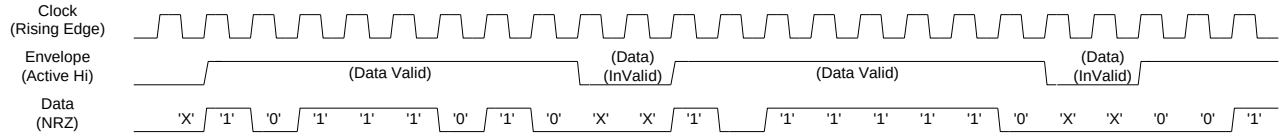
- Clocking Data on either rising or falling edge of the clock.
- Active Hi or Active Lo polarity for the Envelope Signal
- NRZ (Level) or NRZB (Inverted Level) Data Encoding
- Continuous Transmit Clock or Transmit Clock disabled when Data is invalid (Clock present only for valid Data).
- Transmit Word Size may be configured from 1 to 64k bits (consecutive bit count).
- Transmit Gap Size (number of clocks between transmit words) may be configured from 0 to 64k bits.
- Data may be transmitted MSB first or LSB first (8-bit or less word size).
- Transmit Clock may be configured from 10MHz down to 400Hz on a per channel basis.
- Auxiliary Clock Input from cable may be used as Transmit Clock.

The following sections show some typical examples of how the SIO4BXR-SYNC can be configured to support different two and three signal interfaces.

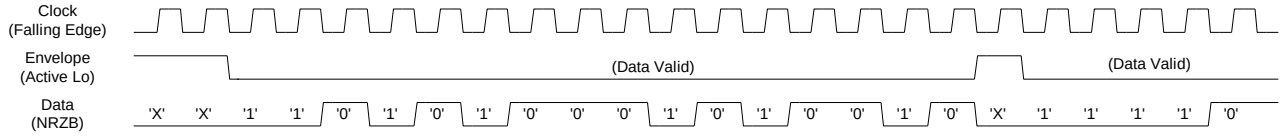
1.1.1 Three Signal Serial Interface

Figure 1-2 shows two examples of typical 3-signal interfaces. The two diagrams show how the card can be configured to handle different interface requirements. For the top diagram, Data and Envelope change on the rising edge of the Clock. The Data and Envelope are both Active Hi. The Clock is continuous – e.g. the Clock continues even when Data is Invalid (TxC Idl). Data is transmitted in 8 bit words (TxBitSiz), with a two Clock 'gap' (TxGap) in between each word (Data Valid for 8 bits, Invalid for 2).

In the lower example, Data and Envelope change on the falling edge of the Clock. The Data and Envelope signals are both Active Lo. The Clock is still continuous – Clock continues even when Data is Invalid (TxC Idl). Data is transmitted in 16 bit words (TxBitSiz), with a one Clock 'gap' (TxGap) in between each word (Data Valid for 16 bits, Invalid for 1).



TxCount = 8, TxGap = 2, TxC Idl = 0



TxCount = 16, TxGap = 1, TxC Idl = 0

Figure 1-2 Three Signal Serial Interface

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1.1.2 Two Signal Serial Interface

Figure 1-3 shows how the Clock can be used to qualify the Data to give a two signal serial interface. In this case, Data is considered valid at every Clock. In this example, Data is Active Hi and changes on the rising edge of the Clock. The Clock is not present when Data is invalid (TxC Idl). Data is transmitted in 8 bit words (TxBitSiz), with a two clock 'gap' (TxGap) in between each word (Data Valid for 8 bits, Invalid for 2).

In the lower example, Data and Envelope change on the falling edge of the Clock. The Data and Envelope signals are both Active Lo. The clock is still continuous – Clock continues even when Data is Invalid (TxC Idl). Data is transmitted in 16 bit words (TxBitSiz), with a one Clock 'gap' (TxGap) in between each word (Data Valid for 16 bits, Invalid for 1).

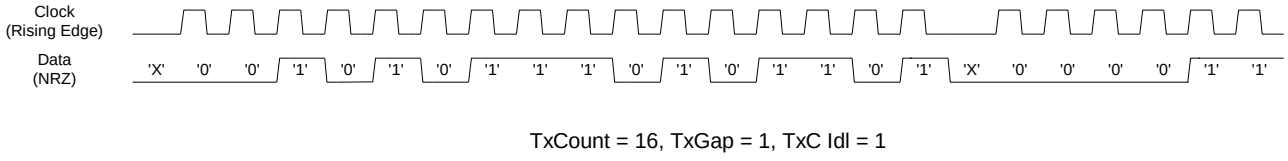


Figure 1-3 Two Signal Serial Interface

1.2 Deep Transmit/Receive FIFOs

Data is transferred to/from the serial interface through Transmit and Receive FIFOs. Each of the four serial channels has an independent Transmit FIFO and a Receive FIFO for a total of eight separate on-board FIFOs. These FIFOs can vary from 4k bytes to 32k bytes (based on ordering option). FIFOs allow data transfer to continue to/from the IO interface independent of PCI interface transfers and software overhead. The required FIFO size may depend on several factors including data transfer size, required throughput rate, and the software overhead (which will also vary based on OS). Generally, faster baud rates (greater than 500kbps) will require deeper FIFOs. Deeper FIFOs help ensure no data is lost for critical systems.

The SIO4BXR provides access to complete FIFO status to optimize data transfers. In addition to Empty and Full indicators, each FIFO has a programmable Almost Empty Flag and a programmable Almost Full Flag. These FIFO flags may be used as interrupt sources to monitor FIFO fill levels. In addition, real-time FIFO counters showing the exact number of words in the FIFO are also provided for each FIFO. By utilizing these FIFO counters, data transfers can be optimized to efficiently send and receive data.

1.3 Multiprotocol Transceivers

The SIO4BXR data is transferred over the user interface using high-speed multiprotocol transceivers. These multiprotocol transceivers are software selectable as RS422/RS485, RS423, or RS232 on a per channel basis. Each channel direction may also be configured as DTE or DCE configuration. This allows for either full duplex or half duplex configurations.

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1.4 PMC/PCI Interface

The control interface to the SIO4BXR-SYNC is through the PMC/PCI interface. An industry standard PCI9056 bridge chip from PLX Technology is used to implement PCI Specification 2.2. The PCI9056 provides the 32bit, 66MHz (264MBit/sec) interface between the PCI bus and the Local 32 bit bus. It also provides for high-speed DMA transfers to efficiently move data to and from the board.

1.5 General Purpose IO

Since some signals may not be used in all applications, the SIO4BXR provides the flexibility to remap unused signals to be used as general purpose IO. For example, this would allow support for an application requiring DTR/DSR signals to be implemented on an unused DCD or TxAuxC signals. This also allows signals from unused channels to be available as general purpose IO.

1.6 Connector Interface

The SIO4BXR provides a user IO interface through a front-side card edge connector. All four serial channels interface through this high-density, 68 pin SCSI-3 type connector, and are grouped to simplify separating the cable into four distinct serial connectors.

Standard cables are available from General Standards in various lengths to adapt the single 68 pin SCSI-3 connector into four DB25 connectors (one per channel). A standard cable is also available with a single 68 pin SCSI-3 connector on one end and open on the other. This allows the user to add a custom connector (or connect to a terminal block). General Standards will also work with customers to fabricate custom cables. Consult factory for details on custom cables.

1.7 Timestamp

The timestamp feature allows a relative 24-bit timestamp to be recorded along with the received data stream. The timestamp can be recorded at the start of a frame or with each received word. The timestamp uses an internal 100us clock and reset, or can use a user input clock and/or reset via the user connector. If external connections are used, the timestamp will clock on the external rising clock edge and reset when external reset =1. The signals can be inverted if necessary by reversing the +/- connections (RS422). The timestamp feature has been added with firmware version v41D (v11D).

1.8 Standard Channels

The PMC66-SIO4BXR-SYNC has been upgraded to also support the standard serial protocols utilizing the Zilog Z16C30 Universal Serial Controller (USC) of our PMC66-SIO4BXR board on a channel by channel basis. Since this is a relatively new feature, please check with General Standards for driver support of this feature.

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CHAPTER 2: LOCAL SPACE REGISTERS

2.0 GSC Firmware (Local Space) Registers

The PMC66-SIO4BXR-SYNC is accessed through two sets of registers – PCI Registers and GSC Firmware Registers. The GSC Firmware Registers (referred to as Local Space Registers), which provide the control/status for the SIO4BXR-SYNC board, are described below. The PCI registers (internal to the PLX 9056 PCI controller) are discussed in Chapter 3.

Offset Address	Size	Access*	Register Name	Default Value (Hex)
0x0000	D32	Read Only	Firmware Revision	E22404XX
0x0004	D32	Read/Write	Board Control	00000000
0x0008	D32	Read Only	Board Status	000001XX
0x000C	D32	Read Only	Timestamp	00000000
0x0010	D32	Read/Write	Ch 1 Tx Almost Full/Empty	00070007
0x0014	D32	Read/Write	Ch 1 Rx Almost Full/Empty	00070007
0x0018	D32	Read/Write	Ch l Data FIFO	000000XX
0x001C	D32	Read/Write	Ch 1 Control/Status	0000CC00
0x0020	D32	Read/Write	Ch 2 Tx Almost Full/Empty	00070007
0x0024	D32	Read/Write	Ch 2 Rx Almost Full/Empty	00070007
0x0028	D32	Read/Write	Ch 2 Data FIFO	000000XX
0x002C	D32	Read/Write	Ch 2 Control/Status	0000CC00
0x0030	D32	Read/Write	Ch 3 Tx Almost Full/Empty	00070007
0x0034	D32	Read/Write	Ch 3 Rx Almost Full/Empty	00070007
0x0038	D32	Read/Write	Ch 3 Data FIFO	000000XX
0x003C	D32	Read/Write	Ch 3 Control/Status	0000CC00
0x0040	D32	Read/Write	Ch 4 Tx Almost Full/Empty	00070007
0x0044	D32	Read/Write	Ch 4 Rx Almost Full/Empty	00070007
0x0048	D32	Read/Write	Ch 4 Data FIFO	000000XX
0x004C	D32	Read/Write	Ch 4 Control/Status	0000CC00
0x0050-0x005C	---	--	RESERVED	--------
0x0060	D32	Read/Write	Interrupt Control	00000000
0x0064	D32	Read/Write	Interrupt Status/Clear	00000000
0x0068	D32	Read Only	Interrupt Edge/Level	FFFFFFFF
0x006C	D32	Read/Write	Interrupt High/Low	FFFFFFFF
0x0070	D32	Read/Write	Ch 1Pin Source B	00000000
0x0074	D32	Read/Write	Ch 2 Pin Source B	00000000
0x0078	D32	Read/Write	Ch 3 Pin Source B	00000000
0x007C	D32	Read/Write	Ch 4 Pin Source B	00000000
0x0080	D32	Read/Write	Ch 1Pin Source	00000020
0x0084	D32	Read/Write	Ch 2 Pin Source	00000020
0x0088	D32	Read/Write	Ch 3 Pin Source	00000020
0x008C	D32	Read/Write	Ch 4 Pin Source	00000020
0x0090	D32	Read Only	Ch 1Pin Status	000000XX
0x0094	D32	Read Only	Ch 2 Pin Status	000000XX
0x0098	D32	Read Only	Ch 3 Pin Status	000000XX
0x009C	D32	Read Only	Ch 4 Pin Status	000000XX
0x00A0	D32	Read/Write	Prog Osc RAM Addr	00000000
0x00A4	D32	Read/Write	Prog Osc RAM Data (Ch 1-3)	00000000
0x00A8	D32	Read/Write	Prog Osc Control/Status	00000000
0x00AC	D32	Read/Write	Prog Osc RAM Data (Ch 4)	00000000

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0x00B0	D32	Read/Write	Ch1 Tx Bit Size / Tx Gap	00000000
0x00B4	D32	Read/Write	Ch2 Tx Bit Size / Tx Gap	00000000
0x00B8	D32	Read/Write	Ch3 Tx Bit Size / Tx Gap	00000000
0x00BC	D32	Read/Write	Ch4 Tx Bit Size / Tx Gap	00000000
0x00C0	D32	Read/Write	Ch1 Rx Bit Size / Rx Bit Count	00000000
0x00C4	D32	Read/Write	Ch2 Rx Bit Size / Rx Bit Count	00000000
0x00C8	D32	Read/Write	Ch3 Rx Bit Size / Rx Bit Count	00000000
0x00CC	D32	Read/Write	Ch4 Rx Bit Size / Rx Bit Count	00000000
0x00D0	D32	Read Only	Ch1 FIFO Count	00000000
0x00D4	D32	Read Only	Ch2 FIFO Count	00000000
0x00D8	D32	Read Only	Ch3 FIFO Count	00000000
0x00DC	D32	Read Only	Ch4 FIFO Count	00000000
0x00E0	D32	Read Only	Ch1 FIFO Size	XXXXXXXX
0x00E4	D32	Read Only	Ch2 FIFO Size	XXXXXXXX
0x00E8	D32	Read Only	Ch3 FIFO Size	XXXXXXXX
0x00EC	D32	Read Only	Ch4 FIFO Size	XXXXXXXX
0x00F0-0x00F4	---	--	RESERVED (Test)	--------
0x00F8	D32	Read/Write	FW Type Register	04040404
0x00FC	D32	Read Only	Features Register	00F979F4

2.1 Firmware Revision: Local Offset 0x0000

The Firmware ID register provides version information about the firmware on the board. This is useful for technical support to identify the firmware version.

D31:16	HW Board Rev	0xE225	PMC66-SIO4BXR Rev E
D15:8	Firmware Type ID	0x04	Sync Firmware
D7:0	Firmware Revision	XX	Firmware Version (

2.2 Board Control: Local Offset 0x0004

The Board Control Register defines the general control functions for the board. The main function in this register defines the Demand mode DMA channel requests.

D31 Board Reset
1 = Reset all Local Registers and FIFOs to their default values
Notes: This bit will automatically clear to 0 following the board reset.
Board Reset will NOT reset programmable oscillator.
Following a Board Reset, ResetInProgress bit (D31) of the Board Status Register will remain set until the Board reset is complete;

D30 RESERVED (Debug Test)

D29 RESERVED (Debug Test)

D28:27 RESERVED (FIFO Config)

D26 LED D2
1 = Turn on green LED D2

D25 LED D3
1 = Turn on green LED D3

D24 LED D4
1 = Turn on green LED D4

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D23	TimeStamp Reset 1 = Reset Timestamp to 0 **Notes:** This timestamp reset can be asserted regardless of Timestamp source.
D22:20	TimeStamp Source 000 = Internal 1us Clock / Internal Reset 001 = External Clock AuxC4 / Internal Reset 010 = External Clock DCD4 / Internal Reset 100 = Internal 1us Clock / External Reset DCD4 101 = External Clock AuxC4 / External Reset DCD4 110 = External Clock DCD4 / External Reset DCD3
D19:D9	RESERVED
D8	Rx FIFO Stop on Full 1 = If Rx FIFO becomes full, stop receiving data (disable receiver).
D7	Demand Mode DMA Channel 1 Single Cycle Disable
D6:4	Demand Mode DMA Channel 1 Request 000 = Ch1 Rx 100 = Ch1 Tx 010 = Ch2 Rx 110 = Ch2 Tx 001 = Ch3 Rx 101 = Ch3 Tx 011 = Ch4 Rx 111 = Ch4 Tx
D3	Demand Mode DMA Channel 0 Single Cycle Disable
D2:0	Demand Mode DMA Channel 0 Request 000 = Ch1 Rx 100 = Ch1 Tx 010 = Ch2 Rx 110 = Ch2 Tx 001 = Ch3 Rx 101 = Ch3 Tx 011 = Ch4 Rx 111 = Ch4 Tx

2.3 Board Status: Local Offset 0x0008

The Board Status Register gives general overall status for a board. The Board Jumpers (D1:D0) are physical jumpers which can be used to distinguish between boards if multiple SIO4 boards are present in a system.

D31:D9	RESERVED
D8	0 = Standard **1** = Sync
D7	**0** = Standard 1 = External Timetag Option
D6	**0** - Standard PCB 1 - L3RIO PCB
D5:D4	FIFO Size 00 = 48KLC 01 = 64K 10 = 256K

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D3:D0	Board Jumper (J5)
D3	Board ID4 0=J5:7-J5:8 jumper installed
D2	Board ID3 0=J5:5-J5:6 jumper installed
D1	Board ID2 0=J5:3-J5:4 jumper installed
D0	Board ID1 0=J5:1-J5:2 jumper installed

2.4 TimeStamp: Local Offset 0x000C

The TimeStamp Register is a 32-bit counter to allow a relative time to be recorded along with received data. Although the timestamp register is a 32 bit register, only the lower 24 bits are recorded in the received data stream. The Timestamp clock and reset source may be internal or external (Board Control Reg D22:D20). The Receive TimeStamp is enabled for each channel in the Channel Control/Status Register (D3:D2).

D31:24	TimeStamp Upper Byte (not recorded)
D23:0	TimeStamp (1us resolution)

2.5 Channel TX Almost Flags: Local Offset 0x0010 / 0x0020 / 0x0030 / 0x0040

The Tx Almost Flag Registers are used to set the Almost Full and Almost Empty Flags for the transmit FIFOs. The Almost Full/Empty Flags may be read as status bits in the Channel Control/Status Register, and are also edge-triggered interrupt sources to the Interrupt Register.

D31:16	TX Almost Full Flag Value Number of words from FIFO Full when the Almost Full Flag will be asserted (i.e. FIFO contains {FIFO Size – Almost Full Value} words or more.)
D15:0	TX Almost Empty Flag Value Number of words from FIFO Empty when the Almost Empty Flag will be asserted.

2.6 Channel Rx Almost Flags: Local Offset 0x0014 / 0x0024 / 0x0034 / 0x0044

The Rx Almost Flag Registers are used to set the Almost Full and Almost Empty Flags for the transmit FIFOs. The Almost Full/Empty Flags may be read as status bits in the Channel Control/Status Register, and are also edge-triggered interrupt sources to the Interrupt Register.

D31:16	RX Almost Full Flag Value Number of words from FIFO Full when the Almost Full Flag will be asserted (i.e. FIFO contains {FIFO Size – Almost Full Value} words or more.)
D15:0	RX Almost Empty Flag Value Number of words from FIFO Empty when the Almost Empty Flag will be asserted

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2.7 Channel FIFO: Local Offset 0x0018 / 0x0028 / 0x0038 / 0x0048

The Channel FIFO Register passes serial data to/from the serial controller. The same register is used to access both the Transmit FIFO (writes) and Receive FIFO (reads).

D31:9 RESERVED
D8 Timestamp Flag (Rx Only)
D7:0 Channel FIFO Data

2.8 Channel Control/Status: Local Offset 0x001C / 0x002C / 0x003C / 0x004C

The Channel Control/Status Register provides the reset functions and data transceiver enable controls, and the FIFO Flag status for each channel.

D31 RESERVED

D30:24 Channel Control Bits

D30 Receive Gap Enable
0 = Bit D24 (Receiver Enable) controls when data reception starts.
1 = Data reception will begin when D24=1 and RxE is negated. This waits for a gap in the data stream before data reception begins.

D29 Receive Bit Count Reset
1 = Reset Receive Bit Counter

D28 Transmit MSB/LSB
0 = Transmit MSB first (default)
1 = Transmit LSB first

D27 Receive MSB/LSB
0 = Receive MSB first (default)
1 = Receive LSB first

D26 Stop Transmit On FIFO Empty
0 = Transmitter remains enabled under software control (D17)
1 = Transmitter will be disabled (D25 = '0') if Tx FIFO becomes empty

D25 Transmit Enable
1 = Transmitter enabled. Note that cable transceiver direction should be set and transceivers enabled before the Transmit Enable is set.

D24 Receive Enable
1 = Receiver enabled. Note that cable transceiver direction should be set and transceivers enabled before the Receive Enable is set.

D23:20 LED Control
Each Channel controls 2 LEDs on the back of the PCB. See Section 5.3 for more detailed information about the LEDs.

D19 Rx Stop on Full

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D18:8 Channel Status Bits

D18	Rx FIFO Underflow	
D17	Tx FIFO Overflow (Latched)	
D16	Rx FIFO Overflow (Latched)	
	1= Rx Data was lost due to Rx Overflow.	
	Note: This bit is latched. Write D16=1 to clear.	
D15	Rx FIFO Full Flag Lo	(0 = Rx FIFO Full)
D14	Rx FIFO Almost Full Flag Lo	(0 = Rx FIFO Almost Full)
D13	Rx FIFO Almost Empty Flag Lo	(0 = Rx FIFO Almost Empty)
D12	Rx FIFO Empty Flag Lo	(0 = Rx FIFO Empty)
D11	Tx FIFO Full Flag Lo	(0 = Tx FIFO Full)
D10	Tx FIFO Almost Full Flag Lo	(0 = Tx FIFO Almost Full)
D9	Tx FIFO Almost Empty Flag Lo	(0 = Tx FIFO Almost Empty)
D8	Tx FIFO Empty Flag Lo	(0 = Tx FIFO Empty)

D7:0 Channel Control Bits

D7	RESERVED
D6	Reserved (Channel Reset)
D5:D4	FIFO Rx/Tx Allocation (-48KLC and- 64K options only)
	00 = 48KLC - 8kRx/4kTx ; 64K - 16kRx/8kTx
	01 = 48KLC - 4kRx/8kTx ; 64K - 8kRx/16kTx
D3:D2	RESERVED
D1	Reset Channel Rx FIFO (Pulsed)
	Note: This value will automatically clear to '0'.
D0	Reset Channel Tx FIFO (Pulsed)
	Note: This value will automatically clear to '0'.

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2.9 Interrupt Registers

There are 32 on-board interrupt sources (in addition to PLX interrupts), each of which may be individually enabled. Four interrupt registers control the on-board interrupts – Interrupt Control, Interrupt Status, Interrupt Edge/Level, and Interrupt Hi/Lo. The Interrupt sources are:

IRQ #	Source	Default Level	Alternate Level
IRQ0	Ch1 RxE	Rising Edge	Falling Edge
IRQ1	Ch1 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ2	Ch1 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ3	Ch1 RxSp	Rising Edge	Falling Edge
IRQ4	Ch2 RxE	Rising Edge	Falling Edge
IRQ5	Ch2 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ6	Ch2 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ7	Ch2 RxSp	Rising Edge	Falling Edge
IRQ8	Ch3 RxE	Rising Edge	Falling Edge
IRQ9	Ch3 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ10	Ch3 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ11	Ch3 RxSp	Rising Edge	Falling Edge
IRQ12	Ch4 RxE	Rising Edge	Falling Edge
IRQ13	Ch4 Tx FIFO Almost Empty	Rising Edge	Falling Edge
IRQ14	Ch4 Rx FIFO Almost Full	Rising Edge	Falling Edge
IRQ15	Ch4 RxSp	Rising Edge	Falling Edge
IRQ16	Ch1 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ17	Ch1 Tx FIFO Full	Rising Edge	Falling Edge
IRQ18	Ch1 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ19	Ch1 Rx FIFO Full	Rising Edge	Falling Edge
IRQ20	Ch2 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ21	Ch2 Tx FIFO Full	Rising Edge	Falling Edge
IRQ22	Ch2 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ23	Ch2 Rx FIFO Full	Rising Edge	Falling Edge
IRQ24	Ch3 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ25	Ch3 Tx FIFO Full	Rising Edge	Falling Edge
IRQ26	Ch3 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ27	Ch3 Rx FIFO Full	Rising Edge	Falling Edge
IRQ28	Ch4 Tx FIFO Empty	Rising Edge	Falling Edge
IRQ29	Ch4 Tx FIFO Full	Rising Edge	Falling Edge
IRQ30	Ch4 Rx FIFO Empty	Rising Edge	Falling Edge
IRQ31	Ch4 Rx FIFO Full	Rising Edge	Falling Edge

For all interrupt registers, the IRQ source (IRQ31:IRQ0) will correspond to the respective data bit (D31:D0) of each register (D0 = IRQ0, D1 = IRQ1, etc.).

All FIFO interrupts are edge triggered active high. This means that an interrupt will be asserted (assuming it is enabled) when a FIFO Flag transitions from FALSE to TRUE (rising edge triggered) or TRUE to FALSE (falling edge). For example: If Tx FIFO Empty Interrupt is set for Rising Edge Triggered, the interrupt will occur when the FIFO transitions from NOT EMPTY to EMPTY. Likewise, if Tx FIFO Empty Interrupt is set as Falling Edge Triggered, the interrupt will occur when the FIFO transitions from EMPTY to NOT EMPTY.

All Interrupt Sources share a single interrupt request back to Local Interrupt Input of the PCI9056 PLX chip. This Local Interrupt input must be enabled in the PLX Interrupt Control/Status Register to be recognized as a PCI interrupt source.

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2.8.1 Interrupt Control: Local Offset 0x0060

The Interrupt Control register individually enables each interrupt source. A '1' enables each interrupt source; a '0' disables. An interrupt source must be enabled for an interrupt to be generated.

2.8.2 Interrupt Status/Clear: Local Offset 0x0064

The Interrupt Status Register shows the status of each respective interrupt source. If an interrupt source is enabled in the Interrupt Control Register, a '1' in the Interrupt Status Register indicates the respective interrupt has occurred. The interrupt source will remain latched until the interrupt is cleared, either by writing to the Interrupt Status/Clear Register with a '1' in the respective interrupt bit position, or the interrupt is disabled in the Interrupt Control Register. Clearing an interrupt which is not enabled or not asserted will have no effect.

2.8.3 Interrupt Edge/Level: Local Offset 0x0068

The Interrupt Edge Register is an information only (read only) register. This register can be used by a generic driver to determine if the interrupt source is edge or level triggered. All interrupt sources on the SIO4BXR-SYNC are edge triggered.

2.8.4 Interrupt Hi/Lo: Local Offset 0x006C

The Interrupt Edge Register is an information only register which denotes all interrupt sources as edge triggered. The Interrupt Hi/Lo Register defines each interrupt source as rising edge or falling edge. For example, a rising edge of the TX Empty source will generate an interrupt when the TX FIFO becomes empty. Defining the source as falling edge will trigger an interrupt when the TX FIFO becomes "NOT Empty".

2.10 Channel Pin Source B: Local Offset 0x0070 / 0x0074 / 0x0078 / 0x007C

The Channel Pin Source Register B configures interface for a Pulsed Envelope / Delayed Data

D31:8 RESERVED
D7:5 Rx Envelope Delay - Number of clock cycles (0-7) data is delayed from RxE
D4 Rx Envelope Pulse - Rx Envelope is a single clock pulsed signal - data will be received for Receive Bit Size clocks (D31:16 of Rx Bit Size Register)
D3:1 Tx Data Delay - Number of clock cycles (0-7) data is delayed from TxE
D0 Tx Envelope Pulse - Tx Envelope is a single clock pulsed signal - data will be transmitted for Transmit Bit Count clocks (D15:0 of Tx Bit Size Register)

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2.11 Channel Pin Source: Local Offset 0x0080 / 0x0084 / 0x0088 / 0x008C

The Channel Pin Source Register configures the function of the cable interface signals as well as controls the transceiver protocols.

31	30	29	28	27	26	25	24
Cable Xcvr Enable	X	Ext Loopback Enable	DCE/DTE Mode	Transceiver Protocol Mode			

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Int LB	XXX			TxD Idl	X	RxD Src		RxE Src		RxC Src	TxSp Src		TxAuxC Src		TxD Src			TxE Src		TxC Idl	TxC Src		

Pin Source Register

D31 Cable Transceiver Enable
Setting this bit turns on the cable transceivers. If this bit is cleared, the transceivers are tristated.

D30 RESERVED (Termination Disable)

D29 External Loopback Mode
When Cable Transceiver is enabled (Bit D31), this bit will automatically loopback the TxC/RxC, TxD/RxD, and TxE/RxE signals at the cable (transceivers enabled).
Notes:

- The DCE/DTE mode will select the set of signals (DCE or DTE) to be looped back
- Since the transceivers will be enabled in this mode, all external cables should be disconnected to prevent interference from external sources.

D28 DCE/DTE Mode
This bit sets up the transceiver direction. Setting the mode to '1' will enable DCE mode, while '0' will set DTE mode (default). See Section 5.3 for a detail of the signal direction as defined for each mode.

D27:24 Transceiver Protocol Mode

D27	D26	D25	D24	Transceiver Mode
0	0	0	0	RS-422 / RS-485
0	0	0	1	RS-423
0	0	1	0	RS-232
0	0	1	1	RESERVED
0	1	X	X	RESERVED
1	X	X	X	RESERVED

D23 Int LB
0 Normal Mode
1 Internal Loopback – TxC, TxD, TxE looped back internally

D22:21 RESERVED

D20 TxC Idl
0 TxC driven low ('0') while Idle (Envelope Negated)
1 TxC driven high ('1') while Idle (Envelope Negated)

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D19	TxD Idl	0	TxD driven low (‘0’) while Idle (Envelope Negated)
		1	TxD driven high (‘1’) while Idle (Envelope Negated)
D18:17	RESERVED		
D16	RxD Src	0	RxD Active Hi (NRZ)
		1	RxD Active Lo (NRZB)
D15:14	RxE Src	00	RxE Active Hi
		01	RxE Active Lo
		1X	RxE Disabled
D13	RxC Src	0	Sample Data on Falling Edge of Clock (Data Change on Rising)
		1	Sample Data on Rising Edge of Clock (Data Change on Falling)
D12:11	TxSp Src	00	Disabled
		01	Input
		10	'0'
		11	'1'
D10:9	TxAuxC Src	00	Tri-State
		01	ProgClk/2
		10	'0'
		11	'1'
D8:6	TxD Src	0X0	TxD Active Hi (NRZ)
		0X1	TxD Active Lo (NRZB)
		1X0	'0'
		1X1	'1'
D5:4	TxE Src	00	TxE Active Hi
		01	TxE Active Lo
		10	'0'
		11	'1'
D3	TxC Idl	0	TxC driven while Idle (Envelope Negated)
		1	No TxC while Idle (Envelope Negated)
D2:0	TxC Src	000	Clock Data on Rising Edge of Internal Programmable Clock / 2 (Data/Envelope change on rising edge)
		001	Clock Data on Falling Edge of Internal Programmable Clock / 2 (Data/Envelope change on falling edge)
		010	Clock Data on Rising Edge of External Clock (Data/Envelope change on rising edge)
		011	Clock Data on Falling Edge of External Clock (Data/Envelope change on falling edge)
		1X0	'0'
		1X1	'1'

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2.12 Channel Pin Status: Local Offset 0x0090 / 0x0094 / 0x0098 / 0x009C

In addition to standard inputs, unused inputs may be utilized as general purpose input signals. The Channel Pin Status Register allows the input state of all the IO pins to be monitored. Output signals as well as inputs are included to aid in debug operation.

D31:D10	RESERVED
D9	SPARE Output
D8	SPARE Input
D7	AuxC Output
D6	TxE Output
D5	TxD Output
D4	TxC Output
D3	AuxC Input
D2	RxE Input
D1	RxD Input
D0	RxC Input

2.13 Programmable Clock Registers: Local Offset 0x00A0 / 0x00A4 / 0x00A8

The Programmable Clock Registers allow the user to program the on-board programmable oscillator and configure the channel clock post-dividers. As GSC should provide software routines to program the clock, the user should have no need to access these registers. See Section 4.6 for more information.

2.14 Tx Bit Register: Local Offset 0x00B0 / 0x00B4 / 0x00B8 / 0xBC

D31:16	Gap Bit Count When transmitting, these bits indicate the number of idle clocks between transmitted words. To output a continuous stream of bits, this value should be set to zero.
D15:0	Transmit Bit Size These bits indicate the number of consecutive bits to transmit for each transmit word.

2.15 Rx Bit Register: Local Offset 0x00C0 / 0x00C4 / 0x00C8 / 0xCC

D31:16	Receive Bit Size These bits indicate the number of consecutive bits to receive for each received word.
D15:0	Receive Bit Count When receiving, these bits indicate the number of consecutive bits received for the last received word.

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2.16 FIFO Count Register: Local Offset 0x00D0 / 0x00D4 / 0x00D8 / 0x00DC

The FIFO Count Registers display the current number of words in each FIFO. This value, along with the FIFO Size Registers, may be used to determine the amount of data which can be safely transferred without over-running (or under-running) the FIFOs.

D31:D16	Number of words in Rx FIFO
D15:D0	Number of words in Tx FIFO

2.17 FIFO Size Register: Local Offset 0x00E0 / 0x00E4 / 0x00E8 / 0x00EC

The FIFO Size Registers display the sizes of the installed data FIFOs. This value is calculated at power-up. This value, along with the FIFO Count Registers, may be used to determine the amount of data which can be safely transferred without over-running (or under-running) the FIFOs.

D31:D16	Size of installed Rx FIFO
D15:D0	Size of installed Tx FIFO

2.18 FW Type ID Register: Local Offset 0x00F8

This register allows boards to be designed with different functionality on each channel. For example, a board could contain two Standard SIO channels (with Z16C30), and two Synchronous channels. Each byte corresponds to a channel. The default FW type for all channels will reflect the board channels as ordered: 04=SYNC; 01=Standard

D31:D24	Channel 4 FW Type
D23:D16	Channel 3 FW Type
D15:D8	Channel 2 FW Type
D7:D0	Channel 1 FW Type

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2.19 Features Register: Local Offset 0x00FC

The Features Register allows software to account for added features in the firmware versions. Bits will be assigned as new features are added. See Appendix B for more details.

D31:24	RESERVED
D23	**1** = Sync Timestamp + Rx Bit Size
D22	**1** = Rx Stop on Full in Ch_Ctrl
D21	**1** = SRAM Debug
D20	**1** = No Rx Status byte (std only)
D19:D18	**10** = Internal Timestamp (std only)
D17:D16	**01** = FPGA Reprogram field
D15:D14	**01** = Configurable FIFO space
D13	**1** = FIFO Test Bit
D12	**1** = FW Type Reg
D11:8	Features Rev Level **0xA** = BX level
D7	**1** = Demand Mode DMA Single Cycle Disable feature implemented
D6	**1** = Board Reset
D5	**1** = FIFO Counters/Size
D4	**1**
D3:0	Programmable Clock Configuration **0x4** = Two CY22393 - 6 Oscillators

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CHAPTER 3: PROGRAMMING

3.1 Serial Interface

3.1.1 Serial Interface Definition

The Pin Source Register contains information which defines the physical serial interface. This register contains fields to setup the polarity of the TxC, RxC, TxD, RxD, TxE, and RxE signals. As these signals are all individually configurable, it is possible to setup the Receive channel differently than the Transmit channel. In addition, the TxD Idle field defines the state of the TxD signal while idling (not sending data).

The MSB/LSB for both transmit and receive is setup in the Channel Control/Status register. Note that this acts only upon the current byte. MSB will send/receive bit D7 first, LSB will send/receive D0 first. For word lengths of other than 8 bits, the word should be right/left justified accordingly. Since the MSB/LSB only acts upon 8 bits, if the bit length is greater than 8 bits, the bits will only be reversed on a byte by byte basis. The user may need to rearrange bytes for bit lengths greater than 8 bits.

3.1.2 Two Signal Interface

A two signal interface is a special setup case of the three signal serial interface. In a three signal interface, an envelope signal defines when data is valid. For a two wire case, every clock indicates valid data. When data is invalid, the clock simply stops.

For transmit, the TxC Idle field defines the two signal interface. By setting the TxC Idle enable, the clock will stop during idle periods. The TxCount and TxGap still apply. The TxE signal may be left enabled and simply unconnected, or may be reconfigured as a general purpose output.

For receive, a two wire interface is defined when RxE is set as a general purpose input. When RxE is set as an input, the internal logic simply assumes the internal RxE is always valid. Thus, all data is considered valid based on the RxC clock.

3.1.3 Tx Word Bit Size / Tx Gap

The TxBitSiz/TxGap register defines the number of consecutive bits to transmit in a word, as well as the number of idle clock cycles between words. This configurability allows this board to interface with a custom user interface. All data sent to/from the board is in 8 bit increments. Therefore, if TxCount is not a multiple of 8, all extra bits will be padded with zeros. For example, a TxBitSizof 14 would use 14 bits out of two consecutive bytes (and the two extra bits would be ignored).

Note that there is no hardware interlock to ensure that TxBitSiz bits are present in the Tx FIFO before a transmit can begin. If TxCount is greater than 8 bits (and transmit is enabled), the first 8 bits will be transmitted as soon as it is loaded into the TxFIFO. If the TxFIFO is empty when the first 8 bits complete, a gap will be inserted. Therefore, if the TxCount is greater than 8 bits, some data should be preloaded into the TxFIFO before the transmit is enabled. This will ensure a continuous data stream of the correct length.

For a optimized continuous data stream, the TxBitSiz should be set to 8 and TxGap to 0.

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Certain TxCount/TxGap combinations may not work correctly in a very few instances. In general, a data word cannot be transmitted or received faster than 500ns per byte. If the TxCount, TxGap, and serial data rate result in a throughput rate of greater than 1 byte in 500ns, correct operation cannot be guaranteed. If an application requires such an interface, please contact GSC tech support to determine if the board will work for your application.

3.1.4 Rx Word Bit Size / Rx Bit Count

(Rx Bit Size is a new feature with firmware version 0x11D / 0x41D)

The Rx Word Bit Size represents the expected bit size of the Rx word. For a continuous bit stream, this allows the Rx Words to be saved in a non-packed format. If the Rx Bit Size value is defined non-zero, the Rx word will be saved after Rx Bit Size bits are received. If the Rx Bit Size is less than 8, each Rx word will be Rx Bit Size in length. If the Rx Bit Size is greater than 8, the Rx word will be saved in 8 bit words until the final byte. If Rx Bit Size is defined zero, the Rx data will be recorded in 8 bit words until the frame valid is negated (only the last byte may be less than 8 bits).

The Rx Bit Size is also used to define the expected Rx Bit Size for a frame pulse mode (see 3.9).

The Rx Bit Count is primarily a debug feature to check that the expected number of bits in a frame were received. The Rx Bit Count will simply count received bits in the current frame. It will reset at the beginning of each frame based on RxE, or may be reset via the Rx Bit Count Reset bit of the Channel Control Register. For a two signal interface, this register will count all bits received.

3.2 FIFOs

Deep transmit and receive FIFOs are the key to providing four high speed serial channels without losing data. Several features have been implemented to help in managing the on-board FIFOs. These include FIFO flags (Empty, Full, Almost Empty and Almost Full) presented as both real-time status bits and interrupt sources, and individual FIFO counters to determine the exact FIFO fill level. DMA of data to/from the FIFOs provides for fast and efficient data transfers.

A single memory address is used to access both transmit and receive FIFOs for each channel. Data written to this memory location will be written to the transmit FIFO, and data read from this location retrieves data from the receive FIFO. Individual resets for the FIFOs are also provided in the Channel Control/Status Register.

3.2.1 FIFO Flags

Four FIFO flags are present from each on-board FIFO: FIFO Empty, FIFO Full, FIFO Almost Empty, and FIFO Almost Full. These flags may be checked at any time from the Channel Control/Status Register. Note these flags are presented as active low signals (‘0’ signifies condition is true). The Empty and Full flags are asserted when the FIFO is empty or full, respectively. The Almost Empty and Almost Full flags are software programmable such that they may be asserted at any desired fill level. This may be useful in determining when a data transfer is complete or to provide an indicator that the FIFO is in danger of overflowing and needs immediate service.

The Almost Flag value represents the number of bytes from each respective “end” of the FIFO. The Almost Empty value represents the number of bytes from empty, and the Almost Full value represents the number of bytes from full (NOT the number of bytes from empty). For example, the default value of “0x0007 0007” in the FIFO Almost Register means that the Almost Empty Flag will indicate when the FIFO holds 7 bytes or fewer. It will transition as

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the 8th byte is read or written. In this example, the Almost Full Flag will indicate that the FIFO contains (FIFO Size – 7) bytes or more. For the standard 32Kbyte FIFO, an Almost Full value of 7 will cause the Almost Full flag to be asserted when the FIFO contains 32761 (32k – 7) or more bytes of data .

The values placed in the FIFO Almost Registers take effect immediately, but should be set while the FIFO is empty (or the FIFO should be reset following the change). Note that this is a little different than the method for FIFO Flag programming which has previously been implemented on SIO4 boards. No FIFO programming delay is necessary.

3.2.2 FIFO Counters

The FIFO Size and FIFO count registers can be used to determine the exact amount of data in a FIFO as well as the amount of free space remaining in a FIFO. The size of each FIFO is auto-detected following a board reset. Real-time FIFO counters report the exact number of data words currently in each FIFO. By utilizing this information, the user can determine the exact amount of data which can safely be transferred to the transmit FIFOs or transferred from the receive FIFO. This information should help streamline data transfers by eliminating the need to continuously check empty and full flags, yet still allow larger data blocks to be transferred.

3.2.3 FIFO Size

In some applications, 4K byte FIFOs may be all that is required to implement a serial interface. This typically includes baud rates slower than 500kbps, or applications where the transfer size is limited to less than 4K bytes at a time (and an effective throughput rate less than 500kpbs). For faster applications, deeper external FIFOs are required to ensure no data will be lost. For slower or low data applications, the 4K/8K FIFOs provided in a PMC66-SIO4BXR-SYNC-48KLC board should be adequate. The PMC66-SIO4BXR-SYNC-64K provides an intermediate solution with 8K/16K FIFO sizes, while the PMC66-SIO4BXR-SYNC-256K provides 32K FIFOs on each channel.. Please contact General Standards if you have any questions about determining which FIFO size may be necessary for a specific application.

Since the Rx/Tx FIFO sizes are different in the -48KLC and -64K options (the -64K option actually provides 96K bytes of FIFO space by utilizing internal board memory), the FIFO size may be further customized for Rx or Tx applications by allocating the larger memory to either the Rx or Tx FIFOs. (D5:D4 of Ch Control Reg).

3.3 Board vs. Channel Registers

Since four serial channels are implemented on a single board, some registers apply to the entire board, while others are unique to each channel. It is intended that each channel can act independently, but the user must keep in mind that certain accesses will affect the entire board. Typically, the driver will adequately handle keeping board and channel interfaces separate. However, the user must also be mindful that direct access to certain registers will affect the entire board, not just a specific channel.

The Board Control and Board Status registers provide board level controls. Fundamentally, a board reset will do just that, reset all the GSC registers and FIFOs to their default state. Interrupt control is also shared among all registers, although local bits are segregated by channel. The device driver should take care of appropriately handling the inter-mixed channel interrupts and pass them on to the application appropriately.

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3.4 Programmable Oscillator / Programmable Clocks

The On-Board Programmable Oscillator provides each channel with a unique programmable clock source using a Cypress Semiconductor CY22393 Programmable Clock generator. In order to program the oscillator, it is necessary to calculate and program values for different clock frequencies. General Standards has developed routines to calculate the necessary values for a given setup and program the clock generator. These clock setup routines have been incorporated into most of the drivers.

The default clock configuration at power-up for the programmable clock on all channels is 20MHz. See Appendix A for more detailed information concerning programming the on-board clock frequencies, as well as common frequency setups. The specific driver manual should have information on clock setup. If not, please contact GSC tech support for assistance.

3.5 Multiprotocol Transceiver Control

The SIO4BX-SYNC has multiprotocol transceivers which allow RS422/RS485, RS232, or RS423. The mode is set by the Protocol Mode field in the Pin Source Register. Note that RS423 remaps the TxC/RxC and TxD/RxD signals to the AuxC and Spare pins on the user connector. See RS423 Connector pinout for more details.

3.6 DCE/DTE Mode

As all signals are bidirectional, the DCE or DTE mode will set the direction for each signal. For the transceivers to be configured as either DTE or DCE, set the DCE/DTE Enable bit in the Pin Source register (D31). The following table gives the input/output configuration for each signal: The DCD direction is set in the Pin Source register fields, independent of DCE/DTE mode.

Signal	DTE	DCE
TxC	TxC Out	RxC In
RxC	RxC In	TxC Out
TxD	TxD Out	RxD In
RxD	RxD In	TxD Out
TxE	TxE Out	RxE In
RxE	RxE In	TxE Out
AuxC	Direction controlled by Pin Source Reg D10:9	
Spare	Direction controlled by Pin Source Reg D12:11	

3.7 Loopback Modes

For normal operation, the Cable Transceiver Enable bit of the Pin Source Register will turn on the cable transceivers, and the DTE/DCE Mode bit will set the transceiver direction. These bits must be set before any data is transmitted over the user interface.

Additionally, there are several ways to loopback data to aid in debug operations. Data may be physically looped back externally by connecting one channel to another. For DB25 cable applications, this simple loopback method will require a gender changer to connect one channel to another. One channel will be set to DTE mode, the other to DCE mode. Data sent from one channel will be received on the other.

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An External Loopback mode (External Loopback bit set in the Pin Source Register) is also provided to loop back data on the same channel without requiring any external cabling. In this mode, the DTE/DCE mode will control the location for the transmit signals (TxC, TXD, TXE), and the receive signals will use these same signals as the receive inputs. Since signals are transmitted and received through the transceivers, this mode allows the setup to be verified (including signal polarity) without any external connections. Since external signals could interfere with loopback operation, all cables should be disconnected when running in external loopback mode.

An Internal Loopback Mode is also provided which loops back on the same channel internal to the board. This provides a loopback method which does not depend on DTE/DCE mode or signal polarity. This can remove cable transceiver and signal setup issues to aid in debugging. If the Cable Transceivers are enabled, the transmit data will still appear on the appropriate transmit pins (based on DTE/DCE Mode setting). The Pin Status register will not reflect internally looped back signals, only signals to/from the transceivers.

3.8 Timestamp

(Timestamp is a new feature with firmware version 0x11D / 0x41D)

The timestamp feature allows a relative 24-bit timestamp to be recorded along with the received data stream. The timestamp clock can be set to either an internal 1us clock or can be input from the AUXC4 or SPARE4 signals.

Two modes are implemented for recording timestamp data: at the start of a frame or with every received word. For start of frame, the timestamp is recorded only once at the start of frame when RxE is asserted. If timestamp is recorded with every word, the timestamp will be saved preceding each Rx word (defined by Rx Bit Size).

For PXI applications, the timestamp and reset can be connected to TTL PXI signals on a semi-custom basis. Please contact General Standards for to inquire about TTL input timestamp options.

3.9 Frame Valid Pulse / Delay Mode

(Pulse/Delay is a new feature with firmware version 0x115 / 0x415, modified for RxBitSize in 0x11D / 0x41D)

To support applications where a single pulse defines start of frame, the RxE may be defined as a single pulse. For transmit, the Transmit Bit Size will define the length of the frame. Likewise, the Rx Bit Size will define the expected receive frame size. The Tx and Rx Pulse enables are defined in the Pin Source B register.

For sync applications that require an envelope that is skewed from the data, a delay mode has also been defined in the Pin Source B register. The envelope may precede the data by up to 7 clocks, individually defines for Rx and Tx.

3.10 General Purpose IO

Unused signals at the cable may be used for general purpose IO. The Pin Source and Pin Status Registers provide for simple IO control of all the cable interface signals. For outputs, the output value is set using the appropriate field in the Pin Source Register. All inputs can be read via the Pin Status register.

Since TxAuxC and RxAuxC share a single pin, the TxAuxC Src field in the Pin Source Register controls whether AuxC will function as an input or output. If the field is set to ‘Tri-State’, the pin is set as RxAuxC Input. Otherwise, The TxAuxC output will be driven (and the RxAuxC input will be equal to the TxAuxC output). Likewise, the TxSp Src field in the Pin Source Register controls the Spare pin direction. If the field is set to ‘Tri-State’, RxSp will be an Input. Otherwise, RxSp will follow the TxSp output.

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3.11 Interrupts

The PMC66-SIO4BXR-SYNC has a number of interrupt sources which are passed to the host CPU via the PCI IRQA. Since there is only one physical interrupt source for the board, the interrupts pass through a number of "levels" to get multiplexed onto this single interrupt. The interrupt originates in the PCI9056 PCI Bridge, which combines the internal PLX interrupt sources (DMA) with the Local on-board interrupt. The single Local Interrupt is made up of the interrupt sources described in Section 2.8. The user should be aware that interrupts must be enabled at each level for an interrupt to occur. For example, if a FIFO interrupt is used, it must be setup and enabled in the GSC Firmware Interrupt Control Register, as well as enabled in the PCI9056. In addition, the interrupt must be acknowledged and/or cleared at each level following the interrupt. The driver will typically take care of setting up and handling the PCI9056 interrupts as well as most local interrupts. The specific driver manual should have more information on how to handle these interrupts.

3.10 PCI DMA

The PCI DMA functionality allows data to be transferred between host memory and the SIO4BXR onboard FIFOs with the least amount of CPU overhead. The PCI9056 bridge chip handles all PCI DMA functions, and the device driver should handle the details of the DMA transfer. (Note: DMA refers to the transfer of Data from the on-board FIFOs over the PCI bus. This should not be confused with the DMA mode of the USC – transfer of data between the USC and the on-board FIFOs. This On-Board DMA is setup by the driver and should always be enabled).

There are two PCI DMA modes – Demand Mode DMA and Non-Demand Mode DMA. Demand Mode DMA refers to data being transferred on demand. For receive, this means data will be transferred as soon as it is received into the FIFO. Likewise, for transmit, data will be transferred to the FIFOs as long as the FIFO is not full. The disadvantage to Demand Mode DMA is that the DMA transfers are dependent on the user data interface. If the user data transfer is incomplete, the Demand mode DMA transfer will also stop. If a timeout occurs, there is no way to determine the exact amount of data transferred before it was aborted.

Non-Demand Mode DMA does not check the FIFO empty/full flags before or during the data transfer – it simply assumes there is enough available FIFO space to complete the transfer. If the transfer size is larger than the available data, the transfer will complete with invalid results. This is the preferred mode for DMA operation. The FIFO Counters may be used to determine how much space is available for DMA so that the FIFO will never over/under run. Demand Mode DMA requires less software control, but runs the risk of losing data due to an incomplete transfer. The GSC library uses this method (Non-Demand DMA and checking the FIFO counters) as the standard transfer method.

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CHAPTER 4: PCI INTERFACE

4.0 PCI Interface Registers

The PMC/PCI interface is handled by a PCI9056 I/O Accelerator from PLX Technology. The PCI interface is compliant with the 5V, 66MHz 32-bit PCI Specification 2.2. The PCI9056 provides dual DMA controllers for fast data transfers to and from the on-board FIFOs. Fast DMA burst accesses provide for a maximum burst throughput of 264MB/s to the PCI interface. To reduce CPU overhead during DMA transfers, the controller also implements Chained (Scatter/Gather) DMA, as well as Demand Mode DMA.

Since many features of the PCI9056 are not utilized in this design, it is beyond the scope of this document to duplicate the PCI9056 User's Manual. Only those features, which will clarify areas specific to the PMC66-SIO4BXR are detailed here. Please refer to the PCI9056 User's Manual (See Related Publications) for more detailed information. Note that the BIOS configuration and software driver will handle most of the PCI9056 interface. Unless the user is writing a device driver, the details of this PCI Interface Chapter may be skipped.

4.1 PCI Registers

The PLX 9056 contains many registers, many of which have no effect on the SIO4BXR performance. The following section attempts to filter the information from the PCI9056 manual to provide the necessary information for a SIO4BXR specific driver.

The SIO4BXR uses an on-board serial EEPROM to initialize many of the PCI9056 registers after a PCI Reset. This allows board specific information to be preconfigured correctly.

4.1.1 PCI Configuration Registers

The PCI Configuration Registers allow the PCI controller to identify and control the cards in a system.

PCI device identification is provided by the Vendor ID/Device ID (Addr 0x0000) and Sub-Vendor ID/Sub-Device ID Registers (0x002C). The following definitions are unique to the General Standards SIO4BXR boards. All drivers should verify the ID/Sub-ID information before attaching to this card. These values are fixed via the Serial EEPROM load following a PCI Reset, and cannot be changed by software.

Vendor ID	0x10B5	PLX Technology
Device ID	0x9056	PCI9056
Sub-Vendor ID	0x10B5	PLX Technology
Sub-Device ID	0x3198	GSC SIO4BXR

The configuration registers also setup the PCI IO and Memory mapping for the SIO4BXR. The PCI9056 is setup to use PCIBAR0 and PCIBAR1 to map the internal PLX registers into PCI Memory and IO space respectively. PCIBAR2 will map the Local Space Registers into PCI memory space, and PCIBAR3 is unused. Typically, the OS will configure the PCI configuration space.

For further information of the PCI configuration registers, please consult the PLX Technology PCI9056 Manual.

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4.1.2 Local Configuration Registers

The Local Configuration registers give information on the Local side implementation. These include the required memory size. The SIO4BXR memory size is initialized to 4k Bytes. All other Local Registers initialize to the default values described in the PCI9056 Manual.

4.1.3 Runtime Registers

The Runtime registers consist of mailbox registers, doorbell registers, and a general-purpose control register. The mailbox and doorbell registers are not used and serve no purpose on the SIO4BXR. All other Runtime Registers initialize to the default values described in the PCI9056 Manual.

4.1.4 DMA Registers

The Local DMA registers are used to setup the DMA transfers to and from the on-board FIFOs. DMA is supported only to the four FIFO locations. The SIO4BXR supports both Demand (DREQ# controlled) and Non-Demand mode DMA. Both Channel 0 and Channel 1 DMA are supported.

4.1.4.1 DMA Channel Mode Register: (PCI 0x80 / 0x94)

The DMA Channel Mode register must be setup to match the hardware implementation.

Bit	Description	Value	Notes
D1:0	Local Bus Width	11 = 32 bit 00 = 8 bit	Although the serial FIFOs only contain 8 bits of data, the register access is still a 32bit access. It is possible to "pack" the data by setting the Local Bus Width to 8, but this is only guaranteed to work with Non-Demand Mode DMA
D5:2	Internal Wait States	0000 = Unused	
D6	Ready Input Enable	1 = Enabled	
D7	Bterm# Input Enabled	0 = Unused	
D8	Local Burst Enable	1 = Supported	Bursting allows fast back-to-back accesses to the FIFOs to speed throughput
D9	Chaining Enable (Scatter Gather DMA)	X	DMA source addr, destination addr, and byte count are loaded from memory in PCI Space.
D10	Done Interrupt Enable	X	DMA Done Interrupt
D11	Local Addressing Mode	1 = No Increment	DMA to/from FIFOs only
D12	Demand Mode Enable	X	Demand Mode DMA is supported for FIFO accesses on the SIO4BXR. (See Section 3.3)
D13	Write & Invalidate Mode	X	
D14	DMA EOT Enable	0 = Unused	
D15	DMA Stop Data Transfer Enable	0 = BLAST terminates DMA	
D16	DMA Clear Count Mode	0 = Unused	
D17	DMA Channel Interrupt Select	X	
D31:18	Reserved	0	

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CHAPTER 5: HARDWARE CONFIGURATION

5.0 Board Layout

The following figure is a drawing of the physical components of the PMC66-SIO4BXR-SYNC:

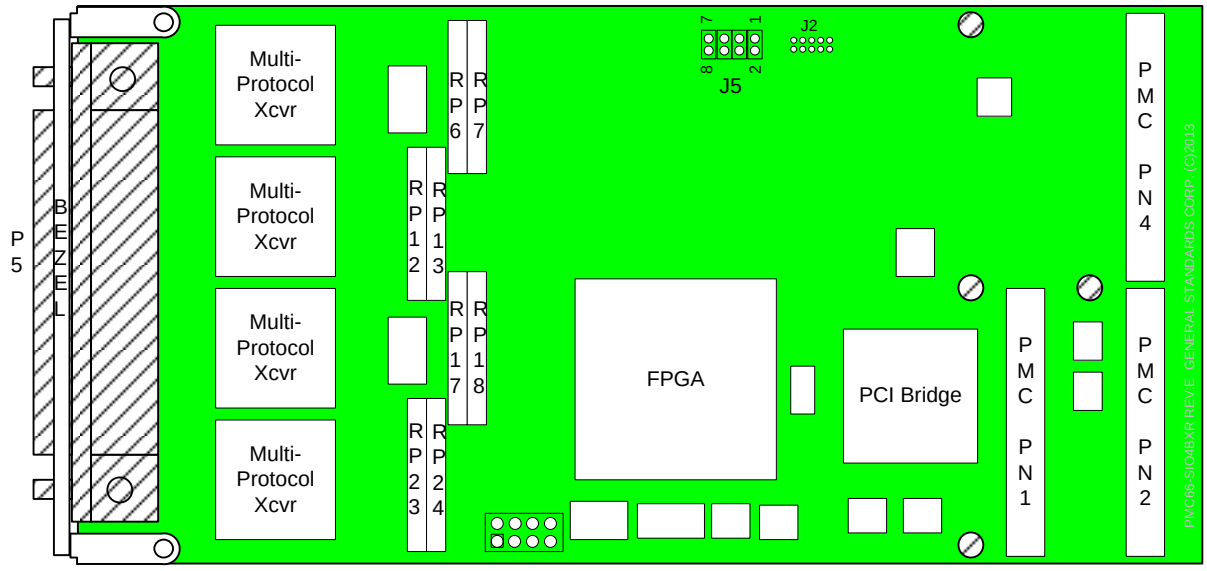


Figure 5-1: Board Layout – Top

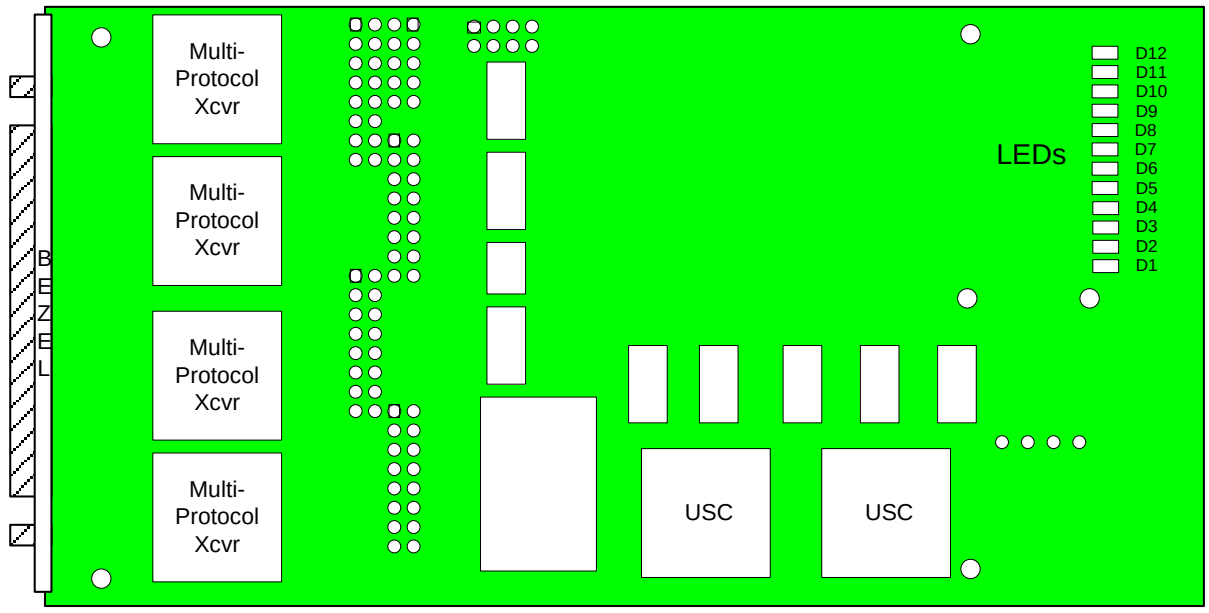


Figure 5-2: Board Layout - Bottom

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5.1 Board ID Jumper J5

Jumper J5 allows the user to set the Board ID in the GSC Board Status Register (See Section 2.1.3). This is useful to uniquely identify a board if more than one SIO4BXR card is in a system. When the Board ID jumper is installed, it will read '1' in the Board Status Register. The Board Status Register bit will report '0' when the jumper is removed. Refer to Figure 5-1 for Jumper J5 location.

J5 Jumper	Description	Notes
1 - 2	Board ID 1	Board ID 1 in Board Status Register (D1)
3 - 4	Board ID 2	Board ID 2 in Board Status Register (D3)
5 - 6	Board ID 3	Board ID 3 in Board Status Register (D4)
7 - 8	Board ID 4	Board ID 4 in Board Status Register (D5)

5.2 Termination Resistors

The PMC66-SIO4BXR-SYNC board is designed with socketed external parallel termination. The external termination resistors are 8 pin SIPs. There are 8 termination SIPs – RP6, RP7, RP12, RP13, RP17, RP18, RP23, and RP24. The external parallel resistors are for RS422/RS485 termination only. No bias resistors are installed.

The -SYNC board is shipped with 120 Ohm external termination resistors. Refer to Figure 5-1 for resistor pack locations.

Note: Since –SYNC boards now also support standard USC channels, care must be taken to ensure the termination resistors are enabled correctly. For a SYNC channel, external termination resistors should be installed if termination is required. For standard USC channels, internal 120 Ohm resistors are enabled by default for RxC, RxC, AuxC, and DCD. If internal resistors are enabled for the standard USC channel (Pin Source D30), the external resistors should be removed for that channel.

Please contact quotes@generalstandards.com if a different termination value or bias resistors are required.

5.3 LEDs

Eleven green LEDs (D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12) are accessible via software. Refer to Figure 5-2 for these LED locations.

LED_D2 is controlled by Board Control Register D26.
LED_D3 is controlled by Board Control Register D25.
LED_D4 is controlled by Board Control Register D24.

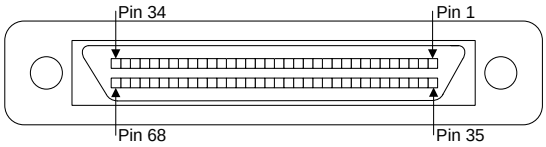
The remaining 8 LEDs are controlled 2 each from D23:D20 of the Channel Control Register. Additionally, if all the LED controls are set to 0 in all four of the Channel Control Registers (power up default), the LEDs will display the lower 6 bits of the firmware revision in LED_D7 to LED_D12. LED_D5 should power up off, and LED_D7 should power up on to indicate all channels are set to -SYNC.

Channel Control Register D23:D20 allow software control of the LEDs. Each Channel Control Register controls 2 LEDs (in order from Ch4 to Ch1). If D23:D22="10", the upper LED will turn off. Likewise, if D23:D22="11", the upper LED will turn on. D21:D20 control the lower LED in the pair.

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5.4 Interface Connector

User I/O Connector: 68-pin SCSI connector (female) - P5
Part Number: AMP/TYCO 787170-7
Mating Connector: AMP/TYCO 749111-6 (or equivalent)



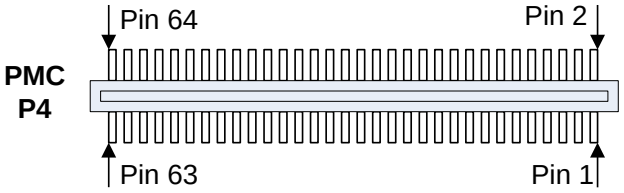
Note: Protocol Mode is set on a per channel basis.

Pin #	RS422/RS485 V.35		RS232		RS423		Pin #	RS422/RS485 V.35		RS232		RS423	
	DTE	DCE	DTE	DCE	DTE	DCE		DTE	DCE	DTE	DCE	DTE	DCE
1	AUXC1+		Unused		TXC1	RXC1	35	AUXC3+		Unused		TXC3	RXC3
2	AUXC1-		AUXC1		RXC1	TXC1	36	AUXC3-		AUXC3		RXC3	TXC3
3	SPARE1+		Unused		TXD1	RXD1	37	SPARE3+		Unused		TXD3	RXD3
4	SPARE1-		SPARE1		RXD1	TXD1	38	SPARE3-		SPARE3		RXD3	TXD3
5	RXE1+	TXE1+	Unused		Unused		39	RXE3+	TXE3+	Unused		Unused	
6	RXE1-	TXE1-	RXE1	TXE1	RXE1	TXE1	40	RXE3-	TXE3-	RXE3	TXE3	RXE3	TXE3
7	RXD1+	TXD1+	Unused		Unused		41	RXD3+	TXD3+	Unused		Unused	
8	RXD1-	TXD1-	RXD1	TXD1	Unused		42	RXD3-	TXD3-	RXD3	TXD3	Unused	
9	RXC1+	TXC1+	Unused		Unused		43	RXC3+	TXC3+	Unused		Unused	
10	RXC1-	TXC1-	RXC1	TXC1	Unused		44	RXC3-	TXC3-	RXC3	TXC3	Unused	
11	TXE1+	RXE1+	Unused		Unused		45	TXE3+	RXE3+	Unused		Unused	
12	TXE1-	RXE1-	TXE1	RXE1	TXE1	RXE1	46	TXE3-	RXE3-	TXE3	RXE3	TXE3	RXE3
13	TXD1+	RXD1+	Unused		Unused		47	TXD3+	RXD3+	Unused		Unused	
14	TXD1-	RXD1-	TXD1	RXD1	Unused		48	TXD3-	RXD3-	TXD3	RXD3	Unused	
15	TXC1+	RXC1+	Unused		Unused		49	TXC3+	RXC3+	Unused		Unused	
16	TXC1-	RXC1-	TXC1	RXC1	Unused		50	TXC3-	RXC3-	TXC3	RXC3	Unused	
17	SGND1		SGND1		SGND1		51	SGND3		SGND3		SGND3	
18	SGND2		SGND2		SGND2		52	SGND4		SGND4		SGND4	
19	RXE2+	TXE2+	Unused		Unused		53	RXE4+	TXE4+	Unused		Unused	
20	RXE2-	TXE2-	RXE2	TXE2	RXE2	TXE2	54	RXE4-	TXE4-	RXE4	TXE4	RXE4	TXE4
21	RXD2+	TXD2+	Unused		Unused		55	RXD4+	TXD4+	Unused		Unused	
22	RXD2-	TXD2-	RXD2	TXD2	Unused		56	RXD4-	TXD4-	RXD4	TXD4	Unused	
23	RXC2+	TXC2+	Unused		Unused		57	RXC4+	TXC4+	Unused		Unused	
24	RXC2-	TXC2-	RXC2	TXC2	Unused		58	RXC4-	TXC4-	RXC4	TXC4	Unused	
25	TXE2+	RXE2+	Unused		Unused		59	TXE4+	RXE4+	Unused		Unused	
26	TXE2-	RXE2-	TXE2	RXE2	TXE2	RXE2	60	TXE4-	RXE4-	TXE4	RXE4	TXE4	RXE4
27	TXD2+	RXD2+	Unused		Unused		61	TXD4+	RXD4+	Unused		Unused	
28	TXD2-	RXD2 -	TXD2	RXD2	Unused		62	TXD4-	RXD4-	TXD4	RXD4	Unused	
29	TXC2+	RXC2+	Unused		Unused		63	TXC4+	RXC4+	Unused		Unused	
30	TXC2-	RXC2-	TXC2	TXC2	Unused		64	TXC4-	RXC4-	TXC4	RXC4	Unused	
31	SPARE2+		Unused		TXD2	RXD2	65	SPARE4+		Unused		TXD4	RXD4
32	SPARE2-		SPARE2		RXD2	TXD2	66	SPARE4-		SPARE4		RXD4	TXD4
33	AUXC2+		Unused		TXC2	RXC2	67	AUXC4+		Unused		TXC4	RXC4
34	AUXC2-		AUXC2		RXC2	TXC2	68	AUXC4-		AUXC4		RXC4	TXC4

Table 1- Front Panel (P5) IO Connections

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System I/O Connections (cont):



Note: Protocol Mode is set on a per channel basis.

Pin #	RS422/RS485 V.35		RS232		RS423		Pin #	RS422/RS485 V.35		RS232		RS423	
	DTE	DCE	DTE	DCE	DTE	DCE		DTE	DCE	DTE	DCE	DTE	DCE
1	TXC1-	RXC1-	TXC1	RXC1	Unused		33	TXC3-	RXC3-	TXC3	RXC3	Unused	
2	TXC1+	RXC1+	Unused		Unused		34	TXC3+	RXC3+	Unused		Unused	
3	TXD1-	RXD1-	TXD1	RXD1	Unused		35	TXD3-	RXD3-	TXD3	RXD3	Unused	
4	TXD1+	RXD1+	Unused		Unused		36	TXD3+	RXD3+	Unused		Unused	
5	TXE1-	RXE1-	TXE1	RXE1	TXE1	RXE1	37	TXE3-	RXE3-	TXE3	RXE3	TXE3	RXE3
6	TXE1+	RXE1+	Unused		Unused		38	TXE3+	RXE3+	Unused		Unused	
7	AUXC1-		AUXC1		RXC1	TXC1	39	AUXC3-		AUXC3		RXC3	TXC3
8	AUXC1+		Unused		TXC1	RXC1	40	AUXC3+		Unused		TXC3	RXC3
9	SPARE1-		SPARE1		RXD1	TXD1	41	SPARE3-		SPARE3		RXD3	TXD3
10	SPARE1+		Unused		TXD1	RXD1	42	SPARE3+		Unused		TXD3	RXD3
11	RXC1-	TXC1-	RXC1	TXC1	Unused		43	RXC3-	TXC3-	RXC3	TXC3	Unused	
12	RXC1+	TXC1+	Unused		Unused		44	RXC3+	TXC3+	Unused		Unused	
13	RXD1-	TXD1-	RXD1	TXD1	Unused		45	RXD3-	TXD3-	RXD3	TXD3	Unused	
14	RXD1+	TXD1+	Unused		Unused		46	RXD3+	TXD3+	Unused		Unused	
15	RXE1-	TXE1-	RXE1	TXE1	RXE1	TXE1	47	RXE3-	TXE3-	RXE3	TXE3	RXE3	TXE3
16	RXE1+	TXE1+	Unused		Unused		48	RXE3+	TXE3+	Unused		Unused	
17	TXC2-	RXC2-	TXC2	TXC2	Unused		49	TXC4-	RXC4-	TXC4	RXC4	Unused	
18	TXC2+	RXC2+	Unused		Unused		50	TXC4+	RXC4+	Unused		Unused	
19	TXD2-	RXD2 -	TXD2	RXD2	Unused		51	TXD4-	RXD4-	TXD4	RXD4	Unused	
20	TXD2+	RXD2+	Unused		Unused		52	TXD4+	RXD4+	Unused		Unused	
21	TXE2-	RXE2-	TXE2	RXE2	TXE2	RXE2	53	TXE4-	RXE4-	TXE4	RXE4	TXE4	RXE4
22	TXE2+	RXE2+	Unused		Unused		54	TXE4+	RXE4+	Unused		Unused	
29	AUXC2-		AUXC2		RXC2	TXC2	55	AUXC4-		AUXC4		RXC4	TXC4
30	AUXC2+		Unused		TXC2	RXC2	56	AUXC4+		Unused		TXC4	RXC4
25	SPARE2-		SPARE2		RXD2	TXD2	57	SPARE4-		SPARE4		RXD4	TXD4
26	SPARE2+		Unused		TXD2	RXD2	58	SPARE4+		Unused		TXD4	RXD4
27	RXC2-	TXC2-	RXC2	TXC2	Unused		59	RXC4-	TXC4-	RXC4	TXC4	Unused	
28	RXC2+	TXC2+	Unused		Unused		60	RXC4+	TXC4+	Unused		Unused	
29	RXD2-	TXD2-	RXD2	TXD2	Unused		61	RXD4-	TXD4-	RXD4	TXD4	Unused	
30	RXD2+	TXD2+	Unused		Unused		62	RXD4+	TXD4+	Unused		Unused	
31	RXE2-	TXE2-	RXE2	TXE2	RXE2	TXE2	63	RXE4-	TXE4-	RXE4	TXE4	RXE4	TXE4
32	RXE2+	TXE2+	Unused		Unused		64	RXE4+	TXE4+	Unused		Unused	

Table 2- PMC (P4) Rear IO Connections

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CHAPTER 6: ORDERING OPTIONS

6.0 Ordering Information

PMC66 – SIO4BXR - SYNC - <*FIFO Size*> - <*Temperature*>

Option	Valid Selections	Description
FIFO Size	48KLC	(software selectable) 4K byte Tx / 8K byte Rx FIFO or 8K byte Tx / 4K byte Rx FIFO
	64K	(software selectable) 8K byte Tx / 16K byte Rx FIFO or 16K byte Tx / 8K byte Rx FIFO
	256K	32K byte Tx / 32K byte Rx FIFO
Temperature	<blank>	0°C to +70°C – Commercial (Standard)
	I	-40°C to +85°C – Industrial

Please consult our sales department with your application requirements to determine the correct ordering options. (quotes@generalstandards.com).

6.1 Interface Cable

General Standards Corporation can provide off-the-shelf or custom interface cables for the PMC66-SIO4BXR-SYNC board. The standard cable is a non-shielded, twisted pair 68-conductor ribbon cable for increased noise immunity. Several standard cable lengths are offered, or the cable length can be custom ordered. Versions of the cable are available with connectors on both ends, or the cable may be ordered with a single connector to allow the user to adapt the other end for a specific application. A standard cable is also available which will breakout the serial channels into four DB25 connectors. Shielded cable options are also available. Please consult our sales department for more information on cabling options and pricing.

6.2 Device Drivers

General Standards has developed many device drivers for the PMC66-SIO4BXR boards, including VxWorks, Windows, Linux, and LabView. As new drivers are always being added, please consult our website (www.generalstandards.com) or consult our sales department for a complete list of available drivers and pricing.

6.3 Custom Applications

Although the PMC66-SIO4BXR-SYNC board provides extensive flexibility to accommodate most user interfaces, some applications may require modifications to conform to a specialized user interface. General Standards Corporation has worked with many customers to provide customized versions based on the SIO4BXR boards. Please consult our sales department with your specifications to inquire about a custom application.

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APPENDIX A: PROGRAMMABLE OSCILLATOR PROGRAMMING

The four on-baord clock frequencies (one per channel) are supplied via a Cypress Semiconductor CY22393 Programmable Clock Generator. This chip must be reprogrammed in order to change the clock frequencies. This document supplies the information necessary to reprogram the on-board clock frequencies.

The serial drivers supplied by GSC should include routines to calculate and program the on-board oscillator for a given set of frequencies. Therefore, it should not be necessary for the user need the following reprogramming information. It is provided for documentation purposes. Please contact GSC for help in setting up the on-board oscillator.

The CY22393 contains several internal address which contain the programming information. GSC has mirrored this data internal to the FPGA to allow the user to simply setup the data in the FPGA RAM and then command the on-board logic to program the clock chip. This isolates the user from the hardware serial interface to the chip. For detailed CY22393 programming details, please refer to the Cypress Semiconductor CY22393 data sheet.

The GSC CLOCK RAM (internal to FPGA) is accessed through 2 registers at local offsets 0x00A0 (Address Reg) and 0x00A4 (Data Reg). The user simply sets the RAM Address register to the appropriate offset, then reads or writes the the RAM data. The Programmable Osc Control/Status register allows the user to program the CY22393 or setup the clock post-dividers.

The GSC Local Programmable Clock Registers are defined as follows:

0x00A0 – RAM Address Register

Defines the internal CLOCK RAM address to read/write.

0x00A4 – RAM Data Register

Provides access to the CLOCK RAM pointed to by the RAM Addr Register.

0x00A8 – Programmable Osc Control/Status Register

Provides control to write the contents of the CLOCK RAM to the CY22393 and setup additional post-dividers for the input clocks.

Control Word (Write Only)

D0	Program Oscillator 1 = Program contents of CLOCK RAM to CY22393. Automatically resets to 0.
D1	Measure Channel 1 Clock
D2	Measure Channel 2 Clock
D3	Measure Channel 3 Clock
D4	Measure Channel 4 Clock
D5	Reserved (Unused)
D6	Status Word Readback Control 0 => Status Word D31-D8 == Measured Channel Value 1 => Status Word D31-D8 == Control Word D23-D0
D7	Post-divider set 0 = Ignore D23-D8 during Command Word Write 1 = Set Channel Post-Dividers from D23-D8 during Command Word Write
D11-D8	Channel 1 Post-Divider

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D15-D12	Channel 2 Post-Divider
D19-D16	Channel 3 Post-Divider
D23-D20	Channel 4 Post-Divider
D31-D24	Reserved (Unused)

Status Word (Read Only)

D0	Program Oscillator Done 0 = Oscillator Programming in progress.
D1	Program Oscillator Error 1 = Oscillator Programming Error has occurred.
D2	Clock Measurement complete. 0 = Clock Measurement in progress.
D7-D3	Reserved (Unused)
D31-D8	If Command Word D6 = 0, Measured Channel Clock Value If Command Word D6 = 1, Control Word D23-D0

Channel Clock Post-Dividers:

The Control Word defines 4 fields for Channel Clock Post-dividers, one field for each channel (D8-D23). These post-dividers divide down the clocks from the programmable oscillator (CY22393 outputs) to provide for slower baud rates. These divided-down clocks are used as the final programmable clock values. Each 4 bit field will allow a post divider of 2^n. For example, if the post-divider value=0, the input clock is not post-divided. A value of 2 will provide a post-divide of 4 (2^2). This will allow for a post-divide value of up to 32768 (2^15) for each input clock.

Bit D7 of the Control Word qualifies writes to the post-divide registers. This allows other bits in the command register to be set while the post-divide values are maintained.

A value of '0' in the post divider field will bypass the post-divider (final programmamle clock = CY22393 output).

Channel Clock Measurement:

The Control Word defines 4 bits which will select one of the 4 channel clocks (input clock + post-divide) for a measurement. This will allow the user feedback as to whether the programmable oscillator was programmed correctly. To measure a clock, select the clock to measure in the Control word, and also clear Bit D6 to allow for readback of the result. Read back the Status Word until D2 is set. Status Word D31-D8 should contain a value representing 1/10 the measured clock frequency (Value * 10 = Measured Frequency in MHz). Keep in mind that this value will not be exactly the programmed frequency due to the 100ppm (0.01%) accuracy of the on-board reference.

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The Internal FPGA RAM is defined as follows: RAM Address 0x08–0x57 correspond directly to the CY22393 registers. Do not change 'Reserved' values from their defaults.

Address	Description	Default Value
0x00 – 0x05	Reserved (Unused)	0x00
0x06	Reserved	0xD2
0x07	Reserved	0x08
0x08	ClkA Divisor (Setup0)	0x01
0x09	ClkA Divisor (Setup1)	0x01
0x0A	ClkB Divisor (Setup0)	0x01
0x0B	ClkB Divisor (Setup1)	0x01
0x0C	ClkC Divisor	0x01
0x0D	ClkD Divisor	0x01
0x0E	Source Select	0x00
0x0F	Bank Select	0x50
0x10	Drive Setting	0x55
0x11	PLL2 Q	0x00
0x12	PLL2 P Lo	0x00
0x13	PLL2 Enable/PLL2 P Hi	0x00
0x14	PLL3 Q	0x00
0x15	PLL3 P Lo	0x00
0x16	PLL3 Enable/PLL3 P Hi	0x00
0x17	OSC Setting	0x00
0x18	Reserved	0x00
0x19	Reserved	0x00
0x1A	Reserved	0xE9
0x1B	Reserved	0x08
0x1C-0x3F	Reserved (Unused)	0x00
0x40	PLL1 Q (Setup0)	0x00
0x41	PLL1 P Lo 0 (Setup0)	0x00
0x42	PLL1 Enable/PLL1 P Hi (Setup0)	0x00
0x43	PLL1 Q (Setup1)	0x00
0x44	PLL1 P Lo 0 (Setup1)	0x00
0x45	PLL1 Enable/PLL1 P Hi (Setup1)	0x00
0x46	PLL1 Q (Setup2)	0x00
0x47	PLL1 P Lo 0 (Setup2)	0x00
0x48	PLL1 Enable/PLL1 P Hi (Setup2)	0x00
0x49	PLL1 Q (Setup3)	0x00
0x4A	PLL1 P Lo 0 (Setup3)	0x00
0x4B	PLL1 Enable/PLL1 P Hi (Setup3)	0x00
0x4C	PLL1 Q (Setup4)	0x00
0x4D	PLL1 P Lo 0 (Setup4)	0x00
0x4E	PLL1 Enable/PLL1 P Hi (Setup4)	0x00
0x4F	PLL1 Q (Setup5)	0x00
0x50	PLL1 P Lo 0 (Setup5)	0x00
0x51	PLL1 Enable/PLL1 P Hi (Setup5)	0x00
0x52	PLL1 Q (Setup6)	0x00
0x53	PLL1 P Lo 0 (Setup6)	0x00
0x54	PLL1 Enable/PLL1 P Hi (Setup6)	0x00
0x55	PLL1 Q (Setup7)	0x00
0x56	PLL1 P Lo 0 (Setup7)	0x00
0x57	PLL1 Enable/PLL1 P Hi (Setup7)	0x00
0x58-0xFF	Reserved (Unused)	0x00

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APPENDIX B: FIRMWARE REVISIONS / FEATURES REGISTER

Since SIO4 boards can exist across multiple form factors and with various hardware features, the firmware/features registers attempt to help identify the exact version of a SIO4 board. This appendix provides a more detailed breakdown of what the firmware and features registers, and detail differences between the firmware revisions.

Firmware Register - Local Offset 0x00 (0xE2250418)

D31:16 HW Board Rev 0xE225 PMC66-SIO4BXR Rev E

- D31 **1** = Features Register Present
- D30 **1** = Complies with this standard
- D29 **1** = 66MHz PCI bus interface
  0 = 33MHz PCI bus interface
- D28 1 = 64 bit PCI bus interface
  0 = 32 bit bus interface
- D27:D24 Form Factor
  0 = Reserved
  1 = PCI
  2 = PMC
  3 = cPCI
  4 = PC104P
  5 = PCIe
  6 = XMC
- D23:D20 HW Board (sub-field of form factor)
  0 = PMC-SIO4AR
  1 = PMC-SIO4BX
  2 = PMC66-SIO4BXR
- D19:D16 HW Board Rev (lowest rev for firmware version)
  0=NR
  1=A,
  2=B
  3=C
  4=D
  5=E

D15:8	Firmware Type ID	0x01	Std Firmware default
		0x04	Sync Firmware default
D7:0	Firmware Revision	XX	Firmware Version

0x1D - External Timestamp bug fix (Common PLX9056 code release)
0x1C - USC Timestamp / RCSR bug fix
0x1B - Add RxBit, Sync Timestamp, speed up DMA to 0 wait, “speedup” bug fixes
0x1A - Rework SRAM, USC, Tx/Rx IF
0x19 - Revert to v117 with Rev E support, Add Rx Stop on Full to Ch Ctrl
0x18 - Add Rev E, speed up SRAM, USC, Tx/Rx IF
0x17 - External SRAM bug, adjust FIFO read timing, enhance Clock Programming
0x16 - Fix Rx (Sync)
0x15 - Add Channel reset, SRAM pipeline, Envelope Delay (Sync), PinSrcB Reg (Sync), fix Ch4 Configurable FIFO

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D7:0 Firmware Revision (cont)

0x14 - Add Configurable FIFO size, Tx fix (Sync)
0x13 - Add Sync code
0x12 - (Standard release) Remove External Timestamp Clock
0x11 - (Timestamp release) External FIFO Fix
0x10 - (Timestamp release) Add status word feature (RCSR inserted in FIFO) (always 256k)
0x09 - (Timestamp release) External FIFO fix (always 256k)
0x08 - (Timestamp release) Add Biphase encoder/decoder workaround
0x07 - (Timestamp release) Allow 32 bit FIFO access
0x06 - (Timestamp release) Add timestamp control, add support for 9 bit FIFO
0x05 - HW Rev D release
0x04 - HW Rev C release
0x03 - Falling interrupt edge fix, add LED control, link in 4th PLL (Internal Only)
Note: v103 was post released on Rev D with ProgClk fix (from v117)
0x02 - Add code for 4th programmable PLL (Internal Only)
0x01 - Add RS423 support (Internal Only)
0x00 - Initial Release (Internal Only)

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Feature Register - Local Offset 0xFC (0x00F97AF4)

D31:24	RESERVED
D23	**1 =** Sync Timestamp + RxWord Bit Size
D22	**1 =** Rx Stop on Full in Ch_Ctrl
D21	**1 =** SRAM Debug
D20	**1** = Rx Status byte (std only)
D19:D18	Std Timestamp
	01 = single external clock
	10 = single internal clock
D17:D16	FPGA Reprogram field
	01 = Present
	00 = Not Present
D15:D14	Configurable FIFO space
	01 - Rx/Tx select. Up to 32k deep FIFOs
D13	**1** = FIFO Test Bit
D12	**1** = FW Type Reg
D11:D8	FW Feature Level (Set at common code level)
	0x0A = Falling Int fix
	0x09 = No Legacy Support (No Clock Control Register)
	0x08 = Clock to 50Hz with 10Hz resolution
	0x07 = Rx Underrun Only, Reset Status
	0x06 = DMA_Single_Cycle_Dis, updated Pin_Src
	0x05 = Demand mode DMA Single Cycle for Tx
	0x04 = FIFO Latched Underrun/Overrun/Level
	0x03 = Common Internal/External FIFO Support
	0x02 = Multi-Protocol support
	0x01 = RS232 support, Pin Source Change
D7	**1** = DMA Single Cycle Disable
D6	**1** = Board Reset, FIFO present bits
D5	**1** = FIFO Size/Counters present
D4	**1** = FW ID complies with this standard
D3:D0	Clock Oscillator
	0x0 = Fixed
	0x1 = ICD2053B (1 Osc)
	0x2 = ICD2053B (4 Osc)
	0x3 = CY22393 (4 Osc)
	0x4 = 2 x CY22393 (6 Osc)

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