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Rev: 090406

PMC-16AI64

64-CHANNEL 16-BIT
PMC ANALOG INPUT BOARD

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC-16AI64 board is a single-width PCI mezzanine card (PMC) that provides high-speed 16-bit analog input capability for PMC applications. 64 analog input lines can be configured either as 64 single-ended input channels or as 32 differential channels, and are digitized at rates up to 500,000 conversions per second in single-channel mode. The voltage range is software controlled as ±2.5V, ±5V or ±10V. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.2, and is mechanically and electrically compatible with the IEEE compact mezzanine card (CMC) specification IEEE 1386. A PCI interface adapter supports the "plug-n-play" initialization concept.

Power requirements consist of +5 VDC from the PCI bus in accordance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling. Specific details of physical characteristics and power requirements are contained in the PMC-16AI64 product specification. Figure 1.1-1 shows the physical configuration of the board, and the arrangement of major components.

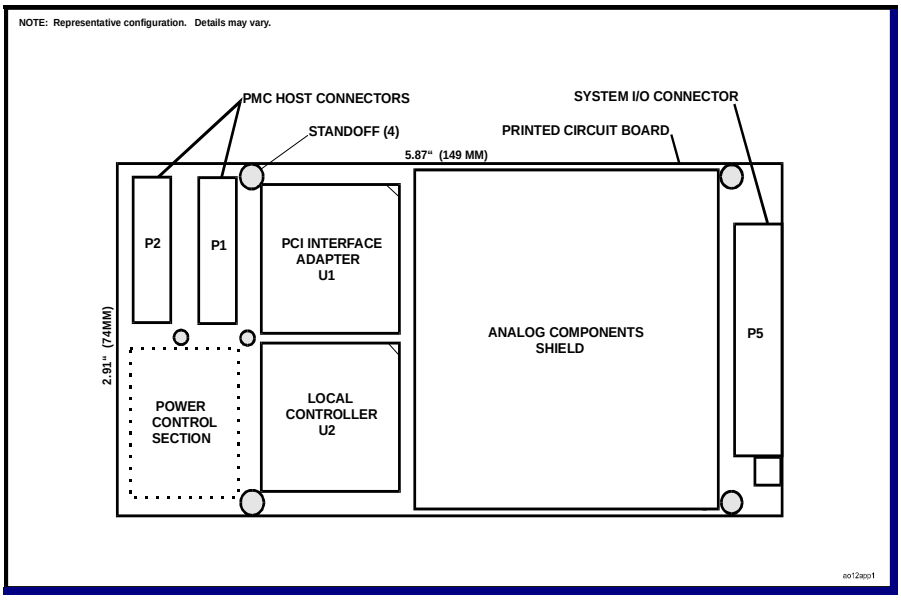


Figure 1.1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and autocalibration features that eliminate the need for disconnecting or removing the module from the system for calibration. All system input and output connections are made through a single 68-pin, dual-ribbon front-access I/O connector.

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1.2 Functional Overview

Principal capabilities of the PMC-16AI64 board are summarized in the following list of features:

- ❑ 64 Single-Ended or 32 Differential 16-Bit Scanned Analog Input Channels
- ❑ Software-Selectable Analog Input Ranges of ±10V, ±5V or ±2.5V
- ❑ 64K-Sample Analog Input FIFO Buffer
- ❑ 500 KSPS Conversion Rate in Single-Channel Mode; 1.0 MSPS in Multichannel Mode;
- ❑ Multiple-Channel and Single-Channel Input Scanning Modes
- ❑ Dual cascadable Internal Rate Generators
- ❑ Supports Multiboard Synchronization of Analog Inputs
- ❑ Internal Autocalibration of Analog Input Channels
- ❑ Mastering DMA Engine

The PMC-16AI64 board is a scanning analog digitizer that performs high-speed sampling and 16-bit A/D conversion of as many as 64 single-ended or 32 differential analog input channels. The resulting 16-bit sampled data is available to the PCI bus through a data buffer that is configured as a 64K-Sample FIFO. All operational parameters are software configurable.

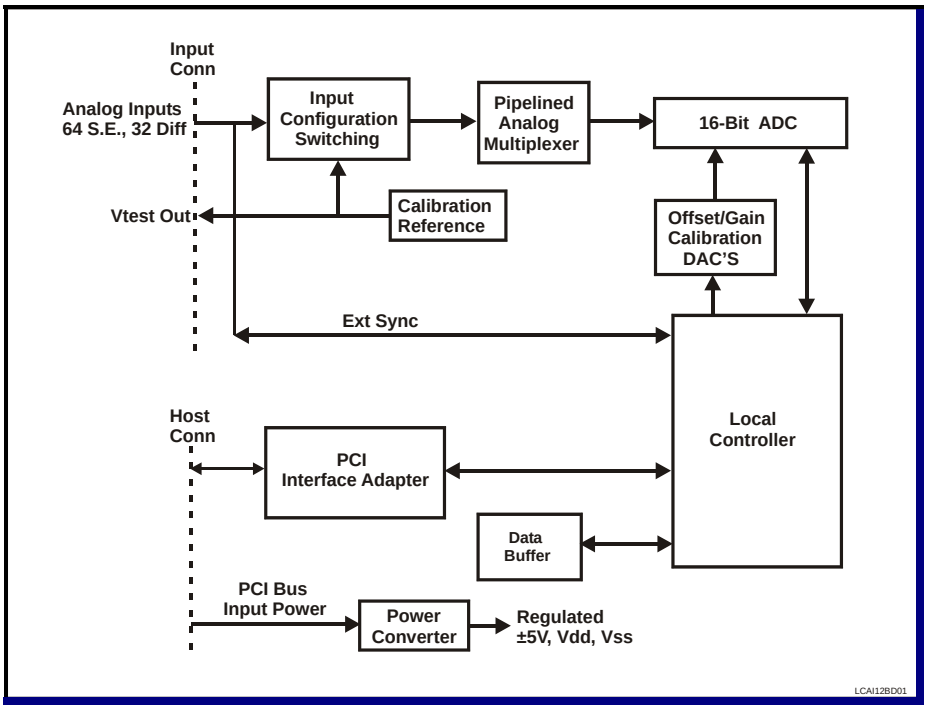


Figure 1.2-1. Functional Organization

The analog inputs can be sampled in scans of 2, 4, 8, 16, 32 or 64 single-ended channels, or in scans of 2, 4, 8, 16 or 32 differential channels. The scan rate can be controlled internally or externally up to 175,000 scans per second for a 2-channel scan. Sync input and output signals permit multiple boards to perform synchronous scanning. Input buffer amplifiers on all channels eliminate the high input currents that are produced by nonbuffered multiplexers running at high scan rates.

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An internal autocalibration utility uses hardware D/A converters to correct for offset and gain errors in the input signal path, and eliminates the missing codes that are inevitably introduced when software correction methods are used. A selftest switching network routes calibration signals through the input multiplexer to the A/D converter to support internal autocalibration, and permits board integrity to be tested by the host. Autocalibration is performed automatically after reset or upon demand from the PCI bus, and calibrates the offset and gain of the converter to a precision internal reference voltage.

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SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector, with the mating connectors on the host board. Then carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the standoffs and bezel are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four mounting holes on the board. Tighten the screws carefully to complete the installation. Do not overtighten.

2.2.2 Input/Output Cable Connections

System cable signal pin assignments are listed in Table 2.2-1. The I/O connector is designed to mate with a 68-pin dual-ribbon connector, equivalent to Robinson Nugent #P50E-068-S-TG. The insulation displacement (IDC) Robinson Nugent cable connector accepts two 34-wire 0.050-inch ribbon cables, with the pin numbering convention shown in Table 2.2-1 and in Figure 2.2-1. Contact the factory if preassembled cables are required.

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Table 2.2-1. System I/O Connector Pin Functions

PIN	ROW-A SIGNAL	
	S.E. MODE	DIFF MODE
1	INP00	INP00 HI
2	INP01	INP00 LO
3	INP02	INP01 HI
4	INP03	INP01 LO
5	INP04	INP02 HI
6	INP05	INP02 LO
7	INP06	INP03 HI
8	INP07	INP03 LO
9	INP08	INP04 HI
10	INP09	INP04 LO
11	INP10	INP05 HI
12	INP11	INP05 LO
13	INP12	INP06 HI
14	INP13	INP06 LO
15	INP14	INP07 HI
16	INP15	INP07 LO
17	AGND	AGND
18	AGND	AGND
19	INP16	INP08 HI
20	INP17	INP08 LO
21	INP18	INP09 HI
22	INP19	INP09 LO
23	INP20	INP10 HI
24	INP21	INP10 LO
25	INP22	INP11 HI
26	INP23	INP11 LO
27	INP24	INP12 HI
28	INP25	INP12 LO
29	INP26	INP13 HI
30	INP27	INP13 LO
31	INP28	INP14 HI
32	INP29	INP14 LO
33	INP30	INP15 HI
34	INP31	INP15 LO

PIN	ROW-B SIGNAL	
	S.E. MODE	DIFF MODE
1	INP32	INP16 HI
2	INP33	INP16 LO
3	INP34	INP17 HI
4	INP35	INP17 LO
5	INP36	INP18 HI
6	INP37	INP18 LO
7	INP38	INP19 HI
8	INP39	INP19 LO
9	INP40	INP20 HI
10	INP41	INP20 LO
11	INP42	INP21 HI
12	INP43	INP21 LO
13	INP44	INP22 HI
14	INP45	INP22 LO
15	INP46	INP23 HI
16	INP47	INP23 LO
17	AGND	AGND
18	AGND	AGND
19	INP48	INP24 HI
20	INP49	INP24 LO
21	INP50	INP25 HI
22	INP51	INP25 LO
23	INP52	INP26 HI
24	INP53	INP26 LO
25	INP54	INP27 HI
26	INP55	INP27 LO
27	INP56	INP28 HI
28	INP57	INP28 LO
29	INP58	INP29 HI
30	INP59	INP29 LO
31	INP60	INP30 HI
32	INP61	INP30 LO
33	INP62/ SYNC HI *	INP31 HI/ SYNC HI*
34	INP63/ SYNC LO*	INP31 LO/ SYNC LO*

* Software-selected.

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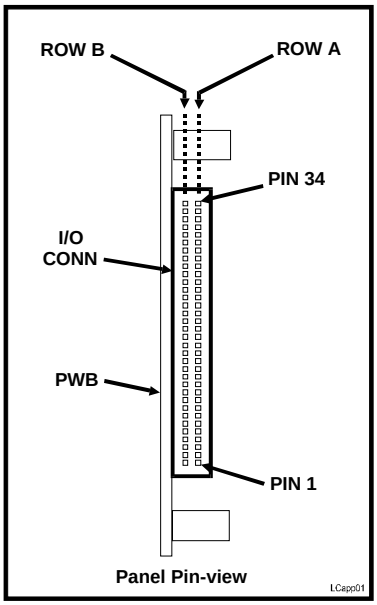


Figure 2.2-1. Input/Output Connector

2.3 System Configuration

2.3.1 Analog Inputs

2.3.1.1 Single-Ended Inputs

Analog inputs can be configured either as 64 single-ended channels or as 32 differential channels. The hardware input configuration must be acknowledged by the control software, which configures the controller for either single-ended or differential operation. Pull-down resistors are provided on all analog inputs. Table 2.2-1 provides separate pin assignment columns for single-ended and differential input configurations.

Single-ended operation (Figure 2.3-1a) offers the maximum number of input channels, but generally provides optimum performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return.

Single-ended inputs share a common input return that provides a return path for all inputs, making isolation from other system grounds a critical issue. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and input return can cause erroneous measurements, or may generate excessive ground current and damage the board.

2.3.1.2 Differential Inputs

Differential input operation usually provides the best performance, and is essential when the input signal sources are not isolated from each other and have returns that are at significantly different potentials. A potential difference between grounds is significant if it is larger than the maximum tolerable measurement error.

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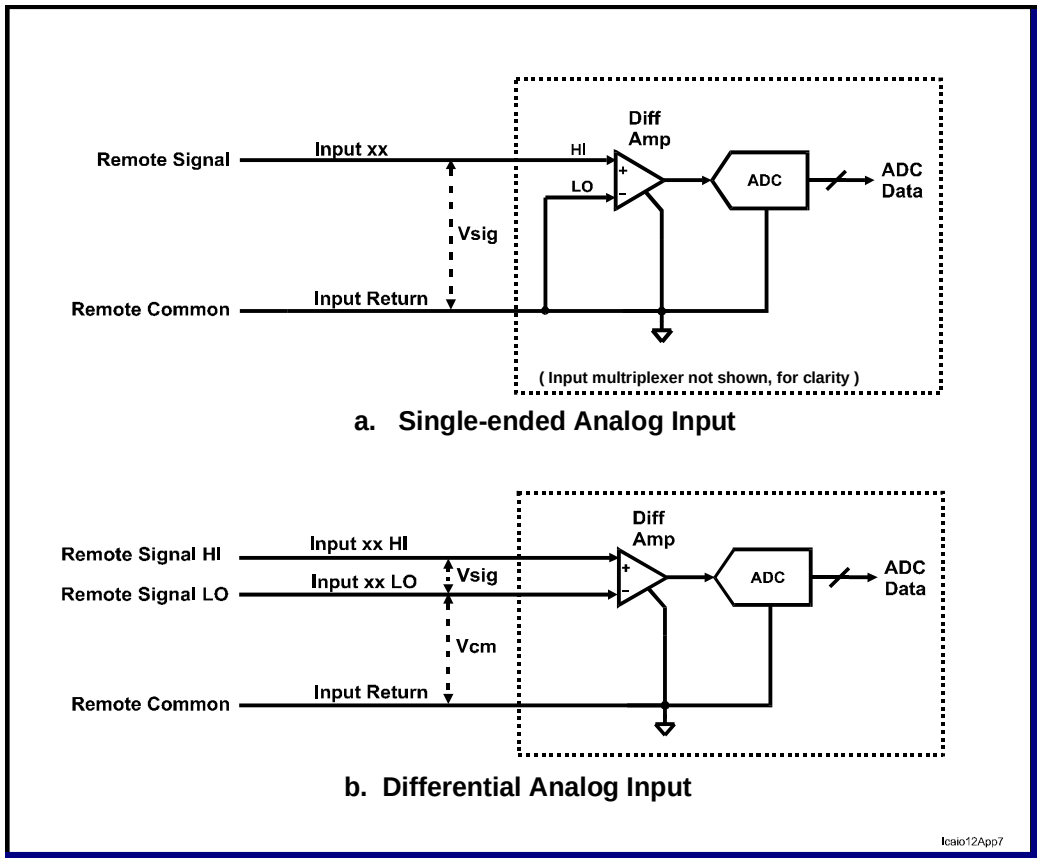


Figure 2.3-1. Analog Input Configurations

This operating mode also offers the highest rejection of the common mode noise that is a characteristic of long cables in typical instrumentation environments. When operating in the differential mode, shown in Figure 2.3-1b, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return (INPUT RTN in Table 2.2-1) is connected to a ground point that: (a) ensures that the common mode voltage of all signals remains within the range specified for the board, and (b) will not produce potentially destructive ground currents.

2.3.2 External Sync

Pins 33 and 34 of I/O connector Row-B can be software-configured as a bidirectional TTL SYNC signal that provides external control of analog input scan timing. The SYNC signal is present on the SYNC HI pin, and is referenced to the SYNC LO pin, which is connected internally to digital ground.

When configured as an input, this signal initiates a single scan of all active input channels. The SYNC input signal is asserted LOW, and is pulled HIGH internally through a 4.7 KOhm resistor.

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When configured as an output, the SYNC signal is asserted for approximately 75-90 nanoseconds at the beginning of each scan. The SYNC output signal is a TTL level that is available for synchronizing the operation of multiple target boards to a single initiator board. Like the SYNC input signal, the SYNC output signal is asserted LOW. Loading of the SYNC output should be limited to 10 milliamps or less.

Specific input/output configurations are determined by individual system requirements, and must be acknowledged by the control software.

2.3.3 Multiboard Synchronization

If multiple boards are to be synchronized together, the SYNC HI and LO pins from one board, the *initiator*, are connected to the SYNC HI and LO pins of as many as three *target* boards (Figure 2.3-2). The controlling software determines specific synchronization functions.

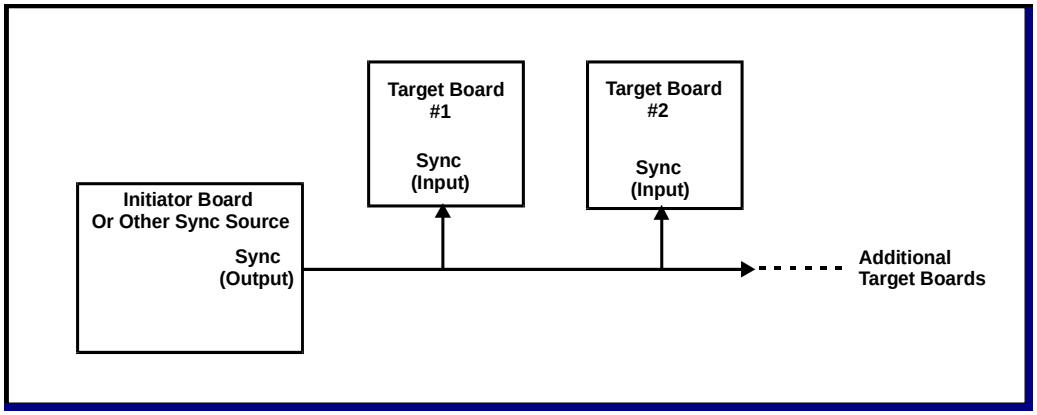


Figure 2.3-2. Multiboard Synchronization

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference verification and possible adjustment. The optimum verification interval will vary, depending upon the specific application, but in most instances an interval of one year is sufficient.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and system interface signal levels, should be evaluated before troubleshooting of the board itself is attempted. A board that is suspected to be defective should be returned to the factory for detailed problem analysis and repair.

2.5 Reference Verification

All analog input channels are software-calibrated to a single internal voltage reference by an embedded autocalibration software utility. The procedure presented here describes the verification and adjustment of the internal reference.

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2.5.1 Equipment Required

Table 2.5-1 lists the equipment required for verifying or adjusting the internal reference. Alternative equivalent equipment may be used.

Table 2.5-1. Reference Verification Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Test cable; suitable for connecting the digital multimeter to two 0.024-inch square test posts.	---	---

2.5.2 Verification and Adjustment

The following procedure describes the verification of the single reference voltage that ensures conformance to the product specification. Adjustment of the internal reference, if necessary, is performed with an internal trimpot that is accessible from the front of the board, as shown in Figure 2.5-1. Two right-angle 0.024-inch pins provide side-access to the VTEST and VTEST RTN test points.

This procedure assumes that the board is installed on a host board, and that the host is installed in an operating system. The board can be operating in any mode while the adjustment is performed.

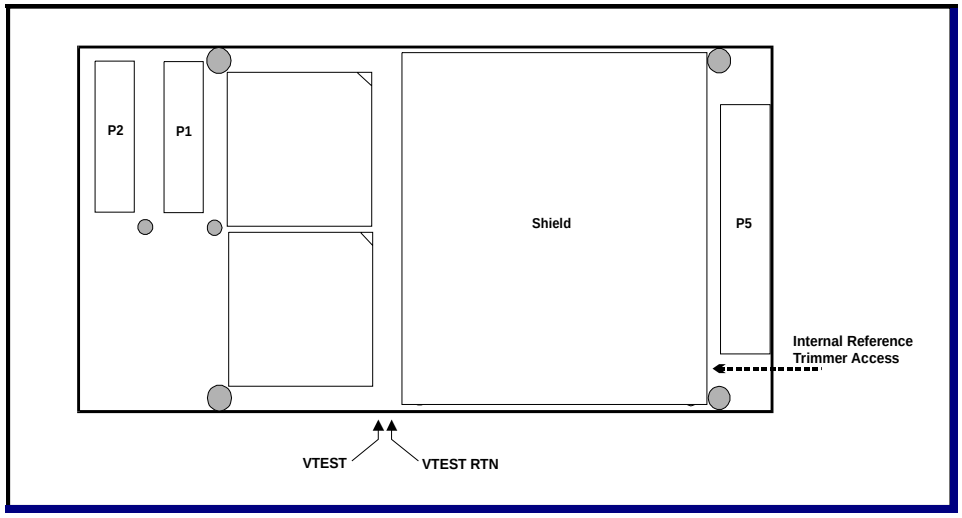


Figure 2.5-1. Reference Adjustment Access

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1. Connect the digital multimeter between the VTEST (+) and VTEST RTN (-) pins at the edge of the board (Figure 2.5-1). Reverse the test leads if a negative voltage is indicated.
2. If power has been removed from the board, apply power now. Wait at least 10 minutes after power is applied before proceeding..
3. Verify that the digital multimeter indication is +9.4780 VDC ±0.0009 VDC. If the indication is not within this range, adjust the INTERNAL REFERENCE trimmer until the digital multimeter indication is within the specified range.
4. Verification and adjustment is completed. Remove all test connections.

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SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC-16AI64 board is compatible with the PCI Local Bus specification, and supports auto configuration at the time of power-up. A PLX™ PCI-9080 I/O accelerator device controls the PCI interface. Configuration-space registers are initialized internally to support the location of the board on any 16-longword boundary in memory space. After initialization has been completed, communication between the PCI bus and the local bus takes place through the control and data registers shown in Table 3.1-1. All data transfers are long-word D32. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board. DMA access is supported for data transfers from the analog input data buffer.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	ACTIVE BITS	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	16	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	12	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	16	---	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	18	000X FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	17	0001 0960h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	17	0000 0050h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	16	0000 0000h	Number of values in the input buffer
001C	(Reserved)	---	---	---	Inactive
0020	SCAN AND SYNC CONTROL	R/W	19	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	(Reserved)	---	---	---	Inactive
0028	(Reserved)	---	---	---	Inactive
002C	(Reserved)	---	---	---	Inactive
0030-3F	(Reserved)	---	---	---	Inactive

R/W = Read/Write, RO = Read-Only.

3.2 Board Control Register (BCR)

As Table 3.2-1 indicates, the BCR consists of 16 control bits and status flags. Specific control bits are cleared automatically after the associated operations have been completed. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section.

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Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	AIM0	0	Analog input mode. Selects input configuration or selftest mode. Defaults to differential input mode. .
D01	R/W	AIM1	0	
D02	R/W	AIM2	0	
D03	R/W	(Reserved)	0	---
D04	R/W	RANGE0	0	Analog input range. Defaults to ±10V range.
D05	R/W	RANGE1	1	
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.
D07	R/W	ENABLE EXTERNAL SYNC	0	Configures the board for external sync I/O when HIGH. (SYNC I/O pins are reassigned as a TTLI/O pair).
D08-11	R/W	(Reserved)	0	---
D12	R/W	*INPUT SYNC	0	Triggers a single sample of active channels when BCR Input Sync is selected in the Scan and Sync Control Register. Clears automatically upon scan completion,
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets defaults for all registers.
D16-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only. *Clears automatically when operation is completed

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRY's. Configuration operations are executed in the sequence shown in Table 3.3-1.

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted as described in Section 3.7.

Table 3.3-1. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

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Loading of the PCI configuration registers is completed within 3 milliseconds or less after the assertion of a PCI bus reset, and should be required only once after the initial application of power. During this interval, the response to PCI target accesses is RETRYs. PCI register configuration terminates with the PCI interrupts disabled (Section 3.7).

3.3.2 Initialization

Internal control logic is initialized without invoking configuration, by setting the INITIALIZE control bit in the BCR. This action initializes the internal logic, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following default conditions:

- The BCR is initialized; all defaults are invoked.
- Calibration D/A converters are initialized to midrange.
- Analog input voltage range is ±10 Volts.
- Analog inputs are configured as 32 differential channels.
- Input scan clocking is from the Rate-A generator at 10,000 scans per second.
- Analog input data coding format is offset binary.
- The analog input buffer is reset to empty.
- Input rate generator Rate-A is disabled (Rate Generator Register D16 = HI).

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Input Parameters

3.4.1 Input Voltage Range

BCR control field RANGE[], as shown in Table 3.4-1 selects the analog input voltage range.

Table 3.4-1. Analog Voltage Range Selection

RANGE[1:0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±5 Volts
2	±10 Volts
3	±10 Volts

3.4.2 Timing Organization

Figure 3.4-1 illustrates the manner in which timing signals are organized within the board. The input scan clock multiplexer is controlled by the Scan and Sync control register, which provides direct software control of clocking and sync operations. The external sync input and output lines permit external control of timing. Two rate generators operate directly from the master clock, which has a frequency of 24 MHz on the PMC-16AI64 board.

Each Input Scan Clock initiates a complete scan of all active input channels at the maximum conversion rate. An input scan can contain from two to 64 channels, or any single channel can be digitized at the maximum conversion rate. Each multiple-channel scan commences with Channel 00, and proceeds upward through consecutive channels until the selected number of channels has been digitized.

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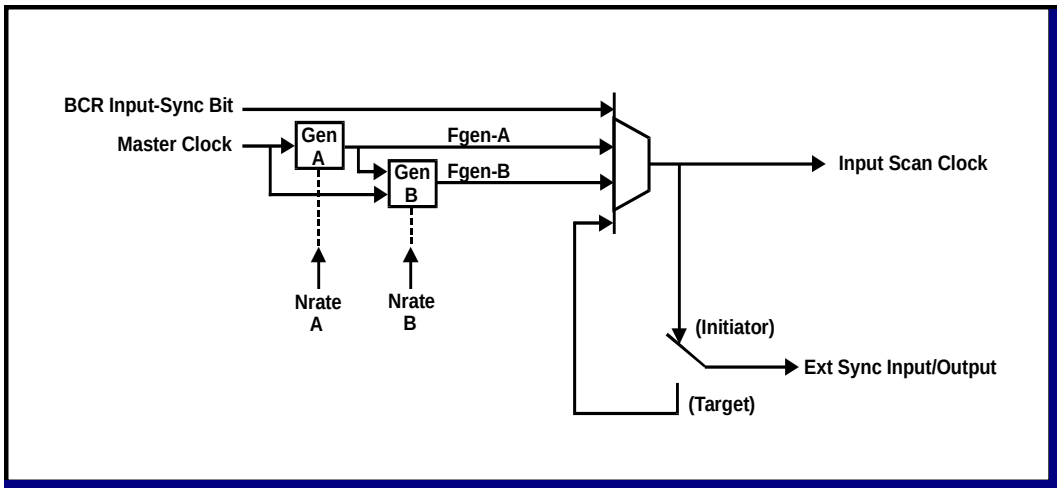


Figure 3.4-1. Clock and Sync Organization

3.4.3 Scan and Sync Control Register

The Scan and Sync control register (Table 3.4-2) controls the configuration of internal timing signals. Bits D00-02 select the number of channels in an input scan size from two channels to 64 channels, or select the single-channel mode if zero. (See Paragraph 3.5.5; Scanning Modes).

3.4.4 Scan-Trigger Rate Generators

Each of the two rate generators consists of a 16-bit down-counter that divides the master clock frequency by a 16-bit integer contained in the associated rate register. The two rate registers are organized as shown in Table 3.4-3. Bits D00-D15 represent the frequency divisor Nrate, and D16 disables the associated generator when set HIGH. To prevent the input buffer from filling with extraneous data at power-up, D16 defaults to the HIGH state in the Rate-A control register.

3.4.4.1 Scan Rate Control

Each rate generator contains a divisor that can be adjusted up to a maximum value of FFFFh (65535 decimal). With a master clock frequency of 24 MHz, the output frequency **Fgen** of each generator is determined as:

$$\textbf{Fgen (Hz) = 24,000,000 / Nrate,}$$

where **Nrate** is the decimal equivalent of D0-D15 in the rate generator register. **Fgen** is the scanning trigger frequency, and establishes the rate at which complete scans are initiated. The maximum permissible scanning frequency **Fgen-max** equals the maximum conversion rate, divided by the number of channels in a scan:

$$\textbf{Fgen-max = Fconv / Nchan,}$$

where **Fconv** is 500 kHz in the single-channel sampling mode (Nchan = 1), and 350 kHz for multichannel scanning. Values for **Fgen** higher than **Fgen-max** will produce unpredictable results, and are not recommended. Table 3.4-5 provides examples of various scan rates and scan sizes.

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Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D02	R/W	SCAN SIZE	5	Number of input channels per scan: 0 => Single-Channel mode * 1 => 2 channels per scan 2 => 4 channels per scan 3 => 8 channels per scan 4 => 16 channels per scan 5 => 32 channels per scan (Default value) 6 => 64 channels per scan (S.E. mode only) 7 =>(Reserved) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	ANALOG INPUTS SCAN CLOCK	0	Selects the analog input scan clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line 3 => BCR Input Sync control bit.
D05-D09	R/W	(Reserved)	0	---
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	(Reserved)	0	---
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	(Reserved)	0	---
D19-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-3. Scan-Trigger Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 0960 (Rate-A), 0000 0050h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

Table 3.4-4. Scan-Trigger Rate Generator Frequency Selection

Nrate	(RATE[15..0])	FREQUENCY Fgen *
(Dec)	(Hex)	(Hz)
48	0030	500,000
49	0031	489,796
---	---	Fgen (Hz) = 24,000,000 / Nrate
65534	FFFE	366.222
65535	FFFF	366.217

* ±0.015 percent.

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Table 3.4-5. Scan-Trigger Rate Examples

Channels Per Scan (Nchan)	Maximum Scan Rate (Fgen-max, Hz)	Required Scan Rate (Fgen, Hz)	Rate Generator Register (Nrate, Dec)
64	5.468	5,000	4,800
64	5,468	1,000	24,000
64	5,468	500	48,000
16	21,875	12,000	2,000
8	43,750	20,000	1,200
2	175,000	20,000	1,200
1 *	500,000	500,000	48
1 *	500,000	20,000	1,200

* Single-scan mode.

3.4.4.2 Generator Cascading

To provide very low scanning rates, the Rate-B generator can be configured to operate from the output of the Rate-A generator instead of from the master clock. When operating in this *cascaded* configuration, the output frequency of the Rate-B generator is:

Fgen-B (Hz) = 24,000,000 / (Nrate-A * Nrate-B) ,

which can produce scan triggering rates as low as 0.0056 Hz.

3.4.5 Multiboard Synchronization

Multiple boards can be externally interconnected to produce analog input scans simultaneously. Figure 2.3-2 illustrates the interconnections required. External sync I/O is enabled by setting the ENABLE EXTERNAL SYNC control bit HIGH in the BCR. One of the boards is designated as the *Initiator*, and the remaining boards are designated as *targets*.

A board that is enabled for external sync I/O is designated as a *target* by selecting the External Sync Input Line with the ANALOG INPUTS SCAN CLOCK field in the Scan and Sync control register. Any other value for the ANALOG INPUTS SCAN CLOCK field designates the board as an *initiator*, and routes the internal scan clock to the I/O connector. The sync signal can originate either on the initiator board itself, or externally as an input to a group of targets.

The initiator generates a sync pulse at the beginning of each scan, and each of the target boards responds to the sync pulse by initiating a single input scan. The initiator and target boards can be operating with various scan sizes, but the duration, or period, of the initiator scan must equal or exceed those of the targets in order to avoid "dropping" target scans. Also, the scan rate selected for the target boards should be slightly higher than that of the initiator board.

NOTE: Enabling external sync I/O reassigns the function of the SYNC pins in the I/O connector as a bidirectional TTL port. Voltages applied externally in this configuration must not extend outside the range of -0.5V to +7V.

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3.5 Analog Input Control

3.5.1 Input Data Organization

Conversion data from the analog-to-digital converter (ADC) flows through a transfer register into the analog input data buffer, and from the data buffer to the PCI bus as analog input data. The data buffer appears to the PCI bus as a single read-only register.

3.5.1.1 Input Data Buffer

Analog input data is read from the Analog Input Data Buffer in longword-serial format, as shown in Table 3.5-1. Each value is right-justified to the LSB, and occupies bit positions D00 through D15. D16-D31 are always returned as zero's. The capacity of the input data buffer is 64K-samples.

Table 3.5-1. Input Data Buffer

Offset: 0008h **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16-D31	RO	(Inactive)	---

* RO indicates read-only access. Write-data is ignored.

3.5.1.2 Data Coding Format

Analog input data is arranged as 16 active right-justified data bits with the coding conventions shown in Table 3.5-2. The default format is offset binary. Two's complement format is selected by clearing the Offset Binary control bit LOW in the BCR.

Note: Unless indicated otherwise, offset binary coding is assumed throughout this document.

Table 3.5-2. Input Data Coding; 16-Bit Data

ANALOG INPUT LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	0000 FFFF	0000 7FFF
Zero plus 1 LSB	0000 8001	0000 0001
Zero	0000 8000	0000 0000
Zero minus 1 LSB	0000 7FFF	0000 FFFF
Negative Full Scale plus 1 LSB	0000 0001	0000 8001
Negative Full Scale	0000 0000	0000 8000

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3.5.2 Input Data Buffer Control

The Input Data Buffer control register shown in Table 3.5-3 controls and monitors the flow of data through the analog input data buffer. Asserting the Clear Buffer control bit HIGH clears, or empties, the buffer, and aborts any input scan that might be in progress. The Threshold Flag is HIGH when the number of values in the input data buffer exceeds the input threshold value defined by bits D00-D15, and is LOW if the number is equal to or less than the threshold value. An interrupt (Section 3.7) can be programmed to occur on either the rising or falling edge of the threshold flag.

The Buffer Size register shown in Table 3.5-4 contains the number of input values present in the buffer, and is updated continuously.

Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0000 FFFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-15	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D16	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer when asserted HIGH. Aborts current input scan.
D17	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D18-D31	RO	(Inactive)	0	---

*Clears automatically when operation is completed

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-15	RO	BUFFER SIZE	0000h	Number of values in the input buffer
D16-D31	RO	(Inactive)	0	---

3.5.3 Analog Input Function Modes

BCR control bits D00-D02 (AIM0-AIM2) control the analog input configuration, and provide selftest modes for monitoring the integrity of the analog input networks. Table 3.5-5 summarizes the input function modes.

3.5.3.1 Differential Inputs

The analog inputs default to the differential configuration when power is applied, or after initialization. In this mode, the 64 analog input lines are arranged as 32 differential pairs, with each HI/LO pair representing a single input channel.

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Table 3.5-5. Analog Input Function Selection

AIM[2:0]	FUNCTION OR MODE
0	Differential analog input mode (Default mode).
1	Single-Ended analog input mode.
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

3.5.3.2 Single-Ended Inputs

With the single-ended input mode selected, each of the 64 analog input lines is measured in reference to a common *Input Return*, and represents an individual input channel.

3.5.3.3 Selftest Modes

In the selftest modes, the analog input lines from the system I/O connector are ignored and have no effect on selftest results. Specified board accuracy applies to all selftest measurements, and for critical measurements, the average value of multiple readings should be used.

The ZERO selftest measures a dead-zero reference signal and should produce a nominal midscale reading of 0000 8000h. For the +VREF test, a precision reference voltage equal to 94.780% of fullscale is applied as an analog input, and should produce a nominal reading of 0000 F951h.

3.5.4 Input Scan Timing

For each analog input scan clock, all selected analog inputs are scanned once at the maximum conversion rate, with one conversion performed per channel. The number of channels included in each scan is controlled from two to 64 channels by the Scan Size control bit field (D00-D01) in the Scan and Sync control register, or any single channel can be selected. Each scan commences with Channel 00 and proceeds upward through successive input channels until the selected number of channels has been digitized.

3.5.4.1 Conversion Rate

For single-channel sampling (3.5.5), the ADC conversion rate equals the frequency of the rate generator (3.4.4), which can be adjusted up to 500,000 Hz. For multiple-channel scans, the selected channels are scanned and digitized at a fixed rate that is slightly higher than 350,000 conversions per second. The analog input scan clocking rate has no effect on the conversion rate during multiple-channel scanning.

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3.5.4.2 Maximum Scan Rate

For single-channel sampling, the analog input clock frequency **Finput** must not exceed:

Finput-max (Hz) = 500,000.

For multiple-channel scanning, the maximum value for **Finput** is:

Finput-max (Hz) = 350,000 / Nchan,

where **Nchan** is the number of channels in a scan. For example, a 4-channel scan should not be clocked at a frequency higher than 350,000/4 = 87,500Hz.

3.5.4.3 Scan Clocking Source

The Scan and Sync control register (Section 3.4.2) provides multiple sources for analog input scan clocks. The clock can be provided by (a) either or both of the two rate generators on the board, (b) the External Sync hardware input line, or (c) the Input Sync control bit in the BCR.

If the BCR Input Sync bit is selected as the analog input clock source, an input scan occurs each time the control bit is set HIGH. The Input Sync bit remains HIGH until the scan is completed, after which the bit is cleared automatically.

If the External Sync input line is the analog input clock source, each HIGH-to-LOW transition of the input line initiates an input scan.

3.5.5 Scanning Modes

The analog inputs can be scanned in groups of 2, 4, 8, 16, 32 or 64 channels (32 maximum for differential inputs), or any single channel can be selected for digitizing. The number of channels in a scan is selected by the SCAN SIZE[] field in the scan and sync control register. An input scan commences with Channel-00, and proceeds upward through successive channels until the selected number of channels has been digitized and stored in the input data buffer.

For Single-Channel sampling (SCAN SIZE[] = 0), the channel to be digitized is selected by the SINGLE-CHANNEL SELECT control field.

3.6 Autocalibration

To obtain maximum accuracy from the PMC-16AI64 board, autocalibration should be performed after power warmup and after each initialization. Autocalibration uses current settings for the analog input voltage range, and ignores all other control parameters such as input configuration, clocking rates, etc. No control settings are altered during autocalibration, and external analog input signals are ignored.

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Autocalibration is invoked by setting the Autocal control bit HIGH in the BCR. The control bit returns LOW (normal operation) automatically at the end of autocalibration. Autocalibration can be invoked at any time, and has a duration of approximately 2-4 seconds. Completion of the operation can be detected either by selecting the 'Autocalibration Operation Completed' interrupt condition (paragraph 3.7) and waiting for the interrupt request, or by simply waiting a sufficient amount of time to ensure that autocalibration has been completed.

To compensate for component aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the necessary correction values in calibration DAC's. If a board is defective, the autocalibration process may be unable to successfully calibrate the inputs. If this situation occurs, the AUTOCAL PASS status bit in the BCR will be cleared LOW at the end of the autocalibration interval, and will remain LOW until a subsequent initialization or autocalibration occurs. AUTOCAL PASS is initialized HIGH, and remains HIGH unless an autocalibration failure occurs.

3.7 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. The internal controller must generate a Local Interrupt Request (Section 3.7.1)
b. The *PCI interrupt* must be enabled (Section3.7.2).

If the internal controller generates a local interrupt request, a PCI bus interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.7.2.

3.7.1 Local Interrupt Request

The Interrupt Control Register shown in Table 3.7-1 controls the single local interrupt request line. Two simultaneous source conditions (IRQ 0 and1) are available for the request, with multiple conditions available for each source. IRQ 0 and 1 are logically OR'd together to produce the single interrupt available to the board.

When one or more selected conditions occur for either of the IRQ's, a local interrupt request is generated and the associated IRQ REQUEST flag bit is set HIGH. The request remains asserted until the PCI bus clears the request flag. A local interrupt request is generated automatically at the end of initialization, through IRQ0.

Interrupt conditions are *edge-sensitive*, and an interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

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Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT CONDITION
D00-02	R/W	IRQ0 A0,1,2	0	0	Idle. Interrupt disabled unless initializing. Default state after reset.
				1	Autocalibration operation completed
				2	Input scan initiated (Sync)
				3	Input scan completed
				4-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

3.7.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX^{TM} PCI-9080 reference manual..

3.8 DMA Operation

DMA transfers from the analog input buffer are supported with the board operating as bus master. Table 3.8-1 illustrates a typical PCI register configuration that would control a non-chaining, non-incrementing DMA transfer, and in which a PCI interrupt is generated when the transfer has been completed. Bit 02 in the PCI Command register (04h) must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 data manual for a detailed description of these registers.

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Table 3.8-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial Analog Input Buffer local address (Analog input buffer)	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

For most applications, the DMA Command Status Register (A8h) should be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

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SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PMC-16AI64 board contains a 64-channel analog multiplexer and a high-speed 16-bit A/D converter for digitizing up to 64 single-ended or 32 differential analog input channels. A PCI interface adapter provides the interface between the controlling PCI bus and an internal local controller (Figure 4.1-1). Gain and offset corrections of the analog input channels are performed by calibration DAC's that are loaded with channel correction values during autocalibration

The analog inputs are software-configurable either as 64 single-ended channels, or as 32 differential signal pairs. Buffer amplifiers on all input lines suppress multiplexer input switching noise, and minimize crosstalk and input bias currents. A selftest switching network routes a precision reference to the A/D converter during autocalibration. Analog input data accumulates in a 64K-sample buffer until retrieved by the PCI bus.

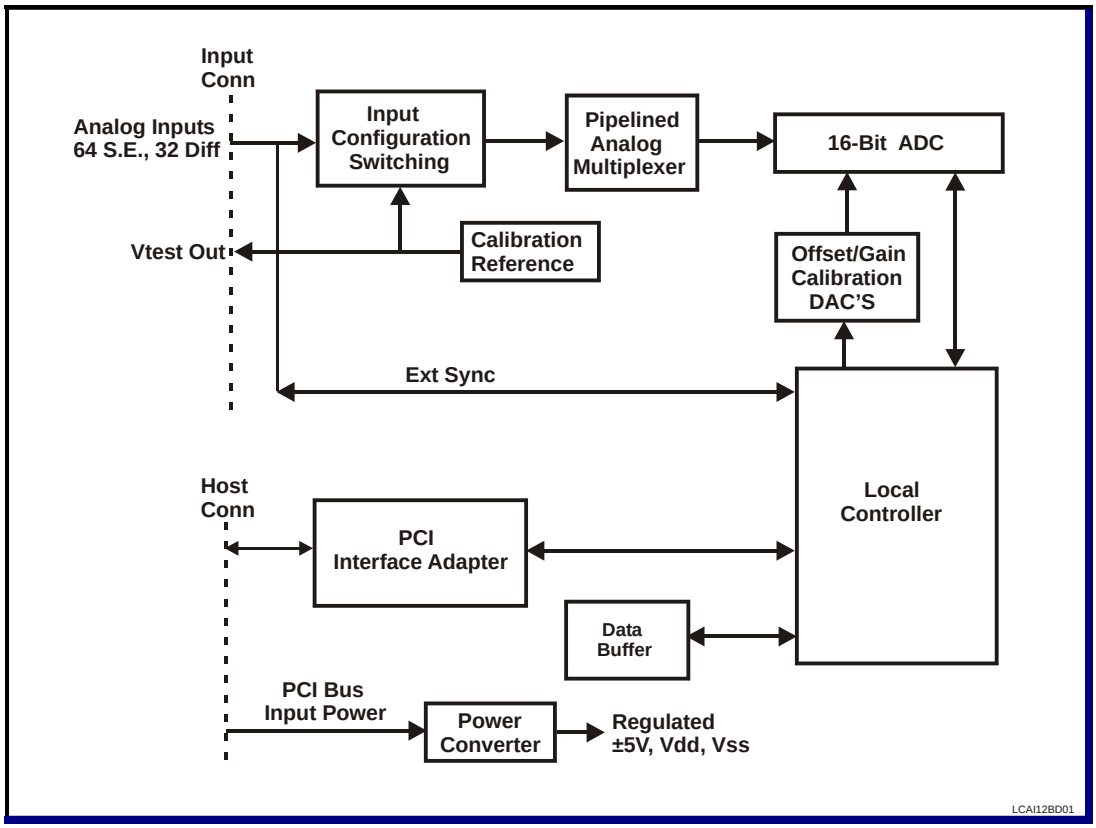


Figure 4.1-1. Functional Block Diagram

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Analog input scanning on multiple PMC-16AI64 target boards can be synchronized to the analog scanning sequence on a single software-designated initiator board.

An interrupt request can be generated in response to selected conditions, including the status of the analog input data buffer. The analog input voltage range for all channels is software-selectable as ±2.5V, ±5V or ±10V.

4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the selftest switches and analog multiplexer shown in Figure 4.1-1. During normal operation, analog input channels from the input/output connector are scanned and digitized. For selftest and autocalibration operations, the internal voltage reference can be routed through the selftest switches to the ADC. The analog multiplexer establishes the input configuration as either single-ended or differential, in response to software control.

The selected input signals pass through input buffer amplifiers, and subsequently are selected by an analog multiplexer for digitizing by the 16-bit ADC. The buffer amplifiers provide the fast response necessary to drive the analog multiplexer. They also minimize interchannel crosstalk and prevent charge coupling from the multiplexer back to the signal source. By routing all inputs through the same signal path, the errors introduced by all components in that path are accounted for during autocalibration.

The output of the multiplexer is buffered by a differential amplifier, and finally is converted by the ADC into a 16-bit digital code. Data is extracted from the ADC in parallel format, and passes through a transfer register into the main analog input data buffer. Offset and gain trimming of the ADC is provided by a pair of 10-bit DAC's that are loaded with trim values determined during autocalibration.

Analog channels from the input/output connector are scanned in a pipeline sequence, in which the subsequent channel in the scanning sequence is selected and allowed to settle, while the current sample is being digitized. This approach increases the effective scan rate without requiring shorter settling or conversion times. Digitizing always occurs at the maximum conversion rate, and a single scan of all selected input channels commences at the beginning of each scan interval. The input scan rate can be controlled from: (a) either of two internal rate generators, (b) software, through a control register, or (c) an external hardware sync source.

4.3 Rate Generators

The local controller contains two independent rate generators, each of which divides a master clock frequency by a software-controlled 16-bit integer. Either generator can be assigned as a clocking source for the analog inputs, and the generators can be cascaded to produce very long clocking intervals.

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4.4 Data Buffer

The analog input data buffer and the PCIbus share a common memory element that is arbitrated to produce effectively independent read/write buffer functions. To avoid the data loss that might otherwise occur during arbitration cycles, data to the input buffer passes through a transfer register that ensures an uninterrupted flow of data in the critical input data paths.

4.5 Autocalibration

Autocalibration is an embedded firmware utility that calibrates all analog input channels to a single internal voltage reference. The utility can be invoked at any time by the control software, and has an approximate duration of 2-4 seconds.

An internal voltage reference is used to calibrate the span of each channel, and a dead-zero ground reference is used to calibrate the offset value. Each of the two 10-bit calibration DAC's is adjusted in a successive approximation sequence that commences with the DAC in an all-zero state. The most significant bit initially is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response from the channel, the bit either is cleared or is left in the "1" state. The next lower significant bit is then tested in the same manner, and this process continues until all 10 bits have been tested and adjusted. The final value in the calibration DAC remains in the DAC until the autocalibration sequence is repeated, or until power is removed.

4.6 Power Control

Regulated supply voltages of ±5 Volts and ±14 Volts are required by the analog networks, and are derived from the +5-Volt input provided by the PCI bus. A DC/DC converter produces preregulated voltages that are subsequently series-regulated to the required output levels. Series regulation ensures minimum noise and optimum performance of the power supply outputs.

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APPENDIX A

LOCAL REGISTER QUICK REFERENCE

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APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3.1-1. Control and Data Registers

OFFSET (Hex)	REGISTER	ACCESS MODE*	ACTIVE BITS	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	16	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	12	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	16	---	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	18	000X FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	17	0001 0960h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	17	0000 0050h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	16	0000 0000h	Number of values in the input buffer
001C	(Reserved)	---	---	---	Inactive
0020	SCAN AND SYNC CONTROL	R/W	19	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	(Reserved)	---	---	---	Inactive
0028	(Reserved)	---	---	---	Inactive
002C	(Reserved)	---	---	---	Inactive
0030-3F	(Reserved)	---	---	---	Inactive

Table 3.2-1. Board Control Register (BCR)

Offset: 0000h **Default: 0000 4060h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00	R/W	AIM0	0	Analog input mode. Selects input configuration or selftest mode. Defaults to differential input mode. .
D01	R/W	AIM1	0	
D02	R/W	AIM2	0	
D03	R/W	(Reserved)	0	---
D04	R/W	RANGE0	0	Analog input range. Defaults to ±10V range.
D05	R/W	RANGE1	1	
D06	R/W	OFFSET BINARY	1	Selects offset-binary analog I/O data format when asserted HIGH, or two's complement when LOW.
D07	R/W	ENABLE EXTERNAL SYNC	0	Configures the board for external sync I/O when HIGH. (SYNC I/O pins are reassigned as a TTLI/O pair).
D08-11	R/W	(Reserved)	0	---
D12	R/W	*INPUT SYNC	0	Triggers a single sample of active channels when BCR Input Sync is selected in the Scan and Sync Control Register. Clears automatically upon scan completion,
D13	R/W	*AUTOCAL	0	Initiates an autocalibration operation when asserted. Clears automatically upon autocal completion,
D14	RO	AUTOCAL PASS	1	Set HIGH at reset or autocal initialization. A HIGH state after autocal confirms a successful calibration.
D15	R/W	*INITIALIZE	0	Initializes the board when set HIGH. Sets defaults for all registers.
D16-D31	RO	(Reserved)	0	Inactive

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Table 3.4-1. Analog Voltage Range Selection (BCR field)

RANGE[1:0]	ANALOG INPUT RANGE
0	±2.5 Volts
1	±5 Volts
2	±10 Volts
3	±10 Volts

Table 3.4-2. Scan and Sync Control Register

Offset: 0020h **Default: 0000 0005h**

DATA BIT	MODE	DESIGNATION	DEF	DESCRIPTION
D00-D02	R/W	SCAN SIZE	5	Number of input channels per scan: 0 => Single-Channel mode * 1 => 2 channels per scan 2 => 4 channels per scan 3 => 8 channels per scan 4 => 16 channels per scan 5 => 32 channels per scan (Default value) 6 => 64 channels per scan (S.E. mode only) 7 =>(Reserved) * Channel selected by Single-Channel Select field below.
D03-D04	R/W	ANALOG INPUTS SCAN CLOCK	0	Selects the analog input scan clocking source: 0 => Internal Rate-A generator output 1 => Internal Rate-B generator output 2 => External Sync input line 3 => BCR Input Sync control bit.
D05-D09	R/W	(Reserved)	0	---
D10	R/W	RATE-B CLOCK SOURCE	0	Selects the clock input source for the Rate-B generator: 0 => Master clock 1 => Rate-A generator output.
D11	R/W	(Reserved)	0	---
D12-17	R/W	SINGLE-CHANNEL SELECT	0	Selects the input channel number when operating in the Single-Channel scanning mode.
D18	R/W	(Reserved)	0	---
D19-D31	RO	(Reserved)	0	Inactive

R/W = Read/Write, RO = Read-Only.

Table 3.4-3. Scan-Trigger Rate Generator Register

Offset: 0010h (Rate-A), 0014h (Rate-B) **Default: 0001 0960 (Rate-A), 0000 0050h (Rate-B)**

DATA BIT	MODE*	DESIGNATION	DEFAULT	DESCRIPTION
D00-D15	R/W	NRATE	---	Rate generator frequency control
D16	R/W	GENERATOR DISABLE	1	Disables the rate generator when HIGH
D17-D31	RO	(Inactive)	0	---

R/W = Read/Write, RO = Read-Only.

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Table 3.4-4. Scan-Trigger Rate Generator Frequency Selection

Nrate (Dec)	(RATE[15..0]) (Hex)	FREQUENCY Fgen * (Hz)
48	0030	500,000
49	0031	489,796
---	---	Fgen (Hz) = 24,000,000 / Nrate
65534	FFFE	366.222
65535	FFFF	366.217

Table 3.4-5. Scan-Trigger Rate Examples

Channels Per Scan (Nchan)	Maximum Scan Rate (Fgen-max, Hz)	Required Scan Rate (Fgen, Hz)	Rate Generator Register (Nrate, Dec)
64	7,812	7,812	3,072
64	7,812	1,000	24,000
64	7,812	500	48,000
16	31,250	12,000	2,000
8	62,500	20,000	1,200
2	250,000	20,000	1,200
1 *	500,000	500,000	48
1 *	500,000	20,000	1,200

* Single-scan mode.

Table 3.5-1. Input Data Buffer

Offset: 0008h **Default: N/A**

DATA BIT	MODE*	DESIGNATION	DESCRIPTION
D00	RO	DATA00	Least significant data bit
D01-D14	RO	DATA01 - DATA14	Intermediate data bits
D15	RO	DATA15	Most significant data bit
D16-D31	RO	(Inactive)	---

* RO indicates read-only access. Write-data is ignored.

Table 3.5-2. Input Data Coding; 16-Bit Data

ANALOG LEVEL	DIGITAL VALUE (Hex)	
	OFFSET BINARY	TWO'S COMPLEMENT
Positive Full Scale minus 1 LSB	0000 FFFF	0000 7FFF
Zero plus 1 LSB	0000 8001	0000 0001
Zero	0000 8000	0000 0000
Zero minus 1 LSB	0000 7FFF	0000 FFFF
Negative Full Scale plus 1 LSB	0000 0001	0000 8001
Negative Full Scale	0000 0000	0000 8000

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Table 3.5-3. Input Data Buffer Control Register

Offset: 000Ch **Default: 0000 FFFEh**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-15	R/W	THRESHOLD VALUE	FFFEh	Input buffer threshold value.
D16	R/W	CLEAR BUFFER *	0	Clears (empties) the input buffer when asserted HIGH. Aborts current input scan.
D17	RO	THRESHOLD FLAG	0	Asserted HIGH when the number of values in the input buffer exceeds the THRESHOLD VALUE.
D18-D31	RO	(Inactive)	0	---

*Clears automatically when operation is completed

Table 3.5-4. Buffer Size Register

Offset: 0018h **Default: 0000 0000h**

DATA BIT	MODE*	DESIGNATION	DEF	DESCRIPTION
D00-15	RO	BUFFER SIZE	0000h	Number of values in the input buffer
D16-D31	RO	(Inactive)	0	---

Table 3.5-5. Analog Input Function Selection (BCR field)

AIM[2:0]	FUNCTION OR MODE
0	Differential analog input mode (Default mode).
1	Single-Ended analog input mode.
2	ZERO test. Internal ground reference is connected to all analog input channels.
3	+VREF test. Internal voltage reference is connected to all analog input channels.
4-7	(Reserved)

Table 3.7-1. Interrupt Control Register

Offset: 0000 0004h **Default: 0000 0008h**

DATA BIT	MODE	DESIGNATION	DEF	VALUE	INTERRUPT CONDITION
D00-02	R/W	IRQ0 A0,1,2	0	0	Idle. Interrupt disabled unless initializing. Default state after reset.
				1	Autocalibration operation completed
				2	Input scan initiated (Sync)
				3	Input scan completed
				4-7	(Reserved)
D03	R/W	IRQ0 REQUEST	1*	---	Group 0 interrupt request flag. Set HIGH when the selected interrupt condition occurs. Clears the request when cleared LOW by the bus.
D04-06	R/W	IRQ1 A0,1	0	0	Idle; no interrupt condition selected.
				1	Input buffer threshold LOW-HIGH transition
				2	Input buffer threshold HIGH-LOW transition
				3-7	(Reserved)
D07	R/W	IRQ1 REQUEST	0	---	Group 1 interrupt request flag. See D03.
D08-31	RO	(Inactive)	0	---	

R/W = Read/Write, RO = Read-Only. * HIGH after reset.

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Table 3.8-1. Typical DMA Register Configuration

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Initial Analog Input Buffer local address (Analog input buffer)	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

PMC-16AI64 REGISTER LIST
MAINTENANCE INFORMATION

OFFSET (Hex)	REGISTER	ACCESS MODE*	ACTIVE BITS	DEFAULT	PRIMARY FUNCTION
0000	BOARD CONTROL (BCR)	RW	16	0000 4060h	Board Control Register (BCR)
0004	INTERRUPT CONTROL	RW	12	0000 0008h	Interrupt conditions and flags
0008	INPUT DATA BUFFER	RO	16	---	Analog input data buffer
000C	INPUT BUFFER CONTROL	R/W	18	000X FFFEh	Input buffer threshold and control
0010	RATE-A GENERATOR	RW	17	0001 04B0h	Rate-A generator freq selection
0014	RATE-B GENERATOR	RW	17	0000 0050h	Rate-B generator freq selection
0018	BUFFER SIZE	RO	16	0000 0000h	Number of values in the input buffer
001C	(Reserved)	---	---	---	Inactive
0020	SCAN AND SYNC CONTROL	R/W	19	0000 0005h	Channels per scan; Clocking and Sync sources.
0024	(Reserved)	---	---	---	Inactive
0028	FIRMWARE REVISION **	RO	16	0000 xxxxh	Firmware revision
002C	AUTOCAL VALUES **	R/W	12	0000 080xh	Autocal value readback.
0030-3F	(Reserved)	---	---	---	Inactive

R/W = Read/Write, RO = Read-Only. ** Nonsupported register; development function only.

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