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General Standards Corporation

High Performance Bus Interface Solutions

Revision 090406

PMC-16AIO-88

16-CHANNEL, 16-BIT
ANALOG INPUT/OUTPUT BOARD

REFERENCE MANUAL

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SECTION 1.0

INTRODUCTION

1.1 General Description

The PMC-16AIO-88 board is a single-width PCI mezzanine card (PMC) that provides eight 16-bit analog input channels and eight 16-bit analog output channels for the PCI bus. The board is functionally compatible with the IEEE PCI local bus specification Revision 2.3, is mechanically compatible with the IEEE compact mezzanine card (CMC) specification, and supports the "plug-n-play" initialization concept. Power requirements consist of +5 VDC in accordance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling. Specific details of physical characteristics and power requirements are contained in the PMC-16AIO-88 specification. Figure 1-1 shows the physical configuration of the board, and the arrangement of major components.

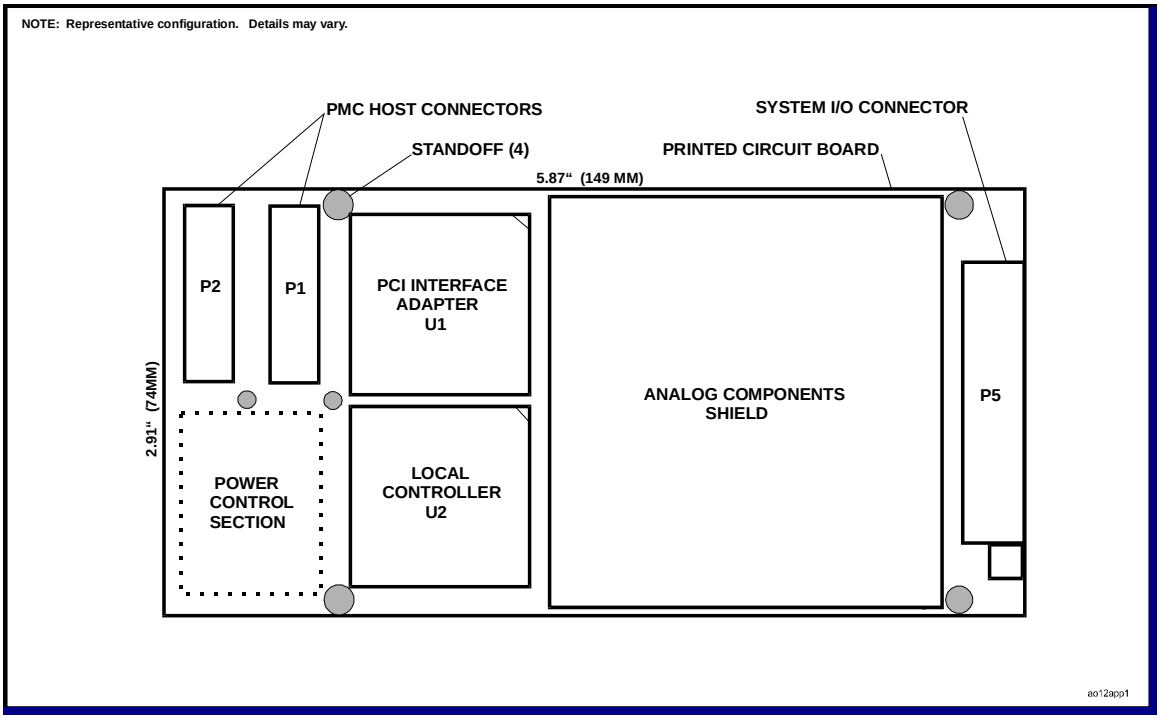


Figure 1-1. Physical Configuration

The board is designed for minimum off-line maintenance, and includes internal monitoring and loopback features that eliminate the need for disconnecting or removing the module from the system for calibration. All analog input and output system connections are made through a single 50-pin subminiature-D front-access I/O connector.

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1.2 Functional Overview

The 16-channel PMC-16AIO-88 analog I/O board provides high resolution 16-bit analog input and output resources in a high-density single-width PMC module. Principal capabilities of the board are summarized in the following list of features.

- ❑ 8 Analog Input Channels, 8 Analog Output Channels
- ❑ 16-Bit Scanning ADC for 8 Single-Ended or 4 Differential Analog Input Channels
- ❑ 16-Bit D/A Converter per Analog Output Channel
- ❑ Independent Input and Output FIFO Buffers; 32K-Sample Input Capacity
- ❑ Autocalibration of all Analog Channels; Internally Controlled
- ❑ Input and Output Ranges of ±10V, ±5V or ±2.5V
- ❑ Continuous and Triggered-Burst Input Modes.
- ❑ Loopback Feature for Built-in-Test Support and Autocalibration
- ❑ Programmable Rate Generator Supports Both Inputs and Outputs
- ❑ Single-width PMC Form Factor.

Figure 1-2 outlines the internal functional organization of the board. Communication with the host PCI bus is provided by a PCI interface adapter which furnishes a 16-bit local bus for exchanging information between the adapter, the local controller, and the control and data registers.

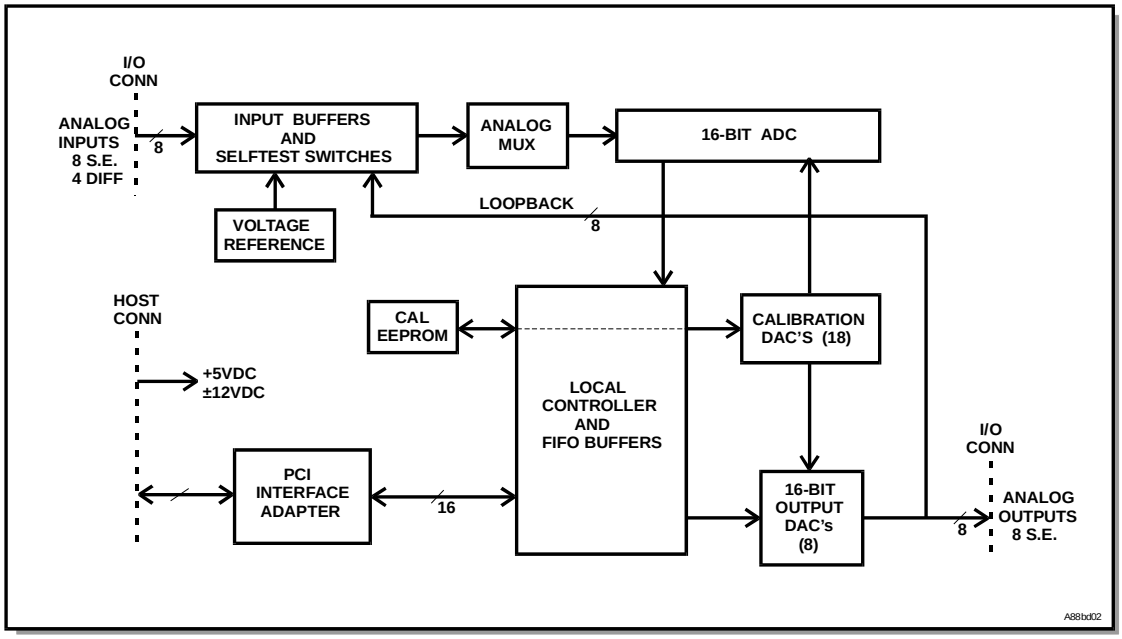


Figure 1-2. Functional Organization

Analog input channels are configurable as either differential or single-ended inputs. Input scanning can be performed continuously, or can be burst-triggered by either a software trigger or a hardware trigger. A FIFO buffer accumulates input data samples for subsequent transfer to the PCI bus. The four analog output channels are controlled through an analog output FIFO buffer, and can be updated either synchronously or asynchronously. Inputs and outputs have a factory-configured range of ±10V, ±5V or ±2.5V.

A programmable rate generator provides an adjustable internal time base for the analog inputs and outputs. The generator can be configured to control either the input scan rate, the output strobe

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rate, or both inputs and outputs simultaneously for input/output synchronization. When applied to the analog outputs, the rate generator supports the generation of arbitrary waveforms or functions.

All input and output channels are calibrated with a single internal voltage reference. This feature produces the optimum calibration situation, in which the accuracy of the board is adjusted in the actual operating environment. Software-controlled test configurations include a loopback mode for monitoring all analog output channels.

Offset and gain trimming of the 16-bit A/D converter (ADC) and output D/A converters (DAC's) is performed by 12-bit calibration DAC's. System analog inputs pass through a selftest network that replaces the system signals either with a precision voltage standard or with the four analog output channels, under software control. Offset and gain correction values are determined during autocalibration, and are stored in nonvolatile EEprom for subsequent transfer to the calibration DAC's during board initialization. Autocalibration can be invoked at any time from the PCI bus.

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SECTION 2.0

INSTALLATION AND MAINTENANCE

2.1 Board Configuration

This product has no field-alterable configuration features, and is completely configured at the factory for field use.

2.2 Installation

2.2.1 Physical Installation

To minimize the opportunity for accidental damage before installation, the board should be stored in the original protective shipping envelope. System power must be turned OFF before proceeding with the installation.

CAUTION: This product is susceptible to damage from electrostatic discharge (ESD). Before removing the board from the conductive shipping envelope, ensure that the work surface, the installer and the host board have been properly discharged to ground.

After removing the board from the shipping envelope, position the board with the shield and standoffs facing the host (carrier) board, and with the 50-Pin I/O connector oriented toward the front panel. Align the two PCI connectors located at the end of the board opposite the I/O connector with the mating connectors on the host board, and carefully press the board into position on the host. Verify that the PCI connectors have mated completely and that the four standoffs are seated against the host board.

Attach the board to the host with four 2.5 x 6.5mm panhead screws. Pass the screws through the back of the host into the four standoffs mounted on the board. Tighten the screws carefully to complete the installation; do not overtighten.

2.2.2 Input/Output Cable Connections

I/O connector P5 is designed to mate with a standard male 50-pin 0.05" subminiature D connector, equivalent to AMP #1-750913-5. The insulation displacement (IDC) AMP cable connector accepts two 25-conductor ribbon cables in the configuration shown in Figure 2-1. Alternative discrete-wire 'round' cables may be used, but must have individually shielded conductors, with the signal conductors connected to even-numbered pins, and with the shields connected to odd-numbered pins.

Signal pin assignments are listed in Table 2-1. Unused input pins may be left disconnected in most applications. However, if very long cables are used or if excessive cable noise is anticipated, the unused analog inputs should be grounded to the input return to minimize the injection of noise into the board. Fine-pitch standard SCSI cables, if used, would intersperse the digital I/O lines with the analog I/O lines, and are not recommended for analog I/O applications.

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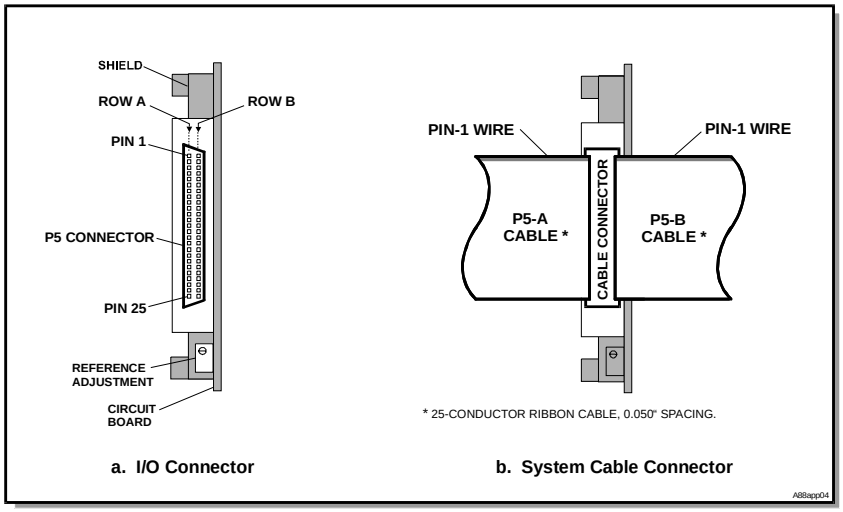


Figure 2-1. Input/Output Connector and Cables

Table 2-1. System Connector Pin Assignments

P5-A	
PIN	SIGNAL
1	OUTPUT RETURN
2	OUTPUT CHAN 00
3	OUTPUT RETURN
4	OUTPUT CHAN 01
5	OUTPUT RETURN
6	OUTPUT CHAN 02
7	OUTPUT RETURN
8	OUTPUT CHAN 03
9	OUTPUT RETURN
10	OUTPUT CHAN 04
11	OUTPUT RETURN
12	OUTPUT CHAN 05
13	OUTPUT RETURN
14	OUTPUT CHAN 06
15	OUTPUT RETURN
16	OUTPUT CHAN 07
17	OUTPUT RETURN
18	(Reserved)
19	DIGITAL RETURN
20	OUTPUT STROBE
21	DIGITAL RETURN
22	OUTPUT STRB RDY
23	ADC RETURN
24	RANGE REFERENCE
25	ADC RETURN

P5-B: SINGLE-ENDED INPUTS	
PIN	SIGNAL
1	DIGITAL RETURN
2	INPUT TRIGGER
3	DIGITAL RETURN
4	INPUT TRIG RDY
5	DIGITAL RETURN
6	DIGITAL RETURN
7	DIGITAL RETURN
8	(Reserved)
9	INPUT RETURN
10	INPUT CHAN 00
11	INPUT RETURN
12	INPUT CHAN 01
13	INPUT RETURN
14	INPUT CHAN 02
15	INPUT RETURN
16	INPUT CHAN 03
17	INPUT RETURN
18	INPUT CHAN 04
19	INPUT RETURN
20	INPUT CHAN 05
21	INPUT RETURN
22	INPUT CHAN 06
23	INPUT RETURN
24	INPUT CHAN 07
25	INPUT RETURN

P5-B: DIFFERENTIAL INPUTS	
PIN	SIGNAL
1	DIGITAL RETURN
2	INPUT TRIGGER
3	DIGITAL RETURN
4	INPUT TRIG RDY
5	DIGITAL RETURN
6	DIGITAL RETURN
7	DIGITAL RETURN
8	(Reserved)
9	INPUT RETURN
10	INPUT CHAN 00 HI
11	INPUT RETURN
12	INPUT CHAN 01 HI
13	INPUT RETURN
14	INPUT CHAN 02 HI
15	INPUT RETURN
16	INPUT CHAN 03 HI
17	INPUT RETURN
18	INPUT CHAN 00 LO
19	INPUT RETURN
20	INPUT CHAN 01 LO
21	INPUT RETURN
22	INPUT CHAN 02 LO
23	INPUT RETURN
24	INPUT CHAN 03 LO
25	INPUT RETURN

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2.3 System Configuration

2.3.1 Analog Inputs

2.3.1.1 Input Configuration

Analog inputs can be configured as either eight single-ended channels or four differential channels, as illustrated in Figure 2-2. The board also permits the inputs to be connected in an eight-channel pseudo-differential arrangement, which is a variation of the single-ended configuration. The hardware input configuration must be acknowledged by the control software, which configures the controller for either single-ended or differential operation. Pull-down resistors are provided on all analog inputs.

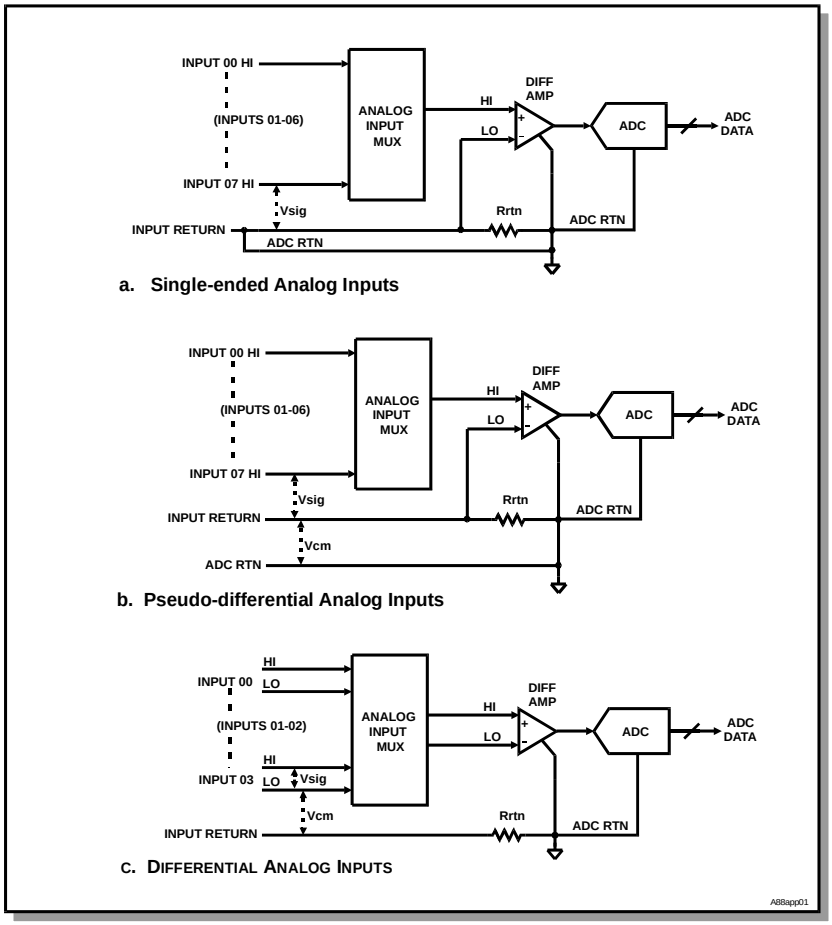


Figure 2-2. Analog Input Configurations

Single-ended and pseudo-differential operating modes offer the maximum number of input channels, but generally provide optimum performance only when the input signal sources either are isolated from each other, or are common only to a single isolated signal return. Table 2-1 provides separate pin assignment columns for single-ended and differential input configurations.

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For applications in which the signal sources are isolated from each other (mutual isolation), single-ended operation usually is recommended. In this case, as shown in Figure 2-2a, the input return is connected to the internal ADC return which provides a return path for all inputs. Isolation from system grounds is a critical issue in single-ended operation. If the signal sources are returned externally to system ground when operating in this mode, a potential difference between the system ground and the ADC return can generate excessive return current and cause erroneous measurements or possibly damage the board.

If the signal sources are connected to a common return, but the return is otherwise isolated from system ground, then pseudo-differential operation probably will produce the best results. Pseudo-differential operation provides a 'soft' return to system ground through an internal resistance, shown as Rrtn in Figure 2-2b. The ADC return is left disconnected in this mode. Rrtn is approximately 100 Ohms, and prevents excessive current from flowing into the ADC return while still providing an input return path. The input return serves as a common differential return for all eight input channels. To prevent excessive dissipation in Rrtn, the potential between the input return and the ADC return must not exceed 3 Volts. INPUT RETURN serves as a remote-sense input in this configuration, and consequently is susceptible to both radiated and conducted system noise. If excessive noise is experienced, a large capacitance (10-100uF) between the INPUT RETURN and VREF RETURN lines may be necessary to alleviate the problem.

Differential operation is necessary when the input sources are not isolated from each other, and when the source returns may be at different potentials. This operating mode also offers the highest rejection of the common mode noise that is characteristic of long unshielded cables. When operating in the differential mode, shown in Figure 2-2c and Table 2-1, the wire pair from each signal source is connected between the HI(+) and LO(-) inputs of a single input channel. The input return is connected to system ground as close as possible to the input sources, and the ADC return usually is left disconnected.

2.3.1.2 Input Trigger

Two signal lines in the I/O connector, INPUT TRIGGER and INPUT TRIG RDY, support external triggering of input burst scans. If the board is software-configured for burst scanning, a HIGH-to-LOW transition of INPUT TRIGGER while INPUT TRIG RDY is HIGH will initiate a single scan of the analog inputs. No other combination of these control signals will trigger a scan. The control levels are TTL compatible, with "HIGH" indicating a level above the TTL high-threshold.

2.3.2 Analog Outputs

2.3.2.1 Output Configuration

The eight analog output channels are single-ended and have a common signal return, referred to in Table 2-1 as "Output Return." In general, single-ended outputs should drive only loads which are isolated from system ground. The best results are obtained when the loads also are isolated from each other. Analog outputs are active during autocalibration.

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The voltage drop in ribbon cable can be a significant source of error in 16-bit systems, even with relatively short cables driving low-current loads. Figure 2-3 shows the effect of load current on the voltage drop in copper wire of various sizes. A 2.0 milliamp load for example, will insert a voltage drop of approximately 130 microvolts *per foot* in conventional #28 AWG ribbon cable; twice that if the return line is also considered. Several feet of ribbon cable therefore can produce significant errors in a 16-bit system, in which 1 LSB may represent only 76 microvolts (±2.5 Volt range). High impedance loads generally will not produce significant DC line loss errors.

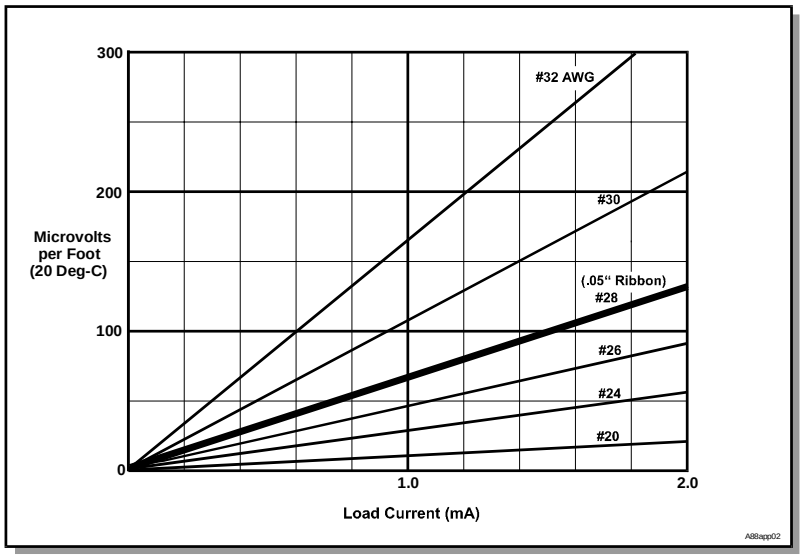


Figure 2-3. Line Loss Versus Load Current

Figure 2-4 shows the primary sources of error in both isolated and nonisolated system configurations. For loads that are isolated from each other (Figure 2-4a), the total line-loss error is twice the loss produced in a single line, assuming equal wire size and length for output and return lines. For loads which have a common return that is isolated from system ground, line loss in the common return appears as crosstalk between channels.

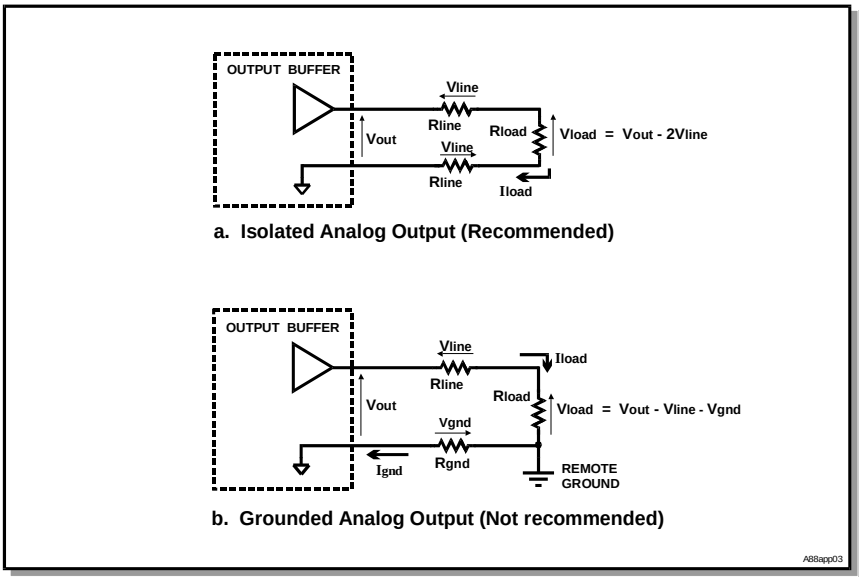


Figure 2-4. Output Configurations

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If the load return is inadvertently connected to a remote system ground (Figure 2-4b), the potential difference Vgnd between the system ground and the internal signal return will introduce an error into the signal delivered to the load. The ground current Ignd developed in the return line is limited essentially only by Rgnd, and may damage the cable or the board if not controlled.

2.3.2.2 Output Strobe

If the board is software-configured for output strobing, all outputs will update simultaneously to stored values if an external strobe occurs. Two signal lines in the I/O connector, OUTPUT STROBE and OUTPUT STRB RDY, provide the external strobing function. If the board is software-configured for output strobing, a HIGH-to-LOW transition of OUTPUT STROBE while OUTPUT STRB RDY is HIGH will generate an external strobe. No other combination of these control signals will generate a strobe. The control levels are TTL compatible, with "HIGH" indicating a level above the TTL high-threshold.

2.4 Maintenance

This product requires no scheduled hardware maintenance other than periodic reference calibration. The optimum calibration interval will vary, depending upon the specific application, but in most instances an interval of one year is recommended.

In the event of a suspected malfunction, all associated system parameters, such as power voltages, control bus integrity, and input signal levels, should be evaluated before troubleshooting of the board itself is attempted. If surface-mount repair capability is not available, a board that is suspected to be defective should be returned to the factory for problem analysis and repair.

2.5 Calibration

All input and output channels are software-calibrated to an internal voltage reference by an embedded autocalibration software utility. The calibration procedure presented here describes the adjustment of the voltage reference. For applications in which the system must not be powered down, the board can be calibrated under normal operating conditions while installed on the existing host board.

To eliminate the requirement for a special test connector, the two test points required for calibration, RANGE REFERENCE and ADC RETURN, can be made available at a system breakout connector or test panel. This arrangement also eliminates the necessity of disconnecting the system input/output cable for calibration.

2.5.1 Equipment Required

Table 2-2 lists the minimum equipment requirements for calibrating the PMC-16AIO-88 board. Alternative equivalent equipment may be used.

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Table 2-2. Calibration Equipment

EQUIPMENT DESCRIPTION	MANUFACTURER	MODEL
Digital Multimeter, 5-1/2 digit, 0.005% accuracy for DC voltage measurements at ±2.5 Volts to ±10 Volts.	Hewlett Packard	34401A
Host board with single-width PMC adapter	(Existing host)	---
Standard 50-Pin, 0.05", subminiature "D" connector, with test leads. (Not required if calibration test points are made permanently available at a system connection point)	AMP	1-750913-5

2.5.2 Reference Adjustment

The following procedure describes the single adjustment that is necessary to ensure conformance to the product specification. The adjustment seal on the trimmer should be removed before beginning the procedure, and the trimmer should then be resealed with a suitable sealing agent after calibration has been completed. The adjustment is accessible from the front panel, and is located next to the system input/output connector as shown in Figure 5-1.

This procedure assumes that the board to be calibrated is installed on a host board, and that the host is installed in an operating system. The board can be in any operating mode when the adjustment is performed.

1. Connect the digital multimeter between the RANGE REFERENCE (+) and ADC RETURN (-) pins in the system I/O connector. Refer to Table 2-1 for pin assignments.

2. If power has been removed from the board, apply power now and wait at least 15 minutes before proceeding..

3. Adjust the REFERENCE ADJUSTMENT trimmer (Figure 2-1) until the digital multimeter indication is within the appropriate range listed in the following table:

INPUT VOLTAGE RANGE	MULTIMETER INDICATION RANGE (DC Volts)
±10 Volts	+9.9902 ±0.0009
± 5 Volts	+4.9951 ±0.0005
±2.5 Volts	+2.4976 ±0.0003.

4. Calibration is complete. Remove all test connections.

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SECTION 3.0

CONTROL SOFTWARE

3.1 Introduction

The PMC-16AIO-88 board is compatible with the PCI Local Bus specification and supports "plug-n-play" autoconfiguration at the time of power-up. That is, the host can obtain the amount of I/O space required by the board, and return the configuration base address into the PCI Configuration Register at Offset 18h on this board. Configuration-space registers are initialized internally to support the location of the board on any eight-longword boundary in PCI memory space.

After initialization and configuration have been completed, communication between the PCI bus and the board takes place through a 16-bit Board Control Register (BCR) and a bidirectional FIFO buffer register. The buffers consist of a 16-bit read-buffer for acquiring analog input data, and a 16-bit write-buffer for delivering analog output data to the board. Register locations are shown in Table 3-1. Data transfers are single-D32, with the upper 16 bits ignored during write operations, and all-zero during read operations. Any of the predefined operational conditions identified throughout this section can invoke a single interrupt request from the board.

Table 3-1. Control and Data Registers

OFFSET	16-BIT REGISTER	ACCESS*	DEFAULT	DESCRIPTION
00	BOARD CONTROL	R/W	2401h	Control and status monitoring
04	RATE GENERATOR	R/W	0064h	Rate generator clocking rate
08	INPUT / OUTPUT DATA	Read	---	Analog input data, Channel-00 first, followed sequentially by remaining channels in scan. Data format is offset binary.
		Write	---	Analog output channel and data. Written as two-word pairs, 3-bit channel first, followed by 16-bit data. Channel code is right-justified; data format is offset binary.
0C	RATE CONTROL	R/W	0000h	Rate generator utilization
10	INPUT BUFFER POINTER	RO	0000h	Number of samples remaining in the analog input buffer.
14	BUFFER FLAGS	RO	0009h	Input and output buffer status flags.
18	FIRMWARE REVISION **	RO	XXXXh	Installed firmware revision.
1C	OUTPUT BUFFER POINTER	RO	0000h	Number of samples remaining in the analog output buffer.

* R/W = Read/Write, RO = Read-Only. ** Maintenance register; Listed for reference only.

3.2 Board Control Register

The BCR controls all board functions except those associated with the bidirectional digital port. As Table 3-2 indicates, the BCR consists of 16 control bits and status flags. Control and monitoring functions of the BCR are described in detail throughout the remainder of this section. The BCR initializes to the value 8001h.

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Table 3-2. Board Control Register

Offset: 00h **Default: 2401h**

DATA BIT	R/W MODE	DESIGNATION	DESCRIPTION
D00	R/W	AIM0	Analog input mode. Selects single-ended or differential input configuration, and the input operational mode. Defaults to burst-scan, single-ended input mode.
D01	R/W	AIM1	
D02	R/W	AIM2	
D03	R/W	LBC0	Loopback channel. Selects one of eight analog output channels for loopback testing. Active only in the Loopback selftest mode. Defaults to Channel-0.
D04	R/W	LBC1	
D05	R/W	LBC2	
D06	R/W	OUTPUT STROBE ENABLE	Enables internal/external analog output strobe. Disables automatic updating of outputs.
D07	R/W	INTERRUPT A0	Interrupt source selection.
D08	R/W	INTERRUPT A1	
D09	R/W	INTERRUPT A2	
D10	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.
D11	R/W	* CM0	Calibration mode. Selects either normal operation or a calibration mode. Defaults to normal operation.
D12	R/W	* CM1	
D13	R/W	* OUTPUT STROBE	Analog output internal (software) strobe, and strobe-ready flag. When set HIGH internally, a strobe will not be accepted.
D14	R/W	* BURST TRIGGER	Analog input internal (software) burst trigger. Initiates a single scan of all analog input channels. Remains asserted until the scan is completed.
D15	R/W	* INITIALIZE	Initializes the board. Sets all defaults.

All bits asserted HIGH. * Cleared automatically when operation is completed.

3.3 Configuration and Initialization

3.3.1 Board Configuration

During *board configuration*, initial values for both the PCI configuration registers and the internal control logic are extracted from internal nonvolatile read-only memory. This process is initiated by a PCI bus reset, and should be required only once after the initial application of power. While the PCI configuration registers are being loaded, the response to PCI target accesses is RETRYs. Configuration operations are executed in the sequence shown in Table 3-3.

Table 3-3. Configuration Operations

Operation	Maximum Duration
PCI configuration registers are loaded from internal ROM	3 ms
Internal control logic is configured from internal ROM	300 ms
Internal control logic is initialized	3 ms

Board configuration terminates with the PCI interrupts disabled. Attempts to access the local bus during configuration should be avoided until the PCI interrupts are enabled and the initialization-complete interrupt request is asserted, as described in Section 3.7.

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3.3.2 Initialization

Internal control logic can be initialized without invoking configuration by setting the INITIALIZE control bit in the BCR. This action causes the internal logic to be initialized, but does not affect the PCI configuration registers and does not reconfigure the internal control logic. Initialization requires 3 milliseconds or less for completion, and produces the following conditions:

- Calibration D/A converters are initialized with values from internal EEprom
- Analog input buffer is reset to empty
- The local interrupt request is asserted
- The BCR is initialized; all defaults are invoked.

Upon completion of initialization, the INITIALIZE control bit is cleared automatically.

3.4 Analog Inputs

Configuration of the analog input networks is controlled by the BCR control bits designated as AIM[2:0], which are summarized in Table 3-4. The analog input configuration arranges the input channels in either single-ended mode or differential mode during normal scanning operations, and establishes either burst-scan or continuous-scan operation. (The convention of "X:Y" indicating "the range from X down to Y" is used throughout this section).

Table 3-4. Analog Input Mode Selection

AIM[2:0]	FUNCTION OR MODE
0	Single-ended analog input configuration. Continuous scan; channels 0-7.
1	Single-ended analog input configuration. Burst scan; channels 0-7. Default state.
2	Differential analog input configuration. Continuous scan; channels 0-3.
3	Differential analog input configuration. Burst scan; channels 0-3.
4	Loopback Selftest: The analog output channel selected by LBC[2:0] is connected to analog input Channel-0. Single-ended input configuration. Burst scan; channel-0 only.
5	+VREF test: Internal voltage reference is connected to all analog input channels. Single-ended input configuration. Burst scan; channels 0-7.
6	(Reserved)
7	ZERO test: Internal ground reference is connected to all analog input channels. Single-ended input configuration. Burst scan; channels 0-7.

An *input sample* produces a 16-bit digital value which represents the signal level present at the input to the internal A/D Converter. A *scan* consists of a set of input samples that corresponds to all analog inputs arranged in channel sequence. Each scan commences with Channel 0, and proceeds upward sequentially through all channels in the scan. In all analog input modes, digitized input values are written to the analog input buffer in the sequence in which the channels are scanned. The input buffer is supported with buffer-empty and buffer-almost-full interrupts.

Control bits AIM[2:0] also permit the board to be configured in any of several selftest modes for system level verification of operational integrity. In the selftest modes, field inputs are replaced with specific internal signals, as listed in Table 3-4, and the burst scan mode is selected. To

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minimize the effect of random noise, each selftest measurement should be acquired as an averaged value determined from at least sixteen samples.

3.4.1 Normal Input Scanning

Normal input scanning modes are selected with AIM[2:0] = 0, 1, 2 or 3. A scan consists of eight channels in the single-ended mode, or four channels in the differential mode. In the continuous scanning modes, the completion of each scan immediately initiates a subsequent scan, thereby producing a continuous sequence of input scans. A burst scan consists of a single scan, and is initiated either (a) by a software trigger, (b) by an external hardware trigger, or (c) by a clock signal from the programmable rate generator (Paragraph 3.9). The default condition after initialization is the burst scan mode with single-ended inputs, and with the rate generator disabled.

3.4.2 Burst Triggering

In the burst scan modes, a single scan is initiated by setting the software trigger control bit (BURST TRIGGER) in the BCR. The scan commences immediately, and BURST TRIGGER is cleared automatically when the scan has been completed and the board is ready to accept a subsequent trigger. A burst scan can be initiated also by a HIGH-to-LOW transition of the external hardware trigger. Both the software trigger and the hardware trigger are edge-detected, and are ignored if asserted while a scan is in progress.

Completion of a scan can be detected by selecting the Scan Complete interrupt condition, and by then waiting for the associated interrupt request. Alternatively, the external triggers can be spaced at intervals that exceed the scan interval, which is eight times the conversion interval when operating in the single-ended mode, or four times the conversion interval in the differential mode.

3.4.3 Loopback Testing

When the loopback mode is selected (AIM[2:0] = 4), one of the eight analog output channels is connected as a test channel to analog input Channel 0. The analog output test channel is selected by LBC[2:0] in the BCR, as shown in Table 3-5. In this mode, a scan consists of only analog input Channel 0.

Table 3-5. Loopback Test Channel Selection

LBC[2:0]	FUNCTION
0	Analog Output Channel 00; Default state.
1	Analog Output Channel 01
2	Analog Output Channel 02
3	Analog Output Channel 03
4	Analog Output Channel 04
5	Analog Output Channel 05
6	Analog Output Channel 06
7	Analog Output Channel 07

The loopback mode can be used to verify the integrity of the analog input and output channels by writing specific values to each output channel, and by then verifying the accuracy of the responses measured through analog input Channel-0. The errors encountered during loopback testing will include the errors present in both the input and output test channels.

3.4.4 Positive Reference Selftest

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When AIM[2:0] = 5, the internal precision voltage reference that is used during autocalibration is connected to all analog input channels. The voltage reference equals 0.99902 times the positive full scale value for the board (e.g.: +4.9951 Volts for the ±5V range). The nominal response for this input level is FFE0h. In this mode, a scan consists of all eight input channels.

3.4.5 Zero Input Selftest

When AIM[2:0] = 7, all analog input channels are connected to internal signal ground, which corresponds to zero-level. The nominal response for this input level is 8000h. All eight input channels are scanned in this mode.

3.4.6 Input Buffer

The analog input buffer has a capacity of 32,768 (8000h) 16-bit conversion values. Operation is supported with buffer-empty and buffer-almost-full conditions for an interrupt request. Reading an empty input buffer extracts the last value written to the buffer by the A/D converter. A buffer-almost-full interrupt indicates that the input buffer can accept a maximum of seven additional analog input values. A full input buffer accepts no further input data, but all data acquired before the full condition occurred is retained. The Input Buffer Pointer register listed in Table 3-1 contains the current number of locations occupied in the input buffer.

3.5 Analog Outputs

Each analog output channel is controlled by writing the channel number, followed by the channel data, to the analog output buffer. The channel number must be right-justified, and must be padded with zero's to the MSB. For example, to adjust analog output Channel 5 to 0.000 Volts, the value 0005h, followed by 8000h, would be written to the analog output buffer. Analog output channels may be accessed in any sequence. The analog outputs are active during autocalibration.

3.5.1 Analog Output Strobe

The analog output channels can be controlled in any of several strobing modes. If the OUTPUT STROBE ENABLE control bit in the BCR is LOW (default), each output value is transferred directly from the buffer to the associated output channel.

If, however, OUTPUT STROBE ENABLE is asserted HIGH, all values extracted from the output buffer are held in an intermediate buffer until either (a) a "1" is written to the OUTPUT STROBE control bit in the BCR, (b) the external hardware strobe is asserted LOW, or (c) an output strobe is received from the programmable rate generator (Paragraph 3.9). An output strobe transfers all values in the intermediate buffer immediately to their associated output channels. If multiple values are written to a single channel in the intermediate buffer, only the last value received before the strobe occurs is transferred to the output channel.

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The OUTPUT STROBE bit is driven HIGH internally if the board is *not ready* to accept a strobe, indicating that either (a) output strobing is not enabled, (b) no output data is available, or (c) the analog output serializer is busy. A LOW state for OUTPUT STROBE indicates that a strobe will be accepted.

3.5.2 Output Buffer

The analog output buffer has a capacity of 16,384 (4000h) 16-bit output samples, or channel-number/channel-data pairs, and is supported with buffer-full and buffer-almost-empty conditions for an interrupt request. Analog output values written to a full buffer will be discarded. A buffer-almost-empty interrupt request indicates that no more than three output values remain in the output buffer. The Output Buffer Pointer register listed in Table 3-1 contains the current number of locations occupied in the output buffer.

A serialization delay of approximately 4 microseconds is introduced as each output value is extracted from the output buffer. Therefore, writing data to the buffer at rates greater than 250,000 channels per second will cause the buffer to fill; lower data rates will permit the buffer to empty. Data is extracted from the output buffer at the maximum possible rate unless the programmable rate generator is enabled for analog outputs (Paragraph 3.9).

3.6 Calibration Modes

Calibration functions are controlled by control bits CM[1:0] in the BCR, and are summarized in Table 3-6. In the default Normal Operation mode, selected with CM[1:0] = 0, all board functions respond to BCR control bits as described throughout this section. For nonzero values of CM[1:0], BCR controls are preempted as necessary to implement the selected calibration operation.

The analog input and output buffers are reset to empty at the beginning of each calibration operation initiated by CM[1:0]. When the selected operation has been completed, CM[1:0] bits are automatically cleared to the default "0" state, and the single-ended burst scan input mode is selected. To clear calibration data from the analog input buffer, the board should be initialized before resuming normal operation.

Table 3-6. Calibration Mode Selection

CM[1:0]	FUNCTION
0	Normal operation. No calibration activity. Default state.
1	Load calibration DAC's from EEprom. Performed automatically during initialization.
2	Invoke Autocalibration
3	Copy calibration values from EEprom to the analog input buffer.

3.6.1 Loading Calibration DAC's

Setting CM[1:0] = 1 causes the calibration values stored in internal EEprom to be transferred to the calibration DAC's. The duration of the transfer is approximately 2 milliseconds. This operation occurs automatically during initialization.

3.6.2 Autocalibration

Calibration correction values for analog input and output channels are stored in nonvolatile EEprom, which retains the values when power is removed. The calibration values are transferred to volatile storage in calibration DAC's after power is applied. Analog outputs are active during autocalibration.

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To compensate for aging, and to minimize the effects of temperature on accuracy, the autocalibration function determines the optimum calibration values for current conditions, and stores the new values in both the EEprom and the calibration DAC's. Autocalibration can be invoked at any time, but should not be implemented while the system is experiencing a major environmental transition such as that which usually occurs directly after power is applied.

Autocalibration is invoked by writing a value of "2" to CM[1:0], and has a duration of approximately 2-4 seconds. Completion of the operation can be detected either by monitoring CM[1:0] for a return to "0" value, or by selecting the 'calibration-mode operation complete' interrupt condition and waiting for the interrupt request. The autocalibration operation should be followed by initialization, in order to clear the contents of the analog input and output buffers.

3.6.3 Reading Calibration Values

The calibration values stored in internal EEprom can be transferred to the analog input buffer by writing a value of "3" to CM[1:0]. The duration of the transfer is approximately 2 milliseconds. Table 3-7 lists the relative locations of the 18 calibration values in the input buffer after the transfer has been completed.

Table 3-7. Calibration Value Locations

INPUT BUFFER POSITION	CALIBRATION FUNCTION
1 (First)	ADC Gain Correction
2	ADC Offset Correction
3	Gain Correction, Output Channel 7
4	Gain Correction, Output Channel 6
5	Gain Correction, Output Channel 5
6	Gain Correction, Output Channel 4
7	Gain Correction, Output Channel 3
8	Gain Correction, Output Channel 2
9	Gain Correction, Output Channel 1
10	Gain Correction, Output Channel 0
11	Offset Correction, Output Channel 7
12	Offset Correction, Output Channel 6
13	Offset Correction, Output Channel 5
14	Offset Correction, Output Channel 4
15	Offset Correction, Output Channel 3
16	Offset Correction, Output Channel 2
17	Offset Correction, Output Channel 1
18 (Last)	Offset Correction, Output Channel 0

A successful autocalibration operation produces 12-bit calibration values that are in the range of 0001h through 0FFEh. A 'saturation' value of either 0000h nor 0FFFh indicates that the associated channel is not calibrated. To ensure the integrity of all analog inputs and outputs, calibration values should be inspected for saturation after each autocalibration operation.

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3.7 Interrupt Control

In order for the board to generate a PCI interrupt, *both* of the following conditions must occur:

a. A *Local Interrupt Reques*t must be generated by the board's internal controller
b. The *PCI interrupt* must be enabled.

If the internal controller generates a local interrupt request, a PCI interrupt will not occur unless the PCI interrupt has been enabled as described in Paragraph 3.7.2.

3.7.1 Local Interrupt Request

The single local interrupt request line is controlled by the INTERRUPT A[2:0] and INTERRUPT REQUEST FLAG control bits in the BCR. The source condition for the request is selected as shown in Table 3-8. When the selected condition occurs, a local interrupt request is generated and the INTERRUPT REQUEST FLAG bit is set in the BCR. The request remains asserted until the BCR request flag is cleared by the PCI bus. A local interrupt request is generated automatically at the end of initialization.

Table 3-8. Interrupt Source Selection

INTERRUPT A[2:0]	INTERRUPT CONDITION
0	Idle. Interrupt disabled unless initializing. Default state.
1	(Reserved)
2	Calibration-mode operation completed
3	Analog input scan completed
4	Analog input buffer almost full
5	Analog output buffer almost empty
6	Analog input buffer empty
7	Analog output buffer full.

Detection of an interrupt condition or event is *edge-sensitive*. An interrupt request is generated if, and only if, a specific interrupt condition undergoes a *transition* from 'false' (not-true) to 'true' while that condition is selected.

3.7.2 Enabling the PCI Interrupt

A local interrupt request will not produce an interrupt on the PCI bus unless the PCI interrupt is enabled. The PCI interrupt is enabled by setting the *PCI Interrupt Enable* and *PCI Local Interrupt Enable* control bits HIGH in the runtime *Interrupt Control/Status Register* described in Section 4 of the PLX™ PCI-9080 reference manual..

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3.8 Data Format

Both analog input data and analog output data are represented in 16-bit offset binary format, as shown in Table 3-10. *Positive Full Scale* is a positive level that equals the range option defined for the board (e.g.: +5.000 Volts for the ±5V option). *Negative Full Scale* is the negative equivalent of positive full-scale . *Full-scale range* is the total voltage range for the input or output. One LSB equals the full-scale range divided by 65,536 (e.g.: 152.59 microvolts for the ±5V option).

Table 3-10. Offset Binary Coding

ANALOG INPUT OR OUTPUT LEVEL	DIGITAL VALUE (Hex)
Positive Full Scale minus 1 LSB	FFFF
Zero plus 1 LSB	8001
Zero	8000
Zero minus 1 LSB	7FFF
Negative Full Scale plus 1 LSB	0001
Negative Full Scale	0000

3.9 Programmable Rate Generator

A programmable rate generator provides an adjustable internal time base for the analog inputs and analog outputs. The generator can be configured to control either (a) the input scan rate, (b) the output strobe rate, or (c) both inputs and outputs simultaneously for input/output synchronization.

3.9.1 Rate Generator Frequency

The rate generator output clock rate **Rc** is calculated from the relationship:

Rc (Hz) = 20,000,000 / Nrate ,

where **Nrate** is the decimal equivalent of the 16-bit value in the Rate Generator Register located at local address 04h. Table 3-11 illustrates the effect of Nrate on the clocking rate. Values less than 80 (50h) for Nrate may produce unpredictable results, and are not recommended.

3.9.2 Rate Control Register

The rate generator output can be directed (a) to the analog inputs as a burst trigger, (b) to the analog outputs as an output strobe, or (c) to both analog inputs and outputs simultaneously. The Rate Control Register located at local address 0Ch performs this control function, as shown in Table 3-12.

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Table 3-11. Rate Generator Frequency Control

Offset: 04h **Default: 0064h**

Nrate (16 Bits)		CLOCKING RATE Rc *
(Dec)	(Hex)	(Clocks per Second)
80	0050	250,000
81	0051	246,914
82	0052	243,902
---	---	Rc (Hz) = 20,000,000 / Nrate
---	---	
---	---	
65535	FFFF	305.18

* ±0.015 percent.

3.9.2.1 Rate Controlled Analog Inputs

If the analog inputs are configured for burst triggering, and if the ENABLE INPUT RATE control bit in the rate control register is asserted, each clock from the rate generator triggers an input scan. The hardware trigger input and the BURST TRIGGER control bit in the BCR both are ignored in this mode.

To ensure that all clocks are acknowledged as input triggers, the rate generator frequency must not exceed the Maximum Scan Rate indicated in the product specification for single-ended or differential input configurations.

Table 3-12. Rate Control Register

Offset: 0Ch **Default: 0000h**

DATA BIT	R/W MODE	DESIGNATION *	DESCRIPTION
D00	R/W	LAST CHANNEL LC0	Control bits LC[2:0] designate the last-channel in an output channel group.
D01	R/W	LAST CHANNEL LC1	
D02	R/W	LAST CHANNEL LC2	
D03	R/W	(Reserved)	---
D04	R/W	ENABLE OUTPUT RATE	Enables the rate generator for analog output strobing.
D05	R/W	ENABLE INPUT RATE	Enables the rate generator for analog input burst triggering.
D06-D15	RO	(Reserved)	All zero.

3.9.2.2 Rate Controlled Analog Outputs

The rate control register enables the rate generator for analog output strobing, and designates the *last-channel* in an *output channel group*. When the ENABLE OUTPUT RATE control bit is asserted, each clock from the rate generator produces an analog output strobe. Also, when this bit is asserted, the analog output controller accumulates all data values from the output buffer in intermediate registers until the last-channel is detected. When the designated last-channel is detected, no further values are read from the buffer and the accumulated values are retained until a strobe is received from the rate generator. When the strobe is received, all accumulated output values are transferred immediately to their respective output DAC's, and the controller resumes reading data values from the output buffer.

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For example, suppose that the channel sequence in the output buffer is 1,2,4,6...1,2,4,6..., and that the last-channel is designated as "6" in the rate control register (LC[2:0] = 6). In this case the values for Channels 1, 2 and 4 are transferred to intermediate registers as they are received from the output buffer. When Channel-6 is received and identified as the last-channel, extraction of data values from the buffer ceases, and the values for all four channels are retained in their intermediate registers until a strobe is received from the rate generator. When the strobe occurs, all four channels are strobed (i.e.: transferred) simultaneously to their respective outputs, and extraction of the next channel group from the buffer commences.

To ensure that all clocks are acknowledged as output strobes, the rate generator frequency must not exceed the *Maximum Sample Rate* indicated in the product specification*, divided by the number of channels in the output channel group*. For example, if the specified maximum sample rate is 250 kHz, and an output group consists of Channels 2, 3, 4, 5 and 6, the maximum effective strobing frequency would be 50 kHz (250,000 ÷ 5).

The external hardware strobe is ignored in this mode, as are the OUTPUT STROBE and OUTPUT STROBE ENABLE control bits in the BCR.

3.10 DMA Operation

Two DMA channels support block mode and demand mode DMA transfers to and from the analog output and input buffers. DMA Channel-0 supports demand mode transfers from the analog input buffer, while demand mode analog output transfers to the board are assigned to Channel-1. Both channels support block-mode transfers.

Note: Availability of demand-mode DMA is indicated by a Firmware Revision (Table 3-1) in the range of 8000h through 8FFFh.

3.10.1 Analog Inputs

DMA transfers from the analog input buffer are supported with the board operating as bus master. Table 3-13 illustrates a typical PCI register configuration that controls a non-chaining, non-incrementing '***block-mode'*** DMA transfer, and in which a PCI interrupt is generated when the transfer has been completed. Bit 02 (0000 0004h) in the PCI Command register must be set HIGH to select the bus mastering mode. Refer to a PCI-9080 reference manual for a detailed description of these registers.

For most applications, the DMA Command Status register would be initialized to the value 0000 0001h, and then changed to 0000 0003h to initiate a transfer.

Bit-12 (0000 1000h) in the Channel-0 DMA Mode configuration register, when HIGH, selects ***'demand-mode'*** DMA operation, in which a DMA transfer is requested automatically when the number of values in the buffer ***exceeds a value of 0x6000***.

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The DMA request is sustained until one of the following events occurs:

(a) The data buffer goes empty,
(b) The board is reset,
(c) Autocalibration is executed.

The DMA request is terminated at the first occurrence of any of these events.

Table 3-13. Typical DMA Register Configuration; Analog Input Buffer

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

3.10.2 Analog Outputs

DMA transfers to the analog output buffer are similar to those from the analog input buffer, with the following exceptions:

a. The transfer direction is from the PCI bus to the Local bus,
b. Analog output demand mode transfers occur in DMA Channel-1.
c. The Channel-1 demand mode DMA request is asserted when the number of values in the analog output buffer ***becomes less than 0x1000***, and is sustained until:
   (1) The analog output data buffer goes full,
   (2) The board is reset,

3.11 Buffer Status Registers

As analog input data flows into the analog input buffer from the ADC, and is read from the buffer by the PCI bus, the 16-bit **Input Buffer Pointer** listed in Table 3-1 continuously indicates the number of samples contained in the buffer. A value of 0000h indicates an empty buffer, while a value of 8000h indicates a full buffer. The value contained in this read-only register can be used to determine the optimum block size to be read from the board during a DMA transfer operation.

Similarly, the **Output Buffer Pointer** continuously indicates the number of locations used in the output buffer. The number of locations equals twice the number of output samples in the buffer

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Status flags for both the input buffer and the output buffer are available as status bits in the read-only **Buffer Flags** register shown below in Table 3.14. Each flag is asserted HIGH if the indicated condition is true, or is LOW if the condition is false.

Table 3-14. Buffer Flags Register

Offset: 14h **Default: 0000h**

Register Bit	Designation	Function
D00 (LSB)	ANALOG INPUT BUFFER EMPTY	Asserted HIGH when the analog input buffer is empty.
D01	ANALOG INPUT BUFFER ALMOST FULL	Asserted HIGH when the analog input buffer has a remaining capacity of seven samples or less.
D02	ANALOG OUTPUT BUFFER FULL	Asserted HIGH when the analog output buffer is full.
D03	ANALOG OUTPUT BUFFER ALMOST EMPTY	Asserted HIGH when the analog output buffer contains three or fewer output values.
D04-D15	(Reserved)	---

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SECTION 4.0

PRINCIPLES OF OPERATION

4.1 General Description

The PMC-16AIO-88 board contains eight 16-Bit D/A converters, an 8-channel 16-bit scanning A/D converter, and all supporting functions necessary for adding analog I/O capability to a PMC host. Offset and gain trimming of the 16-bit ADC and output DAC's is performed by eighteen 12-bit DAC's (Figure 4-1). System analog inputs pass through a selftest network which can replace the system signals with either a precision voltage reference or the eight analog output channels, under software control. This arrangement is used during autocalibration to determine the offset and gain correction parameters for the ADC, and for each of the output D/A converters. Correction parameters are stored in a calibration EEprom for subsequent transfer to the calibration DAC's during board initialization. Autocalibration can be invoked at any time from the PCI bus.

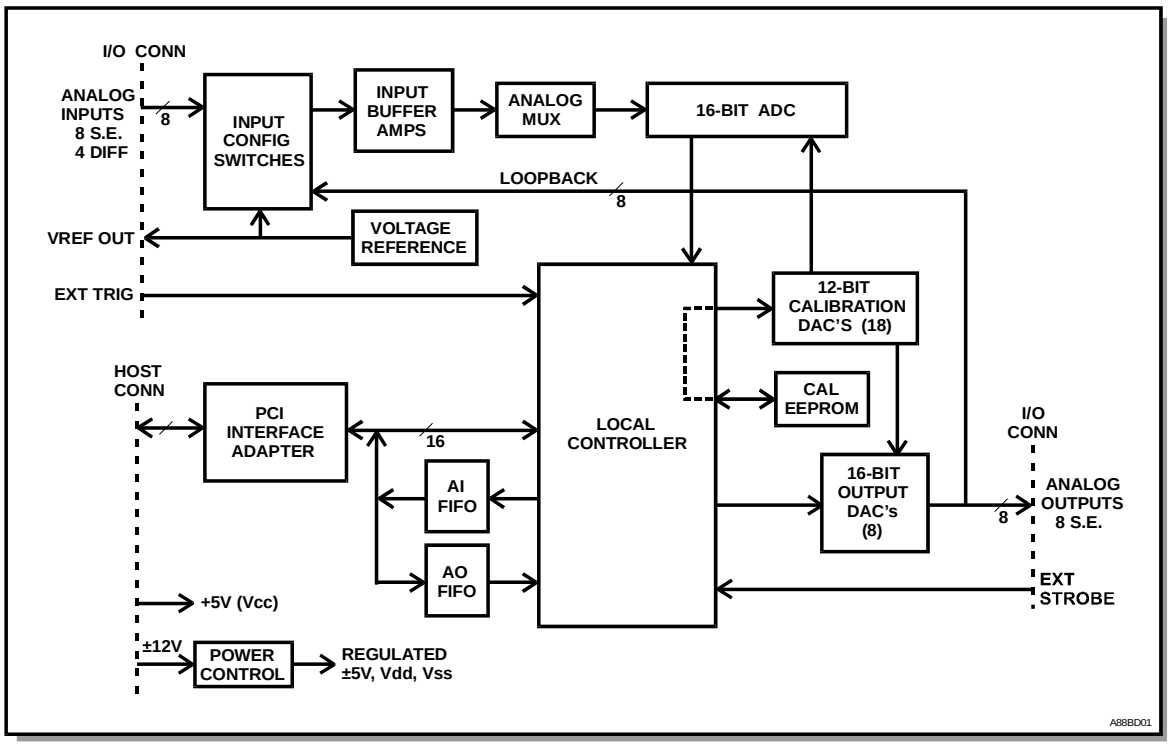


Figure 4-1. Functional Block Diagram

Analog output data and channel identification are received by the board through an analog output FIFO buffer. ADC conversion data and channel identification data are presented to the bus through an analog input FIFO buffer.

Communication with the host PCI bus is provided by a PCI Interface Adapter, which furnishes a 16-bit local bus for exchanging information between the FIFO buffers, the adapter, and the local controller. All internal operations are managed by the local controller.

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4.2 Analog Inputs

Analog-to-digital conversions can be performed on signals from any of several sources, which are selected by the input configuration switches shown in Figure 4-1. During normal operation, the analog input channels from the input/output connector are scanned and digitized. For selftest and autocalibration operations, the internal voltage reference can be routed through the switches to the ADC, or the analog output channels can be monitored by selecting the loopback selftest mode. The configuration switches also establish the input configuration as either single-ended or differential, in response to software control.

The selected input signals pass through input buffer amplifiers, and subsequently are sorted by an analog multiplexer for digitizing by the 16-bit ADC. The buffer amplifiers provide the fast response necessary to drive the analog multiplexer, and also serve to minimize interchannel crosstalk and to prevent charge coupling from the multiplexer back to the signal source. By routing all inputs through the same signal path, the errors introduced by components in that path are accounted for during autocalibration. Final selection of the input signal is provided by the analog multiplexer.

The output of the multiplexer is buffered by a differential amplifier in the ADC functional block, and finally is converted into a 16-bit digital code in offset binary format. Data is extracted from the ADC serially, and is converted to parallel format by the local controller before being written to the analog input FIFO buffer. Offset and gain trimming of the ADC is provided by a pair of 12-bit DAC's which are loaded with trim values that are determined during autocalibration.

Analog channels from the input/output connector are scanned in a pipeline sequence, in which the subsequent channel in the scanning sequence is selected and allowed to settle, while the current sample is being digitized. This approach increases the effective scan rate without requiring shorter settling or conversion times. In the software-selected continuous-scan input mode, all input channels are scanned continuously with no delay between scans. In the burst-scan mode, a single scan of all input channels occurs in response to a software or hardware trigger.

4.3 Analog Outputs

Each of the eight analog output channels consists of a 16-bit output DAC and two 12-bit trim DAC's. The local controller reads the channel number and 16-bit channel data for each channel from the analog output FIFO buffer, and sends the data serially to the appropriate output DAC. The output DAC deserializes the data into a 16-bit data word, and holds the word in an internal buffer until commanded to transfer the data to the output register that drives the DAC conversion ladder. If output strobing is selected by the control software, the transfer command is generated either by a software flag or by the external hardware strobe. If output strobing is not selected, the transfer command is generated automatically by the local controller immediately after the serial data word is sent to the output DAC.

The two trim DAC's in each output channel provide offset and gain trimming of the associated 16-bit output DAC, using trim values that are determined during autocalibration.

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4.4 Autocalibration

Autocalibration is an embedded control utility which calibrates all input and output channels to the single internal voltage reference. The utility can be invoked at any time by the control software, and has a duration of several seconds.

The internal voltage reference is adjusted during the calibration procedure described in Section 2 to equal approximately 99.9 percent of the input/output voltage range. The reference is used by the autocalibration utility to calibrate the ADC, which subsequently is used to calibrate the eight analog output channels.

Each of the 18 trim DAC's used on the board is adjusted in a successive approximation sequence which commences with the DAC in an all-zero state. The most significant bit initially is set to "1", and the resulting effect on the channel is measured. Depending upon the measured response, the bit is either cleared or left in the "1" state. The next lower significant bit is then tested in the same manner, and the process continues until all 12 bits have been tested and adjusted. The final value in the trim DAC is stored in the nonvolatile calibration EEprom for subsequent retrieval during initialization.

4.5 Power Control

Internal power voltages are generated from the +5 VDC PCI bus input, using regulated DC/DC converters and linear postregulators.

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APPENDIX A

LOCAL REGISTER QUICK REFERENCE

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APPENDIX A
LOCAL REGISTER QUICK REFERENCE

This appendix summarizes the local registers and principal control-bit fields described in Section 3.

Table 3-1. Control and Data Registers

OFFSET	16-BIT REGISTER	ACCESS*	DEFAULT	DESCRIPTION
00	BOARD CONTROL	R/W	2401h	Control and status monitoring
04	RATE GENERATOR	R/W	0064h	Rate generator clocking rate
08	INPUT / OUTPUT DATA	Read	---	Analog input data, Channel-00 first, followed sequentially by remaining channels in scan. Data format is offset binary.
		Write	---	Analog output channel and data. Written as two-word pairs, 3-bit channel first, followed by 16-bit data. Channel code is right-justified; data format is offset binary.
0C	RATE CONTROL	R/W	0000h	Rate generator utilization
10	INPUT BUFFER POINTER	RO	0000h	Number of samples remaining in the analog input buffer.
14	BUFFER FLAGS	RO	0009h	Input and output buffer status flags.
18	FIRMWARE REVISION	RO	XXXXh	Installed firmware revision.
1C	OUTPUT BUFFER POINTER	RO	0000h	Number of samples remaining in the analog output buffer.

* R/W = Read/Write, RO = Read-Only. ** Maintenance register; Listed for reference only.

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Table 3-2. Board Control Register

Offset: 00h **Default: 2401h**

DATA BIT	R/W MODE	DESIGNATION	DESCRIPTION
D00	R/W	AIM0	Analog input mode. Selects single-ended or differential input configuration, and the input operational mode. Defaults to burst-scan, single-ended input mode.
D01	R/W	AIM1	
D02	R/W	AIM2	
D03	R/W	LBC0	Loopback channel. Selects one of eight analog output channels for loopback testing. Active only in the Loopback selftest mode. Defaults to Channel-0.
D04	R/W	LBC1	
D05	R/W	LBC2	
D06	R/W	OUTPUT STROBE ENABLE	Enables internal/external analog output strobe. Disables automatic updating of outputs.
D07	R/W	INTERRUPT A0	Interrupt source selection.
D08	R/W	INTERRUPT A1	
D09	R/W	INTERRUPT A2	
D10	R/W	INTERRUPT REQUEST FLAG	Set HIGH when the board requests an interrupt. Clears the request when cleared LOW by the bus.
D11	R/W	* CM0	Calibration mode. Selects either normal operation or a calibration mode. Defaults to normal operation.
D12	R/W	* CM1	
D13	R/W	* OUTPUT STROBE	Analog output internal (software) strobe, and strobe-ready flag. When set HIGH internally, a strobe will not be accepted.
D14	R/W	* BURST TRIGGER	Analog input internal (software) burst trigger. Initiates a single scan of all analog input channels. Remains asserted until the scan is completed.
D15	R/W	* INITIALIZE	Initializes the board. Sets all defaults.

All bits asserted HIGH. * Cleared automatically when operation is completed.

Table 3-4. Analog Input Mode Selection

AIM[2:0]	FUNCTION OR MODE
0	Single-ended analog input configuration. Continuous scan; channels 0-7.
1	Single-ended analog input configuration. Burst scan; channels 0-7. Default state.
2	Differential analog input configuration. Continuous scan; channels 0-3.
3	Differential analog input configuration. Burst scan; channels 0-3.
4	Loopback Selftest: The analog output channel selected by LBC[2:0] is connected to analog input Channel-0. Single-ended input configuration. Burst scan; channel-0 only.
5	+VREF test: Internal voltage reference is connected to all analog input channels. Single-ended input configuration. Burst scan; channels 0-7.
6	(Reserved)
7	ZERO test: Internal ground reference is connected to all analog input channels. Single-ended input configuration. Burst scan; channels 0-7.

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Table 3-5. Loopback Test Channel Selection

LBC[2:0]	FUNCTION
0	Analog Output Channel 00; Default state.
1	Analog Output Channel 01
2	Analog Output Channel 02
3	Analog Output Channel 03
4	Analog Output Channel 04
5	Analog Output Channel 05
6	Analog Output Channel 06
7	Analog Output Channel 07

Table 3-6. Calibration Mode Selection

CM[1:0]	FUNCTION
0	Normal operation. No calibration activity. Default state.
1	Load calibration DAC's from EEprom. Performed automatically during initialization.
2	Invoke Autocalibration
3	Copy calibration values from EEprom to the analog input buffer.

Table 3-7. Calibration Value Locations

INPUT BUFFER POSITION	CALIBRATION FUNCTION
1 (First)	ADC Gain Correction
2	ADC Offset Correction
3	Gain Correction, Output Channel 7
4	Gain Correction, Output Channel 6
5	Gain Correction, Output Channel 5
6	Gain Correction, Output Channel 4
7	Gain Correction, Output Channel 3
8	Gain Correction, Output Channel 2
9	Gain Correction, Output Channel 1
10	Gain Correction, Output Channel 0
11	Offset Correction, Output Channel 7
12	Offset Correction, Output Channel 6
13	Offset Correction, Output Channel 5
14	Offset Correction, Output Channel 4
15	Offset Correction, Output Channel 3
16	Offset Correction, Output Channel 2
17	Offset Correction, Output Channel 1
18 (Last)	Offset Correction, Output Channel 0

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Table 3-8. Interrupt Source Selection

INTERRUPT A[2:0]	INTERRUPT CONDITION
0	Idle. Interrupt disabled unless initializing. Default state.
1	(Reserved)
2	Calibration-mode operation completed
3	Analog input scan completed
4	Analog input buffer almost full
5	Analog output buffer almost empty
6	Analog input buffer empty
7	Analog output buffer full.

Table 3-10. Offset Binary Coding

ANALOG INPUT OR OUTPUT LEVEL	DIGITAL VALUE (Hex)
Positive Full Scale minus 1 LSB	FFFF
Zero plus 1 LSB	8001
Zero	8000
Zero minus 1 LSB	7FFF
Negative Full Scale plus 1 LSB	0001
Negative Full Scale	0000

Table 3-11. Rate Generator Frequency Control

Offset: 04h **Default: 0064h**

Nrate (Dec)	(16 Bits) (Hex)	CLOCKING RATE Rc * (Clocks per Second)
80	0050	250,000
81	0051	246,914
82	0052	243,902
---	---	Rc (Hz) = 20,000,000 / Nrate
---	---	
---	---	
65535	FFFF	305.18

* ±0.015 percent.

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Table 3-12. Rate Control Register

Offset: 0Ch **Default: 0000h**

DATA BIT	R/W MODE	DESIGNATION *	DESCRIPTION
D00	R/W	LAST CHANNEL LC0	Control bits LC[2:0] designate the last-channel in an output channel group.
D01	R/W	LAST CHANNEL LC1	
D02	R/W	LAST CHANNEL LC2	
D03	R/W	(Reserved)	---
D04	R/W	ENABLE OUTPUT RATE	Enables the rate generator for analog output strobing.
D05	R/W	ENABLE INPUT RATE	Enables the rate generator for analog input burst triggering.
D06-D15	RO	(Reserved)	All zero.

Table 3-13. Typical DMA Register Configuration; Analog Input Buffer

PCI Offset	PCI Register	Function	Typical Value
80h	DMA Mode	Bus width (32); Interrupt on done	0002 0D43h
84h	DMA PCI Address	Initial PCI data source address	*
88h	DMA Local Address	Analog Input Buffer local address (Analog input buffer)	0000 0008h
8Ch	DMA Transfer Byte Count	Number of bytes in transfer	*
90h	DMA Descriptor Counter	Transfer direction; Local bus to PCI bus (Analog inputs)	0000 000Ah
A8h	DMA Command Status	Command and Status Register	0000 0001h 0000 0003h (See Text)

* Determined by specific transfer requirements.

Table 3-14. Buffer Flags Register

Offset: 14h **Default: 0000h**

Register Bit	Designation	Function
D00 (LSB)	ANALOG INPUT BUFFER EMPTY	Asserted HIGH when the analog input buffer is empty.
D01	ANALOG INPUT BUFFER ALMOST FULL	Asserted HIGH when the analog input buffer has a remaining capacity of seven samples or less.
D02	ANALOG OUTPUT BUFFER FULL	Asserted HIGH when the analog output buffer is full.
D03	ANALOG OUTPUT BUFFER ALMOST EMPTY	Asserted HIGH when the analog output buffer contains three or fewer output values.
D04-D15	(Reserved)	---

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