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Find the *General Standards PMC-24DSI12* at our website: *Click HERE*

24DSI12

12-Channel 24-Bit Delta-Sigma PMC Analog Input Board

With 200 KSPS Sample Rate per Channel

Available in PMC, PCI, cPCI and PC104-*Plus* and PCI Express form factors as:

PMC-24DSI12:	**PMC**, Single-width
PCI-24DSI12:	**PCI**, short length
cPCI-24DSI12:	**cPCI,** 3U
PC104P-24DSI12:	**PC104-*Plus***
PCIe-24DSI12:	**PCI Express**
PCIe104-24DSI12:	**PCIe, one-lane on PC/104 form factor**

See Ordering Information for details.
Call for availability of other form factors, such as XMC, CCPMC, etc.

FEATURES:

- **12 Differential 24-Bit Analog Input Channels**
- **Delta-Sigma Converter per Channel, with Linear Phase Digital Antialias Filtering**
- **Sample rates from 2 KSPS to 200 KSPS per Channel**
- **Software-Selectable Input Ranges: ±2.5V, ±5V, ±10V**
- 256 K-sample FIFO Buffer
- Synchronous or Independent ADC Clocking
- Internal Sample Rate Generators
- Hardware Sync and Clock I/O for Multiboard Synchronization
- Supports GPS Synchronization to a 1PPS Input
- Low Phase Skew; Typically Less than 55ns with Fsig < 0.35*Fsamp
- DMA Engine Supports both Block-Mode and Demand-Mode Transfers
- Low Power Consumption. 6 Watts Typical. Only +5VDC Required from PCI bus.
- 100dB Dynamic Range to 100KSPS; 93 dB SINAD
- On-demand Autocalibration Ensures DC Precision as well as AC performance
- Integrated DC/DC Conversion and Regulation of Precision Internal Supply Voltages
- Conforms to PCl Bus Specification, Revision 2.3, with Universal Signaling
- Triggered Acquisition feature supports external acquisition triggering
- Available on Adapters for Alternate Form Factors: PCI, cPCI, PC104-*Plus*

TYPICAL APPLICATIONS:

✓ Sonar Arrays	✓ Voltage Acquisition	✓ Phase Comparison
✓ Analog Inputs	✓ Acoustic Research	✓ Audio Waveform Analysis

REV: 011111

General Standards Corporation
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Overview:

The 12-channel PMC-24DSI12 analog input board provides high-density 24-bit analog input resources on a standard single-width PMC. Optimized for flexibility and performance, the board is ideal for a wide variety of applications, ranging from simple precision voltage measurements, to the analysis of complex audio signals and waveforms.

Functional Description:

Each of 12 analog input channels contains a lowpass image filter, and a delta-sigma A/D converter that provides digital antialias filtering. An internal voltage reference can be applied to all channels to support selftest operations and autocalibration. Gain and offset trimming is performed by applying correction values that are determined during on-demand autocalibration. A linear-phase digital antialiasing filter rejects out-of-band signals, and a lowpass analog filter reject those interference signals that fall within the harmonic images of the digital filter.

An internal sample-rate generator is adjustable over a 2:1 frequency range, and is divided down within the local controller to provide individual channel sample rates from 2KSPS to 200KSPS. Conversion data from all active channels is transferred to the PCI bus through a 256K-sample data buffer that is supported by two DMA channels. Multiple channels can be synchronized to perform sampling in "lockstep", either by a software command, or by external hardware sync and clock input signals.

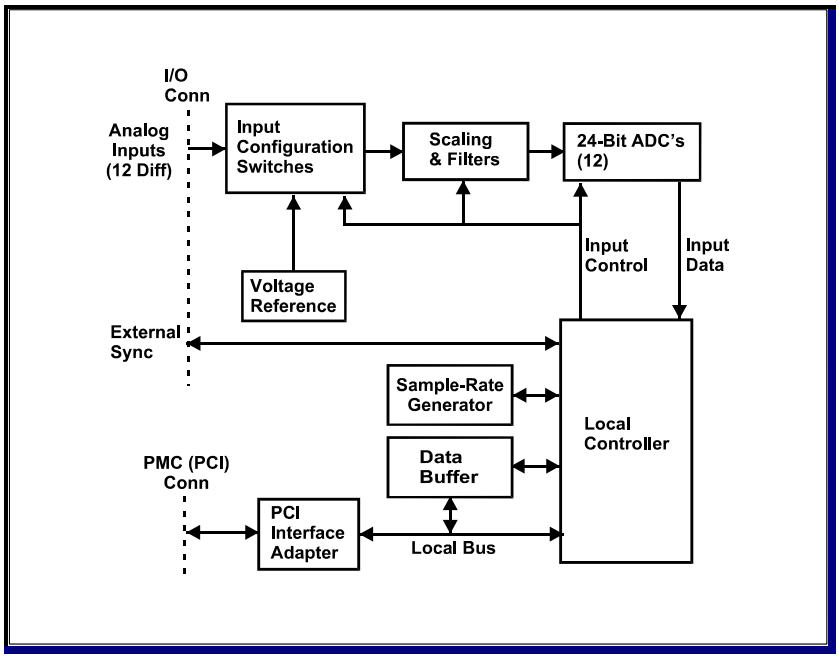


Figure 1. PMC-24DSI12; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3. System input/output connections are made at the front panel through a high-density 68-Pin I/O connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional 200 LFPM air cooling.

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ELECTRICAL SPECIFICATIONS

At +25 ^{O}C, with specified operating conditions.

Input Characteristics:

Configuration:	12 differential input channels. 8 and 4-channel configurations available.
Voltage Range:	Software Configurable as ±2.5 Volts, ±5 Volts or ±10 Volts
Input Impedance:	1.0 Megohm typical, in parallel with 20 pF. 2.0 Megohms line-line.
Common Mode Rejection:	80dB to 1kHz; 60dB to 50kHz.; typical
Common Mode Range:	±11 Volts with zero normal-mode input
Overvoltage Protection:	±25-Volt transients with power applied; ±45 Volts with power removed

Transfer Characteristics:

Quantizing Resolution:	24 Bits
Sample Rate:	2,000 to 200,000 samples per second per channel
Oversampling Factor:	2-50ksps: x128; 50-100ksps: x64; 100-200ksps: x32

DC Accuracy:
(Mean composite error after autocalibration)

Input Range	Midrange (Zero) Accuracy	Gain Accuracy at Fsamp 2-4ksps	4-15ksps	15-200ksps
±10V	±0.5mv	±0.9%	±0.3%	±0.1%
±5V	±0.3mv	±0.9%	±0.3%	±0.1%
±2.5V	±0.1mv	±0.9%	±0.3%	±0.1%

Bandwidth (-3dB): DC to typically 49 percent of selected sample rate for sample rates to 100KSPS, or to 35 percent of sample rate from 100kSPS to 200KSPS. Typically DC to 70 kHz overall.
0.1dB to 0.45Fsamp; 2-100KSPS; 0.24Fsamp 100-200KSPS.

Passband Ripple: ±0.06dB maximum

Phase Skew: Typically less than 55ns (0.1-Degree for Fsig = 5kHz), with Fsig/Fsamp <0.35; channel-channel (board-board for multiboard configurations), excluding noise, with high-frequency image filter.

ADC Stopband:

Sample Rate:	Threshold*	Rejection*
2-50KSPS:	0.58 Fsamp	93dB
50-100KSPS:	0.68 Fsamp	90dB
100-200KSPS:	0.78 Fsamp	95dB

* Typical values. (Fsamp = sample rate)

Antialias Filtering: Each ADC provides linear-phase digital antialias filtering as indicated for "ADC Stopband." A 2-pole Butterworth lowpass analog image filter in each channel provides a software-selected cutoff frequency of either 40kHz or 270kHz, and suppresses images from the digital filter. Optional alternative image filter frequencies are available, and should be selected to be well above the expected passband.

Dynamic Range: 100dB; typical 2 KSPS to 100 KSPS; 80dB from 100ksps to 200ksps.

SINAD: (Signal to Noise-and-Distortion ratio):
93dB typical to 10 kHz input bandwidth; 85 dB typical to 50 kHz.

Interchannel Crosstalk: -96dB typical to 50kHz

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Operating Modes and Controls:

Organization:	Two analog input channel groups. All channels in each group1 operate at the same sample rate, which is further controlled by division of the selected rate generator frequency. Each channel group contains one-half of the channels on the board, and can operate either synchronously from a single rate generator, or independently from either of two generators.
Sample Rate Generators:	Two independent internal PLL rate generators provide sample rates from 2.0 KSPS to 200 KSPS. The frequency of each generator is controlled by the ratio of two 10-Bit integers, and setting accuracy is 25 PPM. Older (legacy) products control each rate generator with a single integer, and are not recommended for new applications. This version will remain available however, as an ordering option.
External Clock I/O:	An LVDS or TTL hardware input clock can be derived either from a 25.6-51.2 MHz external hardware input or from an internal rate generator. Multiple boards can be locked to a common clock by daisy-chaining the output clock from each board to the input clock of the next board in the chain. Any number of boards can be daisy-chained together, with a typical propagation delay of 10ns introduced per board. The 'star-configuration' also is supported.
Synchronization:	Sampling of multiple channel groups can be phase-synchronized through software, or each group can be synchronized to an external hardware clock input. Daisy-chained hardware sync inputs and outputs can be used to synchronize sampling among multiple boards. Synchronization to a 1PPS GPS input also is supported.
Data Format:	Software-selectable as either offset binary or two's complement. Width of the data-field is selectable as 16, 18, 20 or 24 bits.
Channel Tags:	A 4-bit channel tag is appended to each input data value.
Buffer Threshold Flag:	Asserted when the number of samples in the selected buffer exceeds the selected threshold. The threshold can be any integer from zero to 3 FFFEh.
Buffer Access:	The input buffer FIFO is accessed through either of two DMA channels, with both block-mode and demand-mode transfers supported.
Triggered Acquisition	Allows an external event to initiate data acquisition.

PCI Compatibility:

Conforms to PCI Specification 2.3: D32, 33MHz, universal (3.3V/5V) signaling.

Supports "plug-n-play" initialization.

Single multifunction interrupt on INTA#.

Two-Channel DMA as bus master in block and demand modes.

Power Requirements:

+5.0 VDC ±0.25 VDC at 1.2 Amps typical, 1.5 Amps, maximum

Maximum Power Dissipation: Side-1: 6.5 Watts. Side 2: 1.0 Watt.

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Mechanical Characteristics:

(HxWxD): 13.5 mm (0.53 in) x 74.0 mm (2.91 in) x 149.0 mm (5.87 in)

(Mechanical dimensions are shown for the native PMC form factor. See Ordering Information.)

Environmental Specifications:

Ambient Temperature Range:

Standard Temperature:	Operating: 0 to +70 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
Extended Temperature:	Operating: -40 to +80 Degrees Celsius * Storage: -40 to +85 Degrees Celsius
	* Air temperature at board surface.
Relative Humidity:	0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

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Ordering Information:

Specify the basic product model number followed by an option suffix "-A-B-C", as indicated below. For example, model number PMC-24DSI12-12-SF describes a PMC module with 12 input channels, standard lowpass analog filter frequencies and standard operating temperature range.

Basic Model Number	Form Factor
PMC-24DSI12	PMC (Native)
PCI-24DSI12[1]	PCI, short length
cPCI-24DSI12[1]	cPCI, 3U
PCIe-24DSI12[1]	cPCI, 3U
PC104P-24DSI12	PC104-*Plus* (Native)
PCIe104-24DSI12[1,2]	PCIe, one-lane on PC/104 form factor

[1] Module installed and tested on an adapter, with mechanical and functional equivalency. Contact factory for availability in native form factors.

[2] PCIe104 supports only the PCIe bus.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	4 Channels	A = 4
	8 Channels	A = 8
	12 Channels	A = 12
Image Filter Frequencies	Standard 40kHz and 270kHz	B = SF
	Custom Frequencies: 100Hz and 20kHz	B = CF1
	Custom Frequencies: (TBD)	B = CF2 *
Operating Temperature	Standard Range: 0 to +65 Deg-C	C = S (or Blank)
	Extended Range: -40 to +80 Deg-C	C = ET *
Rate Generator	Legacy rate generator	D = L (or Blank)
	PLL Rate Generator (recommended)	D = PLL

* +/-12%, 1kHz-300kHz; 22%, 100Hz-1kHz.. Contact factory for availability of specific frequencies.

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SYSTEM I/O CONNECTIONS

I/O CONNECTOR PIN ASSIGNMENTS

ROW-A	
PIN	**FUNCTION**
1	INPUT RETURN
2	INPUT RETURN
3	**INP CHAN 00 LO**
4	**INP CHAN 00 HI**
5	INPUT RETURN
6	INPUT RETURN
7	**INP CHAN 01 LO**
8	**INP CHAN 01 HI**
9	INPUT RETURN
10	INPUT RETURN
11	**INP CHAN 02 LO**
12	**INP CHAN 02 HI**
13	INPUT RETURN
14	INPUT RETURN
15	**INP CHAN 03 LO**
16	**INP CHAN 03 HI**
17	INPUT RETURN
18	INPUT RETURN
19	**INP CHAN 04 LO**
20	**INP CHAN 04 HI**
21	INPUT RETURN
22	INPUT RETURN
23	**INP CHAN 05 LO**
24	**INP CHAN 05 HI**
25	VTEST RETURN
26	**VTEST**
27	DIGITAL RETURN
28	DIGITAL RETURN
29	**EXT CLK INP LO**
30	**EXT CLK INP HI ***
31	DIGITAL RETURN
32	DIGITAL RETURN
33	**EXT SYNC INP LO**
34	**EXT SYNC INP HI ***

ROW-B	
PIN	**FUNCTION**
1	INPUT RETURN
2	INPUT RETURN
3	**INP CHAN 06 LO**
4	**INP CHAN 06 HI**
5	INPUT RETURN
6	INPUT RETURN
7	**INP CHAN 07 LO**
8	**INP CHAN 07 HI**
9	INPUT RETURN
10	INPUT RETURN
11	**INP CHAN 08 LO**
12	**INP CHAN 08 HI**
13	INPUT RETURN
14	INPUT RETURN
15	**INP CHAN 09 LO**
16	**INP CHAN 09 HI**
17	INPUT RETURN
18	INPUT RETURN
19	**INP CHAN 10 LO**
20	**INP CHAN 10 HI**
21	INPUT RETURN
22	INPUT RETURN
23	**INP CHAN 11 LO**
24	**INP CHAN 11 HI**
25	INPUT RETURN
26	INPUT RETURN
27	DIGITAL RETURN
28	DIGITAL RETURN
29	**EXT CLK OUT LO**
30	**EXT CLK OUT HI ***
31	DIGITAL RETURN
32	DIGITAL RETURN
33	**EXT SYNC OUT LO**
34	**EXT SYNC OUT HI ***

* TTL signal levels when TTL sync I/O is selected.

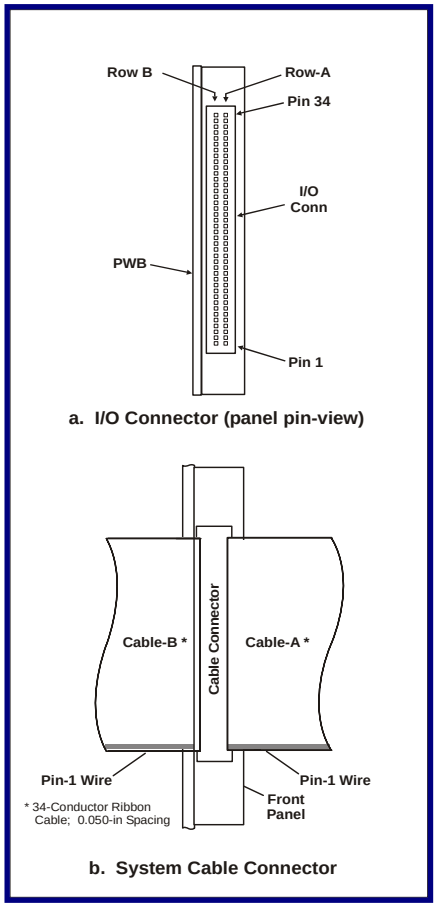


Figure 2. System I/O Connector

System Cable Mating Connector:

68-pin 0.050" Subminiature connector: with metal shield:
AMP #749621-7 or equivalent.

I/O Connector Installed on Board (Ref)**:**

Amp # 787170-7

General Standards Corporation assumes no responsibility for the use of any circuits in this product. No circuit patent licenses are implied. Information included herein supersedes previously published specifications on this product and is subject to change without notice.

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