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PMC-HPDI
PMC bus Very High-speed
Parallel Digital Interface
(with 132 Mbytes/s PMC-DMA engine)



The PMC-HPDI board is a very high speed parallel digital interface. It provides for bi-directional data transfers between two PMC computers or between PMC and an external digital interface at up to **40 Mbytes per second** and can transfer data indefinitely without host intervention. The board employs General Standards' high performance PMC-DMA (PLX) engine. The PMC-DMA is easily set up and operated by writing only a few programming instruction statements to the board. Once the PMC-HPDI link between two PMC computers is established, the desired data transfers between the two computers is performed and is transparent to the user. FIFO buffering decouples the cable and the PCI bus, providing for efficient data transfers to/from the PMC host CPU board.

FEATURES

- 40 Mbytes per second peak cable transfer rate
- Two boards cabled together perform a high performance PMC-to-PMC link
- A single board can interface to a wide variety of external high-speed devices
- "Deep (128 Kbytes) FIFO buffers" allow data bursts to be transferred over the PMC independent of transfers over the cable.
- Input or output direction is software selectable
- On-board cable controller, FIFOs, and PMC-DMA engine provide for continuous data transfer capability
- 132 Mbytes/s transfer rate to/from the PMC bus and on-board high-speed FIFOs.
- Data input clock rate up to 20 MHz
- Data input/output widths of 16 bits (Differential Transceivers)
- "Program-and-forget" DMA engine handles D32 transfers across the PMC interface
- Sample software available
- Interrupts available upon DMA-completion, FIFO status, and a 4-bit identity code
- Status bits on the cable are readable in a linked PMC-HPDI configuration
- Large programmable logic devices allows for easy interface to user devices
- Flexibility and reliability are improved via use of CPLDs

APPLICATIONS

- Camera interface
- High speed link for connecting two PMC based computers.
- High speed video data transmitter/simulator for testing software
- High speed video data capture/generation

- High speed network utilizing a PMC backplane as the network
- General Purpose Parallel DMA interface
- Development and research
- Trainers and simulators
- Satellite/telemetry/radar data ingestion
- Sonar or seismic data capture

Functional Description

The PMC-HPDI board includes the PMC-DMA engine, FIFO memory, a cable input/output controller, and cable transceivers (RS-422/485). The DMA engine is capable of transferring data from host memory using D32 block transfers; whereas, the FIFO memory provides a means for continuous transmission of data without interrupting the DMA transfers or requiring intervention from the Host CPU. The board also includes interrupt generation for interface flexibility, FIFO status and end-of-transfer indication.

Cable Interface
The cable interface provides for very high speed transmission of data (up to 40 M bytes/sec). Using differential I/O drivers (RS-422/484) it provides for a data width of 16 bits. External interrupt inputs can be individually enabled.

High Performance Architecture
The board is designed for the highest performance level using conventional (and moderately priced) components. The PMC-DMA engine is designed to require minimal intervention from the host; it provides for high speed transfers from PMC memory to FIFO memory using DMA instructions (similar to command chaining) stored in RAM. Data is transferred between the FIFO and the cable using a high speed dedicated I/O controller.

Programmable Logic Implementation
The design makes extensive use of large programmable logic devices to provide for: 1) improved reliability; 2) minimized spare requirements (same board can be programmed to implement several user cable interface protocols); and 3) design flexibility to meet unexpected interface requirements.

Custom Interfaces Facilitated
Large complex programmable logic devices (CPLDs) accommodate custom user interface functions. Custom interfaces may be built to handle a variety of high-speed parallel and serial interfaces. The custom interface can be implemented by GSC or by the customer.

Specifications

DMA Transfer Rates
Transfer Rate over cable:
40 M bytes/sec at 20 MHz clock rate and 32-bit data bus width.

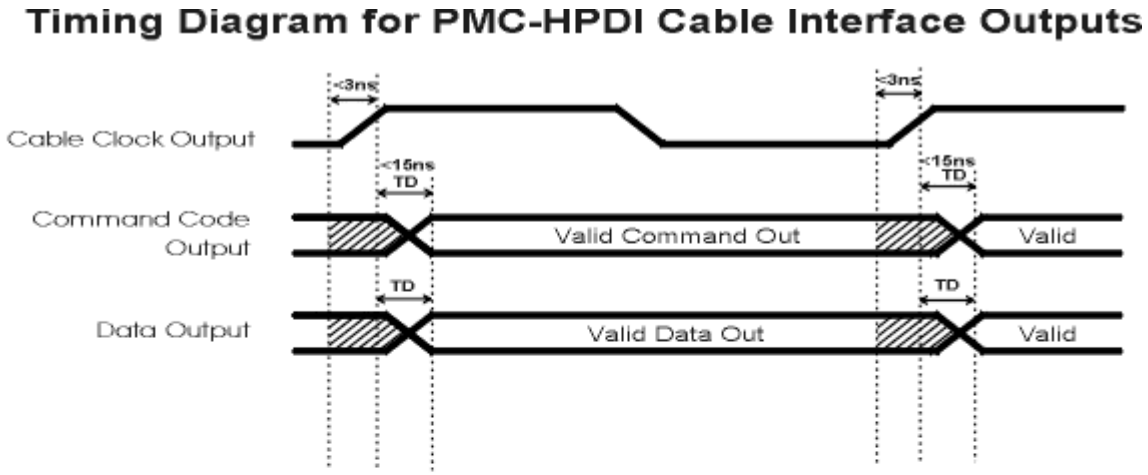
PMC transfer rate from on-board FIFO to/from PMC:
132 Mbytes/sec max (100 Mbytes/sec typ)

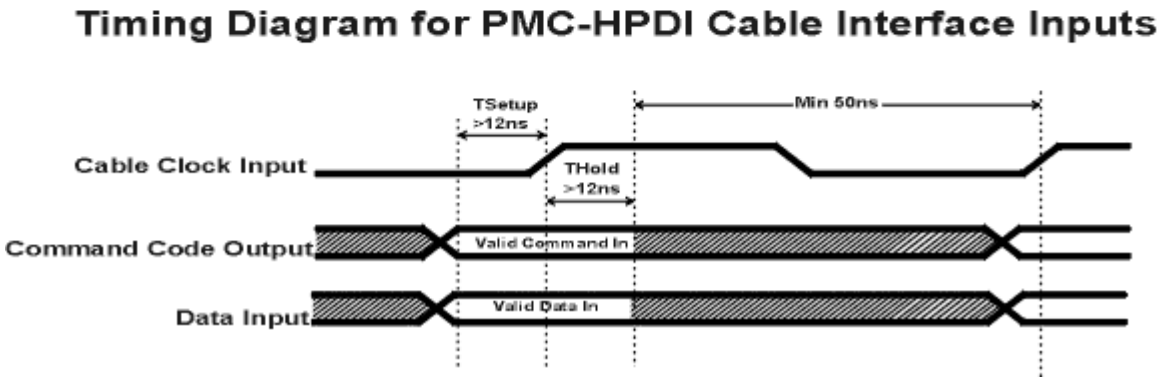
Data transfers over the cable do not interrupt data transfers over PMC since data is decoupled using FIFO buffering. DMA Start Latency (when started by cable input or by CPU) MOVE- instruction: 2 micro-seconds typical (estimate)

FIFO Memory
32 KWords (x4 bytes)deep FIFO - 128 Kbytes total

Interrupts
Interrupt upon DMA engine done and FIFO status
Interrupt upon the reception of a 4-bit identity code (via the cable)

Cable Interface Timing Diagram





Cable Interface Transceivers
RS-422/485 levels (contact factory for availability of TTL levels)
RS-422/485 transceivers provide +- 7.5 Volts of noise immunity and can withstand ±25 Volt transients without damage.

Optional on-board bias resistors or parallel termination: The bias resistors provide a predetermined logic level for open inputs, whereas the parallel terminators provide the usual transmission line termination. In either case unused inputs can be left open; however, the logic level of unconnected inputs is indeterminate with simple parallel terminators.

PMC Interface
Compliant wth PMC specification 2.1
32 bit address / 32 bit data, multiplexed

Power Requirements
+5V +-0.2V at 1 amp (typ)

Physical (PMC-HPDI)
Single PMC size (5.9 in.x 2.9 in.)

Environmental Specifications
Ambient Temperature Range
Operating: 0 to +55 degree Celsius
Storage: -40 to +85 degree Celsius

Relative Humidity
Operating: 0 to 50%, non-condensing
Storage: 0 to 95%, non-condensing

Altitude: Operation to 10,000 ft.

User Connector
Robinson Nugent - # P50E-068P1SR1TG
(on-board connector)

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