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VME-SIO4A

User Manual

Manual Revision: B

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PREFACE

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This user's manual provides information on the specifications, theory of operation, register level programming, and installation of the VME-SIO4 board.

Information required for customized hardware/software development.

This manual assumes that the user is familiar with the VMEbus interface specification. In an effort to avoid redundancy, this manual relies on data books, other manuals, and specifications as indicated in the related publication section.

Related Publications

The following manuals and specifications provide the necessary information for in-depth understanding of the VMEbus and specialized parts used on this board.

EIA Standard for the RS-422-A Interface (EIA order number EIA-RS-422A)

VMEbus Specification Manual (also known as IEC 821 BUS and IEEE P10114/D1/2), for information submit request to:

VITA10229 North Scottsdale Road, Suite B
Scottsdale, AZ 85253
Telephone: 602-951-8866

Zilog's USC Universal Serial Controller (part number: Z16C30) User's Manual and Databook, for information submit request to:

Zilog, Inc.
210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone: 408-370-8000

VME-SIO4 Documentation History

1) The Vme-SIO4 documentation was updated March 1997.
2) The manual was reformatted, for conformity of text, and the table of contents was corrected.
3) The jumper field drawings in Chapter 4 were redrawn and double checked.
4) April 27, 1997: Chapter 3, page 3, Section 3.1.2.1, D6 & D7 bit descriptions were corrected, instead of: 0 will enable Rx…, it was corrected to be a 1 will enable Rx.., and instead of 1 will disable Rx.., it was corrected to be a 0 will disable Rx…
5) April 27, 1997: Chapter 4, page 2, Section 4.3, added pin numbers for J11 & J14 drawing, changed pin 6, & 11 to circles, they were previously squares which represent pin 1.
6) August 15, 1997: merged all files into one.
7) September 15, 1997: corrected errors Section 4.0 and 4.1, typos.
8) September 29, 1997: corrected errors, Section 1.2: deleted reference to figure 1.2-1 Corrected addresses, Sections: 3.1.6.14.2, 3.1.6.15.1, 3.1.6.15.2, 3.1.6.25.1, and 3.1.6.25.2. Temporarily inserted Figure 1.1-1 after Section 1.2. Verified all serial control register offset addresses.
9) September 30, 1997: Section 3.1.5.3, moved D3..7 and D8..15 to end of list, deleted D0..7(text). Changed heading format, created new table of contents. Section 2.3: Reworded, Section 3.1.2.1: added note about self-timed pulse, Section 3.1.4: changed reference to: is status and is not status to: is empty and is not empty. Section 3.1.5.1: added almost to bit descriptions D11and D13. Section 3.1.5.3: inserted description of vector register encoding. Section 3.1.6: inserted reference to Zilog references, which were also inserted into related publications. Section 3.1.6.1.1: added WO to description. Inserted block diagram (figure 1.1-1) directly after section 1.2. Section 1.0,a., (6): added note about VME DMA controller.
10) October 1, 1997: Section 3.1.1.3: added self-timed note to bit D0's description, Section 3.1.4, Section 3.1.5.1, and Section 3.1.5.2: reworded bit descriptions to be more understandable. Section 3.1.5.3: Changed to hardware encoded and software selectable. Section 3.1.5: reworded serial controller note. Section 3.1.6.16: changed Receive Data Register to Status Interrupt Control (which was left out) and inserted it's bit descriptions. Section 3.1.6.17: made Low and High both Tx and Rx.
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CHAPTER 1: INTRODUCTION

1.0 INTRODUCTION

The VME-SI04 interface card is capable of transmitting and receiving serial data, generating interrupts, and providing loop-back testing.

This card provides the following specific functionality:

a. VMEbus Interface:
   (1) 6U card (single slot. IEEE/ANSI-1014 compliant; A16/D16 support or better.
   (2) VMEbus interrupter functionality.
   (3) Jumper selectable configuration of the interrupt level and programmable interrupt vectors.
   (4) FIFOs (32K x 8 bit) are provided for data transmit and for data receive to increase the size of the transmit and receive buffers
   (5) User interface signal connections are provided via 4 connectors on the front panel.
   (6) All data transfers to/from the FIFOs will be via host CPU writes/reads, i.e., the board does not include a VME DMA controller, hence this board cannot act as a VME bus master.
   (7) The card also provides for self-test loop-back for verification of proper operation.

b. The following two modes of loop-back testing will be supported:
   (1) internal loop-back testing (does not drive cable);
   (2) external loop-back testing via an external loop-back test cable.

1.1 FUNCTIONAL DESCRIPTION

As shown in the functional block diagram (see Figure 1.1-1), this board includes the following:

a. VMEbus slave interface;
b. VMEbus interrupt module;
c. board control/status registers;
d. transceiver control logic;
e. LEDs for board status indication;
f. an oscillator (for synchronization of all logic on the board);
g. a cable data driver;
h. a cable data receiver (receive voltage level converter);
i. a transmit FIFO;
j. a receive FIFO.

1.2 BOARD IDENTIFICATION

Two (2) read-only registers will be provided for board identification:

a. manufacturer's ID; and
b. board type.

These two registers will be modeled after the VXI specification.

The manufacturer's ID register will return 0xFEAC when read, while the board type register will return 0xF4E4 when read. These two registers will give an indication of basic board response.

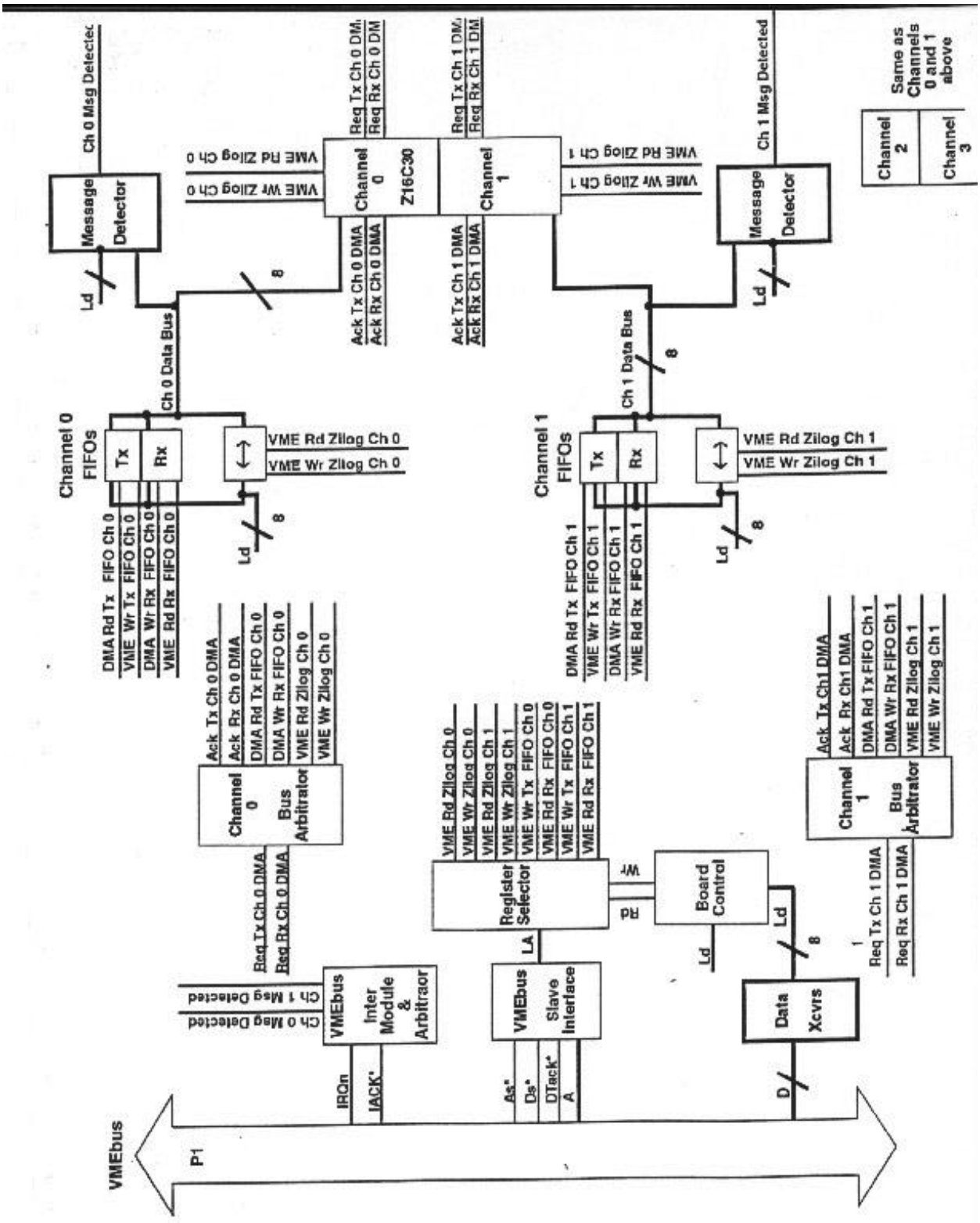


Figure 1.1-1: Functional Block Diagram

1.3 BOARD CONTROL REGISTER

The board control register will provide configuration of the board, including the self-test modes.

1.4 BOARD STATUS REGISTER

The board status register will provide status with regard to receive FIFO status and transmit FIFO status.

1.5 SYNC WORD SELECTION

The sync word selection is used to provide an interrupt upon the reception of a particular character. This character is software programmable.

1.6 DATA RECEPTION

Data is received into the Zilog Z16C30, after which the software may retrieve the data from the Z16C30 or the main Rx FIFOs, depending on how the Z16C30 has been initialized.

1.7 DATA TRANSMIT

Data is received into the Zilog Z16C30, after which the software may write data to the master FIFOs or to the Zilog depending on how the Z16C30 has been initialized. At this point, the Zilog can be placed into a transmit mode.

1.8 LOOP-BACK TESTING

The card is designed with sufficient built-in loop-back testing capability in order to allow software to perform fault isolation to the VME card level, and replacement within 30 minutes.

The following modes of loop-back testing are supported:

a. internal loop-back testing (does not drive the cable);
b. external loop-back testing via an external loop-back test cable.

1.9 ERROR DETECTION

Error detection built into the board includes the following:

a. parity error detection;
b. CRC error detection;
c. Rx overrun;
d. Tx underrun.

1.10 INTERRUPTS

Interrupts will be provided for the following conditions:

a. Sync word detected;
b. Tx FIFO empty;
c. Rx FIFO not empty;
d. Rx FIFO almost full.

Interrupt status bits are cleared by writing a 1 to the respective bit in the interrupt status register. A second interrupt from that bit will not occur until after that status bit has been cleared.

1.11 DIAGNOSTIC LED DISPLAYS

LEDs provide for indication of the following conditions:

a. BIT loop-back pass/fail status (FAIL LED);
b. Channel 0 Receiver is empty
c. Channel 1 Receiver is empty
d. Channel 2 Receiver is empty
e. Channel 3 receiver is empty
f. IRQ Pending
g. VME Access
h. Spare LED.

1.12 CABLE INTERFACE CONNECTIONS

There are four female DB25 cable interface (user I/O interface) connectors mounted at the front edge of the board: P3 – Channel 0, P4 – Channel 1, P5 – Channel 2, P6 – Channel 3. The pinout is shown below:

Signal Name	**Rev N/R**	**Rev A**
Lower TxD/RxD +	Pin 25	Pin 3
Lower TxD/RxD -	Pin 12	Pin 16
Lower CTS/DCD +	Pin 24	Pin 5
Lower CTS/DCD -	Pin 11	Pin 18
Lower Tx/Rx CLK +	Pin 23	Pin 9
Lower Tx/Rx CLK -	Pin 10	Pin 22
Upper TxD/RxD -	Pin 9	Pin 10
Upper TxD/RxD +	Pin 22	Pin 23
Upper CTS/DCD -	Pin 8	Pin 11
Upper CTS/DCD +	Pin 21	Pin 24
Upper Tx/Rx CLK -	Pin 7	Pin 12
Upper Tx/Rx CLK +	Pin 20	Pin 25

CHAPTER 2: THEORY OF OPERATION

2.0 THE BOARD INTERFACE

This board operates as an interface for two Zilog Z16C30s, giving it Quad Channel capabilities. The Zilogs are mapped into the base address of this board and all reads and writes are PIOs. This board does not offer DMA across the VMEbus. All references to DMA in this documentation are in reference to moving data from the external FIFOs into the Zilogs or from the Zilogs into the receive FIFOs, by means of an "onboard only" DMA. These FIFOs operate as additional buffering of 32 K bytes for both transmit and receive. These FIFOs are in addition to the internal FIFOs of the Zilog; however, these FIFOs are not at the same address location. To implement the use of the external FIFOs, the software must first initialize the Zilog to request DMA services for transmit or receive. When the request is made, the onboard logic will either move the data from the transmit FIFO into the Zilog or from the Zilog into the receive FIFOs depending on which request was made.

2.1 INTERRUPTS

The interrupts on this board are divided into two sections:

a. **Master Board Interrupts:** For use with conditions on the board, not pertaining to the Zilogs.
b. **Zilog Interrupts:** For use with conditions within the Zilog, not pertaining to the Board.

The interrupts for the onboard logic use the master vector register. The interrupts for the Zilog use the Zilog vector registers. All interrupts are mapped directly to the VME and they are prioritized via "Round Robin" going from 0 to 3 and then to the master board. No two levels of interrupts will occur at the same time. The interrupt level is selected via jumper.

2.2 DESCRIPTION OF DMA

DMA for all channels is performed in the same manner. The request is made, that is, one of the transmit or receive DMA request signals go active from the Zilog. The onboard DMA logic will handshake with the Zilog to either acknowledge valid data going to the Zilog or to get receive data from the Zilog. This activity will continue until the Zilog no longer needs DMA service, or the external FIFOs can no longer comply. If the Zilog no longer wants DMA, it will remove its request and the DMA will stop. The conditions at which the FIFOs can no longer comply are when during a transmit request and the transmit FIFO is empty or during a receive request when a receive FIFO is full. Channel 0 and 1 operate using the same Zilog bus, so therefore it must arbitrate between Channel 0 transmit and receive, as well as Channel 1 transmit and receive. This arbitration takes place without any software initialization.

If all four (4) DMA requests are active at the same time, this will handshake one word for one request and then proceed to the next. It will start with the receive data and will acknowledge one word for the receive of Channel 0, then one word of the receive for Channel 1, then one word for the transmit for Channel 0, then one word of the transmit for Channel 1 and then it will start over.

This transmission of data from one point to another will only occur if the FIFO's are in a valid state, i.e., transmit FIFO must not be empty; otherwise the handshake will not take place with the Zilog. Then, the Zilog will not get an acknowledge for its' transmit request and will get no data.

The same is true for the receive FIFO. If the receive FIFO is full, the DMA will not remove data from the Zilog. Therefore the Zilog will not get an acknowledge, and will not have any data removed from it.

Channels 2 and 3 work in the same way, but work on a different data bus. Therefore DMAs for Channels 2 and 3, to or from the Zilog will not affect Channels 0 and 1. This means Channel 0 can run at full speed and Channel 2 can

run at full speed without interfering with each other. The VME can read and write the Zilog during DMA cycles. However, it must wait until the end of the current DMA access when the DMA finishes its current access, then the VME will be allowed onto the Zilog bus.

When the Zilog bus is free from the VME, the DMA will restart. The same holds true for interrupts. If a VME or interrupt access to or from the Zilog is currently taking place, and a DMA request is made, the DMA will wait until the current access cycle has completed and the bus for the Zilog is free before it starts the DMA transfers.

2.3 CABLE

The Cable is configured as upper and lower so that one cable can be used for both transmit and receive, therefore allowing full duplex capabilities for each channel. Each channel has a control register that can be set to transmit upper or lower and to receive upper or lower. It is not possible to receive both but it is possible to transmit both. If the channel control register is not told to transmit or receive upper and not told to transmit or receive lower, then this board will not drive the cable, nor will it load the cable, i.e., this channel will be tri-stated.
If an external loopback test is desired to be performed without a cable, the software can set it up to do transmit, upper or lower, and to receive the same. The effect given will be an external loopback without a cable.

2.4 TRANSMIT RECEIVE CLOCK

The transmit receive clock is controlled via a 3 x 5 jumper. If the jumper is removed, for a particular clock, it is expected that the Zilog will produce the transmit receive clock. It cannot output a clock to the half of the cable that it is receiving from. It can output a clock to the cable it is transmitting to. If the jumper is selected for “receive clock”, the Zilog will get its’ clock from the cable, given that the software has chosen the cable as receive. If the Zilog clock is chosen for the onboard transmit receive clock, then the Zilog will get its’ clock from the local oscillator, factory installed at 20.0 megahertz.

NOTE: Care must be taken when setting these jumpers. If the jumper is installed and the Zilog drives a clock out, then a conflict between clocks will exist.

CHAPTER 3: PROGRAMMING

3.0 REGISTER MAP

The register address map for the VME-SI04 is shown below.. This board contains registers for Board Control, I/O Control, FIFO Control, Interrupt Control and Serial Controller.

Table 3.0-1 VME-SI04 Register Address Map

	Address Offset	Size*	Access**	Register Name
Board Control/Status Registers	0x00	D16	RO	Board ID
	0x02	D16	RO	Device Type
	0x08	D16	RW	Board Control
	0x0A	D16	RO	Board Status
Channel Control Registers	0x10	D16	RW	Channel 0 Control
	0x12	D16	RW	Channel 1 Control
	0x14	D16	RW	Channel 2 Control
	0x16	D16	RW	Channel 3 Control
FIFOs	0x18	D16	RW	Channel 0 FIFO
	0x1A	D16	RW	Channel 1 FIFO
	0x1C	D16	RW	Channel 2 FIFO
	0x1E	D16	RW	Channel 3 FIFO
FIFO Status Registers	0x20	D16	RO	Channel 0 FIFO Status
	0x22	D16	RO	Channel 1 FIFO Status
	0x24	D16	RO	Channel 2 FIFO Status
	0x26	D16	RO	Channel 3 FIFO Status
Sync Word Registers	0x28	D16	RW	Channel 0 Sync Word Register
	0x2A	D16	RW	Channel 1 Sync Word Register
	0x2C	D16	RW	Channel 2 Sync Word Register
	0x2E	D16	RW	Channel 3 Sync Word Register
Interrupt Control/Status Registers	0x30	D16	RW	Interrupt Control
	0x32	D16	RW	Interrupt Status
	0x34	D16	RW	Interrupt Vector
Serial Controller Registers	0x200-27E	D16	BD	Channel 0 USC Control
	0x280-2EE	D16	BD	Channel 1 USC Control
	0x300-37E	D16	BD	Channel 2 USC Control
	0x380-3EE	D16	BD	Channel 3 USC Control

* The register address offset can be selected to be in short address space (A16) or in standard address space (A24).

** RO = read only
WO = write only
RW = read/write capability
BD = Bit Dependent

3.1 REGISTER BIT MAPS

All Reserved bits should be set to *0* for future compatibility. Also, the value read from a reserved bit will be indeterminate.

3.1.1 BOARD CONTROL/STATUS REGISTERS:

3.1.1.1 Board ID Register:

D0..D16 Reads back hex CEAC

3.1.1.2 Device Type Register:

D0..D16 Reads back hex F4E4

3.1.1.3 Board Control Register:

D0 Board Reset L (pulsed)
1 will generate a self-timed pulse that will reset the board.
(There is no need for the software to return to clear this bit)
0 will not generate a self-timed pulse that will reset the board
(There is no need for the software to return to clear this bit)

D1 Enable Interrupts
1 will enable this board to generate VME interrupts.
0 will disable the board from generating VME interrupts.

D2..3 Reserved

D4 Spare LED On (A software controlled bit.)
1 will turn **off** the Fail LED
0 will turn **on** the Fail LED

D5..6 Reserved

D7 Fail LED On L (A software controlled bit.)
1 will turn **off** the Fail LED
0 will turn **on** the Fail LED.

D8..D15 Reserved

3.1.1.4 Board Status Register:

D0..D15 Reserved

3.1.2 I/O CONTROL REGISTERS:

3.1.2.1 Channel 0 Control Register: (same format for Channels 1..3 Control Registers)

D0 Reset Tx Buffer (pulsed)
1 will generate a self-timed pulse that will reset the Tx Buffer.
(There is no need for the software to return to clear this bit)

D1 Reset Rx Buffer (pulsed)
1 will generate a self-timed pulse that will reset the Rx Buffer.
(There is no need for the software to return to clear this bit)

D2 Enable interrupts for channel number.
1 will enable this board to generate interrupts for this channel number.
0 will disable the board from generating interrupts for this channel number.

D3 Reserved

D4 En Drive Lower Cable H
1 will enable this board to drive the lower cable.
0 will disable this board from driving the lower cable.

D5 En Drive Upper Cable H
1 will enable this board to drive the upper cable.
0 will disable this board from driving the upper cable.

D6 En Rx Lower Cable L
1 will enable RX to drive the lower cable.
0 will disable RX from driving the lower cable.

D7 En Rx Upper Cable L
1 will enable Rx to drive the upper cable.
0 will disable Rx from driving the upper cable.

D8..D15 Reserved

3.1.3 CHANNEL 0 FIFO: (SAME FORMAT FOR CHANNELS 1..3 FIFO)

D0..D7 Valid
D8..D15 Reserved

3.1.4 CHANNEL 0 FIFO STATUS REGISTER: (SAME FORMAT FOR CHANNELS 1..3 FIFO STATUS REGISTERS)

D0 Tx FIFO Empty L
0 indicates that the Tx FIFO is empty.
1 indicates that the Tx FIFO is not empty.

D1 Tx FIFO Almost Empty L
0 indicates that the Tx FIFO is almost empty.
1 indicates that the Tx FIFO is not almost empty.

D2 Tx FIFO Almost Full L
0 indicates that the Tx FIFO is almost full.
1 indicates that the Tx FIFO is not almost full.

D3 Tx FIFO Full L
0 indicates that the Tx FIFO Full L is full.
1 indicates that the Tx FIFO Full L is not full.

D4 Rx FIFO Empty L
0 indicates that the Rx FIFO is empty.
1 indicates that the Rx FIFO is not empty.

D5 Rx FIFO Almost Empty L
0 indicates that the Rx FIFO is almost empty.
1 indicates that the Rx FIFO is not almost empty.

D6 Rx FIFO Almost Full L
0 indicates that the Rx FIFO is almost full.
1 indicates that the Rx FIFO is not almost full.

D7 Rx FIFO Full L
0 indicates that the Rx FIFO is full.
1 indicates that the Rx FIFO is not full.

D8..D15 Reserved

3.1.5 INTERRUPT CONTROL/STATUS REGISTERS:

3.1.5.1 Interrupt Control Register

D0 Enable Channel 0 Sync Detected
1 will enable this board to generate an interrupt when a sync word is detected.
0 will disable this board from generating an interrupt when a sync word is detected.

D1 Enable Channel 0 Tx FIFO Empty Interrupt
1 will enable this board to generate an interrupt when the Tx FIFO is empty.
0 will disable this board from generating an interrupt when the Tx FIFO is empty.

D2 Enable Channel 1 Sync Detected
1 will enable this board to generate an interrupt when a Sync word is detected
0 will disable this board from generating an interrupt when a Sync word is detected.

D3 Enable Channel 1 Tx FIFO Empty Interrupt
1 will enable this board to generate an interrupt when the Tx FIFO is empty.
0 will disable this board from generating an interrupt when the Tx FIFO is empty.

D4 Enable Channel 2 Tx Sync Detected
1 will enable this board to generate an interrupt when a Tx Sync word is detected.
0 will disable this board from generating an interrupt when a Tx Sync word is detected.

D5 Enable Channel 2 Tx FIFO Empty Interrupt
1 will enable this board to generate an interrupt when the Tx FIFO is empty.
0 will disable this board from generating an interrupt when the Tx FIFO is empty.

D6 Enable Channel 3 Tx Sync Detected
1 will enable this board to generate an interrupt when a Tx Sync word is detected.
0 will disable this board from generating an interrupt when a Tx Sync word is detected.

D7 Enable Channel 3 Tx FIFO Empty Interrupt
1 will enable this board to generate an interrupt when the Tx FIFO is empty.
0 will disable this board from generating an interrupt when the Tx FIFO is empty.

D8 Enable Channel 0 Rx FIFO Not Empty Interrupt
1 will enable this board to generate an interrupt when the Rx FIFO is not empty.
0 will disable this board from generating an interrupt when the Rx FIFO is not empty.

D9 Enable Channel 0 Rx FIFO Almost Full Interrupt
1 will enable this board to generate an interrupt when the Rx FIFO is full.
0 will disable this board from generating an interrupt when the Rx FIFO is full.

D10 Enable Channel 1 Rx FIFO Not Empty Interrupt
1 will enable this board to generate an interrupt when Rx FIFO is not empty.
0 will disable this board from generating an interrupt when Rx FIFO is not empty.

D11 Enable Channel 1 Rx FIFO Almost Full Interrupt
1 will enable this board to generate an interrupt when the Rx FIFO is almost full.
0 will disable this board from generating an interrupt when the Rx FIFO is almost full.

D12 Enable Channel 2 Rx FIFO Not Empty Interrupt

1 will enable this board to generate an interrupt when the Rx FIFO is not empty.
0 will disable this board from generating an Interrupt when the Rx FIFO is not empty.

D13 Enable Channel 2 Rx FIFO Almost Full Interrupt
1 will enable this board to generate an interrupt when the Rx FIFO is almost full.
0 will disable this board from generating an interrupt when the Rx FIFO is almost full.

D14 Enable Channel 3 Rx FIFO Not Empty Interrupt
1 will enable this board to generate an interrupt when the Rx FIFO is not empty.
0 will disable this board from generating an interrupt when the Rx FIFO is not empty.

D15 Enable Channel 3 Rx FIFO Almost Full Interrupt
1 will enable this board to generate an interrupt when the Rx FIFO is almost full.
0 will disable this board from generating an interrupt when the Rx FIFO is almost full.

3.1.5.2 Interrupt Status Register (Dual Purpose Bits): (ICR - Interrupt Control Register)

D0 Channel 0 Tx FIFO Sync Detected
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being not true the source of the interrupt is not present.

D1 Channel 0 Tx FIFO Empty Interrupt
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

D2 Channel 1 Tx FIFO Sync Detected
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

D3 Channel 1 Tx FIFO Empty Interrupt
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

D4 Channel 2 Sync Detected
If this interrupt is enabled:
1 indicates an interrupt has occurred.

0 indicates an interrupt has not occurred.

If this interrupt is not enabled:

0 indicates the current status of this interrupt source.

1 being the source of the interrupt is present.

0 being the source of the interrupt is not present.

D5 Channel 2 Tx FIFO Empty Interrupt

If this interrupt is enabled:

1 indicates an interrupt has occurred.

0 indicates an interrupt has not occurred.

If this interrupt is not enabled:

0 indicates the current status of this interrupt source.

1 being the source of the interrupt is present.

0 being the source of the interrupt is not present.

D6 Channel 3 Sync Detected

If this interrupt is enabled:

1 indicates an interrupt has occurred.

0 indicates an interrupt has not occurred.

If this interrupt is not enabled:

0 indicates the current status of this interrupt source.

1 being the source of the interrupt is present.

0 being the source of the interrupt is not present.

D7 Channel 3 Tx FIFO Empty Interrupt

If this interrupt is enabled:

1 indicates an interrupt has occurred.

0 indicates an interrupt has not occurred.

If this interrupt is not enabled:

0 indicates the current status of this interrupt source.

1 being the source of the interrupt is present.

0 being the source of the interrupt is not present.

D8 Channel 0 Rx FIFO Not Empty Interrupt

If this interrupt is enabled:

1 indicates an interrupt has occurred.

0 indicates an interrupt has not occurred.

If this interrupt is not enabled:

0 indicates the current status of this interrupt source.

1 being the source of the interrupt is present.

0 being the source of the interrupt is not present.

D9 Channel 0 Rx FIFO Almost Full Interrupt

If this interrupt is enabled:

1 indicates an interrupt has occurred.

0 indicates an interrupt has not occurred.

If this interrupt is not enabled:

0 indicates the current status of this interrupt source.

1 being the source of the interrupt is present.

0 being the source of the interrupt is not present.

D10 Channel 1 Rx FIFO Not Empty Interrupt

If this interrupt is enabled:

1 indicates an interrupt has occurred.

0 indicates an interrupt has not occurred.

If this interrupt is not enabled:

0 indicates the current status of this interrupt source.

1 being the source of the interrupt is present.

0 being the source of the interrupt is not present.

D11 Channel 1 Rx FIFO Almost Full Interrupt

If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

D12 Channel 2 Tx FIFO Not Empty Interrupt
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

D13 Channel 2 Rx FIFO Almost Full Interrupt
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

D14 Channel 3 Rx FIFO Not Empty Interrupt
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

D15 Channel 3 Rx FIFO Full Interrupt
If this interrupt is enabled:
1 indicates an interrupt has occurred.
0 indicates an interrupt has not occurred.
If this interrupt is not enabled:
0 indicates the current status of this interrupt source.
1 being the source of the interrupt is present.
0 being the source of the interrupt is not present.

3.1.5.3 Interrupt Vector Register

This is a hardware modifiable Interrupt Vector Register, to indicate the source of the interrupt, encoding is as follows D0 being the LSB:

D0..D2 Hardware Encoded

000	Enable Channel 0 Sync Detected
	Enable Channel 0 Tx FIFO Empty Interrupt
001	Enable Channel 1 Sync Detected
	Enable Channel 1 Tx FIFO Empty Interrupt
010	Enable Channel 2 Sync Detected
	Enable Channel 2 Tx FIFO Empty Interrupt
011	Enable Channel 3 Sync Detected
	Enable Channel 3 Tx FIFO Empty Interrupt
100	Enable Channel 0 Rx FIFO Not Empty Interrupt
	Enable Channel 0 Rx FIFO Almost Full Interrupt
101	Enable Channel 1 Rx FIFO Not Empty Interrupt
	Enable Channel 1 Rx FIFO Almost Full Interrupt
110	Enable Channel 2 Rx FIFO Not Empty Interrupt
	Enable Channel 2 Rx FIFO Almost Full Interrupt
111	Enable Channel 3 Rx FIFO Not Empty Interrupt
	Enable Channel 3 Rx FIFO Almost Full Interrupt

D3..D7 Software Selectable
D8..D15 Reserved

3.1.5 SERIAL CONTROLLER REGISTERS

(Contact your local Zilog Represenative for Data books and User manuals in reference to the Z16C30, USC Universal Serial Controller, for a more detailed description of the following registers, see also Related Publications section of this document.

3.1.6.1 CHANNEL COMMAND/ADDRESS REGISTER (ADDRESS: 00000)

(same format for Channels 1..3 USC Control Registers)

3.1.6.1.1 Low WO: (Offset Address: 0x00)

D0 WO	Upper/Lower Byte Select (Always set to *Lower* for proper operation of this board)
D1..D5 WO	Address 0 . .4
D6 WO	Byte/Word Access (Always set to *Byte* for proper operation of this board)
D7 WO	DMA Continue

3.1.6.1.2 High WO: (Offset Address: 0x02)

Mode Control

D0 WO 0 Normal Operation
1 Auto Echo
0 External Local Loop-back
1 Internal Local Loop-back
D1 WO 0 Normal Operation
0 Auto Echo
1 External Local Loop-back
1 Internal Local Loop-back

D2 WO Channel Reset

Channel Command WO

D7	D6	D5	D4	D3	Bit Map
0	0	0	0	0	Null Command
0	0	0	0	1	Reserved
0	0	0	1	0	Reset Highest IUS
0	0	0	1	1	Reserved
0	0	1	0	0	Trigger Channel Load DMA
0	0	1	0	1	Trigger Rx DMA
0	0	1	1	0	Trigger Tx DMA
0	0	1	1	1	Trigger Rx & Tx DMA
0	1	0	0	0	Reserved
0	1	0	0	1	Rx FIFO Purge
0	1	0	1	0	Tx FIFO Purge
0	1	0	1	1	Rx & Tx FIFO Purge
0	1	1	0	0	Reserved
0	1	1	0	1	Load Rx Character Count
0	1	1	1	0	Load Tx Character Count
0	1	1	1	1	Load RX & Tx Character Count
1	0	0	0	0	Reserved
1	0	0	0	1	Load TCO
1	0	0	1	0	Load TC1
1	0	0	1	1	Load TC0 & TC1
1	0	1	0	0	Select Serial Data LSB First *
1	0	1	0	1	Select Serial Data MSB First
1	0	1	1	0	Select Straight Memory Data *
1	0	1	1	1	Select Swapped Memory Data
1	1	0	0	0	Reserved
1	1	0	0	1	Rx Purge
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	1	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

*****Selected upon reset

3.1.6.2 CHANNEL MODE REGISTER (ADDRESS: 00001)

3.1.6.2.1Low: (Offset Address: 0x04)

Receiver Mode

D3 RW	D2 RW	D1 RW	D0 RW	Bit Map
0	0	0	0	Asynchronous
0	0	0	1	External Synchronous
0	0	1	0	Isochronous
0	0	1	1	Asynchronous with CV
0	1	0	0	Monosync
0	1	0	1	Bisync
0	1	1	0	HDLC
0	1	1	1	Transparent Bisync
1	0	0	0	NBIP
1	0	0	1	802.3
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

Rx Submode

D7 RW	D6 RW	D5 RW	D4 RW
3	2	1	0

3.1.6.2.2High: (Offset Address: 0x06)

Transmitter Mode

D3 RW	D2 RW	D1 RW	D0 RW	Bit Map
0	0	0	0	Asynchronous
0	0	0	1	Reserved
0	0	1	0	Isochronous
0	0	1	1	Asynchronous with CV
0	1	0	0	Monosync
0	1	0	1	Bisync
0	1	1	0	HDLC
0	1	1	1	Transparent Bisync
1	0	0	0	NBIP
1	0	0	1	802.3
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Slaved Monosync
1	1	0	1	Reserved
1	1	1	0	HDLC Loop
1	1	1	1	Reserved

Tx Submode

D7 RW	D6 RW	D5 RW	D4 RW
3	2	1	0

3.1.6.3 CHANNEL COMMAND/STATUS REGISTER (ADDRESS: 00010)

3.1.6.3.1 Low: (Offset Address: 0x08)

D5 RW	Reserved
D6 RO	Loop Sending
D7 RO	On Loop

HDLC Tx Last Character Length

D4 RW	D3 RW	D2 RW	Bit Map
1	1	1	7 Bits
1	1	0	6 Bits
1	0	1	5 Bits
1	0	0	4 Bits
0	1	1	3 Bits
0	1	0	2 Bits
0	0	1	1 Bit
0	0	0	0 Bits

D0 RO Tx ACK
D1 RO Rx ACK

3.1.6.3.2 High: (Offset Address: 0x0A)

D2 RW Clocks Missed Latched/Unlatch
D3 RW Clocks Missed Latched/Unlatch
D4 RW DPLL in Sync/Quick Sync
D5 WO RCC FIFO Clear
D6 RO RCC FIFO Valid
D7 RO RCC FIFO Overflow

DLL Adjust/Sync Edge

D1 RW	D0 RW	Bit Map
0	0	Both Edges
0	1	Rising Edge Only
1	1	Falling Edge Only
1	1	Adjust/Sync Inhibit

3.1.6.4 CHANNEL CONTROL REGISTER (ADDRESS: 00011)

3.1.6.4.1 Low: (Offset Address: 0x0C)

Rx Status Block Transfer

D7 RW	D6 RW	Bit Map
0	0	No Status Block
0	1	One Word Status Block
1	0	Two Word Status Block
1	1	Reserved

D5 RW Wait for Rx DMA Trigger
D0..4 RW Reserved

3.1.6.4.2 High: Address: 00011

Tx Status Block Transfer (Offset Address: 0x0E)

D7 RW	D6 RW	Bit Map
0	0	No Status Block
0	1	One Word Status Block
1	0	Two Word Status Block
1	1	Reserved

D4 RW Tx Flag Preamble
D5 RW Wait for Tx DMA Trigger

Tx Preamble Length

D3 RW	D2 RW	Bit Map
0	0	8 Bits
0	1	16 Bits
1	0	32 Bits
1	1	64 Bits

Tx Preamble Pattern (All Sync)

D1 RW	D2 RW	All Zeros
0	0	All Zeros
0	1	All Ones
1	0	Alternating 1 & 0
1	1	Alternating 0 & 1

D3 RW..D0 RW Tx Shaved Bit Length (Async Only)

3.1.6.5 PRIMARY RESERVED REGISTER (ADDRESS: 00100)

3.1.6.5.1 Low: (Offset Address: 0x10)

D0..D7 RW Reserved

3.1.6.5.2 High: (Offset Address: 0x12)

D0..D7 RW Reserved

3.1.6.6 SECONDARY RESERVED REGISTER (ADDRESS: 00101)

3.1.6.6.1 Low: (Offset Address: 0x14)

D0..D7 RW Reserved

3.1.6.6.2 High: (Offset Address: 0x16)

D0..D7 RW Reserved

3.1.6.7 TEST MODE DATA REGISTER (ADDRESS: 00110)

3.1.6.7.1 Low: (Offset Address: 0x18)

D0..D7 RW Test Data 0 . .7

3.1.6.7.2 High: (Offset Address: 0x1A)

D0..D7 RW Test Data 0 . .7

3.1.6.8 TEST MODE CONTROL REGISTER (ADDRESS: 00111)

3.1.6.8.1 Low: (Offset Address: 0x1C)

Test Register Address

D4 RW	D3 RW	D2 RW	D1 RW	D0 RW	Bit Map
0	0	0	0	0	Null Address
0	0	0	0	1	High Byte of Shifters
0	0	0	1	0	CRC Byte 0
0	0	0	1	1	CRC Byte 1
0	0	1	0	0	Rx FIFO (Write)
0	0	1	0	1	Clock Multiplexer Outputs
0	0	1	1	0	CTR0 and CTR1 Counters
0	0	1	1	1	Clock Multiplexer Inputs
0	1	0	0	0	DPLL State
0	1	0	0	1	Low Byte of Shifters
0	1	0	1	0	CRC Byte 2
0	1	0	1	1	CRC Byte 3
0	1	1	0	0	Tx FIFO (Read)
0	1	1	0	1	Reserved
0	1	1	1	0	I/O and Device Status Latches
0	1	1	1	1	Internal Daisy Chain
1	0	0	0	0	Reserved
1	0	0	0	1	Reserved
1	0	0	1	0	Reserved
1	0	0	1	1	Reserved
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved

1	0	1	1	1	Reserved
1	1	0	0	0	4044H
1	1	0	0	1	4044H
1	1	0	1	0	4044H
1	1	0	1	1	4044H
1	1	1	0	0	4044H
1	1	1	0	1	4044H
1	1	1	1	0	4044H
1	1	1	1	1	4044H

D5..D7 RW Reserved

3.1.6.8.2 High: (Offset Address: 0x1E)

D0..D7 RW Reserved

3.1.6.9 CLOCK MODE CONTROL REGISTER (ADDRESS: 01000)

3.1.6.9.1 Low: (Offset Address: 0x20)

Receive Clock Source

D2 RW	D1 RW	D0 RW	Bit Map
0	0	0	Disabled
0	0	1	/RxC Pin
0	1	0	/TxC Pin
0	1	1	DPLL Output
1	0	0	BRG0 Output
1	0	1	BRG1 Output
1	1	0	CTR0 Output
1	1	1	CTR1 Output

Transmit Clock Source

D5 RW	D4 RW	D3 RW	Bit Map
0	0	0	Disabled
0	0	1	/RxC Pin
0	1	0	/TxC Pin
0	1	1	DPLL Output
1	0	0	BRG0 Output
1	0	1	BRG1 Output
1	1	0	CTR0 Output
1	1	1	CTR1 Output

DPLL Clock Source

D7 RW	D6 RW	Bit Map
0	0	BRG0 Output
0	1	BRG1 Output
1	0	/RxC Pin
1	1	/TxC Pin

3.1.6.9.2 High: (Offset Address: 0x22)

BRG0 Clock Source

D1 RW	D0 RW	Bit Map
0	0	CTR0 Output
0	1	CTR1 Output
1	0	/RxC Pin
1	1	/TxC Pin

BRG1 Clock Source

D3 RW	D2 RW	Bit Map
0	0	CTR0 Output
0	1	CTR1 Output
1	0	/RxC Pin
1	1	/TxC Pin

CRT0 Clock Source

D5 RW	D4 RW	Description
0	0	BRG0 Output
0	1	BRG1 Output
1	0	/RxC Pin
1	1	/TxC Pin

CTR1 Clock Source

D7 RW	D6 RW	Description
0	0	Disabled
0	1	Disabled
1	0	/RxC Pin
1	1	/TxC Pin

3.1.6.10 HARDWARE CONFIGURATION REGISTER (ADDRESS: 01001)

3.1.6.10.1 Low: (Offset Address: 0x24)

D1 RW BRG0 Single Cycle/Continuous
D0 RW BRG0 Enable

Rx ACK Pin Control

D3 RW	D2 RW	Bit Map
0	0	3 - State Output
0	1	Rx Acknowledge Input
1	0	Output 0
1	1	Output 1

D5 RW BRG1 Enable
D4 RW BRG1 Single Cycle/Continuous

Tx ACK Pin Control

D7 RW	D6 RW	Bit Map
0	0	3 - State Output
0	1	Tx Acknowledge Input
1	0	Output 0
1	1	Output 1

3.1.6.10.2 High: (Offset Address: 0x26)

DPLL Mode

D1 RW	D0 RW	Bit Map
0	0	Disabled
0	1	NRZ/NRZI
1	0	Biphase-Mark/Space
1	1	Biphase-Level

PLL Clock Rate

RW	D2 RW	Bit Map
0	0	32x Clock Mode
0	1	16x Clock Mode
1	0	8x Clock Mode
1	1	Reserved

D5 RW	Accept Code Violations
D4 RW	CTR1 Rate Match DPLL/CTR0

CTR0 Clock Rate

D7 RW	D6 RW	Bit Map
0	0	32x Clock Mode
0	1	16x Clock Mode
1	0	8x Clock Mode
1	1	4x Clock Mode

3.1.6.11 INTERRUPT VECTOR REGISTER (ADDRESS: 01010)

3.1.6.11.1 Low: (Offset Address: 0x28)

D7..D0 RW IV 0..7

3.1.6.11.2 High: (Offset Address: 0x2A)

D0 RO IV 0

Modified Vector

D3 RO	D2 RO	D1 RO	Bit Map
0	0	0	None
0	0	1	Device Status
0	1	0	I/O Status
0	1	1	Transmit Data
1	0	0	Transmit Status
1	0	1	Receive Data
1	1	0	Receive Status
1	1	1	Not Used

D4..D7 IV (4..7)

3.1.6.12 I/O CONTROL REGISTER (ADDRESS: 01011)

3.1.6.12.1 Low: (Offset Address: 0x2C)

RxC Pin Control

D2 RW	D1 RW	D0 RW	Bit Map
0	0	0	Input Pin
0	0	1	Rx Clock Output
0	1	0	Rx Byte Clock Output
0	1	1	SYNC Output
1	0	0	BRG0 Output
1	0	1	BRG1 Output
1	1	0	CTR0 Output
1	1	1	DPLL Rx Output

TxC Pin Control

D5 RW	D4 RW	D3 RW	Bit Map
0	0	0	Input Pin
0	0	1	Tx Clock Output
0	1	0	Tx Byte Clock Output
0	1	1	Tx Complete Output
1	0	0	BRG0 Output
1	0	1	BRG1 Output
1	1	0	CTR1 Output
1	1	1	DPLL Tx Output

TxD Pin Control

D7 RW	D6 RW	Bit Map
0	0	Tx Data Output
0	1	3-State Output
1	0	Output 0
1	1	Output 1

3.1.6.12.2 High: (Offset Address: 0x2E)

RxREQ Pin Control

D1 RW	D0 RW	Bit Map
0	0	3-State Output
0	1	Rx Request Output
1	0	Output 0
1	1	Output 1

TxREQ Pin Control

D3 RW	D2 RW	Bit Map
0	0	3-State Output
0	1	Rx Request Output
1	0	Output 0
1	1	Output 1

DCD Pin Control

D5 RW	D4 RW	Bit Map
0	0	/DCD Input
0	1	/DCD//SYNC Input
1	0	Output 0
1	1	Output 1

CTS Pin Control

D7 RW	D6 RW	Bit Map
0	0	/CTS Input
0	1	/CTS Input
1	0	Output 0
1	1	Output 1

3.1.6.13 INTERRUPT CONTROL REGISTER (ADDRESS: 01100)

3.1.6.13.1 Low: (Offset Address: 0x30)

D0 RW Device Status IE
D1 RW I/O Status IE
D2 RW Transmit Data IE
D3 RW Transmit Status IE
D4 RW Receive Data IE
D5 RW Receive Status IE
IE Command

D7 WO	D6 WO	Bit Map

0	0	Null Command
0	1	Null Command
1	0	Reset IE
1	1	Set IE

3.1.6.13.2 High: (Offset Address: 0x32)

D0 RW Reserved

VIS Level

D3 RW	D2 RW	D1 RW	Bit Map
0	0	0	All
0	0	1	All
0	1	0	I/O Status and Above
0	1	1	Transmit Data and Above
1	0	0	Transmit Status and Above
1	0	1	Receive Data and Above
1	1	0	Receive Status Only
1	1	1	None

D7 RW MIE
D6 RW DLC
D5 RW NV
D4 RW VIS

3.1.6.14 DAISY-CHAIN CONTROL REGISTER (ADDRESS: 01101)

3.1.6.14.1 Low: (Offset Address: 0x34)

D0 RW Device Status IP
D1 RW I/O Status IP
D2 RW Transmit Data IP
D3 RW Transmit Status IP
D4 RW Receive Data IP
D5 RW Receive Status IP

IP Command

D7 WO	D6 WO	Bit Map
0	0	Null Command
0	1	Reset IP and IUS
1	0	Reset IP
1	1	Set IP

3.1.6.14.2 High RW: (Offset Address: 0x36)

D0 RW Device Status IUS
D1 RW I/O Status IUS
D2 RW Transmit Data IUS
D3 RW Transmit Status IUS

D4 RW Receive Data IUS
D5 RW Receive Status IUS

IUS Command

D7 WO	D6 WO	Bit Map
0	0	Null Command
0	1	Null Command
1	0	Reset IUS
1	1	Set IUS

3.1.6.15 MISC. INTERRUPT STATUS REGISTER (ADDRESS: 01110)

3.1.6.15.1 Low: (Offset Address: 0x38)

D0 RW BRG0 ZC Latched/Unlatch
D1 RW BRG1 ZC Latched/Unlatch
D2 RW DPLL SYNC Latched/Unlatch
D3 RW RCC Overflow Latched/Unlatch
D4 RO /CTS
D5 RW /CTS Latched/Unlatch
D6 RO /DCD
D7 RW /DCD Latched/Unlatch

3.1.6.15.2 High: (Offset Address: 0x3A)

D0 RO TxREQ
D1 RW /TxREQ Latched/Unlatch
D2 RO /RxREQ
D3 RW /RxREQ Latched/Unlatch
D4 RO /TxC
D5 RW /TxC Latched/Unlatch
D6 RO /RxC
D7 RW /RxC Latched/Unlatch

3.1.6.16 STATUS INTERRUPT CONTROL REGISTER (ADDRESS: 01111)

3.1.6.16.1 Low: (Offset Address: 0x3C)

D0 RW BRG0 ZC IE
D1 RW BRG1 ZC IE
D2 RW DPLL SYNC IE
D3 RW RCC Overflow IE
D4 RW /CTS Interrupts
D5 RW /CTS Interrupts
D6 RW /DCD Interrupts
D7 RW /DCD Interrupts

3.1.6.16.2 High: (Offset Address: 0x3E65)

D0 RW /TxREQ Interrupts
D1 RW TxREQ Interrupts
D2 RW RxREQ Interrupts
D3 RW RxREQ Interrupts

D4 RW TxC Interrupts
D5 RW TxC Interrupts
D6 RW RxC Interrupts
D7 RW RxC Interrupts

3.1.6.17 TX/RX DATA REGISTER (ADDRESS: 1X000)

3.1.6.17.1 Low: (Offset Address: 0x40)

D0..7 RW - Tx/Rx Data 0..7

3.1.6.17.2 High: (Offset Address: 0x42)

D0..7 RW - Tx/Rx Data 8..15

3.1.6.18 RECEIVER MODE REGISTER (ADDRESS: 10001)

3.1.6.18.1 Low: (Offset Address: 0x44)

Rx Enable

D1 RW	D0 RW	Bit Map
0	0	Disable Immediately
0	1	Disable After Reception
1	0	Enable Without Auto-Enables
1	1	Enable With Auto-Enables

Rx Character Length

D4 RW	D3 RW	D2 RW	Bits
0	0	0	8
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	0	5
1	1	0	6
1	1	0	7

D5 RW Rx Parity Enable

Rx Parity Sense

D7 RW	D6 RW	Bit Map
0	0	Even
0	1	Odd
1	0	Space
1	1	Mark

3.1.6.18.2 High: (Offset Address: 0x46)

D0 RW Queue Abort
D1 RW Rx CRC Enable

D2 RW Rx CRC Preset Value

Rx CRC Polynomial

D4 RW	D3 RW	Bit Map
0	0	CRC-CCITT
0	1	CRC-16
1	0	CRC-32
1	1	Reserved

Rx Data Decoding

D7 RW	D6 RW	D5 RW	Bit Map
0	0	0	NRZ
0	0	1	NRZB
0	1	0	NRZI-Mark
0	1	1	NRZI-Space
1	0	0	Biphase-Mark
1	0	1	Biphase-Space
1	1	0	Biphase-Level
1	1	1	Diff. Biphase-Level

3.1.6.19 RECEIVE COMMAND STATUS REGISTER (ADDRESS: 10010)

3.1.6.19.1 Low: (Offset Address: 0x48)

D0 RO Rx Character Available
D1 RW Rx Overrun
D2 RW Parity Error/Frame Abort
D3 RO CRC/Framing Error
D4 RW Rx CV/EOT/EOF
D5 RW Rx Break Abort
D6 RW Rx Idle
D7 RW Exited Hunt

3.1.6.19.2 High: (Offset Address: 0x4A)

D0 RO Short Frame/CV Polarity
D1 RO Residue Code 0
D2 RO Residue code 1
D3 RO Residue Code 2

Receive Command

	D4 WO	D5 WO		Bit Map
0	0	0	0	Null command
0	0	0	1	Reserved
0	0	1	0	Preset CRC
0	0	1	1	Enter Hunt Mode
0	1	0	0	Reserved
0	1	0	1	Select FIFO Status
0	1	1	0	Select FIFO Interrupt Level
0	1	1	1	Select FIFO Request Level

1	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
0	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	1	Reserved

D6 RO First Byte in Error
D7 RO Second Byte in Error

3.1.6.20 RECEIVE INTERRUPT CONTROL REGISTER (ADDRESS: 10011)

3.1.6.20.1 Low: (Offset Address: 0x4C)

D0 RW TC0R Read Count/TC
D1 RW Rx Overrun IA
D2 RW Parity Error/Frame Abort IA
D3 RW Status on Words
D4 RW Rx CV/EOT/EOF IA
D5 RW Rx Break/Abort IA
D6 RW Rx Idle IA
D7 RW Exited Hunt IA

3.1.6.20.2 High: (Offset Address: 0x4E)

D0..D7 RW Rx FIFO Control and Status (Fill/Interrupt/DMA Level)

3.1.6.21 RECEIVE SYNC REGISTER (ADDRESS: 10100)

3.1.6.21.1 Low: (Offset Address: 0x50)

D0..D7 RW RSYN 0..7

3.1.6.21.2 High: (Offset Address: 0x52)

D0..D7 RW RSYN 0..7

3.1.6.22 RECEIVE COUNT LIMIT REGISTER (ADDRESS: 10101)

3.1.6.22.1 Low: (Offset Address: 0x54)

D0..7 RW RCL 0..7

3.1.6.22.2 High: (Offset Address: 0x56)

D0..7 RW RCL 0..7

3.1.6.23 RECEIVE CHARACTER COUNT REGISTER (ADDRESS: 10110)

3.1.6.23.1 Low: (Offset Address: 0x58)

D0..7 RO RCC 0..7

3.1.6.23.2 High: (Offset Address: 0x5A)

D0..7 RO RCC 0..7

3.1.6.24 TIME CONSTANT 0 REGISTER (ADDRESS: 10111)

3.1.6.24.1 Low: (Offset Address: 0x5C)

D0..7 RW TC0 0..7

3.1.6.24.2 High: (Offset Address: 0x5E)

D0..7 RW TC0 0..7

3.1.6.25 TRANSMIT MODE REGISTER (ADDRESS: 11001)

3.1.6.25.1 Low: (Offset Address: 0x64)

Tx Enable

D1 RW	D0 RW	Bit Map
0	0	Disable Immediately
0	1	Disable After Transmission
1	0	Enable Without Auto-Enables
1	1	Enable With Auto-Enables

Tx Character Length

D4 RW	D3 RW	D2 RW	Bit Maps
0	0	0	8 Bits
0	0	1	1 Bit
0	1	0	2 Bits
0	1	1	3 Bits
1	0	0	4 Bits
1	0	1	5 Bits
1	1	0	6 Bits
1	1	1	7 Bits

D5 RW Tx Parity Enable

Tx Parity Sense

D7 RW	D6 RW	Bit Map
0	0	Even
0	1	Odd
1	0	Space
1	1	Mark

3.1.6.25.2 High: (Offset Address: 0x66)

D2 RW Tx CRC Preset Value
D1 RW Tx CRC Enable
D0 RW Tx CRC on EOF/EOM

Polynomial Tx CRC

D4 RW	D3 RW	Bit Map
0	0	CRC-CCITT
0	1	CRC-16
1	0	CRC-32
1	1	Reserved

Tx Data Encoding

D7 RW	D6 RW	D5 RW	Bit Map
0	0	0	NRZ
0	0	1	NRZB
0	1	0	NRZI-Mark
0	1	1	NRZI-Space
1	0	0	Biphase-Mark
1	0	1	Biphase-Space
1	1	0	Biphase-Level
1	1	1	Diff. Biphase-Level

3.1.6.26 TRANSMIT COMMAND/STATUS REGISTER (ADDRESS: 11010)

3.1.6.26.1 Low: (Offset Address: 0x68)

D0 RO Tx Buffer Empty
D1 RW Tx Underrun
D2 RO All Sent
D3 RW Tx CRC Sent
D4 RW Tx EOF/EOT Sent
D5 RW Tx Abort Sent
D6 RW Tx Idle Sent
D7 RW Tx Preamble Sent

3.1.6.26.2 High: (Offset Address: 0x6A)

Tx Idle Line Condition

D2 RW	D1 RW	D0 RW	Bit Map
0	0	0	SYNC/Flag/Normal
0	0	1	Alternating 1 & 0
0	1	0	All Zeros
0	1	1	All Ones
1	0	0	Reserved
1	0	1	Alternating Mark & Space
1	1	0	Space
1	1	1	Mark

D3 RW Tx Wait on Underrun

Transmit Command

D7 WO	D6 WO	D5 WO	D4 WO	Bit Map
0	0	0	0	Null Command
0	0	0	1	Reserved
0	0	1	0	Preset CRC
0	0	1	1	Reserved
0	1	0	0	Reserved
0	1	0	1	Select FIFO Status
1	1	1	0	Select FIFO Interrupt Level
0	1	1	1	Select FIFO Request Level
1	0	0	0	Send Frame/Message
1	0	0	1	Send Abort
1	0	1	0	Reserved
1	0	1	1	Reserved
1	1	0	0	Reset DLE Inhibit
1	1	0	1	Set DLE Inhibit
1	1	1	0	Reset EOF/EOM
1	1	1	1	Set EOF/EOM

3.1.6.27 TRANSMIT INTERRUPT CONTROL REGISTER (ADDRESS: 11011)

3.1.6.27.1 Low: (Offset Address: 0x6C)

D0 RW TC1R Read Count/TC
D1 RW Tx Overrun IA
D2 RW Wait for Send Command
D3 RW Tx CRC Sent IA
D4 RW Tx EOF/EOT Sent IA
D5 RW Tx Abort Sent IA
D6 RW Tx Idle Sent IA
D7 RW Tx Preamble Sent IA

3.1.6.27.2 High: (Offset Address: 0x6E)

D0..7 RW Tx FIFO Control and Status (Fill/Interrupt/DMA Level)

3.1.6.28 TRANSMIT SYNC REGISTER (ADDRESS: 11100)

3.1.6.28.1 Low: (Offset Address: 0x70)

D0..7 RW TSYN 0..7

3.1.6.28.2 High: (Offset Address: 0x72)

D0..7 RW TSYN 0..7

3.1.6.29 TRANSMIT COUNT LIMIT REGISTER (ADDRESS: 11101)

3.1.6.29.1 Low: (Offset Address: 0x74)

D0..7 RW TCL 0..7

3.1.6.29.2 High: (Offset Address: 0x76)

D0..7 RW TCL 0..7

3.1.6.30 TRANSMIT CHARACTER COUNT REGISTER (ADDRESS: 11110)

3.1.6.30.1 Low: (Offset Address: 0x78)

D0..7 RO TCC 0..7

3.1.6.30.2 High: (Offset Address: 0x7A)

D0..7 RO TCC 0..7

3.1.6.31 TIME CONSTANT 1 REGISTER (ADDRESS: 11111)

3.1.6.31.1 Low: (Offset Address: 0x7C)

D0..7 RW TC1 0..7

3.1.6.31.2 High: (Offset Address: 0x7E)

D0..7 RW TC1 0..7

CHAPTER 4: HARDWARE CONFIGURATION

4.0 THE ON-BOARD TRANSMIT/RECEIVE CLOCK

The on-board oscillator, U28, is used for generating a transmit receive clock as well as the on-board clock for the Zilogs. It is factory installed at 20.0 MHz and may be changed to accommodate a wide range of baud rates. The desired baud rate is determined by the equation:

(Baud rate) (Time Constant + 1) = Oscillator frequency of U28

Using the factory installed 20.0 megahertz oscillator frequency of U28, the following time constants will give the following baud rates:

Time Constants	**Baud Rates**
64	307.2K
256	76.8K
512	38.4K
2048	9.6K

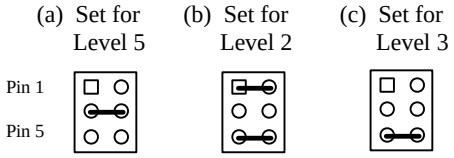
Any standard dip oscillator, 8 pin or 14 pin, will fit into the socket of U28, thereby changing the on-board transmit receive clock.

4.1 IRQ LEVEL SELECT JUMPERS (J6)

These jumpers are used to select or determine the interrupt request level used by this board.

They use a binary encoded method with jumpers for pins 1 and 2 being the LSB of a 3-bit value. If none of the jumpers are in, this is a level select of the lowest priority (7). If all the jumpers are installed, this is a level select of 0 and invalid level select.

Examples of different level select configurations are as follows:

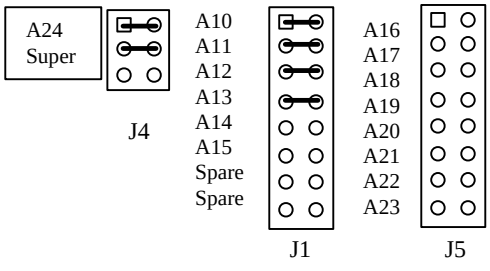


4.2 BASE ADDRESS JUMPERS (J1, J4, J5)

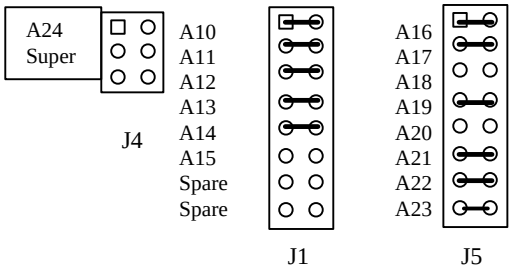
Base address selection involves 3 sets of jumpers. They are J1, J4, and J5. J4 is used to select A16 or A24 space and supervisory or non-supervisory accesses. The jumper for pins 1 and 2 is not installed for address space A24 and is installed for address space A16. Pins 3 and 4 of J4, is installed for non-supervisory; and not installed for supervisory.

Examples of the base address jumpers are shown below:

(a) Set for non-supervisory A16 space at a base address of 0xC000:



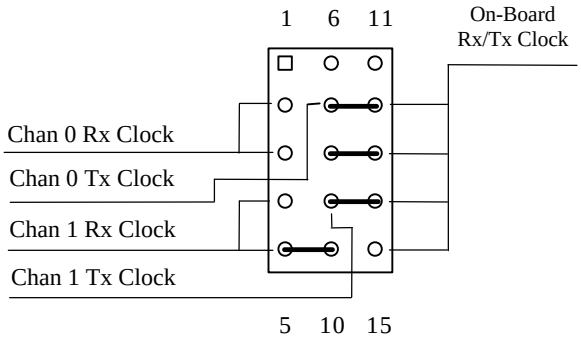
(b) Set for supervisory A24 space at a at a base address of 0x948000.



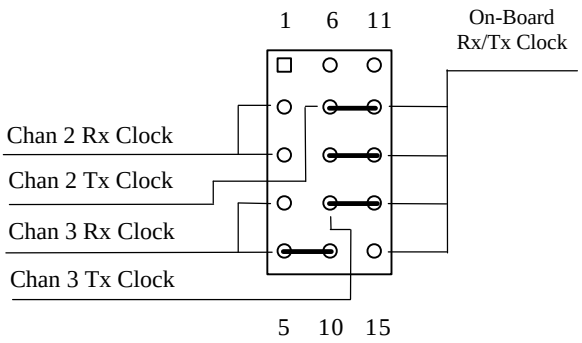
4.3 THE ZILOG CLOCK SELECT JUMPERS (J11, J14)

The purpose of these jumpers is to select where the Zilog clock comes from or goes to. If Zilog clock uses the onboard transmit/receive clock, or the cable clock, then the jumpers should be installed. If the Zilog is going to generate an output clock to the cable, then some of the jumpers should not be installed. The Zilog Clock Select Jumpers are shown below:

- Channel 0/2 Zilog uses the onboard OSC, U28, for Transmit and Receive.
- Channel 1/3 Zilog uses the onboard OSC for Transmit and cable Receive clock for Receive.
- Cable Transmit clock will be onboard OSC.



J11 is used for Channels 0 and 1



J14 is used for Channels 2 and 3

Description of Jumpers shown above:

- Channel 0/2 Zilog uses the on-board OSC for Rcv and will generate and output a transmit clock of a software programmed frequency.
- Channel 1/3 Zilog uses the enable Rx clock for both transmit and Rcv.
- The transmit clock will be the same as the Rcv clock.
- Channel 0/2 and 1/3 will use the cable Rcv clock for Rcv and will generate and output a transmit clock of a software programmed frequency.

4.4 THE CHANNEL PIN-OUT JUMPERS (J10, J12, J13, J15)

Jumpers J10, J12, J13, and J15 may be removed to allow wire wrapping to accommodate various pin-out configurations. It is the suggestion of GSC that any reconfiguration of the pin-out should always maintain paired signals on the cable, i.e., the "+" signals should travel beside or be twisted with the "-" signal.

If the jumpers are installed in the factory configuration, then the following pin-outs will apply:

Table 4.4-1 Pin-Out for User Connectors (P3 Channel 0, P4 Channel 1, P5 Channel 2, P6 Channel 3)

Jumper Pin #	Signal Name	Connector Pin #
1-2	**LWR Cable TxD/RxD +**	**3**
3-4	**LWR Cable TxD/RxD -**	**16**
5-6	**NC**	
7-8	**LWR Cable Cts/DCD +**	**5**
9-10	**LWR Cable Cts/DCD -**	**18**
11-12	**NC**	
13-14	**NC**	
15-16	**Ground**	**7**
17-18	**Ground**	**20**
19-20	**NC**	
21-22	**NC**	
23-24	**LWR Cable Tx/Rx/CLK +**	**9**
25-26	**LWR Cable Tx/Rx/CLK -**	**22**
27-28	**UPR Cable TxD/RxD -**	**10**
29-30	**UPR Cable TxD/RxD +**	**23**
31-32	**UPR Cable CTS/DCD -**	**11**
33-34	**UPR Cable CTS/DCD +**	**24**
35-36	**UPR Cable Tx/Rx/CLK -**	**12**
37- 38	**UPR Cable Tx/Rx/CLK +**	**25**

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