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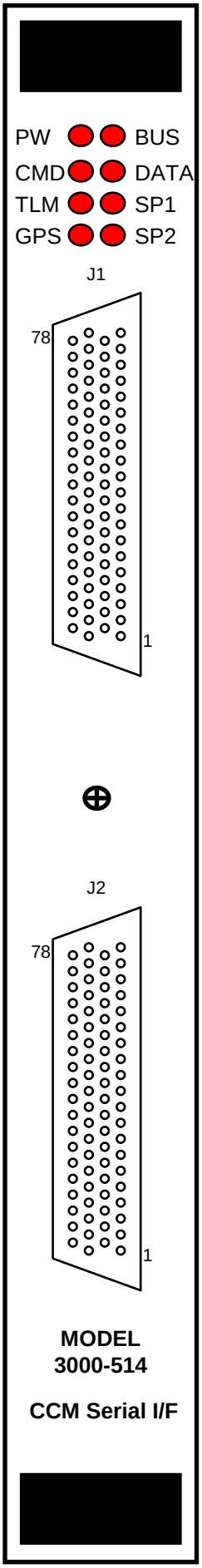
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MODEL 3000-514

CCM Serial I/F

07500830

REVISION 7

ASCOR INC.

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Introduction

This manual provides the necessary information for the operation and maintenance of the Model 3000-514 CCM Serial I/F VXI Module.

General Description

The CCM Serial I/F is a single-wide VXI Module which provides six (6) Custom Serial Interface Ports for the Command Control Module (CCM). The six 3000-514 Ports are the CMD Port, the Data Port, the TLM Port, Status Port 1, Status Port 2, and the GPS Port. Each of these Ports are individually configurable, and are electrically isolated from all others. The 3000-514 also provides full Primary and Redundant Drivers and Receivers.

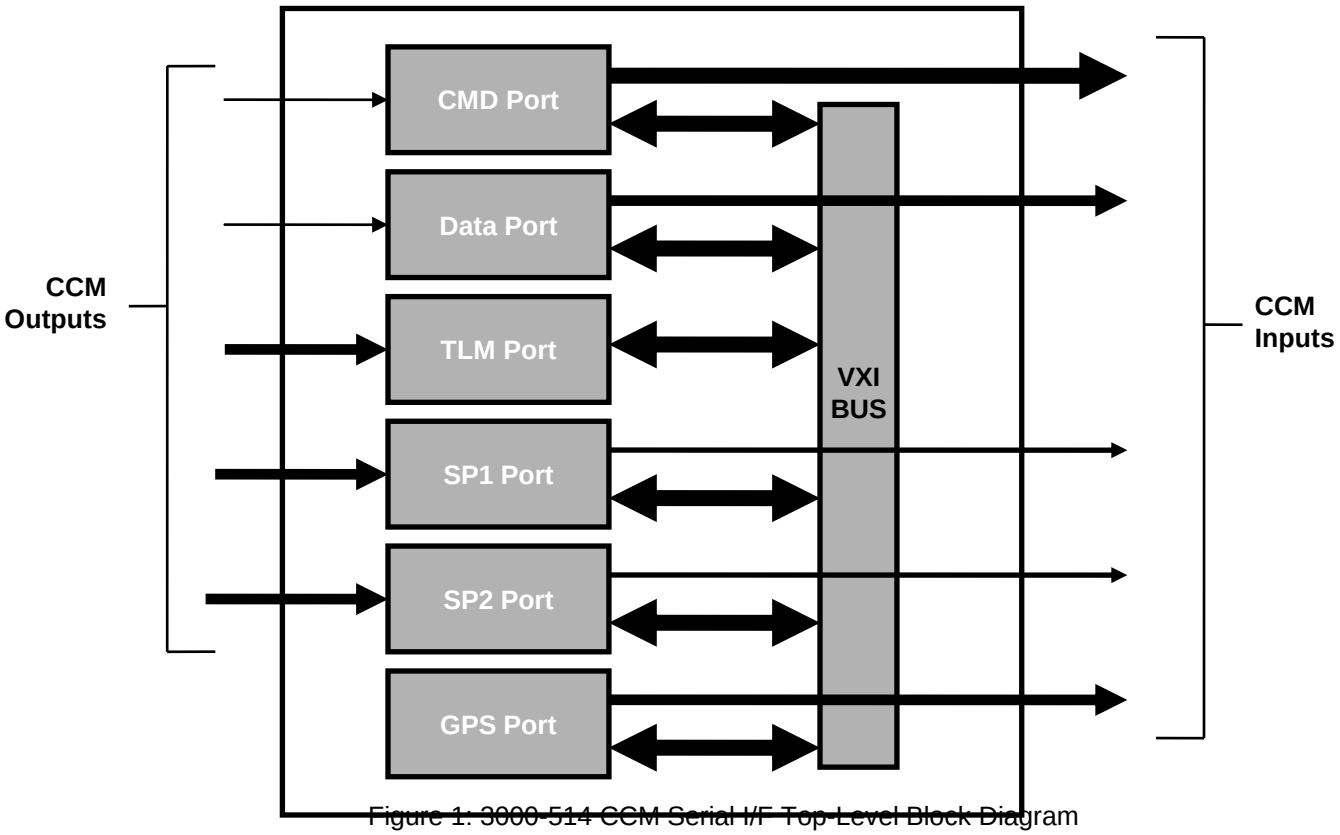


Figure 1: 3000-514 CCM Serial I/F Top-Level Block Diagram

The 3000-514 CCM Serial I/F is a single Motherboard VXI Module which provides a VXI register based interface as well as the six CCM Serial I/F Ports (85002330).

The 3000-514 is a register based device and supports VXIbus register maps. All controls to the 3000-514 are done through registers. All registers can be accessed with the use of slot 0 computers, host computers with VXI-MXI, or host computers with GPIB and GPIB-VXI slot 0 controllers. The 3000-514 CCM Serial I/F is not a message based device and does not support VXIbus communication protocols.

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General Information

- Register-based Architecture: Allows VXI bus speeds to control I/O actions, resulting in much improved operating speeds when compared to message-based modules.

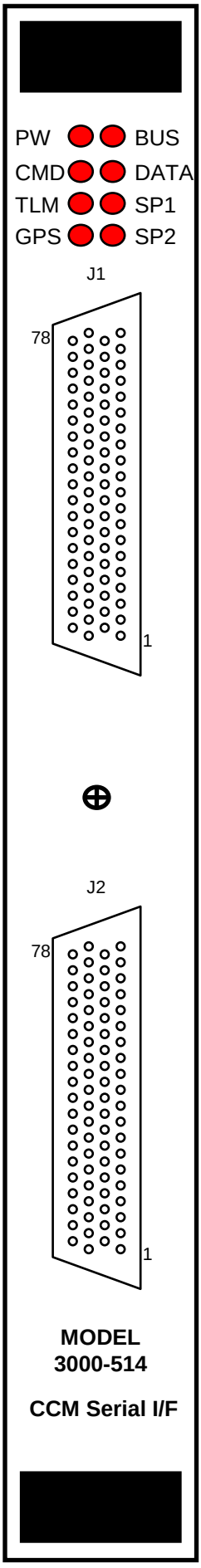
- A16/A32 Address Space: This module utilizes both the A16 and A32 Address space for mapping I/O functions. The A16 Address space contains the VXIbus configuration registers which are defined by the VXIbus specification for all VXIbus devices. The A32 Address space contains the CCM Serial I/F Port Registers.

- 16/32 Data Bus operation: ASCOR's VXIMAX 16/32 VXIbus Interface allows this module to operate in either 16-bit or 32-bit data bus modes. The A16 Address Space is addressed in 16-bit mode only. The A32 Address Space is addressed in 32-bit mode only.

- Static and Dynamic Configuration: The 3000-514 supports both Static Configuration and Dynamic Configuration of the Logical Address. In Static Configuration mode the Logical Address of the Module is manually set, and cannot be changed by the Resource Manager. In Dynamic Configuration mode the Logical Address is determined by the Resource Manager based on other devices in the system.

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ASCOR Model 3000-514



- **6 Custom CCM Serial I/F Ports**
- **Register-Based Architecture**
- **A16 / A32 Addressing**
- **16 / 32-Bit Data Bus Operation**
- **Static / Dynamic Logical Address Configuration**

Figure 2: 3000-514 CCM Serial I/F VXI Module

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Electrical Specifications

Power

+5V	2.70 amps (quiescent)

Driver (26LS31)

Output Voltage HIGH (V_{OH})	2.5 Vdc Minimum
Output Voltage LOW (V_{OL})	0.5 Vdc Maximum
Output Current HIGH (I_{OH})	-20 mA Maximum
Output Current LOW (I_{OL})	20 mA Maximum
Short Circuit Output Current (I_{OS})	-30 mA Minimum -150 mA Maximum (One Output only)

Receiver (26LS32)

Common Mode Input Voltage (V_{IC})	±7 Vdc Maximum
Input Threshold HIGH (V_{TH})	0.2 Vdc Maximum
Input Threshold LOW (V_{TL})	-0.2 Vdc Minimum
Input Hysteresis (V_{HYS})	50 mV Typical
Line Input Current (I_I)	1.2 mA Maximum

Single-Ended Buffer (74ABT16541)

Output Voltage HIGH (V_{OH})	2 Vdc Minimum
Output Voltage LOW (V_{OL})	0.55 Vdc Maximum
Output Current HIGH (I_{OH})	-32 mA Maximum
Output Current LOW (I_{OL})	64 mA Maximum

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Mechanical Specifications

Weight	2 lbs. 9 Oz.
Dimensions	Single-wide “C” size VXI (13.4” x 9.2”)
Connectors	
J1, J2	78-Position, Socket, Right angle, High Density D Connector, w/Female Screw-Locks, AMP HDP-22 Series #748483-6.
Mating Connector	78-Position, Pin, High Density D Cable Connector, AMP HDP-22 Series #748368-1. 28-22AWG, Crimp, Snap-in, Gold (30), Contact, AMP HDP Series #748333-4 Plug, Shell Size 5, Full Metal Shell, Shielding Hardware Enclosure Kit, w/Jackscrews, AMP HDP-22 Series #748477-1. .422-.490 Cable Diameter, Stepped Ferrule, Full Metal Shell, AMP HDP-22 Series #747580-5.
Installation Kit:	Installation Kit, 89800400, Available on request (Optional). Includes a full complement of mating connectors, contacts, Backshells, and ferrules.

Environmental Specifications

Temperature	
Operating	0°C to 55°C
Storage	-40°C to 75°C
Relative Humidity	
Operating	10 to 90% non-condensing
Storage	0 to 95% non-condensing
Altitude	
Operating	Less than 6,000 ft.
Cooling	External Cooling Air Required

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Memory Map

A16 Space

Offset (hex) This offset is added to the A16 Base Address of the module. The A16 Base Address for the 3000-514 CCM Serial I/F is equal to the VXIbus logical address assigned to the CCM Serial I/F shifted left six times and ORed with hex C000. These registers reside in the VXI Interface circuitry on the Motherboard (85002330).

00	VXIbus ID Register
02	Device Type Register
04	VXIbus Status/Control Register
06	Offset Register
3E	ASCOR Module Control Register

A32 Space

Offset (hex) This offset is added to the A32 Base Address of the module. The A32 Base Address can be derived from the value stored in the Offset Register (A16 Address Space, 06h). Take the 16 Bits of the Offset Register and map them into the 16 Most Significant bits of the A32 Base Address. The 16 Least Significant Bits are set to zeros. These registers reside in the CCM Serial I/F circuitry on the Motherboard (85002330).

8000	CCM Serial I/F Control Register
8004	CCM Serial I/F Status Register
8008	CCM Serial I/F CMD FIFO
800C	CCM Serial I/F CMD/Data Word Delay Register
8010	CCM Serial I/F Data FIFO
8014	CCM Serial I/O TLM Shift Register
8018	CCM Serial I/F TLM Sync Word Register
801C	CCM Serial I/F TLM FIFO #1
8020	CCM Serial I/F TLM FIFO #2
8024	CCM Serial I/F TLM FIFO #3
8028	CCM Serial I/F TLM FIFO #4
802C	CCM Serial I/F Status Port 1 Register
8030	CCM Serial I/F Status Port 2 Register
8034	CCM Serial I/F GPS Clock Skew Register

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VXI Device Register Description

The ASCOR 3000-514 CCM Serial I/F Module has VXI Device Registers located in the A16 Address Space. The VXI Specification defines 32 VXI Device Registers and they are all 16 bits wide. The first 4 registers are VXI Configuration Registers. The next 12 registers are VXI Device Class Dependent Registers. The last 16 registers are VXI Device Dependent Registers.

The 3000-514 supports 5 of the 32 VXI Device Registers, four in VXI Configuration Registers and one in VXI Device Dependent Register. All other registers are not supported. Some Device Registers must be written only by a Resource Manager. Table 1 lists the VXI Device Registers.

VXI Device Registers for ASCOR 3000-514			
VXI Device Dependent Registers			
Address	Description	Read	Write
3Eh	**ASCOR Module Control Reg**	**Yes**	**Yes**
3Ch	**Register Not Used**	**-**	**-**
3Ah	**Register Not Used**	**-**	**-**
38h	**Register Not Used**	**-**	**-**
36h	**Register Not Used**	**-**	**-**
34h	**Register Not Used**	**-**	**-**
32h	**Register Not Used**	**-**	**-**
30h	**Register Not Used**	**-**	**-**
2Eh	**Register Not Used**	**-**	**-**
2Ch	**Register Not Used**	**-**	**-**
2Ah	**Register Not Used**	**-**	**-**
28h	**Register Not Used**	**-**	**-**
26h	**Register Not Used**	**-**	**-**
24h	**Register Not Used**	**-**	**-**
22h	**Register Not Used**	**-**	**-**
20h	**Register Not Used**	**-**	**-**
VXI Device Class Dependent Registers			
Address	Description	Read	Write
1Eh	**Register Not Used**	**-**	**-**
1Ch	**Register Not Used**	**-**	**-**
1Ah	**Register Not Used**	**-**	**-**
18h	**Register Not Used**	**-**	**-**
16h	**Register Not Used**	**-**	**-**
14h	**Register Not Used**	**-**	**-**
12h	**Register Not Used**	**-**	**-**
10h	**Register Not Used**	**-**	**-**
0Eh	**Register Not Used**	**-**	**-**
0Ch	**Register Not Used**	**-**	**-**
0Ah	**Register Not Used**	**-**	**-**
08h	**Register Not Used**	**-**	**-**
VXI Configuration Registers			
Address	Description	Read	Write
06h	**Offset Register**	**Yes**	**Res. Man. Only**
04h	**Status / Control Register**	**Yes**	**Yes**
02h	**Device Type Register**	**Yes**	**Res. Man. Only**
00h	**ID / Logical Address Register**	**Yes**	**Res. Man. Only**

Table 1: 3000-514 VXI Device Registers

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VXI Device Register Description (Continued)

VXI Configuration Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Device Class		Address Space		Manufacturer ID											

Offset **Description**

00h **ID Register (read) / Logical Address Register (write)**

A read of this 16-bit register provides information about the 3000-514 Module's configuration.

(Bits 15-14) Device Class: This field indicates the classification of the VXIbus device.
- 00b = Memory
- 01b = Extended
- 10b = Message Based
- 11b = Register Based (ASCOR VXI Module)

(Bits 13-12) Address Space: This field indicates the addressing mode(s) of the device's operational registers.
- 00b = A16/A24
- 01b = A16/A32
- 10b = RESERVED
- 11b = A16 Only

(Bits 11-0) Manufacturer ID: This field uniquely identifies the manufacturer of the device.
- FB5h = ASCOR

For the 3000-514 Module, the register should read back a value of DFB5h.

A write to this 16-bit register is provided for Dynamic Configuration protocol. This register should only be written to by a resource manager. ***Do not write to this register.***

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VXI Device Register Description (Continued)

VXI Configuration Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Required Memory				Model Code											

Offset Description

02h Device Type (read/write)

A read of this 16-bit register provides information about the 3000-514 Module's Device Type. This register indicates how much VMEbus memory is required by the VXI module, as well as the manufacture's unique model code.

(Bits 15-12) Required Memory: This field contains the value used for determining the A24 or A32 memory space resident on the device
7h = 64K bytes in A24 Address Space
Fh = 64K bytes in A32 Address Space

(Bits 11-0) Model Code: This field contains the manufacturer's unique module identifier.
D1Ah = The ASCOR Model Code for the 3000-514. This number is different from the ASCOR Model number.

For the 3000-514 Module, the register should read back a value of FD1Ah.

A write to this 16-bit register is provided for VXIbus definition. ***Do not write to this register.***

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VXI Device Register Description (Continued)

VXI Configuration Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A24/ A32	MODID	Device Dependent (Not used)										Ready	Passed	Dev. Dep.	

Offset Description

04h Status Register (read) / Control Register (write)

A read of this 16-bit register provides information about the 3000-514 status.

(Bit 15) A24/A32 Active: This bit indicates the accessibility of A24 or A32 registers.
1b = A24 or A32 Address Space Active
0b = A24 or A32 Address Space not Active (for A16 only devices)

(Bit 14) MODID: This bit indicates if the device is selected via the P2 MODID line.
1b = Device is not selected via the P2 MODID line. Used by the resource manager during Dynamic Configuration.

(Bits 13-4) Device Dependent (Not used)

(Bit 3) Ready: This bit indicates if the device is ready to accept operational commands.
1b = Device is ready after power-on initialization sequence

(Bit 2) Passed: This bit indicates if the power-on self test has successfully completed.
1b = Device does not support power-on self test (always pass)

(Bits 1-0) Device Dependent
00b = State of the corresponding bits of the Control register

For the 3000-514 Module, the register should read back a value of FFFCh.

A write to this 16-bit register causes specific actions to be executed.

(Bit 15) A24/A32 Enable: This bit enables or disables A24 / A32 VMEbus registers.
1b = Enables A24 or A32 VMEbus registers. This bit must always remain a one after being set to one by the resource manager.
0b = Disables A24 or A32 VMEbus registers. This bit must always remain a zero after being cleared to zero by the resource manager. (for A16 only devices)

(Bits 14-2) Device Dependent (Not used)

(Bit 1) Sysfail Inhibit: This bit controls the device's ability to drive the SYSFAIL line.
0b = Always set to zero (Sysfail not inhibited)

(Bit 0) Device Reset: This bit controls the state of the device.
1b = Reset the device to power-on state.
0b = Normal operational mode

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VXI Device Register Description (Continued)

VXI Configuration Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Offset Value															

06h Offset Register (read/write)

A read of the 16-bit register provides information for calculating the base address of the 3000-514 A32 operational registers.

(Bits 15-0) Offset Value: This field is used for calculating the A32 Base Address.

To obtain the A32 base address for the 3000-514, take the 16 bits of the Offset register and map them to the 16 most significant bits of the A32 Base Address. All other bits in the A32 Base Address are set to zeroes.

A write to this 16-bit register is provided for Dynamic Configuration protocol. This register should only be written to by a resource manager. ***Do not write to this register.***

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VXI Device Register Description (Continued)

VXI Device Class Dependent Registers

The ASCOR 3000-514 Module does not use nor provide any of the 12 Device Class Dependent Registers.

Offset	Description
08h	Not Used
0Ah	Not Used
0Ch	Not Used
0Eh	Not Used
10h	Not Used
12h	Not Used
14h	Not Used
16h	Not Used
18h	Not Used
1Ah	Not Used
1Ch	Not Used
1Eh	Not Used

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VXI Device Register Description (Continued)

VXI Device Dependent Registers for the 3000-514

The VXI Specification defines 16 Device Dependent Registers in the A16 address space following the Device Class Dependent Register space. Each register is 16 bits wide. The first 15 registers are not used nor provided by the ASCOR 3000-514 Module, only the last register is used.

Offset	Description
20h	Not Used
22h	Not Used
24h	Not Used
26h	Not Used
28h	Not Used
2Ah	Not Used
2Ch	Not Used
2Eh	Not Used
30h	Not Used
32h	Not Used
34h	Not Used
36h	Not Used
38h	Not Used
3Ah	Not Used
3Ch	Not Used

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VXI Device Register Description (Continued)

VXI Device Dependent Registers for the 3000-514

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved								IRQ Level Select			GPS ENBL	SP2 ENBL	SP1 ENBL	DATA ENBL	CMD ENBL

3Eh Control Register (read/write)

This 16-bit register provides the 3000-514 module control status.

(Bits 15-8) Reserved
0h = Should always be set to zeroes

(Bits 7-5) IRQ Level Select: These bits control the module's Interrupt Request Level
0h = No IRQ Level Selected, module Interrupt disabled.
1h = IRQ Level 1 Selected, module Interrupt enabled.
2h = IRQ Level 2 Selected, module Interrupt enabled.
3h = IRQ Level 3 Selected, module Interrupt enabled.
4h = IRQ Level 4 Selected, module Interrupt enabled.
5h = IRQ Level 5 Selected, module Interrupt enabled.
6h = IRQ Level 6 Selected, module Interrupt enabled.
7h = IRQ Level 7 Selected, module Interrupt enabled.

(Bit 4) GPS Driver Output Enable: This bit controls the GPS Port Drivers
0h = Driver Outputs Tristated
1h = Driver Output Enabled

(Bit 3) Status Port 2 Driver Output Enable: This bit controls the Status Port 2 Drivers
0h = Driver Outputs Tristated
1h = Driver Output Enabled

(Bit 2) Status Port 1 Driver Output Enable: This bit controls the Status Port 1 Drivers
0h = Driver Outputs Tristated
1h = Driver Output Enabled

(Bit 1) Data Driver Output Enable: This bit controls the Data Port Drivers
0h = Driver Outputs Tristated
1h = Driver Output Enabled

(Bit 0) CMD Driver Output Enable: This bit controls the CMD Port Drivers
0h = Driver Outputs Tristated
1h = Driver Output Enabled

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Circuit Description

The 3000-514 CCM Serial I/F provides six (6) Custom Serial Interface Ports for the Command Control Module (CCM). The six 3000-514 Ports are the CMD Port, the Data Port, the TLM Port, Status Port 1, Status Port 2, and the GPS Port. Each of the Ports is described in the following pages.

CMD Port

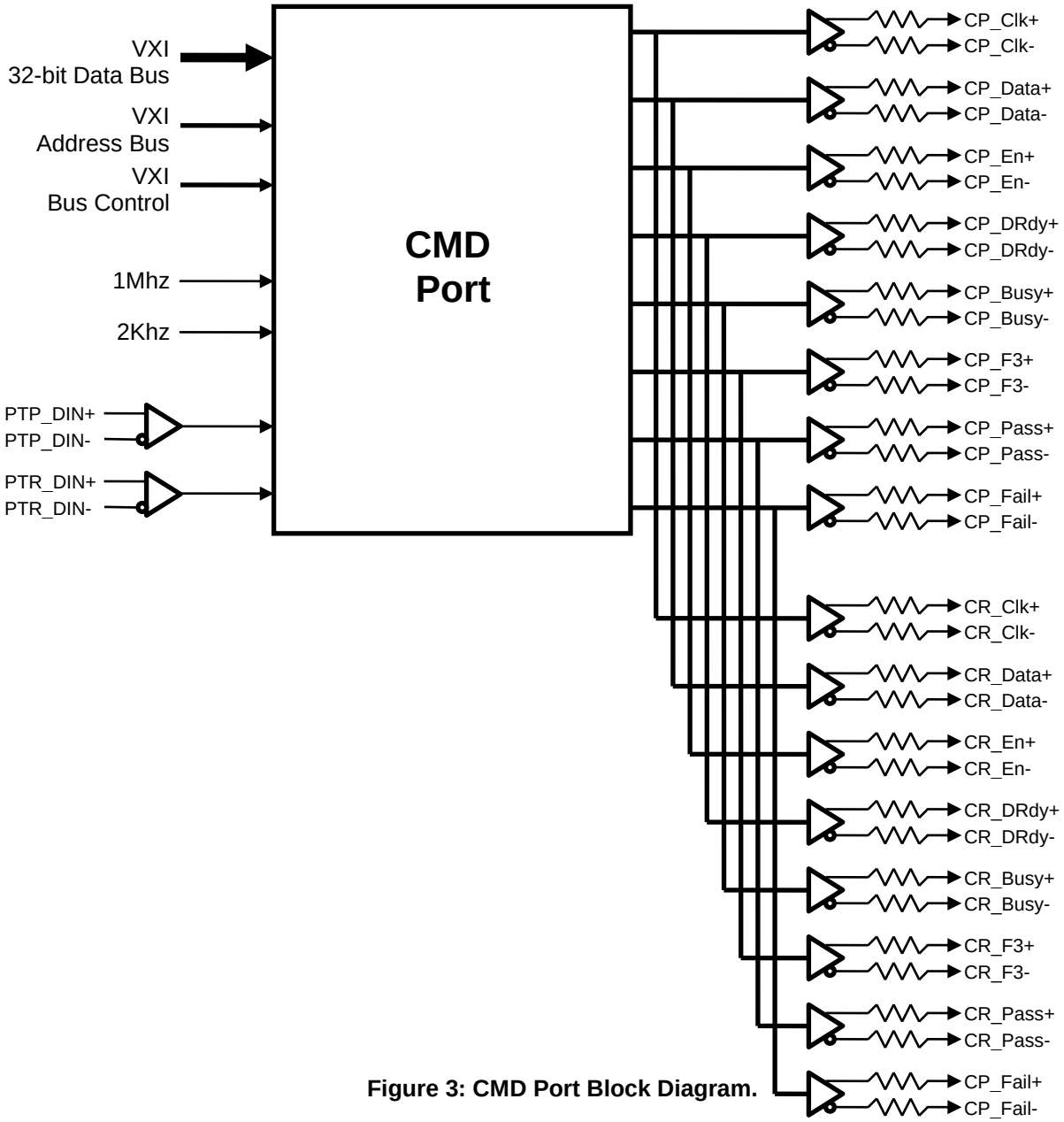


Figure 3: CMD Port Block Diagram.

The CMD Port transmits 32-bit Command Words at a rate of 2 Kbps with a programmable delay between each word. The CCM I/F provides a 32-bit FIFO for up to 63 command words and is configurable for sending the commands either Least Significant Bit (LSB) or Most Significant Bit (MSB) first.

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CMD Port (Continued)

The CMD Port consists of 8 output signals and 1 input signal as described below.

Signal Name	I/O	Description
Clock	O	2 Khz rate
Data	O	32 Bits
Enable	O	Active High Gate
DataRdy	O	Same as Enable or programmable as Static '0' or '1'
BusyOut	O	Not Enable
F3Flag	O	Programmable as Static '0' or '1'
PassOut	O	Programmable as Static '0' or '1'
FailOut	O	Programmable as Static '0' or '1'
PT_DIN	I	Active Low Pulse

The CMD Port utilizes Differential Line Drivers (26LS31), as well as Differential Line Receivers (26LS32). Each signal is redundant, with the CMD Port Primary/Redundant Select Bit (Offset 8000h, Bit 1) selecting either all Primary signals (default) or all Redundant signals. A CMD Port Output Disable (Offset 8000h, Bit 0) permits loading Command Words into the 63-Word FIFO. The CMD Clock is a burst clock with a 50% duty cycle. Data bits change on the falling edge of the clock and are stable on the rising edge of the clock. A low transition on the PT_DIN input signal sets the CMD Port PT_DIN Flag in the Status Register (Offset 8004h, Bit 0).

The CCM Serial I/F provides the following CMD Port configurations:

Configuration Mode	Default Value	Selectable
Command Output	Disabled	Enabled
Drivers / Receivers	Disabled	Primary or Redundant
Data	MSB first	LSB first
Data Rate	2Khz	32Khz or 1.024Mhz (for Self Test)
Word Size	32-Bit	16-Bit (for Self Test)
DataRdy	Follow Enable Signal	0 or 1
F3Flag	0	1
PassOut	0	1
FailOut	0	1
Command Delay	977ns	977ns to 16ms in 244ns steps

See the CCM Serial I/F Control Register description (Page 25), and the CCM Serial I/F Status Register Description (Page 29) for complete details on the CMD Port.

CMD Port Programming Notes:

- Pre-configure all of the CMD Port options (Primary/Redundant, MSB/LSB, Clock Rate, Word Size, Delay, …) prior to enabling it.

- Once enabled (by setting the CMD Port Output Enable bit in the CCM Serial I/F Control Register), the CMD Port will output any words in the FIFO until it is empty. If left enabled the CMD Port will wait for the next word to be written into the FIFO, and output it as soon as the empty condition is negated. In order to guarantee the programmed inter-word delay, the CMD Port should be disabled during loading.

- Do not overfill the 63-Word FIFO. If this occurs (as indicated by the Over-Full Flag in the CCM Serial I/F Status Register), subsequent writes to the CMD FIFO will be ignored. Empty the CMD FIFO and perform 2 Dummy Writes to clear the Over-Full condition.

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Data Port

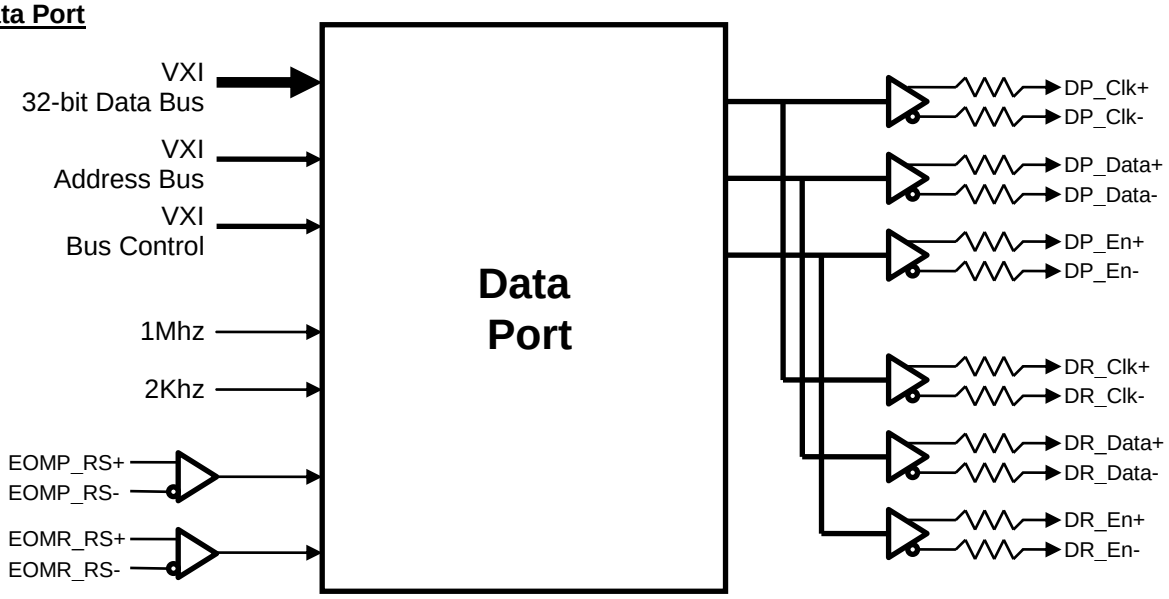


Figure 4: Data Port Block Diagram

The Data port transmits 64 or 32-bit Data Words at a rate of 2 Kbps with a programmable delay between each word. The CCM I/F provides a 511-Word FIFO for 64-bit transfers or a 1023-Word FIFO for 32-bit transfers, and is configurable for sending the data either LSB or MSB first.

The Data Port consists of 3 output signals and 1 input signal as described below.

Signal Name	I/O	Description
Clock	O	2 Khz rate
Data	O	64 or 32 Bits
Enable	O	Active High Gate
EOM_RST	I	Active Low Pulse

The Data Port utilizes Differential Line Drivers (26LS31), as well as Differential Line Receivers (26LS32). Each signal is redundant, with the Data Port Primary/Redundant Select Bit (Offset 8000h, Bit 12) selecting either all Primary signals (default) or all Redundant signals. A Data Port Output Disable (Offset 8000h, Bit 11) permits loading Data Words into the FIFO. The Data Clock is a burst clock with a 50% duty cycle. Data bits change on the falling edge of the clock and are stable on the rising edge of the clock. A low transition on the EOM_RS input signal terminates any transfer currently active on the Data Port, clears the Data FIFO, and sets the Data Port EOM_RS Flag in the Status Register (Offset 8004h, Bit 4).

The CCM Serial I/F provides the following Data Port configurations:

Configuration Mode	Default Value	Selectable
Data Output	Disabled	Enabled
Drivers / Receivers	Disabled	Primary or Redundant
Data	MSB first	LSB first
Data Rate	2Khz	None
Word Size	64-Bit	32-Bit
Command Delay	977ns	977ns to 16ms in 244ns steps

See the CCM Serial I/F Control Register description (Page 25), and the CCM Serial I/F Status Register Description (Page 29) for complete details on the Data Port.

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Data Port programming Notes:

- Pre-configure all of the Data Port options (Primary/Redundant, MSB/LSB, Word Size, Delay, …) prior to enabling it.
- Once enabled (by setting the Data Port Output Enable bit in the CCM Serial I/F Control Register), the Data Port will output any words in the FIFO until it is empty. If left enabled the Data Port will wait for the next word to be written into the FIFO, and output it as soon as the empty condition is negated. In order to guarantee the programmed inter-word delay, the Data Port should be disabled during loading.
- Do not overfill the 1023-Word FIFO. If this occurs (as indicated by the Over-Full Flag in the CCM Serial I/F Status Register), subsequent writes to the Data FIFO will be ignored. Empty the Data FIFO and perform 2 Dummy Writes to clear the Over-Full condition.
- During 64-bit Data Port Self Test (Gated 64-Bit Mode) the TLM Port will store twelve 64-bit Words (in the form of twenty four 32-bit words) in each TLM FIFO.

TLM Port

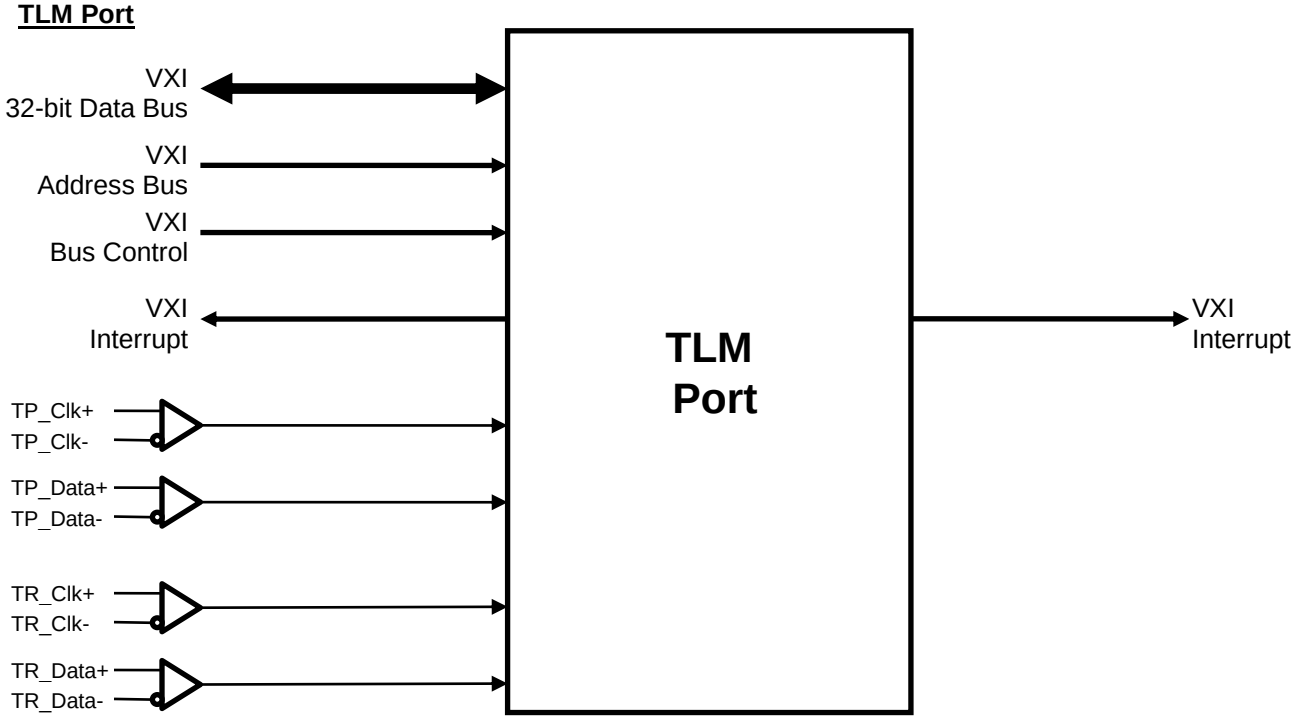


Figure 5: TLM Port Block Diagram.

The CCM I/F TLM port receives data Frames which consist of 800 bits of data, or 25 32-bit words, at a rate of 32 Kbps. The TLM Port provides four 63 Word FIFO's and is configurable for receiving the data either LSB or MSB first. The four FIFO's work in a circular mode, ie: the TLM Port writes the first Frame (25 words) to FIFO #1, sets the FIFO #1 Frame Status Flag, and generates a programmable VXI Interrupt back to the VXI controller. Then the next Frame is written to FIFO #2, and the FIFO #2 Frame Status Flag as well as another VXI Interrupt are asserted. This process is repeated for FIFO's #3 and #4 in turn. After all four FIFO's have been filled, the TLM Port begins the cycle again by writing the next Frame into FIFO #1. Each FIFO is reset as soon as the preceding FIFO has received a Frame of data. The TLM Port also sets the associated FIFO Flags (Empty, Half-Full, and Over-Full) in the CCM Serial I/F Status Register.

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The TLM port consists of 2 input signals as described below.

Signal Name	I/O	Description
Clock	I	32 Khz rate
Data	I	32 Bits

The TLM Port utilizes Differential Line Receivers (26LS32). Each signal is redundant, with the TLM Port Primary/Redundant Select Bit (Offset 8000h, Bit 12) selecting either all Primary signals (default) or all Redundant signals. The TLM Port Mode Select Bits (Offset 8000h, Bit 17,18) configure the TLM Port to be either disabled (default), in Free-Running Mode, in Sync Mode, or in Gated Mode (Self Test) as described below.

Disabled: In Disabled Mode the TLM Port ignores all incoming data.

Free-Running Mode: In Free-Running mode the TLM port captures every 32-bits as a Word and stores it in the current FIFO. After each FIFO receives a Frame of data (25 Words), the TLM Port sets the associated Frame Status Flag and generates an Interrupt .

Sync Mode: In Sync Mode the TLM Port compares the incoming serial data stream to a programmable 32-bit Sync word. Once detected, the Sync Word is stored in the first Word location of the current FIFO, followed by the next 24 32-bit words. The TLM Port then begins searching for the Sync Word again.

Gated Mode (Self Test): This mode is similar to the Free-Running Mode, except the TLM Port receives a Gated Burst Clock, and stores 24 data Words in the normal circular method.

The incoming Clock has a 50% duty cycle. Data bits are changed on the rising edge of the clock, and are clocked-in on the falling edge of the clock. The TLM Port has been designed to accept both Internal and External Loop-Back data from the CMD Port, the Data Port, Status Port 1, and Status Port 2, for Self Test purposes. See the Self Test Descriptions for each Port (Page 37-42) for specific details on each Port.

The CCM Serial I/F provides the following Telemetry Port configurations:

Configuration Mode	Default Value	Selectable
Receivers	Primary	Redundant
Data	MSB first	LSB first
Data Capture Mode	Disabled	Free-Running Mode Sync Mode Gated Mode (for Self Test)
Word Size	32-Bit	64 or 16-Bit (for Self Test)
Clock Source / Edge	External / Falling	External / Rising (for Self Test) Internal CMD Port / Rising (for Self Test) Internal Data Port / Rising (for Self Test)
Gate Source	Internal CMD Port (for Self Test)	Internal Data Port (for Self Test)
Data Source	External	Internal CMD Port (for Self Test) Internal Data Port (for Self Test) Internal Status Port 1 (for Self Test) Internal Status Port 2, Data 1 (for Self Test) Internal Status Port 2, Data 1 (for Self Test)

See the CCM Serial I/F Control Register description (Page 25), and the CCM Serial I/F Status Register Description (Page 29) for complete details on the TLM Port.

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TLM Port programming Notes:

- Pre-configure all of the TLM Port options (Primary/Redundant, MSB/LSB, Word Size, Sync Word, …) prior to enabling the TLM Mode.
- Read the Frame data from each TLM FIFO within 3 Frames of It's associated Frame Interrupt. Each FIFO is reset as soon as the preceding FIFO has received a Frame of data.
- The TLM Port circular FIFO controls are reset when the TLM Port is in Disabled Mode. Always Empty FIFO #1 and pass through Disabled Mode prior to entering another TLM Mode. This will configure the TLM Port to begin storing data in the first Word location of FIFO #1.
- Enabling the Sync Mode prior to entering the Sync Word may result in an inadvertent Sync Match and the initiation of a Frame capture. For example, on power-up the Sync Word Register contains "0h" and will match with "0" or Low data, initiating a Frame capture.
- Do not read the Sync Word Register when Sync Mode is enabled. This will cause a Sync match and initiate a Frame Capture.
- Do not utilize Sync words which contain a repeating pattern such as "11111111h". This type of Sync Word may be misinterpreted with data as they are serially received. For example, if the Sync Word is set to "AAAAAAAAh" and a data word of "55555555h" is received followed by one "0" bit, it will match and initiate a Frame capture.
- Do not repeat the Sync Pattern in the final word position (25th Word) of a Frame. It will be matched and cause the initiation of another Frame capture.
- In Free and Sync Modes, 25 Words are stored in each FIFO. In Gated Mode (Self Test), 24 Words are stored in each FIFO. See the Self Test Descriptions for each Port (Page 37-42) for specific details on each Port.
- Do not overfill the 63-Word FIFO's. If this occurs (as indicated by the Over-Full Flag in the CCM Serial I/F Status Register), subsequent writes to the TLM FIFO will be ignored. Empty the TLM FIFO and perform 2 Dummy Writes to clear the Over-Full condition.

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Status Port 1

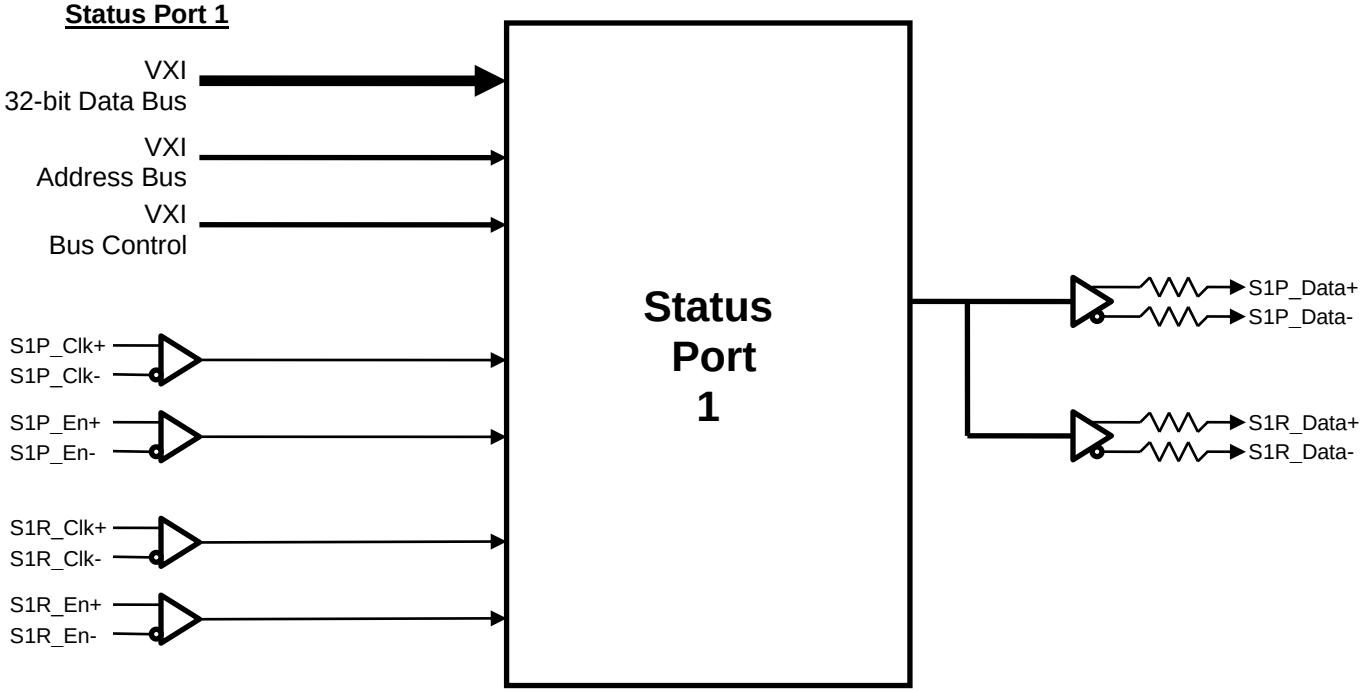


Figure 6: Status Port 1 Block Diagram.

The CCM I/F Status Port 1 transmits 32-bit data Words at a rate of 1.024 Mbps. Status Port 1 provides a 32-bit Register which is serially output upon receipt of the Status Port 1 Clock and Enable. Status Port 1 is configurable for sending the data either LSB or MSB first.

Status Port 1 consists of 2 input signals and 1 output signal as described below.

Signal Name	I/O	Description
Clock	I	1.024 Mhz rate
Data	O	32 Bits
Enable	I	Active High Gate

Status Port 1 utilizes Differential Line Drivers (26LS31), as well as Differential Line Receivers (26LS32). Each signal is redundant, with the Status Port 1 Primary/Redundant Select Bit (Offset 8000h, Bit 27) selecting either all Primary signals (default) or all Redundant signals. The incoming Clock has a 50% duty cycle. Data bits are changed on the rising edge of the clock, and are stable on the falling edge of the clock.

The CCM I/F provides the following Status Port 1 configurations:

Configuration Mode	Default Value	Selectable
Drivers / Receivers	Disabled	Primary or Redundant
Data	MSB first	LSB first

See the CCM Serial I/F Control Register description (Page 25) for complete details on Status Port 1.

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Status Port 2

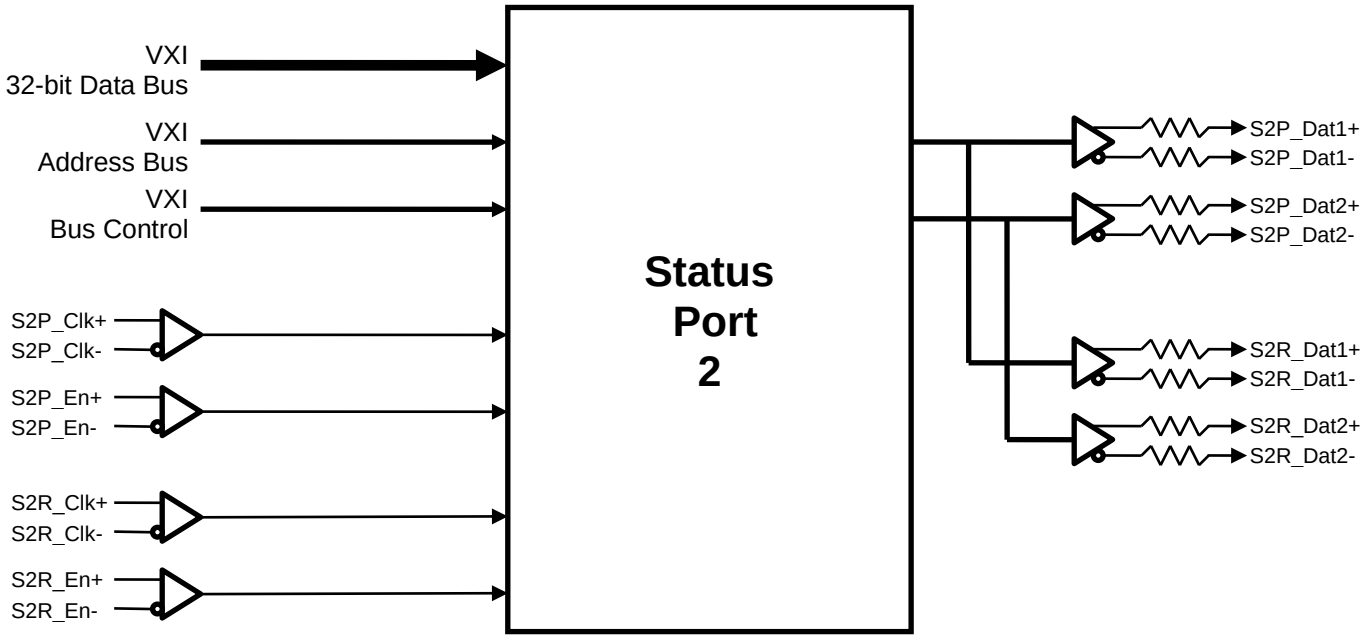


Figure 7: Status Port 2 Block Diagram.

The CCM I/F Status Port 2 transmits two simultaneous 16-bit data words at a rate of 1.024 Mbps. Status Port 2 provides a 32-bit register which is serially output as two unique 16-bit words (Data 1 = bits 0-15, Data 2 = bits 16-31) upon receipt of the Status Port 2 Clock and Enable. Status Port 2 is configurable for sending both data words either LSB or MSB first.

Status Port 2 consists of 2 input signals and 1 output signal as described below.

Signal Name	I/O	Description
Clock	I	1.024 Mhz rate
Data 1	O	16 Bits
Data 2	O	16 Bits
Enable	I	Active High Gate

Status Port 2 utilizes Differential Line Drivers (26LS31), as well as Differential Line Receivers (26LS32). Each signal is redundant, with the Status Port 2 Primary/Redundant Select Bit (Offset 8000h, Bit 29) selecting either all Primary signals (default) or all redundant signals. The incoming Clock has a 50% duty cycle. Data bits are changed on the rising edge of the clock, and are stable on the falling edge of the clock.

The CCM I/F provides the following Status Port 2 configurations:

Configuration Mode	Default Value	Selectable
Drivers / Receivers	Disabled	Primary or Redundant
Data	MSB first	LSB first

See the CCM Serial I/F Control Register description (Page 25) for complete details on Status Port 2.

SP1 Port programming Notes:

- During SP2 Self Test (Gated 16-Bit Mode) the direction determines which half of the 32-bit word to mask when reading the TLM FIFO. If the TLM Shift Register is configured for MSB first, the upper 16-bits of each word stored in the TLM FIFO should be masked. If the TLM Shift Register is configured for LSB first, the lower 16-bits of each word stored in the TLM FIFO should be masked.

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GPS Port

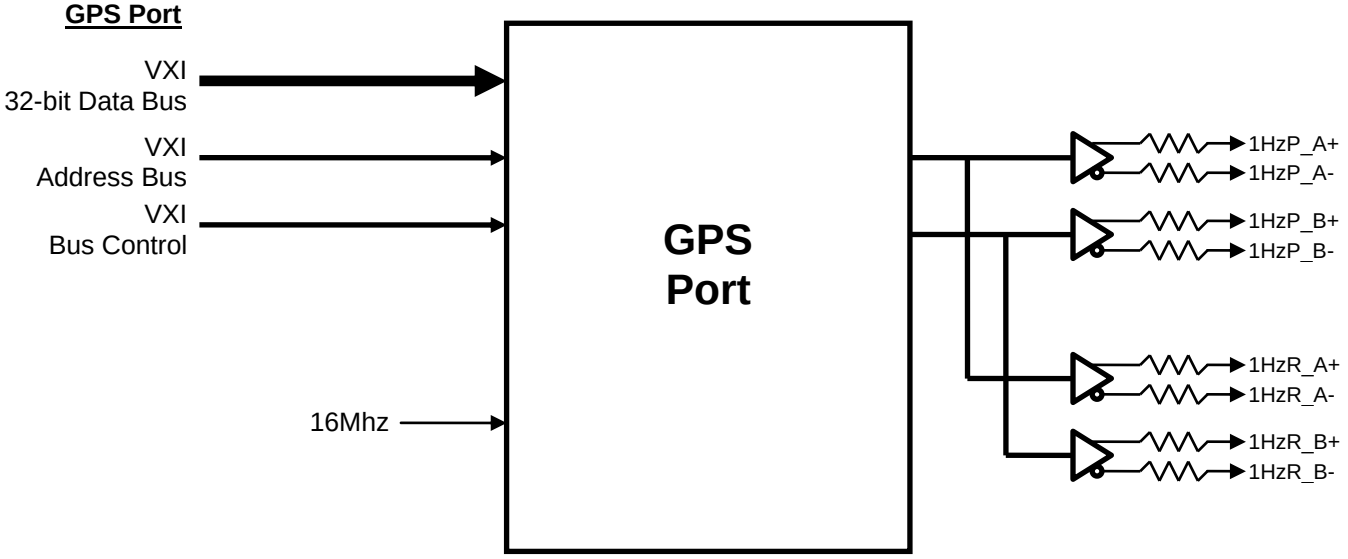


Figure 8: GPS Port Block Diagram.

The CCM Serial I/F generates two GPS 1 Hz clocks. GPS clock 2 has a programmable skew with respect to GPS clock 1.

The GPS Port consists of 2 output signals as described below.

Signal Name	I/O	Description
Clock 1	O	1hz
Clock 2	O	1hz

The GPS Port utilizes Differential Line Drivers (26LS31). Each signal is redundant, with the GPS Port Primary/Redundant Select Bit (Offset 8000h, Bit 31) selecting either all Primary signals (default) or all Redundant signals. The GPS clock 2 Skew is programmable in 1μsec steps from 1μsec up to 499.999ms.

The CCM I/F provides the following GPS Port configurations:

Configuration Mode	Default Value	Selectable
Drivers	Disabled	Primary or Redundant

See the CCM Serial I/F Control Register description (Page 25) for complete details on the GPS Port.

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32-BIT REGISTER MAP

DESCRIPTION: CCM Serial I/F, Mother Board
PCB NUMBER: 85002330

ADDRESS	SIZE	TYPE	DESCRIPTION
8000h	32 bit	R/W	CCM Serial I/F Control Register
8004h	32 bit	R	CCM Serial I/F Status Register
8008h	32 bit	R/W	CCM Serial I/F CMD FIFO
800Ch	32 bit	R/W	CCM Serial I/F CMD/Data Word Delay Register
8010h	32 bit	R/W	CCM Serial I/F Data FIFO
8014h	32 bit	R/W	CCM Serial I/O TLM Shift Register
8018h	32 bit	R/W	CCM Serial I/F TLM Sync Word Register
801Ch	32 bit	R/W	CCM Serial I/F TLM FIFO #1
8020h	32 bit	R/W	CCM Serial I/F TLM FIFO #2
8024h	32 bit	R/W	CCM Serial I/F TLM FIFO #3
8028h	32 bit	R/W	CCM Serial I/F TLM FIFO #4
802Ch	32 bit	R/W	CCM Serial I/F Status Port 1 Register
8030h	32 bit	R/W	CCM Serial I/F Status Port 2 Register
8034h	24 bit	R/W	CCM Serial I/F GPS Clock Skew Register

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32-BIT REGISTER DESCRIPTION

ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

CCM Serial I/F Control Register : This register provides the configuration control for each of the Ports. Writing a 1 to a bit location enables the associated function. Writing a 0 to a bit location disables the associated function. The power-up/reset default register configuration is all functions disabled. A read at this address returns the contents of the CCM Serial I/F Control Register (0=Disabled, 1=Enabled). The Power-up / Reset state is 00000000h.

BIT	FUNCTION
0	CMD Port Output Enable
1	CMD Port Redundant Driver Enable
2	CMD Port LSB First Data Output Enable
3	CMD Port Clock Rate Select (Lsb)
4	CMD Port Clock Rate Select (Msb)
5	CMD Port 16-Bit Word Size
6	CMD Port DataRdy Static Mode Enable
7	CMD Port DataRdy Static Level
8	CMD Port F3 Static Level
9	CMD Port PASS Static Level
10	CMD Port Fail Static Level
11	Data Port Output Enable
12	Data Port Redundant Driver Enable
13	Data Port LSB First Data Output Enable
14	Data Port 32-Bit Word Size
15	TLM Port Redundant Input Enable
16	TLM Port LSB First Data Input Enable
17	TLM Port Mode Select (Lsb)
18	TLM Port Mode Select (Msb)
19	TLM Port Word Size Select (Lsb)
20	TLM Port Word Size Select (Msb)
21	TLM Port Clock Source Select (Lsb)
22	TLM Port Clock Source Select (Msb)
23	TLM Port Gate Source Select
24	TLM Port Data Source Select (Lsb)
25	TLM Port Data Source Select
26	TLM Port Data Source Select (Msb)
27	Status Port 1 Redundant Driver Enable
28	Status Port 1 LSB First Data Output Enable
29	Status Port 2 Redundant Driver Enable
30	Status Port 2 LSB First Data Output Enable
31	GPS Port Redundant Driver Select

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Any or all Ports can be configured with a single 32-bit write operation. Care must be taken when values are written in order to prevent unintended Function enabling or disabling. In order to preserve the configuration of the Ports that you do not want to alter, perform the following sequence of operations:

1. Read the CCM Serial I/F Control Register and save the register contents.
2. Modify the copy of the CCM Serial I/F Control Register by setting or clearing only the bits associated with the desired function.
3. Write the new value back to the CCM Serial I/F Control Register.

ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

CCM Serial I/F Control Register : CMD Port Configuration Control

Bit 0 - CMD Port Output Enable: (Default = CMD State Machine disabled)
Setting this bit enables the CMD Port to begin outputting Data.

Bit 1 - CMD Port Redundant Enable: (Default = CMD Port Primary Outputs enabled)
Setting this bit enables the Redundant outputs of the CMD Port.

Bit 2 - CMD Port LSB First: (Default = CMD Port Data MSB First)
Setting this bit configures the CMD Data to output Least Significant Bit First.

Bit 4,3 - CMD Port Clock Rate: (Default = CMD Port Clock 2Khz)
These bit configures the CMD Port Clock Rate: 00 = 2Khz
01 = 32Khz (TLM Self Test)
10 = 1.024Mhz (Status Port Self Test)
11 = Not Used

Bit 5 - CMD Port 16 Bit Data: (Default = CMD Port Data Word 32-bit)
Setting this bit configures the CMD Data Word size to 16-bits.

Bit 6 - CMD Port DataRdy Static: (Default = CMD Port DataRdy follows CMD Enable)
Setting this bit configures the CMD Port DataRdy Signal to static level mode.

Bit 7 - CMD Port DataRdy Static 1: (Default = CMD Port DataRdy static mode 0)
Setting this bit configures the CMD Port DataRdy Signal to a static level of 1.

Bit 8 - CMD Port F3 Static 1: (Default = CMD Port F3 static mode 0)
Setting this bit configures the CMD Port F3 Signal to a static level of 1.

Bit 9 - CMD Port PASS Static 1: (Default = CMD Port PASS static mode 0)
Setting this bit configures the CMD Port PASS Signal to a static level of 1.

Bit 10 - CMD Port FAIL Static 1: (Default = CMD Port FAIL static mode 0)
Setting this bit configures the CMD Port FAIL Signal to a static level of 1.

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ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

CCM Serial I/F Control Register : Data Port Configuration Control

Bit 11 - Data Port Output Enable: (Default = Data State Machine disabled)
Setting this bit enables the Data Port to begin outputting Data.

Bit 12 - Data Port Redundant Enable: (Default = Data Port Primary Outputs enabled)
Setting this bit enables the Redundant outputs of the Data Port.

Bit 13 - Data Port LSB First: (Default = Data Port Data MSB First)
Setting this bit configures the Data Port Data to output Least Significant Bit First.

Bit 14 - Data Port 32 Bit Data: (Default = Data Port Data Word 64-bit)
Setting this bit configures the Data Port Word size to 32-bits.

ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

CCM Serial I/F Control Register : TLM Port Configuration Control

Bit 15 - TLM Port Redundant Enable: (Default = TLM Port Primary Inputs enabled)
Setting this bit selects the Redundant inputs of the TLM Port.

Bit 16 - TLM Port LSB First: (Default = TLM Port Data MSB First)
Setting this bit configures the TLM Port to input data Least Significant Bit First.

Bit 18,17 - TLM Port Mode: (Default = TLM Port Disabled)
These bits configure the TLM Port Mode:
00 = TLM Port Disabled
01 = Free-Running Mode (No Sync Detect)
10 = Sync Mode (32-bit Sync Detect)
11 = Gated Mode (Self Test)

Bit 20,19 - TLM Port Word Size: (Default = TLM Port Data Word 32-bit)
Setting this bit configures the TLM Port Word size:
00 = 32-bit
01 = 64-bit (Data Port Self Test)
10 = 16-bit (Status Port Self Test)
11 = Not Used

Bit 22,21 - TLM Port Clock Source: (Default = TLM Port Primary/Redundant Clock Source, Falling Edge)
Setting this bit configures the TLM Port Clock Source and Clock Edge:

00 = Primary/Redundant External Clock, Falling Edge Data Capture
01 = Primary/Redundant External Clock, Rising Edge Data Capture
10 = CMD Port Internal Clock, Rising Edge Data Capture (Self Test)
11 = Data Port Internal Clock, Rising Edge Data Capture (Self Test)

Bit 23 - TLM Port Gate Source: (Default = TLM Port internal CMD Gate Source)
Setting this bit configures the TLM Port gate source to internal Data Gate Source.

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ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

Bit 26-24 - TLM Port Data Source: (Default = TLM Port Primary/Redundant Data Source)
Setting this bit configures the TLM Port Data Source:
000 = Primary/Redundant Receivers
001 = Internal CMD Port (Self Test)
010 = Internal Data Port (Self Test)
011 = Internal Status Port 1 (Self Test)
100 = Internal Status Port 2 Data 1(Self Test)
101 = Internal Status Port 2 Data 2(Self Test)
110-111 = Not Used

ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

CCM Serial I/F Control Register : Status Port 1 Configuration Control

Bit 27 - Status Port 1 Redundant Enable: (Default = Status Port 1 Primary Outputs enabled)
Setting this bit enables the Redundant outputs of Status Port 1.

Bit 28 - Status Port 1 LSB First: (Default = Status Port 1 Data MSB First)
Setting this bit configures the Status Port 1 Data to output Least Significant Bit First.

ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

CCM Serial I/F Control Register : Status Port 2 Configuration Control

Bit 29 - Status Port 2 Redundant Enable: (Default = Status Port 2 Primary Outputs enabled)
Setting this bit enables the Redundant outputs of Status Port 2.

Bit 30 - Status Port 2 LSB First: (Default = Status Port 2 Data MSB First)
Setting this bit configures the Status Port 2 Data to output Least Significant Bit First.

ADDR: 8000h **Read / Write**

BIT	31	30-29	28-27	26-15	14-11	10-0
FUNCTION	GPS Port	Status Port 2	Status Port 1	TLM Port	Data Port	CMD Port

CCM Serial I/F Control Register : GPS Port Configuration Control
Bit 31 - GPS Port Redundant Enable: (Default = GPS Port Primary Outputs enabled)
Setting this bit enables the Redundant outputs of the GPS Port.

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32-BIT REGISTER DESCRIPTION

ADDR: 8004h **Read Only**

BIT	31-24	23-8	7-4	3-0
FUNCTION	Unused	TLM Port	Data Port	CMD Port

CCM Serial I/F Status Register : This register provides the status for each of the Ports. The function for each bit is described below. A read at this address returns the contents of the CCM Serial I/F Status Register. The Power-up / Reset state is 00DB60CCh.

BIT	FUNCTION
0	CMD Port PT_DIN Flag
1	CMD Port FIFO Empty Flag
2	CMD Port FIFO Half Full Flag
3	CMD Port FIFO Over-Full Flag
4	DATA Port EOM_RST Flag
5	DATA Port FIFO Empty Flag
6	DATA Port FIFO Half Full Flag
7	DATA Port FIFO Over-Full Flag
8	TLM Port FIFO #1 Interrupt
9	TLM Port FIFO #2 Interrupt
10	TLM Port FIFO #3 Interrupt
11	TLM Port FIFO #4 Interrupt
12	TLM Port FIFO #1 Empty Flag
13	TLM Port FIFO #1 Half Full Flag
14	TLM Port FIFO #1 Over-Full Flag
15	TLM Port FIFO #2 Empty Flag
16	TLM Port FIFO #2 Half Full Flag
17	TLM Port FIFO #2 Over-Full Flag
18	TLM Port FIFO #3 Empty Flag
19	TLM Port FIFO #3 Half Full Flag
20	TLM Port FIFO #3 Over-Full Flag
21	TLM Port FIFO #4 Empty Flag
22	TLM Port FIFO #4 Half Full Flag
23	TLM Port FIFO #4 Over-Full Flag
24	Unused (Tied Low)
25	Unused (Tied Low)
26	Unused (Tied Low)
27	Unused (Tied Low)
28	Unused (Tied Low)
29	Unused (Tied Low)
30	Unused (Tied Low)
31	Unused (Tied Low)

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ADDR: 8004h **Read Only**

BIT	31-24	23-8	7-4	3-0
FUNCTION	Unused	TLM Port	Data Port	CMD Port

CCM Serial I/F Status Register : CMD Port Status

Bit 0 - PT_DIN Flag: (Default = Flag Inactive Low)
When set (1), this bit indicates that the PT_DIN Signal was asserted since the Status Register was last read. A low (0) indicates that there has been no activity on the PT_DIN Signal since the Status Register was last read. Reading the Status Register clears this bit.

Bit 1 - CMD Port FIFO Empty Flag: (Default = Flag active Low)
When set (1), this bit indicates that the CMD FIFO is not empty. A low (0) indicates that the CMD FIFO is empty.

Bit 2 - CMD Port FIFO Half Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that the CMD FIFO is not Half Full (<=32 Words). A low (0) indicates that the CMD FIFO is Half Full (>32 Words).

Bit 3 - CMD Port FIFO Over-Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that the CMD FIFO has not been Over-Filled (<=63 Words). A low (0) indicates that the CMD FIFO has been Over-Filled (>63 Words).

ADDR: 8004h **Read Only**

BIT	31-24	23-8	7-4	3-0
FUNCTION	Unused	TLM Port	Data Port	CMD Port

CCM Serial I/F Status Register : Data Port Status

Bit 4 - EOM_RST Flag: (Default = Flag Inactive Low)
When set (1), this bit indicates that the EOM_RST Signal was asserted since the Status Register was last read. A low (0) indicates that there has been no activity on the EOM_RST Signal since the Status Register was last read. Reading the Status Register clears this bit.

Bit 5 - DATA Port FIFO Empty Flag: (Default = Flag active Low)
When set (1), this bit indicates that the DATA FIFO is not empty. A low (0) indicates that the DATA FIFO is empty.

Bit 6 - DATA Port FIFO Half Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that the DATA FIFO is not Half Full (<=512 Words). A low (0) indicates that the DATA FIFO is Half Full (>512 Words).

Bit 7 - DATA Port FIFO Over-Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that the DATA FIFO has not been Over-Filled (<=1023 Words). A low (0) indicates that the DATA FIFO has been Over-Filled (>1023 Words).

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ADDR: 8004h **Read Only**

BIT	31-24	23-8	7-4	3-0
FUNCTION	Unused	TLM Port	Data Port	CMD Port

CCM Serial I/F Status Register : TLM Port Status

Bit 8 - TLM Port FIFO #1 Frame Flag: (Default = Flag Inactive Low)
When set (1), this bit indicates that the TLM Port FIFO #1 contains a Full Frame of Data (25 Words) and is ready to be read. A low (0) indicates that the TLM Port FIFO #1 does not contain a Full Frame of Data (25 Words).

Bit 9 - TLM Port FIFO #2 Frame Flag: (Default = Flag Inactive Low)
When set (1), this bit indicates that the TLM Port FIFO #2 contains a Full Frame of Data (25 Words) and is ready to be read. A low (0) indicates that the TLM Port FIFO #2 does not contain a Full Frame of Data (25 Words).

Bit 10 - TLM Port FIFO #3 Frame Flag: (Default = Flag Inactive Low)
When set (1), this bit indicates that the TLM Port FIFO #3 contains a Full Frame of Data (25 Words) and is ready to be read. A low (0) indicates that the TLM Port FIFO #3 does not contain a Full Frame of Data (25 Words).

Bit 11 - TLM Port FIFO #4 Frame Flag: (Default = Flag Inactive Low)
When set (1), this bit indicates that the TLM Port FIFO #4 contains a Full Frame of Data (25 Words) and is ready to be read. A low (0) indicates that the TLM Port FIFO #4 does not contain a Full Frame of Data (25 Words).

Bit 12 - TLM Port FIFO #1 Empty Flag: (Default = Flag active Low)
When set (1), this bit indicates that TLM FIFO #1 is not empty. A low (0) indicates that TLM FIFO #1 is empty.

Bit 13 - TLM Port FIFO #1 Half Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that TLM FIFO #1 is not Half Full (<=32 Words). A low (0) indicates that TLM FIFO #1 is Half Full (>32 Words).

Bit 14 - TLM Port FIFO #1 Over-Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that TLM FIFO #1 has not been Over-Filled (<=63 Words). A low (0) indicates that TLM FIFO #1 has been Over-Filled (>63 Words).

Bit 15 - TLM Port FIFO #2 Empty Flag: (Default = Flag active Low)
When set (1), this bit indicates that TLM FIFO #2 is not empty. A low (0) indicates that TLM FIFO #2 is empty.

Bit 16 - TLM Port FIFO #2 Half Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that TLM FIFO #2 is not Half Full (<=32 Words). A low (0) indicates that TLM FIFO #2 is Half Full (>32 Words).

Bit 17 - TLM Port FIFO #2 Over-Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that TLM FIFO #2 has not been Over-Filled (<=63 Words). A low (0) indicates that TLM FIFO #2 has been Over-Filled (>63 Words).

Bit 18 - TLM Port FIFO #3 Empty Flag: (Default = Flag active Low)
When set (1), this bit indicates that TLM FIFO #3 is not empty. A low (0) indicates that TLM FIFO #3 is empty.

Bit 19 - TLM Port FIFO #3 Half Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that TLM FIFO #3 is not Half Full (<=32 Words). A low (0) indicates that TLM FIFO #3 is Half Full (>32 Words).

Bit 20 - TLM Port FIFO #3 Over-Full Flag: (Default = Flag Inactive High)

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When set (1), this bit indicates that TLM FIFO #3 has not been Over-Filled (<=63 Words). A low (0) indicates that TLM FIFO #3 has been Over-Filled (>63 Words).

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ADDR: 8004h **Read Only**

BIT	31-24	23-8	7-4	3-0
FUNCTION	Unused	TLM Port	Data Port	CMD Port

Bit 21 - TLM Port FIFO #4 Empty Flag: (Default = Flag active Low)
When set (1), this bit indicates that TLM FIFO #4 is not empty. A low (0) indicates that TLM FIFO #4 is empty.

Bit 22 - TLM Port FIFO #4 Half Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that TLM FIFO #4 is not Half Full (<=32 Words). A low (0) indicates that TLM FIFO #4 is Half Full (>32 Words).

Bit 23 - TLM Port FIFO #4 Over-Full Flag: (Default = Flag Inactive High)
When set (1), this bit indicates that TLM FIFO #4 has not been Over-Filled (<=63 Words). A low (0) indicates that TLM FIFO #4 has been Over-Filled (>63 Words).

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32-BIT REGISTER DESCRIPTION

ADDR: 8008h **Read / Write**

BIT	MSB	31-0	LSB
FUNCTION	CMD Port FIFO		

CCM Serial I/F CMD Port FIFO: This is the 63x32-bit FIFO for the CMD Port. A write to this address loads a word into the FIFO. A read from this address returns the contents of the FIFO. Reading the FIFO when it is empty will return the last value read. The Power-up / Reset state is CMD FIFO Empty.

ADDR: 800Ch **Read / Write**

BIT	31-16	15-0
FUNCTION	Data Port Delay	CMD Port Delay

CCM Serial I/F CMD / Data Port Word Delay Register: This Register holds the Delay Words for the CMD and Data Ports. A write to this address loads a word into the Delay Register. A read from this address returns the contents of the Delay Register. The delay increment is 244nS (1 clock period of the 4.096Mhz Clock). The Power-up / Reset state is 00000000h which yields the default minimum 977nS delay between both the CMD and Data Words.

Either or both Port Delays can be configured with a single 32-bit write operation. Care must be taken when values are written in order to prevent unintended modification of the other Port Delay value. In order to preserve the values that you do not want to alter, perform the following sequence of operations:

1. Read the CCM Serial I/F CMD/Data Port Word Delay Register and save the register contents.
2. Modify the copy of the CCM Serial I/F CMD/Data Port Word Delay Register by setting or clearing only the value associated with the desired Port.
3. Write the new value back to the CCM Serial I/F CMD/Data Port Word Delay Register.

ADDR: 800Ch **Read / Write**

BIT	31-16	15-0
FUNCTION	Data Port Delay	CMD Port Delay

CCM Serial I/F CMD / Data Port Word Delay Register: CMD Port Word Delay

Bit 15-0 - CMD Port Word Delay: (Default = 0000h or 977nS Delay)
Each Delay Count represents a 244nS delay between consecutive words of the CMD Port. Values 0000h-0004h yield the Minimum Delay which is 977nS (four 4.096Mhz Clock Cycles) between CMD Words. Each Value above 0004h yields a delay equal to the Value X 244nS. For example a Value 4000h yields a delay of 4mS (16384 X 244nS). The Maximum allowable value is FFFFh which yields 16mS Delay between CMD Words.

ADDR: 800Ch **Read / Write**

BIT	31-16	15-0
FUNCTION	Data Port Delay	CMD Port Delay

CCM Serial I/F CMD / Data Port Word Delay Register: Data Port Word Delay

Bit 31-16 - Data Port Word Delay: (Default = 0000h or 977nS Delay)
Each Delay Count represents a 244nS delay between consecutive words of the Data Port. Values 0000h-0004h yield the Minimum Delay which is 977nS (four 4.096Mhz Clock Cycles) between Data Words. Each Value above 0004h yields a delay equal to the Value X 244nS. For example a Value 4000h yields a delay of 4mS (16384 X 244nS). The Maximum allowable value is FFFFh which yields 16mS Delay between Data Words.

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32-BIT REGISTER DESCRIPTION

ADDR: 8010h **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	Data Port FIFO

CCM Serial I/F Data Port FIFO: This is the 1023x32-bit FIFO for the Data Port. A write to this address loads a word into the FIFO. A read from this address returns the contents of the FIFO. Reading the FIFO when it is empty will return the last value read. The Power-up / Reset state is Data FIFO Empty.

ADDR: 8014h **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	TLM Shift Register

CCM Serial I/F TLM Port Shift Register: This is the 32-bit Shift Register for the TLM Port. In normal operating mode this is a 32-Bit Serial-in/Parallel-out Shift Register which receives the incoming TLM Serial data stream and stores the 32-Bit Parallel data to the TLM FIFO's. A write to this address in overwrites the contents of the 32-Bit Shift Register. A read from this address returns the contents of the Register. The Power-up / Reset state is 00000000h.

ADDR: 8018h **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	TLM Synchronizing Word

CCM Serial I/F TLM Port Sync Register: This is the 32-bit Synch Word for the TLM Port. When configured for Sync Mode the TLM Port will compare the incoming data stream and begin storing data when the Sync Word is detected. A write to this address loads the Sync Word into the Register. A read from this address returns the contents of the Register. The Power-up / Reset state is 00000000h.

ADDR: 801Ch **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	TLM Port FIFO #1

CCM Serial I/F TLM Port FIFO #1: This is the #1 63x32-bit FIFO for the TLM Port. A write to this address loads a word into the FIFO. A read from this address returns the contents of the FIFO. Reading the FIFO when it is empty will return the last value read. The Power-up / Reset state is TLM FIFO #1 Empty.

ADDR: 8020h **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	TLM Port FIFO #2

CCM Serial I/F TLM Port FIFO #2: This is the #2 63x32-bit FIFO for the TLM Port. A write to this address loads a word into the FIFO. A read from this address returns the contents of the FIFO. Reading the FIFO when it is empty will return the last value read. The Power-up / Reset state is TLM FIFO #2 Empty.

ADDR: 8024h **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	TLM Port FIFO #3

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CCM Serial I/F TLM Port FIFO #3: This is the #3 63x32-bit FIFO for the TLM Port. A write to this address loads a word into the FIFO. A read from this address returns the contents of the FIFO. Reading the FIFO when it is empty will return the last value read. The Power-up / Reset state is TLM FIFO #3 Empty.

32-BIT REGISTER DESCRIPTION

ADDR: 8028h **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	TLM Port FIFO #4

CCM Serial I/F TLM Port FIFO #4: This is the #4 63x32-bit FIFO for the TLM Port. A write to this address loads a word into the FIFO. A read from this address returns the contents of the FIFO. Reading the FIFO when it is empty will return the last value read. The Power-up / Reset state is TLM FIFO #4 Empty.

ADDR: 802Ch **Read / Write**

BIT	MSB 31-0 LSB
FUNCTION	Status Port #1 Shift Register

CCM Serial I/F Status Port #1 Shift Register: This is the 32-bit Shift Register for Status Port#1. A write to this address loads a word into the Shift Register. A read from this address returns the contents of the Shift Register. The Power-up / Reset state is 00000000h.

ADDR: 8030h **Read / Write**

BIT	31-16	15-0
FUNCTION	Status Port #2 Data 2	Status Port #2 Data 1

CCM Serial I/F Status Port #2 Shift Register: This Register holds the two 16-bit Data Words for the Status Port #2. A write to this address loads a word into the Shift Register. A read from this address returns the contents of the Shift Register. The Power-up / Reset state is 00000000h.

Either or both Port Data words can be configured with a single 32-bit write operation. Care must be taken when a Data word is written in order to prevent unintended modification of the other Data Word. In order to preserve the Data that you do not want to alter, perform the following sequence of operations:

1. Read the CCM Serial I/F Status Port #2 Shift Register and save the register contents.
2. Modify the copy of the CCM Serial I/F Status Port #2 Shift Register by setting only the Data word desired.
3. Write the new value back to the CCM Serial I/F Status Port #2 Shift Register.

ADDR: 8030h **Read / Write**

BIT	31-16	15-0
FUNCTION	Status Port #2 Data 2	Status Port #2 Data 1

CCM Serial I/F Status Port #2 Shift Register: Status Port #2 Data 1

Bit 15-0 - Status Port #2 Data 1: (Default = 0000h)
This is the #1 16-bit Data word for Status Port #2. Once written, the word will be shifted out each time the Status Port #2 Clock and Enable are received.

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32-BIT REGISTER DESCRIPTION

ADDR: 8030h **Read / Write**

BIT	31-16	15-0
FUNCTION	Status Port #2 Data 2	Status Port #2 Data 1

CCM Serial I/F Status Port #2 Shift Register: Status Port #2 Data 2

Bit 31-16 - Status Port #2 Data 2: (Default = 0000h)

This is the #2 16-bit Data word for Status Port #2. Once written, the word will be shifted out each time the Status Port #2 Clock and Enable are received.

ADDR: 8034h **Read / Write**

BIT	MSB 23-0 LSB
FUNCTION	GPS Port Clock Skew

CCM Serial I/F GPS Port Clock Skew Register: This is the 24-bit Register for GPS Port Clock Skew control. A write to this address loads a word into the Clock Skew Register. A read from this address returns the contents of the Clock Skew Register. Each Skew increment is 1μS and is entered in decimal format (valid states for each 4-bit digit are 0-9). For example if you want a 700μS Skew between the GPS_CLK1 and GPS_CLK2 outputs you would write 000700h into the Clock Skew Register. Values of 000000h and 000001h yield the minimum 1μS Skew. The maximum value is 499999h which yields a 499.999mS Skew. The Power-up / Reset state is 00000000h.

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CCM Serial I/F Self Test

There are two methods of Self Test for the 3000-514 CCM Serial I/F: Internal, and External. The Internal Self Test verifies all circuit functionality up to, but excluding the Differential Drivers and Receivers. It is performed in the VXI Mainframe utilizing software only, and requires no external connections to the CCM Serial I/F Drivers and Receivers (at J1 and J2). The External Self Test performs similar functional testing, but requires the external connection of the appropriate CCM Serial I/F Drivers and Receivers (at J1 and J2). Both the Internal and External Self Test Procedures are described for each of the six CCM Serial I/F Ports in the following section.

CMD Port Internal Self Test:

Verifies the functionality of the CMD State Machine, CMD FIFO, and CMD Shift Register.

1. Configure the CMD Port for normal operation (default)
   - Primary, MSB first, 2Khz, 32-bit word, DRDY = Enable, F3=0, Pass=0, Fail=0
2. Load test words into the CMD FIFO
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
3. Configure TLM Port for CMD Port Self Test operation
   - Primary, MSB first, Gated Mode, 32-bit word, Clk=CMD, Gate=CMD, Data=CMD
4. Enable the CMD State Machine
5. Verify the Words in the TLM FIFO
6. Repeat steps 2-5 with the CMD Port configured for LSB operation

CMD Port External Self Test:

Verifies the functionality of the CMD State Machine, CMD FIFO, and CMD Shift Register, CMD Drivers and Receivers, and the CMD Handshake lines.

1. Jumper the Primary CMD Clock / Data outputs to the Primary TLM Clock / Data inputs.
2. Jumper the Redundant CMD Clock / Data outputs to the Redundant TLM Clock / Data inputs.
3. Jumper the Primary CMD F3Flag output to the Primary CMD PT_DIN input (invert F3Flag output by swapping the ±).
4. Jumper the Redundant CMD F3Flag output to the Redundant CMD PT_DIN input (invert F3Flag output by swapping the ±).
5. Configure the CMD Port as follows:
   - Primary, MSB first, 2Khz, 32-bit word, DRDY = Enable, Busy=0, F3=0, Pass=0, Fail=0
6. Load test words into the CMD FIFO
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
7. Configure TLM Port for CMD Port Self Test operation
   - Primary, MSB first, Gated Mode, 32-bit word, Clk=External / Rising, Gate=CMD, Data=External
8. Enable the CMD State Machine
9. Verify the Words in the TLM FIFO
10. Repeat steps 6-9 with the CMD Port configured for LSB operation
11. Load A's into the CMD FIFO
12. Connect The Scope to the CMD_SE output
13. Enable the CMD State Machine
14. Verify the Words in the TLM FIFO and check the Data Rate on the Scope
15. Load 5's into the CMD FIFO
16. Connect The Scope to the CMD DataRdy output
17. Initialize the CMD Port Inter-Word delay to 1us
18. Enable the CMD State Machine
19. Verify the Words in the TLM FIFO and verify the Inter-Word delay on the Scope
20. Repeat steps 15-20 for the Busy output
21. Connect the F3Flag output to the Scope and verify static operation
22. Connect the Pass output to the Scope and verify static operation
23. Connect the Fail output to the Scope and verify static operation
24. Reconfigure the CMD Port for Primary inputs and toggle the F3Flag Low and then High
25. Read the Status Register to verify that the PT_DIN Flag is set
26. Read the Status Register to verify that the PT_DIN Flag is clear
27. Repeat steps 6-27 for the Redundant side

Data Port Internal Self Test:

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Verifies the functionality of the Data State Machine, Data FIFO, and Data Shift Register.

1. Configure the Data Port for normal operation (default)
   - Primary, MSB first, 2Khz, 64-bit word
2. Load test words into the Data FIFO
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
3. Configure TLM Port for Data Port Self Test operation
   - Primary, MSB first, Gated Mode, 64-bit word, Clk=Data, Gate=Data, Data=Data
4. Enable the Data State Machine
5. Verify the Words in the TLM FIFO
6. Repeat steps 2 -5 with the Data Port configured for LSB operation
7. Repeat steps 2 -5 with the Data Port configured for 32-bit operation

Data Port External Self Test:

Verifies the functionality of the Data State Machine, Data FIFO, and Data Shift Register, as well as the Data Drivers and Receivers.

1. Jumper the Primary Data Clock / Data outputs to the Primary TLM Clock / Data inputs.
2. Jumper the Redundant Data Clock / Data outputs to the Redundant TLM Clock / Data inputs.
3. Jumper the Primary CMD F3Flag output to the Primary EOM_RS input (invert F3Flag output by swapping the ±).
4. Jumper the Redundant CMD F3Flag output to the Redundant EOM_RS input (invert F3Flag output by swapping the ±).
5. Configure the Data Port as follows:
   - Primary, MSB first, 2Khz, 64-bit word
6. Load test words into the Data FIFO
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
7. Configure TLM Port for Data Port Self Test operation
   - Primary, MSB first, Gated Mode, 32-bit word, Clk=External / Rising, Gate=Data, Data=External
8. Enable the Data State Machine
9. Verify the Words in the TLM FIFO
10. Repeat steps 6-9 with the Data Port configured for LSB operation
11. Repeat steps 6-9 with the Data Port configured for 32-bit operation
12. Disable the Data State Machine and load some dummy words into the Data FIFO
13. Reconfigure the Data Port for Primary inputs and toggle the F3Flag Low and then High
14. Read the Status Register to verify that the EOM_RS Flag is set and the Data FIFO is empty
15. Read the Status Register to verify that the EOM_RS Flag is clear
16. Repeat steps 6-15 with the Data and TLM Ports configured for Redundant operation

Note: During 64-bit Data Port Self Test (Gated 64-Bit Mode) the TLM Port will store twelve 64-bit Words, in the form of twenty four 32-bit words, in each TLM FIFO.

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TLM Port Internal Self Test:

Verifies the functionality of the TLM State Machine, TLM Shift Registers, TLM Comparator, and TLM FIFO's.

1. Configure the CMD Port as follows:
   - Primary, MSB first, 32Khz, 32-bit word, DRDY = Enable, F3=0, Pass=0, Fail=0
2. Enable VXI Interrupts
3. Load 25 test words into the CMD FIFO
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
4. Configure TLM Port for TLM Port Self Test operation
   - Primary, MSB first, Free Mode, 32-bit word, Clk=CMD, Gate=CMD, Data=CMD
5. Enable the CMD State Machine
6. Verify that a VXI Interrupt has occurred
7. Read the Status Register and verify that the TLM FIFO Status Flag is set
8. Read the Status Register and verify that the TLM FIFO Status Flag is clear
9. Verify the Words in the TLM FIFO
10. Repeat steps 2-5 with the TLM Port configured for LSB operation
11. Initalize the Sync Word Register
12. Load some dummy words into the CMD FIFO
13. Load the Sync Word into the CMD FIFO
14. Load 24 test words into the CMD FIFO
15. Configure TLM Port for TLM Port Self Test operation
    - Primary, MSB first, Sync Mode, 32-bit word, Clk=CMD, Gate=CMD, Data=CMD
16. Enable the CMD State Machine
17. Verify that a VXI Interrupt has occurred
18. Read the Status Register and verify that the TLM FIFO Status Flag is set
19. Read the Status Register and verify that the TLM FIFO Status Flag is clear
20. Verify the Words in the TLM FIFO
21. Repeat steps 2-20 with the TLM Port configured for LSB

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TLM Port External Self Test:

Verifies the functionality of the TLM State Machine, the TLM Shift Register, the TLM Comparator, the TLM FIFO's, and TLM Drivers and Receivers.

1. Jumper the Primary CMD Clock / Data outputs to the Primary TLM Clock / Data inputs.
2. Jumper the Redundant CMD Clock / Data outputs to the Redundant TLM Clock / Data inputs.
3. Configure the CMD Port as follows:
   - Primary, MSB first, 32Khz, 32-bit word, DRDY = Enable, F3=0, Pass=0, Fail=0
4. Enable VXI Interrupts
5. Load 25 test words into the CMD FIFO
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
6. Configure TLM Port for TLM Port Self Test operation
   - Primary, MSB first, Free Mode, 32-bit word, Clk=CMD, Gate=CMD, Data=CMD
7. Enable the CMD State Machine
8. Verify that a VXI Interrupt has occurred
9. Read the Status Register and verify that the TLM FIFO Status Flag is set
10. Read the Status Register and verify that the TLM FIFO Status Flag is clear
11. Verify the Words in the TLM FIFO
12. Repeat steps 2-5 with the TLM Port configured for LSB operation
13. Initalize the Sync Word Register
14. Load some dummy words into the CMD FIFO
15. Load the Sync Word into the CMD FIFO
16. Load 24 test words into the CMD FIFO
17. Configure TLM Port for TLM Port Self Test operation
    - Primary, MSB first, Sync Mode, 32-bit word, Clk=CMD, Gate=CMD, Data=CMD
18. Enable the CMD State Machine
19. Verify that a VXI Interrupt has occurred
20. Read the Status Register and verify that the TLM FIFO Status Flag is set
21. Read the Status Register and verify that the TLM FIFO Status Flag is clear
22. Verify the Words in the TLM FIFO
23. Repeat steps 4-22 with the TLM Port configured for LSB
24. Repeat steps 4-23 with the CMD and TLM Ports configured for Redundant operation

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SP1 Internal Self Test:

Verifies the functionality of the SP1 Shift Register.

1. Configure the CMD Port as follows:
   - Primary, MSB first, 1.024Mhz, 32-bit word, DRDY = Enable, F3=0, Pass=0, Fail=0
2. Load a dummy word into the CMD FIFO
3. Load a test word into the SP1 Shift Register
4. Configure TLM Port for SP1 Port Self Test operation
   - Primary, MSB first, Gated Mode, 32-bit word, Clk=CMD, Gate=CMD, Data=SP1
5. Enable the CMD State Machine
6. Verify the Word in the TLM FIFO
7. Repeat steps 2 -5 with different test words.
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
8. Repeat steps 2 -5 with the SP1 Port configured for LSB operation.

SP1 Port External Self Test:

Verifies the functionality of the SP1 Shift Register and SP1 Drivers and Receivers.

1. Jumper the Primary CMD Clock / Enable outputs to the Primary SP1 Clock (invert clock by swapping the ±) / Enable inputs.
2. Jumper the Redundant CMD Clock / Enable outputs to the Redundant SP1 Clock (invert clock by swapping the ±) / Enable inputs.
3. Jumper the Primary SP1 Data 1 outputs to the Primary TLM Data inputs.
4. Jumper the Redundant SP1 Data 1 outputs to the Redundant TLM Data inputs.
5. Configure the CMD Port as follows:
   - Primary, MSB first, 1.024Mhz, 32-bit word, DRDY = Enable, Busy=0, F3=0, Pass=0, Fail=0
6. Load a dummy word into the CMD FIFO
7. Load a test word into the SP1 Shift Register
8. Configure TLM Port for SP1 Port Self Test operation
   - Primary, MSB first, Gated Mode, 32-bit word, Clk=CMD, Gate=CMD, Data=External
9. Enable the CMD State Machine
10. Verify the word in the TLM FIFO
11. Repeat steps 5-10 with different test words
    - A's, 5's, 3's, C's, Walking 1's, Walking 0's
12. Repeat steps 5-11 with the SP1 Port configured for LSB operation
13. Repeat steps 5-12 with the SP1 Port configured for Redundant operation

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SP2 Internal Self Test:

Verifies the functionality of the SP2 Shift Register.

1. Configure the CMD Port for normal operation
   - Primary, MSB first, 1.024Mhz, 16-bit word, DRDY = Enable, F3=0, Pass=0, Fail=0
2. Load a dummy word into the CMD FIFO
3. Load a test word into the lower 16-bits of the SP2 Shift Register
4. Configure TLM Port for SP2 Port Self Test operation
   - Primary, MSB first, Gated Mode, 16-bit word, Clk=CMD, Gate=CMD, Data=SP2 Data 1
5. Enable the CMD State Machine
6. Verify the Word in the TLM FIFO
7. Repeat steps 2-6 with different test words.
   - A's, 5's, 3's, C's, Walking 1's, Walking 0's
8. Repeat steps 2-7 with the SP1 Port configured for LSB operation.
9. Load a dummy word into the CMD FIFO
10. Load a test word into the upper 16-bits of the SP2 Shift Register
11. Configure TLM Port for SP2 Port Self Test operation
    - Primary, MSB first, Gated Mode, 16-bit word, Clk=CMD, Gate=CMD, Data=SP2 Data 2
12. Enable the CMD State Machine
13. Verify the Word in the TLM FIFO
14. Repeat steps 9-13 with different test words.
    - A's, 5's, 3's, C's, Walking 1's, Walking 0's
15. Repeat steps 9-14 with the SP1 Port configured for LSB operation.

SP2 Port External Self Test:

Verifies the functionality of the SP2 Shift Register and SP2 Drivers and Receivers.

1. Jumper the Primary CMD Clock / Enable outputs to the Primary SP2 Clock (invert clock by swapping the ±) / Enable inputs.
2. Jumper the Redundant CMD Clock / Enable outputs to the Redundant SP2 Clock (invert clock by swapping the ±) / Enable inputs.
3. Jumper the Primary SP2 Data 1 outputs to the Primary TLM Data inputs.
4. Jumper the Redundant SP2 Data 1 outputs to the Redundant TLM Data inputs.
5. Configure the CMD Port as follows:
   - Primary, MSB first, 1.024Mhz, 16-bit word, DRDY = Enable, Busy=0, F3=0, Pass=0, Fail=0
6. Load a dummy word into the CMD FIFO
7. Load a test word into the lower 16-bits of the SP2 Shift Register
8. Configure TLM Port for SP2 Port Self Test operation
   - Primary, MSB first, Gated Mode, 16-bit word, Clk=CMD, Gate=CMD, Data=External
9. Enable the CMD State Machine
10. Verify the word in the TLM FIFO
11. Repeat steps 5-10 with different test words
    - A's, 5's, 3's, C's, Walking 1's, Walking 0's
12. Repeat steps 5-11 with the SP1 Port configured for LSB operation
13. Repeat steps 5-12 with the SP1 Port configured for Redundant operation
14. Jumper the Primary SP2 Data 2 outputs to the Primary TLM Data inputs.
15. Jumper the Redundant SP2 Data 2 outputs to the Redundant TLM Data inputs.
16. Load a dummy word into the CMD FIFO
17. Load a test word into the lower 16-bits of the SP2 Shift Register
18. Configure TLM Port for SP2 Port Self Test operation
    - Primary, MSB first, Gated Mode, 16-bit word, Clk=CMD, Gate=CMD, Data=External
19. Enable the CMD State Machine
20. Verify the word in the TLM FIFO
21. Repeat steps 16-20 with different test words
    - A's, 5's, 3's, C's, Walking 1's, Walking 0's
22. Repeat steps 16-21 with the SP2 Port configured for LSB operation
23. Repeat steps 16-22 with the SP2 Port configured for Redundant operation

Note: During SP2 Self Test (Gated 16-Bit Mode) the direction determines which half of the 32-bit word to mask when reading the TLM FIFO. If the TLM Shift Register is configured for MSB first, the upper 16-bits of each word

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stored in the TLM FIFO should be masked. If the TLM Shift Register is configured for LSB first, the lower 16-bits of each word stored in the TLM FIFO should be masked.

GPS Port External Self Test:

Verifies the functionality of the GPS Clock Generators and GPS Drivers.

1. Connect the Scope to the GPS Clock outputs.
2. Enable the GPS Drivers.
3. Configure the GPS Clock Skew for 1uS.
4. Verify the Skew on the Scope.
5. Repeat steps 3-4 for various skew values:
    - 10uS, 100uS, 1mS, 10mS, 100mS, 499.999mS

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CCM Serial I/F CONNECTOR SIGNAL ASSIGNMENT

(Module Front View)

J1	J2	PIN	
CHASSIS	CHASSIS	78	•
CP_BUSY+	CR_BUSY+	77	•
CP_F3+	CR_F3+	76	•
CP_F3-	CR_F3-	75	•
CP_PASS+	CR_PASS+	74	•
CP_FAIL+	CR_FAIL+	73	•
CP_FAIL-	CR_FAIL-	72	•
EOMP_RS+	EOMR_RS+	71	•
DP_DATA+	DR_DATA+	70	•
DP_DATA-	DR_DATA-	69	•
TP_DATA+	TR_DATA+	68	•
TLM_SE	NC	67	•
S1P_DAT+	S1R_DAT+	66	•
SP1_SE	NC	65	•
S2P_CLK+	S2R_CLK+	64	•
S2P_DAT2+	S2R_DAT2+	63	•
SP2_SE2	NC	62	•
GP_CLK2+	GR_CLK2+	61	•
CHASSIS	CHASSIS	60	•

J1	J2	PIN	
CHASSIS	CHASSIS	59	•
SHIELD	SHIELD	58	•
CP_BUSY-	CR_BUSY-	57	•
SHIELD	SHIELD	56	•
SHIELD	SHIELD	55	•
CP_PASS-	CR_PASS-	54	•
SHIELD	SHIELD	53	•
CMD_SE	NC	52	•
EOMP_RS-	EOMR_RS-	51	•
SHIELD	SHIELD	50	•
DATA_SE	NC	49	•
TP_DATA-	TR_DATA-	48	•
SHIELD	SHIELD	47	•
S1P_DAT-	S1R_DAT-	46	•
S2P_CLK-	S2R_CLK-	45	•
SHIELD	SHIELD	44	•
S2P_DAT2-	S2R_DAT2-	43	•
SHIELD	SHIELD	42	•
GP_CLK2-	GR_CLK2-	41	•
CHASSIS	CHASSIS	40	•

J1	J2	PIN	
CHASSIS	CHASSIS	39	•
PTP_DIN-	PTR_DIN-	38	•
SHIELD	SHIELD	37	•
SHIELD	SHIELD	36	•
CP_EN-	CR_EN-	35	•
SHIELD	SHIELD	34	•
SHIELD	SHIELD	33	•
CP_DRDY-	CR_DRDY-	32	•
SHIELD	SHIELD	31	•
SHIELD	SHIELD	30	•
DP_EN-	DR_EN-	29	•
TP_CLK-	TR_CLK-	28	•
S1P_CLK-	S1R_CLK-	27	•
S1P_EN-	S1R_EN-	26	•
S2P_EN-	S2R_EN-	25	•
SHIELD	SHIELD	24	•
SP2_SE1	NC	23	•
SHIELD	SHIELD	22	•
CHASSIS	CHASSIS	21	•

J1	J2	PIN	
CHASSIS	CHASSIS	20	•
PTP_DIN+	PTR_DIN+	19	•
CP_CLK+	CR_CLK+	18	•
CP_CLK-	CR_CLK-	17	•
CP_EN+	CR_EN+	16	•
CP_DATA+	CR_DATA+	15	•
CP_DATA-	CR_DATA-	14	•
CP_DRDY+	CR_DRDY+	13	•
DP_CLK+	DR_CLK+	12	•
DP_CLK-	DR_CLK-	11	•
DP_EN+	DR_EN+	10	•
TP_CLK+	TR_CLK+	9	•
S1P_CLK+	S1R_CLK+	8	•
S1P_EN+	S1R_EN+	7	•
S2P_EN+	S2R_EN+	6	•
S2P_DAT1+	S2R_DAT1+	5	•
S2P_DAT1-	S2R_DAT1-	4	•
GP_CLK1+	GR_CLK1+	3	•
GP_CLK1-	GR_CLK1-	2	•
CHASSIS	CHASSIS	1	•

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ASCOR
MODEL 3000-514

CCM SERIAL I/F

PROGRAMMING GUIDE

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ASCOR 3000-514 CCM Serial I/F Register Programming

The ASCOR 3000-514 CCM Serial I/F is a Register-Based VXI Module with registers in both the A16 and A32 Address Spaces. The A16 Address Space contains the VXI Device Registers, which are 16-bit registers defined by the VXI Specification. See pages 7-14 for a description of the contents of the Device Registers. See pages 45-49 for Device Register programming Examples. The A32 Address Space contains the CCM Serial I/F Registers. See pages 24-36 for a description of the contents of the CCM Serial I/F Registers. See pages 50-51 for CCM Serial I/F Register programming Examples.

Programming VXI Device Registers

The ASCOR 3000-514 CCM Serial I/F VXI Device Registers are read / write registers located in the A16 Address Space. Some Device Registers must be written only by a Resource Manager. Table 2 lists the VXI Device Registers.

VXI Device Registers for ASCOR 3000-514			
VXI Device Dependent Registers			
Address	**Description**	**Read**	**Write**
3Eh	ASCOR Control Register	Yes	Yes
3Ch	Register Not Used	-	-
3Ah	Register Not Used	-	-
38h	Register Not Used	-	-
36h	Register Not Used	-	-
34h	Register Not Used	-	-
32h	Register Not Used	-	-
30h	Register Not Used	-	-
2Eh	Register Not Used	-	-
2Ch	Register Not Used	-	-
2Ah	Register Not Used	-	-
28h	Register Not Used	-	-
26h	Register Not Used	-	-
24h	Register Not Used	-	-
22h	Register Not Used	-	-
20h	Register Not Used	-	-
VXI Device Class Dependent Registers			
Address	**Description**	**Read**	**Write**
1Eh	Register Not Used	-	-
1Ch	Register Not Used	-	-
1Ah	Register Not Used	-	-
18h	Register Not Used	-	-
16h	Register Not Used	-	-
14h	Register Not Used	-	-
12h	Register Not Used	-	-
10h	Register Not Used	-	-
0Eh	Register Not Used	-	-
0Ch	Register Not Used	-	-
0Ah	Register Not Used	-	-
08h	Register Not Used	-	-
VXI Configuration Registers			
Address	**Description**	**Read**	**Write**
06h	Offset Register	Yes	Res. Man. Only
04h	Status / Control Register	Yes	Yes
02h	Device Type Register	Yes	Res. Man. Only
00h	ID / Logical Address Register	Yes	Res. Man. Only

Table 2: 3000-514 Device Registers

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Programming VXI Device Registers (Continued)

Since all 16 bits of the Device Register are programmed with a single write operation, care must be taken when values are written to the Device Registers in order to prevent unintended function enabling or disabling. In order to preserve the states of the functions that you do not want to alter, perform the following sequence of operations:

1. Read the Device Register first,
2. Modify only the bits you intend to program using the copy of the Device Register,
3. Write the new value back to the Device Register.

Here are some example codes for reading the ID Register of the 3000-514 Module.

Example using National Instruments NI-VXI calls with the Logical Address of 5

```
/* C code segment for reading the ID Register using VXIinReg call.*/

         int16   ret;
         uint16  la          = 5;   /* Logical Address */
         uint16  reg         = 0;   /* ID Register offset */
         uint16  value16;

         /* Read the ID Register */
         ret = VXIinReg (la, reg, &value16);

         /* Check for read error */
         if (ret < 0)
                /* Error occurred during read. */;

/* C code segment for reading the ID Register using VXIin call. */

         int16   ret;
         uint16  accessparms= 1;      /* A16, Nonprivileged data access, Motorola Byte Order */
         uint32  address    = 0xC140; /* LA * 0x40 + 0xC000 + ID Register offset */
         uint16  width      = 2;      /* 16-bit word */
         uint16  value16;

         /* Read the ID Register */
         ret = VXIin (accessparms, address, width, &value16);

         /* Check for read error */
         if (ret < 0)
                /* Error occurred during read. */;
```

Example using VXI*plug&play* VISA calls

```
/* C code segment for reading the ID Register using ViIn16 call. */

         ViStatus            as3xxx_status;
         ViSession    vi;            /* vi from previous call to as3xxx_init */
         ViUInt16            space   = VI_A16_SPACE;
         ViBusAddress offset  = 0x00; /* Offset of the ID Register */
         ViUInt16            val16;

         /* Read the ID Register */
         as3xxx_status = viIn16 (vi, space, offset, &val16);

         /* Check for read error */
         if (as3xxx_status < VI_SUCCESS)
                /* Error occurred during read. */;
```


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Resetting ASCOR VXI Module

The ASCOR 3000-514 CCM Serial I/F VXI Module can be reset to a power up state by setting the Device Reset bit in the Status / Control (04h) register in the VXI Configuration Registers. Care must be taken when writing to this register since all bits other than the Device Reset bit must not be changed. In order to preserve the states of all other bits, perform the following sequence of operations:

1. Read the Status / Control register,
2. Set only the Device Reset bit,
3. Write the modified word to the Status / Control register.

After the reset operation, the module must be brought back to a normal operational mode. The 3000-514 Module can be set back to the normal operation mode by clearing the Device Reset bit without modifying any other bits.

Here are some example codes for resetting the 3000-514 Module.

Example using National Instruments NI-VXI calls with the Logical Address of 5

```
/* C code segment for resetting the ASCOR VXI module using VXIinReg and VXIoutReg calls */

        int16   ret;
        uint16  la          = 5;   /* Logical Address */
        uint16  reg         = 4;   /* Status / Control register offset */
        uint16  value16;

        /* Read the Status / Control Register */
        ret = VXIinReg (la, reg, &value16);

        /* Check for read error */
        if (ret < 0)
               /* Error occurred during read. */;


        /* Set the Device Reset bit in the copy of the Status / Control Register */
        value16 |= 0x0001;


        /* Write to the Status / Control Register */
        ret = VXIoutReg (la, reg, value16);

        /* Check for write error */
        if (ret < 0)
               /* Error occurred during write. */;


        /* Bring the module back to the normal operation by
          clearing the Device Reset bit in the copy of the Status / Control Register */
        value16 &= 0xFFFE;


        /* Write to the Status / Control Register */
        ret = VXIoutReg (la, reg, value16);

        /* Check for write error */
        if (ret < 0)
               /* Error occurred during write. */;
```


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3000-514 Reset Programming Example using National Instruments NI-VXI Calls (Continued)

```
/* C code segment for resetting the ASCOR VXI module using VXIin and VXIout calls */

        int16   ret;
        uint16  accessparms= 1;      /* A16, Nonprivileged data access, Motorola Byte Order */
        uint32  address    = 0xC144; /* LA * 0x40 + 0xC000 + Control / Status Register */
        uint16  width      = 2;      /* Word */
        uint16  value16;
        uint32  value32;

        /* Read the Status / Control Register */
        ret = VXIin (accessparms, address, width, &value16);

        /* Check for read error */
        if (ret < 0)
               /* Error occurred during read. */;

        /* Set the Device Reset bit in the copy of the Status / Control Register */
        value32 = value16;
        value32 |= 0x0001;


        /* Write to the Status / Control Register */
        ret = VXIout (accessparms, address, width, value32);

        /* Check for write error */
        if (ret < 0)
               /* Error occurred during write. */;


        /* Bring the module back to the normal operation by
          clearing the Device Reset bit in the copy of the Status / Control Register */
        value32 &= 0xFFFE;


        /* Write to the Status / Control Register */
        ret = VXIout (accessparms, address, width, value32);

        /* Check for write error */
        if (ret < 0)
               /* Error occurred during write. */;
```


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3000-514 Reset Programming Example using VXI*plug&play* VISA Calls

```
/* C code segment for resetting the ASCOR VXI Module */

        ViStatus            as3xxx_status;
        ViSession    vi;            /* vi from previous call to as3xxx_init */
        ViUInt16            space   = VI_A16_SPACE;
        ViBusAddress offset  = 0x04; /* Offset of the Status / Control Register */
        ViUInt16            value16;

        /* Read the Status / Control Register */
        as3xxx_status = viIn16 (vi, space, offset, &value16);

        /* Check for read error */
        if (as3xxx_status < VI_SUCCESS)
               /* Error occurred during read. */;


        /* Set the Device Reset bit in the copy of the Status / Control Register */
        value16 |= 0x0001;


        /* Write to the Status / Control Register */
        as3xxx_status = viOut16 (vi, space, offset, value16);

        /* Check for write error */
        if (as3xxx_status < VI_SUCCESS)
               /* Error occurred during write. */;


        /* Bring the module back to the normal operation by
          clearing the Device Reset bit in the copy of the Status / Control Register */
        value16 &= 0xFFFE;


        /* Write to the Status / Control Register */
        as3xxx_status = viOut16 (vi, space, offset, value16);

        /* Check for write error */
        if (as3xxx_status < VI_SUCCESS)
               /* Error occurred during write. */;
```


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ASCOR 3000-514 CCM Serial I/F Registers

The ASCOR 3000-514 CCM Serial I/F Registers are located in the A32 address space and are accessed only in 32-bit mode. The method of accessing the Registers in the A32 address space is different from accessing the VXI Device Registers in the A16 address space. Therefore, care must be taken whenever accessing registers that are located in different address spaces.

Offset Address in 32-Bit Mode

The 3000-514 Registers start at offset 8000h within the A32 address space assigned by the Resource Manager. Address offsets for the registers increment by four (4). Table 3 lists the 3000-514 Registers. Pages 24-36 describe the contents of these registers.

ADDRESS	SIZE	TYPE	DESCRIPTION
8000h	32 bit	R/W	CCM Serial I/F Control Register
8004h	32 bit	R	CCM Serial I/F Status Register
8008h	32 bit	R/W	CCM Serial I/F CMD FIFO
800Ch	32 bit	R/W	CCM Serial I/F CMD/Data Word Delay Register
8010h	32 bit	R/W	CCM Serial I/F Data FIFO
8014h	32 bit	R/W	CCM Serial I/O TLM Shift Register
8018h	32 bit	R/W	CCM Serial I/F TLM Sync Word Register
801Ch	32 bit	R/W	CCM Serial I/F TLM FIFO #1
8020h	32 bit	R/W	CCM Serial I/F TLM FIFO #2
8024h	32 bit	R/W	CCM Serial I/F TLM FIFO #3
8028h	32 bit	R/W	CCM Serial I/F TLM FIFO #4
802Ch	32 bit	R/W	CCM Serial I/F Status Port 1 Register
8030h	32 bit	R/W	CCM Serial I/F Status Port 2 Register
8034h	24 bit	R/W	CCM Serial I/F GPS Clock Skew Register

Table 3: 3000-514 Registers

Programming ASCOR 3000-514 CCM Serial I/F Registers in A32 Mode

A unique A32 base address is assigned by the Resource Manager to the A32 module in the system. The assignment of the base address is performed every time the Resource Manager is executed. ASCOR 3000-514 Registers start at an offset of 8000h from the module's assigned A32 base address. The sum of the two values, A32 base address and the register offset, gives the unique register address. Some interface library calls require the A32 register address. VXI*plug&play* library calls require only the offset of the register from the A32 base address. The A32 base address is added to the offset internally.

Here are some example codes for writing to the 3000-514 registers.

Example using National Instruments NI-VXI calls

```
/* C code segment for writing the value 0x10000000 to the first register,
  assume A32 Base Address of 20000000h */

        int16   ret;
        uint16  accessparms= 3;   /* A32, Nonprivileged data access, Motorola Byte Order */
        uint32  address;
        uint16  width      = 4;   /* Longword */
        uint32  value32;

        address = 0x20008000;     /* A32 Base Address + first register offset */
        value32 = 0x10000000;     /* Value to write to the first register */

        /* Write to the first register */
        ret = VXIout (accessparms, address, width, value32);

        /* Check for write error */
        if (ret < 0)
                /* Error occurred during write. */;
```


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Example using VXI*plug&play* VISA calls

```
/* C code segment for writing the value 0x10000000 to the first register */

         ViStatus            as3xxx_status;
         ViSession    vi;
         ViUInt16            space   = VI_A32_SPACE;
         ViBusAddress offset  = 0x8000;      /* Offset of the first register */
         ViUInt32            value32;

         value32 = 0x10000000;/* Value to write to the first register */

         /* Write to the first register */
         as3xxx_status = viOut32 (vi, space, offset, value32);

         /* Check for write error */
         if (as3xxx_status < VI_SUCCESS)
                /* Error occurred during write. */;
```


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Miscellaneous Questions and Answers

Q: How do I calculate the 3000-514 Module's A16 Base Address?

A: The A16 Base Address of the 3000-514 is derived from the Logical Address. The formula for calculating the A16 Base Address is as follows:

A16 Base Address = C000h + LA x 40h

where LA is the Logical Address of a module

Logical Address	A16 Base Address
1	C040h
2	C080h
3	C0C0h
4	C100h
5	C140h

and so on . . .

If the module's Logical Address is 5 then A16 Base Address is C140h and Device Register addresses are as follows:

Address	Device Registers
C140h	ID Register / Logical Address Register
C142h	Device Type Register
C144h	Status / Control Register
C146h	Offset Register
C17Eh	Control Register

If the module's Logical Address is 8 then A16 Base Address is C200h and Device Register addresses are as follows:

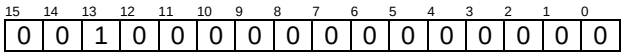
Address	Device Registers
C200h	ID Register / Logical Address Register
C202h	Device Type Register
C204h	Status / Control Register
C206h	Offset Register
C23Eh	Control Register

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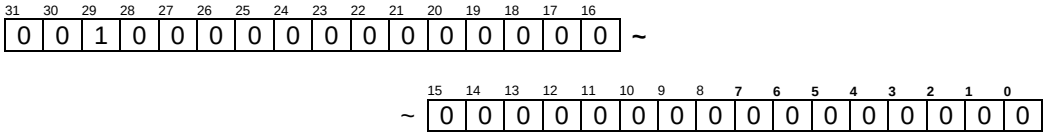
Q: How do I Get the Module's A32 Base Address

A: The A32 Base Address of a VXI module can be derived from the value stored in the Offset Register (06h). To obtain ASCOR VXI Module's A32 base address, take the 16-bits of the Offset register and map them to the 16 most significant bits of the A32 Base Address. All other bits in the A32 Base Address are set to zeroes. This conversion works for the modules whose Required Memory in the Device Type Register (A16 Address Space, Offset 02h) is set to Fh (Bits 12-15).

Offset Register (06h)



A32 Base Address



Following are some examples of the Offset Register Values and the corresponding A32 Base Addresses.

Offset Register Values	**Derived A32 Base Addresses**
2000h	20000000h
3000h	30000000h
7000h	70000000h

Alternatively, A32 Base Address of a device can be obtained by issuing a library call.

Example using National Instruments NI-VXI calls with the Logical Address of 5

```
/* C code segment for obtaining the device's A32 Base Address */

        int16   ret;
        uint16  la          = 5;   /* Logical Address */
        uint16  field       = 12;  /* Base of A24/A32 address space */
        uint32  baseA32;

        /* Get the A32 Base Address */
        ret = GetDevInfo (la, field, &baseA32);

        /* Check for function error */
        if (ret < 0)

              /* Error occurred during GetDevInfo. */;
```


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