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Graphic Strategies, Inc.

VME Colorgraphic Display Controller Board

VGME-34010

Hardware Reference Manual

Part Number #0800-10000

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549 East Weddell Drive, Sunnyvale, California 94089-2114 Tel 408·745·6500 WATS 800·336·2733 FAX 408·744·0235

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1.0 Introduction

The VGME-34010 is a single board graphics controller for the VME bus. It is based on the Texas Instruments TMS34010 Graphics System Processor (GSP). The VGME-34010 can control displays with resolutions up to 1280 x 1024 pixels using 256 colors out of a palette of more than 16.7 million. In addition to up to two megabytes of video frame buffer memory, the VGME-34010 can also have two megabytes of dynamic memory for programs, data, fonts, images, etc. All of this memory is directly accessible to both the 34010 GSP and as a slave to the VME bus in A24 and A32 modes.

The VGME-34010 provides standard RS-343A or RS-170 compatible RGB outputs using a Brooktree or equivalent 451/458 triple RAMDAC. A Brooktree or equivalent 431 cursor controller provides hardware control of a user-definable cursor. Both of these parts are accessible to both the 34010 GSP and the VME bus host.

2.0 Architecture

The block diagram for the VGME-34010 is shown on the data sheet at the end of this manual.

2.1 34010 Graphics System Processor

The TMS34010, a 32-bit microprocessor operating at 50 MHz, is the heart of the VGME-34010. Using its 256 byte instruction cache, the TMS34010 results in a greater than six MIPS performance. It executes powerful graphics instructions that perform window checking and boolean and arithmetic operations on the fly on pixels while they are being manipulated during pixel block transfers, line drawing operations, or fill operations.

The 34010 GSP generates the memory control signals for both the video and standard dynamic memories used on board, and also the CRT control signals. The sync and blanking signals are programmable, and can be set to support virtually any display resolution up to 1280 x 1024 pixels, at a depth of 8 bits per pixel. The sync signals are also fed back into the 34010 GSP external interrupt request inputs to provide local real-time clock resources.

The VGME-34010 generates a software programmable vectored interrupt, which is routed to any one of seven software selectable VME interrupt request lines.

2.2 Memory

There are three data busses, one multiplexed address/data bus, and three address busses on the VGME-34010. The 34010 GSP communicates with the VME bus via a 16-bit host interface data bus, D[0-15], which acts as a VME slave. The GSP also has a local memory interface, signals LAD[0-15], which provides address and data signals for on-board memory. During an external memory cycle, the VME address is driven onto these lines, and a state machine PAL emulates the control lines of the 34010 GSP. Both the host interface and the LAD busses are connected via transceivers to the graphics data bus, signals GD[0-31], which is the main data bus for all memory and peripherals on board. The other data bus is the 32-bit display data bus, signals DD[0-31], which provides serial pixel data to the look-up table RAM of the RAMDAC.

The video memory is organized as two banks of 256K words x 32 bits, using dual-port 1 megabit video memories. Processor memory is also implemented in two bank of 256K words x 32 bits using regular dynamic memories. All of this memory is 32 bits, wide permitting longword transfers over the VME bus.

The master pixel clock, which can be as fast as 125 MHz, is divided by four to generate the serial video transfer clock. This signal clocks the shift registers inside the video memories and loads four pixels of data into the RAMDAC where the four bytes are multiplexed into one. The least significant pixel of each longword is displayed as the leftmost of the four pixels, and has the lowest address.

The RAMDAC and the cursor controller also share the graphics data bus, and as they are byte-wide peripherals, only use signals GD[0-7]. For software purposes, they must be viewed as the least significant half of a sixteen bit location. Note that in the memory map, there are different addresses for reading and writing these peripherals.

This was done to speed up data transfers, as the timing requirements for these devices would not permit no-wait state accesses, given the characteristics of the 34010.

All on-board resources are accessible to VME bus masters via the bus request input of the GSP and external cycle control logic. A state machine PAL emulates the 34010 GSP's RAM control signals to allow VME masters to share VGME-34010 memory and to permit fast block transfers to VGME-34010 memory. The video memory and processor memory are mapped to a contiguous block of VME space, in either A24 or A32 modes, and can transfer data in D8, D16, or D32 modes. The host interface registers of the 34010 GSP, the RAMDAC, the cursor controller, and other registers are mapped to a jumper selectable 256 byte block of A16 short I/O space.

In A32 mode, the VGME-34010 will respond to accesses with address modifier codes of 0x09, 0x0a, 0x0b, 0x0d, 0x0e, and 0x0f. In A24 mode, the allowable codes are 0x39, 0x3a, 0x3b, 0x3d, 0x3e, and 0x3f. Address modifier codes 0x29 and 0x2d are recognized in A16 mode.

3.0 Jumpers, Connectors, and Oscillators

The following explanations refer to the diagram labeled "VGME-34010 Jumpers and Connectors" at the end of this manual.

3.1 VME Bus Connectors

The P1 and P2 connectors at the bottom of the diagram are the connections to the VME bus. It is possible to operate the VGME-34010 in a system that has only the P1 connector, but this will limit operation to only 24 address bits and 16 data bits.

3.2 Expansion and Video Connectors

The J1, J2, J10, and J11 connectors at both sides of the VGME-34010 board are for external expansion modules. These are dual row pin headers designed to have a mating connector on an expansion board just plug right on to them. Generally, the J1 and J2 connectors are for the multiplexed high speed video data bus, and the J10 and J11 connectors are for the 34010 GSP related busses.

The J3, J4, J5, J6, and J7 connectors are for the video and sync signal output. J3, J4, and J5 respectively are the red channel, green channel with composite sync, and blue channel, all of which are RS-343A or RS-170 voltage level compatible. J6 and J7 are both at TTL voltage levels and are horizontal sync, and vertical or composite sync, respectively. All 5 of these connectors are the SMA female type connectors which are also used on other products from Graphic Strategies.

J8 and J9 are male DB-9 style connectors for the two RS-232 serial ports. These connectors are directly compatible with most mouse type devices sold for personal computers.

3.3 Jumpers

Jumpers JP1 and JP9 select either a TTL or an ECL type oscillator and are used in combination with other components on the board. These jumpers should not be changed from the factory configuration unless the related components are either added or removed.

JP2 controls DTACK* response time for VMEbus cycles. Having the jumper between pins 1 and 2 sets an 80 nSec delay time, while having the jumper between pins 2 and 3 sets a 60 nSec delay. Normally, this jumper is set between pins 1 and 2.

JP3 is for jumpering the blue video signal from an expansion board. With the jumper on pins 1 and 2, the blue video signal from the onboard RAMDAC is used. Installing the jumper on pins 2 and 3 passes the blue channel from the expansion board.

JP4 has the exact same affect as JP3, except it is for the red video signal.

The jumpers on JP5 set the short I/O address for the VGME-34010 board. When a jumper is installed for any of the 8 address lines, a match will occur when that address line is a logical 0. A jumper not present will match a logical 1. Address line

8 selected by a jumper between pins 1 and 2 of JP5, and address line 15 is selected by a jumper between pins 15 and 16 of JP5.

JP6 selects whether vertical sync or composite sync goes to J7. Setting the jumper between pins 1 and 2 selects vertical sync, while setting the jumper between pins 2 and 3 selects composite sync.

JP7 and JP8 select either the carrier detect signal or the data set ready signal for the two RS-232 ports. Setting the jumper between pins 1 and 2 will select carrier detect, while setting the jumper between pins 2 and 3 will select data set ready. JP7 is for port 1 and JP8 is for port 2.

Jumpers JP10, JP11, and JP12 select either an RS-232 or an inverted TTL interface for serial port number two. With all three jumpers between pins 1 and 2, the TTL interface is enabled, and with all three jumpers between pins 2 and 3, the RS-232 interface is selected. In TTL mode, data transmitted to the VGME-34010 will be on pin 2 and data transmitted from the VGME-34010 will be on pin 3 of serial port #2.

With the proper settings in the serial controller, it is possible to provide an external baud clock for serial port number 2. With the jumper on JP8 between pins 1 and 2, this external clock will be on pin 1, and with the jumper on JP8 between pins 2 and 3, the external clock will be on pin 6.

See the data manual for the 68681 serial controller for the use of the IP2 pin.

Pin 9 of port 2 is connected to VCC to allow the serial device to tap the +5 power supply on the VGME-34010 board.

3.4 Default Jumper Settings

Below is a list of the factory default jumpers for the VGME-34010.

JP1: Jumper installed.
JP2: Jumper installed between pins 1 and 2.
JP3: Jumper installed between pins 1 and 2.
JP4: Jumper installed between pins 1 and 2.
JP5: Jumpers installed between pins 1 and 2, 5 and 6,
7 and 8, 9 and 10, 11 and 12, and 15 and 16.
JP6: Jumper between pins 2 and 3.
JP7: Jumper between pins 2 and 3.
JP8: Jumper between pins 1 and 2.
JP9: Jumper installed.
JP10: Jumper between pins 2 and 3.
JP11: Jumper between pins 2 and 3.
JP12: Jumper between pins 2 and 3.

3.5 Oscillators

The VGME-34010 uses three different oscillator frequencies. One of these oscillators is a single crystal and the other two are metal can type oscillators.

The crystal just on top of the dynamic memories is a fixed 3.6864 MHz crystal used for the 68681 serial controller.

The 50 MHz crystal oscillator located in the corner of the board is the main timebase for the 34010 GSP.

The oscillator shown on the right side of the diagram is the oscillator for the video pixel clock and is the only one of the three that is meant to be changed by the user. It is mounted in a 14 pin DIP socket for this very reason.

The VGME-34010 will accept either an ECL type or a TTL type crystal oscillator for the pixel clock. This is a feature of the VGME-34010 in which the VGME-34010 can support a wide variety of display resolutions. Generally, a pixel clock of less than 60MHz will use a TTL oscillator and greater then 60 MHz will use an ECL oscillator.

TTL oscillators must have VCC, GND, and the output on pins 14, 7, and 8 respectively. Single-ended ECL oscillators must have VEE, GND, and the output on pins 7, 14, and 8 respectively. Differential ECL oscillators must have VEE, GND, and the differential 10KH outputs on pins 7, 14, 1, and 8 respectively.

Differential ECL oscillators will work directly with the Brooktree or equivalent Bt438 clock driver. An additional clock driver circuit must be added to the VGME-34010 when using a single-ended ECL or TTL type oscillator.

4.0 Programming Information

4.1 458/451 RAMDAC

The VGME-34010 can use either the 451 or the 458 RAMDAC for converting 8-bit pixel information into the standard RS-343A RGB outputs. The 458 contains a 256 x 24 bit RAM lookup table, and three 8-bit video converters, allowing the use of 256 colors out of a 16.7 million color palette. The 451 has a 256 x 12 bit RAM lookup table, and three 4-bit D/A converters, allowing the user to select 256 colors out of 4096 possible combinations.

The 451/458 has an 8-bit data bus to communicate with the GSP and the VME bus, but it must be mapped as a 16-bit device, as there is no byte-swapping performed on board. It occupies eight words of space, with read and write operations mapped to different locations.

Complete programming information is available in the 451/458 data sheet, available from Brooktree Corporation. Bit 7 of the command register must be set to a 0, which chooses 4:1 multiplexing of the pixel information. Also, bit 1 (overlay 1 enable) must be set to 0 to disable the OL1 inputs. The OL0 inputs are generated by the 431 cursor controller, and should be disabled if that device is not installed or not enabled.

4.2 Bt431 Cursor Controller

The VGME-34010 contains the Brooktree or equivalent 431 Cursor Controller. This device creates and controls a user-definable cursor, substantially reducing the software overhead. The 431 counts video clock pulses to determine when to send overlay information to the RAMDAC, eliminating the need to move data in and out of the display memory.

The only requirement in programming this device is to ensure that bits D3 and D2 of the command register are set to 0 and 1, respectively, to select 4:1 multiplexing. Full programming information is available in the Bt431 data sheet from Brooktree.

4.3 34010 Video Interface

It is necessary for anyone who is going to write software for the TMS34010 to obtain and use a copy of the TMS34010 User's Guide from Texas Instruments. There are a few I/O registers in the 34010 that must take into consideration requirements of the hardware. They are as follows:

4.3.1 CONTROL register

Bit 2, DRAM refresh mode, must be set to 1 (CAS before RAS refresh). Bits 3-4, DRAM refresh rate, must be set to 00 (every 32 local clock periods).

4.3.2 PSIZE register

This register must be programmed to 8.

4.3.3 Display control registers

The 9 video registers control the way the TMS34010 scans the video memory and generates the sync signals for the monitor. There are many ways to program these registers. See the video.cfg configuration file distributed with Graphic Strategies' C Language Library for examples.

4.3.4 Horizontal sync registers

These registers (HCOUNT, HEBLNK, HESYNC, HSBLNK, HTOTAL) are dependent on the period of the VCLK input, which is equal to sixteen times the period of the pixel clock.

4.4 Serial Controller

The 68681 dual-channel serial controller requires no special programming with regards with how it will operate with the 34010 GSP. It is even possible to use the vectored interrupt feature of this part with the 34010, but the 34010 will have to poll for this vector. There is a separate address in the VGME-34010 memory map for this function.

5.0 Specifications

5.1 Display

Resolution: Programmable, limited by maximum pixel frequency of 125 MHz and amount of video RAM.

Depth: 8 bits/pixel.

Output: RS-343A or RS-170 RGB analog video via SMA connectors with sync on green. Also horizontal/composite sync and vertical sync also on SMA connectors at TTL levels.

Color Palette: 4096 colors with 451, 16.7 million with 458.

5.2 VME Interface (Slave mode only)

Memory access modes: A24, A32; D8, D16, D32.

Peripheral and GSP interface access modes: A16; D8, D16.

Peripheral location: jumper selectable.

Memory location: software programmable

Interrupt generation: software programmable to any level.

Block Transfer capability: A24/A32 and D16/D32 modes.

Block transfer speed: DTACK delay from VME DS/ true: 100 nS max.

Random response time: 400 nS.

Address Modifier Codes: Responds to those defined in VME spec Rev C.1

5.3 TMS34010 Local Memory Interface

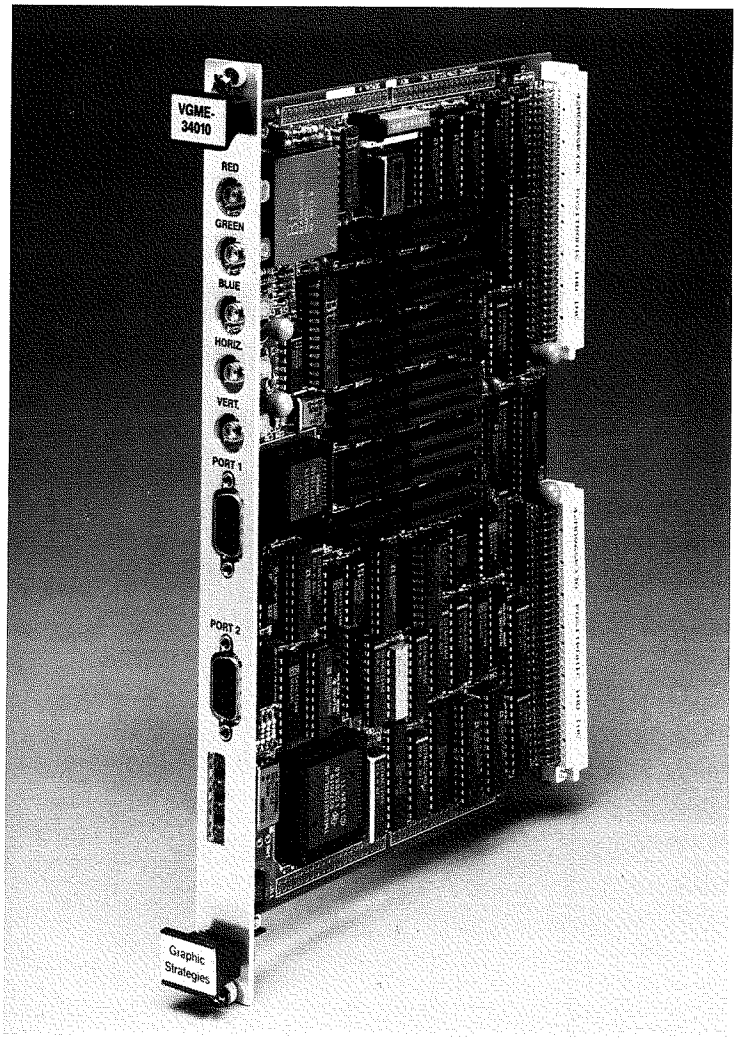
Maximum clock frequency: 50 MHz.
Memory Cycle Time: 320 nS (no wait states) for RAM and peripherals.
DRAM capacity: 2 Megabytes maximum
VRAM capacity: 2 Megabytes maximum

5.4 Environmental

Temperature: 0 to 50 operating; -40 to +70 non-operating.
Humidity: 5 to 90% (non-condensing).
Power Consumption: +5V @ 2.5A typ; 4.0A max.

- **TMS34010 Graphics System Processor (GSP) with drawing speeds to 6.2 Mpixels per second**
- **Configurable resolution to 1280 by 1024 displayed pixels / 256 colors**
- **2 MB VRAM and 2 MB DRAM with direct image access**
- **Hardware cursor, scroll, pan, and zoom**
- **Two user-configurable RS-232 I/O ports for mouse and keyboard**
- **Onboard X11 server, GSI Graphics Primitive Support (GPS), and text fonts**

VGME-34010 VMEbus Graphics Controller



■ Video synchronization and refresh, pixel copying, high-speed graphics primitive processing, and X windows server are all handled onboard by the 50 MHz Graphics System Processor (GSP). Simple software calls and standard VMEbus block transfer and interrupts free the host for application processing.

■ Simple reconfigurations allow the VGME-34010 to support any display resolution to 1280 x 1024, any clock rate to 125 MHz, and interlaced or non-interlaced displays. 8-bit pixels and a high-speed 3-channel RAMDAC allow display of 256 colors from a palette of 16.7 million.

■ 2 MB of video RAM comprise a 2048 x 1024 x 8 frame buffer. 2 MB of additional dynamic RAM provide memory for resident software, bitmaps, and fonts, as well as offscreen image storage. Direct, high-speed host access to all VGME-34010 memory and control registers simplifies simultaneous display of image, text, and geometric data.

■ A hardware cursor controller provides a non-destructive overlay display of crosshair or 64 x 64 bitmap cursors. The user determines the cursor's bitmap and its unique color. Scroll and pan functions allow the display of any screensized window in the 2048 x 1024 x 8 frame buffer. Display zoom by pixel replication is handled completely onboard.

■ A dual UART provides two serial ports for a mouse and keyboard or other communications devices. The serial devices can use software running on the VGME-34010 or access the host directly through the VMEbus. One port also allows optional TTL I/O levels and external clocking.

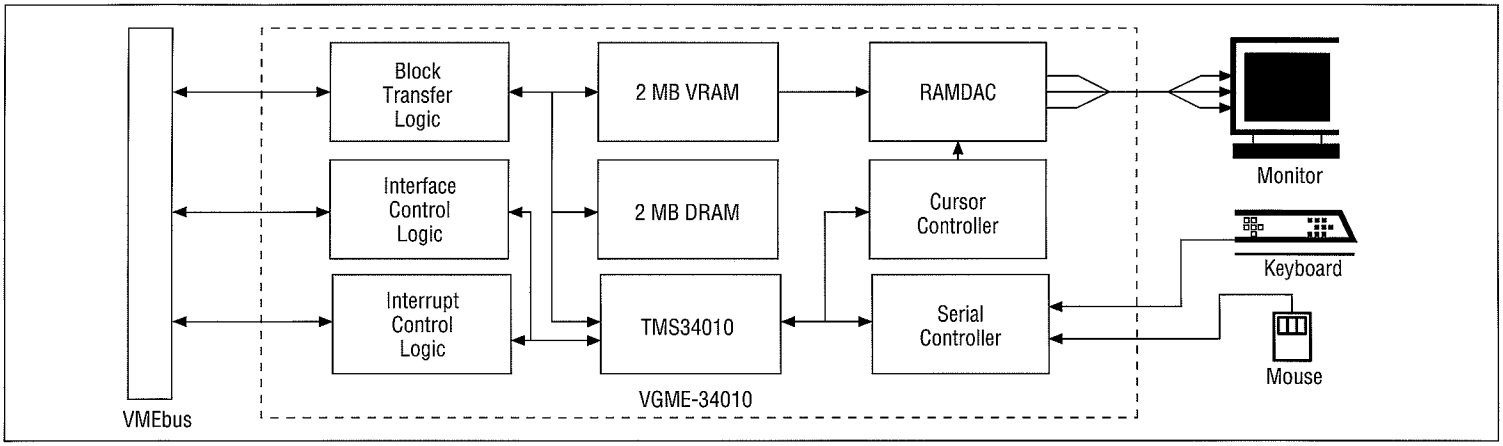
■ A variety of available software allows users fast, efficient access to VMEbus graphics. The X windows server provides complete compatibility and standard libraries for X11. The C-language GPS library provides graphics primitives and mouse, cursor, and text support on many host computers and operating systems. Both the X11 server and the GPS offer wide varieties of standard and optional fonts.

Graphic Strategies, Inc. (GSI) specializes in the design, manufacture, and support of VMEbus graphics systems. GSI offers both off-the-shelf and custom graphics hardware and software solutions.

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Functional Description

The VGME-34010 is designed around the TMS34010 Graphics System Processor (GSP). The GSP is a 16-bit, 50 MHz microprocessor with built-in video control logic and an instruction set optimized for high-speed graphics.

Communication with the host processor uses the full 32-bit VMEbus interface. The host processor has direct block access to all VGME-34010 memory and control registers. All VMEbus interrupt protocols are supported.

Onboard memory includes up to 2 MB of video RAM and up to 2 MB of additional dynamic RAM for software character fonts and offscreen image storage.

A 3-channel RAMDAC includes both a 256-entry color lookup table and 3 fast digital-to-analog converters to control the color monitor. Video data rates as high as 125 MHz are supported. A specialized hardware cursor controller allows display and control of a bitmap or crosshair cursor without affecting the video memory or the color lookup table.

The dual UART provides direct user communication with the VGME-34010 through a keyboard, a mouse, or other serial devices.

Standard and optional software allow the VGME-34010 to operate on a wide variety of computers and operating systems. The VGME-34010 library provides both downward compatibility with other GSI products and unique TMS34010 extensions.

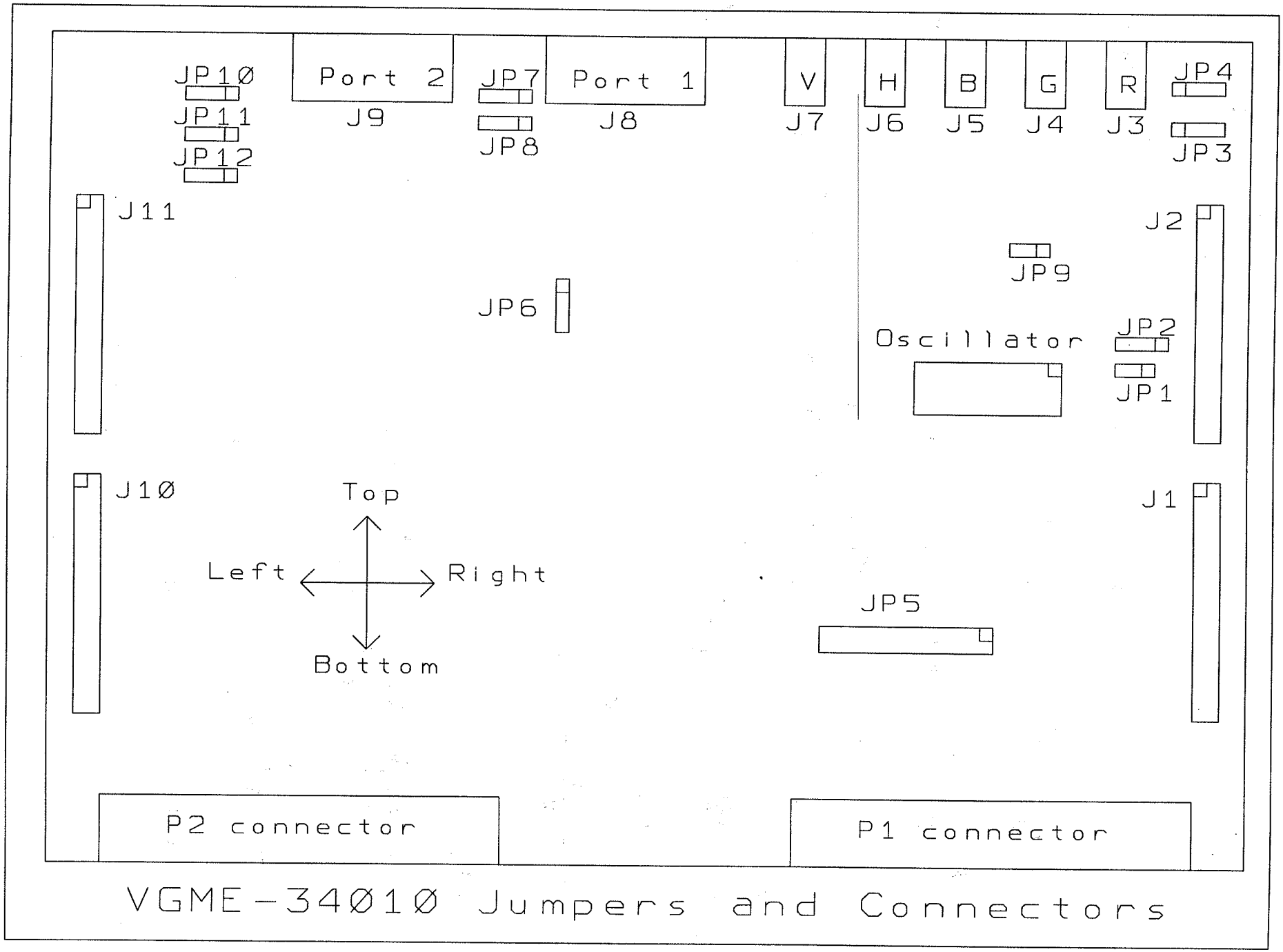
Specifications

Bus: VMEbus A16/D16, A24/D16, A24/D32, A32/D16, or A32/D32
Form Factor: Double height (160 x 230 mm) 6U card, DIN connector interface
Graphics System Processor: TMS34010
Display Resolution: Monitor-dependent to 1280 x 1024
Video Clock Frequency: Monitor-dependent to 125 MHz
Video Refresh: Monitor-dependent, interlaced or non-interlaced
Video Word Size: 8 bits/pixel
Maximum Display Memory: 2048 x 1024 x 8 (2 MB)
Maximum CPU Memory: 2 MB
Memory Access: Direct VMEbus host access to all onboard memory and devices
Colors/Grayscale: 256 colors from palette of 16.7 million or 256 shades of gray
Video Outputs: RS-343A compatible RGB, independent and composite synchronization
Cursor: 64 x 64 bitmap cursor or variable width crosshair cursor, non-destructive
Interrupts: Full VMEbus vectored interrupt system / onboard interrupts for TMS34010
Communications: Two full-duplex RS-232 channels with programmable characteristics
Expansion: Connectors provided for custom expansion boards
Power Requirements: 4.0 A maximum (typical 3 A) @ 5 VDC; 100 mA maximum @ ±12 VDC
Environmental Requirements: Operating temperature 0-50 degrees C; humidity 5-95% non-condensing

GSI Family of Graphics Controllers

Product	Maximum Resolution	Programmable Colors/Palette	Drawing Speed in Mpixels/Sec	CRT Controller	Onboard CPU	Direct Image Access
VGME-512	512 x 512 x 4	16	.8	NEC 7220	N	N
VGME-640	640 x 480 x 4	16/64	.8	NEC 7220	N	N
VGME-1024	1024 x 1024 x 4	16/64	.8	NEC 7220	N	N
VGME-6408	1024 x 1024 x 8	256/16.7 Million	1.3	HITACHI 63484	N	Y
VGME-34010	1280 x 1024 x 8	256/16.7 Million	6.2	TI 34010	Y	Y

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VGME-34010 Jumpers and Connectors

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