User Manual

IP-Driver 40

40 Channel
Low Side Driver
IndustryPack®

Revision ii
Corresponding Hardware: Revision A

IP-Driver 40

40 Channel
Low-Side Driver
IndustryPack®

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Product Description

IP-Driver 40 is optimized for driving loads in industrial environments and OEM applications where density, cost and reliability are critical. The 40 low-side switches provide up to 160 switches per system slot. Each switch consists of an independent N-channel power FET in an open-drain configuration. Typical loads are lamps, solenoids, actuators, valves, relays and small motors.

The switches sink up to 250 mA of load current continuously with an off-state voltage of up to 48 VDC. Individual switches may handle up to one amp continuous on current as long as the aggregate current through the IndustryPack is limited to 10 amps. The switch transistors themselves are rated at 3.6 amps each. Low ON resistance of only 0.13 ohms keeps local power dissipation to a minimum. Maximum drive current is limited by external cabling and long-term heat dissipation. 2 oz. solid copper internal planes in the IP-Driver 40 provide excellent heat dissipation. Channels may be ganged for higher drive current. The use of power FETs is ideal for handling the high starting currents of loads such as lamps and small motors.

The 40 switches are controlled by five, 8-bit read back latches that are accessed as 16-bit words. Writing a "0" to the appropriate bit in the latch turns the FET ON (i.e. switch closed). Similarly, reading back a "0" indicates that the FET is ON.

For safety, IP-Driver 40 has been designed to clear all latches upon RESET. This results in opening all switches upon hardware RESET.

The simplified block diagram of the IP-Driver 40 is shown below in Figure 1.

Simplified Block Diagram

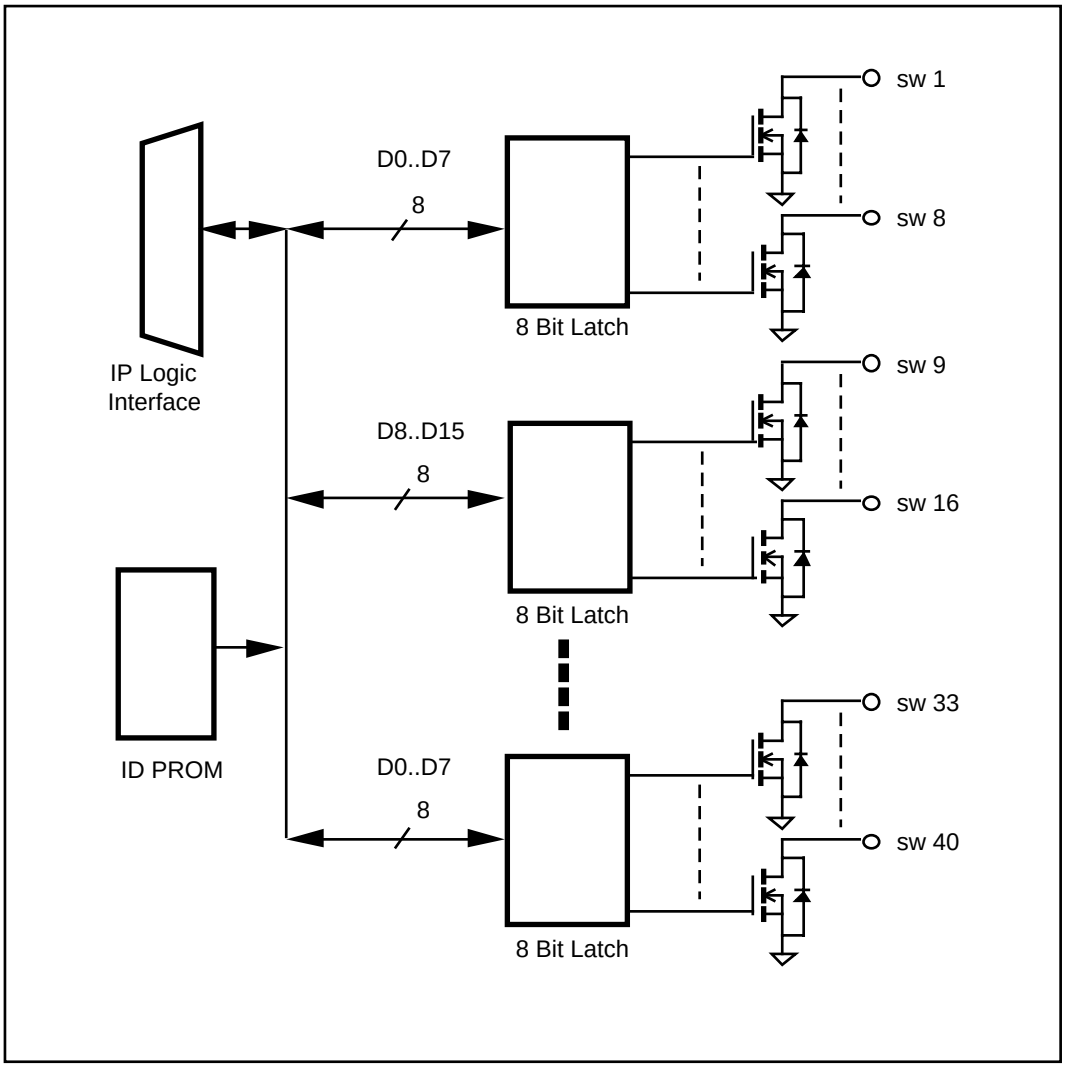

Figure 1 IP-Driver 40 Block Diagram

Applications Guide

Programming and interfacing the IP-Driver 40 should be relatively straight forward but there are a few things to keep in mind:

Programming

Logical "0" turns FET ON. The 40 switches are controlled by read back latches that are be accessed in 16-bit words. Writing a "0" to the latch turns the FET ON (i.e. switch closed). Reading back a "0" indicates that the FET is ON. Writing a "1" to the latch turns the FET OFF (i.e. switch open).

Interfacing

Sink, don't source current. The power NMOS MOSFET switches of the Driver 40 can sink a current through an external load from an external positive power supply. This is called a "low-side switch," because the switch is near the low—near ground potential—side of the load. See the three Application Example schematics below. The IP-Driver 40 cannot source current. For this, "high-side" switches are needed; consider using the IP-Opto Driver.

Only DC can be switched. The power NMOS MOSFET switches of the Driver 40 have an internal substrate to source connection. This is equivalent to having a reverse bias diode from drain to source. Applying negative voltage or AC voltage to the FET drain will cause a direct short to ground. The external DC power supply that will run the external load must be connected so that the switch connection on the IP-Driver 40 is always zero or positive. The DC power supply may have a large AC component (ripple) but must never be negative.

Use "snubber" or "freewheel" diodes on inductive loads. High voltages are produced across switches that disrupt DC current flow through inductors. These high voltages can destroy semiconductor switches. The NMOS MOSFET power transistors used on the IP-Driver 40 are very rugged, but can be damaged by high voltage. Switching inductive loads causes electromagnetic noise that can instigate system anomalies. "Snubber" or "Freewheel" diodes allow inductor currents to dissipate at the source without damaging other circuit elements and reduce electromagnetic interference.

Reset state is always OFF. The IP-Driver 40 powers up and resets all the switches to the open, or OFF state. Be sure that resetting the IP resets external hardware to safe default conditions.

Use switch closed for ON and switch open for OFF. Writing a zero turns the switch and the external load ON. Writing a one turns the switch and the external load OFF..

Use adequate ground returns. The IP-Driver 40 I/O interface provides 10 ground return connections for 40 lines. Large gauge ground returns will improve overall system performance. A rule of thumb is that the ground lines should be four times heavier than the signal lines (since they must carry the current of four lines). The one amp per line rating applies to ground return lines, as well as signal lines, through the IP and flat-ribbon cable connectors.

Comparing the IP-Driver 40's switches to mechanical switches. The NMOS MOSFET power transistors behave with close to ideal switch characteristics as long as two conditions are met: (1) the maximum voltage and current are not exceeded, and (2) only positive voltage is being switched. Use the table below to compare key switch characteristics:

Characteristic	IP-Driver 40	Mechanical Switch
ON Resistance	.13Ω typ	0.01Ω typ, can vary with age
OFF Leakage	2 μA @ 25°C	very low, can vary considerably
Polarized	DC only	AC and DC
Max Voltage	48 VDC	generally high
Min Voltage	0 volts	0 volts
Turn ON time	150 nsec typ	2 to 20 msec
Turn OFF time	150 nsec typ	2 to 20 msec
ON/OFF bounce	no bounce	large mechanical bounce
Rise/Fall time	constant, 150 nsec typ	very fast, with many bounces
Reliability	very high	moderate
Contact Life	unlimited	10K to 1M cycles
Physical size	small	large
Sound	silent	audible clicking

Applications Examples

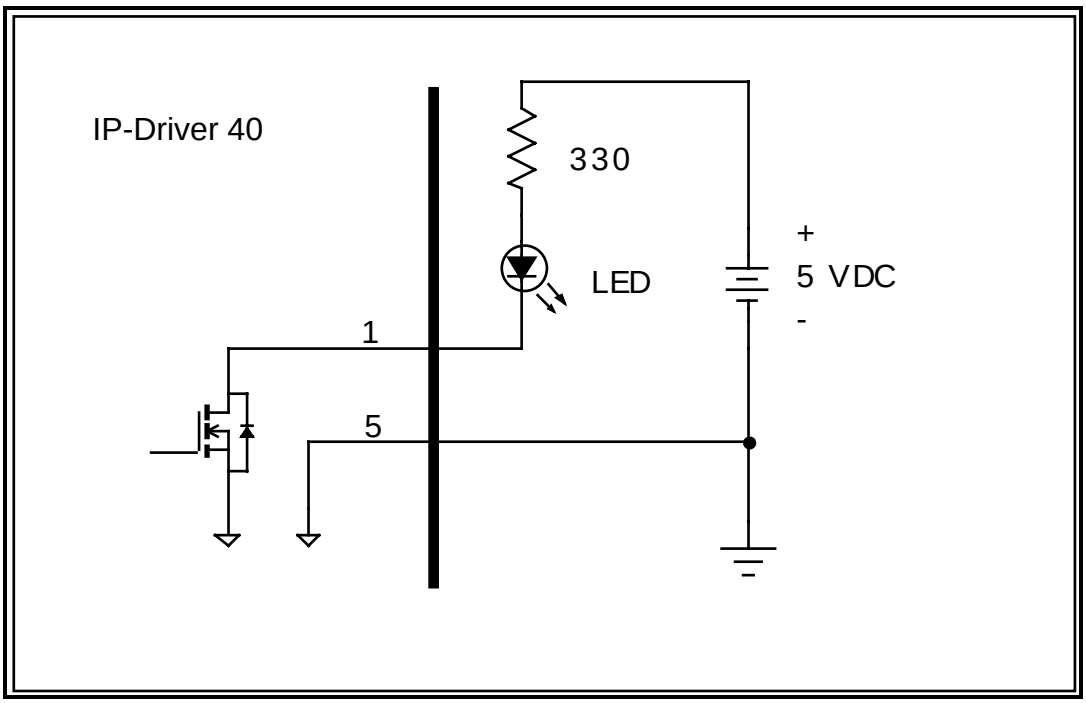

Figure 2 LED Driver Example

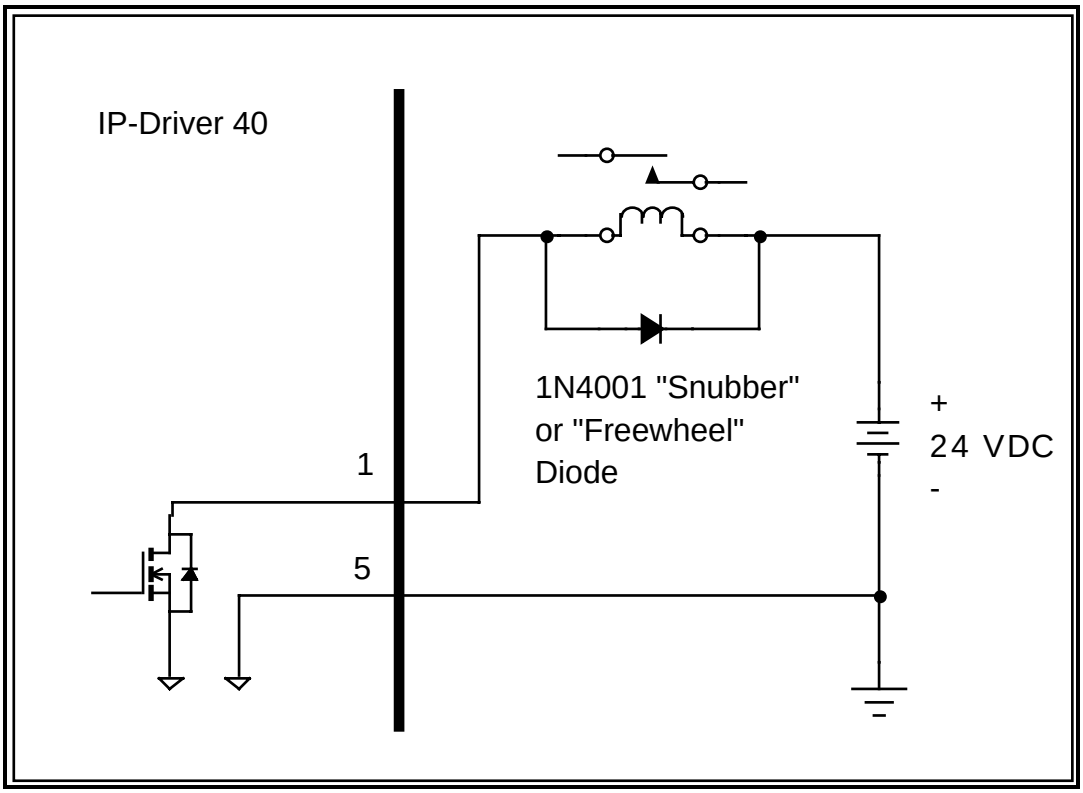

Figure 3 Relay Driver Example

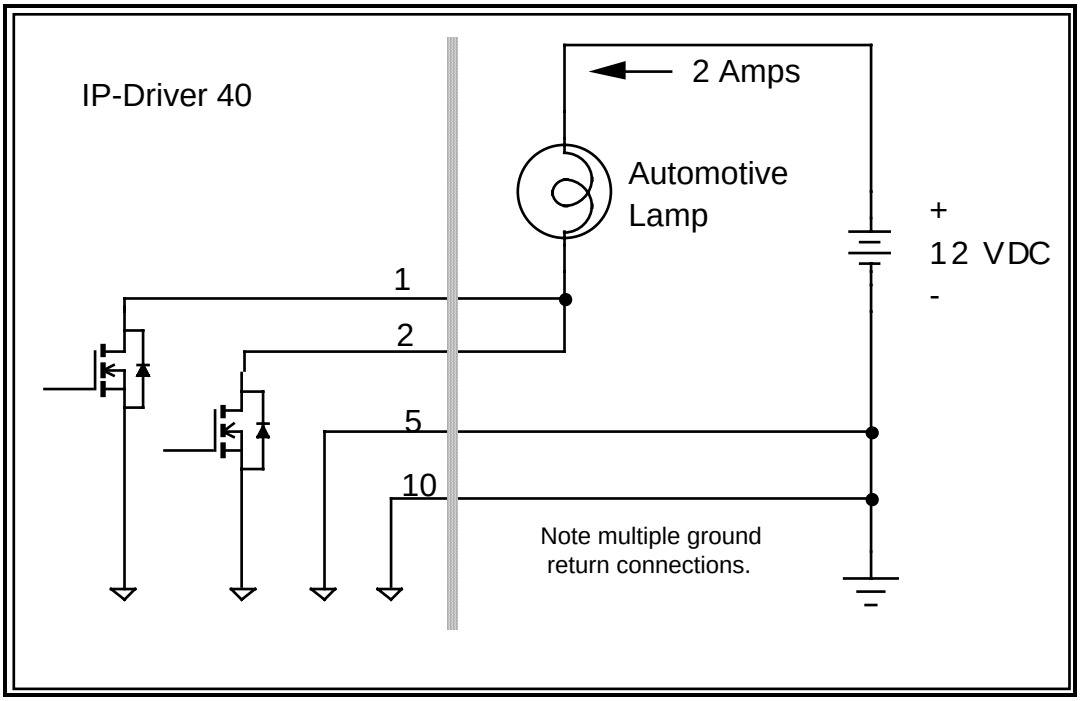

Figure 4 High Current Example

VME Addressing

Both word and byte address nodes are supported by IP-Driver 40. The actual application will depend on your IP carrier board. See your carrier card manual for details.

Standard Word I/O Accessing

The IP-Driver 40 is normally accessed one word at a time in the host's I/O space. I/O to switches beyond 40 will be ignored.. Do not access I/O addresses greater than four. Figures 5 and 6 below show the address and bit assignments of the forty switches.

Offset	I/O Size	Switches effected
Base + 0	word	1 through 16
Base + 2	word	17 through 32
Base + 4	word	33 through 40*

* Note: Data bits D15..D8 ignored at this address

Figure 5 VME Word Access Addressing

Data Bit	Offset=0,1	Offset=2,3	Offset=4
0 LSB	Sw 1	Sw 17	Sw 33
1	Sw 2	Sw 18	Sw 34
2	Sw 3	Sw 19	Sw 35
3	Sw 4	Sw 20	Sw 36
4	Sw 5	Sw 21	Sw 37
5	Sw 6	Sw 22	Sw 38
6	Sw 7	Sw 23	Sw 39
7	Sw 8	Sw 24	Sw 40
8	Sw 9	Sw 25	*
9	Sw 10	Sw 26	*
10	Sw 11	Sw 27	*
11	Sw 12	Sw 28	*
12	Sw 13	Sw 29	*
13	Sw 14	Sw 30	*
14	Sw 15	Sw 31	*
15 MSB	Sw 16	Sw 32	*

* Note: Data bits D15..D8 ignored at this address

Figure 6 Bit to Switch Assignments

Byte I/O Accessing

IP-Driver 40 supports byte access. On 68K (big endian byte ordering) VME systems, the low order data bits D0 through D7 are accessed at odd memory locations. See Figure 7 below for the byte address map. Use Figure 6 above for the bit assignments.

Offset	I/O Size	Switches effected
Base + 1	byte	1 through 8
Base + 0	byte	9 through 16
Base + 3	byte	17 through 24
Base + 2	byte	25 through 32
Base + 5	byte	33 through 40

Figure 7 VME Byte Access Addressing

Nubus Addressing

Both word and byte address modes are supported by IP-Driver 40. The actual application will depend on your IP carrier board. See your carrier card manual for details.

The formula for conversion from VME to Nubus, for 16-bit word address is:

Nubus address = (VME address x 2)

Standard Word I/O Accessing

The IP-Driver 40 is normally accessed one word at a time in the host's I/O space. I/O to switches beyond 40 will be ignored. Do not access I/O addresses greater than Base + four. Figure 8 below show the address assignments of the forty switches. Byte accesses are not recommended.

Offset	I/O Size	Switches effected
Base + 0	word	1 through 16
Base + 4	word	17 through 32
Base + 8	word	33 through 40*

* Note: Data bits D15..D8 ignored at this address

Figure 8 Nubus Word Access

ISA (IBM PC-AT) Addressing

Both word and byte address modes are supported by IP-Driver 40. The actual application will depend on your carrier card. See your carrier card manual for details.

Standard Word I/O Accessing

The IP-Driver 40 is normally accessed one word at a time in the host's I/O space. I/O to switches beyond 40 will be ignored. Do not access I/O addresses greater than Base + four. Figures 9 below and 6 above show the address and bit assignments of the forty switches.

Offset	I/O Size	Switches effected
Base + 0	word	1 through 16
Base + 2	word	17 through 32
Base + 4	word	33 through 40*

* Note: Data bits D15..D8 ignored at this address

Figure 9 ISA Word Access

Byte I/O Accessing

IP-Driver 40 supports byte access. On Intel (little-endian byte ordering) AT systems, the low order data bits D0 through D7 are accessed at even memory locations. See Figure 10 below for the byte address map. Use Figure 6 above for the bit assignments. Word access is strongly preferred because of the more logical bit-to-switch ordering.

Offset	I/O Size	Switches effected
Base + 0	byte	1 through 8
Base + 1	byte	9 through 16
Base + 2	byte	17 through 24
Base + 3	byte	25 through 32
Base + 4	byte	33 through 40

Figure 10 ISA Byte Access

I/O Pin Wiring

This section gives the pin assignments for IP-Driver 40.

The pin numbers given in Figure 11 correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board and to the screw terminal numbers on the IP-Terminal block included in the engineering kit.

I/O Pin	Signal	I/O Pin	Signal
1	Sw 1	26	Sw 21
2	Sw 2	27	Sw 22
3	Sw 3	28	Sw 23
4	Sw 4	29	Sw 24
5	GND	30	GND
6	Sw 5	31	Sw 25
7	Sw 6	32	Sw 26
8	Sw 7	33	Sw 27
9	Sw 8	34	Sw 28
10	GND	35	GND
11	Sw 9	36	Sw 29
12	Sw 10	37	Sw 30
13	Sw 11	38	Sw 31
14	Sw 12	39	Sw 32
15	GND	40	GND
16	Sw 13	41	Sw 33
17	Sw 14	42	Sw 34
18	Sw 15	43	Sw 35
19	Sw 16	44	Sw 36
20	GND	45	GND
21	Sw 17	46	Sw 37
22	Sw 18	47	Sw 38
23	Sw 19	48	Sw 39
24	Sw 20	49	Sw 40
25	GND	50	GND

Figure 11 I/O Pin Out Assignment

IndustryPack Logic Interface Pin Assignment

Figure 12 below gives the pin assignments for the IndustryPack Logic Interface connector on the IP-Driver 40. Pins marked n/c below are defined by the specification, but not used on IP-Driver 40. See also your User Manual for your IP Carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	n/c	5	30
D2	n/c	6	31
D3	n/c	7	32
D4	n/c	8	33
D5	n/c	9	34
D6	IOSel*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	n/c	17	42
D14	A4	18	43
D15	n/c	19	44
BS0*	A5	20	45
BS1*	n/c	21	46
n/c	n/c	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 12 Logic Interface Pin Assignment

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-Driver 40 is shown in Figure 13 below.
For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers.

The location of the ID PROM in the host's address space is dependent on the carrier board used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 13 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

The ID PROM is equivalent to a Philips (Signetics) 8