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IP-OCTAL-422

Eight Channel RS-422
IndustryPack®

User's Manual

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Hardware Revision: A
Part # 89002068 Rev. 1.0
20050125

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IP-OCTAL-422

Eight Channel RS-422
IndustryPack®

SBS Tecnologies, Inc
1284 Corporate Center Drive
St. Paul, MN 55121
Tel (651) 905-4700
FAX (651) 905-4701
Email: support.commercial@sbs.com
http://www.sbs.com

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Product Description

IP-OCTAL-422 is part of the Industry Pack™ family of modular I/O components. It is based around the Signetics CMOS SCC2698 Octal Universal Asynchronous Receiver/Transmitter. This component provides eight channels of full-duplex asynchronous serial communications, baud rate generators, state change detect logic, and four 16-bit counter/timers.

A block diagram of the IP-OCTAL-422 is shown below in Figure 1.

RS-422 communication levels are provided by 26LS31 and 26LS32 transmitters and receivers. Differential transmit data (TxD) and receive data (RxD) lines are provided, plus ground. RS-422 communication is preferred over RS-232 because it provides significantly higher noise immunity. A second advantage is that no ±12 volt power is required at either the send or receive end.

Vectored interrupts are fully supported. A common 8-bit vector register is provided. Channels a,b,c,d interrupt on IRQ0. Channels e,f,g,h interrupt on IRQ1.

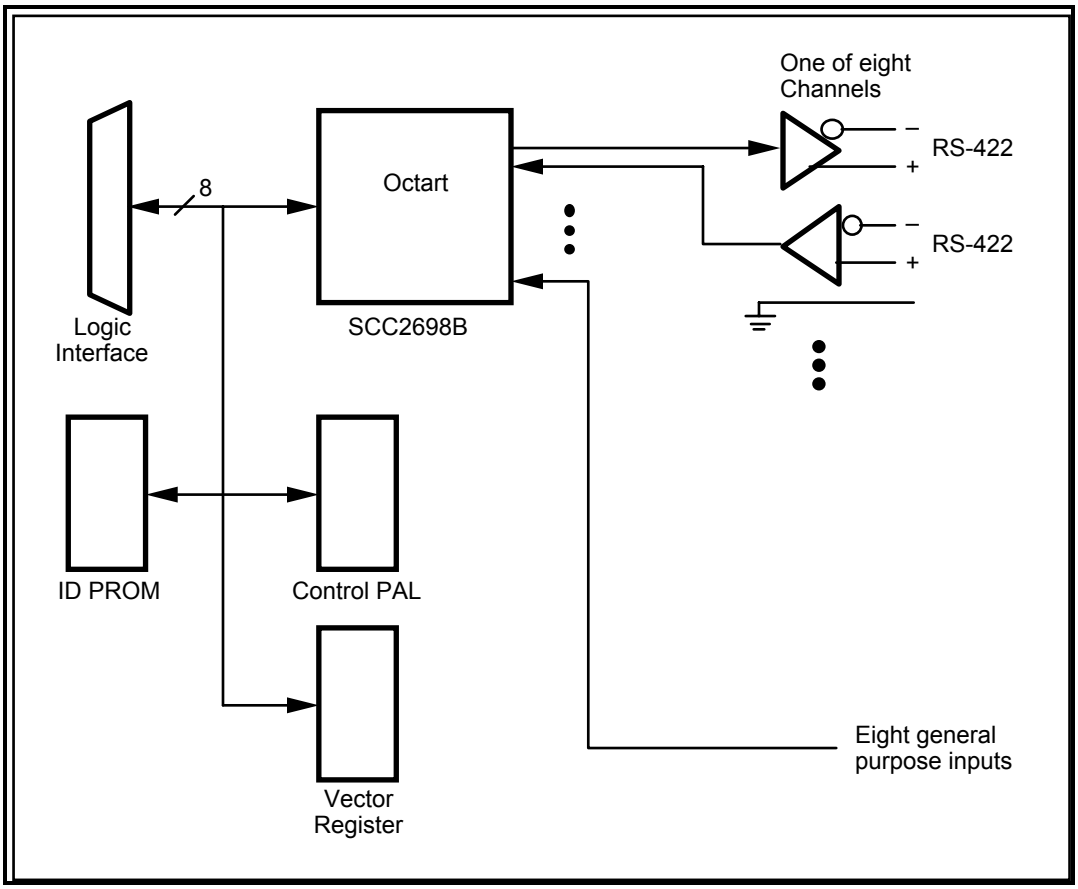


Figure 1 Simplified Block Diagram of IP-OCTAL-422

DMA is supported on channels c and d.

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The IndustryPack is controlled by a single CMOS 22V10 type PAL.

Connection to the IP-OCTAL-422 is via a standard 50-conductor ribbon cable. An optional connection panel is available which provides a 50-pin flat cable input with 16 DB-9 male or female connectors. The metal reinforced connection panel mounts in a standard 19 inch rack-mount space.

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VMEbus Addressing

IP-OCTAL-422 is accessed using 8-bit bytes at odd locations only. It is usually accessed in the I/O space. Shown below in Figures 2 and 3 are the register maps of the IP-OCTAL-422. All addresses are offsets from the I/O base address of the IP as set on the IP carrier board.

The SCC2698B Octal UART has four major internal sections, called functional blocks A through D. Each functional block has two serial channels, one timer, and one I/O port.

Hex	Dec	Binary	Read	Write
		Functional Block A		
1	1	0000001	MR1a, MR2a	MR1a, MR2a
3	3	0000011	SRa	CSRa
5	5	0000101	RESERVED	CRa
7	7	0000111	RHRa	THRa
9	9	0001001	IPCRA	ACRA
B	11	0001011	ISRA	IMRA
D	13	0001101	CTUA	CTURA
F	15	0001111	CRLB	CTLRB
11	17	0010001	MR1b, MR2b	MR1b, MR2b
13	19	0010011	SRb	CSRb
15	21	0010101	RESERVED	CRb
17	23	0010111	RHRb	RHRb
19	25	0011001	RESERVED	RESERVED
1B	27	0011011	INPUT PORT A	OPCRA
1D	29	0011101	START C/T A	RESERVED
1F	31	0011111	STOP C/T A	RESERVED
		Functional Block B		
21	33	0100001	MR1c, MR2c	MR1c, MR2c
23	35	0100011	SRc	CSRc
25	37	0100101	RESERVED	CRc
27	39	0100111	RHRc	THRc
29	41	0101001	IPCRB	ACRB
2B	43	0101011	ISRB	IMRB
2D	45	0101101	CTUB	CTURB
2F	47	0101111	CRLB	CTLRB
31	49	0110001	MR1d, MR2d	MR1d, MR2d
33	51	0110011	SRd	CSRd
35	53	0110101	RESERVED	CRd
37	55	0110111	RHRd	THRd
39	57	0111001	RESERVED	RESERVED
3B	59	0111011	INPUT PORT B	OPCRB
3D	61	0111101	START C/T B	RESERVED
3F	63	0111111	STOP C/T B	RESERVED

Figure 2 Register Map of SCC2698, Blocks A and B

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Hex	Dec	Binary	Read	Write
		Functional Block C		
41	65	1000001	MR1e, MR2e	MR1e, MR2e
43	67	1000011	SRe	CSRe
45	69	1000101	RESERVED	CRe
47	71	1000111	RHRe	THRe
49	73	1001001	IPCRC	ACRC
4B	75	1001011	ISRC	IMRC
4D	77	1001101	CTUC	CTURC
4F	79	1001111	CRLC	CTLRC
51	81	1010001	MR1f, MR2f	MR1f, MR2f
53	83	1010011	SRf	CSRf
55	85	1010101	RESERVED	CRf
57	87	1010111	RHRf	THRf
59	89	1011001	RESERVED	RESERVED
5B	91	1011011	INPUT PORT C	OPCRC
5D	93	1011101	START C/T C	RESERVED
5F	95	1011111	STOP C/T C	RESERVED
		Functional Block D		
61	97	1100001	MR1g, MR2g	MR1g, MR2g
63	99	1100011	SRg	CSRg
65	101	1100101	RESERVED	CRg
67	103	1100111	RHRg	THRg
69	105	1101001	IPCRD	ACRD
6B	107	1101011	ISRD	IMRD
6D	109	1101101	CTUD	CTURD
6F	111	1101111	CRLD	CTLRD
71	113	1110001	MR1h, MR2h	MR1h, MR2h
73	115	1110011	SRh	CSRh
75	117	1110101	RESERVED	CRh
77	119	1110111	RHRh	RHRh
79	121	1111001	RESERVED	RESERVED
7B	123	1111011	INPUT PORT D	OPCRD
7D	125	1111101	START C/T D	RESERVED
7F	127	1111111	STOP C/T D	RESERVED

Figure 3 Register Map of SCC2698, Blocks C and D

For NuBus applications see the section following, Nubus Addressing.

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NuBus Addressing

Since the Nubus uses only 32-bit wide accesses, 8-bit wide peripherals such as the IP-OCTAL-422 appear in the host address space every fourth byte.

To calculate the RM1260 Springboard register addresses from the VMEbus address (given in the previous section in Figures 2 and 3), multiply by two and subtract one. To convert VME addresses to RM1270 SupportBoard addresses multiply by two and add one.

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I/O Pin Assignments

This section gives the pin assignments for IP-OCTAL-422 connections.

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Pin Number	Channel	Function	Level
1	Channel a	GND	RS-422
2	Channel a	TxD–	RS-422
3	Channel a	TxD+	RS-422
4	Channel a	RxD–	RS-422
5	Channel a	RxD+	RS-422
6	Channel b	GND	RS-422
7	Channel b	TxD–	RS-422
8	Channel b	TxD+	RS-422
9	Channel b	RxD–	RS-422
10	Channel b	RxD+	RS-422
11	Channel c	GND	RS-422
12	Channel c	TxD–	RS-422
13	Channel c	TxD+	RS-422
14	Channel c	RxD–	RS-422
15	Channel c	RxD+	RS-422
16	Channel d	GND	RS-422
17	Channel d	TxD–	RS-422
18	Channel d	TxD+	RS-422
19	Channel d	RxD–	RS-422
20	Channel d	RxD+	RS-422
21	Channel e	GND	RS-422
22	Channel e	TxD–	RS-422
23	Channel e	TxD+	RS-422
24	Channel e	RxD–	RS-422
25	Channel e	RxD+	RS-422
26	Channel f	GND	RS-422
27	Channel f	TxD–	RS-422
28	Channel f	TxD+	RS-422
29	Channel f	RxD–	RS-422
30	Channel f	RxD+	RS-422
31	Channel g	GND	RS-422
32	Channel g	TxD–	RS-422
33	Channel g	TxD+	RS-422
34	Channel g	RxD–	RS-422
35	Channel g	RxD+	RS-422
36	Channel h	GND	RS-422
37	Channel h	TxD–	RS-422
38	Channel h	TxD+	RS-422
39	Channel h	RxD–	RS-422 40
Channel h		RxD+	RS-422
41	--	GND	--
42	--	no connection	
43	Channel a	MPI - a	CMOS*
44	Channel b	MPI - b	CMOS*
45	Channel c	MPI - c	CMOS*
46	Channel d	MPI - d	CMOS*
47	Channel e	MPI - e	CMOS*
48	Channel f	MPI - f	CMOS*
49	Channel g	MPI - g	CMOS*
50	Channel h	MPI - h	CMOS*

***Note:** I/O lines on pins 43–50 are ±50 µA input current, TTL thresholds.

Figure 4 I/O Pin Assignment

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Each channel has five lines. Each channel is wired identically at the 50-pin connector. The five lines are Ground, Transmit Data output Minus, Transmit Data output Plus, Receive Data input Minus, and Receive Data input Plus. The common ground line for all channels connects to the local logic ground.

Eight general purpose input lines at non-RS-422 levels are provided on pins 43 through 50. These are unbuffered CMOS logic inputs connected directly to the SCC2698B. They may be programmed as general purpose inputs or as the counter/timer external input. The switching threshold for inputs is at TTL levels (1.5 volts nominal). Since these lines are unbuffered, the user is cautioned to observe anti-static rules in handling cabling, the IndustryPack and all connecting hardware. External equipment connected to these lines should be powered up and down at the same time as the IndustryPack.

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IndustryPack Logic Interface Pin Assignment

Figure 5 below gives the pin assignments for the IndustryPack Logic Interface on the IP-OCTAL-422. Pins marked n/c below are defined by the specification, but not used on IP-OCTAL-422.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	DMAReq0	5	30
D2	MEMSel*	6	31
D3	DMAReq1	7	32
D4	INTSel*	8	33
D5	DMAck0*	9	34
D6	IOSel*	10	35
D7	DMAck1*	11	36
n/c	A1	12	37
n/c	n/c	13	38
n/c	A2	14	39
n/c	n/c	15	40
n/c	A3	16	41
n/c	n/c	17	42
n/c	A4	18	43
n/c	n/c	19	44
n/c	A5	20	45
n/c	Strobe*	21	46
–12V	A6	22	47
+12V	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 5 Logic Interface Pin Assignment

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Programming

The IP-OCTAL-422 is designed around the SCC2698B and all of the SCC2698 functions are available. The SCC2698B is divided into four Functional Blocks lettered A through D. Each functional block contains two serial channels. The channels are identified by lower case letters a through h. The SCC2698B contains 64 internal registers, 16 for each functional block. Each of these registers are accessible using a read or write to the IP-OCTAL-422 I/O space. The SCC2698 manual is included with the Technical Documentation to provide the user with detailed information about these registers.

The IndustryPack provides an external vector register. The address of the vector register, which may also be read normally, is in the upper half of the ID PROM space of the IndustryPack, on odd bytes. The address offsets are shown in Figure 6.

There is also provision for mapping the vector register to IP memory space. This is required primarily when the IP is installed on a Motorola MVME162 CPU board. In this mode, no address offset is required; the memory base address is sufficient.

Carrier	Bus	Address
VIPC310	VMEbus	IP I/O base + $C1
VIPC610	VMEbus	IP I/O base + $C1
MVME162	IPIC	IP Memory base
RM1260	NuBus	IP ID base + $81
RM1270	NuBus	IP ID base + $83

Figure 6 Location of the Vector Register

The eight bit vector is loaded by the host software prior to enabling interrupts. The interrupts service routine polls the SCC2698B to determine the detailed cause of the interrupt. Function Blocks A and B interrupt on IRQ0. Function Blocks C and D interrupt on IRQ1. See the User Manual for your IP Carrier tor interrupt mapping to your bus. Note that although two distinct interrupt levels are provided, there is a single vector for the IndustryPack.

A Hypercard stack is available that permits quick demonstration, testing and prototyping of the IP-OCTAL-422. A user provide Apple® Macintosh® II family computer is required.

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ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-OCTAL-422 is shown in Figure 7 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from SBS.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 7 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

The ID PROM used is an AMD 27LS19A or equivalent.

3F 19	(available for user)	
17	CRC	
15	No of bytes used	(0B)
13	Driver ID, high byte	
11	Driver ID, low byte	
0F	reserved	(00)
0D	Revision	(A1)
0B	Model No IP-OCTAL-422	(2A)
09	Manufacturer ID SBS	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 7 ID PROM Data (hex)

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User Options

User options consist of connecting to the Strobe pin on the Logic Interface and connections to support DMA.

The location of the shunt groups is shown near the end of this Manual in Figure 10.

The Strobe pin on the Logic Interface (pin 46) is provided for secondary clock input or output. This pin may be driven by the Channel a Multi-Purpose Output from the SCC, or it may be connected to provide for the external input the to Counter/Timer. These options are shown below in Figure 8. Note that in most cases some corresponding programming of SCC modes is required. The SCC may be programmed to drive the connected pin for other functions that those listed in the Figure below. The IndustryPack Logic Interface Specification restricts the Strobe pin to clock functions, however. Only those functions listed below should programmed.

Shunt E1	I/O	SCC Pin	Function
1-2	Output	MPOa	Counter/Timer output
1-2	Output	MPOa	Transmit Clock (1X or 16X)
1-2	Output	MPOa	Receive Clock (1X or 16X)
2–3	Input	MPI1a	General Purpose Input
2–3	Input	MPI1a	Counter/Timer External Input
OUT	none	none	Strobe Pin floating **default**

Figure 8 Strobe Connection Options

The IP-OCTAL-422 is configured to support minimum Direct Memory Access (DMA) on Channels C and D. To use DMA, program the SCC for TxRDY or RxRDY on MPOc and/or MPOd. See Figure 9 below for DMA Shunt Assignments.

Shunt	SCC Pin	Logic Pin	Function
E2 IN	MPOc	DMAReq0	TxRDY or RxRDY
E3 IN	MPOd	DMAReq1	TxRDY or RxRDY
E2,E3 OUT	--	--	No DMA **default**

Figure 9 DMA Shunt Assignments

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Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-OCTAL-422 is constructed out of 0.062 inch thick FR4 material. The six copper layers consist of a ground plane, a power plane and four signal planes.

Surface mounting of components is used extensively. IC sockets for the control PAL and ID PROM use gold plated screw-machined pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is optionally secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

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Repair

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the factory for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS will not be responsible for damages due to improper packaging of returned items.

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Shunt Locations

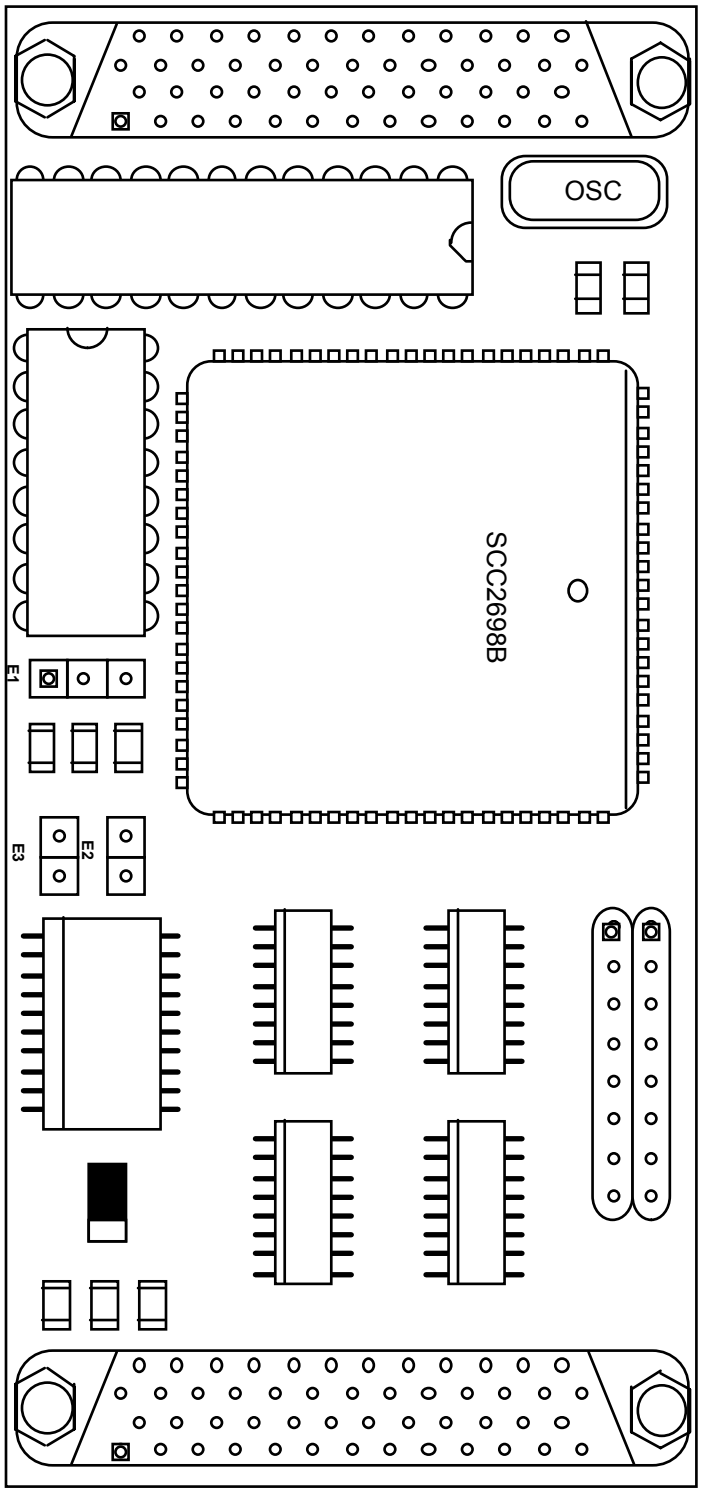


Figure 10 Shunt Locations

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Specifications

Logic Interface	IndustryPack logic Interface
Wait States	Zero on ID and Interrupts, One on SCC accesses
Number of Channels	Eight
Type of Channels	Full-duplex asynchronous RS-422
Baud Rates	18 fixed rates from 50 to 38.4K Four user-defined rates using timers
Implemented Signals	TxD+, TxD–, RxD+, RxD–, GND
Stop Bits	1, 1.5, 2 in 1/16 bit increments
Clock Source	Local crystal oscillator, or external
Error Detection	Parity, framing, overrun, false start bit, break
Channel Modes	Full duplex, automatic echo, local loopback, remote loopback
Number of Timers	Four
Type of Timers	16-bit, multi-function, programmable
Interrupt Sources	32, maskable, vectored
Interrupt Vector	8 bits, may be independently read/writable
Auxiliary Input lines	8 TTL/CMOS level inputs, programmable bit input or state change detect causes interrupt or counter/external clock input
IP Strobe Options	Timer output, or baud rate clock input, or none
Power Requirements	+5 VDC, 285 mA, typical +12 VDC, 0 mA –12 VDC, 0 mA
Dimensions	1.800 by 3.900 by 0.340 inches maximum
Environmental	Operating temperature: +10 to +50°C Humidity: 5% to 95% non-condensing Storage: –10 to +85°C

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