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IP-OptoDA12

Opto-Isolated 12-bit D/A Conversion IndustryPack®

User's Manual

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IP-OptoDA12

Opto-Isolated 12-bit D/A Conversion IndustryPack®

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Product Description

The IP-OptoDA12 is an IndustryPack compatible module with 8 (IP-OptoDA12-8CH) or 4 (IP-OptoDA12-4CH) 12 bit D/A channels which are galvanically isolated from the IndustryPack logic interface.

Output voltage ranges of ±10 V or 0 V to 10 V are selectable by jumper for each group of 4 D/A channels. After RESET all D/A channels default to 0V.

Each IP-OptoDA12 is calibrated at the factory. Calibration information of the D/A channels is stored in the Identification PROM unique to each IP.

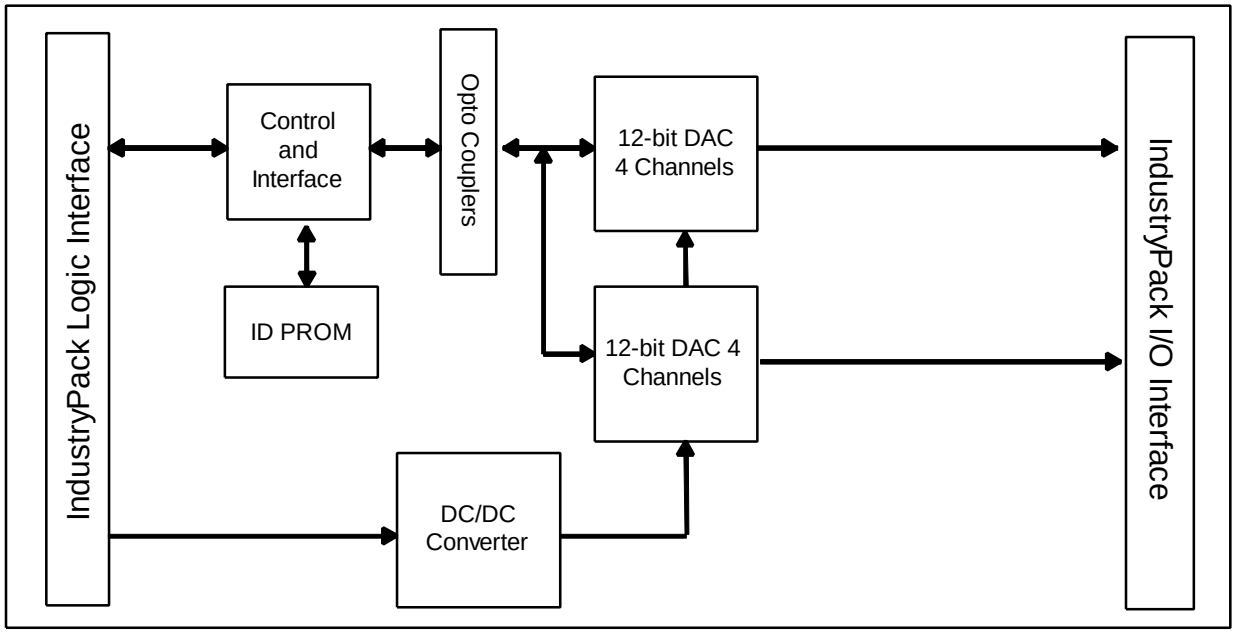


Figure 1 IP-OptoAD12 Block Diagram

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Functional Description

Analog Output

The IP-OptoDA12 includes 2(1) group of 4 channels of analog outputs with a voltage range of ±10V or 0V to 10V. The maximum output current for each channel is ±4mA. Each channel has a typical settling time to 0.01% of 13ms .

Two voltage ranges are jumper selectable: ±10V or 0V to 10V. Each group of D/A channels (channel 1-4 and channel 5-8) can be assigned one of the two voltage ranges.

The 8(4) analog outputs of the IP-OptoDA12 are galvanically isolated from the IndustryPack logic interface by optocoupler. On board DC/DC converters supply the isolated part.

Data Correction

There are two errors which affect the DC accuracy of the DAC. The first is the zero error (offset). For the DAC this is the data value required to produce a zero voltage output signal. This error is corrected by subtracting the known error from all readings.

The second error is the gain error. Gain error is the difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the data value by a correction factor.

The data correction values are obtained during factory calibration and are stored in the modules individual version of the ID PROM. The DAC has a pair of offset and gain correction values for each single output channel. The correction values are stored in the ID PROM as two's complement byte wide values in the range -128 to 127. For higher accuracy they are scaled to ¼ LSB.

Because offset and gain correction values are dependent on the selected output voltage range the IP-OptoDA12-8CH has 4 different sets of ID PROM data (4 combinations of the output voltage range for the 2 groups of D/A channels) and the IP-OptoDA12-4CH has 2 different sets of ID PROM data (2 combinations of the output voltage range for one group of D/A channels).

Note: Before accessing the correction values of the ID PROM the Control Register CONTROL must be set up identical with the voltage ranges configured by jumper.

DAC Correction Formula for 0V - 10V Output Range

The basic formula for correcting unipolar DAC output value is:

$$\mathbf{Data = Value * (1 - Gain_{corr} / 16384) - Offset_{corr} / 4}$$

Data is the digital value that will be sent to the DAC, Value is the desired output value, $Gain_{corr}$ and $Offset_{corr}$ are the correction factors from the ID PROM.

DAC Correction Formula for ±10V Output Range

The basic formula for correcting bipolar DAC output value is:

$$\mathbf{Data = Value * (1 - Gain_{corr} / 8192) - Offset_{corr} / 4}$$

Data is the digital value that will be sent to the DAC, Value is the desired output value, $Gain_{corr}$ and $Offset_{corr}$ are the correction factors from the ID PROM.

$Gain_{corr}$ and $Offset_{corr}$ correction factors are stored separately for each for the eight (four) DAC outputs.

Note: Floating point arithmetics or scaled integer arithmetics is necessary to avoid rounding error while computing above formula.

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ID PROM Contents

The VRGx bits of the DAC Control Register are used to select the correct set of ID PROM correction values and the output code. These bits must be configured first before reading any correction values from the ID PROM and before starting any data conversion.

ID PROM Contents IP-OptoDA12-8CH

ADDRESS	FUNCTION	
$01	ASCII 'I'	$49
$03	ASCII 'P'	$50
$05	ASCII 'A'	$41
$07	ASCII 'C'	$43
$09	Manufacturer ID	$B3
$0B	Model Number	$19
$0D	Revision	$10
$0F	RESERVED	$00
$11	Driver-ID low-byte	$00
$13	Driver-ID high-byte	$00
$15	number of bytes used	$1D
$17	C R C	$variable
$19	Version -10	$0A
$1B	DAC1 Offset	$ board dependent
$1D	DAC2 Offset	$ board dependent
$1F	DAC3 Offset	$ board dependent
$21	DAC4 Offset	$ board dependent
$23	DAC5 Offset	$ board dependent
$25	DAC6 Offset	$ board dependent
$27	DAC7 Offset	$ board dependent
$29	DAC8 Offset	$ board dependent
$2B	DAC1 Gain	$ board dependent
$2D	DAC2 Gain	$ board dependent
$2F	DAC3 Gain	$ board dependent
$31	DAC4 Gain	$ board dependent
$33	DAC5 Gain	$ board dependent
$35	DAC6 Gain	$ board dependent
$37	DAC7 Gain	$ board dependent
$39	DAC8 Gain	$ board dependent
.....	Not used	.....
$3F		$00

Figure 2 ID PROM Contents IP-OptoDA12-8CH

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ID PROM Contents IP-OptoDA12-4CH

ADDRESS	FUNCTION	
$01	ASCII 'I'	$49
$03	ASCII 'P'	$50
$05	ASCII 'A'	$41
$07	ASCII 'C'	$43
$09	Manufacturer ID	$B3
$0B	Model Number	$19
$0D	Revision	$10
$0F	RESERVED	$00
$11	Driver-ID low-byte	$00
$13	Driver-ID high-byte	$00
$15	number of bytes used	$1D
$17	C R C	$ variable
$19	Version -11	$ 0B
$1B	DAC1 Offset	$ board dependent
$1D	DAC2 Offset	$ board dependent
$1F	DAC3 Offset	$ board dependent
$21	DAC4 Offset	$ board dependent
$23		$00
$25		$00
$27		$00
$29		$00
$2B	DAC1 Gain	$ board dependent
$2D	DAC2 Gain	$ board dependent
$2F	DAC3 Gain	$ board dependent
$31	DAC4 Gain	$ board dependent
$33		$00
$35		$00
$37		$00
$39		$00
.....	Not used	
$3F		$00

Figure 3 ID PROM Contents IP-OptoDA12-4CH

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IP Addressing

The IP-OptoDA12 is controlled by a set of registers, which are directly accessible in the I/O address space of the IP.

All registers are automatically cleared by assertion of IP_RESET.

ADDRESS	NAME	FUNCTION	SIZE	ACCESS
$ 01	CHANSEL	DAC Channel Select Reg.	byte	R/W
$ 03	STATUS	DAC Status Register	byte	RO
$ 04	DATAREG	DAC Data Register	word	R/W
$ 07	INTVEC	Interrupt Vector Register	byte	R/W
$ 09	IDWRENA	ID Write Enable Register	byte	R/W
$ 0B	CONTROL	DAC Control Register	byte	R/W

Note: IDWRENA is for factory use only, do not write to this register.

Channel Select Register Address $01

The DAC Channel Select Register CHANSEL is used to select an output channel. This is done by writing the corresponding bit pattern into bit 0 to bit 2. A write access to the CHANSEL register starts the serial datatransfer to the DAC of the value stored in the DAC Data Register DATAREG. Be sure that the desired value is stored in the DATAREG before starting the conversion by writing to the DAC Channel Select Register CHANSEL.

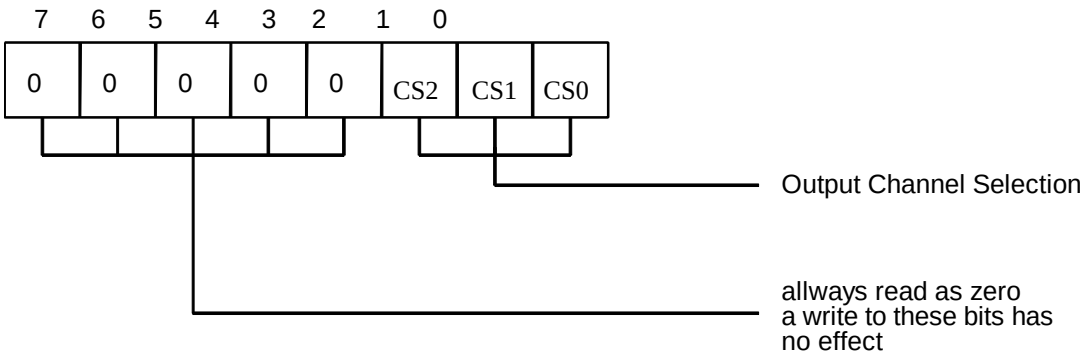


Figure 4 CHANSEL Channel Select Register

Note: The IP-OptoDA12-4CH has only four output channels. Bit 2 of the Channel Select Register CHANSEL must be `0`.

Output Channel Selection

Bit 0 to bit 2 of the Channel Select Register are used to select the output channel of the IP-OptoDA12.

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CS2	CS1	CS0	CHANNEL	TIP550-	0	0	0	1	10/11
0	0	1	2	10/11					
0	1	0	3	10/11					
0	1	1	4	10/11					
1	0	0	5	10					
1	0	1	6	10					
1	1	0	7	10					
1	1	1	8	10					

Figure 5 Output Channel Select Table

Status Register Address $03

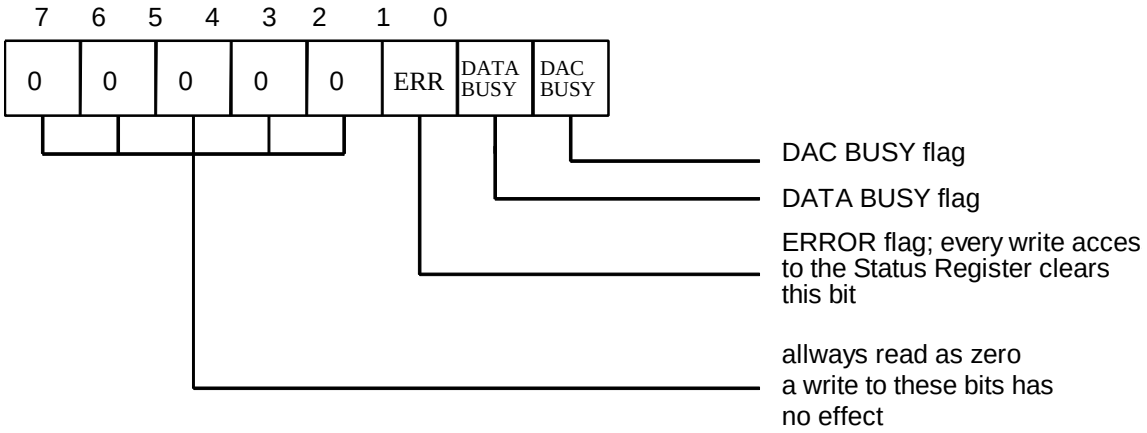


Figure 6 STATREG Status Register

DACBUSY

Reading Bit 0 of the DAC Status Register STATREG as `1` indicates that a serial data transfer to the DAC is in progress. Write accesses to the DAC Channel Select Register CHANSEL during DACBUSY active are ignored and set the ERROR flag in the DAC Status Register STATREG.

DATABUSY

Bit 1 of the DAC Status Register STATREG indicates that a data value written to the DAC Data Register DATAREG is not transmitted to the DAC. The data transfer to the DAC starts by a write access to the DAC Channel Select Register CHANSEL.

Writing a new value to the DAC Data Register DATAREG sets the DATABUSY flag to `1`. Starting the serial data transfer to the DAC by a write access to the DAC Channel Select Register CHANSEL clears the DATABUSY flag to `0`.

ERROR

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Write accesses to the DAC Channel Select Register CHANSEL during DACBUSY active are ignored and set the ERROR flag (bit 2) in the DAC Status Register STATREG to `1`. Any write access to the DAC Status Register STATREG clears the ERROR flag.

Data Register Address $04

The DAC Data Register DATAREG is a 12 bit wide read/write register. The DAC Data Register contains the desired DAC value. After a write access to the DATAREG the flag DATABUSY of the DAC Status Register STATREG is set to '1'. A write access to the DAC Channel Select Register CHANSEL starts the serial data transfer to the DAC and the conversion into an analog value. This write access clears the flag DATABUSY and sets the flag DACBUSY of the DAC Status Register STATREG. Now a new value can be written to the DAC Data Register DATAREG, or after transfer and conversion are completed (DACBUSY = `0`) the same value of the DAC Data Register can be written to another channel.

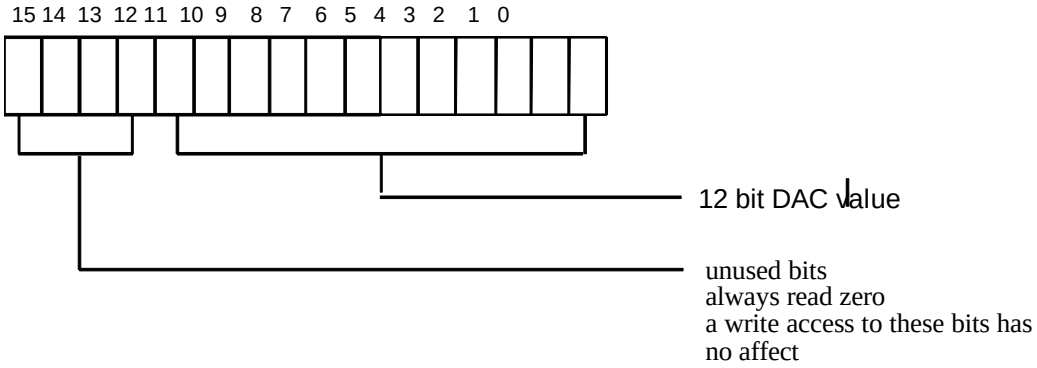


Figure 7 DATAREG Data Register

Note: For output mode look Figure 10 Analog Output Code

Interrupt Vector Register Address $07

The Interrupt Vector Register INTVEC is a byte wide read/write register. A read cycle (interrupt acknowledge cycle) to the INTVEC Register clears the interrupt request. If interrupts are enabled in the DAC Control Register CONTROL interrupts are generated each time the DACBUSY flag of the DAC Status Register becomes inactive (set to `0`).

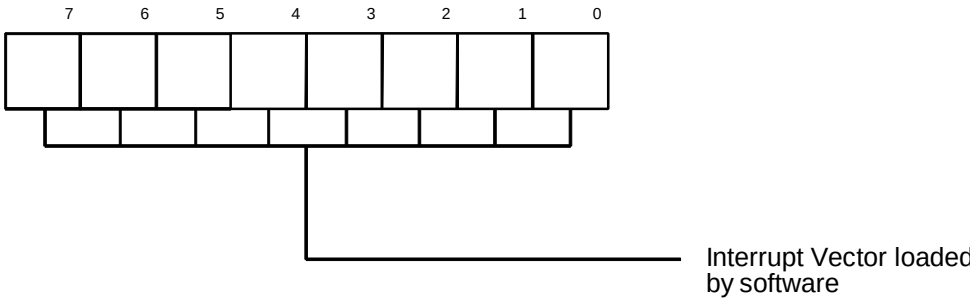


Figure 8 INTVEC Interrupt Vector Register

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Control Register Address $0B

The DAC Control Register CONTROL is a byte wide read/write register.

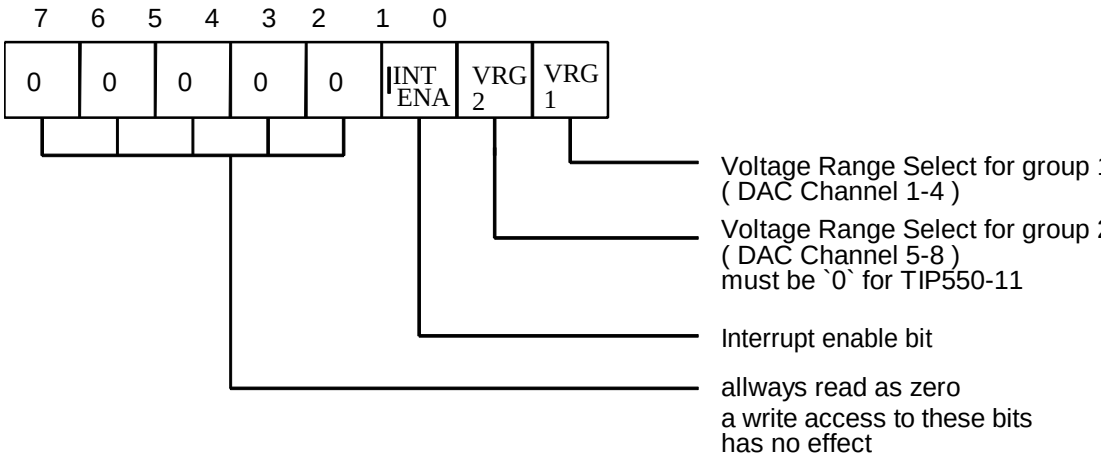


Figure 9 CONTROL DAC Control Register

VRG1/2 Voltage Range Group 1/2

Bit 0 and 1 of the DAC Control Register are the Voltage Range selects for group1 and 2 of the DAC channels. The VRG1 and VRG2 bits must be configured according to the jumper setting for the output voltage ranges of group 1 and 2 of the IP-OptoDA12. Setting a VRGx bit to `1` selects +/- 10V output range and binary two`s complement as output code, setting a VRGx bit to `0` selects 0V to 10V output range and straight binary as output code.

Note: The VRGx bits of the DAC Control Register are used to select the correct set of ID PROM correction values and the output code. These bits must be configured first before reading any correction values from the ID PROM and before starting any data conversion.

Interrupt Enable

Bit 2 of the DAC Control Register controls the interrupt enable. Writing a '1' to bit 2 of this register enables interrupts, writing a '0' to bit 2 disables interrupts. If interrupts are enabled in the DAC Control Register CONTROL interrupts are generated each time the DACBUSY flag of the DAC Status Register becomes inactive (set to `0`).

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Analog Output Code

Bipolar Output Code

If a group of 4 DAC channels is configured for +/- 10V output range by the corresponding jumpers and by programming the VRGx bits of the DAC Control Register the following analog output code is valid:

DATAREG	OUTPUT
$7FF	**+ Full-Scale**
$800	**- Full-Scale**
$000	**Midscale**

Unipolar Output Code

If a group of 4 DAC channels is configured for 0V to10V output range by the corresponding jumpers and by programming the VRGx bits of the DAC Control Register the following analog output code is valid:

DATAREG	OUTPUT
$FFF	Full-Scale
$800	Midscale
$000	Zero-Scale

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State Diagram

State Diagram

After a write access to the DAC Data Register DATAREG the IP-OptoDA12 changes to the DATABUSY state and the flag DATABUSY is set to '1'. A write access to the DAC Channel Select Register CHANSEL starts the serial data transfer to the DAC and the conversion of the value in the DACBUSY state. In this state the flag DACBUSY is set to '1'.

The data of the DAC Data Register DATAREG are valid as long as they are not changed by a new write access to this register. To use the same value for another output channel just write the new channel to the DAC Channel Select Register.

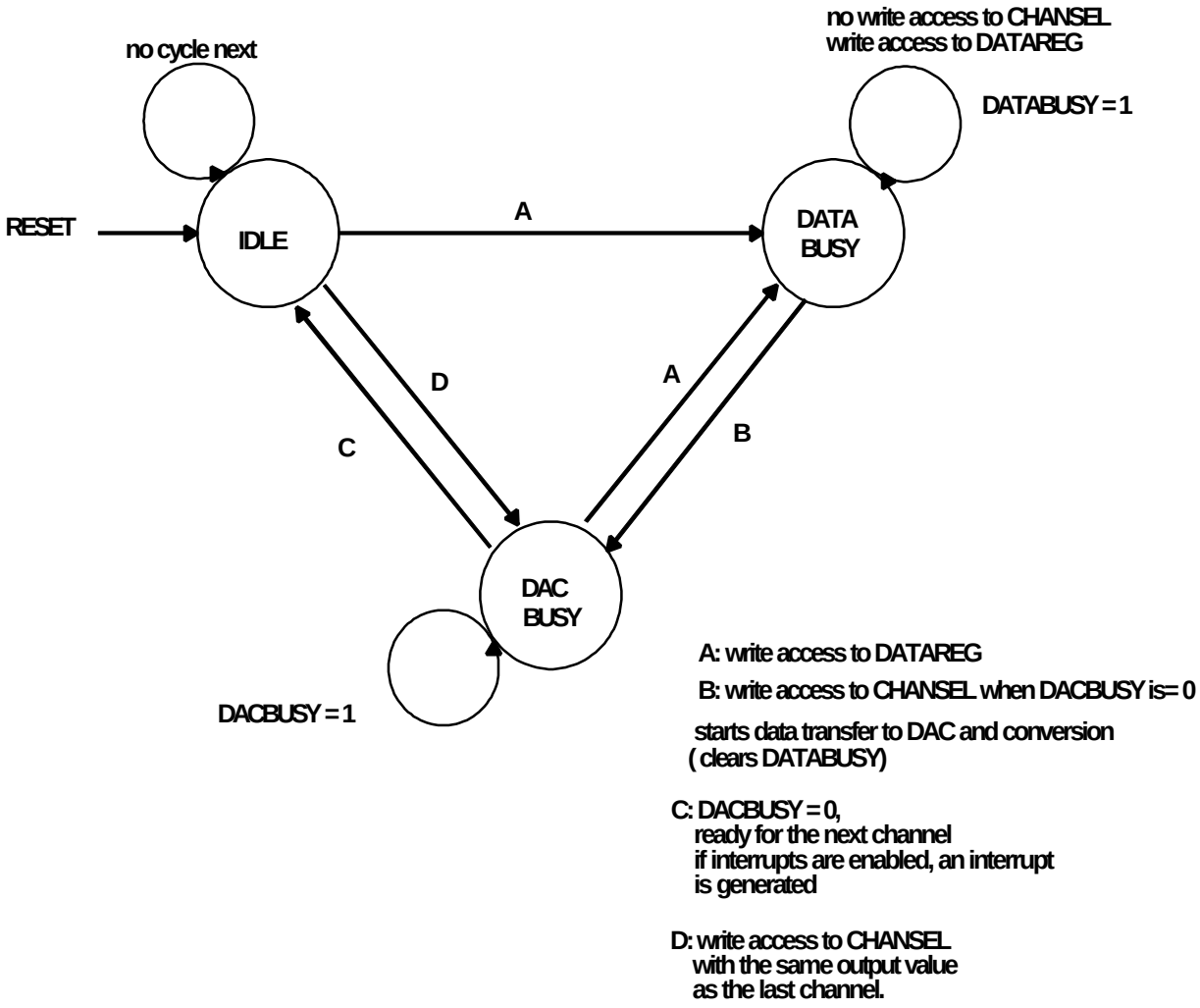


Figure 10 State Diagram DAC

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Jumper Configuration

The IP-OptoDA12 must be configured by jumperfields for the desired output voltage range ±10V or 0V to 10V. For the IP-OptoDA12-8CH it is possible to select different voltage ranges for channel 1-4 and channel 5-8. See the following table for the corresponding jumper settings.

IP-OptoDA12-8CH/4CH	**IP OptoDA12-8CH**	
Group 1 (Channel 1-4)	Group 2 (Channel 5-8)	
Voltage range ±10V:	J1, J2 1-2 installed	J3, J4 1-2 installed
Voltage range 0V to 10V:	J1, J2 2-3 installed	J3, J4 2-3 installed

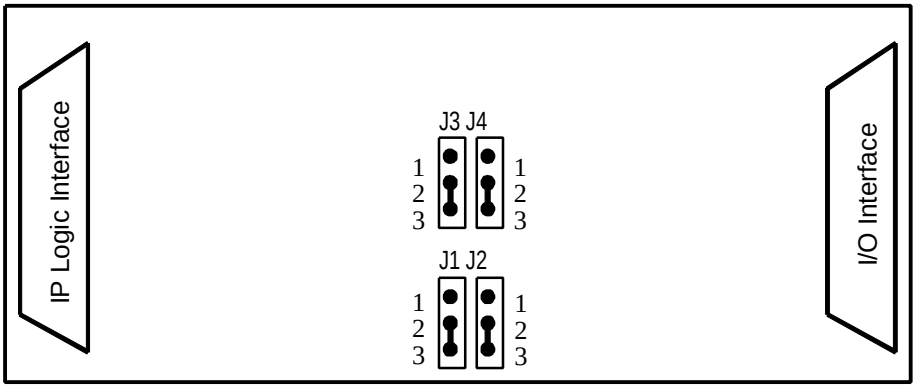


Figure 11 IP-OptoDA12 Jumper Configuration for Voltage Ranges

Note: Factory configuration is 0 to 10V for all channels.

Note: The VRGx bits of the DAC Control Register are used to select the correct set of ID PROM correction values and the output code. These bits must be configured first before reading any correction values from the ID PROM and before starting any data conversion.

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IP I/O connector

Analog Output Connections

Pin-Number	Signal	
01	DAC output 1	
02	AGND	
03	DAC output 2	
04	AGND	
05	DAC output 3	
06	AGND	
07	DAC output 4	
08	AGND	
09	DAC output 5	OptoDA12-8CH only
10	AGND	
11	DAC output 6	OptoDA12-8CH only
12	AGND	
13	DAC output 7	OptoDA12-8CH only
14	AGND	
15	DAC output 8	OptoDA12-8CH only
16	AGND	

Figure 12 IP-OptoDA12 Analog Output Connections

Power Input Connections

Pin-Number	Function
44	AGND
45	-15V
46	AGND
47	+15V
48	AGND
49	+5V
50	AGND

Figure 13 IP-OptoDA12 Power Input Connections

Note: The power input connections are reserved for special versions of the IP-OptoDA12 without on board DC/DC converter.

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Specifications

Logic Interface	IndustryPack Logic Interface
Size	single wide IP
I/O Interface	50-conductor flat cable
Analog Outputs	IP-OptoDA12-8CH: 2 groups of 4 channels IP-OptoDA12-4CH: 1 group of 4 channels
Isolation	All D/A channels are galvanically isolated from the IP Interface
Output Voltage Range	±10V or 0V to 10V, jumper selectable
Settling Time of DAC's	to 0.01% typ. 13 ms
Calibration Data	Calibration data for gain and offset correction of each channel stored in ID PROM
Output Current	±4mA for each channel
Load Capacitance	typical 2 nF
Accuracy	± 1LSB, after calibration
Linearity	± 1LSB
Wait States	IDSEL 1 wait state IOSEL 0 wait state INTSEL 0 wait state
Power Requirements	typ. 245mA @ 5V no load typ. 350mA @ 5V with 4mA output current for each channel
Environmental	Operating: -40°C to 85°C Storage: -45°C to 125°C Humidity: 5 - 95% non-condensing

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Warranty and Repair

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Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS GreenSpring will not be responsible for damages due to improper packaging of returned items. For service on SBS GreenSpring products not purchased directly from SBSGreenSpring, contact your reseller. Products returned to SBS GreenSpring for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

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SBS GreenSpring Modular I/O
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Menlo Park, CA 94025
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