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IP-UD-ID

24 Line Differential Input/Output with Interrupts IndustryPack®

User's Manual

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IP-UD-ID
24 Line Differential Input/Output with Interrupts
IndustryPack®

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Product Description

The IP-UD-ID is part of the IndustryPack™ family of modular I/O components. It provides 24 lines of digital I/O, with any line capable of generating an interrupt. All the I/O lines feature EIA-422 and EIA-485 (formerly RS422 and RS485) compatible differential drivers and receivers. Each line may be dynamically and individually configured for either input or output. Both internal read back and direct read registers are provided for ease of software development. 16-bit word and 8-bit byte operations are supported.

The IP-UD-ID conforms to the Industry Pack Interface Specification. This guarantees compatibility with multiple Support Modules. Because the IPs may be mounted on different form factors, while maintaining plug and software compatibility, system prototyping may be done on one Support Module with final system implementation on a different one.

The IP-UD-ID is software compatible with the IP-UD-IE and the IP-UD-I. The IP-UD-IE is a single ended version with TTL and CMOS level compatible I/O with SBS' unique LineSafe™ ESD protection circuit on all the I/O pins. The IP-UD-I is a single ended buffered version with 64 mA open collector output drivers and inputs which will handle +15V to –5V. Other products in the UniDig line that share common software but have different output drives are the IP-UD-ID with differential I/O, and the IP-UD-IHV-16I8O with 100V inputs and high current output switches.

The interrupt latch circuits are edge sensitive with programmable polarity and are controlled through the following five 24-bit registers: interrupt pending, interrupt request, interrupt polarity, interrupt enable, and interrupt clear. Each line corresponds to one bit in each of the registers, making programming uniform and simple. This architecture also prevents the loss of an event during the execution of the interrupt service routine.

The differential receiver for each line is always enabled, allowing the state of each I/O line to be determined at any time. The output enable for each differential transmitter is controlled by a bit in the Output Enable Register. Writing a zero to any bit in this register enables the corresponding output driver. Writing a one to any bit disables the output driver, allowing the I/O line to be used as an input. The power up default disables all the output drivers.

Input and output lines may double buffered by setting a bit in the Control Register. When this bit is set, the user must provide an external clock of up to 1 MHz. Unlike the other inputs, this is a single ended TTL level input. Another bit in the Control Register selects the polarity of this clock, allowing inputs and outputs to be latched on either the rising or falling clock edge.

Two separate locations in I/O space are provided for each signal line. The first location is used to set the output state and also to read back the written value at the internal latch. This read back function is valuable to support bit operations (which are implemented by processors as read-modify-write cycles). It is also useful in debugging, making it possible to observe directly the last written value to the port. The second location is the direct read port, which is always used for reading input values. This register may also be used to verify the correct logic signal is actually on the interface cable.

Figure 1 shows a block diagram of the IP-UD-ID.

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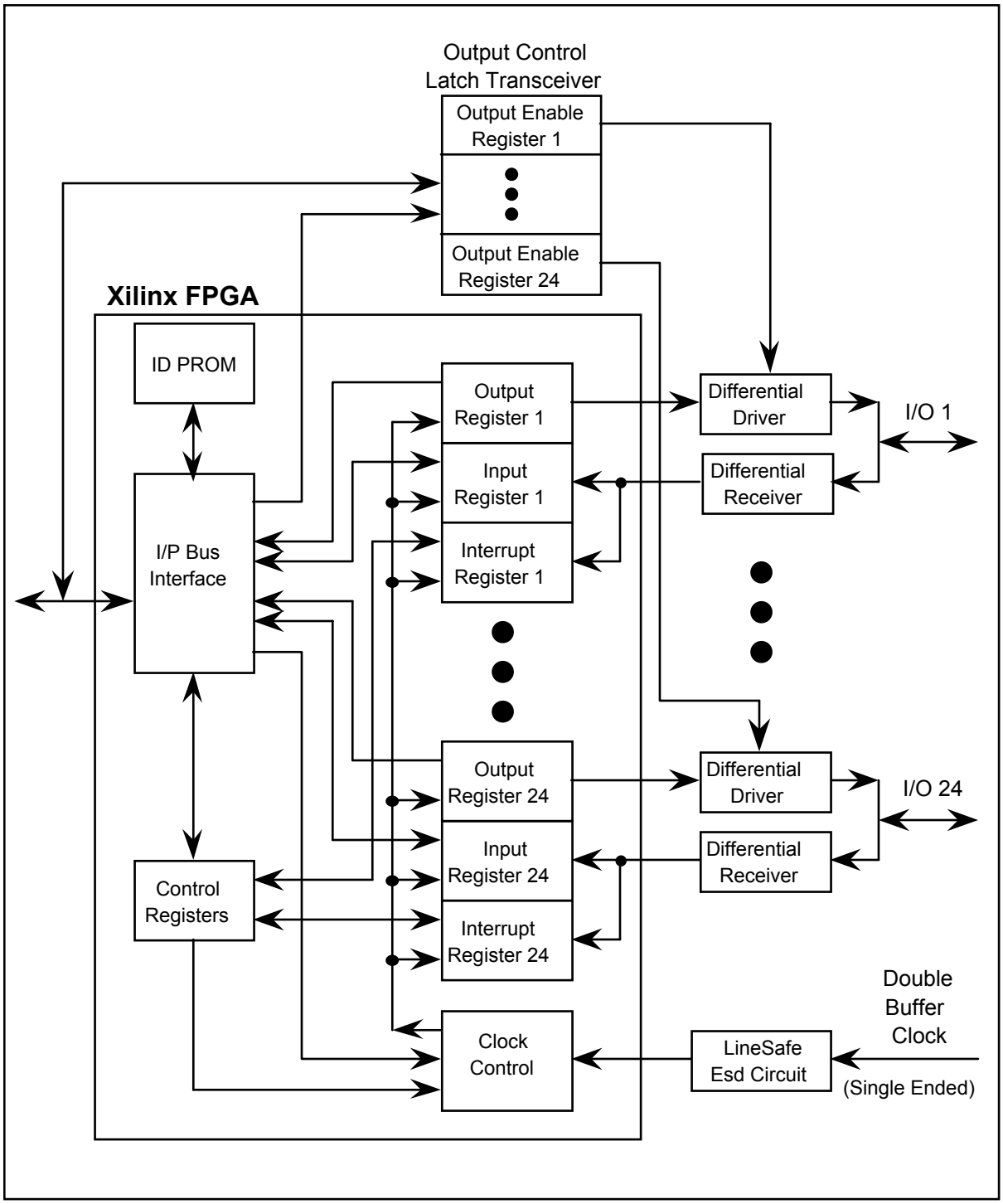


Figure 1 Simplified Block Diagram

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VMEbus Addressing

IP-UD-ID normally is accessed one word at a time in the host's I/O space. Alternatively, byte or long word accesses may be used. If long words are used, the host (or support module) must map 32-bit long words into two 16-bit cycles. This is common for 68020 and 68030 implementation of the I/O space.

Standard Word Access, I/O Space

base + $0	word	write	Output lines 1—16
base + $2	word	write	Output lines 17—24
base + $0	word	read	Read back lines 1—16
base + $2	word	read	Read back lines 17—24
base + $4	word	read	Direct read lines 1—16
base + $6	word	read	Direct read lines 17—24
base + $8	word	read/write	Output Enable Lines 1—16
base + $A	word	read/write	Output Enable Lines 17—24
base + $C	word	read/write	Control Register
base + $10	word	read/write	Interrupt Vector Register
base + $12	word	read/write	Interrupt Enable Register lines 1—16
base + $14	word	read/write	Interrupt Enable Register lines 17—24
base + $16	word	read/write	Interrupt Polarity Register lines 1—16
base + $18	word	read/write	Interrupt Polarity Register lines 17—24
base + $1A	word	write	Interrupt Clear Register lines 1—16
base + $1C	word	write	Interrupt Clear Register lines 17—24
base + $1A	word	read	Interrupt Pending Register lines 1—16
base + $1C	word	read	Interrupt Pending Register lines 17—24

Figure 2 VME Bus Addressing, Word Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for word accesses.

Bit map of words at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

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Bit map of words at base + $2, base + $6, base + $14, base + $18 and base + $1C

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of words at base + $8

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output En:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $A

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output En:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of word at base + $C

Data Bit #	[15:2]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

Bit map of the Interrupt Vector Register at base + $10

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vec. Bit:	-	-	-	-	-	-	-	-	7	6	5	4	3	2	1	0

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

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Alternate Byte Access, I/O Space

base + $0	byte	write	Output lines 9—16
base + $1	byte	write	Output lines 1—8
base + $3	byte	write	Output lines 17—24
base + $0	byte	read	Read back lines 9—16
base + $1	byte	read	Read back lines 1—8
base + $3	byte	read	Read back lines 17—24
base + $4	byte	read	Direct read lines 9—16
base + $5	byte	read	Direct read lines 1—8
base + $7	byte	read	Direct read lines 17—24
base + $8	byte	read/write	Output Enable Lines 9—16
base + $9	byte	read/write	Output Enable Lines 1— 8
base + $B	byte	read/write	Output Enable Lines 17—24
base + $D	byte	read/write	Control Register
base + $11	byte	read/write	Interrupt Vector Register
base + $12	byte	read/write	Interrupt Enable Register lines 9—16
base + $13	byte	read/write	Interrupt Enable Register lines 1—8
base + $15	byte	read/write	Interrupt Enable Register lines 17—24
base + $16	byte	read/write	Interrupt Polarity Register lines 9—16
base + $17	byte	read/write	Interrupt Polarity Register lines 1—8
base + $19	byte	read/write	Interrupt Polarity Register lines 17—24
base + $1A	byte	write	Interrupt Clear Register lines 9—16
base + $1B	byte	write	Interrupt Clear Register lines 1—8
base + $1D	byte	write	Interrupt Clear Register lines 17—24
base + $1A	byte	read	Interrupt Pending Register lines 9—16
base + $1B	byte	read	Interrupt Pending Register lines 1—8
base + $1D	byte	read	Interrupt Pending Register lines 17—24

Figure 3 VME Bus Addressing, Byte Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for byte accesses.

Bit map of bytes at base + $1, base + $5, base + $13, base + $17 and base + $1B

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

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Bit map of bytes at base + $3, base + $7, base + $15, base + $19 and base + $1D

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of bytes at base + $8

Data Bit #	7	6	5	4	3	2	1	0
Output En:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $9

Data Bit #	7	6	5	4	3	2	1	0
Output En:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $A

Data Bit #	7	6	5	4	3	2	1	0
Output En:	24	23	22	21	20	19	18	17

Bit map of byte at base + $D

Data Bit #	[7:2]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

Bit map of the Interrupt Vector Register at base + $11

Data Bit #	7	6	5	4	3	2	1	0
Vec. Bit:	7	6	5	4	3	2	1	0

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Alternate Long Word Access, I/O Space

base + $0	long	write	Output lines 1—24
base + $0	long	read	Read back lines 1—24
base + $4	long	read	Direct read lines 1—24
base + $8	long	read/write	Output Enable Lines 1—24
base + $C	long	read/write	Control Register
base + $10	long	read/write	Interrupt Vector Register
base + $12	long	read/write	Interrupt Enable Register lines 1—24
base + $16	long	read/write	Interrupt Polarity Register lines 1—24
base + $1A	long	write	Interrupt Clear Register lines 1—24
base + $1A	long	read	Interrupt Pending Register lines 1—24

Figure 4 VME Bus Addressing, Long Word Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for long word accesses.

Bit map of long words at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of long words at base + $8

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Output En:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output En:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

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Bit map of long word at base + $C

Data Bit #	[31:18]	17	16	[15:0]
Write:	-	Clock Polarity	Dbl. Buffer En.	-
Read:	0	Clock Polarity	Dbl. Buffer En.	0

Bit map of long word at base + $10

Data Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Vec. Bit:	-	-	-	-	-	-	-	-	7	6	5	4	3	2	1	0

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vec. Bit:	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

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NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

NuBus byte address = (VMEbus byte address * 2) – 1

All byte data is still transferred on data lines D7..D0.

Word addresses on the NuBus are the same as for VME. Word data is transferred on data lines D15..D0.

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ISA (IBM PC-AT) Addressing

Both word and byte address modes are supported by the IP-UD-ID. The actual application will depend on the carrier card. See the carrier card manual for details.

Standard Word Access, I/O Space

base + $0	word	write	Output lines 1—16
base + $2	word	write	Output lines 17—24
base + $0	word	read	Read back lines 1—16
base + $2	word	read	Read back lines 17—24
base + $4	word	read	Direct read lines 1—16
base + $6	word	read	Direct read lines 17—24
base + $8	word	read/write	Output Enable Lines 1—16
base + $A	word	read/write	Output Enable Lines 17—24
base + $C	word	read/write	Control Register
base + $10	word	read/write	Interrupt Vector Register
base + $12	word	read/write	Interrupt Enable Register lines 1—16
base + $14	word	read/write	Interrupt Enable Register lines 17—24
base + $16	word	read/write	Interrupt Polarity Register lines 1—16
base + $18	word	read/write	Interrupt Polarity Register lines 17—24
base + $1A	word	write	Interrupt Clear Register lines 1—16
base + $1C	word	write	Interrupt Clear Register lines 17—24
base + $1A	word	read	Interrupt Pending Register lines 1—16
base + $1C	word	read	Interrupt Pending Register lines 17—24

Figure 5 ISA Bus Addressing, Word Access

Each I/O line corresponds to one bit in each register except the Interrupt Vector Register. The following map shows the bit correspondence for word accesses.

Bit map of words at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $2, base + $6, base + $14, base + $18 and base + $1C

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I/O Line:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

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Bit map of words at base + $8

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output En:	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1

Bit map of words at base + $A

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Output En:	-	-	-	-	-	-	-	-	24	23	22	21	20	19	18	17

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

Bit map of word at base + $C

Data Bit #	[15:2]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

Bit map of the Interrupt Vector Register at base + $10

Data Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Vec. Bit:	-	-	-	-	-	-	-	-	7	6	5	4	3	2	1	0

Note: data in bits 15 through 8 are ignored in writes, read as "0"s.

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Alternate Byte Access, I/O Space

base + $0	byte	write	Output Lines 1—8
base + $1	byte	write	Output Lines 9—16
base + $2	byte	write	Output Lines 17—24
base + $0	byte	read	Read-back Lines 1—8
base + $1	byte	read	Read-back Lines 9—16
base + $2	byte	read	Read-back Lines 17—24
base + $4	byte	read	Direct Read Lines 1—8
base + $5	byte	read	Direct Read Lines 9—16
base + $6	byte	read	Direct Read Lines 17—24
base + $8	byte	read/write	Output Enable Lines 1—8
base + $9	byte	read/write	Output Enable Lines 9—16
base + $A	byte	read/write	Output Enable Lines 17—24
base + $C	byte	read/write	Control Register
base + $10	byte	read/write	Interrupt Vector Register
base + $12	byte	read/write	Interrupt Enable Register lines 1—8
base + $13	byte	read/write	Interrupt Enable Register lines 9—16
base + $14	byte	read/write	Interrupt Enable Register lines 17—24
base + $16	byte	read/write	Interrupt Polarity Register lines 1—8
base + $17	byte	read/write	Interrupt Polarity Register lines 9—16
base + $18	byte	read/write	Interrupt Polarity Register lines 17—24
base + $1A	byte	write	Interrupt Clear Register lines 1—8
base + $1B	byte	write	Interrupt Clear Register lines 9—16
base + $1C	byte	write	Interrupt Clear Register lines 17—24
base + $1A	byte	read	Interrupt Pending Register lines 1—8
base + $1B	byte	read	Interrupt Pending Register lines 9—16
base + $1C	byte	read	Interrupt Pending Register lines 17—24

Figure 6 ISA Bus Addressing, Byte Access

Bit map of bytes at base + $0, base + $4, base + $12, base + $16 and base + $1A

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $1, base + $5, base + $13, base + $17 and base + $1B

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	16	15	14	13	12	11	10	9

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Bit map of bytes at base + $2, base + $6, base + $14, base + $18 and base + $1C

Data Bit #	7	6	5	4	3	2	1	0
I/O Line:	24	23	22	21	20	19	18	17

Bit map of bytes at base + $8

Data Bit #	7	6	5	4	3	2	1	0
Output En:	8	7	6	5	4	3	2	1

Bit map of bytes at base + $9

Data Bit #	7	6	5	4	3	2	1	0
Output En:	16	15	14	13	12	11	10	9

Bit map of bytes at base + $A

Data Bit #	7	6	5	4	3	2	1	0
Output En:	24	23	22	21	20	19	18	17

Bit map of byte at base + $C

Data Bit #	[7:2]	1	0
Write:	-	Clock Polarity	Dbl. Buffer En.
Read:	0	Clock Polarity	Dbl. Buffer En.

Bit map of the Interrupt Vector Register at base + $10

Data Bit #	7	6	5	4	3	2	1	0
Vec. Bit:	7	6	5	4	3	2	1	0

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I/O Pin Wiring

This section gives the pin assignments and wiring recommendations for IP-UD-ID.

The pin numbers given in Figure 7 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

I/O 1+	1	I/O 1–	2
I/O 2+	3	I/O 2–	4
I/O 3+	5	I/O 3–	6
I/O 4+	7	I/O 4–	8
I/O 5+	9	I/O 5–	10
I/O 6+	11	I/O 6–	12
I/O 7+	13	I/O 7–	14
I/O 8+	15	I/O 8–	16
I/O 9+	17	I/O 9–	18
I/O 10+	19	I/O 10–	20
I/O 11+	21	I/O 11–	22
I/O 12+	23	I/O 12–	24
I/O 13+	25	I/O 13–	26
I/O 14+	27	I/O 14–	28
I/O 15+	29	I/O 15–	30
I/O 16+	31	I/O 16–	32
I/O 17+	33	I/O 17–	34
I/O 18+	35	I/O 18–	36
I/O 19+	37	I/O 19–	38
I/O 20+	39	I/O 20–	40
I/O 21+	41	I/O 21–	42
I/O 22+	43	I/O 22–	44
I/O 23+	45	I/O 23–	46
I/O 24+	47	I/O 24–	48
Double Buffer Clk	49	GND	50

Figure 7 I/O Pin Assignment

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IndustryPack Logic Interface Pin Assignment

Figure 8 below gives the pin assignments for the IndustryPack Logic Interface on the IP-UD-ID. Pins marked n/c below are defined by the specification, but are not used on IP-UD-ID. Also see the User Manual for your IP Carrier board for more information.

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	n/c 5	30	
D2	n/c	6	31
D3	n/c 7	32	
D4	INTSel*	8	33
D5	n/c 9	34	
D6	IOSel*	10	35
D7	n/c 11	36	
D8	A1	12	37
D9	n/c 13	38	
D10	A2	14	39
D11	n/c 15	40	
D12	A3	16	41
D13	IntReq0*	17	42
D14	A4	18	43
D15	n/c 19	44	
BS0*	A5	20	45
BS1*	n/c 21	46	
–12V	A6	22	47
+12V	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 8 Logic Pin Assignment

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Programming

Programming the IP requires only the ability to read and write data in the host's I/O space. The base address is determined by the IP Support Module. This document refers to this address as "base".

Initialization

The IP-UD-ID does not require any special initialization sequence. However, upon reset, the IP requires a minimum delay of 300 milliseconds before any accesses are made by the host system. This is the time it takes the Xilinx FPGAs to configure themselves. All the registers are cleared on reset, and all I/O lines are set to be inputs.

Data I/O

Each of the 24 bits may be individually set as input or output. To set a bit to be input, write a "1" to the I/O bit location. This is the default on reset.

Each of the 24 I/O lines has a differential transceiver on it. This makes it possible to individually set each bit as input or output. The receiver circuit in the transceiver is always enabled, allowing the user to read the state of the I/O line at any time. The transmitter circuit in the transceiver must be enabled to make a bit an output. The enable for each transmitter is controlled by a corresponding bit in the Output Control Register. Writing a "0" to a bit in the Output Control Register will turn on that bit's output transmitter, making it an output. The value written to the Output Register will then appear on the I/O line. Writing a "1" to a bit in the Output Control Register will turn off the transmitter, making the bit an input. The Output Control Register defaults to all "1"s on reset, disabling all the output transmitters.

Data may be read from two sets of address locations. The first set of locations, base + 0x0 and base + 0x2 for word operations, function as the Internal Read Back Register. The data latched in the Output Latch is read from these addresses. They support processor bit operations implemented as read-modify-write cycles, and are also useful for debugging purposes.

The second set of locations, base + 0x4 and base + 0x6 for word operations, is the Direct Read Register. Data is latched into the Input Register on the rising edge of the 8 MHz IP Clock. Figure 11 in the Theory of Operations section shows a block diagram.

Using word access, up to 16 bits may be programmed at once. The IP implements a read back register at the same address used for writing to the signal line I/O bits. This permits "set bit" and "clear bit" instructions to be used in programming, which are implemented by the host hardware as read-modify-write cycles. Thus, single bits at well as bit fields may be accessed.

The IP may also be accessed using byte or long word accesses. If long word accesses are used from a 68020, 68030, or 68040 host, the I/O space must be mapped into "D16". 68000 and 68010 hosts internally map all long word accesses into 16 bits, so no special precaution is necessary.

Inputs and outputs may be double buffered by providing an external TTL level clock on Pin 49 of the I/O connector. This clock must have an edge rate faster than 60 ns. When double buffering is enabled, data will be latched by the external clock, allowing

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multiple IPs to be synchronized. The IP uses a Control Register to enable double buffering and control the polarity of the Double Buffer Clock.

Bit #	Definition	Access
0	Double Buffer Enable	Read/Write
1	Double Buffer Clock Polarity Select	Read/Write
2—7	Reserved	Read as "0"

Figure 9 Control Register Bit Definitions

Control Register Bit Definitions:

Bit [0] = D0 LSB Double Buffer Enable
Double Buffer Enable bit. This bit enables double buffering. If this bit is set to a "1", the user must provide a TTL level clock on the Double Buffer Clock, pin 49. This clock may be up to 1 MHz and must have an edge rate faster than 60 ns. Writing a "0" disables double buffering. This is the default.

Bit [1] = D1 Double Buffer Clock Polarity Select
Double Buffer Clock Polarity Select bit. This bit controls the Double Buffer Clock polarity. Writing a "1" will cause output data to be latched out of the IP and input data to be latched into the IP on the falling edge of the Double Buffer Clock. Writing a "0" will cause data to be latched on the rising edge of the Double Buffer Clock. This is the default.

Bit [7..2] Reserved
These bits are reserved for future use and will be read as "0"

Double Buffering

Double buffering is a feature that allows all the inputs and outputs to be latched at the same time, whether on a single IP or a system with multiple IPs. This is useful for systems that require many inputs and outputs to be updated simultaneously. To use double buffering, an external single ended TTL compatible clock with an edge rate faster than 60 ns must be provided on Pin 49, the Double Buffer Clock Input pin. The Double Buffer Enable bit, Bit [0], in the Control Register must also be set. The Double Buffer Clock polarity is programmable via the Double Buffer Clock Polarity bit, Bit [1], in the Control Register. Setting this bit to a "0" will cause the input and outputs to be latched on the rising edge of the Double Buffer Clock, while setting the bit to "1" will latch the inputs and outputs on the falling edge.

Interrupts

The IP-UD-ID uses five 24-bit registers to control interrupt generation. Each bit in each register corresponds to one I/O line, simplifying software development. Inputs are not debounced. Users may need to provide this feature either in software or with external hardware if noisy inputs, such as mechanical switches, are used to generate interrupts. Interrupts from all enabled I/O lines are OR'd together and are asserted on IntReq0*. The IP responds to an interrupt cycle be putting out its 8-bit vector from the Interrupt Vector Register onto the data bus.

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Interrupt Enable Register

The Interrupt Enable Register is used to enable and disable interrupts from individual I/O channels. Programming any bit to a "1" enables an interrupt from the corresponding I/O channel. Programming any bit to a "0" disables an interrupt from the corresponding I/O channel.

For the IP to actually request an interrupt, an edge or level must be seen on the corresponding I/O channel. Since the IP monitors interrupts regardless of the state of the enable bit, it is possible to get an interrupt immediately upon enabling any bit in this register.

The Interrupt Enable Register is cleared on reset. Thus, all channels are disabled from generating interrupts on reset.

Interrupt Polarity Register

The Interrupt Polarity Register is used to set the polarity of the transition that is to generate an interrupt for each I/O channel. Programming any bit to a "1" will generate an interrupt when the input data changes from a logic zero to a logic one on the corresponding I/O channel. Programming any bit to a "0" will generate an interrupt when the input data changes from a logic one to a logic zero. For the IP to actually request an interrupt, the corresponding bit in the Interrupt Enable Register must be "1".

The Interrupt Polarity Register is cleared on reset. This makes the default to interrupt on a falling edge for all I/O channels.

The IP's logic monitors writing to this register. If a bit in this register is changed, and the static input on the corresponding channel matches the programmed bit, the interrupt flip-flop for that channel is set. This feature is critical to prevent the loss of an interrupt due to a channel transition that might occur during an interrupt service routine.

Example: The software reads an input, determines it is zero, then enable that channel to generate an interrupt on a rising edge. Between the read and the write, however, the input changed to one. With this special logic, an interrupt is immediately generated, or generated at the end of the current routine if interrupts are masked. Without the logic, the input transition would have been lost.

If the software does not care what the current state of the input channels are and does not wish to receive any immediate interrupts, then the procedure is (1) disable interrupts in the processor, (2) program the IP's Polarity Register, (3) write to all channels of the Clear Interrupt Register, (4) enable interrupts in the processor.

Inverting a bit in this register each time the corresponding bit generates an interrupt will result in an interrupt for both rising and falling edges.

Clear Interrupt Register and Pending Interrupt Register

These two registers are used to detect and clear pending interrupts from any combination of channels. Both registers access the same interrupt flip-flops. They are arranged as one read-only register, the Pending Interrupt Register, and one write-only register, the Clear Interrupt Register.

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The flip-flops that make up these two registers are set only by a transition on an input channel of the programmed polarity. They are cleared by the software writing to the Clear Interrupt Register or by IP Reset.

Reading a one in the Pending Interrupt Register means the corresponding channel either has generated an interrupt if that channel is enabled, or has an interrupt pending if that channel is disabled. A pending interrupt will drive the interrupt request line as soon as the corresponding bit in the Interrupt Enable Register is set to "1".

Both interrupts and pending interrupts are cleared for any channel by writing a one to the corresponding bit position in the Clear Interrupt Register. In general, only channels which have been detected as pending by a read of the Pending Interrupt Register should be cleared. This will prevent the loss of an interrupt that arrives between the read and write. If the write to the Clear Interrupt Register were to be all "1"s, an interrupt arriving on a new channel between the read and write would be lost. Writing a "0" to any bit in the Clear Interrupt Register has no affect on the corresponding channel.

Note that for simplicity, the host software need only read the Pending Interrupt Register, then immediately write the same value to the Clear Interrupt Register. The software may then check the bits in that byte, taking whatever actions are required by the one or more channels recognized to need service.

To clear all pending and latent interrupts, the software writes all "1"s to the Clear Interrupt Register. The Pending Interrupt register is cleared on reset, which clears all interrupts and pending interrupts.

Interrupt Vector Register

The IP has an 8-bit read/write register to hold the interrupt vector required to service IP interrupts.

All interrupts from one IP-UD-ID use the same vector. The Pending Interrupt Register is used to determine what combination of channels need service. This allows the software to handle any number of equally weighted channels in a single interrupt service routine.

This register is cleared on reset.

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ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-UD-ID is shown in Figure 10 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from SBS Technologies. The ID PROM on the IP-UD-ID is implemented in the Xilinx FPGA device.

The location of the ID PROM in the host's address space is dependent on the carrier board used. For most VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 19	(available for user)
17 (0F)	CRC for bytes used
15 (0C)	No of bytes used
13 (00)	Driver ID, high byte
11 (00)	Driver ID, low byte
0F (00)	reserved
0D (A1)	Revision
0B (69)	Model No IP-UD-ID
09 (F0)	Manufacturer ID SBS (GreenSpring)
07 (43)	ASCII "C"
05 (41)	ASCII "A"
03 (50)	ASCII "P"
01 (49)	ASCII "I"

Figure 10 ID PROM Data (hex)

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Theory of Operation

IndustryPack Standards

The IP-UD-ID is part of the IndustryPack™ family of modular I/O products. It meets the IndustryPack Logic Specification. (Contact SBS Technologies for a copy of this Specification.) It is assumed the reader is at least casually familiar with both this document and 68000 processor architecture.

Control Logic

All control logic is contained within a two Xilinx FPGAs. They are clocked by the 8 MHz IP Logic clock from the Support Module. The IP responds to I/O and ID selects. It does not respond to memory selects, however the MEMSel* line is routed to the FPGA, enabling easy modification for special needs.

The IP does not require wait states for either read or write cycles. Thus, the FPGA generates Ack* on the clock cycle following either I/O or ID Select. Hold cycles (from the Support Module) are supported for both read and write cycles by extending Ack* as required. If no hold cycles are requested by the Support Module, the IP is capable of supporting the full 8 MByte per second data transfer rate of the IP Logic Interface Specification.

I/O Data Lines

All input and output latches are contained within the Xilinx FPGA. Each I/O line has a EIA-485/EIA-422 differential transceiver with an extended common mode range of +12V to -7V. A socketed 8-pin SIP resistor network provides parallel termination to groups of four transceivers. A 100Ω value is the factory default value, though the user may substitute other values if desired. The resistor network may be removed if no termination is desired, or individual leads may be cut off if terminations are required only for specific I/O lines.

Data Output

Each differential transceiver's transmitter has an output enable that is controlled by a corresponding bit in the Output Enable Register. When the bit in the Output Enable Register is set to a "0", the transmitter is enabled and the data written to the Output Register will appear on the I/O line. When the bit in the Output Enable Register is set to a "1", the transmitter outputs maintain a high impedance over the entire common mode range.

Each output has two latches associated with it. If double buffering is enabled, the Double Buffer Latch is clocked by the Double Buffer Clock. Without double buffering, this latch is clocked on the falling edge of the IP Clock. Figure 11 shows a block diagram. Outputs from the Double Buffer Latch directly drive the I/O output lines. Data is latched into the internal latch on the rising edge of the IP Clock after the IOSel* line is driven low.

Double buffering is enabled by setting the Double Buffer Enable Bit (bit [0]) in the Control Register to a "1". A single ended TTL compatible signal must be provided on the External Clock, pin 49. This signal must have an edge rate faster than 60 ns. If double buffering is enabled, the Double Buffer Clock Polarity Bit (bit [1]) in the Control Register is used to set the Double Buffer Clock polarity. Setting the Double

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Buffer Clock Polarity Bit to a "0" will latch data on the rising edge and setting it to a "1" will latch data on the falling edge. The power up default is "0" for both these bits.

Data Input

The data may be read from two sets of address locations. The first set of locations, base + 0 and base + 2 for word operations, function as the Internal Read Back Register. The data latched in the Internal Output Latch is read from these addresses. They support processor bit operations implemented as read-modify-write cycles, and are also useful for debugging purposes.

The second set of locations, base + 4 and base + 6 for word operations, is the Direct Read Register. Data is latched into Input Register with the same clock that latches the Double Buffer Latch. Figure 11 shows a block diagram.

Interrupts

The interrupt generation circuitry consists of an edge detector and a level sensor that feed the input of a latch. The edge detector uses two latches in series clocked by the 8 MHz IP Clock to compare the current state of the I/O line with the previous state. If the two states are different and the difference matches the polarity set in the Polarity Register, the Interrupt Latch is set. If the Interrupt Enable bit is set for that I/O line, an interrupt is generated on IntReq0*. This series of latches means there will be a minimum 125 ns. delay (one 8 MHz clock pulse) from the time the I/O line transitions until the interrupt is generated. Individual interrupts are cleared by writing a "1" to the corresponding bit in the Interrupt Clear Register.

The level sensor is only active when writing to the Interrupt Polarity Register. If a "1" is written to a bit in the Interrupt Polarity Register, corresponding to a rising edge interrupt, and the level on the I/O line is already a "1", the level sensor will generate a pending interrupt. If the Interrupt Enable bit is set for that I/O line, an interrupt is generated on IntReq0*. This can be used to ensure an edge will not be missed when generating interrupts on both the rising and falling edge. In this case, the interrupt service routine (ISR) should change the Interrupt Polarity Register. If the I/O line has transitioned already, an interrupt will be generated immediately. When the ISR completes, the interrupt will be waiting.

If a bit is used as an output, it will still generate an interrupt when it is written to if the corresponding bit in the Interrupt Enable Register is set. If this is undesired, care must be taken to enable interrupts only for those bits used as input.

Figure 11 shows a block diagram of the structure for each I/O line.

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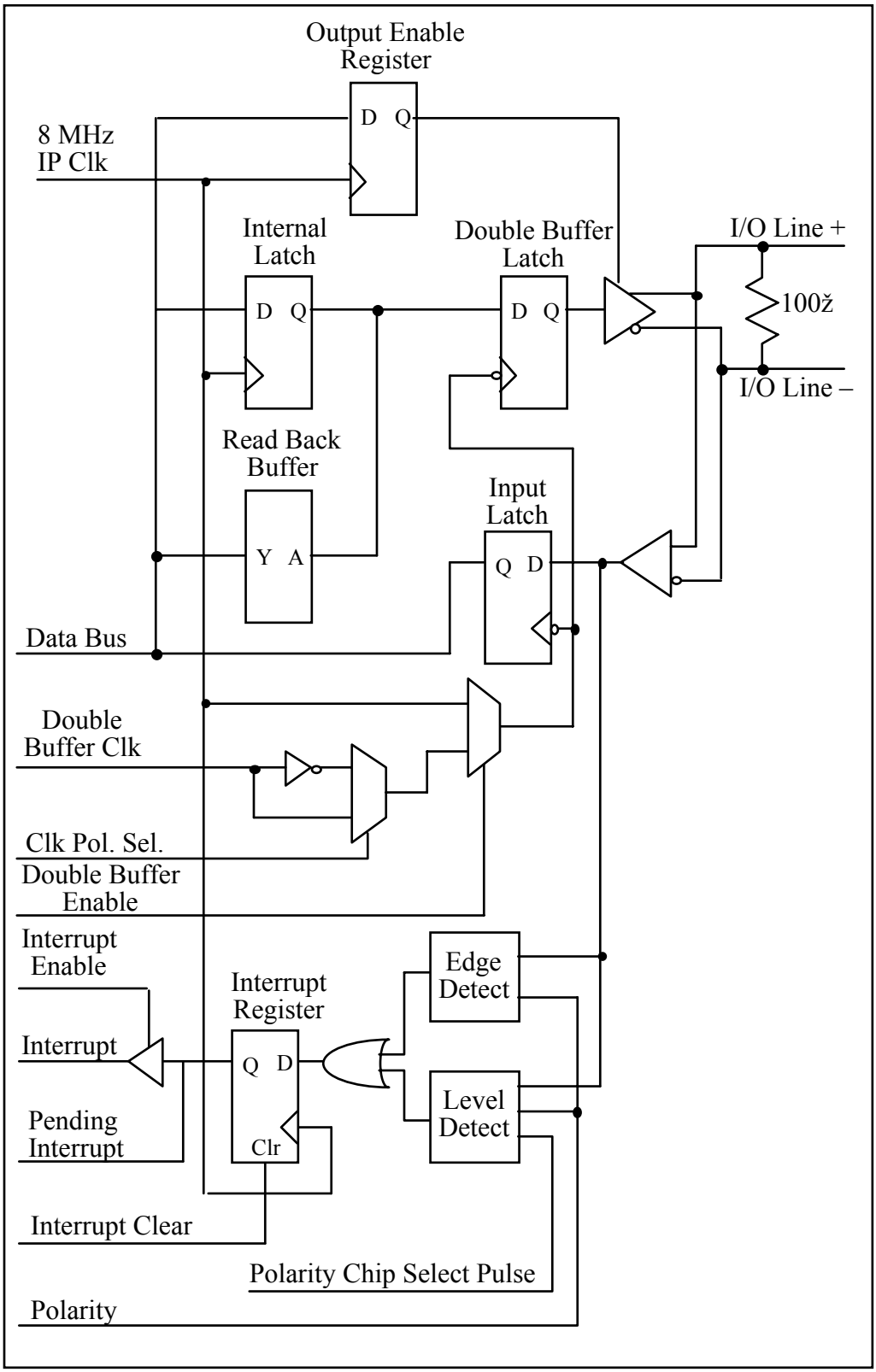


Figure 11 I/O Line Block Diagram

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Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-UD-ID is constructed out of 0.062 inch thick FR4 V0 material. The six copper layers consist of two signal layers on the top and bottom, and two internal power and ground plane layers and two internal signal layers.

Through hole and surface mounting of components are used. IC sockets use gold plated screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and have gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four M2 metric stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of 0.31 W/m-°C, taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, then the temperature difference between the component and the solder side is one degree Celsius.

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Repair

Service Policy

Before returning a product for repair, verify as soon as possible that the suspected unit is at fault; then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if it is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include the return address and telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS Technologies will not be responsible for damages due to improper packaging of returned items. For service of SBS Technologies products not purchased directly from SBS Technologies, contact your reseller. Products returned to SBS Technologies for repair by other than the original customer will be treated as out-of-warranty.

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FAX: (651) 905-4701
Email: support.commercial@sbs.com

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Specifications

Logic Interface	IndustryPack™ Logic Interface.
Digital Interface and	24 digital signal lines with double buffered inputs outputs. Each line is either an input or an output.
Interface Level	EIA-422 and EIA-485 compatible, short circuit protected. Outputs: 3 Volt Common Mode Output. Inputs: Common Mode range –7V to +12V with 70 mV of hysteresis.
Software Interface	Seven 24-bit registers: Output Read Back Input Interrupt Enable Interrupt Pending Interrupt Polarity Interrupt Clear Two 8-bit registers: Control Interrupt Vector
Initialization	300 millisecond delay from reset. Forces all lines to be inputs. Clears all registers. Clears and disables all interrupts. Disables Double Buffering.
Interrupts	All lines can be programmed to generate an interrupt. Programmable polarity - rising or falling edge. Interrupts are cleared by writing a 1 to the appropriate interrupt clear bit. Programmable vector.
Access Mode	Byte or word in I/O Space. Byte or word in ID Space.
Wait States	Zero
Transfer Rate	8 Mbytes/second maximum, continuous.
Onboard Options	All options are software programmable.
Dimensions	Standard Single High Industry Pack width and length 1.8 x 3.9 inches.
Construction:	Conformal Coated FR4 4 layer Printed Circuit. Surface mounted components.
Temperature Coefficient:	0.89 W/°C for uniform heat across IP.
Power Requirements	+5.0 VDC, 60 mA typical.

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