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SBS Technologies, Inc.

www.sbs.com

IP-Unidig-HV

IndustryPack Module With 24 High Voltage I/O Lines

Application Information

The IP-UniDig-HV provides high voltage inputs and outputs. Two variants are available: the -16I8O has 16 inputs and 8 outputs and the -8I16O has 8 inputs and 16 outputs. Both inputs and outputs are double buffered, providing an ideal solution for simulation systems requiring many inputs and outputs to be latched simultaneously.

Outputs use NMOS power FET low side switches with an off-state voltage of up to 50 Volts. The switches sink up to one Amp of continuous load current as long as the aggregate current through the IndustryPack is limited to 8 Amps. Channels may be ganged for higher drive currents. Writing a one to an output turns on the switch, writing a zero turns it off.

Inputs use differential amplifiers which handle from 0 to 100 Volts. The outputs of the amplifiers feed comparators with a programmable threshold. A 12 bit D/A converter is used to set the threshold from 0 to 60 Volts with 15 mV resolution. The outputs of the comparators are latched into data latches. When the differential input voltage is greater than the threshold voltage, the input latch will be read as a logic one.

If double buffering is required, an external clock source must be provided to latch the input and output registers. An EIA-422 differential receiver is used for this clock for greater noise immunity. The IP-UniDig-T-D is ideally suited for generating this clock, though any differential source may be used. Double buffering is controlled by a bit in the Control Register.

Reset turns off the output switches and disables double buffering to provide a consistent software interface.

A subroutine library and Windows NT drivers are available.

Features

- 24 high voltage I/O lines on a single-wide IndustryPack
- 1000 mA 50V output operation
- 100 V input operation
- Programmable input voltage threshold
- Available as 16 inputs and 8 outputs or 16 outputs and 8 inputs
- Double-buffered input and output
- External clock triggers double-buffering

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Specifications

Form Factor	Single-wide Type I IndustryPack
IndustryPack Interface	Complies with ANSI/VITA-4
Interface Speed	8 MHz
Wait States	None
Number of Input Lines	-16I8O: Sixteen –8I16O: Eight
Number of Output Lines	-16I8O: Eight –8I16O: Sixteen
Input Drivers	Programmable logic threshold 0 to 100 V in 15 mV steps Input clock is EIA-422 differential with –7 V to +12 V operation and 70 mV hysteresis
Output Drivers	Low side FET switches 50 V max @ 1A (8A max per IndustryPack)
ESD Protection	None
Interrupts	None
Dimensions	1.8 inches x 3.9 inches
Weight	0.06 kg (0.1 lb)
Power Requirements (no load)	+5 VDC, 130 mA typ +12 VDC, 10 mA typ –12 VDC, 20 mA typ
Environmental	Operating temperature: -0 to +70°C Humidity: 5 to 95% non-condensing Storage: –40 to +85°C

SBS Technologies, Inc.
8371C Central Avenue, Newark, CA 94560
(510) 742-2500 • sales.mio@sbs.com • www.sbs.com

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Ordering Information

IP-UNIDIG-HV-16I8O	IndustryPack with 16 high voltage input and 8 high voltage output lines
IP-UNIDIG-HV-8I16O	IndustryPack with 8 high voltage input and 16 high voltage output lines
EKIP50-UNIDIG16	Engineering kit for IP-Unidig-HV if mounted on a carrier with 50-pin ribbon cable header front panel I/O connectors. Contains: Six foot 50 conductor ribbon cable (C-IP50F-IP50F-6) Fifty screw terminal block with ribbon header (IP-TERM) *(More items as below)*
EKHD50-UNIDIG16	Engineering kit for IP-Unidig-HV if mounted on a carrier with HD50 front panel I/O connectors. Contains: Six foot cable HD50 male to HD50 male (C-HD50M-HD50M) Fifty screw terminal block with HD50 female (IP-TERM-HD50) *(More items as below)*
EKCM50-UNIDIG16	Engineering kit for IP-Unidig-HV if mounted on a carrier with Champ50 front panel I/O connectors. Contains: Six foot Champ50 male to HD50 male cable (C-HD50M-CM50M) Fifty screw terminal block with HD50 female (IP-TERM-HD50) *(More items as below)*
All IP-UNIDIG-HV engineering kits include:	Printed hardware user manual Bill of materials Board schematics Assembly diagram Sipex: SP481/485 data sheet National Semiconductor: LM339A and LM324A data sheets Siliconix: SI9945DY data sheet Linear Tech: LTC1257CS8 data sheet
QP-UNIDIG-DIG	QuickPack subroutine library for IP-Unidig-HV. Contains: Printed software user manual Floppy Disk containing: C source code Release notes
ND-SDPACK	Windows NT 4.0 SDpacK IndustryPack driver CDROM

Associated Products

IP-UNIDIG-IHV-16I8O	IndustryPack with 16 high voltage input and 8 high voltage output lines and interrupts
IP-UNIDIG-IHV-8I16O	IndustryPack with 8 high voltage input and 16 high voltage output lines and interrupts
C-IP50M-IP50M-3	Three foot 50 conductor ribbon cable
C-IP50M-IP50M-6	Six foot 50 conductor ribbon cable
C-CM50M-IP50M	Three foot Champ50 male to ribbon cable
C-HD50M-HD50M	Six foot HD50 male to HD50 male cable
C-HD50M-CM50M	Six foot Champ50 male to HD50 male cable
IP-TERM	50 screw terminal block with ribbon cable connector
IP-TERM-HD50	50 screw terminal block with HD50 female connector

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