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User Manual

VIPC310

3U VMEbus
IndustryPack[®] Carrier

VIPC310

3U VMEbus
IndustryPack®
Carrier

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This product has been designed to operate with IndustryPack carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

VIPC310 is part of the IndustryPack family of modular I/O components. The VIPC310 provides mechanical support and electrical interface for two single high IndustryPacks, or one double high IndustryPack. The VIPC310 is GreenSpring's general purpose, low cost, 3U IP carrier. The Rev C version features reliable surface mount CMOS technology and an improved power system. The Rev C is fully compatible with its predecessors; all existing programmable logic has been retained, and the interrupt scheme is identical. Memory and I/O addressing shunts have been re-located, but function in the same manner. The new revision is offered in optional extended temperature range or optional twinax I/O connectors for use with IP-1553.

The VIPC310 conforms to the IndustryPack Logic Interface Specification. This guarantees compatibility with the wide range of IndustryPacks currently available and planned. As of this writing, the current IP Logic Specification is ANSI/VITA 4—1996

Each of the IndustryPacks interfaces with a 50-pin flat cable header accessible through the front panel of the VIPC310. The two IPs are identified as A and B. The interface connectors are mounted directly on the

IndustryPack carrier, providing a modular and reliable cabling system. Interface cables may be inserted or removed without removing the VIPC310 from the VME chassis. IPs may be snapped in or removed without interfering with the I/O cabling.

VIPC310 meets VMEbus Specification C.1 (also known as IEEE P1014/D1.2 and IEC 821 bus) for 3U, or "single high," form factor. VMEbus I/O, standard memory, and interrupt functions are all supported on the VIPC310.

IndustryPack I/O is mapped into the VMEbus A16/D16 space "short I/O". Both user and supervisor access are supported, as are read-modify-write ("test and set") operations. The size of I/O on each IP is fixed by the IP Specification at 64, 16-bit, words. In addition each IP has an identification PROM which occupies 64 words. Thus the two IPs, A and B, occupy 512 bytes in the VMEbus system's 64 kilobytes of short I/O space.

VIPC310 provides VMEbus A24/D16 "standard memory space" access for IPs with memory. This carrier is configurable from 64 kilobytes to 2 megabytes of memory per IP, for a maximum of 4 megabytes.

Interrupts are fully supported. Each IP may generate up to two separate interrupt requests. The VIPC310 supports these as VMEbus interrupt levels 1, 2, 4, & 5. Each IP that requests interrupt service must provide its own 8-bit vector. This vector is provided to the VMEbus during bus interrupt acknowledge cycles.

Access acknowledge and power check LEDs are provided on the front panel for quick visual verification. IP Logic Interface cycles trigger LED flashes that indicate IP slot selection and normal cycle completion. Two access acknowledge LEDs are provided, one for each IP slot. A power check circuit detects blown fuses and line faults on either IP slot. When the power check LED is lit, VIPC310 is ready and both IP slots are energized.

The VIPC310 now provides fuse protection, RF filtering, and de-coupling capacitance on all IP power lines. Power filtering improves performance of precision analog IPs. VMEbus power-up, power-down, and bus reset functions are fully supported.

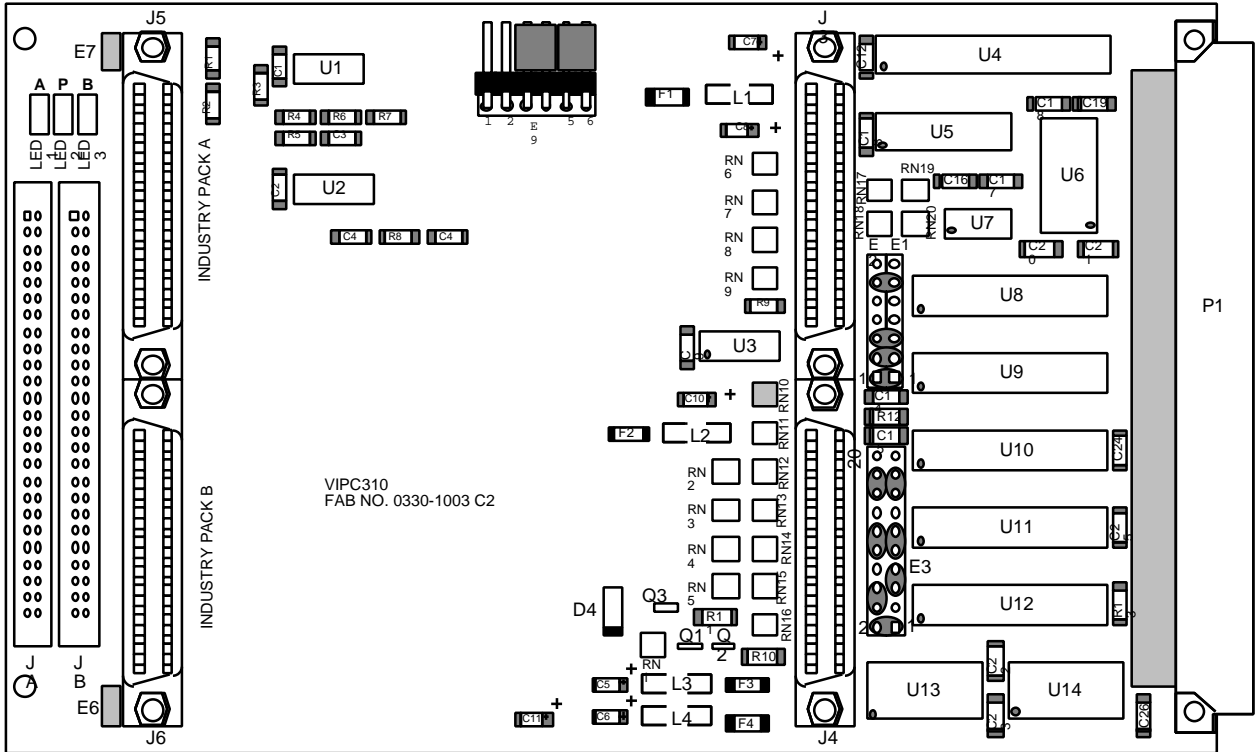


Figure 1 VIP310 Rev. C Assembly Diagram

Installation of IndustryPacks

IndustryPacks are installed on the VIPC310 carrier board by simply snapping them in. Press the IP and the carrier board together with your fingers until the two pairs of mating connectors are flush. The connectors are keyed, so the IP can only be installed correctly.

There are two locations for IPs. These are identified as A and B. The white lettering on the VIPC310 shows the location of each slot.

All IPs mate with 50-pin flat cable receptacle connectors for their I/O. The front panel labeling indicates which connector is associated with which IP. Pin 1 for each cable is identified by the arrow mark on the connector or a square solder pad.

Many connector manufacturers are able to provide suitable mass terminated receptacles. The following are recommended:

| | |
|-----------------|------------------|
| AMP | 1-499506-2 |
| Robinson Nugent | IDS-C50NPK-SR-TG |

After an IP has been installed, four stainless steel screws may be used to secure the IP to the carrier board. This is normally necessary only in high vibration or shock environments. Insert the screw through the IP and the two connectors. Attach the nut on the solder side of the VIPC310. Tighten using small tools, taking care not to damage either the IP or the support board. The screws used are standard (metric) M2 x 18 stainless slotted flat head. These screws and nuts come with each IP.

Cables, Screw kits and Engineering Kits are available from GreenSpring Computers.

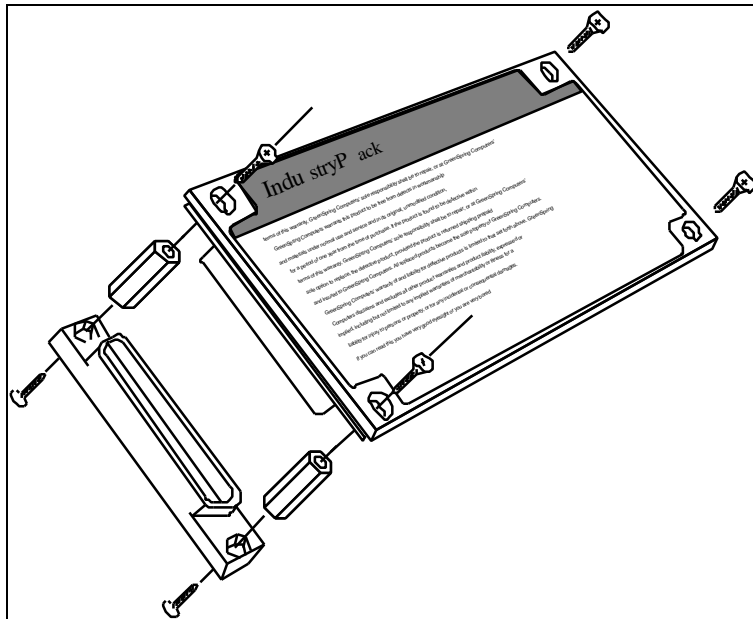


Figure 2 IndustryPack Installation

IndustryPack installation instructions

Install the four hex standoffs onto the IndustryPack Connectors. Fasten the standoffs to the IndustryPacks with four M2 x 5mm flat head machine screws. Install the IndustryPack onto the carrier board. Fasten the IndustryPack to the carrier with four M2 x 5mm pan head machine screws.

Please use a thread locking compound on all screws.

IndustryPack installation for non-compliant carriers

Some carrier boards use non-compliant 50 pin connectors. These connectors mate with IndustryPacks but cannot use the standard mounting hardware. A hardware kit for non-compliant carriers is available. The order number is EK-NCC. This must be ordered separately. Contact your local GreenSpring Representative or the factory for price and delivery.

Install the IndustryPack onto the carrier board. Fasten the IndustryPack to the carrier with four M2 x 16mm flat head machine screws and four M2 hex nuts. Use caution when tightening the screws. Too much force may damage the IndustryPack.

I/O Addressing

IP Spaces

I/O and ID addressing on the VIPC310 is determined by two elements. The first is the base address of the carrier. Second is the offset of the IP and the desired access subspace.

The 512 bytes the VIPC310 occupies in the A16 VMEbus short I/O space is divided into four subspaces. Each IndustryPack has an I/O space of 128 bytes, or 0x80 bytes in hexadecimal. Additionally, each IndustryPack has an ID PROM space occupying the adjacent 128 bytes. The VIPC310 provides two IndustryPacks slots, A and B. The I/O Space of slot B starts at an offset of 256 bytes from the carrier base address. The figure below shows the subspace allocations.

| Address | VIPC310 Subspace |
|-----------------------|------------------|
| Carrier Base + 0x0000 | IP A, I/O Space |
| Carrier Base + 0x0080 | IP A, ID Space |
| Carrier Base + 0x0100 | IP B, I/O Space |
| Carrier Base + 0x0180 | IP B, ID Space |

Figure 2 VIPC310 I/O & ID Subspaces

I/O Spaces and Configuration

The VIPC310 occupies 512 continuous bytes in the VMEbus short I/O space. This consists of 64, 16-bit, words for each IP's I/O and ID space. The carrier base address is set with shunt groups E1 and E2. The relationship of shunts to VMEbus A16 address lines is shown in Figure 3.

Select signals are generated by comparing VMEbus address lines with the shunt group values. A shunt installed between E1 and E2 selects a given address line as zero. A shunt removed selects the address line as a one. Thus, a carrier base address of 0x0000 is selected when all seven shunts are installed, and carrier base address of 0xFE00 is selected when all seven shunts are removed. The VIPC310 may be located on any 512 byte, or 0x200 hex, boundary however; GreenSpring recommends the common practice of locating VME carriers on 4096 byte, or 0x1000, boundaries.

| Shunt Location | Add. Line | Default | Value |
|----------------|-----------|---------|-------|
| E1-7 to E2-7 | A15 | IN | 0 |
| E1-6 to E2-6 | A14 | OUT | 1 |
| E1-5 to E2-5 | A13 | OUT | 1 |
| E1-4 to E2-4 | A12 | IN | 0 |
| E1-3 to E2-3 | A11 | IN | 0 |
| E1-2 to E2-2 | A10 | IN | 0 |
| E1-1 to E2-1 | A09 | IN | 0 |

**Figure 3 E1 & E2, I/O Base Address Shunts
Default Base Address = 0x6000**

VIPC310s are shipped with the default I/O base address set to 0x6000. For reference, the default base address shunt setting is shown below. For new system development and debug, we recommend starting with the 0x6000 default address to test carriers and IPs before re-configuration to other locations.

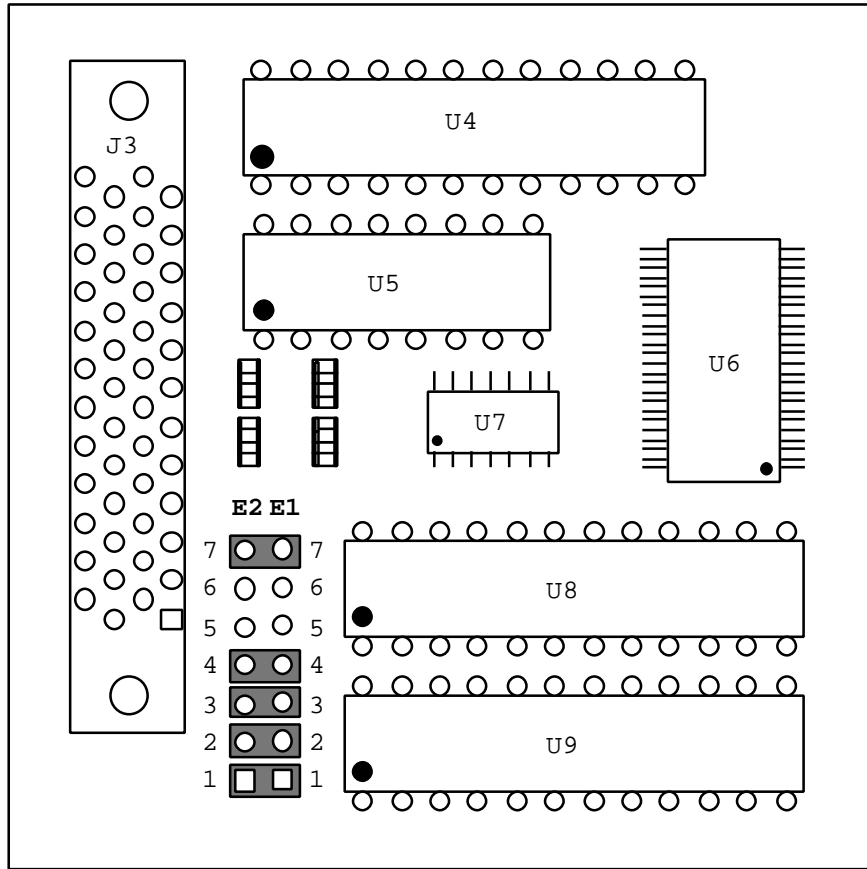


Figure 4 Default I/O Base Address Shunt Settings
I/O Base Address = 0x6000

To improve visual orientation all shunt groups and through hole components have square solder pads on pin number one.

The I/O base address shunts are also used to select the memory base address, if memory is enabled. As an example, if the I/O base address is 0x6000 (in A16 space), then the memory base address is 0x600000 (in the A24 space). See the Memory Addressing section for more information. To disable memory entirely, remove the shunt between E3.1 and E3.2.

ID Spaces

All IPs must have an ID PROM. This ID PROM is at least 32 bytes. It may be larger. It provides certain fixed information about the IP, which is defined in the IndustryPack Specification. This information includes the IP's manufacturer, model code, and manufacturing revision level. It may also include driver identification codes and calibration information.

ID PROMs are typically used by software for auto configuration, auto calibration, and revision maintenance. Additional configuration management functions are possible. The ID PROM is not required to be accessed nor its information used by the host software. However, since the IP PROM may contain critical calibration or configuration information, software usage is highly encouraged.

The figure below shows the required information in each ID PROM. See the IndustryPack Specification and the User Manual for each IP for more information.

| Address | Description | Contents |
|----------|---|-----------------|
| 0x3F | | |
| 0x2*nn+1 | User Space | |
| 0x2*nn-1 | | |
| 0x19 | IP Module Specific Space | |
| 0x17 | CRC | |
| 0x15 | Number of bytes used | = nn |
| 0x13 | Driver ID, high byte | |
| 0x11 | Driver ID, low byte | |
| 0x0F | Reserved | 0x00 |
| 0x0D | Revision | |
| 0x0B | Model Number | |
| 0x09 | Manufacturer ID | |
| 0x07 | ASCII "C" for 8Mhz or ASCII "H" for 32 Mhz | 0x43 or 0x48 |
| 0x05 | ASCII "A" | 0x41 |
| 0x03 | ASCII "P" | 0x50 |
| 0x01 | ASCII "I" | 0x49 |

Figure 5 Required ID PROM Information

Other Addressing Issues

Many IPs use only the low order, or odd, byte. For these IndustryPacks the bytes are accessed at location offsets of 0x1, 0x3, etc. This odd byte I/O convention is a Motorola 68000 micro-processor family convention and VMEbus standard. Furthermore, Motorola processors and VMEbus use so called "Big Endian" byte ordering, that is; in a 16 bit word, the bits are ranked in descending order from left to right (i.e. D₁₅...D₈ D₇...D₀). On "Little Endian" processors, like Intel products, the byte order is reversed; the low order byte is on the left (i.e. D₇...D₀ D₁₅...D₈). In systems using Little Endian CPUs this difference can cause considerable confusion

IPs are not required to decode all of their allotted I/O space. Normally accessing un-decoded space, or empty IP slots, will cause a VMEbus BERR generated by the offending CPU's bus time out circuitry. If a CPU's time out is disabled, BERR will not occur, and the bus will "hang."

Memory Addressing

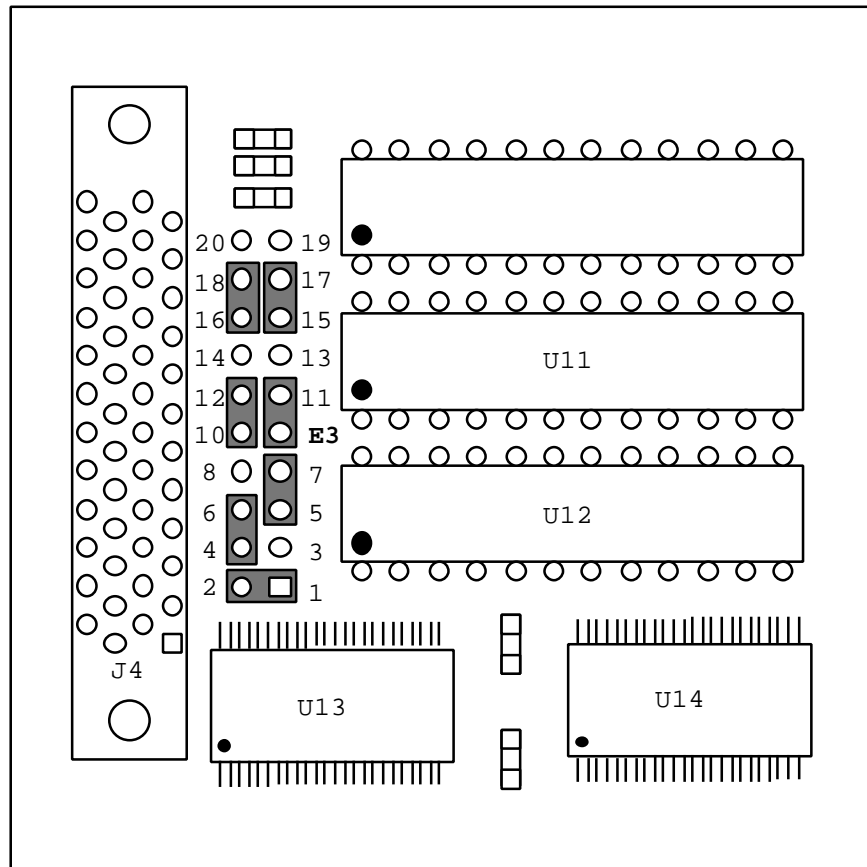
IndustryPacks may contain memory as well as I/O. VIPC310 supports up to 2 megabytes per IP, or 4 megabytes per carrier. This should be adequate for most A24/D16 applications. Systems with larger memory requirements should consider an extended memory carrier. Memory addressing on the VIPC310 consists of three parts: The first is enabling memory. Second is calculating and setting the IP memory size and offset. The last is setting the memory base address.

Enabling Memory

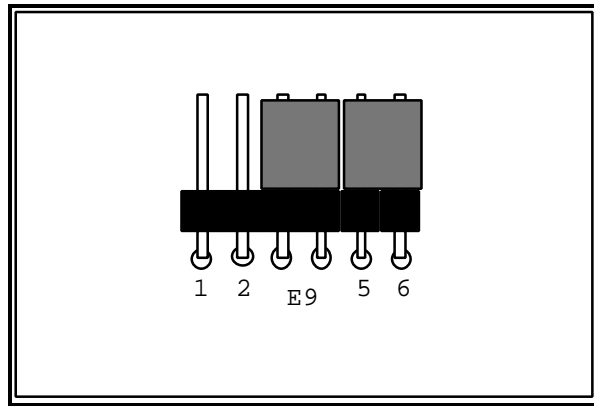
To enable A24/D16 memory access on the VIPC310 install a shunt from E3.1 to E3.2. To disable memory access, remove the shunt between E3.1 and E3.2.

Setting Memory Size and Offset

Shunt group E3 enables memory and sets the size. Shunt E9 determines the memory offset between IPs. VIPC310 is configured for two 128 kilobyte IPs at the factory. Below shows the default settings for the E3 group. E3.1 and E3.2 enable memory, the rest of the E3 group is used to select the memory size. Select signals are generated by comparing VME address values to the base address value. The E3 shunts route comparator inputs to VME address lines or short pairs to identical states. The E9 group determines the offset between IPs. To determine shunt settings, use the charts below Separate charts are provided for one or two memory IP applications.



**Figure 6 Default Memory Size Shunt Settings
256 kilobytes**



**Figure 7 Default Memory Offset Shunt Settings
128 Kilobytes per IP**

| Total VIPC310 Memory Size | IP Size | IP Slot | IP Location Base + | E 9 | | | | | | E 3 | |
|------------------------------|------------|------------|-----------------------|-----|-----|---|---|---|---|-----|----|
| 128 kilobytes | 64 k | A | 0x000000 | 1 | 2 | 3 | 4 | 5 | 6 | 20 | 19 |
| | 64 k | B | 0x010000 | | | | | | | 18 | 17 |
| | | | | | | | | | | 16 | 15 |
| | | | | | | | | | | 14 | 13 |
| | | | | | | | | | | 12 | 11 |
| | | | | | | | | | | 10 | 9 |
| | | | | | | | | | | 8 | 7 |
| | | | | | | | | | | 6 | 5 |
| | | | | | | | | | | 4 | 3 |
| | | | | | | | | | | 2 | 1 |
| Legend: | | | | | | | | | | | |
| SHADED | | | | = | IN | | | | | | |
| NO SHADING | | | | = | OUT | | | | | | |

| Total VIPC310 Memory Size | IP Size | IP Slot | IP Location Base + | E 9 | | | | | | E 3 | |
|------------------------------|------------|------------|-----------------------|-----|---|---|---|---|---|-----|----|
| 256 kilobytes | 128 k | A | 0x000000 | 1 | 2 | 3 | 4 | 5 | 6 | 20 | 19 |
| | 128 k | B | 0x020000 | | | | | | | 18 | 17 |
| | | | | | | | | | | 16 | 15 |
| | | | | | | | | | | 14 | 13 |
| | | | | | | | | | | 12 | 11 |
| | | | | | | | | | | 10 | 9 |
| | | | | | | | | | | 8 | 7 |
| | | | | | | | | | | 6 | 5 |
| | | | | | | | | | | 4 | 3 |
| | | | | | | | | | | 2 | 1 |
| DEFAULT SETTING | | | | | | | | | | | |

| Total VIPC310 Memory Size | IP Size | IP Slot | IP Location Base + | E 9 | | | | | | E 3 | |
|------------------------------|------------|------------|-----------------------|-----|---|---|---|---|---|-----|----|
| 512 kilobytes | 256 k | A | 0x000000 | 1 | 2 | 3 | 4 | 5 | 6 | 20 | 19 |
| | 256 k | B | 0x040000 | | | | | | | 18 | 17 |
| | | | | | | | | | | 16 | 15 |
| | | | | | | | | | | 14 | 13 |
| | | | | | | | | | | 12 | 11 |
| | | | | | | | | | | 10 | 9 |
| | | | | | | | | | | 8 | 7 |
| | | | | | | | | | | 6 | 5 |
| | | | | | | | | | | 4 | 3 |
| | | | | | | | | | | 2 | 1 |

| | | | | | |
|--------------------------------------|--------------------|--------------------|-------------------------------|-------------|---|
| Total VIPC310 Memory Size | IP Size | IP Slot | IP Location Base + | E 9 | E 3 |
| 1 megabyte | 512 k | A | 0x000000 | 1 2 3 4 5 6 | 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 |
| | 512 k | B | 0x080000 | | |
| Total VIPC310 Memory Size | IP Size | IP Slot | IP Location Base + | E 9 | E 3 |
| 2 megabytes | 1 M | A | 0x000000 | 1 2 3 4 5 6 | 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 |
| | 1 M | B | 0x100000 | | |
| Total VIPC310 Memory Size | IP Size | IP Slot | IP Location Base + | E 9 | E 3 |
| 4 megabytes | 2 M | A | 0x000000 | 1 2 3 4 5 6 | 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 |
| | 2 M | B | 0x200000 | | |

Figure 8 Memory Size Configurations for two memory IPs

| | | | | | | | | | | | | | | | | | | | | | | | | |
|---|--|--|----|----|----|----|----|----|--|--|----|----|----|---|---|---|--|--|---|---|---|---|---|---|
| <p>Total VIPC310</p> <p>Memory Size</p> <p>128 kilobytes</p> <p>128 Kbytes in Slot A if E1.1 to E2.1 is IN</p> <p>128 Kbytes in Slot B if E1.1 to E2.1 is OUT</p> | <p>E 9</p> <p>1 2 3 4 5 6</p> | <p>E 3</p> <p>20 19</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>18</td><td>17</td></tr> <tr><td>16</td><td>15</td></tr> <tr><td>14</td><td>13</td></tr> <tr><td> </td><td> </td></tr> <tr><td>12</td><td>11</td></tr> <tr><td>10</td><td>9</td></tr> <tr><td>8</td><td>7</td></tr> <tr><td> </td><td> </td></tr> <tr><td>6</td><td>5</td></tr> <tr><td>4</td><td>3</td></tr> <tr><td>2</td><td>1</td></tr> </table> | 18 | 17 | 16 | 15 | 14 | 13 | | | 12 | 11 | 10 | 9 | 8 | 7 | | | 6 | 5 | 4 | 3 | 2 | 1 |
| 18 | 17 | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | 15 | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | 13 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | 11 | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 9 | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | 7 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 5 | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | |
| <p>Total VIPC310</p> <p>Memory Size</p> <p>256 kilobytes</p> <p>256 Kbytes in Slot A if E1.2 to E2.2 is IN</p> <p>256 Kbytes in Slot B if E1.2 to E2.2 is OUT</p> | <p>E 9</p> <p>1 2 3 4 5 6</p> | <p>E 3</p> <p>20 19</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>18</td><td>17</td></tr> <tr><td>16</td><td>15</td></tr> <tr><td>14</td><td>13</td></tr> <tr><td> </td><td> </td></tr> <tr><td>12</td><td>11</td></tr> <tr><td>10</td><td>9</td></tr> <tr><td>8</td><td>7</td></tr> <tr><td> </td><td> </td></tr> <tr><td>6</td><td>5</td></tr> <tr><td>4</td><td>3</td></tr> <tr><td>2</td><td>1</td></tr> </table> | 18 | 17 | 16 | 15 | 14 | 13 | | | 12 | 11 | 10 | 9 | 8 | 7 | | | 6 | 5 | 4 | 3 | 2 | 1 |
| 18 | 17 | | | | | | | | | | | | | | | | | | | | | | | |
| 16 | 15 | | | | | | | | | | | | | | | | | | | | | | | |
| 14 | 13 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | |
| 12 | 11 | | | | | | | | | | | | | | | | | | | | | | | |
| 10 | 9 | | | | | | | | | | | | | | | | | | | | | | | |
| 8 | 7 | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 5 | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | |
| <p>Total VIPC310</p> <p>Memory Size</p> <p>512 kilobytes</p> <p>512 Kbytes in Slot A if E1.3 to E2.3 is IN</p> <p>512 Kbytes in Slot B if E1.3 to E2.3 is OUT</p> | <p>E 9</p> <p>1 2 3 4 5 6</p> | <p>E 3</p> <p>20 19</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr><td>18</td><td>17</td></tr> <tr><td>16</td><td>15</td></tr> <tr><td>14</td><td>13</td></tr> <tr><td> </td><td> </td></tr> <tr><td>12</td><td>11</td></tr> <tr><td>10</td><td>9</td></tr> <tr><td>8</td><td>7</td></tr> <tr><td> </td><td> </td></tr> <tr><td>6</td><td>5</td></tr> <tr><td>4</td><td>3</td></tr> <tr><td>2</td><td>1</td></tr> </table> | 18 | 17 | 16 | 15 | 14 | 13 | | | 12 | 11 | 10 | 9 | 8 | 7 | | | 6 | 5 | 4 | 3 | 2 | 1 |
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| | | | | | | | | | | | | | | | | | | | | | | | | |
| 6 | 5 | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | 3 | | | | | | | | | | | | | | | | | | | | | | | |
| 2 | 1 | | | | | | | | | | | | | | | | | | | | | | | |

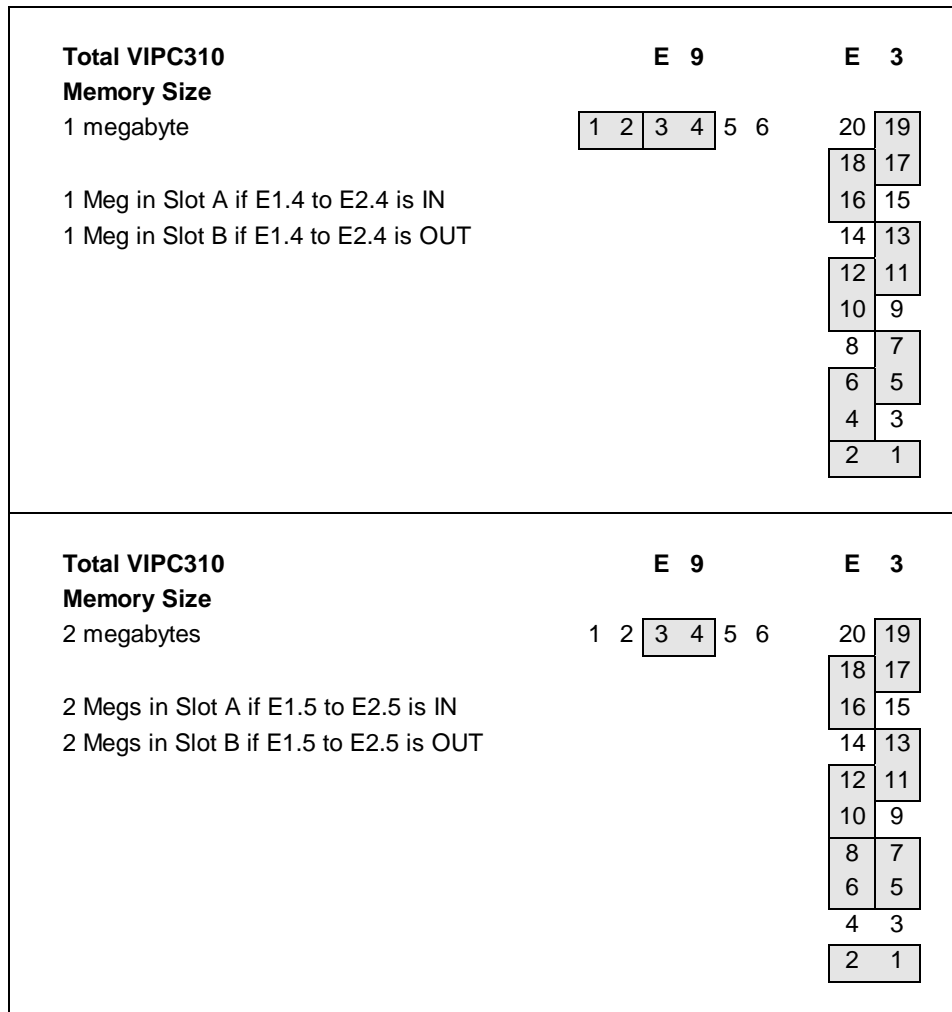


Figure 9 Memory Size Configurations for one memory IP

Setting Memory Base Address

The base address is set with the same seven shunts used to set the I/O base address. The memory and I/O base addresses "track" each other. The base address for memory is 256 times the base address of I/O. In other words, the E1 to E2 shunt group value is shared for both memory and I/O selection. In hexadecimal notation this conversion is done by shifting left one byte, or two zeros. For example: the VIPC310 default I/O base address is 0x6000 in the A16 space therefore the default memory base address in A24 space is 0x600000. For reference the default base address diagram is shown, again, below.

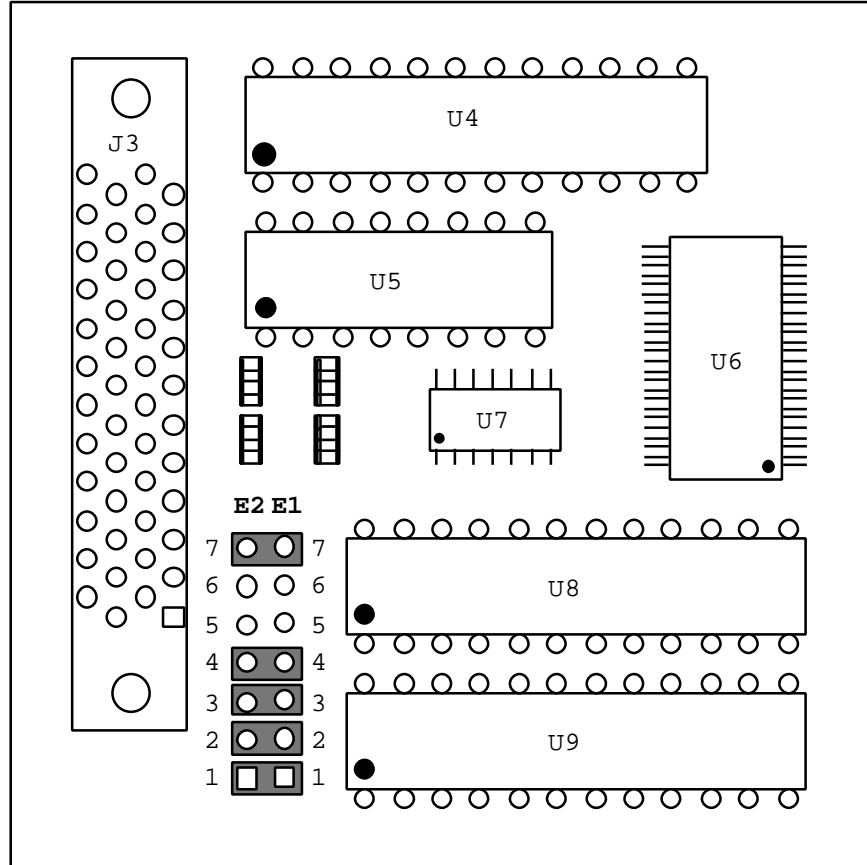


Figure 10 Default I/O Base Address Shunt Settings
Memory Base Address = 0x600000

In the E1 to E2 group, a shunt installed selects a given address line as zero. A shunt removed selects the address line as a one. Thus, for memory, a base address of 0x000000 is created when all seven shunts are installed. A base address of 0xFE0000 is created when all seven shunts are removed. The correspondence between shunt locations and VME A24 address lines is shown below.

| Shunt Location | Address Line | Default | Value |
|----------------|--------------|---------|-------|
| E1-7 to E2-7 | A23 | IN | 0 |
| E1-6 to E2-6 | A22 | OUT | 1 |
| E1-5 to E2-5 | A21 | OUT | 1 |
| E1-4 to E2-4 | A20 | IN | 0 |
| E1-3 to E2-3 | A19 | IN | 0 |
| E1-2 to E2-2 | A18 | IN | 0 |
| E1-1 to E2-1 | A17 | IN | 0 |

**Figure 11 Memory Base Address Shunts
Default = 0x600000**

On VIP310 memory cycles the higher order VMEbus address lines are routed directly to the IP address lines. This simplifies matters by eliminating complicated address re-mapping and decoding wait states. The memory sizing scheme uses the base address shunt values as well. **When using memory, these two factors require the carrier A24 base address be on a boundary equal to the sum of all memory space available on the carrier.**

For example: Using a VIP310 with two memory IPs, the largest of which being one megabyte, would require configuring the carrier for one megabyte per slot. The sum of available memory space on the carrier is two megabytes total, or one megabyte per slot. The carrier base, and IP slot A base, must be on a two megabyte boundary in the A24 space (i.e. 0x400000, 0x600000, 0x800000 etc.). The slot B base would be at carrier base + one megabyte (i.e 0x500000, 0x700000, 0x900000 etc.).

Shunt Functions, by Location

The following tables provide functional descriptions, indexed by shunt, of all shunts and default settings on the VIPC310.

| Shunt | to | Shunt | State | Factory | Function |
|-------|----|-------|-----------|---------|--|
| E1.1 | to | E2.1 | IN OUT | DEFAULT | Base address select; I/O A09 = 0, Memory A17 = 0 Base address select; I/O A09 = 1, Memory A17 = 1 |
| E1.2 | to | E2.2 | IN OUT | DEFAULT | Base address select; I/O A10 = 0, Memory A18 = 0 Base address select; I/O A10 = 1, Memory A18 = 1 |
| E1.3 | to | E2.3 | IN OUT | DEFAULT | Base address select; I/O A11 = 0, Memory A19 = 0 Base address select; I/O A11 = 1, Memory A19 = 1 |
| E1.4 | to | E2.4 | IN OUT | DEFAULT | Base address select; I/O A12 = 0, Memory A20 = 0 Base address select; I/O A12 = 1, Memory A20 = 1 |
| E1.5 | to | E2.5 | IN OUT | DEFAULT | Base address select; I/O A13 = 0, Memory A21 = 0 Base address select; I/O A13 = 1, Memory A21 = 1 |
| E1.6 | to | E2.6 | IN OUT | DEFAULT | Base address select; I/O A14 = 0, Memory A22 = 0 Base address select; I/O A14 = 1, Memory A22 = 1 |
| E1.7 | to | E2.7 | IN OUT | DEFAULT | Base address select; I/O A15 = 0, Memory A23 = 0 Base address select; I/O A15 = 1, Memory A23 = 1 |

Figure 12 E1 & E2, Base Address
Default = 0x6000

| Shunt | to | Shunt | to | Shunt | State | Factory | Memory Select if all E3 terms are TRUE. Function |
|-------|----|-------------------------|----|-------|-----------------|---------|---|
| E3.1 | to | E3.2 | | | IN OUT | DEFAULT | A24 memory enable A24 memory disable. All E3 Shunts disabled. |
| E3.3 | to | E3.5 E3.5 E3.5 | to | E3.7 | IN IN OUT | DEFAULT | TRUE if VME A17 = E1.1—E2.1 state Always TRUE Illegal if Memory Enabled |
| E3.9 | to | E3.11 E3.11 E3.11 | to | E3.13 | IN IN OUT | DEFAULT | TRUE if VME A18 = E1.2—E2.2 state Always TRUE Illegal if Memory Enabled |
| E3.15 | to | E3.17 E3.17 E3.17 | to | E3.19 | IN IN OUT | DEFAULT | TRUE if VME A19 = E1.3—E2.3 state Always TRUE Illegal if Memory Enabled |
| E3.4 | to | E3.6 E3.6 E3.6 | to | E3.8 | IN IN OUT | DEFAULT | TRUE if VME A20 = E1.4—E2.4 state Always TRUE Illegal if Memory Enabled |
| E3.10 | to | E3.12 E3.12 E3.12 | to | E3.14 | IN IN OUT | DEFAULT | TRUE if VME A21 = E1.5—E2.5 state Always TRUE Illegal if Memory Enabled |
| E3.16 | to | E3.18 E3.18 E3.18 | to | E3.20 | IN IN OUT | DEFAULT | TRUE if VME A22 = E1.6—E2.6 state Always TRUE Illegal if Memory Enabled |

Figure 13 E3, Memory Size
Default = 256 kilobytes

| Shunt | State | Factory | Function |
|-------|-------|---------|---------------------|
| E6 | IN | DEFAULT | Short Shield to GND |
| | OUT | | Floating shield |
| E7 | IN | DEFAULT | Short Shield to GND |
| | OUT | | Floating shield |

Figure 14 E6 & E7, Shields

| Shunt | to | Shunt | State | Factory | Function |
|-------|----|-------|-------|---------|----------|
| E9.1 | to | E9.2 | IN | DEFAULT | SIZ0 = 0 |
| | | | OUT | | SIZ0 = 1 |
| E9.3 | to | E9.4 | IN | DEFAULT | SIZ1 = 0 |
| | | | OUT | | SIZ1 = 1 |
| E9.5 | to | E9.6 | IN | DEFAULT | SIZ2 = 0 |
| | | | OUT | | SIZ2 = 1 |

**Figure 15 E9, IP Offset
Default = 128 kilobytes/IP**

| SIZ0 | SIZ1 | SIZ2 | SIZn Settings Decoded |
|------|------|------|------------------------|
| 0 | 0 | 0 | 64k per IP, 128k base |
| 0 | 0 | 1 | 1M per IP, 2M base |
| 0 | 1 | 0 | 256k per IP, 512k base |
| 0 | 1 | 1 | 4M per IP, 8M base |
| 1 | 0 | 0 | 128k per IP, 256k base |
| 1 | 0 | 1 | 2M per IP, 4M base |
| 1 | 1 | 0 | 512k per IP, 1M base |
| 1 | 1 | 1 | reserved |

Figure 16 E9, Size Settings Decoded

Interrupts

Each IndustryPack may generate up to two interrupts, called IRQ0* and IRQ1*. Since there are two packs, A and B, there are four possible interrupt sources. Each of these four sources is mapped to a fixed VMEbus interrupt level, as shown in the figure below.

| Interrupt Source | VMEbus Level |
|-------------------------|---------------------|
| Pack A, IRQ 0 | level 4 |
| Pack A, IRQ 1 | level 5 |
| Pack B, IRQ 0 | level 2 |
| Pack B, IRQ 1 | level 1 |

Figure 17 Interrupt Map

On the VMEbus, higher level numbers are higher priority. Some IndustryPacks allow the user to choose either IRQ0 or IRQ1 for the Pack's interrupt. Some IPs use both interrupts; some use none. IPs with only one interrupt level are required to use IRQ0.

All VMEbus interrupts are vectored. All IndustryPack interrupts are vectored. The IP provides the vector. Although two IPs mounted on the VIPC310 have only four distinct levels, there are up to 192 available vectors. Many IPs take advantage of vectors to send information. For example, serial communication errors use a different vector than buffer-full/buffer-empty vectors. Some IPs are able to generate a large number of distinct vectors. The VME systems integrator should maintain a vector map to assure that there is no overlap of vector usage of different IP or VME boards.

Per the IndustryPack Specification, a system reset will clear any pending interrupts from the IPs. Most IPs require a specific write operation to enable interrupts following a reset. It is good practice for the software to initialize all IPs in a system prior to enabling interrupts.

Front Panel Indicators

ACK LEDs

There are three green LED indicators on the VIP310 front panel. These are labeled IndustryPack Select A, PWR and B on the front panel or LED1, LED2 & LED3, respectively, on the fab. Each time IP A is successfully accessed the A indicator will turn on for about one third second. The B indicator functions in the same manner. Accesses more frequent than three times a second will show as a continuously illuminated indicator. The ACK LEDs respond to I/O, memory and interrupt accesses cycles.

The trigger for the pulse stretcher that drives the LEDs is the acknowledge signal from the IPs. Thus if the host software attempts to access an IP, but selects an unused location to which the IP does not respond, the indicator LED on the front panel will not blink. The indicators do not show that the IndustryPack carrier is being selected, but rather that the associated IP has completed an access. Similarly, the indicator LEDs do not show interrupts pending, but do show interrupt acknowledge cycles.

Power Check LED

The power check LED is marked with PWR. The power check circuit detects blown fuses or line faults on either IP slot. When the power check LED is lit, VIP310 is ready and both IP slots are energized.

User Options

Disabling Memory Access

All memory accesses to the VIPC310 may be disabled by removing the shunt on header E3.1 to E3.2. Removing this shunt does not disable I/O, ID or interrupt accesses. Removal is recommended if no IndustryPack with memory (or memory based I/O addressing) is installed. Removing the E3.1 to E3.2 shunt is the *only* way to disable the carrier from responding to VMEbus memory accesses.

(If no memory based IP is installed, but E3.1 to E3.2 is in place, then the carrier board will decode some group of memory locations, enabling its data bus drivers. Since no IP responds, no VMEbus DTACK* will be issued, nor will either of the front panel indicators illuminate. Should another VME board be decoding memory, however, at the same address, its data transfer cycle will be corrupted. This condition must be cleared with a system reset.)

Ground Plane under I/O connectors

The VIPC310 is constructed from a six layer printed circuit board. Two of the layers are primarily for power and ground distribution via copper planes. These copper planes do not extend to I/O connectors of the IndustryPacks nor the front panel I/O connectors. This is to reduce noise on I/O cabling. Digital power and ground planes tend to carry a moderate amount of high frequency noise. This noise may capacitively couple to sensitive analog wiring on these connectors.

The default shipping configuration is: no ground plane under the I/O connectors. This is the recommended configuration for most IndustryPacks.

Users may connect a floating ground plane under the I/O connectors to the local digital ground plane by placing shunts in locations E7 and E8. This configuration reduces the impedance of the I/O wiring, and generally reduces cross talk slightly on digital signals. This configuration is optional for high speed digital IndustryPacks, such as SCSI.

IP Logic Interface

The VITA-4 specification is the definitive reference for the IP bus logic interface. When this manual was written, the current revision was:

ANSI/VITA 4-1996
Specification Revision 1.0
IP Mezzanine Module Standard

This document, or its successor, is available from GreenSpring or VITA. VITA can be contacted at the following address.

VITA Standards Organization
10229 North Scottsdale Road, Suite B
Scottsdale Az. 85252
Voice: 602-951-8866
Fax: 602-951-0720

For quick reference, the table below shows the IP Logic pin assignments. Some of these signals may not be supported on this product.

| Pin # | Signal | Pin # | Signal | Pin # | Signal | Pin # | Signal |
|-------|--------|-------|--------|-------|----------|-------|----------|
| 1 | GND | 2 | CLK | 26 | GND | 27 | + 5V |
| 3 | Reset* | 4 | D0 | 28 | R/W* | 29 | IDSel* |
| 5 | D1 | 6 | D2 | 30 | DMAReq0* | 31 | MemSel* |
| 7 | D3 | 8 | D4 | 32 | DMAReq1* | 33 | IntSel* |
| 9 | D5 | 10 | D6 | 34 | DMAck* | 35 | IOSel* |
| 11 | D7 | 12 | D8 | 36 | Reserved | 37 | A1 |
| 13 | D9 | 14 | D10 | 38 | DMAEnd* | 39 | A2 |
| 15 | D11 | 16 | D12 | 40 | Error* | 41 | A3 |
| 17 | D13 | 18 | D14 | 42 | IntReq0* | 43 | A4 |
| 19 | D15 | 20 | BS0* | 44 | IntReq1* | 45 | A5 |
| 21 | BS1* | 22 | - 12V | 46 | Strobe* | 47 | A6 |
| 23 | +12V | 24 | + 5V | 48 | Ack* | 49 | Reserved |
| 25 | GND | | | 50 | GND | | |

Figure 18 IP Logic Interface Pin Assignment

Construction and Reliability

IndustryPacks, and carriers, were conceived and engineered for rugged industrial environments. The VIPC310 is constructed out of 0.062 inch thick FR4 material. The six copper layers consist of a ground plane, a power plane and four digital signal planes.

Through hole component mounting is used. IC sockets use gold plated screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron. Shunts may be replaced with wire-wrap® wires if desired.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, and correct, insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of these screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

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For Service Contact:

Customer Service Department
GreenSpring Computers
181 Constitution Drive
Menlo Park, CA 94025. U.S.A.
(415) 327-1200
(415) 327-3808 fax

Specifications

| | |
|---------------------------|--|
| VMEbus Conformance | Revision IEEE P1024/D1.2 |
| VMEbus Form Factor | 3U (single high) |
| IndustryPack® Conformance | ANSI/VITA 4—1996 |
| Number of IndustryPacks | Two single high, or One double high |
| IP Memory Mapping | A24/D16 VME AM Codes: 39, 3A, 3D & 3E |
| Memory Size | None, or 128 Kbytes to 4 MB in 6 increments. |
| IP I/O Mapping | A16/D16 VME AM Codes: 29 & 2D |
| I/O Size | 512 bytes |
| VMEbus Interrupts | IRQ1, IRQ2, IRQ4, IRQ5 |
| I/O Interconnect | Two 50-pin .100 inch flat cable connectors |
| Front Panel Indicators | IP access acknowledge LEDs for each slot One power check LED |
| Power Requirements | +5 V @ 460 mA typical +12V @ 0 mA -12V @ 0 mA Additional power is consumed by IndustryPacks |
| Environmental | 0°C to 70°C operating, Standard Product. -40°C to 85°C for —ET and —TX options. 5 to 95% relative humidity non-condensing |
| Size | 172 mm deep 128.5 mm high (incl. front panel) 13.6 mm thick |
| Weight | 0.14 Kg |



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