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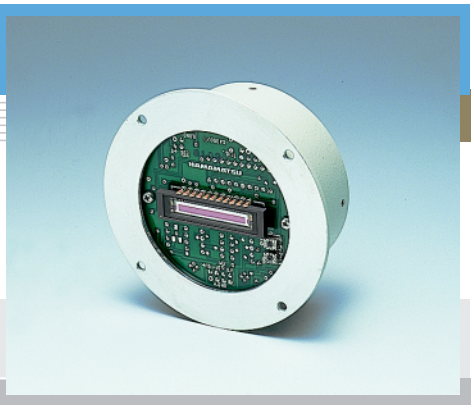
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NMOS multichannel detector head
C4350

Integrated low-noise driver/amplifier circuit for NMOS linear image sensor



C4350 is multichannel detector head incorporating low-noise driver/amplifier circuit developed for Hamamatsu NMOS linear image sensors. C4350 is designed especially for compactness, having an overall length as short as 40 mm or less.
In addition, C4350 is designed for ease of use. It is provided with circular flange for connection to monochrometer and adjustment mechanism for optical alignment for NMOS linear image sensor. The flange is interchangeable, thus facilitating connection to various models of monochrometer. The housing case also provides a shielding effect against external noise. As useful options, peripheral devices are available for driving C4350, and for the output signal processing.

Features

- Low noise
- Wide dynamic range
- Operatable with simple input signals
  (Only a master start pulse, a master clock pulse, +5 V and ±15 V are required.)
- Interchangeable flange
- Simple electrical and optical adjustments

Applications

- Multichannel spectrophotometry
- Optical spectrum analysis
- Time-resolved photometry

■ Compatible NMOS linear image sensors

Type No. of NMOS linear image sensor *1	Number of pixels	Active area per pixel (pixel pitch × height)
S3901-128Q, S8380-128Q	128	50 µm × 2.5 mm
S3901-256Q/F, S8380-256Q	256	
S3901-512Q/F, S8380-512Q	512	
S3902-128Q	128	50 µm × 0.5 mm
S3902-256Q/F	256	
S3902-512Q/F	512	
S3903-256Q	256	25 µm × 0.5 mm
S3903-512Q/F	512	
S3903-1024Q/F	1024	
S3904-256Q, S8381-256Q	256	25 µm × 2.5 mm
S3904-512Q/F, S8381-512Q	512	
S3904-1024Q/F, S8381-1024Q	1024	

*1: The suffix of type number indicates:
Q: quartz window, F: fiber optic window

SOLID STATE DIVISION

■ Absolute maximum ratings

Parameter	Symbol	Value	Unit
Supply voltage (digital)	Vd	7	V
Supply voltage (analog)	Va	±18	V
Operating temperature	Topr	0 to 50 *2	°C
Storage temperature	Tstg	-10 to 60 *2	°C

*2: No condensation

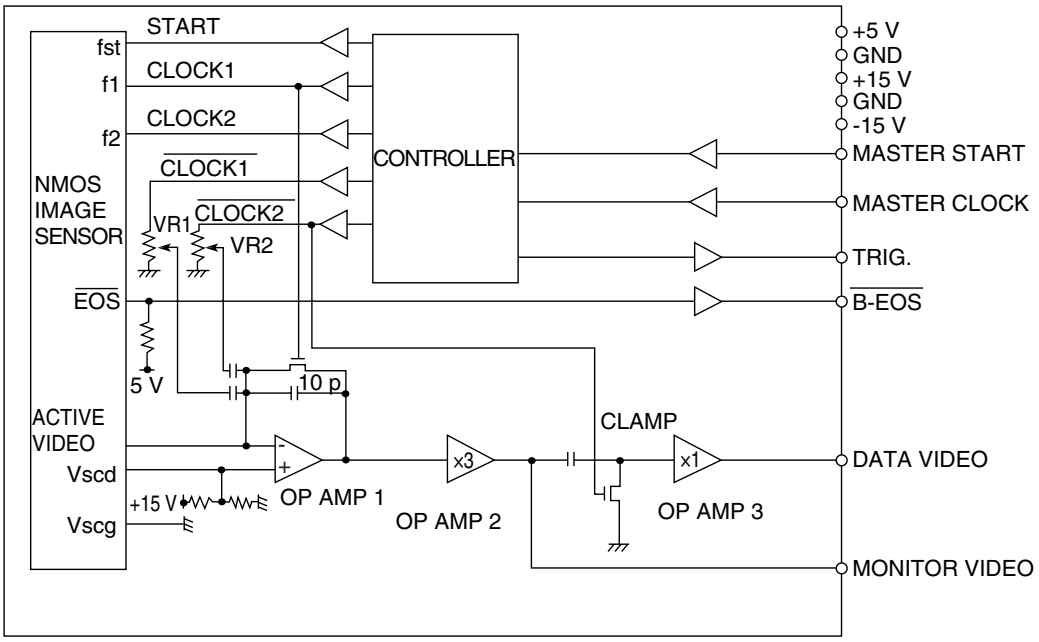
■ Electrical characteristics (Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Input	Supply voltage	Digital	Vd	4.85	5	5.5	V
		Analog	Va	±13.5	±15	±16.5	
	Master start pulse (ϕms)	Voltage	Vms (H)	2.0	5	-	V
			Vms (L)	0	-	0.8	
		Width	tpwϕms	1/fϕms	-	-	s
		Rise/fall Time	trϕms, tfϕms	-	-	500	ns
	Master clock pulse (ϕmc)	Voltage	Vmc (H)	2.0	5.0	-	V
			Vmc (L)	0	-	0.8	
		Frequency	fϕmc	-	-	375	kHz
		Width *3	tpwϕmc	30	-	-	ns
		Rise/fall time	trϕmc, tfϕmc	-	-	500	ns
Output *4	Start pulse (ϕst)	Voltage	Vst (H)	4.75	-	5.4	V
			Vst (L)	-	-	0.4	
		Rise/fall time	trϕst, tfϕst	-	-	100	ns
		Width	tpwϕst	-	2/fϕmc	-	s
	Clock pulse (ϕ1, ϕ2)	Voltage	V1, V2 (H)	4.75	-	5.4	V
			V1, V2 (L)	-	-	0.4	
		Rise/fall time	trϕ1, trϕ2	-	-	100	ns
			tfϕ1, tfϕ2				
	Clock pulse (ϕ1) width		tpwϕ1	-	1/fϕmc	-	s
	Clock pulse (ϕ2) width		tpwϕ2	-	3/fϕmc	-	s
	End of scan pulse	Voltage	Veos (H)	4.75	-	5.4	V
			Veos (L)	-	-	0.4	
		Rise/fall time	treos, tfeos	-	-	100	ns
		Width	tpweos	-	3/fϕmc	-	s
	Trigger pulse	Voltage	Vtrig (H)	4.75	5	5.4	V
			Vtrig (L)	-	-	0.4	
		Rise/fall time	trtrig, tftrig	-	-	100	ns

*3: The operation of 50 % Typ. duty ratio is recommended.

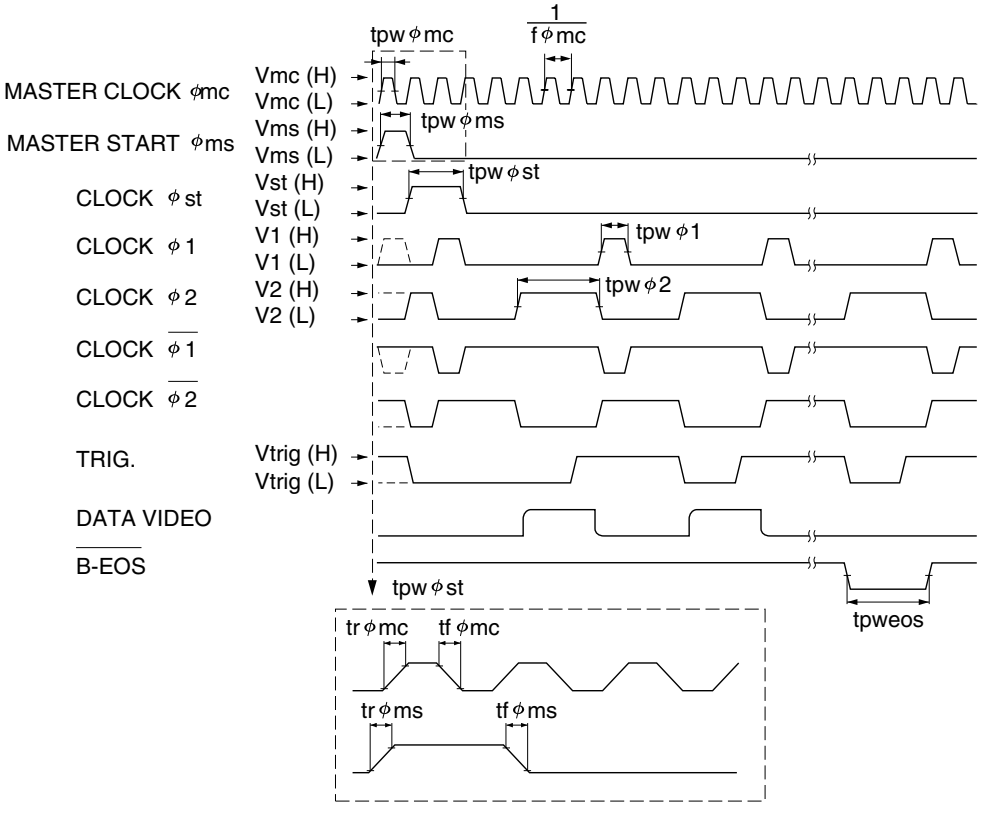
*4: The outputs of start-pulse and clock-pulse are to be obtained from a front part where an image sensor is installed. The outputs of end-of-scan and trigger-pulse are to be obtained from a back-side part where a connector for input/output signal is fixed.

■ Block diagram



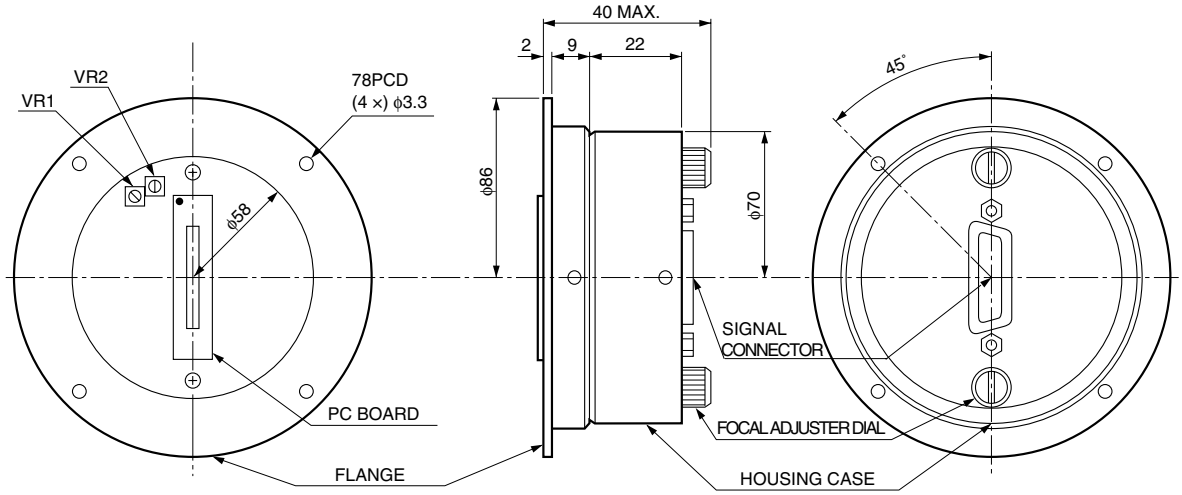
KACCC0009EA

■ Timing chart



KACCC0010EA

■ Dimensional outline (unit: mm)

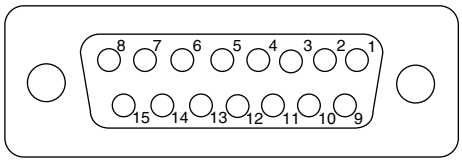


The focal position can be adjusted backward within the range from 0 to 4.5 mm (circuit stroke length) with a focal adjustment dial.

WEIGHT: approx. 0.16 kg

KACCA0008EA

■ Pin assignment of "Signal I/O" connector (15-pin D-sub)



KACCC0069EA

Pin No.	Terminal name	Description
1	Monitor video	Video output for electrical adjustment of the circuit
2	Data video	Video output
3	+15 V	Power supply for analog circuit (30 mA)
4	-15 V	Power supply for analog circuit (30 mA)
5	+5 V	Power supply for digital circuit (70 mA)
6	Master start	Scan start signal
7	Master clock	Scan signal (fmax=375 kHz)
8	$\overline{\text{B-EOS}}$	End-of-scan signal
9	A. GND	Ground for analog circuit
10	A. GND	Ground for analog circuit
11	Shield	Same potential as the housing, separate from the circuit ground
12	D. GND	Ground for digital circuit
13	D. GND	Ground for digital circuit
14	D. GND	Ground for digital circuit
15	TRIG.	Timing pulses for the A/D conversion

- Video data rate is 1/6 of master clock frequency (62.5 kHz Max.).
- The operation of circuit stroke length below 4.5 mm is recommended.
- The relation between data video output voltage and output charges from NMOS image sensor can be expressed by the following formula.

$$\text{Vout}(\text{V}) = 3 \times \frac{\text{Output charge}}{10 \times 10^{-12}[\text{F}]}$$

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Cat. No. KACC1004E03
Aug. 2001 DN

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