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HARRIS SEMICONDUCTOR

HI-574A, HI-674A, HI-774

Complete, 12-Bit A/D Converters with Microprocessor Interface

August 1997

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-Bit, 12-Bit or 16-Bit Microprocessor Bus Interface
- Bus Access Time 150ns
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- Fast Conversion Times
  - HI-574A (Max) 25µs
  - HI-674A (Max) 15µs
  - HI-774 (Max) 9µs
- Digital Error Correction (HI-774)
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_O Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by Start Convert Input (To Set the Conversion Length)
- Supply Voltage . . . . . ±12V to ±15V

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-X74(A) is a complete 12-bit, Analog-to-Digital Converter, including a +10V reference clock, three-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 lead package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

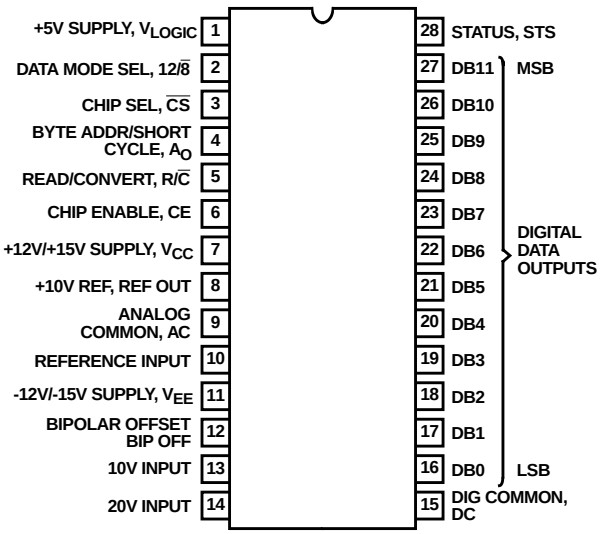
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital ICs. Also, the clock oscillator is current controlled for excellent stability over temperature.

The HI-X74(A) offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

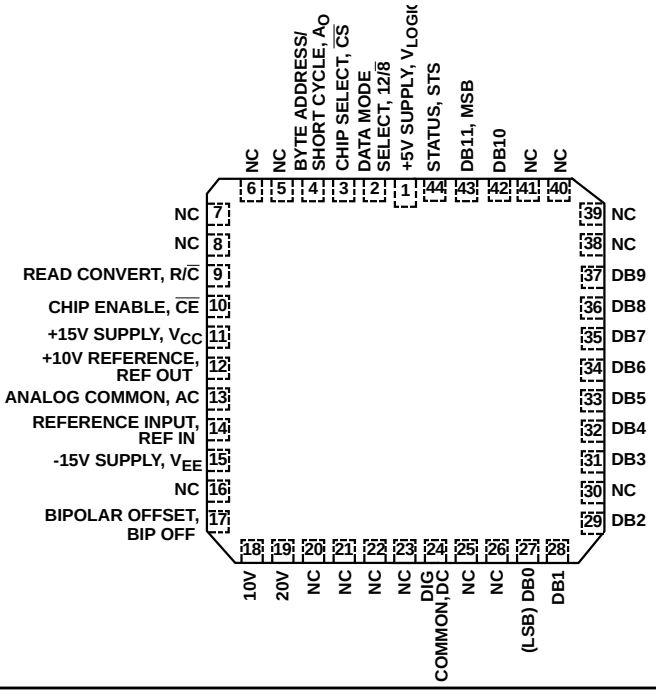
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW (HI-574A/674A) and 390mW (HI-774) at 12V. All models are available in sidebrazed DIP, PDIP, and CLCC. For additional HI-Rel screening including 160 hour burn-in, specify "-8" suffix. For MIL-STD-883 compliant parts, request HI-574A/883, HI-674A/883, and HI-774/883 data sheets.

Pinouts

(PDIP, SBDIP)
TOP VIEW



(CLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

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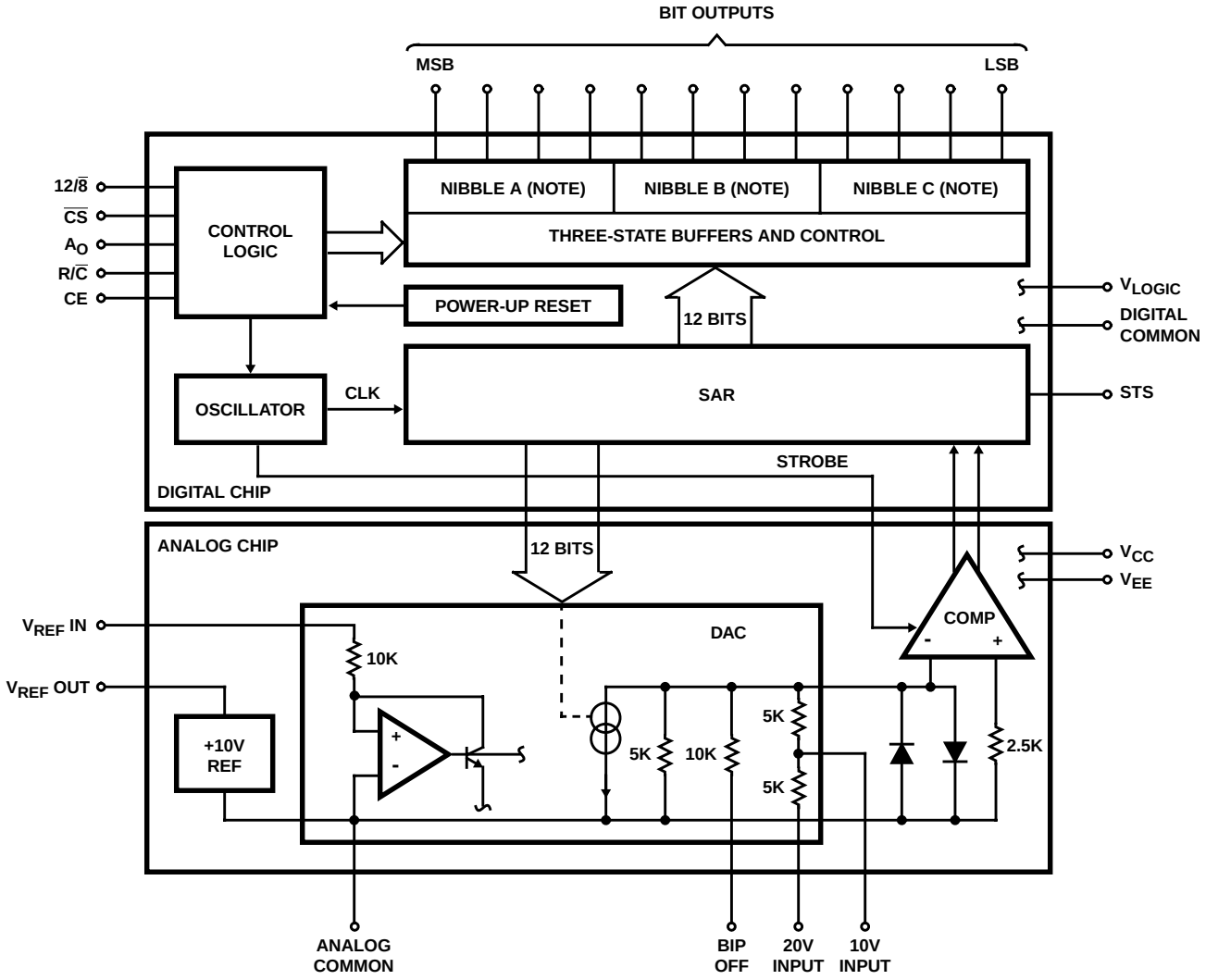
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Ordering Information

PART NUMBER	INL	TEMPERATURE RANGE (^{o}C)	PACKAGE	PKG. NO.
HI3-574AJN-5	±1.0 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-574AKN-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-574ALN-5	±0.5 LSB	0 to 70	28 Ld PDIP	E28.6
HI1-574AJD-5	±1.0 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-574AKD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-574ALD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-574ASD-2	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574ATD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574AUD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574ASD/883	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574ATD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-574AUD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI4-574ASE/883	±1.0 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-574ATE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-574AUE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI3-674AJN-5	±1.0 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-674AKN-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-674ALN-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI1-674AJD-5	±1.0 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-674AKD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-674ALD-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-674ASD-2	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674ATD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674AUD-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674ASD/883	±1.0 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674ATD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-674AUD/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI4-674ASE/883	±1.0 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-674ATE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-674AUE/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI3-774J-5	±1.0 LSB	0 to 75	28 Ld PDIP	E28.6
HI3-774K-5	±0.5 LSB	0 to 75	28 Ld PDIP	E28.6
HI1-774J-5	±1.0 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-774K-5	±0.5 LSB	0 to 75	28 Ld SBDIP	D28.6
HI1-774U-2	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI1-774T/883	±0.5 LSB	-55 to 125	28 Ld SBDIP	D28.6
HI4-774S/883	±1.0 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-774T/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A
HI4-774U/883	±0.5 LSB	-55 to 125	44 Ld CLCC	J44.A

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Functional Block Diagram



NOTE: “Nibble” is a 4-bit digital word.

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Absolute Maximum Ratings

Supply Voltage
- V_{CC} to Digital Common . . . . . 0V to +16.5V
- V_{EE} to Digital Common. . . . . 0V to -16.5V
- V_{LOGIC} to Digital Common. . . . . 0V to +7V
- Analog Common to Digital Common±1V

Control Inputs
- (CE, $\overline{CS}$, A_O, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common . . -0.5V to V_{LOGIC} +0.5V

Analog Inputs
- (REFIN, BIPOFF, 10VIN) to Analog Common. . . . . ±16.5V
- 20VIN to Analog Common . . . . . ±24V

REFOUT . . . . Indefinite Short To Common, Momentary Short To V_{CC}

Operating Conditions

Temperature Range
- HI3-574AxN-5, HI1-574AxD-5 . . . . . .0^oC to 75^oC
- HI3-674AxN-5, HI1-674AxD-5 . . . . . .0^oC to 75^oC
- HI3-774xN-5, HI1-774xD-5. . . . . .0^oC to 75^oC
- HI1-574AxD-2, HI1-674AxD-2, HI1-774xD-2 . . . . -55^oC to 125^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CLCC Package	65	14
SBDIP Package	60	18
HI3-574AxN-5, HI3-674AxN-5, HI3-774xN-5	65	N/A

Maximum Junction Temperature
- HI3-574AxN-5, HI3-674AxN-5, HI3-774xN-5. . . . . 150^oC
- HI1-574AxD-2, HI1-574AxD-5 . . . . . 175^oC
- HI1-674AxD-2, HI1-674AxD-5 . . . . . 175^oC
- HI1-774xD-2, HI1-774xD-5 . . . . . 175^oC

Maximum Storage Temperature Range
- HI3-574AxN-5, HI3-674AxN-5, HI3-774xN-5. . . . . -40^oC to 85^oC
- HI1-574AxD-2, HI1-574AxD-5 . . . . . -65^oC to 150^oC
- HI1-674AxD-2, HI1-674AxD-5 . . . . . -65^oC to 150^oC
- HI1-774xD-2, HI1-774xD-5 . . . . . -65^oC to 150^oC

Maximum Lead Temperature (Soldering, 10s) . . . . . 300^oC

Die Characteristics

Transistor Count
- HI-574A, HI-674A 1117
- HI-774 2117

DC and Transfer Accuracy Specifications

Typical at 25^oC with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETER		TEMPERATURE RANGE -5 (0^oC to 75^oC) J SUFFIX	K SUFFIX	L SUFFIX	UNITS
DYNAMIC CHARACTERISTICS					
Resolution (Max)		12	12	12	Bits
Linearity Error					
25^oC (Max)		±1	±1/2	±1/2	LSB
0^oC to 75^oC (Max)		±1	±1/2	±1/2	LSB
Max Resolution For Which No Missing Codes Is Guaranteed					
25^oC	HI-574A, HI-674A	12	12	12	Bits
	HI-774	11	12	12	Bits
T_{MIN} to T_{MAX}	HI-574A, HI-674A	11	12	12	Bits
	HI-774	11	12	12	Bits
Unipolar Offset (Max)					
Adjustable to Zero		±2	±1.5	±1	LSB
Bipolar Offset (Max)					
V_{IN} = 0V (Adjustable to Zero)		±4	±4	±3	LSB
V_{IN} = -10V		±0.15	±0.1	±0.1	% of FS
Full Scale Calibration Error					
25^oC (Max), With Fixed 50Ω Resistor From REF OUT To REF IN (Adjustable to Zero)		±0.25	±0.25	±0.15	% of FS
T_{MIN} to T_{MAX} (No Adjustment At 25^oC)		±0.475	±0.375	±0.20	% of FS
T_{MIN} to T_{MAX} (With Adjustment To Zero 25^oC)		±0.22	±0.12	±0.05	% of FS

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DC and Transfer Accuracy Specifications Typical at 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEMPERATURE RANGE -5 (0°C to 75°C) J SUFFIX	K SUFFIX	L SUFFIX	UNITS
Temperature Coefficients Guaranteed Max Change, T_{MIN} to T_{MAX} (Using Internal Reference)					
Unipolar Offset	HI-574A, HI-674A	±2	±1	±1	LSB
	HI-774	±2	±1	±1	LSB
Bipolar Offset	HI-574A, HI-674A	±2	±1	±1	LSB
	HI-774	±2	±2	±1	LSB
Full Scale Calibration	HI-574A, HI-674A	±9	±2	±2	LSB
	HI-774	±9	±5	±2	LSB
Power Supply Rejection Max Change In Full Scale Calibration					
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V		±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V		$\pm^1/_2$	$\pm^1/_2$	$\pm^1/_2$	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V		±2	±1	±1	LSB
ANALOG INPUTS					
Input Ranges					
Bipolar		-5 to +5			V
		-10 to +10			V
Unipolar		0 to +10			V
		0 to +20			V
Input Impedance					
10V Span		5K, ±25%			Ω
20V Span		10K, ±25%			Ω
POWER SUPPLIES					
Operating Voltage Range					
V_{LOGIC}		+4.5 to +5.5			V
V_{CC}		+11.4 to +16.5			V
V_{EE}		-11.4 to -16.5			V
Operating Current					
I_{LOGIC}		7 Typ, 15 Max			mA
I_{CC} +15V Supply		11 Typ, 15 Max			mA
I_{EE} -15V Supply		21 Typ, 28 Max			mA
Power Dissipation					
±15V, +15V		515 Typ, 720 Max			mW
±12V, +5V		385 Typ			mW
Internal Reference Voltage					
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max			V
Output Current, Available For External Loads (External Load Should Not Change During Conversion).		2.0 Max			mA

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DC and Transfer Accuracy Specifications Typical at 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETER		TEMPERATURE RANGE -2 (-55°C to 125°C) S SUFFIX	T SUFFIX	U SUFFIX	UNITS
DYNAMIC CHARACTERISTICS					
Resolution (Max)		12	12	12	Bits
Linearity Error					
25°C		±1	±1/2	±1/2	LSB
-55°C to 125°C (Max)		±1	±1	±1	LSB
Max Resolution For Which No Missing Codes Is Guaranteed					
25°C	HI-574A, HI-674A	12	12	12	Bits
	HI-774	11	12	12	Bits
T_{MIN} to T_{MAX}	HI-574A, HI-674A	11	12	12	Bits
	HI-774	11	12	12	Bits
Unipolar Offset (Max)					
Adjustable to Zero	HI-574A, HI-674A	±2	±1.5	±1	LSB
	HI-774	±2	±2	±1	LSB
Bipolar Offset (Max)					
V_{IN} = 0V (Adjustable to Zero)		±4	±4	±3	LSB
V_{IN} = -10V		±0.15	±0.1	±0.1	% of FS
Full Scale Calibration Error					
25°C (Max), With Fixed 50Ω Resistor From REF OUT To REF IN (Adjustable To Zero)		±0.25	±0.25	±0.15	% of FS
T_{MIN} to T_{MAX} (No Adjustment At 25°C)		±0.75	±0.50	±0.275	% of FS
T_{MIN} to T_{MAX} (With Adjustment To Zero At 25°C)		±0.50	±0.25	±0.125	% of FS
Temperature Coefficients Guaranteed Max Change, T_{MIN} to T_{MAX} (Using Internal Reference)					
Unipolar Offset		±2	±1	±1	LSB
Bipolar Offset		±2	±2	±1	LSB
Full Scale Calibration		±20	±10	±5	LSB
Power Supply Rejection Max Change In Full Scale Calibration					
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V		±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V		±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V		±2	±1	±1	LSB
ANALOG INPUTS					
Input Ranges					
Bipolar		-5 to +5			V
		-10 to +10			V
Unipolar		0 to +10			V
		0 to +20			V

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DC and Transfer Accuracy Specifications Typical at 25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEMPERATURE RANGE -2 (-55°C to 125°C) S SUFFIX	T SUFFIX	U SUFFIX	UNITS
Input Impedance				
10V Span	5K, ±25%			Ω
20V Span	10K, ±25%			Ω
POWER SUPPLIES				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			V
V_{CC}	+11.4 to +16.5			V
V_{EE}	-11.4 to -16.5			V
Operating Current				
I_{LOGIC}	7 Typ, 15 Max			mA
I_{CC} +15V Supply	11 Typ, 15 Max			mA
I_{EE} -15V Supply	21 Typ, 28 Max			mA
Power Dissipation				
±15V, +15V	515 Typ, 720 Max			mW
±12V, +5V	385 Typ			mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}	+10.00 ±0.05 Max			V
Output current, available for external loads (External load should not change during conversion).	2.0 Max			mA

Digital Specifications All Models, Over Full Temperature Range

PARAMETER	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 412/$\overline{8}$)			
Logic “1”	+2.4V	-	+5.5V
Logic “0”	-0.5V	-	+0.8V
Current	-	±0.1µA	±5µA
Capacitance	-	5pF	-
Logic Outputs (DB11-DB0, STS)			
Logic “0” (I_{SINK} - 1.6mA)	-	-	+0.4V
Logic “1” (I_{SOURCE} - 500µA)	+2.4V	-	-
Logic “1” (I_{SOURCE} - 10µA)	+4.5V	-	-
Leakage (High-Z State, DB11-DB0 Only)	-	±0.1µA	±5µA
Capacitance	-	5pF	-

Timing Specifications (HI-574A) 25°C, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
CONVERT MODE					
t_{DSC}	STS Delay from CE	-	-	200	ns

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Timing Specifications (HI-574A) 25°C, Note 2, Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_O to CE Setup		0	-	-	ns
t_{HAC}	A_O Valid During CE High		50	-	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX}	15	20	25	µs
		8-Bit Cycle T_{MIN} to T_{MAX}	10	13	17	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	-	-	ns
t_{SAR}	A_O to CE Setup		50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	-	-	ns
t_{HAR}	A_O Valid After CE Low		50	-	-	ns
t_{HS}	STS Delay After Data Valid		300	-	1200	ns

Timing Specifications (HI-674A) 25°C, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	-	200	ns
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_O to CE Setup		0	-	-	ns
t_{HAC}	A_O Valid During CE High		50	-	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX}	9	12	15	µs
		8-Bit Cycle T_{MIN} to T_{MAX}	6	8	10	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns

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Timing Specifications (HI-674A) 25°C, Note 2, Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{SSR}	$\overline{CS}$ to CE Setup	50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup	0	-	-	ns
t_{SAR}	A_O to CE Setup	50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low	0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low	0	-	-	ns
t_{HAR}	A_O Valid After CE Low	50	-	-	ns
t_{HS}	STS Delay After Data Valid	25	-	850	ns

Timing Specifications (HI-774) 25°C, Into a load with R_L = 3kΩ and C_L = 50pF, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	100	200	ns
t_{HEC}	CE Pulse Width		50	30	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	20	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	20	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	0	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	20	-	ns
t_{SAC}	A_O to CE Setup		0	0	-	ns
t_{HAC}	A_O Valid During CE High		50	30	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX} (-5)	-	8.0	9	µs
		8-Bit Cycle T_{MIN} to T_{MAX} (-5)	-	6.4	6.8	µs
		12-Bit Cycle T_{MIN} to T_{MAX} (-2)	-	9	11	µs
		8-Bit Cycle T_{MIN} to T_{MAX} (-2)	-	6.8	8.3	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	35	-	ns
t_{HL}	Output Float Delay		-	70	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	0	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	0	-	ns
t_{SAR}	A_O to CE Setup		50	25	-	ns
t_{HSR}	CS Valid After CE Low		0	0	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	0	-	ns
t_{HAR}	A_O Valid After CE Low		50	25	-	ns
t_{HS}	STS Delay After Data Valid		-	90	300	ns

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

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Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	V_{LOGIC}	Logic supply pin (+5V)
2	12/$\overline{8}$	Data Mode Select - Selects between 12-bit and 8-bit output modes.
3	$\overline{CS}$	Chip Select - Chip Select high disables the device.
4	A_0	Byte Address/Short Cycle - See Table 1 for operation.
5	R/$\overline{C}$	Read/Convert - See Table 1 for operation.
6	CE	Chip Enable - Chip Enable low disables the device.
7	V_{CC}	Positive Supply (+12V/+15V)
8	REF OUT	+10V Reference
9	AC	Analog Common
10	REF IN	Reference Input
11	V_{EE}	Negative Supply (-12V/-15V).
12	BIP OFF	Bipolar Offset
13	10V Input	10V Input - Used for 0V to 10V and -5V to +5V input ranges.
14	20V Input	20V Input - Used for 0V to 20V and -10V to +10V input ranges.
15	DC	Digital Common
16	DB0	Data Bit 0 (LSB)
17	DB1	Data Bit 1
18	DB2	Data Bit 2
19	DB3	Data Bit 3
20	DB4	Data Bit 4
21	DB5	Data Bit 5
22	DB6	Data Bit 6
23	DB7	Data Bit 7
24	DB8	Data Bit 8
25	DB9	Data Bit 9
26	DB10	Data Bit 10
27	DB11	Data Bit 11 (MSB)
28	STS	Status Bit - Status high implies a conversion is in progress.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from “zero” through “full scale”. The point used as “zero” occurs $^1/_2$ LSB (1.22mV for 10V span) before the first code transition (all zeros to only the LSB “on”). “Full scale” is defined as a level $1^1/_2$ LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-X74(A)K and L grades are guaranteed for maximum nonlinearity of $\pm^1/_2$ LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-X74(A)J is guaranteed to ±1 LSB max error. For this grade, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-X74(A)K and L grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-X74(A)J grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level $^1/_2$ LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value $^1/_2$ LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value $1^1/_2$ LSB below the nominal full scale (9.9963V for 10.000V full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10V reference.

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Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25^{o}C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection

The standard specifications for the HI-X74A assume use of +5.00V and ±15.00V or ±12.00V supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10V for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm^{1}/_{2}$ LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-justified Data

The data format used in the HI-X74(A) is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-X74(A)

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

Physical Mounting and Layout Considerations

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12-bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vector board, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-X74(A) (+15V, -15V and +5V) must be “quiet” and well regulated. Voltage spikes on these lines can affect the converter’s accuracy, causing several LSBs to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure “quiet” DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10µF tantalum type in parallel with a 0.1µF ceramic type is recommended.

Ground Connections

Pins 9 and 15 should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) +15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system’s “single point” ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-X74(A)’s Analog Common or Digital Common).

Analog Signal Source

HI-574A and HI-674A

The device chosen to drive the HI-X74A analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6µs and 950ns intervals for the HI-574A and HI-674A, respectively. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-X74A. To check whether the output properties of a signal source are suitable, monitor the HI-X74A’s input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in 1µs or less for the HI-574A and 500ns or less for the HI-674A. (The comparator decision is made about 1.5µs and 850ns after each code change from the SAR for the HI-574A and HI-674A, respectively.)

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

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HI-774

The device driving the HI-774 analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a “kick back” glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350ns intervals so an op amp with a low output impedance and fast settling is desirable. Ultimately the input must settle to within the window of Figure 1 at the bit decision points in order to achieve 12-bit accuracy.

The HI-774 differs from the most high-speed successive approximation type ADC’s in that it does not require a high performance buffer or sample and hold. With error correction the input can settle while the conversion is underway, but only during the first 4.8µs. The input must be within 10.76% of the final value when the MSB decision is made. This occurs approximately 650ns after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input “kick back” disturbances settle within the window of Figure 1 the device will remain accurate. The combined effect of settling and the “kick back” disturbances must remain in the Figure 1 window.

If the design is being optimized for speed, the input device should have closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of Figure 1.

Digital Error Correction

HI-774

The HI-774 features the smart successive approximation register (SSAR) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32 LSB window about the final value. The input can move during the first 4.8µs, after which it must remain stable within $\pm^1/_2$ LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within $\pm^1/_2$ LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 LSBs). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4 LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 LSBs. This results in a total correction range of +31 to -32 LSBs. When an 8-bit conversion is performed, the input must settle to within $\pm^1/_2$ LSB at 8-bit resolution (which equals ±8 LSBs at 12-bit resolution).

With the HI-774 a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.8µs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

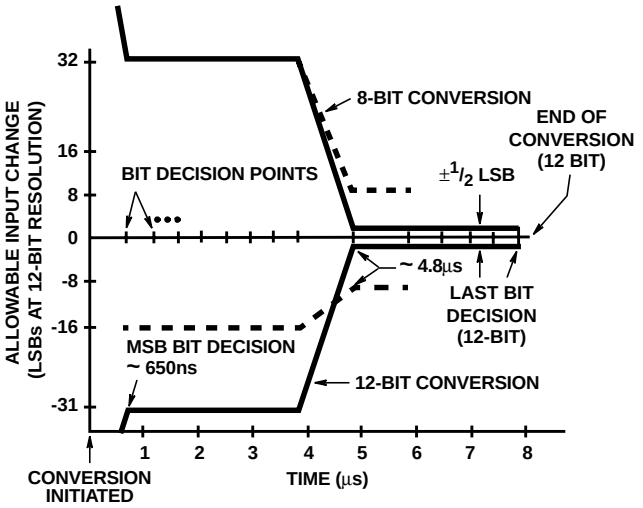
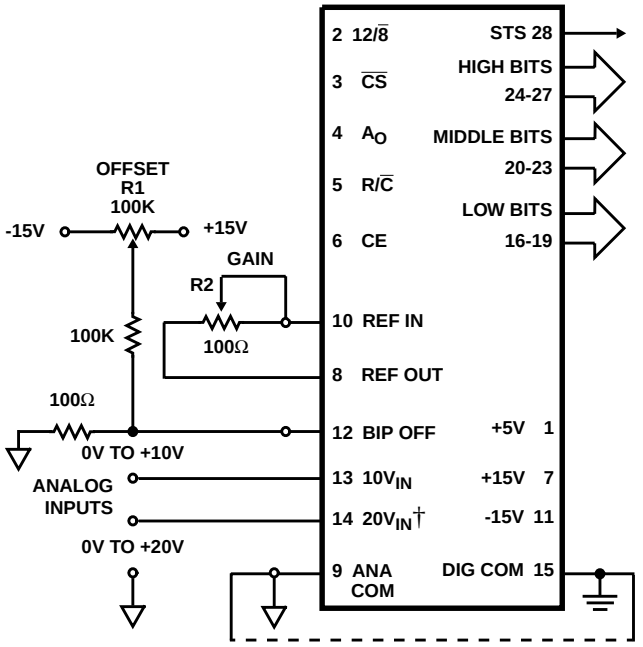


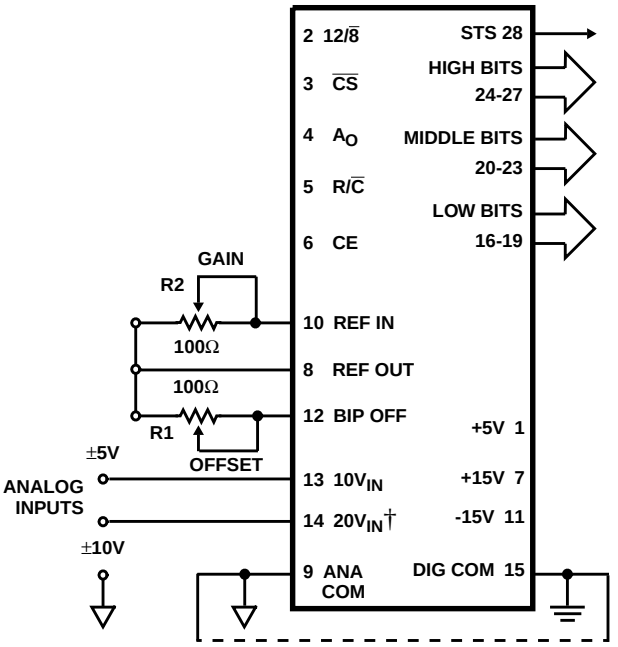
FIGURE 1. HI-774 ERROR CORRECTION WINDOW vs TIME



†When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 2. UNIPOLAR CONNECTIONS

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†When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 3. BIPOLAR CONNECTIONS

Range Connections and Calibration Procedures

The HI-X74(A) is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figure 2 and Figure 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-X74(A) offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration

Refer to Figure 2. The resistors shown (see Note) are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem - the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of $+^1/_2$ LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is $1^1/_2$ LSBs below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2 (see Note). If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage $^1/_2$ LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage $1^1/_2$ LSBs below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

NOTE: The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

Controlling the HI-X74(A)

The HI-X74(A) includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8-bit or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready-choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_O, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 7.

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"Stand-Alone Operation"

The simplest control interface calls for a singe control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_O are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 8 and 9. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing".

HI-574A STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	300	-	1200	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

HI-674A STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	25	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

HI-774 STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	20	-	-	ns
t_{HS}	STS Delay after Data Valid	-	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_O, which determines whether the conversion continues for 12 bits (A_O low) or stops with 8 bits (A_O high). If all 12 bits are read following an 8-bit conversion, the last three LSBs will read ZERO and DB3 will read ONE. A_O is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HI-X74(A) CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_O	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit Output
1	0	1	0	0	Enable 8 MSBs Only
1	0	1	0	1	Enable 4 LSBs Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. However, to ensure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier. See the HI-774 Timing Specifications, Convert Mode.

This variety of HI-X74(A) control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 4.

The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

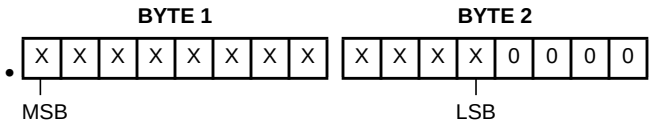
Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_O. Timing constraints are illustrated in Figure 5.

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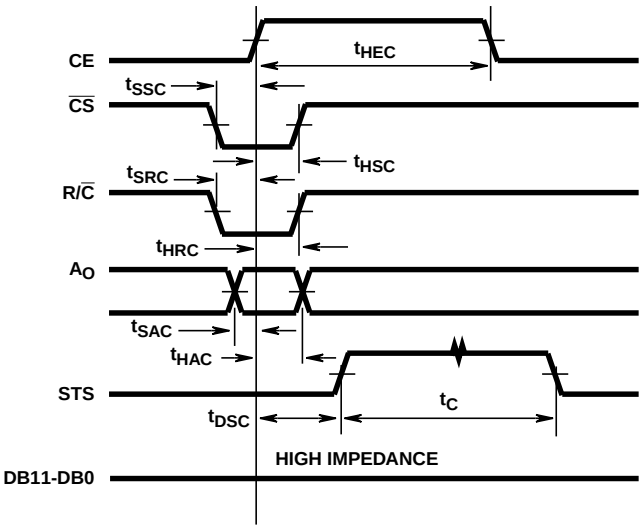
The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12-bit or 16-bit data bus. The A_O input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8-bit bytes, selected one at a time by A_O. This allows an 8-bit data bus to be connected as shown in Figure 6. A_O is usually tied to the least significant bit of the address bus, for storing the HI-X74(A) output in two consecutive memory locations. (With A_O low, the 8 MSBs only are enabled. With A_O high, 4 MSBs are disabled, bits 4 through 7 are forced low, and the 4 LSBs are enabled). This two byte format is considered “left justified data,” for which a decimal (or binary!) point is assumed to the left of byte 1:



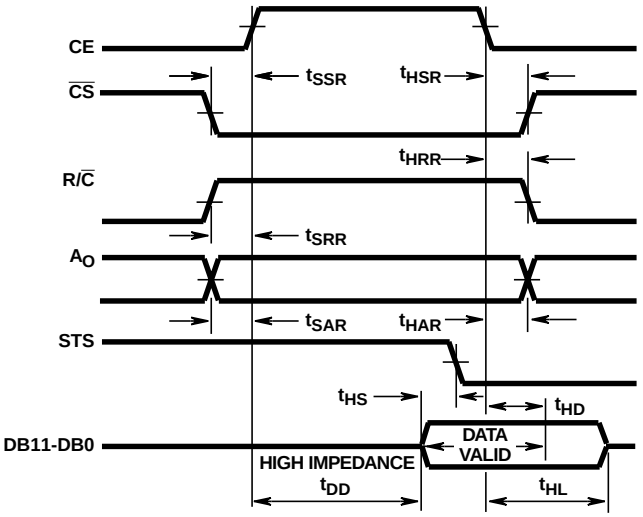
Further, A_O may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 6 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data, however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 5.



See HI-774 Timing Specifications for more information.

FIGURE 4. CONVERT START TIMING



See HI-774 Timing Specifications for more information.

FIGURE 5. READ CYCLE TIMING

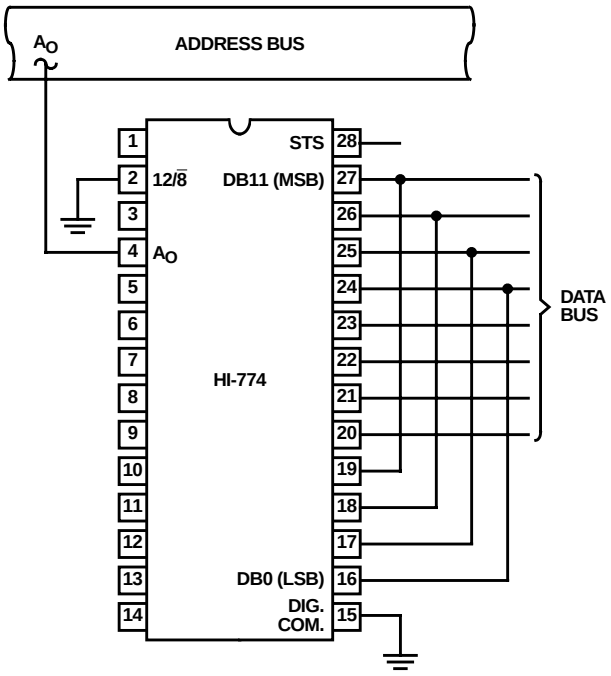


FIGURE 6. INTERFACE TO AN 8-BIT DATA BUS

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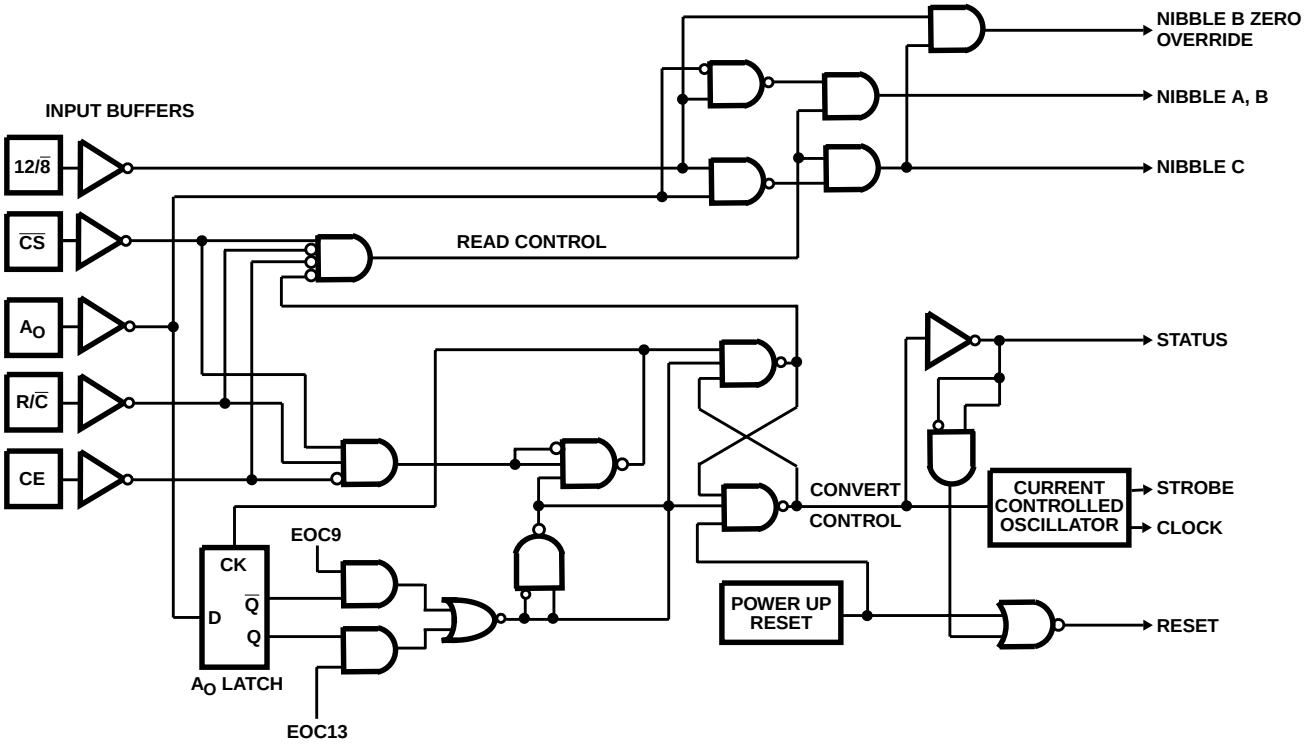


FIGURE 7. HI-774 CONTROL LOGIC

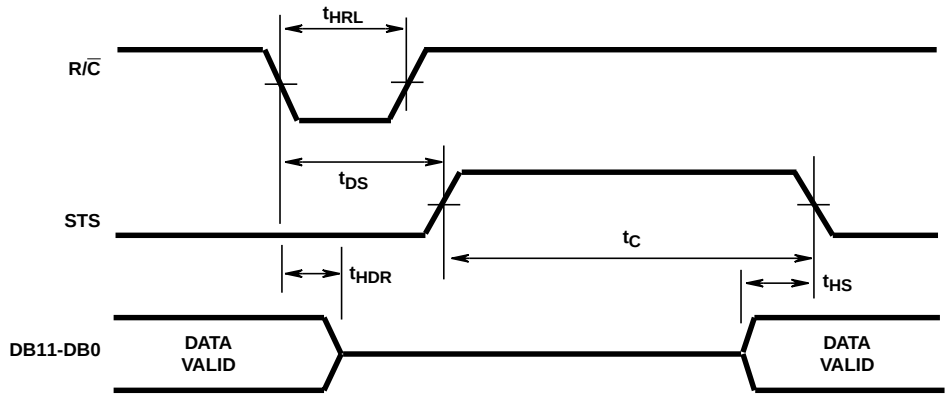


FIGURE 8. LOW PULSE FOR R/C - OUTPUTS ENABLED AFTER CONVERSION

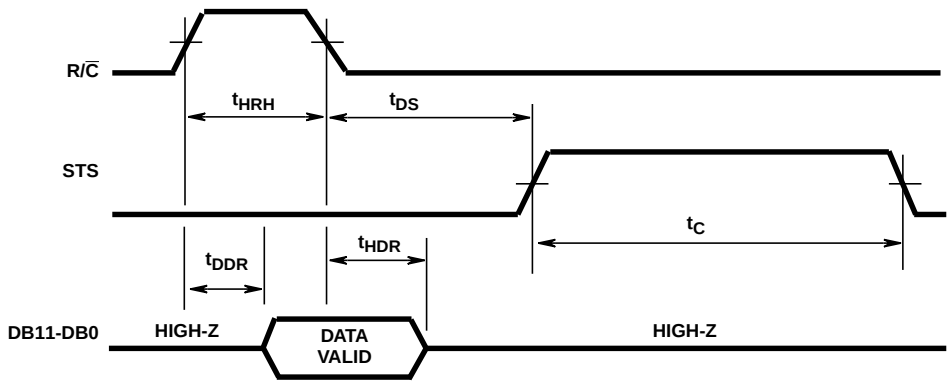


FIGURE 9. HIGH PULSE FOR R/C - OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

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Die Characteristics

DIE DIMENSIONS:

Analog: 3070mm x 4610mm
Digital: 1900mm x 4510mm

METALLIZATION:

Digital Type: Nitrox
Thickness: 10kÅ ±2kÅ

Metal 1: AlSiCu
Thickness: 8kÅ ±1kÅ

Metal 2: AlSiCu
Thickness: 16kÅ ±2kÅ

Analog Type: Al
Thickness: 16kÅ ±2kÅ

PASSIVATION:

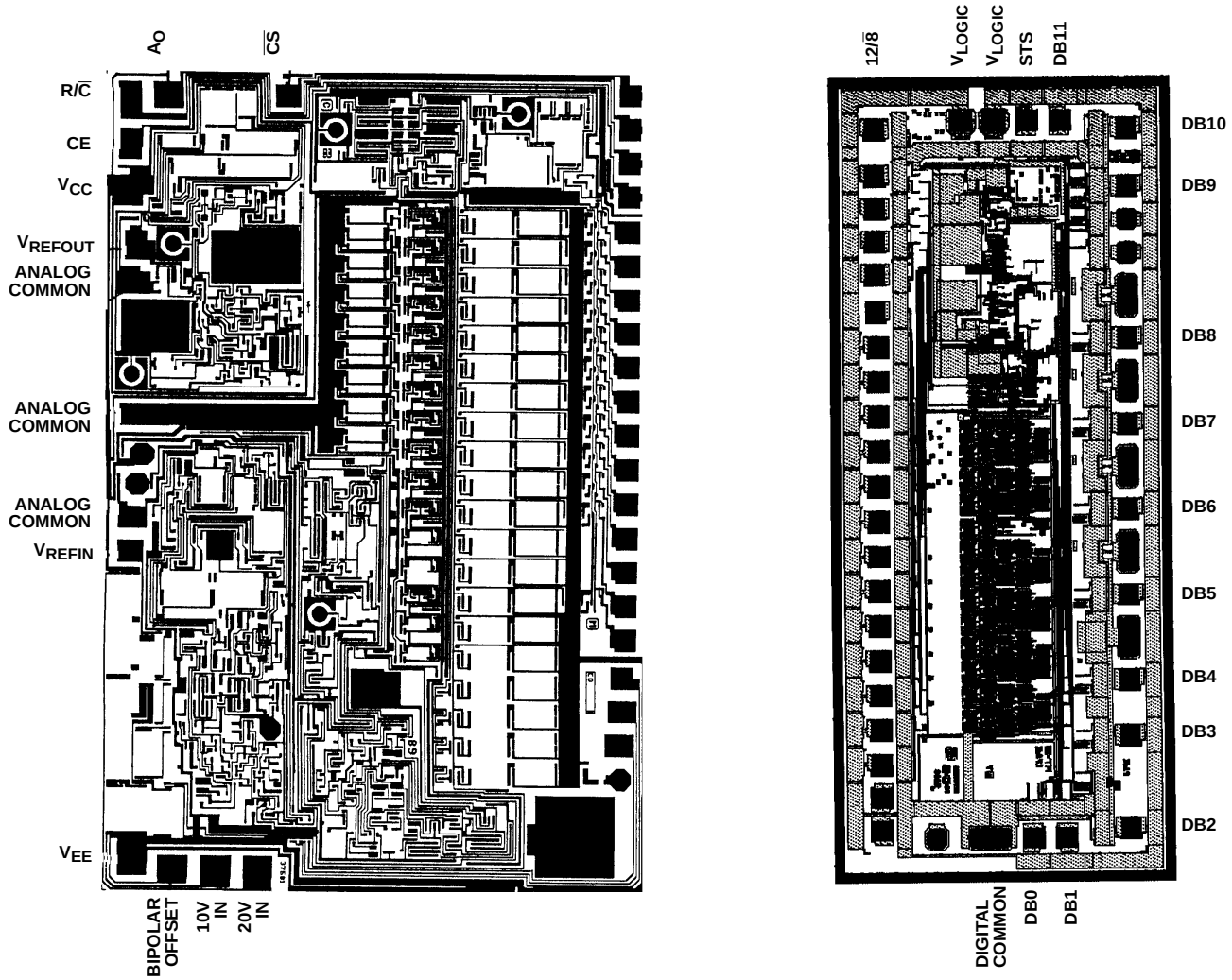
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±0.5kÅ
Silox Thickness: 12kÅ ±1.5kÅ

WORST CASE CURRENT DENSITY:

1.3×10^5 A/cm^2

Metallization Mask Layout

HI-574A, HI-674A, HI-774



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