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Base + 24 Read/Write Counter/Timer Data Register Byte 1

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD7	CTRD6	CTRD5	CTRD4	CTRD3	CTRD2	CTRD1	CTRD0

CTRD7-0 LSB for counter/timers 0 and 1

Base + 25 Read/Write Counter/Timer Data Register Byte 2

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD15	CTRD14	CTRD13	CTRD12	CTRD11	CTRD10	CTRD9	CTRD8

CTRD15-8 CSB (middle byte) for counter/timer 0, MSB for counter/timer 1

Base + 26 Read/Write Counter/Timer Data Register Byte 3

Bit No.	7	6	5	4	3	2	1	0
Name	CTRD23	CTRD22	CTRD21	CTRD20	CTRD19	CTRD18	CTRD17	CTRD16

CTRD23-16 MSB for counter/timer 0

Counter/timer 0 is 24 bits wide and uses all three bytes. Counter/timer 1 is 16 bits wide and uses only bytes 1 and 2. The bytes may be written and read in any order.

Base + 27 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTR	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

CTR	Counter no., 0 or 1
LATCH	Latch selected counter's current data into bytes 1-3 or 1-2 as appropriate
GTDIS	Disable gating on selected counter
GTEN	Enable gating on selected counter
CTDIS	Disable counting on selected counter
CTEN	Enable counting on selected counter
LOAD	Load selected counter with data in bytes 1-3 or 1-2 as appropriate
CLR	Clear selected counter to 0

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Base + 28 Read/Write Watchdog Timer A LSB Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDA7	WDA6	WDA5	WDA4	WDA3	WDA2	WDA1	WDA0

WDA7-0 LSB of timer A divisor; loading occurs for both bytes when the MSB is written

Base + 29 Read/Write Watchdog Timer A MSB Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDA15	WDA14	WDA13	WDA12	WDA311	WDA10	WD9	WD80

WDA15-8 MSB of timer A divisor; loading occurs for both bytes when the MSB is written

Base + 30 Read/Write Watchdog Timer B Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDB7	WDB6	WDB5	WDB4	WDB3	WDB2	WDB1	WDB0

WDB7-0 Watchdog timer B data register; loading occurs immediately upon writing to this register.

Base + 31 Read/Write Watchdog Timer Configuration Register

Bit No.	7	6	5	4	3	2	1	0
Name	WDTRIG		WDEN	WDSMI	WDRST	WDT-1	WDEDGE	WDIEN

WDTRIG If this bit is 1, the remaining bits of this register are ignored and instead the watchdog timer A is retriggered, i.e. reloaded with its initial value. If this bit is 0, the remaining bits in this register are used to configure the watchdog timer circuit.

WDEN Enable watchdog timer circuit: 0 = disabled, 1 = enabled

WDSMI Enable SMI interrupt upon watchdog timer timeout

WDRST Enable system reset upon watchdog timer timeout (setting this clears WDSMI)

WDT-1 Enable output pulse from timer A 1 clock early on WDO pin of I/O connectors. This allows WDO to be connected to WDI to prevent watchdog timer timeout as long as the timer is running.

WDEDGE Select active edge for hardware (external) retrigger: 0 = rising edge, 1 = falling edge

WDIEN Enable external input hardware watchdog trigger instead of on-board software trigger: 0 = internal trigger only, 1 = external trigger plus internal trigger are enabled

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10.1.3 PAGE 1 REGISTER DEFINITIONS

Base + 0 Write Page Register + Reset Command

Bit No.	7	6	5	4	3	2	1	0
Name	HOLDOFF	RESET					PAGE1	PAGE0

See page 0 for the definition of this register.

Base + 24 Write PWM Data Register LSB

Bit No.	7	6	5	4	3	2	1	0
Name	PWMD7	PWMD6	PWMD5	PWMD4	PWMD3	PWMD2	PWMD1	PWMD0

PWMD7-0 PWM data bits 7-0

Base + 25 Write PWM Data Register CSB

Bit No.	7	6	5	4	3	2	1	0
Name	PWMD15	PWMD14	PWMD13	PWMD12	PWMD11	PWMD10	PWMD9	PWMD8

PWMD15-8 PWM data bits 15-8

Base + 26 Write PWM Data Register MSB

Bit No.	7	6	5	4	3	2	1	0
Name	PWMD23	PWMD22	PWMD21	PWMD20	PWMD19	PWMD18	PWMD17	PWMD16

PWMD23-16 PWM data bits 23-16

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Base + 27 Write PWM Command Register

This register serves two purposes based on the value of bit 7, PCMD. Bit 7 = 0 indicates a PWM command, and bit 7 = 1 indicates a configuration command.

Bit No.	7	6	5	4	3	2	1	0
Name	0	0	PWM1	PWM0	0	0	0	CTR

0 Indicates a PWM command

0 Reserved for future use

PWM1-0 Indicates which PWM circuit is being accessed

000 Indicates a load counter command; this is the only command currently defined

CTR Indicates which counter to act on: 0 = rate counter, 1 = duty cycle counter

The above may also be thought of as two commands: 00..000 = load ctr 0, and 00..001 = load ctr 1.

Bit No.	7	6	5	4	3	2	1	0
Name	1	0	PWM1	PWM0	CLK	POL	OUTEN	ENAB

1 Indicates a PWM configuration byte

0 Reserved for future use

PWM1-0 Indicates which of the 4 PWM circuits is being accessed

CLK Selects internal clock source for both PWM counters: 0 = 10MHz, 1 = 100 KHz

POL Selects polarity of output pulse (active level): 0 = active low level, 1 = active high level

OUTEN Output enable: 0 = disabled (output held at inactive level based on setting of POL bit), 1 = enabled

ENAB PWM enable: 0 = disabled; 1 = running

Base + 28 Read/Write EEPROM / TrimDAC Data Register

Bit No.	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0

D7-0 Calibration data to be read or written to the EEPROM and/or TrimDAC.

During EEPROM or TrimDAC write operations, the data written to this register will be written to the selected device.

During EEPROM read operations this register contains the data to be read from the EEPROM and is valid after EEBUSY = 0.

The EEPROM data can be both read and written. The TrimDAC data can only be written; it cannot be read back.

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Base + 29 Read/Write EEPROM / TrimDAC Address Register

Bit No.	7	6	5	4	3	2	1	0
Name	A7	A6	A5	A4	A3	A2	A1	A0

A7-A0 EEPROM / TrimDAC address. The EEPROM recognizes address 0 – 255 using address bits A7 – A0. The TrimDAC recognizes addresses 0 – 7 using bits A2 – A0. In each case remaining address bits will be ignored.

NOTE: Current implementations of FPGA/Data Acquisition storage only take advantage of the lower 128 bytes of EEPROM data at the most. The remaining 128 bytes (addresses 128-255) are available for general use.

Base + 30 Write Calibration Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	EE_EN	EE_RW	RUNCAL	CMUXEN	TDACEN			

This register is used to initiate various commands related to autocalibration.

EE_EN EEPROM Enable. Writing a 1 to this bit will initiate a transfer to/from the EEPROM as indicated by the EE_RW bit. However if TDACEN is set simultaneously, EE_EN is ignored.

EE_RW Selects read or write operation for the EEPROM: 0 = Write, 1 = Read.

RUNCAL Writing 1 to this bit causes the board to reload the calibration settings from EEPROM registers 0-7 into the 8 TrimDACs. This is equivalent to a “reload” operation. During the reload operation, TDBUSY = 1.

CMUXEN Calibration multiplexer enable. The CMUXEN bit is used to enable calibration mode. After calibration is complete, CMUXEN is reset and the desired configuration is restored. The cal mux is used to read precision on-board reference voltages that are used in the autocalibration process. It also can be used to read back the value of analog output 0.

1 = enable cal mux and disable user analog input channels / muxes

0 = disable cal mux, enable user inputs

TDACEN TrimDAC Enable. Writing 1 to this bit will initiate a transfer to the TrimDAC. This bit overrides the setting of EE_EN, so that if both bits are set simultaneously, EE_EN will be ignored.

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Base + 30 Read Calibration Status Register

Bit No.	7	6	5	4	3	2	1	0
Name	0	TDBUSY	EEBUSY	CMUXEN	0	0	0	0

TDBUSY TrimDAC busy indicator

0 User may access TrimDAC

1 TrimDAC is being accessed or reload operation is in progress

EEBUSY EEPROM busy indicator

0 User may access EEPROM

1 EEPROM is being accessed

When either signal is 1, do not access the data and address registers at base + 12 and base + 13.

Base + 31 Write EEPROM Access Key Register

The user must write the value 0xA5 (binary 10100101) to this register each time after setting the PAGE bit in order to get access to the EEPROM. This helps prevent accidental corruption of the EEPROM contents.

Base + 31 Read FPGA Revision Code

This register may be read back to indicate the revision number of the FPGA design. The revision code for this design is 0x40.

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10.1.4 PAGE 2 REGISTER DEFINITIONS

Base + 0 Write Page Register + Reset Command

Bit No.	7	6	5	4	3	2	1	0
Name	HOLDOFF	RESET					PAGE1	PAGE0

See page 0 for the definition of this register.

Base + 24 Read A/D Feature ID Register

Bit No.	7	6	5	4	3	2	1	0
Name	ADQ7	ADQ6	ADQ5	ADQ4	ADQ3	ADQ2	ADQ1	ADQ0

ADQ7-0 Indicates the number of A/D channels available on the board

Base + 25 Read D/A Feature ID & FIFO Depth ID Register

Bit No.	7	6	5	4	3	2	1	0
Name	FDID2	FDID1	FDID0	DAQ4	DAQ3	DAQ2	DAQ1	DAQ0

FDID2-0 Indicates the maximum sample depth supported by the FPGA FIFO. Currently, only a value of "001" is defined, which describes a FIFO depth of 2048 samples.

DAQ4-0 Indicates the number of D/A channels available on the board

Base + 26 Read Digital I/O Feature ID Register

Bit No.	7	6	5	4	3	2	1	0
Name	DIOQ7	DIOQ6	DIOQ5	DIOQ4	DIOQ3	DIOQ2	DIOQ1	DIOQ0

DIOQ7-0 Indicates the number of DIO pins available on the board

Base + 27 Read PWM and Ctr/Timer Feature ID Register

This register serves two purposes based on the value of bit 7. Bit 7 = 0 indicates a load counter command, and bit 7 = 1 indicates a configure command.

Bit No.	7	6	5	4	3	2	1	0
Name	PWMQ3	PWMQ2	PWMQ1	PQMQ0	CTRQ3	CTRQ2	CTRQ1	CTRQ0

PWMQ3-0 Indicates the number of PWM channels available on he board

CTRQ3-0 Indicates the number of counter/timers available on the board

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Base + 28 Read Chip ID LSB

Bit No.	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Base + 29 Read CHIP ID MSB

Bit No.	7	6	5	4	3	2	1	0
Name	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

ID15-0 Indicates the unique chip ID according to a format TBD. Each revision of the chip, whether prototype or production, standard or custom, contains a unique 16-bit ID to enable software to distinguish between different versions.

ID15 = 0 indicates a prototype / unreleased version, and ID15 = 1 indicates a released design.

The current revision code (as per this document) should be 0x8000 or higher, as per the prototype / production criteria listed above.

10.1.5 PAGE 3 REGISTER DEFINITIONS

Base + 0 Write Page Register + Reset Command

Bit No.	7	6	5	4	3	2	1	0
Name	HOLDOFF	RESET					PAGE1	PAGE0

See page 0 for the definition of this register.

Base + 1-31 Read Copyright Notice

The remaining bytes 1-31 in page 3 are read-only and contain a copyright notice in 8-bit ASCII format.

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11. DATA ACQUISITION CIRCUIT CONFIGURATION

There are three primary configuration options for the Data Acquisition circuitry on the Hercules-EBX board:

- (A/D) : single-ended versus differential
- (A/D) : unipolar or bipolar
- (D/A) : unipolar or bipolar

These settings are all configured in software – no jumper configurations are required for these options. All of these settings are configured in the register located in PAGE 0; offset Base +1 (Analog Configuration register):

- Bit 0 = ADBU 0 = bipolar, 1 = unipolar A/D input range
- Bit 1 = SEDIFF 0 = single-ended, 1 = differential A/D mode
- Bit 2 = DABU 0 = bipolar, 1 = unipolar D/A output range (Default on reset is unipolar mode)

Single-ended / Differential Inputs

Hercules-EBX can accept both single-ended and differential inputs. A **single-ended** input uses 2 wires, input and ground. The measured input voltage is the difference between these two wires. A **differential** input uses 3 wires: input +, input -, and ground. The measured input voltage is the difference between the + and - inputs.

Differential inputs are frequently used when the grounds of the input device and the measurement device (Hercules-EBX) are at different voltages, or when a low-level signal is being measured that has its own ground wire. A differential input also has higher noise immunity than a single-ended input, since most noise affects both + and – input wires equally, so the noise will be canceled out in the measurement. The disadvantage of differential inputs is that only half as many are available, since two input pins are required to produce a single differential input. Hercules-EBX can be configured for either 32 single-ended inputs or 16 differential inputs.

If you have a combination of single-ended and differential input signals, select differential mode. Then to measure the single-ended signals, connect the signal to the + input and connect analog ground to the - input.

Note that the maximum measureable rail voltage is +/- 10V for differential inputs : any voltage outside of this range will measure as at the maximum rail (so if VIN0+ = +15V and VIN0-=+10V the differential voltage will measure as 0V since both voltages are outside of the maximum measureable range).

WARNING: The maximum range of voltages that can be applied to an analog input on Hercules-EBX without damage is ±35V. If you connect the analog inputs on Hercules-EBX to a circuit whose ground potential plus maximum signal voltage exceeds ±35V, the analog input circuit may be damaged. Check the ground difference between the input source and Hercules-EBX before connecting analog input signals.

Unipolar / Bipolar Inputs

The analog inputs can be configured for unipolar (positive input voltages only) or bipolar (both negative and positive input voltages).

Analog Output Configuration

The 4 analog outputs can also be configured for unipolar (positive voltages only) or bipolar (both negative and positive output voltages). In unipolar mode, the outputs range between 0-10V. In bipolar mode, the outputs range between ±10V.

When the board powers up or is reset, the analog outputs are also reset. The D/A powers up in unipolar mode with zero-scale output (0V default).

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12. ANALOG-TO-DIGITAL INPUT RANGES AND RESOLUTION

12.1.1 OVERVIEW

Hercules-EBX uses a 16-bit A/D converter. The full range of numerical values for a 16-bit number is 0 - 65535. However the A/D converter uses twos complement notation, so the A/D value is interpreted as a signed integer ranging from –32768 to +32767.

The smallest change in input voltage that can be detected is $1/(2^{16})$, or 1/65536, of the full-scale input range. This smallest change results in an increase or decrease of 1 in the A/D code, and so this change is referred to as 1 LSB, or 1 Least Significant Bit.

The analog inputs on Hercules-EBX have three configuration options:

- Single-ended or differential mode
- Unipolar or bipolar mode
- Input range (gain)

The single-ended / differential configuration, unipolar / bipolar configuration, and the input range selection are all handled in software.

12.1.2 INPUT RANGE SELECTION

Hercules-EBX can be configured to measure both unipolar (positive only) and bipolar (positive and negative) analog voltages. This configuration is done via the Analog Configuration Register (Page 0:Base+1) and applies to all inputs. In addition you can select a gain setting for the inputs, which causes them to be amplified before they reach the A/D converter. The gain setting is controlled in software, so it can be changed on a channel-by-channel basis. In general you should select the highest gain (smallest input range) that will allow the A/D converter to read the full range of voltages over which your input signals will vary. If you pick too high a gain, then the A/D converter will clip at either the high end or low end, and you will not be able to read the full range of voltages on your input signals.

12.1.3 INPUT RANGE TABLE

The table below indicates the analog input range for each possible configuration. The polarity is set in the Analog Configuration Register (Page 0:Base+1), and the gain is set with the G1 and G0 bits in the Input Range Control Register (Page 0:Base+4). The Gain value in the table is provided for clarity. Note that the single-ended vs. differential setting has no impact on the input range or the resolution.

Polarity	G1	G0	Input Range	Resolution (1 LSB)
Bipolar	0	0	±10V	305µV
Bipolar	0	1	±5V	153µV
Bipolar	1	0	±2.5V	76µV
Bipolar	1	1	±1.25V	38µV
Unipolar	0	0	0 – 10V	153µV
Unipolar	0	1	0 – 5V	76µV
Unipolar	1	0	0 – 2.5V	38µV
Unipolar	1	1	0 – 1.25V	19µV

Table 33: Data Acquisisition : Analog Input Range

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12.2 Performing an A/D Conversion

This chapter describes the steps involved in performing an A/D conversion on a selected input channel using direct programming (not with the driver software).

There are seven steps involved in performing an A/D conversion:

1. **Select the input channel**
2. **Select the input range**
3. **Wait for analog input circuit to settle**
4. **Initiate an A/D conversion**
5. **Wait for the conversion to finish**
6. **Read the data from the board**
7. **Convert the numerical data to a meaningful value**

12.2.1 SELECT THE INPUT CHANNEL

To select the input channel to read, write a low-channel/high-channel pair to the "A/D Low Channel Register" (Page 0:Base+2) and "A/D High Channel Register" (Page 0:Base+3) pair (see page 63). For the Hercules-EBX, only 5 bits are supported for each setting: "0"-"31" for the 32 potential input source channels. When you write any value to these registers, the current A/D channel is set to the low channel.

For example:

To set the board to channel 4 only, write 0x04 to Base + 2 (low channel) and 0x04 to Base + 3 (high channel).

To set the board to read channels 0 through 15, write 0x00 to Base + 2 (low channel) and 0x0F to Base + 3 (high channel).

⇒ **Note:** When you perform an A/D conversion, the current channel is automatically incremented to the next channel in the selected range. Therefore, to perform A/D conversions on a group of consecutively-numbered channels, you do not need to write the input channel prior to each conversion. For example, to read from channels 0 - 2, write Hex 00 to base + 2 and Hex 02 to base +3. The first conversion is on channel 0, the second will be on channel 1, and the third will be on channel 2. Then the channel counter wraps around to the beginning again, so the fourth conversion will be on channel 0 again and so on.

If you are sampling the same channel repeatedly, then you set both high and low to the same value as in the first example above. Then on subsequent conversions you do not need to set the channel again.

12.2.2 SELECT THE INPUT RANGE

Select the input range from among the available ranges shown on page 79. If the range is the same as for the previous A/D conversion then it does not need to be set again. Write this value to the A/D Input Range Control Register at Base + 4 (see page 64).

For example:

For a global (affects all channels) ±5V range (gain of 2), write 0x01 to Base + 4.

12.2.3 WAIT FOR ANALOG INPUT CIRCUIT TO SETTLE

After writing to either the channel registers (Base + 2, Base +3) or the input range register (Base + 4), you must allow time for the analog input circuit to settle before starting an A/D conversion. The board has a built-in 10μS timer to assist with the wait period. Monitor the WAIT bit at Base + 4 bit 6. When it is 1 the circuit is actively settling on the input signal. When it is 0 the board is ready to perform A/D conversions.

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12.2.4 PERFORM AN A/D CONVERSION ON THE CURRENT CHANNEL

After the above steps are completed, start the A/D conversion by writing to Base + 15, bit 0. This write operation only triggers the A/D if AINTE = 0 (interrupts are disabled). When AINTE = 1, the A/D can only be triggered by the on-board counter/timer or an external signal. This protects against accidental triggering by software during a long-running interrupt-based acquisition process.

```
outp(base +15,0x01);
```

12.2.5 WAIT FOR THE CONVERSION TO FINISH

The A/D converter chip takes up to either 4 or 9 microseconds to complete one A/D conversion, depending on the scan interval setting (Base + 12 : bit 3). Most processors and software can operate fast enough so that if you try to read the A/D converter immediately after starting the conversion, you will beat the A/D converter and get invalid data. Therefore the A/D converter provides a status signal, "ADBUSY," to indicate whether it is busy or idle. This bit can be read back as bit 7 in the "A/D Range/Status Readback Register" at Page 0 : Base+4. When the A/D converter is busy (performing an A/D conversion), this bit is 1 and the program must wait. When the A/D converter is idle (conversion is done and data is available), this bit is 0 and the program may read the data. Here are examples:

```
while (inp(base+4) & 0x80);    // Wait for conversion to finish before proceeding
```

This method could hang your program if there is a hardware fault and the bit is stuck at 1. Better is to use a loop with a timeout:

```
int checkstatus()       // returns 0 if ok, -1 if error
    int i;
    for (i = 0; i < 10000; i++)
    {
        if !(inp(base+4) & 0x80) then return(0);          // conversion completed
    }
    return(-1);         // conversion didn't complete
```

12.2.6 READ THE DATA FROM THE BOARD

Once the conversion is complete, you can read the data back from the A/D converter. The data is a 16-bit value and can be read back as either two 8-bit bytes or one 16-bit word. For 8-bit accesses, the LSB must be read from the board before the MSB, because the data is inserted into the board's FIFO in that order. Unlike other registers on the board, the A/D data may only be read one time, since each time a byte is read from the FIFO, the FIFO's internal pointer advances, and that byte is no longer available. Note that reading data from an empty FIFO returns unpredictable results.

The following pseudo-code illustrates how to read and construct the 16-bit A/D value with 8-bit accesses:

```
LSB = inp(base);
MSB = inp(base+1);
Data = MSB * 256 + LSB;   // combine the 2 bytes into a 16-bit value
```

Alternatively, the value can be read as one 16-bit value (which is preferred – this would increase the overall system bandwidth while reading data from the FIFO):

```
Data = inpw(base); // Where the MSB and LSB are all read in one access
```


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The final data is interpreted as a 16-bit signed integer ranging from –32768 to +32767. The "A/D LSB Register" and "A/D LSB Register" can be combined into one 16-bit read. These two registers fully support 16-bit I/O reads (in hardware), so the most efficient I/O method would be to read the two bytes as a single 16-bit word.

⇒ **Note:** The data range always includes both positive and negative values, even if the board is set to a unipolar input range. The data must now be converted to volts or other engineering units by using a conversion formula as shown on the next page.

In scan mode, the behavior is the same except that when the program initiates a conversion, all channels in the programmed channel range will be sampled once, and the data will be stored in the FIFO. The FIFO depth register will increment by the scan size. When ADBUSY goes low, the program should read out the data for all channels.

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12.2.7 CONVERT THE NUMERICAL DATA TO A MEANINGFUL VALUE

Once you have the A/D value, you need to convert it to a meaningful value. The first step is to convert it back to the actual measured voltage. Afterwards you may need to convert the voltage to some other engineering units (for example, the voltage may come from a temperature sensor, and then you would need to convert the voltage to the corresponding temperature according to the temperature sensor's characteristics).

Since there are a large number of possible input devices, this secondary step is not included here; only conversion to input voltage is described. However you can combine both transformations into a single formula if desired.

To convert the A/D value to the corresponding input voltage, use the following formulas:

Conversion Formula for Bipolar Input Ranges

Input voltage = A/D value / 32768 * Full-scale input range

Example: Input range is ±5V and A/D value is 17761:
Input voltage = 17761 / 32768 * 5V = 2.710V

For a bipolar input range, 1 LSB = 1/32768 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a bipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for ±5V range
-32768	$-V_{FS}$	-5.0000V
-32767	$-V_{FS}$ + 1 LSB	-4.9998V
…	…	…
-1	-1 LSB	-0.00015V
0	0	0.0000V
1	+1 LSB	0.00015V
…	…	…
32767	V_{FS} - 1 LSB	4.9998V

Conversion Formula for Unipolar Input Ranges

Input voltage = (A/D value + 32768) / 65536 * Full-scale input range

Example: Input range is 0-5V and A/D value is 17761:
Input voltage = (17761 + 32768) / 65536 * 5V = 3.855V

For a unipolar input range, 1 LSB = 1/65536 * Full-scale voltage.

Here is an illustration of the relationship between A/D code and input voltage for a unipolar input range (V_{FS} = Full scale input voltage):

A/D Code	Input voltage symbolic formula	Input voltage for 0-5V range
-32768	0V	0.0000V
-32767	1 LSB (V_{FS} / 65536)	0.000076V
…	…	…
-1	V_{FS} / 2 - 1 LSB	2.4999V
0	V_{FS} / 2	2.5000V
1	V_{FS} / 2 + 1 LSB	2.5001V
…	…	…
32767	V_{FS} - 1 LSB	4.9999V

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12.3 A/D Scan, Interrupt, and FIFO Operation

The control bits SCANEN (scan enable) and AINTE (A/D interrupt enable) in conjunction with the FIFO determine the behavior of the board during A/D conversions and interrupts.

At the end of an A/D conversion, the 16-bit A/D data is latched into the 8-bit FIFO in an interleaved fashion, first LSB, and then MSB. A/D Data is read out of the FIFO with 1 16-bit or 2 8-bit read operations, first Base + 0 (LSB) and then Base + 1 (MSB).

When SCANEN = 1, each time an A/D trigger occurs, the board will perform an A/D conversion on all channels in the channel range programmed in the A/D Low Channel Register (Base + 2) and A/D High Channel Register (Base + 3). When SCANEN = 0, each time an A/D trigger occurs, the board will perform a single A/D conversion and then advance to the next channel and wait for the next trigger.

During interrupt operation (AINTE = 1), the FIFO will fill up with data until it reaches the threshold programmed in the FIFO threshold register, and then the interrupt request will occur. If AINTE = 0, the FIFO threshold is ignored and the FIFO continues to fill up.

The FIFO Threshold Registers should be set to the desired depth before configuring the system to begin operation in interrupt mode. The maximum FIFO depth can be read from the FIFO Depth ID Register (Page 2: Base + 25): This register should always return a value of a value of "001" for the FIFO ID: means a maximum depth of 2048 samples.

To set the FIFO depth, the FIFO Threshold should be configured by writing the depth (in samples) to the "FIFO Threshold Register LSB" (Page 0: Base + 8) and "FIFO Threshold Register MSB" (Page 0: Base + 9). Note that this setting is in units of "samples", where one "sample" is 2 bytes. The current maximum setting would be 2047 (Base + 8 = Hex FF; Base + 9 = 0x07).

If the FIFO reaches its limit (as set in the two FIFO Threshold Registers located at Page 0: Base +8 and Base +9), then the next time an A/D conversion occurs the FIFO Threshold flag (Base + 14 : bit 3) would be set. At the same time, an interrupt would be generated (if FIFOEN = 1 and ADINTE = 1).

If the FIFO overflows, then the Overflow flag OVF will be set as the 2049th sample is taken. In this case the FIFO will not accept any more data, and its contents will be preserved and may be read out. In order to clear the overflow condition, the program must reset the FIFO by writing to the FIFORST bit in Base + 15, or a hardware reset must occur.

Note that the current FIFO state can be read at any time by checking the two FIFO Depth Registers: "FIFO Depth Register LSB" at Page 0: Base + 10 and "FIFO Depth Register MSB" at Page 0: Base + 11. These registers will return the number of samples currently in the FIFO. They are incremented with each A/D converter sample stored and are decremented with every FIFO sample read out (via the A/D LSB Register and A/D MSB register located at Base+0 and Base + 1, respectively).

In Scan mode (SCANEN = 1), the FIFO threshold should be set to a number at least equal to the scan size and in all cases equal to an integral number of scans. For example if the scan size is 8 channels, the FIFO threshold could be set to 8, 16, 24, 32, 40, 48, etc. but not less than 8. This way the interrupt will occur at the end of the scan, and the interrupt routine can read in a complete scan or set of scans each time it runs.

In non-scan mode (SCANEN = 0), the FIFO threshold should be set to a level that minimizes the interrupt rate but leaves enough time for the interrupt routine to respond before the next A/D conversion occurs. Remember that no data is available until the interrupt occurs, so if the rate is slow the delay to receive A/D data may be long. Therefore for slow sample rates the FIFO threshold should be small. If the sample rate is high, the FIFO threshold should be high to reduce the interrupt rate. However remember that the remaining space in the FIFO determines the time the interrupt routine has to respond to the interrupt request. If the FIFO threshold is too high, the FIFO may overflow before the interrupt routine responds. A good rule of thumb is to limit the interrupt rate to no more than 1,000-2,000 per second in Windows and Linux or 10,000 per second in DOS. Experimentation may be necessary to determine the optimum FIFO threshold for each application.

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The table on the next page describes the board's behavior for each of the 4 possible cases of AINTE and SCANEN. The given interrupt software behavior describes the operation of the Diamond Systems Universal Driver software. If you write your own software or interrupt routine you should conform to the described behavior for optimum results.

12.4 Hercules-EBX A/D Operating Modes

The following control bits and values are referenced in the descriptions in the table below.

LOW	Page 0: Base + 2 (5-bit number, 0-31)
HIGH	Page 0: Base + 3 (5-bit number, 0-31)
WAIT	Page 0: Base + 4, bit 6
ADBUSY	Page 0: Base + 4, bit 7
FIFO threshold	Page 0: Base + 8 (LSB), Base + 9 (MSB)
CLKEN	Page 0: Base +13, bit 0
CLKSEL	Page 0: Base +13, bit 1
SCANEN	Page 0: Base + 13 bit 2
AINTE	Page 0: Base + 13 bit 4
ADSTS	signal from A/D Converter (called "BUSY" at A/D output)

There are 8 cases to consider for A/D conversions using FIFOEN, SCANEN, and AINTE.

In all cases, at the end of an AD conversion A/D data is latched into the FIFO. Data is read out of the FIFO with 2 read operations, nominally from Base+ 0 and Base + 1. However reading from either address will result in the same byte being read from the FIFO, so the program can actually perform 2 reads from the same address to get the A/D data. For all cases where AINTE = 1, CLKEN must also be set to 1.

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AINTE	FIFOEN	SCANEN	Operation
0	0	0	Single A/D conversions are triggered by write to Base+15, bit 0. ADBUSY = ADSTS (from A/D) No interrupt occurs. The user program monitors ADBUSY and reads A/D data when it goes low.
0	0	1	A/D Scans are triggered by write to Base+15, bit 0. All channels between LOW and HIGH will be sampled. ADBUSY goes high at the first ADSTS high pulse and stays high until the last ADSTS pulse goes low. No interrupt occurs. The user program monitors WAIT and then reads the A/D data when it goes low.
0	1	0	Same operation as case 000 above. The FIFO is not used in this case.
0	1	1	Same operation as case 001 above. The FIFO is not used in this case.
1	0	0	Single A/D conversions are triggered by the source selected with CLKSEL. ADBUSY = ADSTS INT goes high after each conversion is done (when ADBUSY goes low). The interrupt routine reads one A/D sample each time it runs.
1	0	1	A/D Scans are triggered by the source selected with CLKSEL. ADBUSY goes high at the first ADSTS high pulse and stays high until the last ADSTS pulse goes low. INT goes high after the last ADBUSY pulse goes low (i.e. when WAIT goes low). The interrupt routine reads out one entire A/D scan each time it runs.
1	1	0	Single A/D conversions are triggered by the source selected with CLKSEL. ADBUSY = ADSTS A/D interrupt occurs when the FIFO reaches its programmed threshold. The interrupt routine reads out a number of samples equal to the FIFO threshold each time it runs.
1	1	1	A/D scans are triggered by the source selected with CLKSEL. ADBUSY goes high at the first ADSTS high pulse and stays high until the last ADSTS pulse goes low. INT goes high after the last ADBUSY pulse goes low (i.e. when WAIT goes low) AND an integral no. of scans has occurred and the FIFO threshold is reached. The interrupt routine reads out a number of samples equal to the FIFO threshold each time it runs.

Table 34: A/D Operating Modes

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13. DIGITAL-TO-ANALOG OUTPUT RANGES AND RESOLUTION

13.1 Description

Hercules-EBX uses a 4-channel 12-bit D/A converter (DAC) to provide 4 analog outputs. A 12-bit DAC can generate output voltages with the precision of a 12-bit binary number. The maximum value of a 12-bit binary number is 2^{12} - 1, or 4095, so the full range of numerical values that the DACs support is 0 - 4095. The value 0 always corresponds to the lowest voltage in the output range, and the value 4095 always corresponds to the highest voltage minus 1 LSB (the theoretical top end of the range corresponds to an output code of 4096 which is impossible to achieve).

⇒ **Note:** In this manual, the terms analog output, D/A, and DAC are all used interchangeably to mean the conversion of digital data originating from the Hercules-EBX computer hardware to an analog signal terminating at an external source.

13.2 Resolution

The *resolution* is the smallest possible change in output voltage. For a 12-bit DAC the resolution is $1/(2^{12})$, or 1/4096, of the full-scale output range. This smallest change results from an increase or decrease of 1 in the D/A code, and so this change is referred to as 1 LSB, or 1 least significant bit. The value of this LSB is calculated as follows:

1 LSB = Output voltage range / 4096

Example: Output range = 0-10V;

Output voltage range = 10V – 0V = 10V

1 LSB = 10V / 4096 = 2.44mV

Example: Output range = ±10V;

Output voltage range = 10V – (-10V) = 20V

1 LSB = 20V / 4096 = 4.88mV

13.3 Output Range Selection

The Analog Configuration Register located at Page 0: Base +1 is used to select the DAC output range. See page 63 for configuration data. The DACs can be configured for 0-10V or ±10V.

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13.4 D/A Conversion Formulas and Tables

The formulas below explain how to convert between D/A codes and output voltages.

D/A Conversion Formulas for Unipolar Output Ranges

Output voltage = (D/A code / 4096) * Reference voltage

D/A code = (Output voltage / Reference voltage) * 4096

Example: Output range in unipolar mode = 0 – 10V
Full-scale range = 10V – 0V = 10V
Desired output voltage = 2.000V
D/A code = 2.000V / 10V * 4096 = 819.2 => 819

Note the output code is always an integer.

For the unipolar output range 0-10V, 1 LSB = 1/4096 * 10V = 2.44mV.

Here is an illustration of the relationship between D/A code and output voltage for a unipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for 0 – 10V range
0	0V	0.0000V
1	1 LSB (V_{REF} / 4096)	0.0024V
…	…	…
2047	V_{REF} / 2 - 1 LSB	4.9976V
2048	V_{REF} / 2	5.0000V
2049	V_{REF} / 2 + 1 LSB	5.0024V
…	…	…
4095	V_{REF} - 1 LSB	9.9976V

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D/A Conversion Formulas for Bipolar Output Ranges

Output voltage = ((D/A code – 2048) / 2048) * Output reference

D/A code = (Output voltage / Output reference) * 2048 + 2048

Example: Output range in bipolar mode = ±10V
Full-scale range = 10V – (-10V) = 20V
Desired output voltage = 2.000V
D/A code = 2V / 10V * 2048 + 2048 = 2457.6 => 2458

For the bipolar output range ±10V, 1 LSB = 1/4096 * 20V, or 4.88mV.

Here is an illustration of the relationship between D/A code and output voltage for a bipolar output range (V_{REF} = Reference voltage):

D/A Code	Output voltage symbolic formula	Output voltage for ±10V range
0	$-V_{REF}$	-10.0000V
1	$-V_{REF}$ + 1 LSB	-9.9951V
…	…	…
2047	-1 LSB	-0.0049V
2048	0	0.0000V
2049	+1 LSB	0.0049V
…	…	…
4095	V_{REF} - 1 LSB	9.9951V

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13.4.1 GENERATING AN ANALOG OUTPUT

This chapter describes the steps involved in generating an analog output (also called performing a D/A conversion) on a selected output channel using direct programming (not with the driver software).

There are three steps involved in performing a D/A conversion:

1. **Compute the D/A code for the desired output voltage**
2. **Write the value to the selected output channel**
3. **Wait for the D/A to update**

13.4.2 COMPUTE THE D/A CODE FOR THE DESIRED OUTPUT VOLTAGE

Use the formulas on the preceding page to compute the D/A code required to generate the desired voltage.

⇒ **Note:** The DAC cannot generate the actual full-scale reference voltage; to do so would require an output code of 4096, which is not possible with a 12-bit number. The maximum output value is 4095. Therefore the maximum possible output voltage is always 1 LSB less than the full-scale reference voltage.

13.4.3 WRITE THE VALUE TO THE SELECTED OUTPUT CHANNEL REGISTERS

First use the following formulas to compute the LSB and MSB values:

LSB = D/A Code & 255 ;keep only the low 8 bits

MSB = int(D/A code / 256) ;strip off low 8 bits, keep 4 high bits

Example:

Output code = 1776

LSB = 1776 & 255 = 240 (F0 Hex); MSB = int(1776 / 256) = int(6.9375) = 6

The LSB is an 8-bit number in the range 0-255. The MSB is a 4-bit number in the range 0-15.

The MSB is always rounded DOWN. The truncated portion is accounted for by the LSB.

Now write these values to the output registers. The LSB is written to Page 0: Base + 6. The MSB is written to Page 0: Base + 7.

outp(Base + 6, LSB);

outp(Base + 7, MSB);

13.4.4 SET REGISTERS FOR CHANNEL

Now that the value for the given channel is set, the channel selection needs to be made in order to latch the data to the D/A. At this time, the decision must be made as to whether to pass the data to the D/A immediately ("Transparent pass-through" mode) or to latch and hold the data until all of the D/A channels are set ("Simultaneous Update" mode).

"Transparent Mode" will send the data (just written in the previous step) to the D/A beginning immediately after the channel selection is made. The D/A output will be updated as soon as the data is transferred and the internal analog circuitry with a worst-case settling time of ~10usec (as per the DAC7715 specification).

"Simultaneous Update Mode" will latch the data into an internal buffer for that channel, but will not update the A/D until instructed to do so. In this manner, several (or all 4) of the A/D channels can

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be configured and then updated simultaneously. This allows for a uniform transition time for all A/D outputs.

To send the data to the D/A immediately, write the channel number to Page 0: Base+5 bits 1-0. For Transparent mode, bit 8 should be set to "0":

outp(Base + 5, Channel Number);

Where "Channel Number" is 0-3

To latch the data in preparation for more updates (not sending the data to the D/A until channel data updates are completed), write the channel number to Page 0: Base+5 bits 1-0, with bit 8 should be set to "1". :

outp(Base + 5, 0x80 + Channel Number);

Where "Channel Number" is 0-3

The D/A data will be held until a "0" is written to the Simultaneous Update bit, at which time all of the latched data will be updated at the same time. So, if data has previously been latched with the simultaneous update bit set to "1" and the data for the last channel involved in the simultaneous update has just been written to Base + 6 and Base + 7, then the final channel selection (which would send all of the latched data to the D/A) would look just like a "Transparent Mode" write, i.e.:

outp(Base + 5, Channel Number);

Where "Channel Number" is 0-3

At this point, all of the latched data would be enabled through the D/A and the analog outputs would begin the transition to the selected values at the same time.

13.4.5 WAIT FOR THE D/A TO UPDATE

Writing the channel number to Base + 5, regardless of the state of the "SU" bit, starts the D/A update process for the selected channel(s). The update process requires approximately 30 microseconds to transmit the data to the D/A chip (and then update the D/A circuit in the chip, if the data is to be passed through immediately). During this period, no attempt should be made to write to any other channel in the D/A through addresses Base + 6 or Base + 7.

The status bit DABUSY (Page 0 : Base + 4 bit 5) indicates whether the D/A is busy updating (1) or idle (0). After writing to the D/A, monitor this bit until it is zero before proceeding to the next D/A operation.

Note that the time required to transfer data for a channel occurs whether the "Simultaneous Update" bit is set or not: the data is transferred (and the DABUSY signal is active) regardless of whether the data is to be immediately updated or is being latched in preparation for later simultaneous update. The only difference in the two modes occurs after the Digital data is transferred: in "Transparent mode" the data will immediately pass through the D/A whereas "Simultaneous Update" mode will conclude with the D/A output data unchanged.

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13.5 Analog Circuit Calibration Resources

For a board with the Data Acquisition option, the Hercules-EBX Data Acquisition circuitry incorporates some advanced calibration features to allow the system to calibrate both the A/D and D/A signal conversion pathways. The registers involved in controlling these calibration features are listed below:

Register Bit Name	Register location	Signal Name	Description
ADBU	<All pages>Base+1:Bit 0	ADCUNI(OUT)	a one sets A/D section to unipolar input mode
DABU	<All pages>Base+1:Bit 2	DACUNI(OUT)	a one sets D/A section to bipolar output mode
CMUXEN	Page 0:Base+30:Bit 4	MUXEN4(OUT)	a one enables calibration voltages multiplexer
SEDIFF	<All pages>Base+1:Bit 1	ADDIFF(OUT)	a one sets A/D section to differential mode
TrimDAC Data	Page 1 : Base+28 (8-bit)	TrimDAC Data[D7-D0]	Data Sent to TrimDAC
TrimDAC Address	Page 1 : Base+29 : Bits 2-0	TrimDAC Address [A2-A0]	Address for TrimDAC
TDACEN	Page 1 : Base+30 : Bit 3	TDACEN	TrimDAC Enable (when "1") – note that this is mutually-exclusive with EE_EN control

Table 35: Calibration Control Signal Listing

AUTO CALIBRATION TABLE:

When Register bit CMUXEN=1, the board is in auto calibration mode. When this mode is enabled, specific calibration voltages will be fed back to analog channel inputs. There are 5 calibration settings that can be used (named "VCAL0 – 5" below). These feedback voltages are selected based on the "ADCH0" and "ADCH1" settings (ADCH4-2 are ignored during autocalibration):

CMUXEN	SEDIFF	ADCH(1/0)	VCAL	VOLTAGE
0	**Normal Operation**			
1	0	0 (0/0)	0	0
1	0	1(0/1)	1	2.5mV
1	0	2 (1/0)	2	1.12V
1	0	3 (1/1)	3	4.78V
1	1	X	4	VOUT0

Table 36: Calibration Multiplexed Signal Control

Notes:

- VCAL0 is for bipolar A/D offset adjustments
- VCAL1 is for unipolar offset adjustments
- VCAL2 is for full scale 0-1.25, 0-2.5, +/-1.25 and +/-2.5 modes
- VCAL3 is for full scale 0-5, 0-10, +/-5 and +/-10 modes
- VCAL4 is D/A VOUT0 for D/A calibration; this loops Analog output "VOUT0" back

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OUTPUT (TrimDAC Address)	NAME	FUNCTION	POLARITY
O0	ADCOFF coarse	A/D offset, all modes, coarse	The same for bipolar, Inversed for unipolar
O1	ADCOFF fine	A/D offset, fine	The same for bipolar, Inversed for unipolar
O2	ADCFUL coarse	A/D full scale, all modes, coarse	Inversed
O3	ADCFUL fine	A/D full scale, fine	Inversed
O4	DACOFF coarse	D/A offset, coarse	Inversed
O5	DACOFF fine	D/A offset, fine	Inversed
O6	DACFUL coarse	D/A full scale, coarse	The same
O7	DACFUL fine	D/A full scale, fine	The same

Table 37: Trim-DAC (AD8801) Outputs

Notes:

- "The same" means: increase in the trimDAC value increases readout and vice versa
- "Inversed" means: increase in the trimDAC value decreases readout and vice versa
- "Coarse" adjustment is the basic trimDAC variance, while "Fine" only affects adjustment of about 1% of full effect in all modes

13.6 Analog Circuit Calibration Procedures

Calibration applies only to boards with the analog I/O circuitry.

The analog I/O circuit is calibrated during production test prior to shipment. Over time the circuit may drift slightly. If calibration is desired, internal autocalibration can be performed using the software routines provided with the Diamond Software driver libraries (part of the Hercules-EBX development kit). For analog I/O circuit configuration see page 63.

Six adjustments are possible:

- A/D bipolar offset
- A/D unipolar offset
- A/D full-scale
- D/A bipolar offset
- D/A unipolar offset
- D/A full-scale

The specific algorithms required to perform autocalibration can be quite involved, and are too detailed to go into at great length here. Suffice it to say that such procedures are provided in the included drivers and that details of autocalibration can be provided as necessary.

Note that the Autocalibration settings are stored in nonvolatile memory in the calibration EEPROM and are reloaded each time the on-board FPGA (or system) is reset.

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13.7 Using EEPROM

There is an EEPROM used to store all TrimDAC adjustment values. These values are loaded on reset or power-up, so it is critical that these values be correct in order to maintain accurate A/D measurements. These settings are configured to defaults during manufacturing test – be sure that you know what you are doing before changing these settings.

The EEPROM provides 256 bytes of non-volatile storage. The first 128 (addresses 00-0x7F) bytes are reserved for Auto Calibration settings and should not be overwritten. The last 128 bytes are available for user-accessible non-volatile storage.

Note that access to EEPROM data can be handled through the DSCUD software utilities.

Remember that bytes 0-127 are reserved for system use (TrimDAC autocal values); altering those values will adversely affect system calibration.

13.7.1 READING VALUE FROM EEPROM

Example : read one byte from EEPROM location 128:

```
outp(base+0, 0x01);     // set page to page 1
outp(base+15, 0xA5);    // unlock EEPROM
outp(base+29,0x80);     // set address location to 128 (0x80)
outp(base+30, 0xC0);    // Initiate transfer, set to read
while (inp(base+30) & 0x20);    // Wait for EEPROM load to complete
Data = inpb(base+28);   // data returned from EEPROM access
outp(base+0, 0x00);     // set page to page 0 (and re-enables lock on EEPROM / TrimDAC)
```

13.7.2 WRITING VALUE TO EEPROM

Example : write one byte (value = 0xaa) to EEPROM location 254, then verify the data:

```
outp(base+0, 0x01);     // set page to page 1
outp(base+15, 0xA5);    // unlock EEPROM
outp(base+29,0xFE);     // set address location to 254 (0xFE)
outp(base+28, 0xAA);    // Set data to write to EEPROM
outp(base+30, 0x80);    // Initiate transfer, set to write
while (inp(base+30) & 0x20);    // Wait for EEPROM write to complete
outp(base+15, 0xA5);    // unlock EEPROM
outp(base +29,0xFE);    // set address location to 254 (0xFE)
outp(base+30, 0xC0);    // Initiate transfer, set to read
while (inp(base+30) & 0x20);    // Wait for EEPROM load to complete
Data = inpb(base+28);   // data returned from EEPROM access; data should be 0xAA
outp(base+0, 0x00);     // set page to page 0 (and re-enables lock on EEPROM / TrimDAC)
```


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13.8 Digital I/O Operation

Hercules-EBX contains 40 digital I/O lines organized as four 8-bit I/O ports, A, B, C, D, and E. The direction for each port is independently programmable. The ports are accessed at registers Base + 16 through Base + 20 respectively, and the direction register is at Base + 22 (all on Page 0).

Offset	7	6	5	4	3	2	1	0
12	LED	SINGLE	DIOCTR1	DIOCTR0	SCINT	CLKSRC1	CLKFRQ1	CLKFRQ 0
..								
16	DIOA7	DIOA6	DIOA5	DIOA4	DIOA3	DIOA2	DIOA1	DIOA0
17	DIOB7	DIOB6	DIOB5	DIOB4	DIOB3	DIOB2	DIOB1	DIOB0
18	DIOC7	DIOC6	DIOC5	DIOC4	DIOC3	DIOC2	DIOC1	DIOC0
19	DIOD7	DIOD6	DIOD5	DIOD4	DIOD3	DIOD2	DIOD1	DIOD0
20	DIOE7	DIOE6	DIOE5	DIOE4	DIOE3	DIOE2	DIOE1	DIOE0
..								
22	MODE	P2	P1	P0 / DIRE	B2 / DIRD	B1 / DIRC	B0 / DIRB	D / DIRA

Table 38: DIO Data and Control Registers (Page 0)

The digital I/O lines are located at pins 1 through 40 on the I/O header J8 (see page 16). They are 3.3V and 5V logic compatible. Each output is capable of supplying –8mA in logic 1 state and +12mA in logic 0 state. See the specifications on page 107 for more detail.

DIRA, DIRB, DIRC, DIRD, and DIRE control the direction of ports A, B, C, D, and E, respectively. A 0 means input and a 1 means output. All ports power up to input mode and the output registers are cleared to zero. When a port direction is changed to output, its output register is cleared to zero. When a port is in output mode, its value can be read back.

There are two methods of programming the Digital I/O ports: as individual bits (useful for output only) or as bytes (for either input or output).

BIT Mode : To program a specific output bit, bit-mode operation can be used. This is mode is selected by writing a "1" to the MODE bit of the "Digital I/O Configuration / Bit Programming Register" located at Base + 22. When setting this in bit mode, bits 6-4 select the DIO port (A-E, values 0-4), bits 3-1 select the bit within the port (bit selection 0-7), and bit 0 selects the value for the bit in question.

In this mode, an individual output bit for one of the 40 available DIO bits can be individually assigned a value. As an example, the following would set bit 4 of DIO port B to "0" and then would set DIO port B to an output (with all other ports set to input):

```
outp(base+22, 0x98);   // Selects:   Bit Mode (bit 7=1),
                       //            Port B (bits 6-4 = 001),
                       //            bit 4 (bits 3-1 = 100),
                       //            value = 0 (bit 0=0)
outp(base+22, 0x02);   // Selects:   DIO direction Mode (bit 7=0) and
```


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```
                                //          Port B is output; ports A,C,D,E all inputs
```

BYTE Mode : For byte-mode operation, the data for a given byte is read or written to the appropriate DIO byte register: DIO ports A-E are located at Base+16 – Base+20, respectively. As an example, the following illustrates setting port A to output (B-E to input), writing a value of "AA" to port A, and reading data from port C:

```
outp(base+22, 0x01);    // Selects:    DIO direction Mode (bit 7=0) and
                        //             Port A is output; ports B,C,D,E all inputs
outp(base+16, 0xAA);    // Send data to DIO output port A
data = inp(base+18);    // Read data from port C
```

Note that accessing a Digital Output port can be handled as bit or byte-level accesses interchangeably – the two methods are provided to allow maximum flexibility for output operations.

13.9 Special Digital I/O Operation – Port E

In addition to the standard Digital I/O operation detailed above, port E may alternatively be configured for some special I/O functions, allowing access to several special-purpose Digital I/O controls. These special functions are controlled with the DIOCTR0 and DIOCTR1 bits.

DIOCTR0 controls the special functions for DIO E3-E0:

J8 - Pin Number	DIOCTR0	
	0	1
33	DIO E0	PWM0
34	DIO E1	PWM1
35	DIO E2	PWM2
36	DIO E3	PWM3

Table 39: DIOCTR0 (DIO3-0 Alternate Functions)

See section on PWM functionality for details on PWM functions for these pins (when DIOCTR0 = 1).

DIOCTR1 controls the special functions for DIO E7-E4:

J8 - Pin Number	DIOCTR1	
	0	1
37	DIO E4	GATE 0
38	DIO E5	DIOLATCH
39	DIO E6	TOUT 1
40	DIO E7	GATE 1

Table 40: DIOCTR1 (DIO7-4 Alternate Functions)

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See sections on “Counter / Timer Operation” on page 99 and “DIO Handshaking Mode” (below) for details on these special functions (available only when DIOCTR1 is set to “1”).

13.9.1 DIO HANDSHAKING OPERATION

Normally, the DIO data is transferred through the data registers with each read. If a handshaking method is desired, two signals are provided to allow this type of transfer:

- DIOLATCH
  - Input to system (low latches all input data; high passes data through directly)
  - Normally pulled-up (passes all DIO data through without handshaking); affected by DIO pull-up’s
  - Falling edge generates IRQ when “DINTE” (Base+13, bit 5) is “1”
  - Present on DIO Header J8, pin 39
  - NOTE : Only accessible when “DIOCTR is set to “1”
- ACK
  - Output from system (driven high when DIOLATCH transitions from high-to-low; ACK is driven low as soon as latched data is read into the system)
  - Present on DIO Header J8, pin 43

The handshaking sequence would look similar to this over the course of one data transaction:

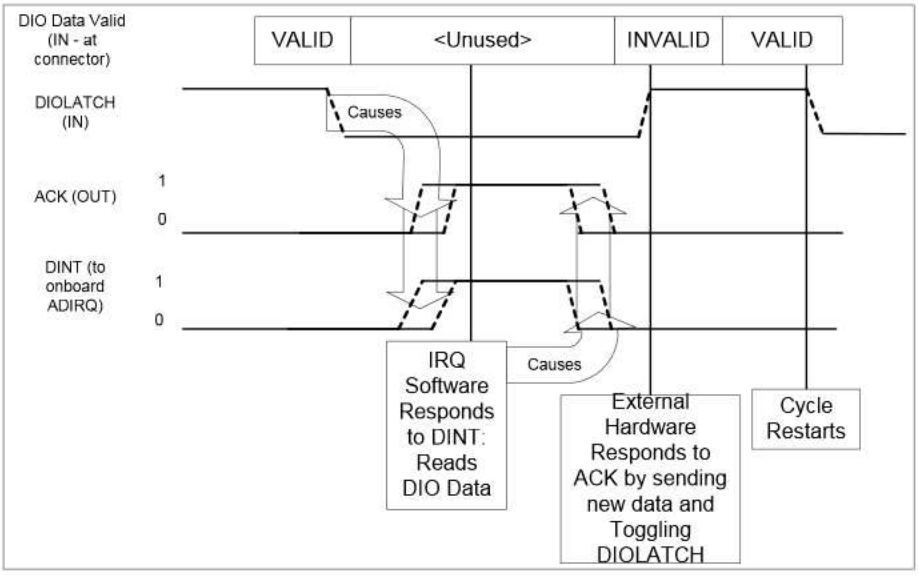


Figure 10 : DIOLATCH / ACK Handshaking Diagram

13.9.2 DIO PULL-UP/DOWN SETTINGS

All DIO signals have some basic ESD and over/under-voltage protection. In addition, all signals can be configured with pull-up or pull-down resistors to set a given I/O voltage when no input signal is provided. This pull-up/pull-down setting should always be made for two reasons:

1. Prevents floating inputs (latch-up from floating input where CMOS I/O pins are involved)
2. Sets a known voltage level for inputs that are not driven

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This is particularly useful for signals such as the DIOLATCH and EXTTRIG signals, for example, where a floating input could cause erratic or erroneous results (latch/counter edge trigger could occur randomly).

To set DIO signal pull-ups or pull-downs, a jumper must be added across signals on header J5, as indicated here:

DIO Signal (Range)	Pull-up	Pull-down	Notes
A7-0, B7-0, C7-0, D7-0, E3-0	1-3	3-5	PWM Outputs are included here
E7-4 (GATE0, TOUT1, GATE1, DIOLATCH)	2-4	4-6	Affects DIO Hanshaking and GATE for both Counters

Table 41: DIO Pull-Up/Down Configuration

Note that:

- "Pull-up" means that a weak (47kOhm) pull-up resistor will be connected between the DIO signal and +3.3V. This sets the DIO signal to a "1" value when there is no external source driving the signal.
- "Pull-down" means that a weak (47kOhm) pull-down resistor will be connected between the DIO signal and ground. . This sets the DIO signal to a "0" value when there is no external source driving the signal.
- FPGA programming / updates: These Pull-up/down resistors also affect signal outputs during the period when the FPGA is being loaded or re-loaded. During an FPGA update, the FPGA will briefly tri-state all signals – during this period, the pull-up/down resistors will be the only current source coming from the board through the DIO signals.

So, for example, to set all standard DIO signals to "0" by default and to allow DIO handshaking to be configured such that the DIOLATCH signal is pulled high (for normal handshaking operation default), a jumper would be placed across J5 pins 3-5 (sets normal DIO's to "0" when not driven) and across J5 pins 2-4 (sets DIO E7-E4 to "1" when not driven, including "DIOLATCH" which is present on DIO E6 pin).

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14. COUNTER/TIMER OPERATION

Hercules-EBX models with Data Acquisition contain two counter/timers that provide various timing functions on the board for A/D timing and user functions. These counters are controlled with registers in the on-board data acquisition controller FPGA. See pages 67 and 70 for information on the counter/timer control register bits and how to perform various functions using these counters.

14.1 Counter 0 – A/D Sample Control

The first counter, Counter 0, is a 24-bit "divide-by-n" counter used for controlling A/D sampling. The counter has an internal clock input, an external gate input ("Gate 0" – alternate function for DIO Channel E bit 4), and a dedicated output ("TOUT 0"). The input is a 10MHz or 100 kHz clock provided on the board and selected with bit CKFRQ0 in Page 0 Base + 12 bit 0. The gate is an optional signal that can be input on pin 40 of the I/O header J8 when DIOCTR1 (Page 0: Base + 12 bit 5) is 1. If this signal is not used, then the counter runs freely. The "TOUT 0" signal output is a positive pulse whose frequency is equal to the input clock divided by the 24-bit divisor programmed into the counter. The output is always present on pin 42 of the I/O header J8.

The counter operates by counting down from the programmed divisor value. When it reaches zero, it outputs a positive-going pulse equal to one input clock period (100ns or 10µs, depending on the input clock selected by CKFRQ0). It then reloads to the initial load value and repeats the process indefinitely.

The output frequency can range from 5MHz (10MHz clock, divisor = 2) down to 0.006Hz (100 kHz clock divided by 16,777,215, or 2^{24}-1). The output is fed into the A/D timing circuit and can be selected to trigger A/D conversions when AINTE is 1 and CLKSEL is 0 in Base + 13 (bit 1). Using the control registers at Page 0 : Base + 13 and Base + 27, the counter can be loaded, cleared, enabled, and disabled, the optional gate can be enabled and disabled, and the counter value can be latched for reading.

14.2 Counter 1 – Counting/Totalizing Functions

The second counter, Counter 1, is similar to Counter 0 except it is a 16-bit counter. It also has an internal clock input, as well as an external input ("EXTTRIG"), an external gate ("GATE 1"), and an output ("TOUT1"). The gate and output signals are present on the I/O header only when DIOCTR=0. The input may come from either the external trigger signal or the on-board clock generator. When the on-board clock generator is used, the clock frequency is either 10MHz or 100 KHz as determined by control bit CKFRQ1, located at Page 0: Base + 12, bit 1.

The output ("TOUT1") is a positive-going pulse that appears on pin 38 of I/O header J8 (when DIOCTR1 = 1). The output pulse occurs when the counter reaches zero. When the counter reaches zero it will reload and start over on the next clock pulse. The output stays high the entire time the counter is at zero, i.e. from the input pulse that causes the counter to reach zero until the input pulse that causes the counter to reload.

When CLKSRC1=1 (external source), then Counter 1 operates as follows: It counts positive edges of the signal on pin 41 ("EXTTRIG") on the I/O header. The counter can either be free running or gated, as determined by the Gate Enable control bit, "GTEN" (Page 0 : Base +27, bit 4).

The gate signal is provided on pin 37 when DIOCTR1 = 1 (enabling counter functions on I/O header) and GTEN = 1 (enabling gating for this counter). If the gate signal is high then the counter will count, and if it is low the counter will hold its value and ignore input pulses. This pin can have a pull-up so the counter can operate without any external gate signal (See section on DIO pull-up's on page 97).

When DIOCTR1=0, Counter 1 operates as follows: It takes its input from the on-board clock generator based on the value of the CKFRQ1 bit located at Page 0: Base + 12. There is no gating and the counter runs continuously.

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Counter 1 may be used as either a pulse generator or a totalizer/counter. In pulse generator mode the output signal on pin 26 is of interest. In totalizer/counter mode the counter value is of interest and may be read by first latching the value and then reading it.

14.3 Command Sequences

Diamond Systems provides driver software to control the counter/timers on Hercules-EBX. The information here is intended as a guide for programmers writing their own code in place of the driver and also to give a better understanding of the counter/timer operation.

The counter control register is shown below for reference (from PAGE 0).

Base + 27 Write Counter/Timer Control Register

Bit No.	7	6	5	4	3	2	1	0
Name	CTR	LATCH	GTDIS	GTEN	CTDIS	CTEN	LOAD	CLR

To make a counter run (load and enable a counter)

1. Load the desired initial value into the counter.
2. If you want to use the gate function, enable the gate.
3. Enable the counter.

To read a counter

1. Latch the counter. The counter continues to operate.
2. Read the value from the data registers.

A counter may be enabled or disabled at any time. If disabled, the counter will ignore incoming clock edges.

The gating may be enabled or disabled at any time. When gating is disabled, the counter will count all incoming edges. When gating is enabled, if the gate is high the counter will count all incoming edges, and if the gate is low the counter will ignore incoming clock edges.

Loading and enabling a counter

For counter 0, three bytes are required to load a 24-bit value. For counter 1, two bytes are needed for a 16-bit value. The value is an unsigned integer.

a. Write the data to the counter:

Break the load value into 3 bytes, low, middle, and high (two bytes for counter 1). Then write the bytes to the data registers in any sequence.

Counter 0
```
outp(base+24,low);
outp(base+25,middle);
outp(base+26,high);
```

Counter 1
```
outp(base+24,low);
outp(base+25,high);
```

b. Load the counter:

Counter 0
```
outp(base+27,0x02);
```

Counter 1
```
outp(base+27,0x82);
```

c. Enable the gate if desired:

Counter 0
```
outp(base+27,0x10);
```

Counter 1
```
outp(base+27,0x90);
```

d. Enable the counter:

Counter 0
```
outp(base+27,0x04);
```

Counter 1
```
outp(base+27,0x84);
```


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Reading a counter

a. Latch the counter:

Counter 0	Counter 1
outp(base+27,0x40);	outp(base+27,0xC0);

b. Read the data:

The value is returned in 3 bytes, low, middle, and high (2 bytes for counter 1)

Counter 0	Counter 1

low=inp(base+24);
middle=inp(base+25);
high=inp(base+25);
	low=inp(base+24);
	high=inp(base+25);

c. Assemble the bytes into the complete counter value:

Counter 0	Counter 1
val = high * 2^16 + middle * 2^8 + low;	val = high * 2^8 + low;

Enabling the counter gate

Counter 0	Counter 1
outp(base+27,0x10);	outp(base+27,0x90);

The counter will run only when the gate input is high.

Disabling the counter gate

Counter 0	Counter 1
outp(base+27,0x20);	outp(base+27,0xA0);

The counter will run continuously.

Clearing a counter

Clearing a counter is done when you want to restart an operation. Normally you only clear a counter after you have stopped (disabled) and read the counter. If you clear a counter while it is still enabled, it will continue to count incoming pulses, so its value may not stay at zero.

a. Stop (disable) the counter:

Counter 0	Counter 1
outp(base+27,0x08);	outp(base+27,0x88);

b. Read the data (optional). See “Reading a counter” above.

c. Clear the counter:

Counter 0	Counter 1
outp(base+27,0x01);	outp(base+27,0x81);

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15. PULSE-WIDTH MODULATION OPERATION

Hercules-EBX models that include Data Acquisition contain four PWM generators for automatic generation of a regular pulse with independently-configurable duty cycle and frequency. These output signals are present on DIO Header J8 pins 33-36 (PWM output channel 0-3) when DIOCTR0 = 1.

Each PWM consists of two 24-bit down counters, CT0 and CT1. CT0 controls the frequency, and CT1 controls the duty cycle, or length of the active pulse. Each counter is initially loaded with the desired data, and desired clock frequencies are selected for each counter. CLK1 and CLK0 select 10MHz (0) or 100 KHz (1) for the clock source for their respective counters.

Each counter contains a 24-bit load register. The load registers are accessed by writing to Page 1 base + 24 to base + 26 followed by a load command (base + 27 bit 7 = 0 indicates a PWM command) and may be written to at any time. When ENAB = 0, each counter is loaded from the load register via the load command. When ENAB = 1, each counter is loaded from its load register on the next clock after CT0 = 0.

When ENAB=1, both counters count down at the same time. While CT1 is running, the PWM output is equal to the polarity selected by POL: 1 = the output is high during the active period when CT1 is counting down, and 0 = the output is low during the active period. This causes the output pulse to occur at the start of the cycle.

After CT1 reaches 0, it stops counting, and the output switches to the opposite inactive polarity on the next clock. CT0 runs continuously. When it is 0, on the next clock, both counters will reload from their load registers, and the cycle will repeat.

CT0 and CT1 may be reloaded while the PWM is running. The reload data is held in a separate load register for each counter and is not loaded into the counter until CT0 = 0. This allows the current cycle to complete without distortion. Note that this implies that a long PWM cycle duration for the current cycle may cause a considerable update delay before the new settings are seen on the PWM outputs: if the current PWM cycle period is several seconds in duration and the PWM data is updated near the beginning of a cycle, then the output will not be updated with the new settings until several seconds later.

ENAB controls the operation of the PWM. ENAB = 1 causes the PWM to run, and ENAB = 0 disables the PWM circuit. In the disabled state the PWM retains its current state but does not count input clocks, and the output is set to the inactive state as determined by POL.

OUTEN controls the output signal. If OUTEN = 1 then the output is active, and if OUTEN = 0, the output is equal to the inactive state determined by POL. When POL = 0, the inactive state is 0, and when POL = 1 the inactive state is 1. The truth table is as follows:

CT1 output	POL	OUTEN	Output pin	Comments
0	0	0	1	Active low, active, disabled
0	0	1	0	Active low, active, enabled
0	1	0	0	Active high, inactive, disabled
0	1	1	0	Active high, inactive, enabled
1	0	0	1	Active low, inactive, disabled
1	0	1	1	Active low, inactive, enabled
1	1	0	0	Active high, active, disabled
1	1	1	1	Active high, active, enabled

Table 42: PWM Control Signal Truth Table

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15.1 Pulse-Width Modulation Example

The following is a programming example to output a 1KHz signal with a 25% high duty cycle on PWM output 2:

a) Note that, for 1KHz output, either reference clock (10MHz or 100KHz) is suitable. For this example we are going to use the 10MHz reference clock.

b) The first step is to determine the value for the output frequency counter (counter 0)

Counter 0 Value = Reference Clock / Desired Rate

Counter 0 Value = 10MHz / 1Khz

Counter 0 Value = 10000

c) The next step is to determine the value for the duty cycle counter (counter 1).

Counter 1 Value = Timer 0 Value * Duty Cycle

Counter 1 value = 10000 * 0.25

Counter 1 value = 2500

d) Program the two counters:

outp(base + 0, 1); //Set page 1 (for PWM functions)

c0 = Counter 0 Value = 10000

outp(base + 24, (c0 >> 0) & 0xFF); //Counter 0 bits 0-7

outp(base + 25, (c0 >> 8) & 0xFF); //Counter 0 bits 8-15

outp(base + 26, (c0 >> 16) & 0xFF); //Counter 0 bitrs 16-23

outp(base + 27, 0x20); //This loads the value into counter 0 for PWM circuit 2

c1 = Counter 1 Value = 2500

outp(base + 24, (c1 >> 0) & 0xFF); //Counter 1 bits 0-7

outp(base + 25, (c1 >> 8) & 0xFF); //Counter 1 bits 8-15

outp(base + 26, (c1 >> 16) & 0xFF); //Counter 1 bitrs 16-23

outp(base + 27, 0x21); //This loads the value into counter 1 for PWM circuit 2

e) Configure and enable PWM output 2. These are the desired configuration values for base+27:

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BIT7 = 1;	Indicates PWM configuration byte
PWM0-1 = 2;	Program PWM output 2
CLK = 0;	Use the 10MHz reference clock
POL = 1;	Active state = high (PWM will be high for the 25% duty cycle)
OUTEN = 1;	Enable PWM output
ENAB = 1;	Enable PWM circuit

From these settings we get a configuration byte of 0xA7 (see page 73 for register description.)

```
outp(base + 0, 1); //Set page 1 (for PWM functions)
outp(base + 27, 0xA7); //Configure and enable PWM output 2
```

f) Finally, to enable PWM outputs (replacing Digital I/O Port E, bit3-0 : see page 96), set DIOCTR0 = 1, leaving the rest of the Configuration Register as-is:

```
Data = inp(base + 12);  // Read current Configuration Register settings
Data = Data || 0x10;    // Set DIOCTR0 = 1, forcing PWM3-0 onto DIO
outp(base + 12, Data);  // Write settings back to Configuration Register
```

At this point, a 1KHz signal with a 25% high duty cycle will be present on PWM output 2 (J8 – pin 35).

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16. WATCHDOG TIMER PROGRAMMING

16.1 Example : Watchdog Timer With Software Trigger

Software trigger relies on a thread of execution to constantly trigger watchdog timer A. If the thread is ever halted, timer A will reach zero and start timer B. Once timer B reaches 0, the board will reset.

In this example we will set the watchdog timer to a countdown period of 4 seconds. Note that longer timeout periods should typically be used when relying on software-based triggers for the Watchdog Timer in order to accommodate varying software latencies (Interrupt latencies, other tasks with priority at certain times, etc)

Setting up the watchdog timer:

```
outp(base + 0, 0x00);                    //set page 0
outp(base + 28, 40000 & 0xFF);           //set LSB of WD timer A (4 seconds)
outp(base + 29, (40000 >> 8) & 0xFF);    //set MSB of WD timer A
outp(base + 30, 0xFF);          //set WD timer B to 0.0255 seconds
outp(base + 31, 0x28);                   //set WDEN=1, WDRST=1 (enable WD timer, reset)
```

The timer is now setup and active. A separate thread should now be constantly running this code:

```
while (1)
{
  outp(base + 31, 0x80);         //trigger watchdog timer
  sleep(1000);                   //sleep one second
}
```

If this thread is interrupted or if the parent process crashes, then the board will reset 4 seconds after the last trigger is received.

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16.2 Example : Watchdog Timer With Hardware Trigger

Hardware trigger relies on an external pulse to constantly trigger watchdog timer A. If the external stream of pulses is ever halted, timer A will reach zero and start timer B. Once timer B reaches 0, the board will reset.

In this example, we will make use of the "T-1" feature of timer A to automatically reset itself unless a physical connection is broken. The physical connection must be made between WDO and WDI on the data acquisition header J9.

Since software is not involved in maintaining the timer, we do can set the reset period to a much smaller value. In this example, the reset pulse will travel across the physical connection every 10 milliseconds.

```
outp(base + 0, 0x00);                  //set page 0
outp(base + 28, 100 & 0xFF);           //set LSB of WD timer A (10 milliseconds)
outp(base + 29, 100 >> 8) & 0xFF);     //set MSB of WD timer A
outp(base + 30, 0xFF);                 //set WD timer B to 0.0255 seconds
outp(base + 31, 0x2D);                 //set WDEN=1, WDRST=1, WDT-1=1, WDIEN=1
```

Now when timer A reaches 1, a rising edge will flow from WDO to WDI, resetting the timer back to 100 and lowering WDO. When the connection from WDO to WDI is severed, the rising edge will never reach WDI and system will reset.

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17. DATA ACQUISITION SPECIFICATIONS

These specifications apply to units with Data Acquisition Only

Analog Inputs

No. of inputs	16 differential or 32 single-ended (user selectable)
A/D resolution	16 bits (1/65,536 of full scale)
Input ranges	Bipolar: ±10V, ±5V, ±2.5V, ±1.25V Unipolar: 0-10V, 0-5V, 0-2.5V
Input bias current	50nA max
Maximum input voltage	±10V for linear operation
Overvoltage protection	±35V on any analog input without damage
Nonlinearity	±3LSB, no missing codes
Drift	5PPM/°C typical
Conversion rate	250,000 samples per second max
Conversion trigger	software trigger, internal pacer clock, or external TTL signal
FIFO	48 samples; programmable interrupt threshold

Analog Outputs

No. of outputs	4
D/A resolution	12 bits (1/4096 of full scale)
Output ranges	Unipolar: 0-10V or user-programmable Bipolar: ±10V or user-programmable
Output current	±5mA max per channel
Settling time	4µS max to ±1/2 LSB
Relative accuracy	±1 LSB
Nonlinearity	±1 LSB, monotonic

Digital I/O

No. of lines	40 (32 dedicated DIO plus two configurable nibbles, 4-bits each)
Compatibility	3.3V and 5V logic compatible
Input voltage	Logic 0: -0.5V min, 0.8V max; Logic 1: 2.0V min, 5.5V max
Input current	±1µA max
Output voltage	Logic 0: 0.0V min, 0.4V max; Logic 1: 2.4V min, 3.3V max
Output current	Logic 0: 12mA max; Logic 1: -8mA max
I/O capacitance	10pF max

Counter/Timers

A/D pacer clock	24-bit down counter with optional external gate
Pacer clock source	10MHz, 100 kHz, or external signal
General purpose	16-bit down counter with optional external gate
GP clock source	10MHz, 100 KHz, or external signal

General

Power supply	+5VDC ±5%
Current consumption	0.7A – 1.1A typical
Operating temperature	-40 to +85°C
Operating humidity	5% to 95% noncondensing

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18. FLASHDISK MODULE

Hercules-EBX is designed to accommodate an optional flashdisk module. This module contains 32MB to 128MB of solid state non-volatile memory that operates like an IDE drive without requiring any additional driver software support.

Model	Capacity
FD-32	32MB
FD-64	64MB
FD-96	96MB
FD-128	128MB



18.1 Installing the Flashdisk Module

The flashdisk module installs directly on the IDE connector J16 and is held down with a spacer and two screws onto a mounting hole on the board.

The flashdisk module contains a jumper for master/slave configuration. For master, install the jumper over pins 1&2, and for slave install the jumper over pins 2&3.

18.2 Configuration

To configure the CPU to work with the Flashdisk module, enter the BIOS (press F2 during startup). Select the Main menu, and then select IDE Primary Master. Enter the following settings:

Type:	User
Cylinders:	489 for 32MB flashdisk
Heads:	4 for 32MB flashdisk
Sectors:	32 for 32MB flashdisk
Multi Sector Transfer:	Disable
LBA Mode Control:	Enable
32 Bit I/O:	Disable
Transfer Mode:	Fast PIO 1
Ultra DMA Mode:	Disable

Exit the BIOS and save your change. The system will now boot and recognize the FlashDisk module as drive C:.

18.3 Using the Flashdisk with Another IDE Drive

Since the flashdisk occupies the board's IDE connector, mounting it on the board prevents the simultaneous use of another IDE drive with the same IDE port. To utilize both the flashdisk and another drive, an adapter board, such as Diamond Systems' ACC-IDEEXT, and cables are required. The ACC-IDEEXT adapter board is described on page 116.

18.4 Power Supply

The 44-pin cable carries power from the CPU to the adapter board and will power the flashdisk module and any drive using a 44-pin connector, such as a notebook hard drive.

A drive utilizing a 40-pin connector, such as a CD-ROM or full-size hard drive, requires an external power source through an additional cable. The power may be provided from the CPU's power out connector (J12) or from one of the two 4-pin headers on the ACC-IDEEXT board. Diamond Systems' cable no. **698006** may be used with either power connector to bring power to the drive.

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19. "UTILITY" BOARD

A small "Utility" board (DSC# **861002**) has been designed for test and development with the Hercules-EBX. It is included with the Hercules-EBX development system (DSC# **DK-HRCEBX-01**). This small board plugs onto the "Utility" connector J7and provides a simple interface for various buttons / LED's:

- Power Button – simple push-button for "Power Button" functionality
- Reset Button – push button causes systemwide hardware reset
- Power LED – lights when main system power is active (note that stand-by power may still be active when this LED is off)
- Ethernet : 100MBit link LED – lights up when 100Mbit link is achieved (will not be illuminated for 10Mbit link)
- Ethernet : Activity LED – pulses with Ethernet activity (reads or writes)
- IDE Activity LED : Lights when any access is made through the two onboard IDE connectors (reflects activity of up to 4 devices potentially active through the two IDE connectors)
- Speaker – this speaker is a typical PC "Beep" speaker; it is not an output for the onboard sound system at all

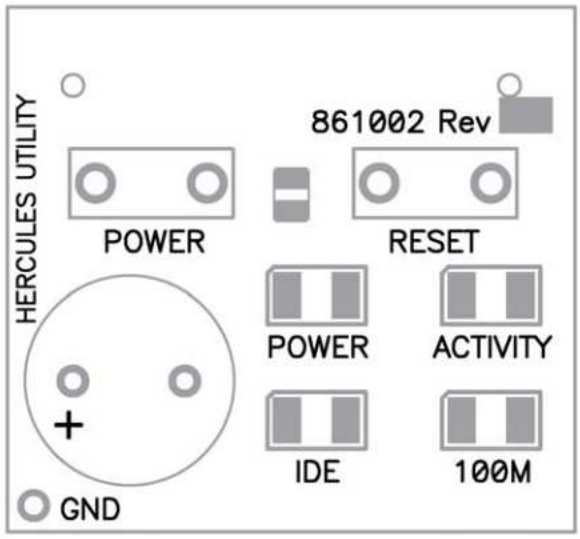


Figure 11 : Utility Board (for J7)

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20. DATA ACQUISITION TEST BOARD

The Data Acquisition Test Board (DSC# **ACC-HRCDAQ**) is provided with the Hercules-EBX development system as a means to do simple tests and verification of the onboard Data Acquisition system (both digital and analog I/O).

The DAQ test board consists of two connectors for ribbon cables (one for digital I/O, the other for analog I/O), A sequence of LEDs (for visual display of one byte of DIO loopback), a bank of DIP switches, and 3 sets of test points.

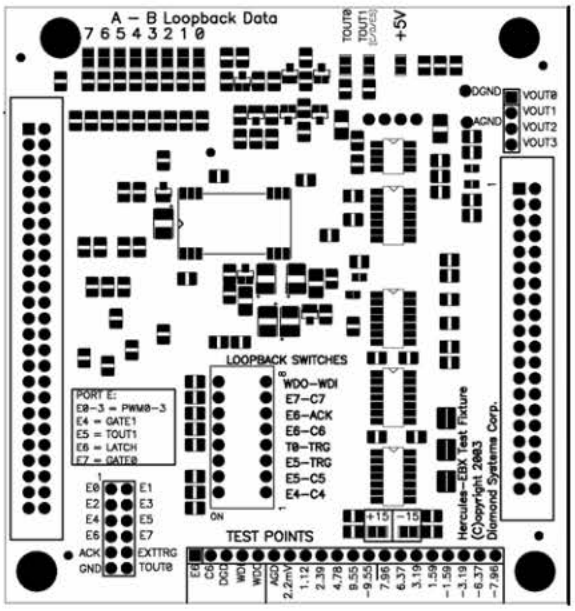


Figure 12 : Data Acquisition (DAQ) Test Board

20.1 Connecting the DAQ Test Board

The DAQ Test board is powered from the ribbon cables and contains sensitive analog amplifiers wired to these cables. As such, the board should only be connected or disconnected while the Hercules-EBX power is "OFF" (standby power is OK – main power, as indicated by the "ON" LED on the main board, should be off).

- One 50-pin ribbon cable (DSC part # **C-50-18**) should be connected from the Hercules-EBX board connector J8 to the DAQ test board J3. Note the pin "1" designations on both boards – ensure that the ribbon cable is connected such that the red pin-1 designation on the ribbon cable is oriented next to the "1" on the board silk screen for each board.
- One 40-pin ribbon cable (DSC part # **C-40-18**) should be connected from the Hercules-EBX board connector J9 to the DAQ test board J2. Note the pin "1" designations on both boards – ensure that the ribbon cable is connected such that the red pin-1 designation on the ribbon cable is oriented next to the "1" on the board silk screen for each board.
- Before using the board, make certain that all DIP switches (SW1 bank) are not conflicting – the best way to ensure this is to set all DIP switches to the "OFF" position.
- Apply power to the main board (press "Power Button" on utility board if main board has been powered off using the on-board power control) and watch for the "+5", "+15", and "-15" LEDs to become active.
- At this point, the board should be ready-to use.

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20.2 DAQ Board DIO interface

The Data Acquisition Test Board provides a complete loopback capability for each DIO bit: each DIO signal can potentially be driven and read back by at least one other DIO channel. The details of this loopback are user-configurable for many DIO bits – see details below.

20.2.1 DIO A – DIO B LOOPBACK

DIO channel A (bits 7-0) are looped back to DIO channel B (bits 7-0). There is one special case for this loopback: bit 0 also goes to "EXTTRIG".

In general, this loopback requires that one port be set up as an output and the other port should be set as an input (on the Hercules-EBX, via software). While there is some protection for the case of both set as outputs, this should not be done and serves no useful purpose in testing.

This loopback is connected to a bank of 8 LED's on the test board. A given LED will be active when the associated data bit is low. For example, if DIO channel A is set as an output and DIO channel B is set as an input then a value of "0xFE" written to the DIO Channel A output register would result in "0xFE" in the channel B input register and would result in one LED (bit 0) being "ON" while the rest of the DIO loopback LED's would be off.

To perform DIO loopback tests, ensure that one of the channels is set as an output and the other channel is set as an input. Any data written to the output channel should be read back on the input channel.

20.2.2 DIO C – DIO D – DIOE LOOPBACK

DIO channel C (bits 7-0) is looped back to DIO channel D (bits 7-0) and DIO channel E (bits 7-0) (through some switches for bits 7-4). For basic loopback testing, switch bank SW1 would be set such that:

- Switch 1 is ON (E bit 4 connected to C bit 4 and D bit 4)
- Switch 2 is ON (E bit 5 connected to C bit 5 and D bit 5)
- Switch 3 is ON (E bit 6 connected to C bit 6 and D bit 6)
- Switch 4 is OFF (E bit 6 NOT connected to ACK output)
- Switch 5 is ON (E bit 7 connected to C bit 7 and D bit 7)

(NOTE: Switch 6 does not affect DIO loopback – it is for watchdog timer functions)

To perform DIO loopback tests, ensure that one of the three channels is set as an output and the other two channels are set as inputs. Any data written to the output channel should be read back on the two input channels.

There are several special cases for Channel E testing:

- Channel E, bits 3-0 can also be used for the Pulse-Width Modulation output function. In this case, channels C and D would both need to be configured as inputs to avoid out-output contention. These PWM waveforms can be readily sampled via DIO Channel C 3-0 or DIO Channel D 3-0, or they can be manually measured at pins 1-4 on testpoint connector TP1.
- Channel E, bit 4 can also be used for the "GATE1" function. It can be connected to DIO Channel C and D bit 4 by selecting SW1 – switch 1 to the "ON" position. In this configuration, it is directly wired for DIO loop back to Channel C bit 4 and Channel D bit 4.

  To test "GATE1" functionality, one of the other sources must be set as an output to assert the required signal or SW1 – switch 1 can be set to the "OFF" position and an

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appropriate signal can be driven into test point TP1 – pin 4. This test point can be used for "GATE1" probing and assertion.

- Channel E, bit 5 is wired to an LED on-board, as well as to SW1 – switch 2. To loopback DIO E bit 5 to DIO C/D bit 5, set SW1-switch 2 to the "ON" position. To test "TOUT1" functionality for DIO E – bit 5, either set both DIO D and C to input or set SW1 – switch 2 to the "OFF" position. DIO E bit 5 can be manually measured at TP1 – pin 6.
- Channel E, bit 6 (which is also used for "LATCH" signal functionality) can be independently connected to DIO channel C / D bit 6 (for DIO loopback testing) or the "ACK" output signal (for "LATCH" functional testing). Test point TP1 – pin 7 can be used for "DIO E bit 6 / LATCH" probing and assertion.
    i. For loopback testing, SW1 – switch 3 should be set "ON" and SW1-switch 4 should be set "OFF".
    ii. For LATCH / ACK testing, SW1 – switch 4 should be set "ON" and SW1-switch 3 should be set "OFF".
- Channel E, bit 7 can also be used for the "GATE0" function. It can be connected to DIO Channel C and D bit 4 by selecting SW1 – switch 5 to the "ON" position. In this configuration, it is directly wired for DIO loop back to Channel C bit 7 and Channel D bit 7. Test point TP1 – pin 8 can be used for "GATE0" probing and assertion.

In general, DIO loop back requires that one port be set up as an output and the other two ports should be set as an input. While there is some protection for the case of two or more outputs, this should not be done and serves no useful purpose in testing.

20.2.3 SPECIAL FUNCTIONS

As has been mentioned previously, Channel E can be used for alternative functions for the DIO interface. In addition, there are several dedicated signals for some of these special functions. (See the section 95 for more details).

- GATE 0 – This signal is used to enable the internal counter 0 of the FPGA, when in "gated mode". A high input enables counting and a low input disables counting. This signal is multiplexed with Channel E bit 7, which means that this input is tied directly to Channel D bit 7 and channel C bit 7 when SW1 – switch 5 is "ON". To test this special function input, either one of these DIO channels (C or D) must be set as an output and bit 7 of the output channel must be used to control this gating function.

  Alternatively, an external source can be used. In this case, SW1 – switch 5 should be set to "OFF" and an external gating signal should be driven in to TP1 – pin 8.

- GATE 1 - This signal is used to enable the internal counter 1 of the FPGA, when in "gated mode". A high input enables counting and a low input disables counting. This signal is multiplexed with Channel E bit 4, which means that this input is tied directly to Channel D bit 4 and channel C bit 4 when SW1 – switch 1 is "ON". To test this special function input, either one of these DIO channels (C or D) must be set as an output and bit 4 of the output channel must be used to control this gating function.

  Alternatively, an external source can be used. In this case, SW1 – switch 1 should be set to "OFF" and an external gating signal should be driven in to TP1 – pin 5.

- TOUT0 – This signal is used as a timer out from the FPGA timer 0 control. It is a dedicated output, and is tied to an LED and a test point (TP1 – pin 12) for probing.

- TOUT1 - This signal is used as a timer out from the FPGA timer 1 control. It is multiplexed with Channel E bit 5, and is wired directly to Channel D bit 5 and

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Channel C bit 5 as well as to an LED. If "TOUT1" function is required, then the two attached DIO signals (D bit 5 and C bit 5) must be configured as inputs. "TOUT1" is also tied to a test point (TP1-pin6) for probing.

- DIOLATCH / ACK – The "LATCH" signal is multiplexed with DIO Channel E Bit 6. The output is connected directly to the dedicated "ACK" signal via SW1-switch 4, so DIO feedback can be directly supported for testing. If this is selected, SW1-switch 3 should be set "OFF" to avoid conflicts (DIO C/D bit 6 unintentionally driving DIOLATCH).

- EXTTRIG – This is a dedicated input signal which is used for latching data or as a clock or pulse source for the internal counter 1. This is connected directly to a test point (TP1-pin 10), Channel A bit 0, Channel B bit 0, as well as two switches :

  i. SW1-switch 3 which routes EXTTRIG to DIO E5 / TOUT1

  ii. SW1-switch 4 which routes EXTTRIG to TOUT0

  There are several ways to test EXTTRIG, given these connections:

  i. Use TOUT0 to drive EXTTRIG. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "ON", DIO ports A and B should both be configured as INPUT, and TOUT0 should be configured to generate the desired output.

  ii. Use TOUT1 to drive EXTTRIG. In this case, SW1-switch 3 should be "ON", SW1-switch 4 should be "OFF", DIO ports A and B should both be configured as INPUT, and TOUT1 should be configured to generate the desired output (making sure that DIO Channel E7-4 are configured for alternate functions).

  iii. Use DIO A bit 0 to drive EXTTRIG. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "OFF", DIO port B should both be configured as INPUT, and DIO port A should be configured as OUTPUT. Data written to DIO port A, bit 0 would then control the EXTTRIG function.

  iv. Use DIO B bit 0 to drive EXTTRIG. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "OFF", DIO port A should both be configured as INPUT, and DIO port B should be configured as OUTPUT. Data written to DIO port B, bit 0 would then control the EXTTRIG function.

  v. Use external trigger source. In this case, SW1-switch 3 should be "OFF", SW1-switch 4 should be "OFF", DIO ports A and B should both be configured as INPUT, and DIO port B should be configured as OUTPUT. The external trigger source should be connected via TP1-pin 10.

- Pulse-Width Modulation Output – There are 4 channels of PWM output that can be independently controlled. These four channels are present on Channel E bits 3-0 when the PWM functions are enabled. Frequency and duty cycle can be varied for each channel.

NOTE: Be certain that the DIP switches for the DIOLATCH / ACK handshaking are correctly configured on the DAQ Test Board before beginning any testing of these functions. If a DIO is inadvertently connected to this lookback, anomalous behavior may result. As mentioned above for LATCH / ACK testing, SW1 – switch 4 should be set "ON" and SW1-switch 3 should be set "OFF".

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20.3 DAQ Board Analog Testing

20.3.1 ANALOG OUTPUT CONNECTIONS

There are 4 output channels (VOUT3-0) from the main Hercules board. All of these are capable of full-rail (+/- 10V) output, and are looped back to input channels for testing. These connections are like so:

- VOUT 0 -> VIN9 and VIN 12 (both buffered); Also, is inverted to VIN10
- VOUT 1 -> VIN13
- VOUT 2 -> VIN14
- VOUT 3 -> VIN15

20.3.2 ANALOG INPUT CONNECTIONS

There are 32 single-ended analog input channels (or 16 differential input channels). These channels are configured like so:

- VIN 0 = Ground (0 V)
- VIN 1 = "Vlowref" (2.2mV)
- VIN 2 = "+Vref-L" (1.1161V)
- VIN 3 = (2.39V)
- VIN 4 = "+Vref-H" (4.7768V)
- VIN 5 = "V+" (9.5536V)
- VIN 6 = "V-" (-9.5536V)
- VIN 7 = Ground (0 V)
- VIN 8 = Ground (0 V)
- VIN 9 = VOUT 0 (buffered)
- VIN 10 = -VOUT 0 (buffered)
- VIN 11 = Ground (0 V)
- VIN 12 = VOUT 0 (buffered)
- VIN 13 = VOUT 1
- VIN 14 = VOUT 2
- VIN 15 = VOUT 3
- VIN 16 = Ground (0 V)
- VIN 17 = Ground (0 V)
- VIN 18 = Ground (0 V)
- VIN 19 = Ground (0 V)
- VIN 20 = Ground (0 V)
- VIN 21 = Ground (0 V)
- VIN 22 = Ground (0 V)
- VIN 23 = "V-" (-9.5536V)
- VIN 24 = (7.961V)
- VIN 25 = (6.369V)
- VIN 26 = (3.185V)
- VIN 27 = (1.592V)
- VIN 28 = (-1.592V)
- VIN 29 = (-3.185V)
- VIN 30 = (-6.369V)
- VIN 31 = (-7.961V)

20.3.3 GENERAL DAQ TESTING SUGGESTIONS / COMMENTS

- Differential Bipolar / Unipolar settings: Note the differential pairs in the listing above. Specifically, note that VIN5+ would be connected to +9.5V and VIN5- would be ground; VIN6+ would be -9.5V and VIN6- would be ground. If the A/D inputs are configured for differential mode and all voltages look correct up to VIN6 (i.e., VIN0-3

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look correct, you get a reading of +9.5V for VIN5, but VIN6 is reading 0V), this is a good indication that the inputs are configured for unipolar mode (i.e., negative differential voltage not being reported). Similarly, voltage readings for channels VIN8 and VIN11 would also be incorrect and readings for VIN9, VIN10, VIN12, VIN13, VIN14, and VIN15 may not be correct (depending on whether the output voltage is higher than the associated "low-side" differential voltage for the given input channel).

- Due to the cable length and relative board location, some of the outputs may show more noise / inaccuracy than others. This board is intended as a means to verify basic functionality and connection (including autocalibration features); it is not intended to provide perfect response for signal performance characterization.

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21. FLASH DISK PROGRAMMER BOARD

The Flash Disk Programmer Board accessory model no. **ACC-IDEEXT** may be used for several purposes. Its primary purpose is to enable the simultaneous connection of both a flashdisk module and a standard IDE hard drive or CD-ROM drive to allow file transfers to/from the flashdisk. This operation is normally done at system setup. The board can also be used to enable the simultaneous connection of two drives to the CPU.

J1 connects to the IDE connector on Hercules-EBX with a 44-pin ribbon cable (Diamond Systems' part no. **698004**). Both 40-pin .1" spacing (J4) and 44-pin 2mm spacing (J3) headers are provided for the external hard drive or CD-ROM drive. A dedicated connector (J2) is provided for the flashdisk module. Any two devices may be connected simultaneously using this board with proper master / slave jumper configurations on the devices.

The Flash Disk Programmer Board comes with a 44-wire cable no. (DSC no. **698004**) and a 40-wire cable no. (DSC no. **C-40-18**) for connection to external drives. The flashdisk module is sold separately.

The 44-pin connector (J1, J2, and J3) and mating cable carry power, but the 40-pin connector (J4) and mating cable do not. J5 and J6 on the accessory board may be used to provide power to a 44-pin device attached to the board when the board is attached to a PC via a 40-pin cable. These headers are compatible with the floppy drive power connector on a standard PC internal power cable.

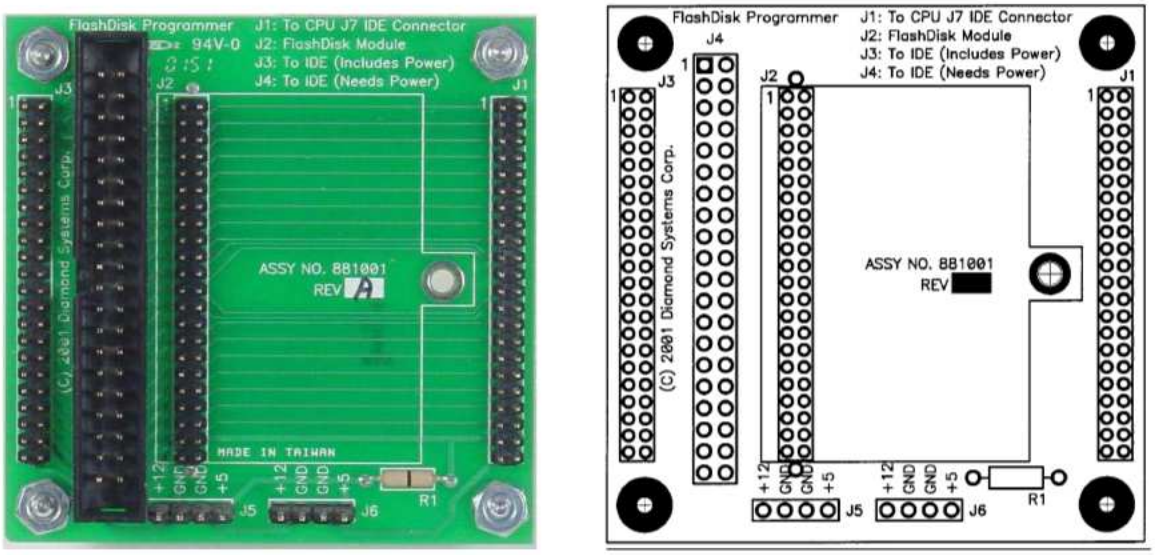


Figure 13 : ACC-IDEEXT *FlashDisk Programmer Board*

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22. I/O CABLES

For custom installations as well as development, Diamond Systems offers a cable kit no. **<DSC# C-HRCEBX-KIT>** with 18 types of cables to connect to all I/O headers on the board. Some cables are also available separately.

The mating cable for each I/O connector is listed in Chapter 4.

NOTE: When the multi-I/O cable (DSC# **C-DB9M-4**) or any other cable is connected to serial ports 1,2,3 or 4, the serial port signals must terminate to another board, or interference problems may occur that will slow down the performance of your CPU.

Photo No.	Cable No.	Description
1	**C-PRZ-02**	(OPTIONAL) 6-wire Ethernet cable with panel-mount RJ-45 connector
2	**698022**	PS/2 Connector for Mouse and Keyboard with PS/2 mini-DIN connectors
3	**698025**	Audio I/O Cable (for line-level and microphone audio)
4	**698017**	TV out cable (S-Video mini-DIN and Composite RCA jack output) NTSC-only
5	**698018**	Amplified audio output (Speaker out), with volume control signals with stripped/tinned leads
6	**698024**	VGA Ribbon cable to VGA Female DB15 for monitor out
7	**C-20-18**	18-inch ribbon cable for "Utility" connections (includes power and reset contacts)
8	**C-40-18**	40-wire data acquisition ribbon cable (Analog I/O)
9	**C-50-18**	50-wire data acquisition ribbon cable (Digital I/O)
10	**C-DB9M-4**	40-pin ribbon cable to 4-serial port male DE-9 connectors
11	**698026**	UDMA/ATA-100 cable for 1 or 2 IDE drives
12	**698004**	44-wire IDE cable for 1 or 2 laptop-style drives
13	**698015**	Standard (low-voltage) input power cable with stripped/tinned leads for connection to external power source
14	**698016**	(OPTIONAL) High-Voltage DC power input cable
15	**698001**	External (3V) Battery power cable
16	**698006**	4-wire output power cable for external drives
17	**698012**	Dual USB cable
18	**861002**	Utility Board (used instead of **C-20-18** for development)

Table 43: Hercules-EBX Cable Kit (DSC#C-HRCEBX-KIT)

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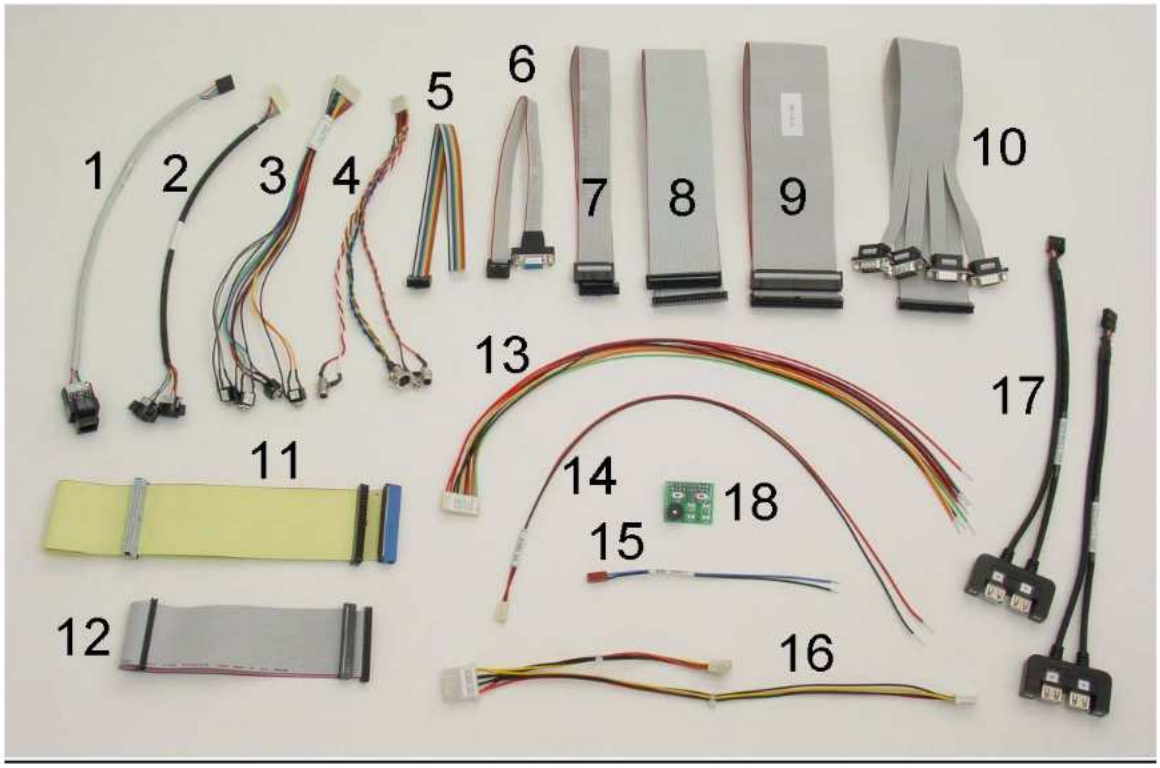


Figure 14 : Hercules-EBX Cable Kit

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23. MOUNTING PC/104(+) CARDS ONTO A HERCULES-EBX BASEBOARD

Hercules-EBX is designed to serve as a baseboard for a stack of PC/104 or PC/104+ boards. Up to 4 PC/104+ boards are supported with the top-most board only supporting slave-mode PCI – no bus mastering supported for that board. Any PC/104 boards should be mounted on top of the PC/104+ board stack, when both board types are to be combined (this should be obvious, given the lack of PC/104+ stack-through connectors on a standard PC/104 board).

PC/104+ requires a board configuration setting for each board in a PC/104+ board stack. Ensure that the lowest board in the stack is assigned to lowest board ID, as per the PC/104+ specification. This setting establishes the PCI Clock, PCI Interrupt routing, the Bus Master signals, and the device ID setting for PCI configuration. Note that these settings are critical – two boards should never be configured with identical board stack settings, as this will cause problems accessing PCI devices, and may cause damage to the main board and/or the PC/104+ boards in the stack. **Do not configure two PC/104+ boards with the same board stack ID!**

PC/104 is much less critical in this regard, but care should be taken to ensure that the ISA resource allocations allow space for the specific boards added in the stack. Resources (IRQ's in particular) can be very limited in a system with so many devices present on the main board. It is important to ensure that ISA I/O, Memory, IRQ, and DMA configuration conflicts are resolved before powering the system up. Otherwise, it is possible that the system boot sequence might be impeded by such conflicts.

Take care to read through this documentation (the section on ISA Resource defaults, in particular) to familiarize yourself with the internal resources used before adding components that might cause conflicts.

When adding boards to the PC/104(+) board stack, be sure to include board standoffs. Inordinate flexing of the main PC/104 and PC/104+ connectors can seriously reduce the effective lifespan of the connectors, as well as causing potential system instability due to incomplete connection across system buses.

24. COMPACT FLASH

There is a Compact Flash connector located on the bottom of the board, under J34. A Compact Flash card placed in this slot will be recognized as an IDE device and will be treated as such. A Compact Flash card can be used as the boot device for a system Note that Compact Flash installation requires that no cable connections be made to J17 – no other IDE devices are supported in this channel when a Compact Flash card is installed (the Primary IDE channel would still be available).

Note that the board is not configured for CompactFlash support by default. To enable CompactFlash, add a jumper to J5 (to enable MASTER support). With this jumper added, any card placed in the CompactFlash slot should be detected as an IDE device upon boot-up. See jumper detail on page 35.

NOTE: Do not add or remove a CompactFlash card while the board is powered-up. Either remove power from the entire system or power the board off before making these changes.

25. CUSTOMIZATION OPTIONS

There are many customer-specific customizations that can be done for the Hercules-EBX, including:

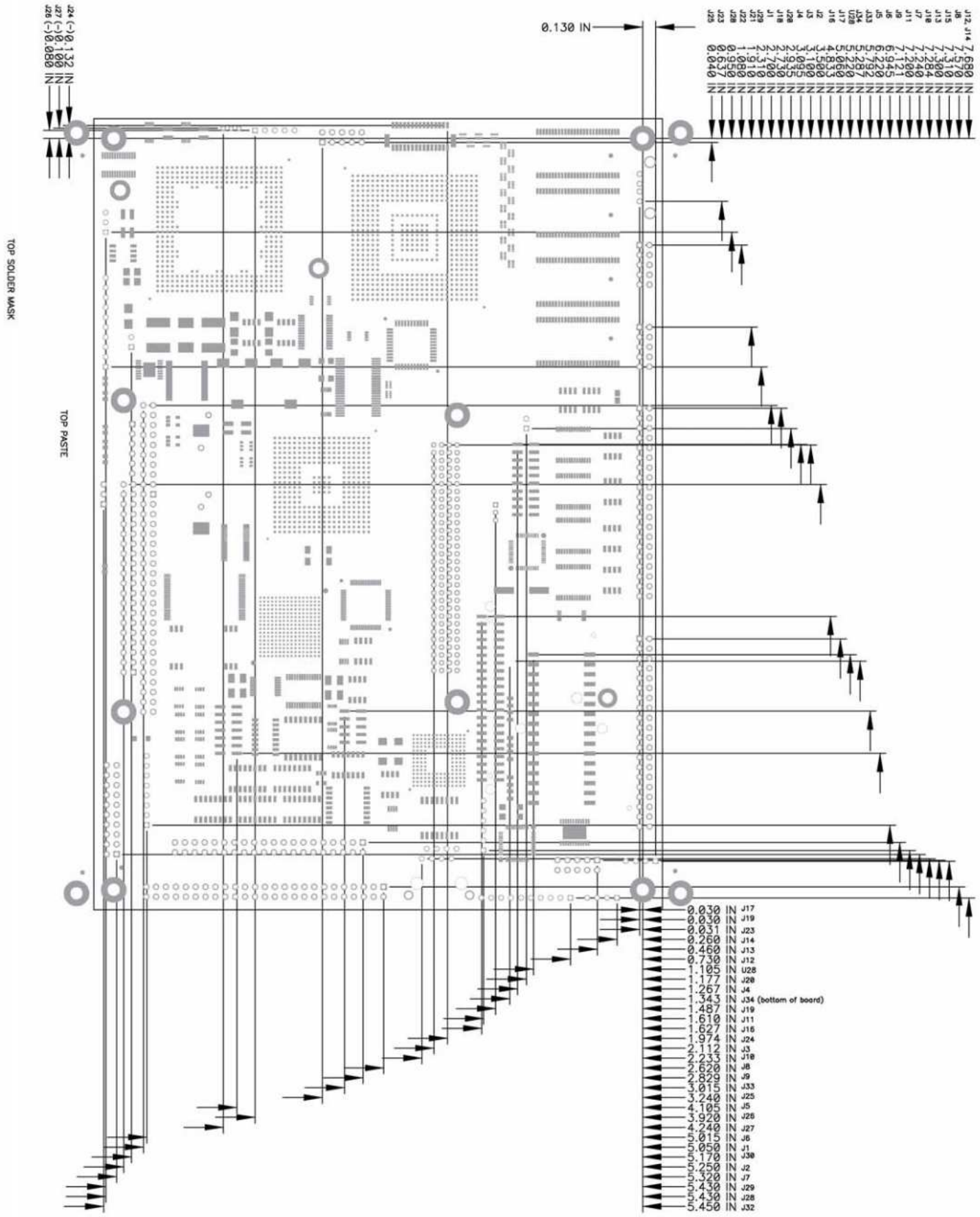
- Latching connectors (replacing the box headers used for most of the board I/O connections)
- Connectors with extra gold contact plating

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- Alternative heatsinks for low air-flow and dusty environments
- Conformal Coating
- Jumperless configuration (all settings made on-board with no jumper headers required)

See your sales representative for details on these special-order options.

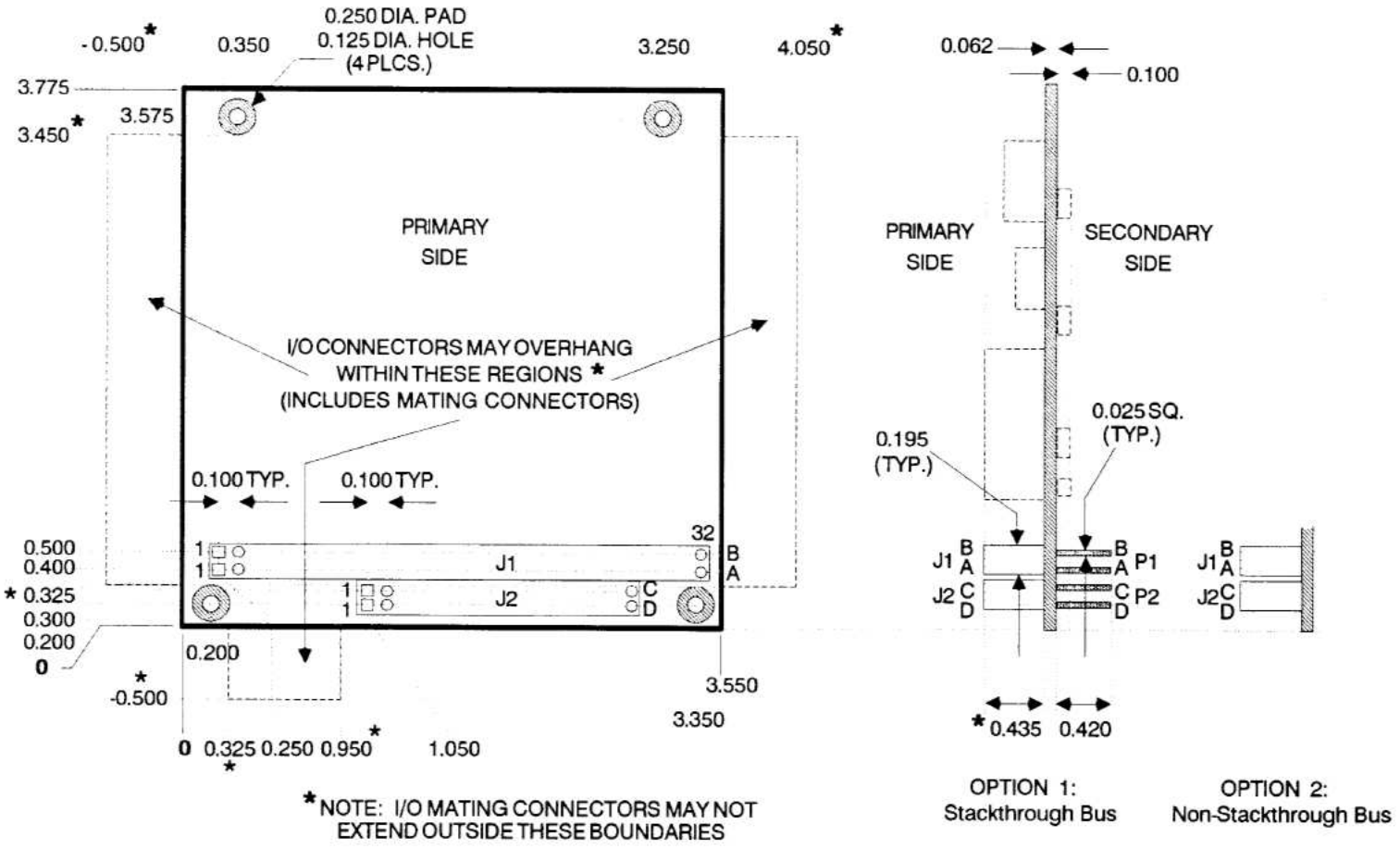
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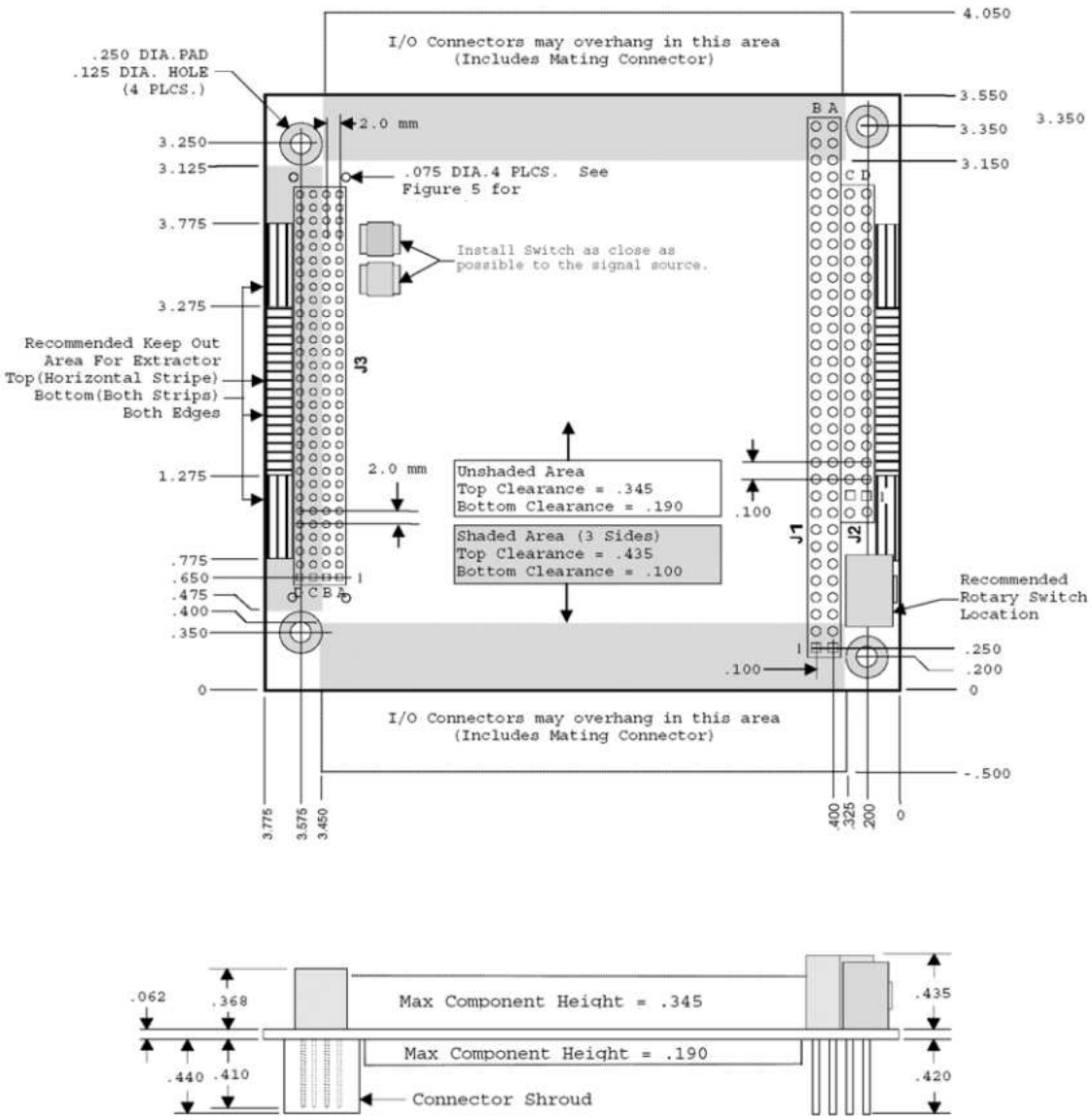
PC/104 Mechanical Drawing

The following drawing is from the PC/104 specification. This document may be downloaded from www.pc104.org or from www.diamondsystems.com/support/techliterature.



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Figure 4: Module Dimensions



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