1. INTRODUCTION

The purpose of this manual is to document the features of the HK68/V20 (tm) (and HK68/V2F and HK68/V2FA) microcomputer boards. Unless stated otherwise, items discussed in this manual apply to all three boards even though only the HK68/V20 may be mentioned.

This manual covers the unique features of the HK68/V20 board. Although general information on the MPU, FPP and MFP is given, details should be obtained from the chip manufacturers data sheets.

1.1 Disclaimer

The information in this manual has been checked and is believed to be accurate and reliable. HOWEVER, NO RESPONSIBILITY IS ASSUMED BY GDCA FOR ITS USE OR FOR ANY INACCURACIES. Specifications are subject to change without notice. GDCA DOES NOT ASSUME ANY LIABILITY ARISING OUT OF USE OR OTHER APPLICATION OF ANY PRODUCT, CIRCUIT OR PROGRAM DESCRIBED HEREIN. This document does not convey any license under patents or the rights of others.

2. HK68/V20 FEATURE SUMMARY

MPU	68020 microprocessor chip; 12.5 Mhz; 32-bit internal architecture, 32-bit address and data paths; 32 address lines; 4 gigabyte addressing range; 256-byte Instruction Cache. (Ref: section 5)
FPP	68881 Floating Point Co-processor. Implements the IEEE-P754 Binary Floating Point Standard. (Ref: section 6)
PMMU	(HK68/V20 only) 68851 chip (or equiv). Provides logical to physical address translation. Demand Paged Virtual Memory operation. (Ref: section 7)
RAM	Four megabyte capacity; One parity bit per byte; Hardware refresh. (Ref: section 9)
EPROM	Two ROM sockets; one socket on the HK68/V2FA. 128 Kbyte total capacity. Page Addressable ROM or EEpROM capability. (Ref: section 9)
VMEbus	32-bit addressing (4 gigabyte range); 32-bit data bus, compatible with 8-bit boards; Seven bus interrupts. (Ref: section 10)
VSB	High speed local memory expansion. Supports secondary bus masters. (Ref: section 10)
Serial I/O	One serial I/O port via the MFP chip; Internal baud rate generator; Asynchronous, synchronous modes; RS-232C interface, RS-422 (optional via external cable). (Ref: section 11.3)
MFP	Mostek MK68901 (or equiv) Multi-Function Peripheral chip; On-card interrupt controller; Four timers; Serial I/O controller; (Ref: section 11)
NV-RAM	Nonvolatile Static RAM; 256 x 4 configuration; Internal EEpROM; 100 year retention; 10,000 store cycle lifetime; For user definable functions. (Ref: section 9.7)
Mailbox	Allows remote control of the HK68/V20 via specified VMEbus addresses; MPU halt, reset, interrupt, and on-card bus lock functions. (Ref: section 10.8)
RTC	Optional Real-Time Clock module for time-of-day maintenance. With battery backup. (Ref: section 12)

3. BLOCK DIAGRAM

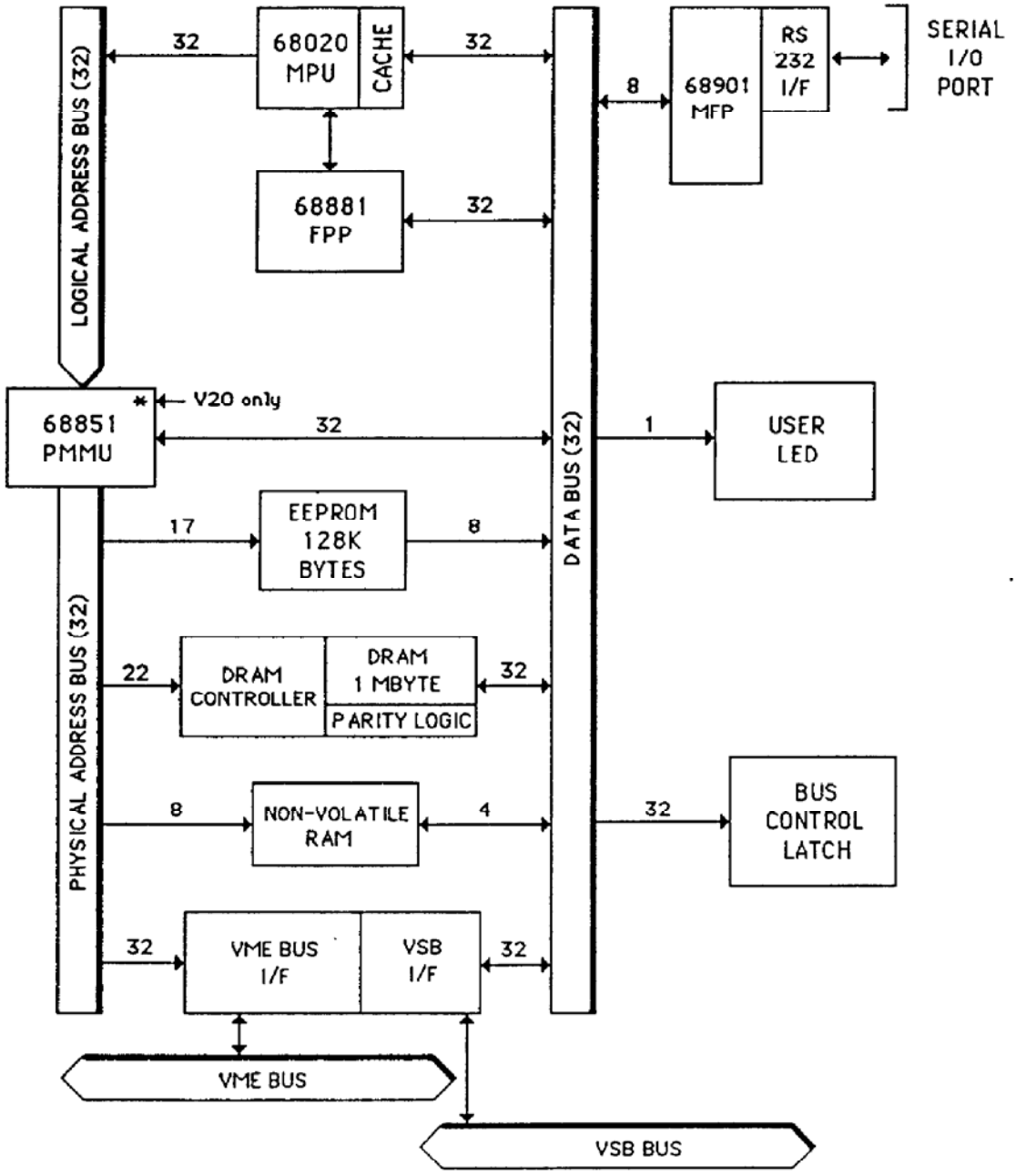

Figure 1. HK68/V20 Block Diagram