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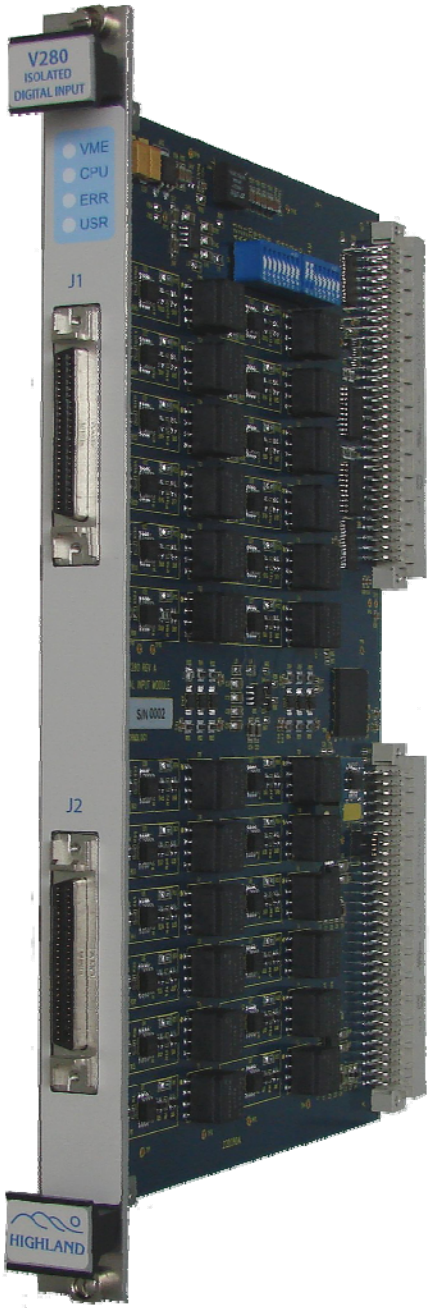
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HIGHLAND TECHNOLOGY



V280
48-CHANNEL VME ISOLATED DIGITAL INPUT MODULE

Technical Manual

March 18, 2015

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Table of Contents

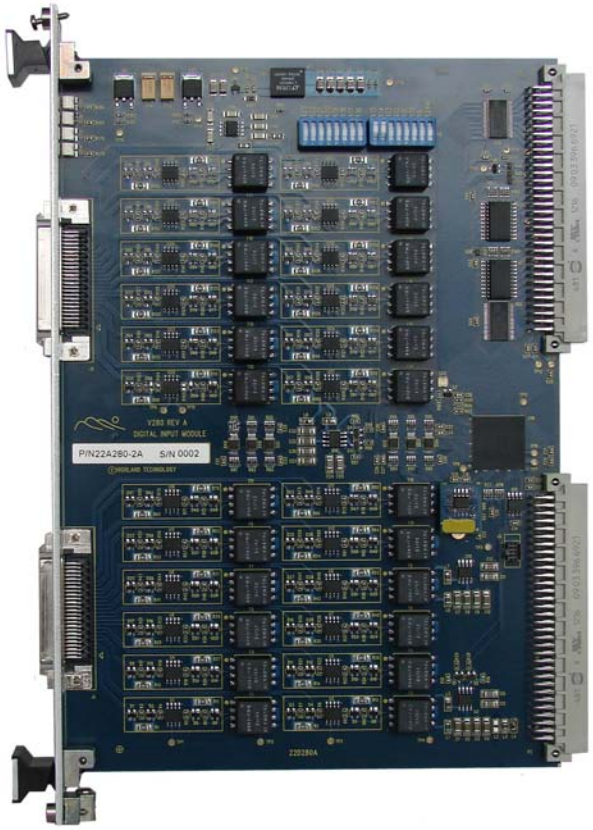
1. Introduction 4
2. Specifications: V280 Digital Input Module 5
3. Overview 6
4. Connectors and Installation 7
   4.1 Address DIP Switches 7
   4.2 Installation 8
   4.3 Input Connectors 9
5. Operation 11
5.1 LEDs 11
   5.2 Powerup Defaults 11
   5.3 Quick Start Procedure 12
6. VME Registers 13
   6.1 VME Register Map 13
   6.2 Detailed Register Descriptions 15
      6.2.1 Module Overhead Registers 15
      6.2.2 ULED - User LED Control 15
      6.2.3 STATE0... STATE2 Input State Registers 16
      6.2.4 RISE and FALL Registers 17
      6.2.5 ERR0...ERR2 Self-test Error Registers 17
      6.2.6 Buffer Registers 18
   6.3 Macros and BIST 18
7. Versions 19
8. Customization 19
9. Hardware and Firmware Revision History 19
   9.1 Hardware Revision History 19
   9.2 Firmware Revision History 19
10. Accessories 20

1. Introduction

This is the manual for the V280, a 48 channel isolated digital input VME module.

Features of the V280 include:

- 48 channels of isolated digital input
- Available in 24V and 5V nominal input versions
- Overvoltage and reverse-voltage protection
- Independently programmable rise and fall time responses for contact debounce or AC inputs
- Glitch-catch capability
- Transparent built-in self-test (BIST)
- Input state readout at full VMEbus speed without handshaking
- Clearly labeled dipswitches set VME address; no jumpers, headers, or trimpots

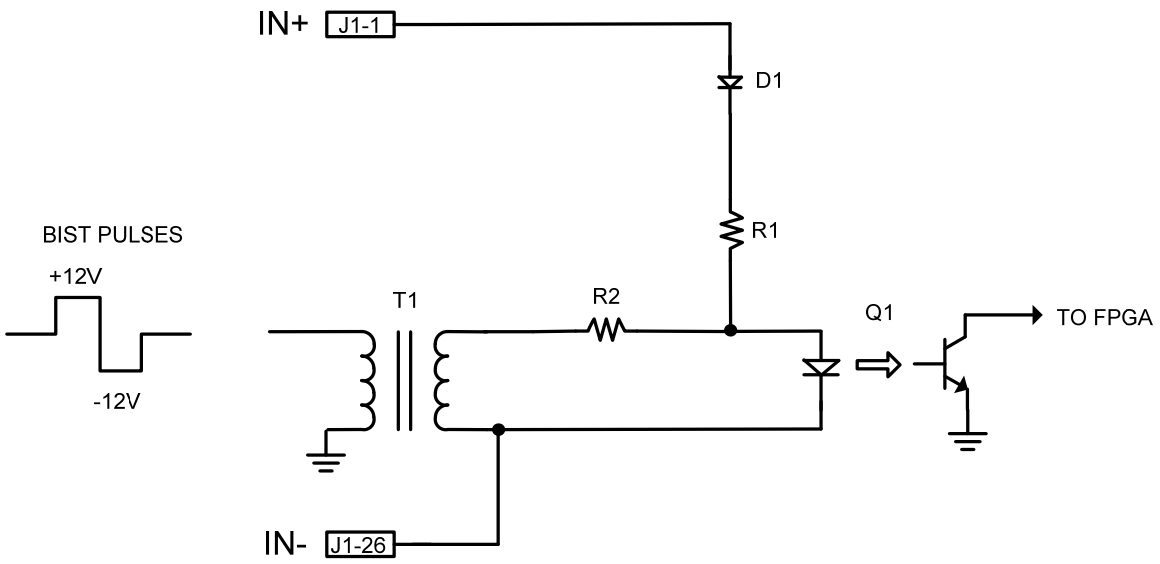


2. Specifications: V280 Isolated Digital Input Module

FUNCTION	48-channel isolated digital input VME module
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16 Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
INPUTS	V280-1 Nom input +5 volts Threshold 2.5 volts typical ± 10 volts operation ± 20 volts max V280-2 Nom input +24 volts Threshold 11 volts typical ± 35 volts operation ± 50 volts max
ISOLATION	± 200 volts continuous
DIGITAL DEBOUNCE	Risetime and falltime programmable in three 16-channel groups, 20 µs to 655 ms with 10 µs resolution
OPERATING TEMPERATURE	0 to 70°C operating -20 to 80°C storage
POWER	VME supplies: + 5 volts, 0.4 amp max + 12 volts, 0.02 amp max - 12 volts, 0.02 amp max
CONNECTORS	P1 VME connector P2 connector for mechanical stability, no D32 VME access J1, J2 50-pin SCSI females, each 24 channels
INDICATORS	LEDs indicate VME access, CPU activity, error conditions; additional LED is user programmable
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec

3. Overview

The V280 provides 48 isolated digital inputs, each with two connector pins. The equivalent circuit of each input channel is:



The normal signal path is from positive input IN+ through D1, R1, optocoupler Q1, and back to IN-. For the V280-1 (5 volt input) version, R1 is about 750 ohms and for the -2 (24 volt input) version, R1 is about 4K ohms. Corresponding input threshold voltages are 2.5 and 11 volts.

Self-test is performed by pulsing transformer T1 with bipolar BIST pulses. A positive BIST pulse makes the optocoupler LED conduct, simulating an active input. A negative test pulse turns the optocoupler off.

The FPGA manages the BIST sequence under control of the MACRO register. The BIST creates a positive 30 µs pulse followed by a negative 30 µs pulse, verifying both optocoupler outputs. Normal data acquisition and debounce filtering is frozen during BIST pulses, so BIST can usually be performed without disturbing normal operation.

4. Connectors and Installation

4.1 Address DIP Switches

The V280 appears as 256 16-bit registers in the VME 16 or 24-bit addressing spaces. The base address of the 256 registers is set by dip switches.

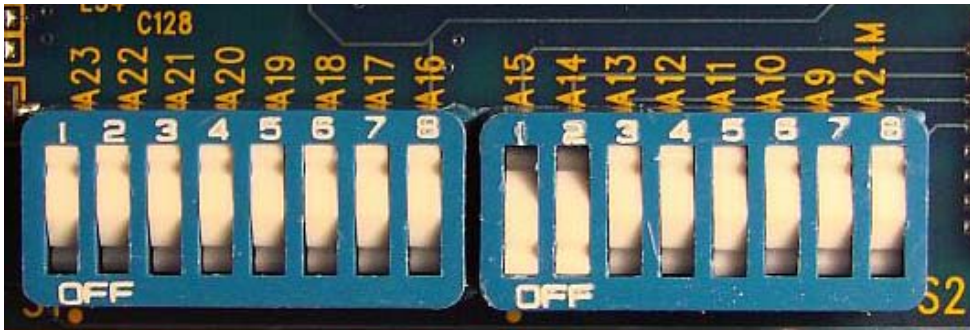
Two rocker-type dipswitches are provided near the top edge of the board. They are labeled, left to right, "A23" through "A9" and finally "A24M".

To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier code 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifier 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space, as shown below.



Address DIP Switch

4.2 Installation

The V280 may be installed in any standard 6U VME crate, including VME64 variants. It supports 16-bit data transfers using the P1 connector. The P2 connector is installed for mechanical reinforcement only; 32-bit data transfers are not supported.

The V280 passes all interrupt and bus grant signals, and may be used with backplane grant jumpers installed or not installed.



CAUTION: Do not install or remove the V280 with crate power on. VME modules are not hot-pluggable. The V280 will be damaged if hot-plugged.



CAUTION: Fully seat the module and secure front-panel screws before applying power.



CAUTION: Handle the V280 with proper ESD precautions to avoid static damage.

4.3 Input Connectors

Two front-panel female 50-pin SCSI connectors are provided. The connectors used are TYCO AMP part number 787171-5 or equivalent.

A suitable 2-meter, double-ended, 25-pair cable is Highland model J52, TRIPPLITE part number S366-006.

Pinout is as follows:

Channel	Connector	IN+ Pin	IN- PIN
0	J1	1	26
1	J1	2	27
2	J1	3	28
3	J1	4	29
4	J1	5	30
5	J1	6	31
6	J1	7	32
7	J1	8	33
8	J1	9	34
9	J1	10	35
10	J1	11	36
11	J1	12	37
12	J1	13	38
13	J1	14	39
14	J1	15	40
15	J1	16	41
16	J1	17	42
17	J1	18	43
18	J1	19	44
19	J1	20	45
20	J1	21	46
21	J1	22	47
22	J1	23	48
23	J1	24	49
24	J2	1	26
25	J2	2	27
26	J2	3	28
27	J2	4	29
28	J2	5	30
29	J2	6	31

Channel	Connector	IN+ Pin	IN- PIN
30	J2	7	32
31	J2	8	33
32	J2	9	34
33	J2	10	35
34	J2	11	36
35	J2	12	37
36	J2	13	38
37	J2	14	39
38	J2	15	40
39	J2	16	41
40	J2	17	42
41	J2	18	43
42	J2	19	44
43	J2	20	45
44	J2	21	46
45	J2	22	47
46	J2	23	48
47	J2	24	49
GND	J1	25	50
GND	J2	25	50

The GND pins listed above are PCB/VME backplane grounds. Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

5. Operation

5.1 LEDs

There are four front-panel LED indicators.

The blue VME LED flashes whenever the module is accessed from the VME bus.

The green CPU LED flashes about once a second to indicate FPGA activity.

The red ERR LED will illuminate to indicate a BIST error.

The orange USR LED displays a user-defined blink pattern.

There is an additional LED on the PCB surface which illuminates green when the FPGA is properly configured.

5.2 Powerup Defaults

At powerup, the module setup will be:

Debounce rise and fall registers set to 1 millisecond

ULED led control register clear

The red ERR LED will be on at powerup, and will go off when the FPGA is properly initialized and operating.

The powerup sequence takes about 1 second.

5.3 Quick Start Procedure

Basic operation of the V280 can be demonstrated by the following steps:

A 6U VME crate and computer interface are required. The crate must be compliant with the IEEE 1014 VME specification, or the equivalent ANSI/VITA 1-1994 (R2002) VMEbus spec. Any crate with the standard power supplies (+12, +5, -12) and the 16-bit "P1" bus is adequate.

The computer interface must allow, as a minimum, reading and writing 16-bit registers in the A16 or A24 address spaces.

Pick an address space and module base address and set the V280 dip switches accordingly. See section 4.1. The as-shipped default is address 0xC000 in the 16-bit supervisory address space.

With crate power off, insert the V280 into any crate slot and firmly secure its mounting screws. **Do not hot-plug VME modules.**

Power up. The green "CPU" LED should blink, and the other LEDs should be off.

Now run software that can display the contents of VME registers.

Read the manufacturer ID register, the 16-bit VME register at the module base address. The default address would be 0xC000 in the A16 supervisory space. The blue "VME" LED should flash, and the register value should be 0xFEEE, identifying this as a Highland VME module.

Read the next register, offset address 2, default 0xC002. It should read 22280 decimal, 0x5708, identifying the module as a V280.

The six risetime/falltime debounce registers will power up at 100 decimal, setting step response times to 1 millisecond. Change these if desired.

Read the states of the 48 inputs in the STATE0 through STATE2 registers. The data is accessible at VMEbus speed, under 400 ns per register read, with no handshaking or software timing required. A "1" bit corresponds to voltage applied at the corresponding input.

To run BIST, write 0x8401 to the MACRO register. The full 48-channel test will take less than 250 microseconds. At the end of the test, the BIST register will self-clear if there are no errors, and will display an error code in its MS byte if any errors are detected.

The red ERR led will reflect the BIST result.

6. VME Registers

The V280 implements 256 16-bit VME registers. REG# below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address.

Registers identified as "RO" are read-only and should not be written from VME.

Read-write (RW) registers are written and read back by VME and, after powerup initialization, are generally not altered by the internal logic.

6.1 VME Register Map

Reg Name	REG#	Offset	R/W	Function
VXI MFR	0	0x00	RO	Highland ID: reads 65262, xFEEE
VXI TYPE	1	0x02	RO	V280 module ID, 22280, 0x5708
MODREV	2	0x04	RO	hardware revision, typically ASCII "B"
SERIAL	3	0x06	RO	unit serial number
ROM ID	4	0x08	RO	firmware ID, typically 22280 decimal
ROM REV	5	0x0A	RO	firmware revision, typically ASCII "B"
MCOUNT	6	0x0C	RO	1 KHz realtime counter
DASH	7	0x0E	RO	module version (dash) number
CALID	8	0x10	RO	Calibration table status
YCAL	9	0x12	RO	Calibration date: year
DCAL	10	0x14	RO	Calibration date: month/day
ULED	12	0x18	RW	user LED control
MACRO	16	0x20	RW	Macro control register
MP0	17	0x22	RW	Macro parameter
MP1	18	0x24	RW	Macro parameter
MP2	19	0x26	RW	Macro parameter
MP3	20	0x28	RW	Macro parameter
STATE0	24	0x30	RO	Inputs 15..0 state
STATE1	25	0x32	RO	Inputs 16-23 state

Reg Name	REG#	Offset	R/W	Function
STATE2	26	0x34	RO	Inputs 24-47 state
RISE0	28	0x38	RW	Inputs 15..0 rise debounce time
RISE1	29	0x3A	RW	Inputs 16..23 rise debounce time
RISE2	30	0x3C	RW	Inputs 24..47 rise debounce time
FALL0	32	0x40	RW	Inputs 15..0 fall debounce time
FALL1	33	0x42	RW	Inputs 16..23 fall debounce time
FALL2	34	0x44	RW	Inputs 24..47 fall debounce time
ERR0	36	0x48	RO	BIST error flags 0..15
ERR1	37	0x4A	RO	BIST error flags 16..23
ERR2	38	0x4C	RO	BIST error flags 24-47
BUF0	128	0x100	RW	read/write buffer, 128 words
...	**...**	**...**	RW	
BUF127	255	0x1FE	RW	

6.2 Detailed Register Descriptions

6.2.1 Module Overhead Registers

A number of read-only overhead registers are provided.

VXIMFR	reads 0xFEEE, Highland's registered VXI module ID code
VXITYPE	reads 22280 decimal to identify a V280 module
MODREV	ASCII code identifying the revision letter of the Hardware, typically 0x0042, ascii "B"
SERIAL	module serial number
ROM ID	firmware version, typically 22280 decimal
ROM REV	ASCII code identifying the revision letter of the firmware, typically 0x0042, ascii "B"
MCOUNT	a 16-bit counter that is incremented by the internal logic at 1 KHz
DASH	module version (dash) number
CALID	reads 22280 decimal to identify firmware
YCAL	displays the calibration year in decimal
YDAY	displays the calibration month and day

6.2.2 ULED - User LED Control

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on.

6.2.3 STATE0... STATE2 Input State Registers

There are three registers which reflect the levels of the 48 isolated digital inputs.

STATE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

STATE1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S31	S30	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16

STATE2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S47	S46	S45	S44	S43	S42	S41	S40	S39	S38	S37	S36	S35	S34	S33	S32

Each bit will go high if a voltage is applied to the corresponding isolated input. These bits are digitally filtered to debounce the inputs, with filtering programmed in the RISE and FALL registers.

These registers may be read at any time, at VMEbus speed.

6.2.4 RISE and FALL Registers

Each channel has a debounce digital filter. Registers are provided to set the rise (voltage ON) and fall (voltage OFF) time delay, in three groups of 16 registers.

```
RISE0 controls ON delay for channels 15..0
RISE1 controls ON delay for channels 23..16
RISE2 controls ON delay for channels 47..24

FALL0 controls OFF delay for channels 15..0
FALL1 controls OFF delay for channels 23..16
FALL2 controls OFF delay for channels 47..24
```

The time-domain behavior is similar to a Bessel lowpass filter followed by a Schmitt trigger, where the risetime and falltime of the filter are separately programmable.

Each of these registers declares a time delay from 10 µs to 655 ms, with LSB value of 10 µs. The powerup default is all six registers set to 100 decimal, for 1 millisecond ON and OFF delay.

The filter facility may also be used to allow clean acquisition of AC inputs. For example, if a RISE register were set to 100 (1 millisecond ON delay) and the corresponding fall were set to 2500 (25 milliseconds OFF delay), 50 or 60 Hz AC inputs would be cleanly displayed in the STATE bits.

Rise/fall programming can also be used to catch momentary glitch inputs. For example, rise/ON delay could be set to 1 millisecond and fall/OFF delay could be set to 600 milliseconds. System software can check the bit state every 500 milliseconds and not miss any momentary closures.

6.2.5 ERR0...ERR2 Self-test Error Registers

The three ERR registers provide 48 error flag bits, one for each input. Bits are cleared by a successful BIST test, and set if a channel fails BIST.

```
ERR0 flags errors on channels 15..0
ERR1 flags errors on channels 23..16
ERR2 flags errors on channels 47..24
```

The bit mapping is identical to the STATE registers.

6.2.6 Buffer Registers

The 128 16-bit buffer registers are used by factory macros. Users may treat them as general-purpose RAM. A read-write data pattern test of this RAM, plus a read of the first two ID registers, is a complete test of the module's VME address and data paths.

6.3 Macros and BIST

The MACRO register is used to invoke special module operations. The only defined user macro is the BIST self-test command.

If an undefined user macro was entered into the MACRO register, the register will read 0x0200 to indicate an invalid macro.

To initiate the BIST sequence,

Verify that the MS bit, bit 15, of the MACRO register is clear. This is the "macro busy" bit.

Write the BIST command, 0x8401, to the MACRO register

Wait for MACRO bit 15 to clear. This will take less than 250 microseconds

Examine the MS byte of MACRO, bits 15...8. If this byte is zero, there were no errors. If nonzero, there was an error.

If there was an error, the ERR0...ERR2 registers will flag the failed channels.

Other macro codes are reserved for factory use.

The channel debounce filters are frozen during the self-test, so no STATE register bits will glitch during the test. Data propagation time, from electrical inputs to STATE register bits, may increase by as much as 250 microseconds. Given that, it is generally practical to run the BIST operation while normal data acquisition is active.

7. Versions

Standard versions of the V280 include:

V280-1: 48-channel VME isolated digital input module with 5V threshold and BIST

V280-2: 48-channel VME isolated digital input module with 24V threshold and BIST

V280-12: 48-channel VME isolated digital input module with 24V threshold, BIST, and conformal coating

8. Customization

Consult factory for information about additional custom versions.

9. Hardware and Firmware Revision History

9.1 Hardware Revision History

22A280 Revision B	Jul 2014 Improved BIST transformer performance at high temperatures
22A280 Revision A	Apr 2014 Initial PCB release

9.2 Firmware Revision History

The firmware is provided as a plug-in EEPROM chip which can be field upgraded.

22C280 Revision B	Oct 2014 Fixed ULED bug
22C280 Revision A	Apr 2014 Initial firmware release

10. Accessories

J51	3' shielded-pair 50 pin male SCSI cable
J52	6' shielded-pair 50 pin male SCSI cable
J280	50 pin SCSI breakout board

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