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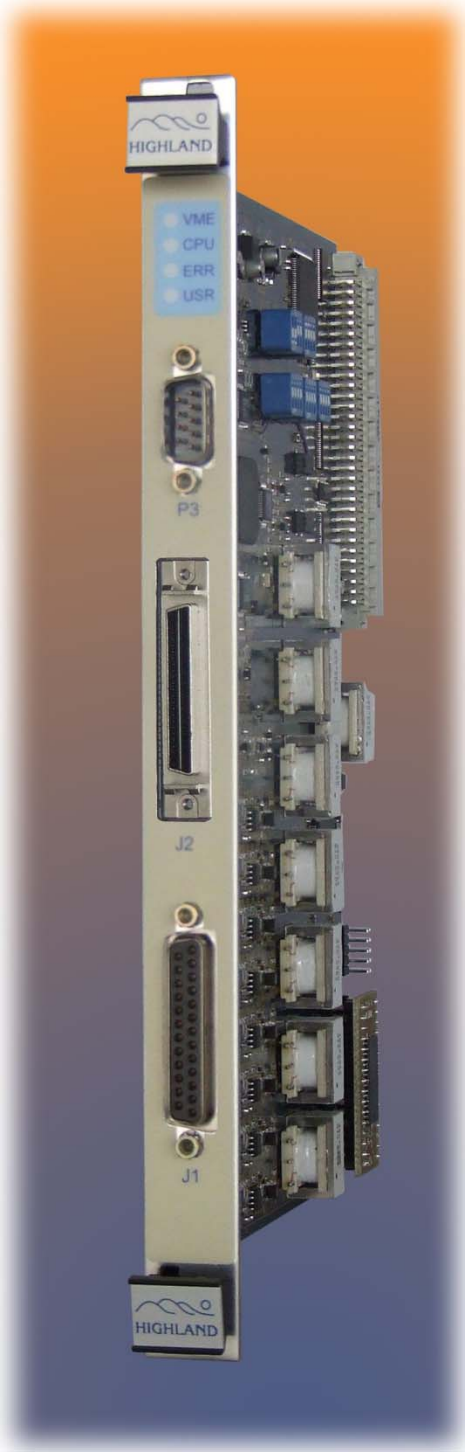
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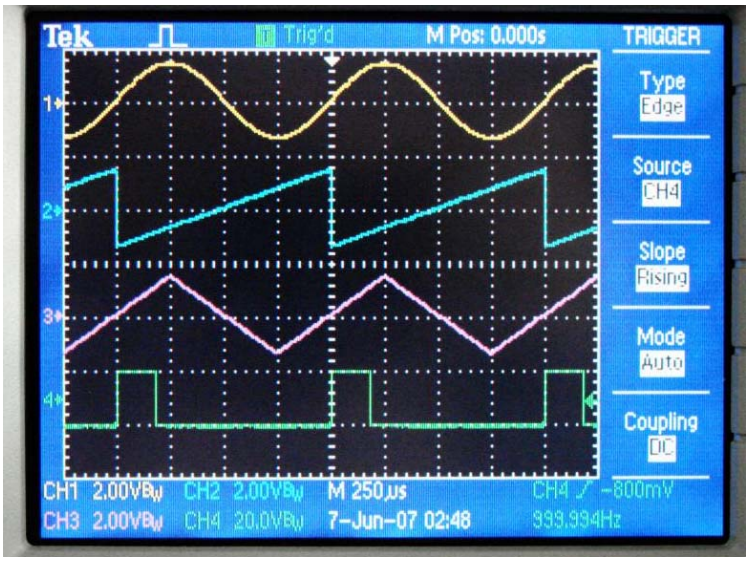
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HIGHLAND TECHNOLOGY



V340 VME WAVEFORM GENERATOR MODULE



Technical Manual

October 9, 2017

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1 *Introduction*

This is the technical manual for the Highland Model V340 eight-channel sinewave generator VME module.

Features of the V340 include:

- 8 channels of independent or synchronized sine, sawtooth, triangle, or square/pulse/PWM waveform generation
- Simple programming procedures for basic sinewave generation
- Output frequency range 0 to 2 MHz with 0.004 Hz resolution
- DC coupled outputs to 20.48 volts p-p
- Programmable offset allows wave+offset or direct DC DAC functionality
- Programmable channel phase allows quadrature or polyphase waveforms
- Optional transformers provide isolated outputs to 100 volts p-p
- Programmable digital pulse/PWM outputs can simulate transducers or quadrature encoders
- Auxiliary connector provides waveform sync outputs and digital expansion
- One general-purpose, differential, frequency counter input
- Clearly labeled dipswitches set VME address; no jumpers, headers, or trimpots
- Includes channel test connector, allowing in-crate check of channel performance without removing field wiring
- Optional built-in self-test (BIST)

This manual applies to the V340-10 through V340-31 versions.

2 *Specifications*

Specifications are typical unless otherwise noted.

FUNCTION	8-channel VME function generator
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16 Implements 128 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
CHANNELS	8 function generators, DC coupled -2x and -3x versions add programmable isolation per channel, fault simulation 8 TTL channel synchronization signals
FUNCTION WAVEFORMS	Sine, sawtooth, triangle, pulse
FAULT SIMULATION (TRANSFORMER VERSIONS ONLY)	High side ground short Low side ground short Differential short Open circuit
FUNCTION AMPLITUDE	DC coupled, programmable ±10.24 V and ±1.024 ranges Optional isolation transformers (1:1 or 5.4:1)
OUTPUT IMPEDANCE	50 Ω typical
RESOLUTION	Amplitude, 14 bits Frequency, 30 bits (~ 0.0037 Hz) Pulse duty, 16 bits (~ 0.0015 %)
BANDWIDTH	DC coupled: DC to 2 MHz 1:1 transformers: 100 Hz to 250 kHz 5.4:1 transformers: 100 Hz to 50 kHz
OFFSET ERROR	±1.024 V range: 2mV typ, 15-35°C Both ranges: 10 mV max, 0-60°C
GAIN ERROR	DC coupled: 0.5 % max, 15-35°C; 1 % max, 0-60°C Transformer coupled: 10% max (unloaded)
FLATNESS	±0.25 dB over DC coupled range
FREQUENCY ACCURACY	100 PPM

SYNC OUTPUTS	$V_{H:}$ 4.8 V typical, 4.2 V min @ 24 mA V_L: 0.1 V typical, 0.6 V max @ 24 mA Duty cycle: 50% ± 22 ns max
FREQUENCY COUNTER INPUT	Differential, 2 V to 300 V P-P 10 Hz to 2 MHz
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies: +5 V, 0.8 A max +12 V, 0.5 A max -12 V, 0.5 A max
CONNECTORS	One D25 female, 8 wave outputs and one differential frequency input One SCSI 50-pin female, sync outputs and digital expansion One D9 male, test/calibration check
INDICATORS	LEDs indicate VME access, CPU activity, error conditions Additional user programmable LED
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes
VERSIONS	V340-10 Standard unit; no transformers, no BIST V340-11 Standard unit; no transformers, with BIST V340-20 With switchable 1:1 transformers V340-21 With switchable 1:1 transformers and BIST V340-30 With switchable 5:1 transformers V340-31 With switchable 5:1 transformers and BIST

3 *Overview*

The V340 includes 8 independent DDS-based waveform generators, one frequency counter, and a general purpose TTL interface.

An internal microprocessor manages all data I/O and communicates with the VMEbus via a transparent, VMEbus-speed dual-port memory.

Relays are provided to reroute any waveform output channel to the internal test bus, thence to the BIST for self-test, or to the dedicated D9 connector for calibration checks without disrupting field wiring.

The overall block diagram of the V340 is shown below:

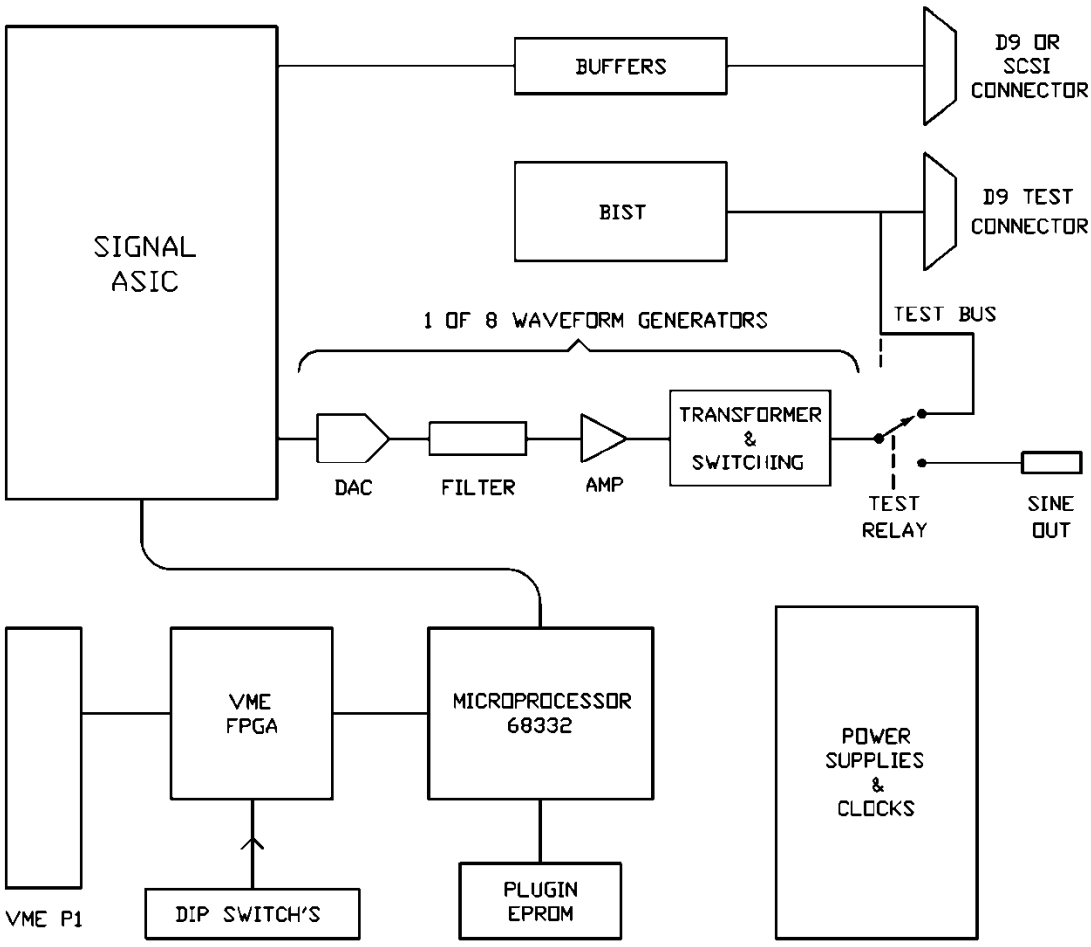


Figure 1. V340 Block Diagram

Waveforms are generated by direct digital synthesis. A 32-bit phase accumulator is clocked at 64 MHz, advancing in phase by a programmable amount. The most significant 11 bits of the advancing phase word is passed through a 2K x 16 bit waveform lookup table, synthesizing a sine, triangle, or sawtooth wave. The output of the lookup table is amplitude scaled by digital multiplication and then drives a 14 bit D/A converter. The DAC output is then lowpass filtered and amplified to become the channel output.

The scale factor of each DAC is programmable X1 or X0.1, allowing low-level outputs to be generated at full 14-bit DAC resolution.

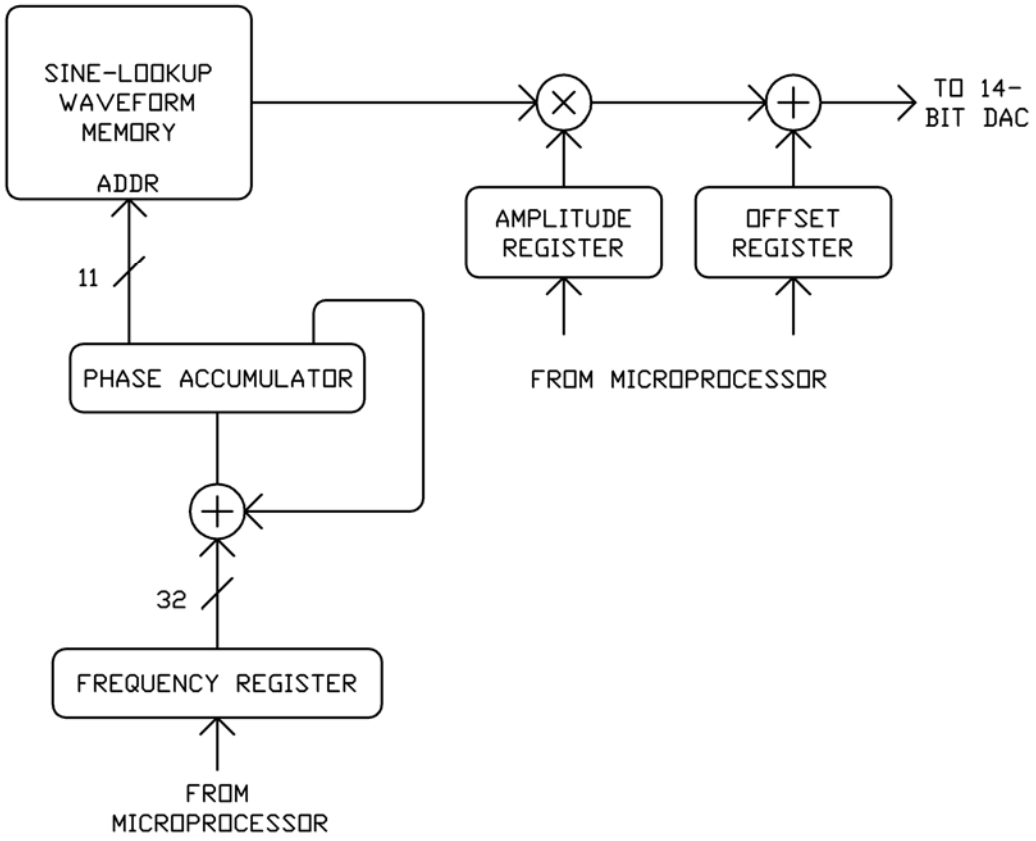


Figure 2.

Each of the eight channels also incorporates a pulse/PWM generator that may be substituted for the waveform lookup table. The PWM logic generates a waveform of variable duty cycle and full-scale bipolar swing, which can then be scaled by the amplitude, offset, and X0.1 signal path.

The output stage of each channel consists of a lowpass filter, 50-ohm power amplifier, and a test-bus relay. An optional per-channel isolation transformer with switching matrix may be included.

On versions without transformers, the high-side output is directly driven from the amplifier output and the low-side pins are grounded. Active output impedance is 50 ohms.

The optional transformers are enabled with solid-state relays, under software control, as shown in the figure below. Additional SSRs allow grounding of either end of the floating transformer output, or allow simulating a line-line short, or setting both pins to a HI-Z state. Two transformer options are available, with unloaded transformer ratios of 1:1 and 5.4:1 step-up.

The 1:1 transformer has a bandwidth of at least 250 KHz. At low frequencies, amplitude must be limited to avoid transformer saturation, with full-scale amplitude available down to 100 Hz. Below 100 Hz, amplitude should be limited to 0.2 volts p-p per Hz. Output impedance is about 100 ohms.

The 5.4:1 step-up transformer can output up to 100 volts p-p from 100 Hz to at least 50 KHz. Below 100 Hz, programmed amplitude must be reduced to prevent transformer saturation and associated waveform distortion; the maximum undistorted output is 1 volt p-p per Hz. Output amplitude rolls off rapidly above 50 KHz, down 3 dB at about 60 KHz, and less with significant capacitive loading. Maximum short-circuit output current is about 18 mA RMS. Output impedance is about 2K ohms, so is fairly sensitive to capacitive cable loading.

A test relay allows the channel output to be diverted to the internal test bus, where it may in turn be routed to the D9 calibration connector or to the internal BIST system.

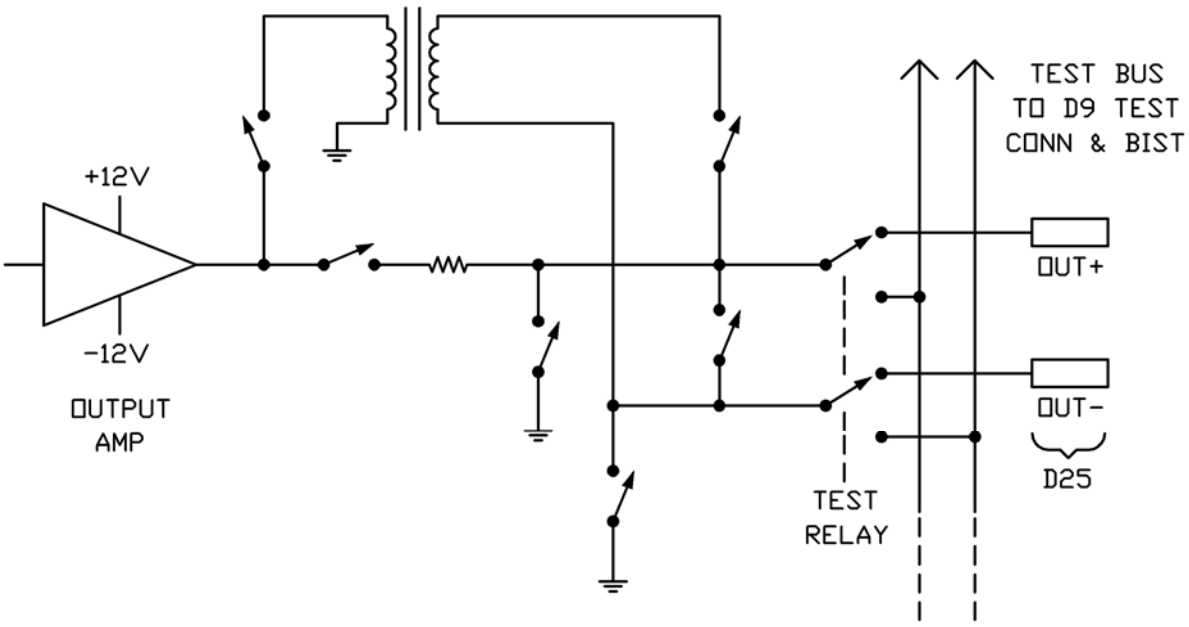


Figure 3.

4 Connections and Installation

4.1 Address DIP Switches

Five 4-position rocker-type dipswitches are provided near the top edge of the board. The addressing switches are labeled "A23" through "A8" and finally "A24M".

To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A8 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space, as shown in the figure below.

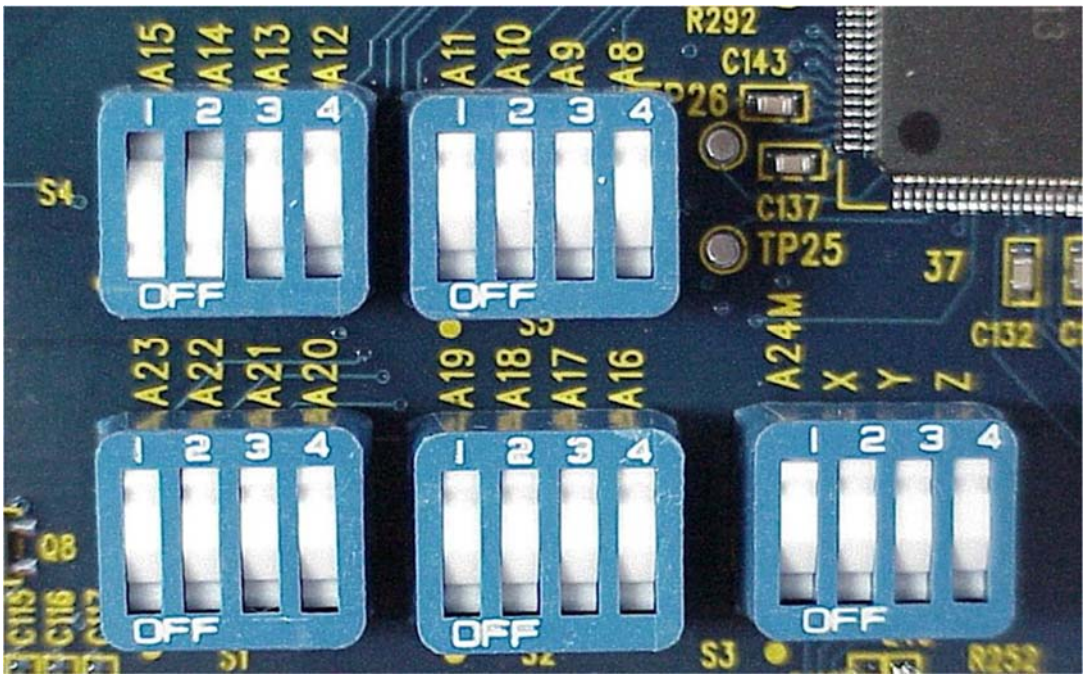


Figure 4. Address DIP Switch Configuration for 0xC000 in A16 Space

4.2 Option Switches

The X-Y-Z dip switches shown in the figure above may be read in the three low bits of the VDIPS register. They are pictured in their OFF positions.

If the Z switch is set ON, the module will power up in DEMO mode. All channels will output 1 volt RMS sine waves, DC coupled, with zero DC offset. Channel sinewave frequencies will be the powerup defaults, with channels 0 through 7 being set to 1 through 8 KHz respectively.

On modules equipped with the optional output transformers, if the Y switch is set on, all channels will power up in the HIZ state. This switch is ignored in DEMO mode.

The photo below shows the waveforms of channels 0, 1, 2, and 3 after the module is started in DEMO mode. The channel frequencies are 1, 2, 3, and 4 KHz respectively, and all are synchronized to zero-cross at the positive zero crossing of the channel 0 sinewave.

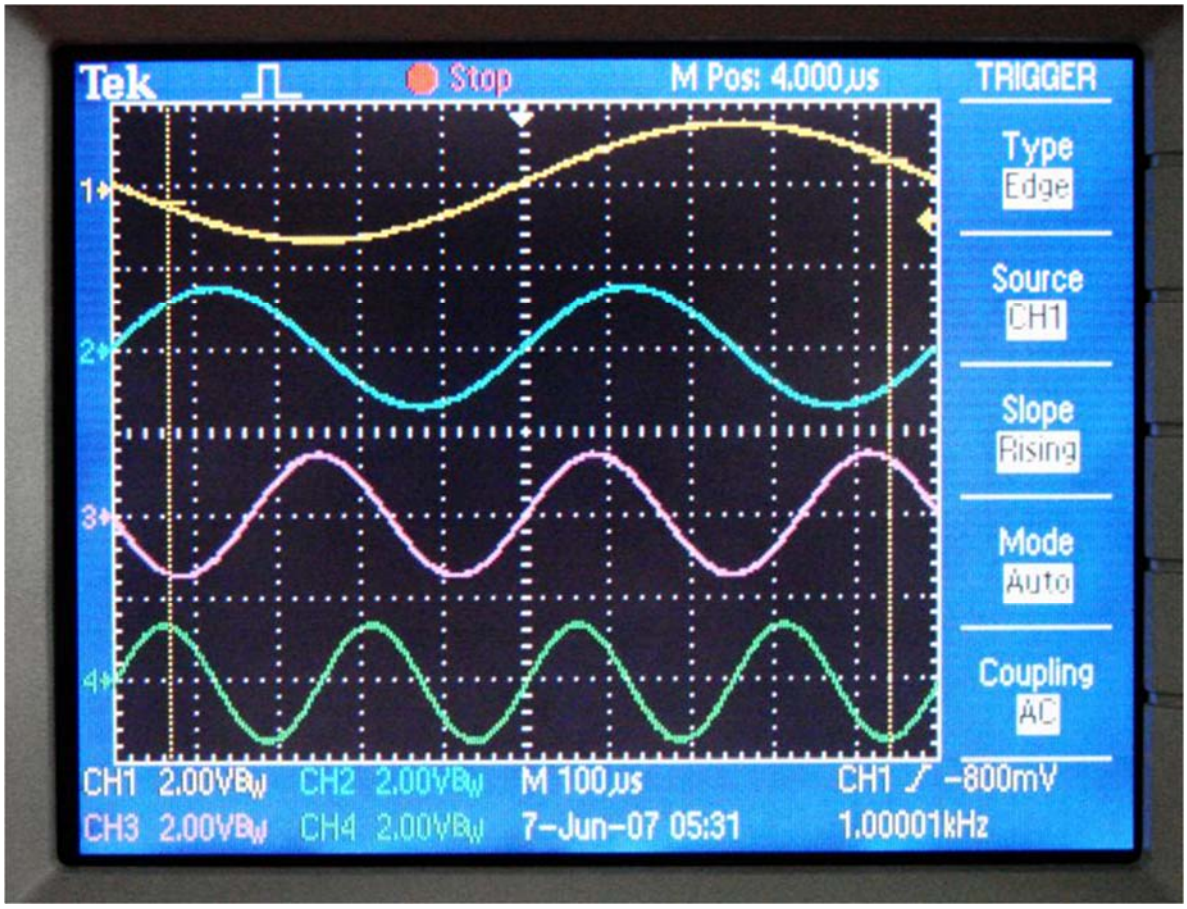


Figure 5. DEMO mode waveforms

4.3 *Installation*

The V340 may be installed in any VME (IEEE 1014) crate, including VME64 variants. It uses only the P1 backplane connector

The V340 passes all interrupt and bus grant signals, so may be used with backplane grant jumpers installed or not installed.

CAUTION: Do not install or remove the V340 with crate power on. VME modules are not hot-pluggable. The V340 will be damaged if hot-plugged.

CAUTION: Fully seat the module and secure front-panel screws before applying power.

CAUTION: Handle the V340 with proper ESD precautions to avoid static damage.

4.4 *D25 Output Connector*

The front-panel female D-25 connector J1 accommodates eight waveform outputs and one differential frequency-counter input.

The pinout of the D25 connector is as follows:

J1 Pin No.	Description	Function
1	Wave0+	Channel 0 waveform out
14	Wave0-	
2	Wave1+	Channel 1 waveform out
15	Wave1-	
3	Wave2+	Channel 2 waveform out
16	Wave2-	
4	Wave3+	Channel 3 waveform out
17	Wave3-	
5	Wave4+	Channel 4 waveform out
18	Wave4-	
6	Wave5+	Channel 5 waveform out
19	Wave5-	
7	Wave6+	Channel 6 waveform out
20	Wave6-	
8	Wave7+	Channel 7 waveform out
21	Wave7-	
22	Freq+	Frequency counter input
23	Freq-	
13		VME Gnd
25		VME Gnd

For versions without transformers, the WAVE- pins are hardwired to VME ground.

On transformer versions, the Wave- pins are switched to VME ground when output transformers are disabled, and each Wave+ / Wave- pin pair becomes a floating differential output when a channel transformer is software enabled.

The "Freq" pair is a differential frequency counter input, with each side having nominal 50K impedance to ground.

4.5 *50-pin SCSI Connector*

The front-panel female 50-pin female SCSI connector J2 has provision for 16 TTL data lines and four control lines. For the versions referenced by this manual, only eight outputs are used, each being a sync signal for one sinewave output channel.

Each sync signal is a 5-volt TTL/CMOS logic level square wave which rises at the positive-going zero crossing of its respective sine wave generator. It is essentially the inverted MSB of the respective phase accumulator. The sync outputs are picked off before any channel phase rotations are applied. Quantization effects result in a small residual jitter, on the order of 20 ns p-p.

Pinout is as follows:

J2 Pin No.	Function
17	Sync Output 0+
42	Sync Output 0 ground
16	Sync Output 1+
41	Sync Output 1 ground
15	Sync Output 2+
40	Sync Output 2 ground
14	Sync Output 3+
39	Sync Output 3 ground
13	Sync Output 4+
38	Sync Output 4 ground
12	Sync Output 5+
37	Sync Output 5 ground
11	Sync Output 6+
36	Sync Output 6 ground
10	Sync Output 7+
35	Sync Output 7 ground

The paired pins correspond to the twisted pairs of a standard SCSI cable. The grounds are pcb/VME ground. Individually-shielded-pair SCSI cables are recommended to minimize crosstalk.

Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws. The V340 does not connect front-panel ground to VME ground.

4.6 *D9 Calibration Connector*

A male D9 connector P3 is provided for connection to external instruments to verify channel output functionality and calibration. Each wave generator channel incorporates a relay which allows it to be switched, under software control, to this test connector.

Pinout is as follows:

P3 Pin No.	Description	Function
7	CalSig+	To external precision DVM/ frequency counter
6	CalSig-	
1		VME Gnd

The RELAYS register is used to control the channel relays, and the MODE register controls external access to the cal bus; see sections 6.4 and 6.6.

5 *Basic Operation*

5.1 *General Considerations*

The V340 occupies 128 16-bit VME registers. DIP switches are provided to set the base address to any 128-word boundary in the A16 or A24 address spaces. All registers are implemented as true dual-port memory which is shared between the VMEbus and the internal microprocessor.

VME access time is typically 200 ns, measured from DS* to DTACK*.

The module is normally shipped configured for base address of 0xC000 in the A16 address space.

Certain register pairs represent 32-bit values and must be written or read atomically to ensure that updates do not create skew errors. Atomic pairs must be written in the order MS:LS, and will not be effective until the LS word is written. Similarly, atomic pairs must be read in the same order, MS:LS.

Note: The V340 does not support single-byte writes from VME.

Although the V340 has many signal-processing features, the user interface allows basic waveform generation to be done with a minimum of programming; it is only necessary to write to the channel frequency and amplitude registers to produce basic sinewave outputs. Section 10 of this manual presents operating scenarios from this basic sinewave generation up through the most complex modes.

5.2 *Front-Panel LEDs*

The blue VME LED will flash whenever the V340 is addressed from the VMEbus.

The green CPU LED will blink once about every two seconds to indicate that the internal firmware is operating normally. See section 8 for notes on LED operation during BIST self-test.

The red ERROR LED will normally be off. It will flash if any error flags are set.

The orange USER LED may be programmed from the VMEbus.

6 *VME Registers*

The V340 implements 128 16-bit VME registers. REG# below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address. The as-shipped default address is 0xC000 in the A16 space.

Registers identified as "RO" should be treated as read-only and should not be written from VME; these registers are periodically refreshed by the V340.

The letter "A" in the R/W column indicates that a register pair is atomically locked for 32-bit operations. Atomic pairs must be read or written in the order MS:LS.

Read-write (RW) registers are written from VME and, after powerup initialization, are not altered by the internal microprocessor.

Registers tagged RWM can be written by VME or by the internal uP, in accordance with the protocol defined for executing Macro operations.

Reg Name	REG#	Offset	R/W	Function
VXI MFR	0	0x00	RO	VXI mfr ID: reads 65262 (0xFEEE)
VXITYPE	1	0x02	RO	module type, always 22340 decimal
VDIPS	2	0x04	RO	option switch settings X Y Z
SERIAL	3	0x06	RO	unit serial number
ROM ID	4	0x08	RO	firmware ID, typically 22340 decimal
ROM REV	5	0x0A	RO	Firmware revision, typically ASCII "A"
MCOUNT	6	0x0C	RO	microprocessor IRQ update counter
DASH	7	0x0E	RO	module version/dash number
EFLAGS	8	0x10	RO	Error flags
SUBS	9	0x12	RW	Channel synchronous update controls
RELAYS	11	0x16	RW	controls calibration-bus relays
ULED	12	0x18	RW	user LED control
MODE	13	0x1A	RW	module operating mode
BERR	14	0x1C	RO	BIST error flags
BISS	15	0x1E	RO	built-in self-test BIST control
MACRO	16	0x20	RW M	macro command register
PARAM0	17	0x22	RW M	macro parameter

Reg Name	REG#	Offset	R/W	Function
PARAM1	18	0x24	RW M	macro parameter
PARAM2	19	0x26	RW M	macro parameter
PARAM3	20	0x28	RW M	macro parameter
PARAM4	21	0x2A	RW M	macro parameter
PARAM5	22	0x2C	RW M	macro parameter
YCAL	24	0x30	RO	calibration date, year
DCAL	25	0x32	RO	calibration date, month:day
VZERO	31	0x3E	RO	BIST ADC zero check, 0x0800 nom
CTL0	32	0x40	RW	Ch 0 control register
AMP0	33	0x42	RW	Ch 0 amplitude
FH0	34	0x44	RW A	Ch 0 frequency, MS 16 bits
FL0	35	0x46	RW A	Ch 0 frequency, LS 16 bits
OFS0	36	0x48	RW	Ch 0 DC offset
PHA0	37	0x5A	RW	Ch 0 phase
PWM0	38	0x4C	RW	Ch 0 duty cycle
CTL1	40	0x50	RW	Ch 1 control register
AMP1	41	0x52	RW	Ch 1 amplitude
FH1	42	0x54	RW A	Ch 1 frequency, MS 16 bits
FL1	43	0x56	RW A	Ch 1 frequency, LS 16 bits
OFS1	44	0x58	RW	Ch 1 DC offset
PHA1	45	0x5A	RW	Ch 1 phase
PWM1	46	0x5C	RW	Ch 1 duty cycle
CTL2	48	0x60	RW	Ch 2 control register
AMP2	49	0x62	RW	Ch 2 amplitude
FH2	50	0x64	RW	Ch 2 frequency, MS 16 bits
FL2	51	0x66	RW	Ch 2 frequency, LS 16 bits
OFS2	52	0x68	RW	Ch 2 DC offset
PHA2	53	0x6A	RW	Ch 2 phase
PWM2	54	0x6C	RW	Ch 2 duty cycle

Reg Name	REG#	Offset	R/W	Function
CTL3	56	0x70	RW	Ch 3 control register
AMP3	57	0x72	RW	Ch 3 amplitude
FH3	58	0x74	RW A	Ch 3 frequency, MS 16 bits
FL3	59	0x76	RW A	Ch 3 frequency, LS 16 bits
OFS3	60	0x78	RW	Ch 3 DC offset
PHA3	61	0x7A	RW	Ch 3 phase
PWM3	62	0x7C	RW	Ch 3 duty cycle
CTL4	64	0x80	RW	Ch 4 control register
AMP4	65	0x82	RW	Ch 4 amplitude
FH4	66	0x84	RW A	Ch 4 frequency, MS 16 bits
FL4	67	0x86	RW A	Ch 4 frequency, LS 16 bits
OFS4	68	0x88	RW	Ch 4 DC offset
PHA4	69	0x8A	RW	Ch 4 phase
PWM4	70	0x8C	RW	Ch 4 duty cycle
CTL5	72	0x90	RW	Ch 5 control register
AMP5	73	0x92	RW	Ch 5 amplitude
FH5	74	0x94	RW A	Ch 5 frequency, MS 16 bits
FL5	75	0x96	RW A	Ch 5 frequency, LS 16 bits
OFS5	76	0x98	RW	Ch 5 DC offset
PHA5	77	0x9A	RW	Ch 5 phase
PWM5	78	0x9C	RW	Ch 5 duty cycle
CTL6	80	0xA0	RW	Ch 6 control register
AMP6	81	0xA2	RW	Ch 6 amplitude
FH6	82	0xA4	RW A	Ch 6 frequency, MS 16 bits
FL6	83	0xA6	RW A	Ch 6 frequency, LS 16 bits
OFS6	84	0xA8	RW	Ch 6 DC offset
PHA6	85	0xAA	RW	Ch 6 phase
PWM6	86	0xAC	RW	Ch 6 duty cycle
CTL7	88	0xB0	RW	Ch 7 control register

Reg Name	REG#	Offset	R/W	Function
AMP7	89	0xB2	RW	Ch 7 amplitude
FH7	90	0xB4	RW A	Ch 7 frequency, MS 16 bits
FL7	91	0xB6	RW A	Ch 7 frequency, LS 16 bits
OFS7	92	0xB8	RW	Ch 7 DC offset
PHA7	93	0xBA	RW	Ch 7 phase
PWM7	94	0xBC	RW	Ch 7 duty cycle
SNP0H	96	0xC0	RO	Ch 0 Phase Snapshot, MS word
SNP0L	97	0xC2	RO	Ch 0 Phase Snapshot, LS word
SNP1H	98	0xC4	RO	Ch 1 Phase Snapshot, MS word
SNP1L	99	0xC6	RO	Ch 1 Phase Snapshot, LS word
SNP2H	100	0xC8	RO	Ch 2 Phase Snapshot, MS word
SNP2L	101	0xCA	RO	Ch 2 Phase Snapshot, LS word
SNP3H	102	0xCC	RO	Ch 3 Phase Snapshot, MS word
SNP3L	103	0xCE	RO	Ch 3 Phase Snapshot, LS word
SNP4H	104	0xD0	RO	Ch 4 Phase Snapshot, MS word
SNP4L	105	0xD2	RO	Ch 4 Phase Snapshot, LS word
SNP5H	106	0xD4	RO	Ch 5 Phase Snapshot, MS word
SNP5L	107	0xD6	RO	Ch 5 Phase Snapshot, LS word
SNP6H	108	0xD8	RO	Ch 6 Phase Snapshot, MS word
SNP6L	109	0xDA	RO	Ch 6 Phase Snapshot, LS word
SNP7H	110	0xDC	RO	Ch 7 Phase Snapshot, MS word
SNP7L	111	0xDE	RO	Ch 7 Phase Snapshot, LS word
FRHI	112	0xE0	RO A	Frequency counter, MS count
FRLO	113	0xE2	RO A	Frequency counter, LS count
FTIM	114	0xE4	RW	Frequency counter timebase/control
PRHI	116	0xE8	RO A	Period measurement, MS
PRLO	117	0xEA	RO A	Period measurement, LS
BLOG	120-127	0xF0+	RO	BIST diagnostic log, 8 words

6.1 *Module Overhead Registers*

A group of read-only, fixed-value registers identify the module. They include:

VXI MFR always reads 0xFEEE, Highland's registered VXI id code.

VXITYPE always reads 22340 decimal

SERIAL module serial number.

ROM ID firmware version, typically 22340 decimal.

ROM REV an ASCII code identifying the revision letter of the firmware, typically 0x41 for the letter "A".

MCOUNT A 16-bit counter that is incremented by the internal logic about every 5 ms.

DASH module version/dash number, decimal 10, 11, 20, 21, 30, or 31.

6.2 *EFLAGS - Error Flags*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						CT	LE	E7	E6	E5	E4	E3	E2	E1	E0

An Ex error flag will be set if a channel is improperly programmed. Error bits will self-clear if the channel returns to normal operation.

LE will be set if an internal logic error is detected.

CT is set if the saved calibration table is invalid and the default cal table is in use.

The red ERR led will flash if any bits are set in the EFLAGS register.

6.3 *SUBS - Channel Synchronous Update Controls*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								S7	S6	S5	S4	S3	S2	S1	S0

Each of the eight waveform generators normally operates independently. If users change a channel amplitude, phase, offset, duty cycle, or frequency, the new settings are by default changed immediately – within about 250 microseconds - and asynchronously. In this mode, channel-channel phase relationships cannot be maintained.

When channels are used in a coordinated manner, it is often necessary to make changes synchronously, so that channel-channel relationships can be maintained. If a channel's Sn bit is set in the SUBS register, the selected channels are excluded from the periodic update loop, so changes made to any channel registers are not installed into that channel's hardware until an UPDATE or UPDATE+RESET macro is executed, in which case a group of channels may be updated simultaneously and coherently. See section 7.2 for discussion of the UPDATE macro functions.

6.4 *RELAYS - Calibration Bus Relays Control*

The RELAYS register controls actuation of the eight channel test relays.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								K7	K6	K5	K4	K3	K2	K1	K0

If the user sets any bit ON, the corresponding channel test relay will be actuated. The analog output of the associated channel will then be disconnected from the front-panel D25 connector and connected to the internal cal bus, which may in turn be routed, under control of the MODE register, to the CALSIG+ and CALSIG- Pins (Pins 7 and 6) of the D9 test connector; see 6.6 below.

See section 9 for a discussion of using the D9 connector for verification of module accuracy.

6.5 *ULED - User LED Control*

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on. Pattern 0xF000 would result in a blink pattern, 0.5 seconds on and 1.5 seconds off.

6.6 *MODE - Calibration Bus Control*

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															M0

Users may set the MODE bit M0 to 0 or 1. Zero is the normal operating mode and the powerup default.

If mode = 1 (M0 set) the module's internal CAL bus is connected to P3 Pins 7 and 6, allowing an external instrument to check the amplitude and frequency any channel whose test relay is actuated. All channels whose relays are not operated will continue to function normally.

6.7 *BISS and BERR - BIST Status Registers*

See section 8, BIST.

6.8 *MACRO, PARAMx - Macro Controls*

See section 7, Macro Operations.

6.9 *CTLx - Channel Control Registers*

Each of the 8 waveform generator channels has an associated channel control register, CTL0 through CTL7. The control register arrangement is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							PWM			HIZ	SHF	GFH	GFL	XFR	DIV

If users leave the DIV bit low, the channel output range is +-10.24 volts peak (7.24 volts RMS), as scaled by the channel amplitude register. If this bit is set high, amplitude is reduced by a factor of 10:1, to +-1.024 volts peak.

The XFR…HIZ bits are operative only on modules equipped with optional output transformers.

The XFR bit controls the output transformer. If XFR is low, the output amplifier is directly connected to the channel WAVE+ pin, and the WAVE- pin is grounded. If the user sets XFR high, the isolation transformer is inserted and the WAVE pin pair becomes a floating transformer-coupled output.

Setting GFL forces a ground-fault short onto the lowside output pin. Setting GFH ground-faults the high pin. Setting SHF shorts the output pin pair. Switching is done by solid-state relays rated for 100 volts max, with nominal 4 ohm ON resistance. These bits should be set only if the XFR bit is set to enable transformer coupling.

Users may set XFR and GFL to create a high-voltage (transformer coupled) output that is low-side grounded.

On units equipped with the optional transformers, if the HIZ bit is set, channel output will be set to high impedance, and no output signal will appear. Both the WAVE+ and WAVE- pins of this channel will become hi-z. If the “Y” dipswitch is set, all channels will power up in HIZ mode, after which users must clear each channel’s HIZ bit to enable outputs.

If the module is a non-transformer version, the HIZ bit is ignored. The WAVE- pin is hard grounded to VME ground and the WAVE+ pin is the direct 50-ohm amplifier output.

If the PWM bit is set, the channel will operate in pulse width/duty-cycle mode; see section 6.14.

At powerup, all eight channel control registers are normally cleared, so all channels operate in normal, sinewave, non-transformer mode, with maximum programmable output of 20.48 volts p-p, and operate in asynchronous update mode. If the "Y" dipswitch is on at powerup, all control registers power up with the HIZ bit set.

6.10 *AMPx - Channel Amplitudes*

Each of the 8 sine generator channels has an amplitude-set register, AMPn. If the DIV control-register bit is low, channel amplitude may be programmed from 0 up to +-10.24 volts (20.48 volts p-p sinewave amplitude, 7.24 volts RMS) over the AMPn range of 0 to +32767, 0x0000 to 0x7FFF.

The AMPx registers are signed, so negative 2’s complement values invert the phase of the outputs; -32768, 0x8000, is full-scale inverted output. This can be useful in phase-synchronized or PWM modes.

If DIV is set, outputs are attenuated by 10:1.

All eight amplitude-set registers power up at zero, unless the "Z" (demo mode) dipswitch is on. In that case, they power up set to 0x11AD, resulting in 1.0 volt RMS sinewave outputs.

6.11 *Channel Frequency-set Registers*

Each of the 8 waveform generator channels has a pair of frequency-set registers FHn and FLn. If they are loaded with a 32-bit value "N", the resulting frequency in Hz will be...

F = 16,000,000 * N / 2^32 or

N = F * 268.4355

which corresponds to an LSB value of 0.00372529 Hz. The maximum allowed value is 2 MHz, at which point N is equal to 0x2000:0000, about 537e6.

For example, to generate a 1 KHz sine wave on channel 0, set FH0 to 0x0004 and then set FL0 to 0x1894.

The pair of frequency-set registers is atomically interlocked to ensure coherent 32-bit writes. The registers must be written in the order FHn followed by FLn. The actual dual-port memory write will occur when the FLn register is written. At powerup, the channel 0 through 7 frequencies are set to 1 through 8 KHz respectively, so writing channel amplitudes will result in immediate sinewave outputs.

If it is required to maintain phase coherence between two or more channels, several conditions must be followed:

- Channels must be used in synchronous-update mode.
- Channel frequency set registers must be the same or exact multiples.
- Channels must be configured and then reset together.
- Any changes to channel settings must be performed synchronously, using an appropriate macro command.

Frequencies in the range of 0 to 2 MHz correspond to FHn:FLn register pair values from 0x0000:0000 to 0x2000:0000. It is also possible to program negative frequencies in the range of, equivalently, 0 to -2 MHz, corresponding to 0x0000:0000 through 0xE000:0000; simply negate the 32-bit FHn:FLn hex value. Negative 1 KHz thus corresponds to 0xFFFB:E76C.

A negative frequency corresponds to walking a waveform table “backwards”, which would reverse the phase relationship of polyphase sinewave or PWM outputs. One could effectively run a simulated 3-phase alternator or quadrature encoder clockwise at positive frequency settings and counterclockwise at negative frequency settings.

6.12 *Channel DC Offset Registers*

Each channel has an OFSn register which allows users to add a DC offset to the waveform output. The register defaults to zero, no offset. A setting of 0x7FFF adds the maximum positive offset, +10.2397 volts, and 0x8000 applies an offset of -10.24 volts. Both values are scaled down by 10:1 if the DIV control bit is set. If the active waveform and the offset sum to over +- 10.24 volts, the DAC output will appropriately clip at its maximum possible electrical output, typically about +-11 volts. If the channel AMPn register is set to zero, the offset register can be used as a simple DC-output DAC channel with +-10.24 volt range.

The programmed offset value is ignored (treated as zero) when a channel transformer is enabled in sine/triangle/sawtooth modes. If a transformer is enabled in PWM mode, the module firmware will compute and apply a dac offset such as to minimize the likelihood of transformer saturation.

6.13 *Channel Phase Registers*

Each channel has a PHAn register which shifts the phase of the output waveform. The 16-bit register can be treated as an unsigned integer “P” from 0 to 65535, where the waveform is advanced in phase (ie, shifted earlier in time) by an angle of 360*P/65536 degrees; a P setting of 4096 thus shifts the waveform phase ahead by 22.5 degrees. P can also be treated as a signed integer from +32767 to -32768, with associated +-180 degree phase shifts.

Phase shifting is only meaningful between channels that are operating in synchronized mode; see section 7.2 for details. Programmed phase shift does not affect the TTL-level SYNC pulses, as the phase shifting occurs downstream of the sync pulse pickoff.

6.14 *Channel PWM Registers*

If a channel’s PWM control bit is set, the channel operates in duty-cycle mode, with its PWMn register setting output duty cycle, the fraction of a cycle that the output is high. "High" corresponds to an equivalent data value of 0x7FFF, and "low" corresponds to data 0x8000. The resulting waveform switches from -10.24 volts "low" to +10.24 volts "high", scalable by the channel amplitude register.

The PWMn register content sets the "high" duty cycle of channel “n” from 0 (0x0000) to 99.9985% (0xFFFF.) The PWMn register is ignored in non-PWM mode and is set to 50% (0x8000) at powerup, corresponding to a square-wave output.

The effective waveform generated in PWM mode goes to maximum positive voltage (+10.24 max) for the first part of each cycle, and to maximum negative voltage (-10.24 volts) for the rest of the cycle, at the frequency defined by the channel frequency-set register pair. This 20.48 volt p-p waveform can be scaled down by the channel’s AMPn amplitude register, offset by the OFSn register, and phase shifted by the PHAn register. The output voltage is reduced by 10:1 if the channel control DIV bit is set. Rise/fall time is typically below 100 ns.

Filter characteristics result in PWM risetime of about 55 ns. Output high or low pulse widths should be no less than 125 ns for good pulse fidelity, which limits the minimum/maximum recommended duty cycle at higher channel frequencies. At 2 MHz, the duty cycle should therefore be in the range of 25 to 75 per cent.

PWM edges may jitter by as much as 20 ns p-p, except at frequencies which are an exact binary sub-multiple of 16 MHz.

Transformers may be enabled in PWM mode, but average output DC level will inherently be zero; V340 logic will adjust amplifier offset as a function of duty cycle to prevent DC from being applied to transformer primaries. Transformer bandwidth will limit edge rates. Transformers may also saturate and distort at low frequencies and certain duty cycles.

Two channels may be used in PWM mode to simulate a quadrature encoder or to drive a stepper motor. See section 10.7.

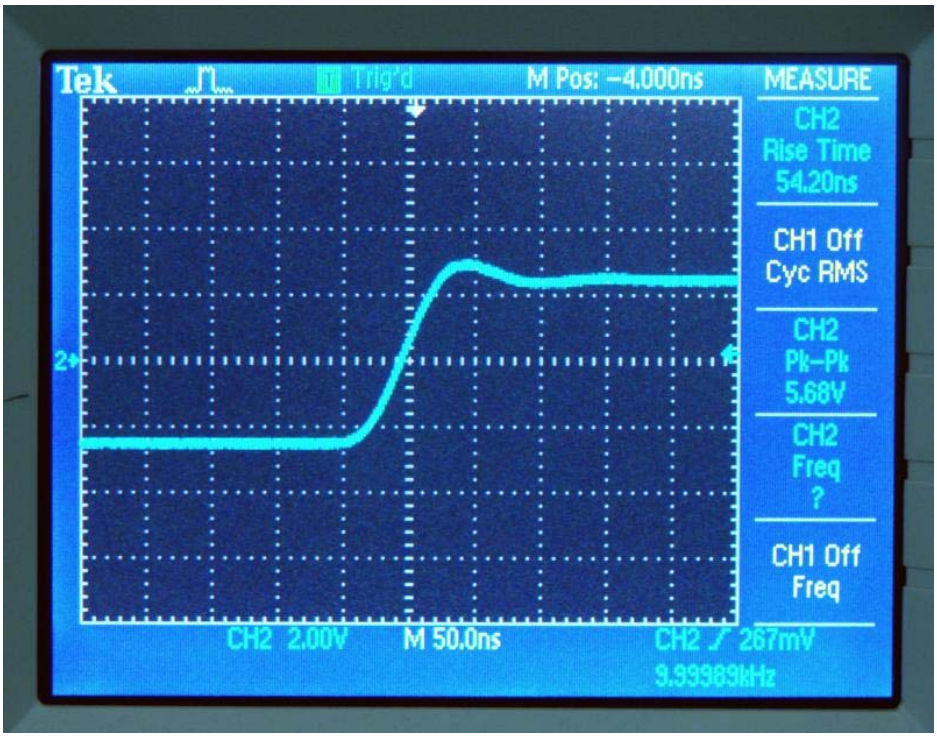


Figure 6. Rising edge in PWM mode

6.15 *Phase Snapshot Registers*

The Phase Snapshot macro (see section 7.3) will sample the phases of all 8 channel waveforms and write them into the "SNP" register block. Each value is a 32-bit phase snapshot. For example, SNP0H:SNP0L is a 32-bit value ranging from 0x0000:0000 (corresponding to 0 degrees phase) to 0xFFFF:FFFF (359.999… degrees). If desired, the SNPnH (MS) word can be used alone as a 16-bit value, with 0x0000 corresponding to 0 degrees and 0xFFFF equivalent to 359.995 degrees. The values reported are independent of any phase offset added by channel PHAn registers.

The absolute values reported here are generally not useful, as they are taken at a real-time instant that is not tightly controlled. However, the phase differences between channels can be significant in some applications, and user algorithms can be used to walk channel-channel phases into desired relationships.

6.16 *Frequency Counter Registers*

The V340 uses two internal crystal oscillators. A 16-MHz oscillator is the basis for synthesized waveforms, and a separate 20 MHz oscillator is used as the uP clock and the time reference for the internal frequency counter.

The internal counter may be selected to measure the frequency of an external input (J1 pins 22 and 23), the frequency of the signal on the internal BIST bus, or the frequency of the 16 MHz waveform generator clock.

The FTIM register controls frequency counter operation:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		S1	S0				X2	G7	G6	G5	G4	G3	G2	G1	G0

The timebase period over which cycles are counted is set by the contents of the G7...G0 bits of the FTIM register, in units of 100 milliseconds.

Users may set the LS byte of FTIM to any value from 1 to 255, corresponding to frequency counter gate times from 100 milliseconds to 25.5 seconds. For example, when measuring very low frequencies, FTIM may be set to 100, for a 10 second timebase, in which case FRHI:FRLO will report frequency in units of 0.1 Hz.

The upper nibble (encoded S1:S0 bits) selects the signal to be counted. Nibble value 0 selects the external (J1) signal; 1 selects the signal on the internal BIST bus; 2 selects the 16 MHz waveform reference oscillator. The signal on the BIST bus cannot be measured on modules which lack the BIST option.

The system normally counts rising edges of the selected signal. If the user sets the X2 bit, both rising and falling edges are counted, doubling frequency measurement resolution.

At the end of every gate interval, the measured frequency is updated into the register pair FRHI and FRLO, where FRHI is the most significant 16 bits of the 32-bit count and FRLO is the least significant. To ensure skew-free atomic reads, users must read FRHI and then FRLO.

FTIM is set to 0x000A on powerup, so FRHI:FRLO, by default, report the external input frequency in Hz.

To measure an output channel frequency in Hz, one can...

Program a channel to produce a sinewave output of at least 8 volts p-p

Route it to the test bus by setting the appropriate bit in the RELAYS register.

Make sure MODE is set to zero

Load FTIM with 0x100A (select test bus, 1 second gate)

Wait at least one second and read the frequency in FRHI:FRLO.

The PRHI and PRLO register pair reports the frequency input as a 32-bit period, with LSB representing 25 ns. The value is updated once each cycle of the selected frequency-counter input signal and is independent of the selected frequency counter timebase. This period measurement can resolve the frequency of low-frequency inputs faster and with higher resolution than the frequency counter mode. If the input signal stops for more than 1 second, the reported value will jump to 0xFFFF:FFFF. This register pair must be read atomically, PRHI and then PRLO.

If PRHI:PRLO is read as a 32-bit integer P, the signal frequency in Hz is

F = 40e6/P

which has better resolution than a typical frequency-mode measurement for signals in the Hz and low KHz range. The period counter ignores the X2 control bit.

6.17 *Miscellaneous Test Registers*

The VDIPS register shows the realtime states of the X, Y, and Z dipswitches.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
													X	Y	Z

If the Z switch is on, bit 0 will be true and the module will power up in demo mode, as noted in section 4.2. The Y dipswitch, HIZ control, is ignored in demo mode.

If the Y dipswitch is ON at powerup, the HIZ bit will be set in all eight channel control registers, disabling electrical outputs for versions of the module that are equipped with transformers. In this case, users must clear individual HIZ bits to enable outputs. See section 6.9.

The X switch is readable in VDIPS but currently unused.

YCAL is the year of last calibration, an integer of the form 2007 decimal.

DCAL is the month and day of calibration. The high byte is month (1-12) and the low byte is day (1-31).

VZERO is a self-test of the BIST analog-to-digital converter. Its nominal value is 2048.

BLOG is a group of eight registers which furnish diagnostic data if any of the BIST tests fail. See section 8.

7 *Macro Operations*

The macro control register allows the execution of pre-defined macros which perform automatic tasks. Some macros also take or return data in the PARAM0 through PARAM5 registers.

To execute a macro,

Verify that the MS bit (bit 15) of the MACRO register is clear, indicating that the uP is ready to accept a command.

Write any required macro parameters.

Write a 16-bit macro code to the MACRO register.

Wait until the MS bit again clears, or wait longer than the maximum macro execution time. If any other bits are then set, an error has occurred.

Read any returned parameters.

MACRO codes are as follows:

Code	Operation	Max Time
0x8400	No operation	350 us
0x8404	Load Sinewaves into channel wave memory	2 ms
0x8405	Load Sawtooth Waves	5 ms
0x8406	Load Triangle Waves	5 ms
0x8408	Reset channels	400 us
0x8409	Hold channels reset	400 us
0x840A	Update channels	500 us
0x840B	Update+Reset	500 us
0x840C	Snapshot Phases	400 us
0x8410	BIST: test module	15 sec

Code	Operation	Max Time
0x8420	Hard reboot; restarts code; disappears from VMEbus for about 4 seconds	4.8 sec
0x8421	Soft reboot the module; remains on bus.	16 ms

7.1 *Waveshape Load Macros*

All channels power up with sinewaves loaded into their waveform memories. Macros are provided to reload waveform memories with triangle or sawtooth waveforms, or to return to sine waves. To load waveform memories, load macro parameter register PARAM0 with a bitmap naming the channel or channels to be loaded (bits 0 through 7 set will select channels 0 through 7) and then write the appropriate code into the MACRO register. Each of the waveforms spans the full range of amplitude, -32767 to +32767, equivalent to -10.24 to +10.24 volts, scalable by the channel amplitude register.

After running a BIST sequence, all channels will be left in sinewave mode.

Square waves or pulses may be created using the PWM facility.

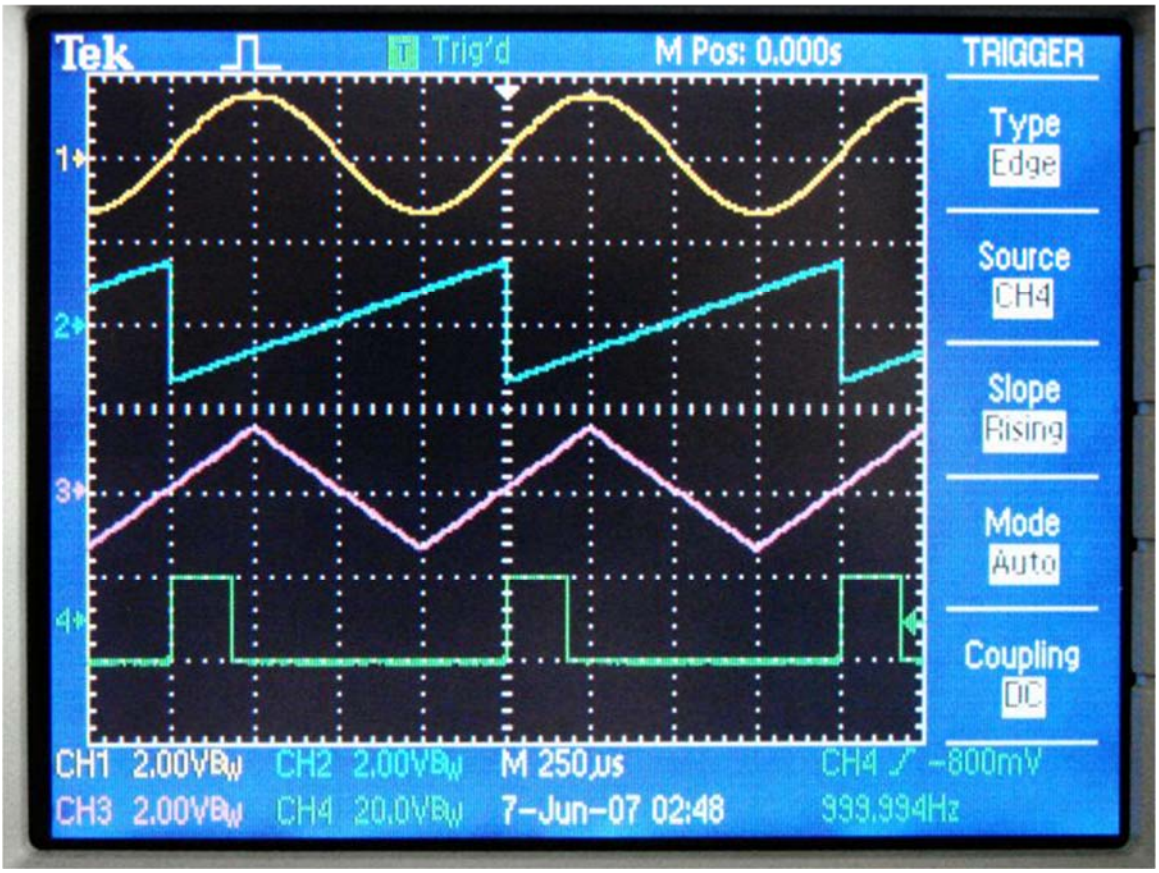


Figure 7

7.2 *Channel Reset and Update Macros*

Each waveform generator defaults to operating in independent mode, wherein any changes to channel settings take place as soon as they are recognized by the normal microprocessor scan. Multiple channels may be coordinated by setting their Sn (synchronous update) bits in the SUBS register, which removes them from the periodic update loop, and then using this group of macros to perform simultaneous, coherent updates of new settings.

Each of these macros accepts one parameter, PARAM0, which is a bitmask specifying which channels are to be acted on. Bits 0 through 7 of PARAM0 enable macro operation on channels 0 through 7 respectively, with any bit combination being legal.

The RESET CHANNELS macro briefly resets the phase accumulators of the named channels, making their waveforms restart at the beginning of their 2048-point waveform memories. Thus all selected channels jump to zero phase angle, offset by any nonzero PHAn register values, and then generate their programmed waveform.

The HOLD CHANNELS RESET macro is like the RESET CHANNELS macro, but the resets are held asserted and all waveforms are frozen at their start phase angle. This static reset state is canceled by a RESET CHANNELS or UPDATE+RESET macro.

In order to initialize a set of channels to be phase coherent, set their SUB register bits (section 6.3), program them as desired, and execute the UPDATE+RESET macro with the appropriate bit mask. All named channels will then be programmed to their new settings and started in phase. Once channels have been started together, subsequent changes can be written, followed by an UPDATE CHANNELS macro, to install the new settings coherently.

See section 10.6 for an example of channel synchronization.

7.3 *Snapshot Phases Macro*

Executing this macro will snapshot all eight phase accumulators and write their 32-bit values into the "SNP" register block; see section 6.15. This macro needs no parameters.

7.4 *BIST Macro*

See section 8.

7.5 *Reboot Macros*

Macros are provided to restart the V340 firmware.

Hard Reboot (0x8420) resets and reconfigures all hardware, and loads all registers to their default values. Total time is about 4.8 seconds, and the module disappears from the VME bus for about the first three seconds.

Soft reboot (0x8421) does not reinitialize the hardware, but sets all registers to their default states. This takes about 16 milliseconds.

Both macros reload all wave memories with sinewaves. Both also read and implement the settings of the DEMO and HIZ dip switches.

For both reboot macros, the MSB of the MACRO register will stay up until the operation is complete. When MACRO returns to zero, the module is ready for use.

8 *BIST*

The V340 features an optional automatic self-test sequence to allow the user to test the functionality of the unit without external equipment and without the need to disconnect field wiring.

Note: BIST is primarily a functional test and checks only approximate quantitative performance limits. It cannot allow absolute verification of module accuracy, as external NIST-traceable standards are required for formal calibration.

Although the BIST operations can detect most module failures, certain errors can be missed. They include:

- Failure of a connector pin or associated printed-circuit traces.
- Failure of a channel test relay.
- Low-order DAC bit errors.

BIST does not test the external frequency counter input or the sync outputs.

Loading the MACRO register with 0x8410 initiates the module self-test. No parameters are required. The BISS register will display test status and the BERR register displays any errors. The full test takes about 15 seconds.

During the test, the green LED will blink rapidly, and the red LED will come on solid for at least one second if any error is detected. After the self-test, all previous module settings will be restored, except that all channels will be loaded with sine waves.

The BISS status register layout is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								BSY							BAV

The BAV bit indicates that the BIST facility is available. BSY is true while the BIST self-test is in progress.

The BERR register flags BIST errors. Bits are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADX	CLX							E7	E6	E5	E4	E3	E2	E1	E0

Bits 7...0 flag errors on respective channels. ADX flags an A/D converter error, and CLX indicates that the DDS reference crystal oscillator is failed or excessively off its correct 16 MHz frequency.

If any error is detected, a diagnostic log is written to "BLOG", VME registers 120 through 127. The values in these registers may be noted and communicated to Highland to determine the specific error and associated measured values. The register functions are as follows:

Register	Function
120	channel ID bitmask, 0 for global tests

Register	Function
121	BERR pattern at time of error
122	error code; see below
123:124	Measured data, DC level in mV for channel tests, long ADC offset for error code 1, 2048 nom Clock frequency for error 2, 1.6e6 nom
125:126	Measured data, AC level for channel tests
127	error counter

Error codes are as follows:

Error Code	Meaning
1	BIST ADC error
2	16 MHz oscillator error
10	channel error, 10 KHz full output amplitude
11	channel error, 10 KHz div10 output amplitude
12	channel error, transformer isolation A
13	channel error, transformer isolation B
14	channel error, bad low ground fault SSR
15	channel error, bad high ground fault SSR
16	channel error, bad signal short SSR
17	channel error, incorrect full-scale transformer output
19	channel error, transformer resonance
21	channel error, +10.24 volts DC out
22	channel error, -10.24 volts DC out

Error Code	Meaning
30	channel error, 100 KHz amplitude
31	channel error, 2 MHz amplitude
32	channel error, lowpass filter rolloff

9 *Calibration Verification*

The calibration of one or more V340 modules may be verified in their operating VME crate.

To verify channel performance and accuracy, the V340 module or modules should be connected to a precision voltmeter/frequency counter, such as the Keithley model 2000. Activate one channel test relay by setting its bit in the RELAYS register; then select module MODE = 1. Now program the selected channel to some known frequency and amplitude, and check the values with the external instrument.

The DVM connection is as follows:

P3 PIN	V340 FUNCTION	DVM CONNECTION
7	CalSig+	INPUT HI
6	CalSig-	INPUT LO

The D9 connector pins of multiple Highland modules may be bussed in parallel to a single precision DVM/counter, provided that only one module is driving the external test bus at any one time.

10 *Operating Examples*

The V340 design intent is to make basic operations simple to program, and more complex modes as direct and transparent as possible. The scenarios below assume that the module is in its default powerup state, or that a module reset macro has been used to equivalently initialize all registers.

10.1 *VME Access*

Before programming the V340, basic VME access should be verified. Set the VME address switches as noted in section 4.1, establishing A16 or A24 access mode and setting the module base address. The V340 is shipped set to base address 0xC000 in the short (A16) address space.

Execute a 16-bit (word) VME read at the module base address, 0xC000 for example. The front-panel blue VME LED should flash and the value read should be 0xFEEE, which is the Highland VXI registered manufacturer's ID. The next register, at base+2 (0xC002 for example) should read back 0x5744, decimal 22340, which identifies the module as a V340.

10.2 *Demo Mode*

To demonstrate basic functionality, set the X and Y dipswitch sections OFF, and set the Z switch on, and then power up the module. All eight channels should output a 1 volt RMS sine wave, with channel 0…7 frequencies being 1…8 KHz respectively.

10.3 *Basic Sinewave Generation*

To make basic sinewaves, it is necessary to load only the channel amplitude control (AMPn) and frequency control (FRHn, FRLn) registers. At powerup, all eight amplitude-set registers (AMP0 through AMP7) are normally (not demo mode) set to zero, and the eight channel frequencies are set to 1 KHz through 8 KHz respectively.

After powerup, to make a sinewave on channel 0, write a 16-bit amplitude setting to the word location AMP0, which would be address 0xC042 for the default setup. If one writes 0x7FFF to AMP0, the maximum sinewave will be generated, 20.48 volts p-p. This 1 KHz sine wave can be measured at J1 pin 1, relative to the low-side (grounded) connector pin 14.

To change the frequency from the default 1 KHz, write to the channel 0 frequency-set register pair FH0 and FL0, as noted in section 6.11. This pair of registers must be loaded in order, FH0 first, then FL0. The frequency will change when FL0 is written.

10.4 *Enabling Transformers*

V340 modules may be optionally equipped with output transformers. The V340-20 and V340-21 have 1:1 transformers, and the V340-30/31 versions have 5:1 step-up transformers.

The module powers up with all channel control registers cleared, which disables transformers, connecting each channel's output amplifier directly to its "high" side output connector pin and grounding its "low" pin. To enable a floating transformer output, set the

XFR bit in the appropriate channel control register. For channel 0, this would entail writing 0x0002 to address base+0x0040 (0xC040 for the default setup.) One could also set the XFR and GFL bits together (0x0006) to implement a transformer-coupled output with the low-side output pin grounded.

10.5 *PWM Outputs*

Each channel may be operated in pulse-width-modulation mode, enabled by setting the PWM bit in that channel's control register. In this mode, the channel outputs a high/low rectangular waveform whose high time is controlled by the value in the channel's PWMn duty-cycle register; see section 6.14.

For example, suppose we want channel 4 to generate a TTL-level (0 to 5 volt) pulse that is 10% high and 90% low. We would…

Set the PWM bit (bit 8) in the CTL4 register to enable PWM mode

Set channel amplitude register AMP4 to 0x1F40 to set output amplitude to 5 volts p-p

Set channel offset register OFS4 to 0x1F40 to add +2.5 volts of DC offset

Write 0x1999 (6553 decimal) to duty-cycle register DC4.

As the channel frequency is changed, the output will maintain the 10% on/off ratio.

If several channels are used in synchronous mode, the PHA4 register could be used to rotate the phase of the PWM pulse relative to other signals.

10.6 *Synchronizing Channels and Phase Control*

The default mode of the V340 is for the eight channels to be operated as independent waveform generators. When any channel parameter is changed, such as amplitude or frequency, the internal microprocessor detects the change and loads the appropriate hardware as soon as possible, usually within 250 microseconds, but with no guaranteed timing. In this mode, channel synchronization is not possible and the values in the channel phase-control registers are essentially meaningless.

In order to coordinate channels, it is necessary to place the channels in synchronous update mode, by setting the appropriate channel-select bits in the SUBS register. Once a channel is in synchronous mode, changes to its parameters will not be installed until the channel is formally "strobed" by an UPDATE or UPDATE+RESET macro command. The macro allows any combination of channels to be strobed together, allowing phase coherence to be enforced.

For example, suppose we want to generate a 3-phase sine wave set using channels 3, 4, and 5. The sequence would be…

Write 0x0038 to the SUBS register to place these channels in synchronous update mode.

Load the identical frequency setting into all three channels. For, say, a 400 Hz system, load FH3 with 0x0001 and FL3 with 0xA36E. Repeat for channels 4 and 5.

Set channel amplitude registers AMP3, AMP4, and AMP5 to the desired values. Writing 0x5863 would set them to 7.071 volts peak, 5 volts RMS.

Set the channel phase-shift registers. To generate standard 3-phase, set PHA3 to 0x0000 (zero shift), PHA4 to 0x5555 (120 degrees lead) and PHA5 to 0xAAAA (240 degrees lead.)

Execute the UPDATE+RESET macro by writing the channel bitmask 0x0038 to the PARM0 register, then writing macro code 0x840B to the MACRO register. Follow the macro handshake procedures noted in section 7.

Executing the macro will install the channel settings coherently, setting up the 3-phase waveform set. Later, one can change channel phases, amplitudes, and frequencies and then execute the UPDATE (0x840A) macro, using the same bitmask parameter, to load the new values. Note that the frequencies must always be updated together to maintain phase synchronization.

If a set of channels are to be run at different but synchronized frequencies, proceed as above but load different frequency settings into each channel. To prevent them from slowly drifting in phase, the 32-bit frequency settings, as loaded into the channel's FHn:FLn pairs, must be in mathematically exact integer ratios.

If we wanted to run channel 7 at exactly 12 times the frequency of channel 6 while still maintaining phase control, we would operate them in synchronous update mode. We would compute the 32-bit FH6:FL6 value for channel 6 and load FH7:FL7 with exactly 12 times that hex value, then UPDATE+RESET with bitmask 0x00C0 to start them in sync. We could later change the frequencies of channels 6 and 7 by loading a new hex frequency setting into channel 6, exactly 12 times that hex frequency value into channel 7, then executing the UPDATE macro with the same bitmask.

Synchronized channels can operate in any waveform or PWM modes.

10.7 *Bidirectional Encoder Simulation*

The PWM mode can be used to simulate a quadrature encoder. As an example, we could simulate a typical quadrature encoder having 1000 counts per revolution. It would output a pair of quadrature square waves, each making 250 cycles per revolution, and would have a third index output that goes high once a rotation. A typical waveform set is shown below. We could use V340 channels 0 and 1 to make the A and B quadrature signals, and channel 2 to make the Z index pulse. We assume a "half cycle index" as shown below.

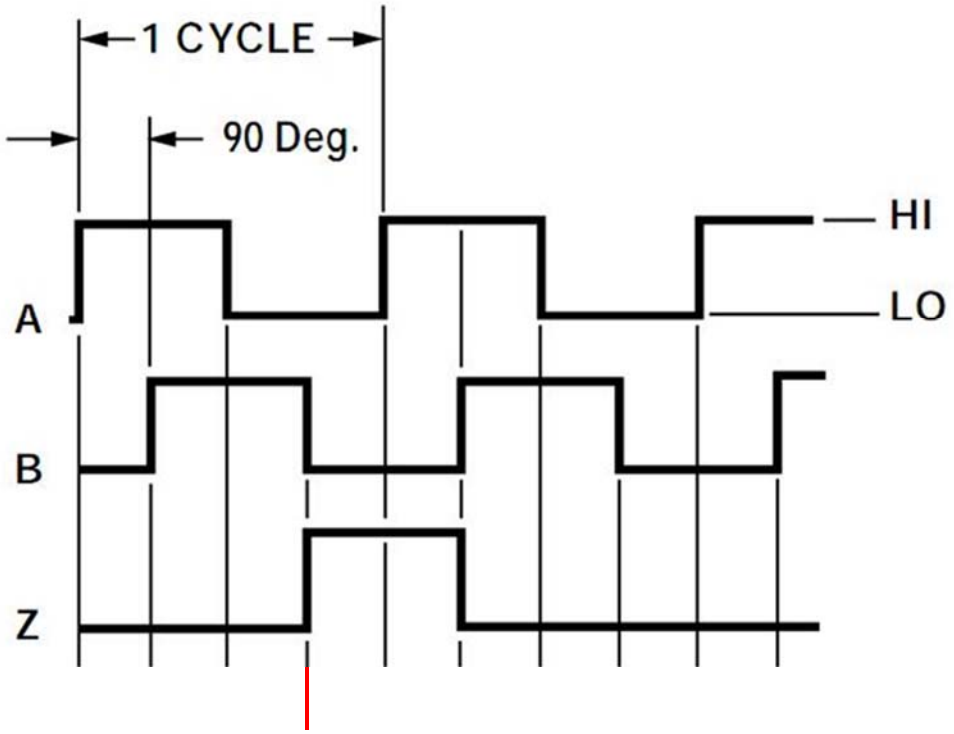


Figure 8. Typical encoder waveform

We could program the V340 as follows:

Set the channels to synchronous mode by writing 0x0007 to the SUBS register.

Hold channels 0, 1, and 2 reset by setting PARAM0 to 0x0007 to select our three channels, then loading the MACRO register with command 0x8409 to hold the channels reset. Follow the macro timing rules of section 7.

Set the channels to non-transformer, PWM mode by writing 0x0100 to CTL0, CTL1, and CTL2.

Set the channels for TTL output levels by writing 0x1F40 to AMP0, AMP1, AMP2, OFS0, OFS1, and OFS2.

Set channels 0 and 1 to 50% duty cycle by writing 0x8000 to PWM0 and PWM1.

The "Z" output (our channel 2) must be high for 1/500 of a rotation for this type of encoder, so set PWM2 to 0x0083, which is decimal 131, namely 65536/500.

Assume we'll start running at 1 revolution per second. Program channel 2, the index, to 1 Hz by setting FH2:FL2 to 0x0000:010C. Set the other two channels to exactly 250 times this frequency by setting FH0:FL0 to 0x0001:05B8; repeat for FH1:FL1.

Set the channel phases:

0 degrees for index channel 2:	write 0x0000 to PHA2.
90 degree lag for channel 0:	write 0xC000 to PHA0
180 degree lag for channel 1:	write 0x8000 to PHA1

Start the simulation running by writing 0x0007 to PARAM0 (to select our channels again) then writing command 0x840B (UPDATE+RESET) to the Macro register, again following the macro handshake protocol. The encoder will begin at phase angle 0 and simulate clockwise rotation at 1 revolution per second. Speed can be changed, or reversed, by coherently changing the three frequency settings and then executing the UPDATE macro. The frequency control words of channels 0 and 1 must always be numerically exactly 250 times the value of channel 2.

The V340 has no direct mechanism for slewing channel phases to absolute angular positions. Users can implement algorithms which read channel phases, using the phase snapshot macro, and dynamically adjust channel frequencies to converge on and stop at a desired absolute angular position.

The A and B channels could be used in sinewave mode by not setting their PWM control bits. This would simulate an encoder that has quadrature sine outputs.

10.8 *Synchro/Resolver/LVDT Simulation*

Synchronized channels can be used to simulate the excitation and outputs of synchros, resolvers, LVDTs, or RVDTs. Note that the V340 cannot accept external excitation, so one channel must be used to generate the simulated excitation signal.

10.9 *DC DAC Outputs*

Any V340 channel can be used as a simple DC output DAC. Program the channel AMPn sinewave amplitude register to zero, then use the DC offset register OFSn to set the output level.

11 *Versions*

Standard parts include:

V340-10: 8-channel VME function generator

V340-10 8-channel VME function generator

V340-11 8-channel VME function generator with BIST

V340-20 8-channel VME function generator with transformer coupling with switchable 1:1 transformers

V340-21 8-channel VME function generator with transformer coupling with switchable 1:1 transformers and BIST

V340-30 8-channel VME function generator with transformer coupling with switchable 5:1 transformers

V340-31 8-channel VME function generator with transformer coupling with switchable 5:1 transformers and BIST

The module version is indicated on the serial-number label on the circuit board, and may also be read in the VXITYPE and DASH registers.

12 Customization

Consult factory for information about additional custom and OEM versions, or for custom PCB laser interposer boards.

13 Hardware Revision History

13.1 *Hardware Revision History*

Revision D	Feb 2010 Rev D fixes noise level on previous revisions. Layer definitions differ from previous revisions.

Revision C Nov 2009
No functional changes, manufacturability improvements only.

Revision B May 2007
Improves LP filters and testability.

Revision A Jan 2007
Initial PCB release.

13.2 *Firmware Revision History*

The standard firmware is version 22E340. Firmware is stored in a plugin EPROM chip which may be upgraded in the field. The firmware version is shown on the label of the EPROM chip and may also be read in the ROMID and ROMREV registers.

Revision D May 2017
Fixes BIST test limits for transformer resonance.

Revision C June 2014
Fixes BIST test limits for peak detector tests.

Revision B Dec 2009
Fixes BIST test limits for transformer amplitude.

Revision A Oct 2007
Initial firmware package.

14 Accessories

J340 Sync signal termination board, with eight SMB connectors, with removable DIN rail clips.

J51 Shielded-pair SCSI cable for connecting V340 SYNC connector to the J340. Length 1 meter.

J52 J51-type SCSI cable, length 2 meters

J34 Waveform and frequency counter breakout cable, with 9 coax cables terminating in BNC male connectors, length 1 meter.

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