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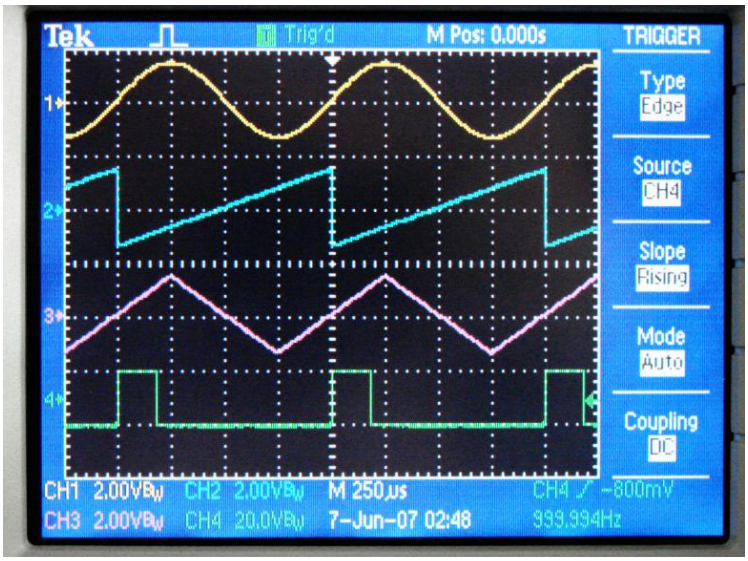
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HIGHLAND TECHNOLOGY



V344/V346 VME WAVEFORM GENERATOR



Technical Manual

May 13, 2015

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1. Introduction

This is the technical manual for the Highland Model V344 and V346 eight-channel 32 MHz waveform generator VME modules.

Features of the V344/V346 include:

- 8 channels of sine, sawtooth, triangle, square/pulse/PWM, Gaussian noise, or arbitrary waveform generation.
- Simple programming procedures for basic waveform generation.
- Any-to-any channel summing.
- Channel-channel synchronization within one module or across up to 16 modules in one crate; expandable to an unlimited number of channels of synchronized waveform generation.
- Generates Gaussian noise with programmable bandwidth, 0 to 2 MHz.
- Selectable output frequency ranges, 0-32 MHz with 0.015 Hz resolution to 0-250 KHz with 166 uHz resolution. Functional past 40 MHz.
- DC coupled 50-ohm outputs to 10.24 volts peak to peak.
- Programmable offset allows wave+offset or direct DC DAC functionality.
- Programmable channel phase allows quadrature or polyphase waveforms.
- Programmable digital pulse/PWM outputs can simulate transducers or quadrature encoders, or drive switchmode H-bridges with complex waveforms.
- Auxiliary connector provides waveform sync outputs and digital expansion.
- External TTL inputs can reset, update, or synchronize channels or initiate single-shot waveforms, for single boards or across multi-board systems.
- Includes channel test connector, allowing in-crate check of channel performance without removing field wiring.
- Built-in self-test (BIST).

Only available on the V346 are:

- Any-to-any channel modulation: AM, FM, PM, and PWM.

- Noise modulation allows calibrated jitter.

- Control channels allow complex sequences of operations to be generated in real-time across multiple channels on one board or many.

The signal-processing capability of the V346 is sufficiently general that a wide range of complex functions can be easily programmed from the "first principles" of signal/systems theory. This includes quadrature signal generation, DSB/SSB of arbitrary waveforms, sweeps and chirps, QAM/constellation generation, frequency hopping, FSK generation, multichannel frequency tracking, and quantitative control of noise and jitter.

One or more V346 modules may also be used to simulate complex, high-channel-count processes, such as radar and sonar arrays, complex rotating machinery and structural systems, diesel/jet engine simulation, stationary and aircraft AC power systems, thyristor/IGBT phase control, and many others.

The ability to generate complex modulated waveform sets, and then convert to PWM drive at any desired carrier frequency, allows versatile, direct generation of servo motor or AC vector drives. V346 PWM outputs may be converted to fiberoptic drive using Highland's VME and standalone electrical/optical converter products.

Electrical and fiberoptic expansion hardware is available to permit the synchronization of an unlimited number of V346 modules, allowing the generation of hundreds or thousands of channels of phase-coherent waveforms.

The T346, a compact stand-alone, non-VME, RS-232/Ethernet controlled version of the V346, is also available for embedded applications.

This manual applies to the V344-1A and V346-1A versions

Related products include…

- V340 VME 8-channel, 2 MHz waveform generator with optional transformer coupling

- V347 VME Global Synchronization fanout module for the V346

- J346 Global Sync bussing strip for 2-16 V346 modules

- T340 Compact embedded 4-channel waveform generator with RS-232/Ethernet interfaces

- T344 Embedded 4-channel version of the V344.

- T346 Embedded 4-channel version of the V346.

2. Specifications

2.1. General

FUNCTION	8-channel VME 32 MHz arbitrary waveform generator
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16 Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
CYCLE TIME	200 ns typical
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies: +5 V, 1.5 A max +12 V, 750 mA max -12 V, 750 mA max
CONNECTORS	SMB jacks for channel/test outputs, clock input, and SYS bus (SMA and LEMO connectors available by special order) 50-pin SCSI-type female for AUX outputs
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes

2.2. Channel Outputs

STANDARD WAVEFORMS	Sine, sawtooth, triangle, Gaussian noise, or square/pulse/PWM outputs
ARBITRARY WAVEFORM	4096 point, 16 bit user-loadable arbitrary waveform with programmable hardware interpolation
SIGNAL SWING	Normal range: ±5.12 V ± 1% Attenuated range: ±1.024 V ± 1%
IMPEDANCE	50Ω nominal output impedance
DC OFFSET	±2 mV typ, 15-35°C ±10 mV max, 0-60°C
GAIN ERROR	±0.5 % max
FLATNESS	-0.1 dB @ 12 MHz typical -1 dB @ 32 MHz typical -3 dB @ 46 MHz typical Amplitude rolls off monotonically with frequency
DAC RESOLUTION	14 bit DAC output resolution
FREQUENCY RANGES	High range: 0 to 32 MHz with 0.0149 Hz resolution Mid range: 0 to 4 MHz with 0.0018 Hz resolution Low range: 0 to 250 KHz with 116 µHz resolution
PHASE RES.	1/65536 cycles ≈ 0.0055°
PWM DUTY RES.	1/65536 ≈ 0.15%
GAUSSIAN NOISE	Programmable amplitude 0 to 1 V RMS, programmable 3 dB bandwidth 0 to 2 MHz
SUMMING	Any channel may be summed with the output of channel 1 to 7, cascadable in any groupings Sums may be modulation sources
MODULATION (V346 ONLY)	Any channel may be amplitude, frequency, phase, or PWM modulated by the outputs of channels 1–7, in any combination

2.3. Clock Input

FREQUENCY	10 MHz ± 50 ppm
SIGNAL SWING	0.2V to 5V
INPUT LOAD	Series 1KΩ + 2.2 µF

2.4. AUX Connector

SYNC OUTPUTS	0 to 5 V square wave; ±24 mA max
TTL COMMAND	Programmable edge sensitive input
TTL RESET	Programmable level sensitive input
TTL INPUTS	V_H = 2-5 V. V_L = 0.7-0 V. ±10 µA max

2.5. SYS Bus

BUS FREQUENCY	8 MHz
EDGE RATE	0.9 ns typical
VOLTAGE	0-3.3V unloaded, 0-2.8V with 50Ω termination

3. Connectors and Installation

3.1. Address DIP Switches

Four 4-position rocker-type dipswitches are provided near the top edge of the board. The address switches are labeled "A23" through "A9" and finally "A24M". The V344/V346 occupies 256 words (512 bytes) of VMEbus space, so bus addresses are multiples of 0x0200.

To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, address switches A23 through A9 are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space.

3.2. Installation

The V344/V346 may be installed in any VME (IEEE 1014) crate, including VME64 variants. It uses only the P1 backplane connector

The V344/V346 passes all interrupt and bus grant signals, so may be used with backplane grant jumpers installed or not installed.



CAUTION: Do not install or remove the V344/V346 with crate power on. VME modules are not hot-pluggable. The V344/V346 will be damaged if hot-plugged.



CAUTION: Fully seat the module and secure front-panel screws before applying power.



CAUTION: Handle the V344/V346 with proper ESD precautions to avoid static damage.



CAUTION: Do not apply voltages to any V344/V346 outputs.

3.3. Connectors

3.3.1. Channel Output SMB Connectors

The front-panel provides eight SMB signal output jacks. They are, from bottom to top:

Connector	Signal
C0	Channel 0 output
C1	Channel 1 output
C2	Channel 2 output
C3	Channel 3 output
C4	Channel 4 output
C5	Channel 5 output
C6	Channel 6 output
C7	Channel 7 output

The connector shells are VME board/system ground.

3.3.2. SYS Global Synchronizing Connector

The front-panel "SYS" SMB jack is used to globally synchronize multiple V344/V346 modules. A 50-ohm connection path is established from one master module, daisy-chaining through a number of slaves, with the physically last slave programmed as a terminator.

A pair of modules may be connected with a simple short SMB-SMB coaxial cable, connecting the SYS jacks on both modules. Groups of modules may use the Highland model J346 bussing assembly, which ensures a proper impedance match for bussing two to as many as 16 modules in a single VME crate.

The global SYS connection is used to lock slave module crystal oscillators to the master module, and also distributes Global Event commands to allow control of coherent waveform sets across multiple modules. Both electrical and fiber optic buffers are available to extend global synchronization to an unlimited number of channels.

3.3.3. TEST Connector

Channel outputs may, under software control, be diverted by test relays into the front-panel "TEST" SMB connector. This allows for testing and in-system calibration without having to disconnect the normal operation field wiring.

3.3.4. CLOCK Connector

A front-panel CLOCK connector is provided to allow the application of an external precision 10 MHz clock. The V344/V346 may be programmed to phase-lock to this clock.

The connector is an SMB jack. It accepts a sine, square, or TTL level from 0.2 to 5 volts p-p. The input impedance is about 1K ohms, and the signal is bandpass filtered to make it relatively immune to waveshape and ground loops.

3.3.5. AUX Connector

The front-panel female 50-pin female SCSI-type connector has provision for 16 TTL data lines and four control lines. For the versions referenced by this manual, only eight outputs and two inputs are used.

Connector pinout is…

Pin	Function	Pin	Function
17	Sync Output 0	42	Ground
16	Sync Output 1	41	Ground
15	Sync Output 2	40	Ground
14	Sync Output 3	39	Ground
13	Sync Output 4	38	Ground
12	Sync Output 5	37	Ground
11	Sync Output 6	36	Ground
10	Sync Output 7	35	Ground
20	TTL Reset Input	45	Ground
21	TTL Event Input	46	Ground

The paired pins correspond to the twisted pairs of a standard SCSI cable. The grounds are PCB/VME ground. Individually-shielded-pair SCSI cables are recommended to minimize crosstalk.

Each sync signal is a 5-volt TTL/CMOS logic level square wave which rises at the positive-going zero crossing of its respective waveform generator. It is essentially the inverted MSB of the respective phase accumulator. The sync outputs are picked off before any channel phase rotations are applied.

Any channel may be programmed to accept the TTL RESET input on pin 20. The channel's phase accumulator will be held statically reset when this signal is in the selected active level, as determined by the TTLCTL register..

Pin 21, the TTL EVENT input, is edge-sensitive. Its functionality is determined by the TTLCTL register. A rising or a falling edge may be programmed to create either a Local or a Global Event, and the "content" of the event is also defined in the control register.

The SCSI connector shell is bonded to the VME front panel, which connects to the crate frame through the module securing screws. The V344/V346 does not make a DC connection between front-panel ground to VME ground.

3.4. Available Accessories

The following V344/V346 accessories are available:

J340	Sync signal termination board, with eight BNC connectors. Includes removable DIN rail mounts.
J51	Shielded-pair SCSI cable for connecting V346 SYNC connector to the J340. Length 1 meter.
J52	J51-type SCSI cable, length 2 meters
J54-1	Short SMB-SMB cable for global sync of two modules.
J346-n	Global bussing assembly for 'n' modules

4. Basic Operation and Concepts

4.1. Channel Architecture

The V344/V346 includes 8 independent DDS-based waveform generators. Channels are numbered 0 through 7. Channels are independently programmable for waveform, frequency, amplitude, phase, and DC offset. Any channel may be AM/FM/PM/PWM modulated by the outputs of channels 1-7. Any channel may have the output of channel 1 through 7 summed into its output, thus any set of channels can be summed in a cascade.

Figure 4.1 summarizes the signal paths of one channel. Channels are identical except that channel 0 cannot be used as a source for modulation or summing.

DDS, or direct digital synthesis, starts out with a frequency tuning word. This frequency tuning word (FTW) is then accumulated over and over again to create a steadily increasing instantaneous phase. The higher the FTW, the faster the phase increases. The phase accumulator is allowed to overflow as it happens, corresponding to the rotation from 359° back to 0°. From here, the V344/V346 provides a dedicated phase rotation adder which provides an additional phase. This allows, for example, two channels to run 90° out of phase; their phase accumulators would remain in lock step, but they would have different phase rotations.

The phase accumulator is also used to generate roughly 50% duty square waves on the SYNC0-SYNC7 pins of the AUX connector, with the rising edge corresponding to the positive transition through 0 phase.

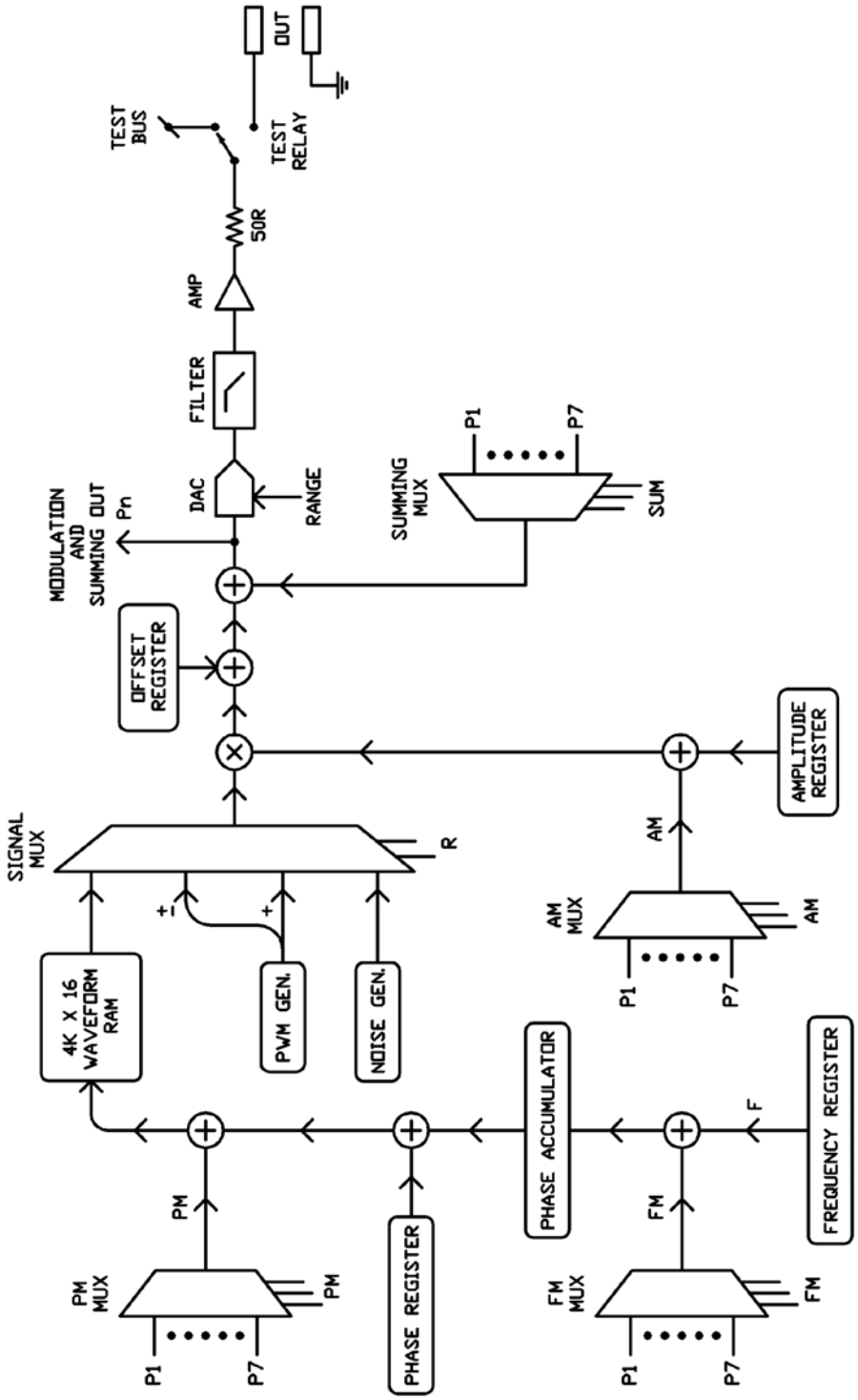


Figure 4.1 – Channel Signal Flow

After phase rotation is applied, the resultant instantaneous phase is used to look up the appropriate instantaneous value from the waveform. Most frequently, this is done by truncating to only the most significant bits of the phase, and then taking this as an address into a RAM-based wavetable. For illustration purposes, Figure 4.2 shows a sine wave as represented in a 64 point wavetable. This would correspond to using the top 6 bits of the phase; if these bits were `110000` (48 in decimal), then the trough of the sine wave would be output.

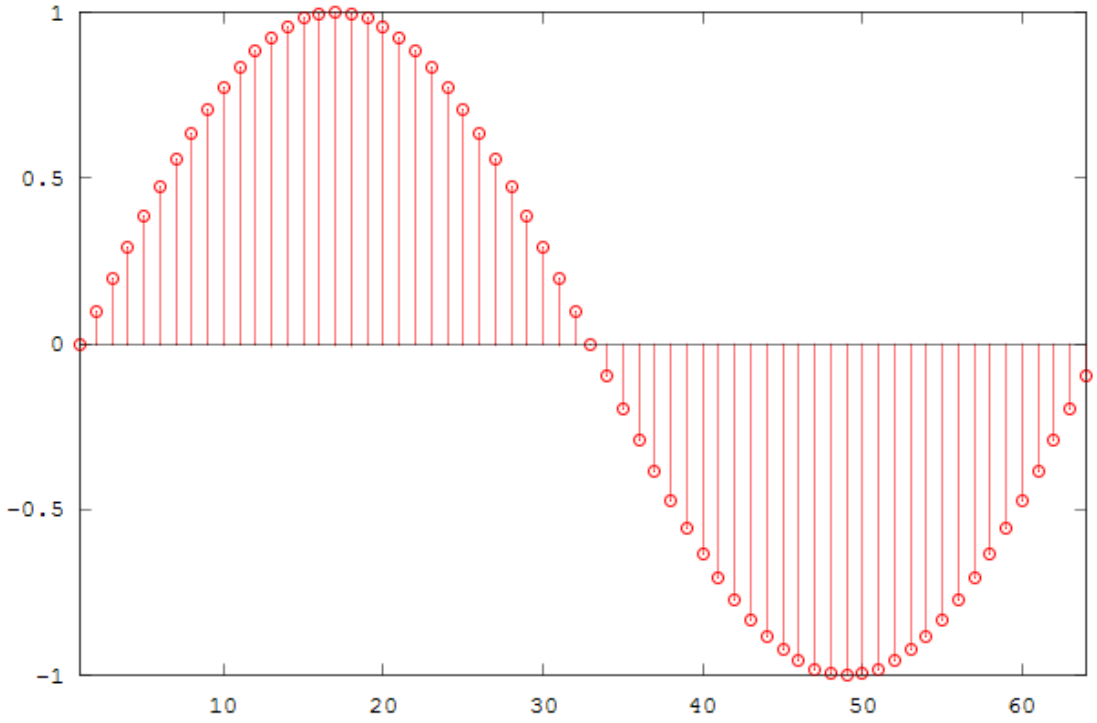


Figure 4.2 – 64 point sine wave

In the case of the V344/V346, the most-significant 12 bits of the phase are looked up in a 4096 point wavetable, providing points that are less than 0.1° apart. In order to improve further on this performance, the V344/V346 offers the option of linear interpolation, which uses additional bits of the phase to interpolate between adjacent points in the wavetable, increasing the effective wavetable size. The PWM modes bypass this wavetable entirely to work with 16 bits of phase for finer control over the duty cycle.

For optimal performance, the waveform stored in the wavetable should be stored occupying the entire available amplitude resolution. For the V344/V346, the signed 16-bit wavetable allows each point to be represented in the range ±32767, corresponding to negative and positive full scale, respectively. After being looked up, each waveform sample is scaled down by the fractional amplitude multiplier and added to the DC offset before being output by the high-performance digital to analog converter. Other channels can also be summed with this one as described in section 6.1.1 - Summing Channels. Should either channel summing or a DC offset cause saturation, the waveform will clip flat rather than overflow.

4.2. Macros

The V344/V346 is able to execute a set of commands known as macros. These macros perform tasks such as writing data into channel waveform memory, taking a snapshot of the phase of all of the channels, resetting channels, and performing the module's built-in self-test.

Macros are executed by first writing a set of parameters to the PARAM0-PARAM5 macro parameter registers. The meaning of these parameters, and the number required, will vary by macro. Some macros, such as the Write Waveform Memory macro, will also require you to write a block of data into the BUFFER registers. Once the parameters and data have been written, the macro can be executed by writing the correct macro command code into the MACRO register. The V344/V346 will then execute the macro, and write a macro return code back into the MACRO register, overwriting the macro command code. All macro command codes have bit 15 set, and all macro return codes have bit 15 clear, so when the MACRO register no longer has the MSB set, the macro is done executing. The macro may return data by writing it into the BUFFER registers, such as the Read Waveform Memory macro.

The use of the macro registers, and the full list of macro commands, is available in section 10.5, and examples of macro use will occur throughout this manual.

4.3. Events

The V344/V346 provides an advanced system control architecture known as Events. Using Events, channels can be controlled by:

- External TTL signals
- Immediate commands, initiated by a VME write to a different V344/V346 and broadcast down the global SYS bus.
- A TTL signal or control channel on a different V344/V346, broadcasting down the global SYS bus.

- A command or a control channel originating on a T344 or T346 small form-factor arbitrary waveform generator, broadcasting down the global SYS bus.

- Timed sequences being generated by a channel on the same V346 that has been configured as a control channel. Channels 6 and 7 can be used as control channels on V346 units only.

By using Events, complex interactions between channels on one V346, channels on several V344/V346s, external hardware, and the VME bus can all be managed.

Events work by an address based message system. First each channel to be managed through Events must be given an address. The ADDR0-ADDR7 registers each hold two 8-bit channel addresses (CADs) for channels 0-7 respectively. Having two CADs available per channel allows for the ability to provide channel groupings as well. For instance, channels 0-3 could be assigned CADs 0-3 respectively, but all of them could also be assigned to CAD 10. Channels default at power up to having both CADs set to 0.

An Event is broadcast to all channels, either locally on one module or globally across the SYS bus, with both an event code specifying the action to be taken and a target address (TAD). Each channel that has the Accept Events bit of its channel control register set then checks to see if either of its CADs matches the Event TAD, and if so, takes the action specified in the event code. In the previous example, sending an event with TAD 2 would only trigger channel 2, but sending an event with TAD 10 would trigger channels 0-3, and an event with TAD 11 would be ignored by all channels.

An Event with TAD 255 is special, and known as a Broadcast Event. Broadcast Events are accepted by all channels that have their Accept Events bit set, regardless of CAD settings. Likewise, any channel with both CADs set to 255 will respond only to Broadcast Events.

An Event that is sent locally will be sent only to channels on the V344/V346 where it originated. An Event sent globally on the SYS bus will be sent to all channels on all units on the bus. This allows a system master to trigger an Event on a channel or channels on one or more different units. Thus a master could simultaneously reset channels on both itself and a slaved board, or even exclusively on channels on slaved boards, by sending a command with the right TAD.

4.4. Control Channels

In order to allow for complex sequences of Events, channels 6 and/or 7 of the V346 can be turned from their normal role as signal output channels into Control channels: generators of Events rather than of waveforms. These Events can be targeted to individual channels or groups of channels, just like any other, and can be made to generate Events either only on the local board, or globally across the SYS bus, selectable on an Event by Event basis. The timing of the entire sequence can be stretched or shrank by adjusting the channel frequency,

Because they remain channels, Control channels can be triggered by Events the same as any other. This allows for such applications as:

- Generating a complex Event sequence upon a rising TTL edge.
- Walking through a long sequence of Events, one per TTL edge, without real-time reprogramming.
- Generating periodic, slow events from a SYS master that trigger fast Event sequences on local boards.

Information on programming Control channels can be found in section 6.3.7. Control channels are not available on the V344.

4.5. VME Interface

The V346 occupies 256 16-bit VME registers. DIP switches are provided to set the base address to any 256-word (address 0x0200) boundary in the A16 or A24 address spaces. All registers are implemented as true dual-port memory which is shared between the VMEbus and the internal microprocessor.

VME access time is typically 200 ns, measured from DS* to DTACK*.

The module is normally shipped configured for base address of 0xC000 in the A16 address space.

Certain register pairs represent 32-bit values and must be written or read as one atomic unit to ensure that updates do not create skew errors. Atomic pairs must be written in the order MS:LS, and will not be effective until the LS word is written. Similarly, atomic pairs must be read in the same order, MS:LS.

The V344/V346 does not support single-byte writes from VME.

Although the V344/V346 has many signal-processing features, the user interface allows basic waveform generation to be done with a minimum of programming; after powerup, it is only necessary to write to the channel frequency and amplitude registers to produce basic sinewave outputs. Chapter 9 of this manual presents operating scenarios from this basic sinewave generation up through the more complex modes.

4.6. Front-Panel LEDs

The blue VME LED will flash whenever the V346 is addressed from the VMEbus.

The green CPU LED will blink once about every two seconds to indicate that the internal firmware is operating normally. See section 7.3.4 for notes on LED operation during BIST.

The red ERROR LED will normally be off. It will flash if any error flags are set. Blinks patterns are…

one blink	channel programming, summing, or modulation error
two blinks	error phase locking to master or 10 MHz source
three blinks	calibration table or BIST adc error
four blinks	serious hardware error

The orange USER LED may be programmed from the VMEbus.

5. Controlling Individual Channels

5.1. Channel Registers

	0x_0	0x_2	0x_4	0x_6	0x_8	0x_A	0x_C	0x_E
0x04_	CTL0	AMP0	FH0	FL0	OFS0	PHA0	PWM0	MOD0
0x05_	CTL1	AMP1	FH1	FL1	OFS1	PHA1	PWM1	MOD1
0x06_	CTL2	AMP2	FH2	FL2	OFS2	PHA2	PWM2	MOD2
0x07_	CTL3	AMP3	FH3	FL3	OFS3	PHA3	PWM3	MOD3
0x08_	CTL4	AMP4	FH4	FL4	OFS4	PHA4	PWM4	MOD4
0x09_	CTL5	AMP5	FH5	FL5	OFS5	PHA5	PWM5	MOD5
0x0A_	CTL6	AMP6	FH6	FL6	OFS6	PHA6	PWM6	MOD6
0x0B_	CTL7	AMP7	FH7	FL7	OFS7	PHA7	PWM7	MOD7

All of the basic tasks involved in controlling individual channels are performed on the channel registers. These control the basic parameters for a given channel: frequency, amplitude, phase, etc. The first of these is the channel control register for channel 0, called CTL0 and located at offset address 0x40. The last is the modulation control register for channel 7, MOD7, located at offset address 0xBE.

5.1.1. CTLx - Channel Control Registers

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OS	IN	R1	R0	D5	K2	K1	K0		S2	S1	S0	TR	AE		SY

Each of the 8 waveform generators has an associated channel control register, CTL0 through CTL7. The channel control register controls aspects of the channel that are less involved with the generation of waveforms, and more its management.

If the SY bit is clear the channel operates in auto-update mode. In this case, any changes written to any channel registers are installed automatically and asynchronously. This is the powerup default mode, wherein channels operate independently. This is generally the simplest mode to get started with, but makes it difficult to synchronize channels. Set the SY bit to use Synchronous Update Mode, which holds onto to parameter updates until given an Update Channels macro, then commits them all at once. This is important when using any of the channel synchronization mechanisms, discussed in later chapters.

Setting the AE bit allows this channel to accept Events, namely to be updated, reset, triggered, and phase snapped coherently with other channels, on one or many modules, using either TTL Events, command channel Events, or Events broadcast on the SYN bus.

If TR is set, this channel can be held in reset by an external signal on the front-panel TTL RESET pin. This is independent of the Accept Events setting.

The three Sn bits allow channel summing. If the encoded value "S" is nonzero, then the output of channel S is summed into the output of this channel. See section 6.1.1 for details on channel summing.

The two R bits set a frequency range for this channel. Ranges are:

Rcode	R1	R0	Frequency Range	LSB Resolution
0	0	0	± 32 MHz	14.90 mHz
1	0	1	± 4 MHz	1.836 mHz
2	1	0	± 250 kHz	116.4 uHz
3	1	1	± 64 MHz	29.80 mHz

Note that the 64 MHz range operates beyond the module's specified performance. The post-synthesizer lowpass filters are 7th order transitional Gaussian, with a 3 dB point of about 40 MHz, after which gain drops off rapidly with frequency, phase shift increases, and image/spur performance degrades. Given these constraints, frequencies up to at least 40 MHz can be generated. Do not use this range in noise generation mode.

If users leave the D5 bit low, the channel full scale output range is ± 5.12 volts peak (3.62 volts RMS), as scaled by the channel amplitude register. If this bit is set high, an analog 1/5 divider reduces the full scale amplitude to ± 1.024 volts peak. Because this is an analog division, the channel output DAC retains its full resolution, allowing for lower signal levels without quantization artifacts. This affects this channel's analog outputs only, not any internal modulation or summing paths.

In addition to playing the waveform programmed into the wavetable, channels can be switched over to provide either a pulse/PWM signal or programmable bandwidth Gaussian noise, both of which are generated by dedicated hardware. The "K" bits control the channel signal source multiplexer.

Kcode	K2	K1	K2	Waveform
0	0	0	0	RAM: Waveform RAM is signal source. This is used for standard wave shapes and for arbitrary waveforms. See section 5.2.1 for information on the standard waveforms, and 5.2.2 for using arbitrary waveforms.
1	0	0	1	BPWM: Use the PWM generator in bipolar mode, with output 0x8001 as "low" and 0x7FFF as "high". See section 5.2.3.
2	0	1	0	UPWM: Use the PWM generator in unipolar mode, 0x0000 "low" and 0x7FFF "high". See section 5.2.3.
3	0	1	1	GAUS: Use the Gaussian noise generator. See section 5.2.4.
4	1	0	0	STEP: Single stepping through waveform RAM is signal source. See section 5.3.2.
5	1	0	1	CNTL: Channel is acting as an Event source rather than a waveform generator. See section 6.3.7. This mode is only available on the V346, and is reserved on the V344.
6	1	1	0	(reserved for future use)
7	1	1	1	(reserved for future use)

If users set the IN bit, waveform table interpolation is enabled. This allows the channel to generate additional virtual points in the wavetable and reduces frequency-domain spurs. Interpolation only operates in R=0 (wave ram source) mode. Enabling interpolation can soften steep rising and falling edges.

If the OS bit is set, the channel operates in one-shot mode. Following a local or global FIRE Event, the phase accumulator will run for one full cycle, making one pass through the waveform memory (or one PWM pulse) and then return to address 0, essentially parking on the 0th wave table entry. See section 5.3 for more information on using one-shots.

At power-up, all eight channel control registers are loaded with 0x0000, and wave tables are set to sine waves, so all channels operate in normal, sine wave mode, 32 MHz range, with maximum programmable output of 10.24 volts p-p, and operate in asynchronous update mode.

5.1.2. AMPx - Channel Amplitudes

Each of the 8 waveform generator channels has an amplitude-set register, AMPn. If the D5 bit is low, channel amplitude may be programmed from 0 up to +-5.12 volts (10.24 volts p-p sinewave amplitude) over the AMPn range of 0x0000 to 0x7FFF.

The AMPx registers are signed, so negative 2's complement values invert the phase of the outputs; 0x8000 is full-scale inverted output. This can be useful in phase-synchronized or PWM modes.

If a waveform memory point is treated as a signed fractional between +1 (0x7FFF) and -1 (0x8000) and the AMPx register is identically scaled, front-panel output will be 5.12 volts times the product of these two values, adjusted by any offset or summing subsequently applied,

If the control register D5 bit is set, analog outputs are attenuated by 5:1. Internal modulation and summing paths are not affected.

All eight amplitude-set registers power up at zero.

5.1.3. FH:FLx - Channel Frequency-set Registers

Each of the 8 waveform generator channels has a pair of frequency-set registers FHn and FLn. These can be treated as a 32-bit signed integer *N*, with the relationship that:

$$\frac{N}{2^{31}} = \frac{F}{F_{MAX}}$$

Where *F* is the desired output frequency, and F_{MAX} is the maximum frequency specified by the range bits: 32 MHz, 4 MHz, 250 kHz, or 64 MHz.

With this in mind, the resulting frequency on the default 32 MHz range, will be...

$F = N * (32{,}000{,}000 / 2^{31})$ Hz or
$N = F * (2^{31} / 32{,}000{,}000) = F * 67.108864$

which corresponds to an LSB value of about 0.0149 Hz. The maximum positive value is of *N* is 0x7FFF:FFFF, equivalent on the 32 MHz range to 31.999,999,985 MHz.

The pair of frequency-set registers is atomically interlocked to ensure coherent 32-bit writes. A register pair must be written in the order FHn followed by FLn. The actual frequency will be updated after the FLn register is written. At power-up, the channel 0 through 7 frequencies are set to 100 through 800 KHz respectively, so writing channel AMPn registers will result in immediate sine wave outputs.

For example, to generate a 1 KHz sine wave on channel 0 (set to 32 MHz range), calculate *N* = 67,108.9 ≈ 67,109, which is 0x10625 in hex. Therefore, set FH0 to 0x0001 and then set FL0 to 0x0625.

If phase coherence is required between two or more channels, several conditions must be followed, then channel frequency set registers must be the same or **exact** multiples, and channels must be configured and then reset together. Procedures for doing this are discussed more thoroughly in section 6.3.2 - Maintaining Phase Relationships.

Frequencies in the range of 0 to 31.999… MHz correspond to FHn:FLn register pair values from 0x0000:0000 to 0x7FFF:FFFF. It is also possible to program negative frequencies in the range of, equivalently, 0 to -32 MHz, corresponding to 0x0000:0000 through 0x8000:0000; simply negate the 32-bit FHn:FLn hex value. Negative 2 MHz thus corresponds to 0xF000:0000.

A negative frequency corresponds to a decreasing, rather than increasing, phase, or walking a waveform table “backwards”, which would reverse the phase relationship of polyphase sine wave or PWM outputs. One could effectively run a simulated 3-phase alternator or quadrature encoder clockwise at positive frequency settings and counterclockwise at negative frequency settings.

Some common frequency settings are…

Frequency	**Frequency Range**	**FH : FL**	**FH : FL in Decimal**
1 Hz	32 MHz (0)	0000:0043	67
1 Hz	250 kHz (2)	0000:218D	8,589
60 Hz	32 MHz (0)	0000:0FBB	4,027
60 Hz	250 kHz (2)	0007:DD44	515,396
100 kHz	250 kHz (2)	3333:3333	858,993,459
100 kHz	4 MHz (1)	0333:3333	53,687,091
100 kHz	32 MHz (0)	0066:6666	6,710,866
1 MHz	4 MHz (1)	2000:0000	536,870,912
1 MHz	32 MHz (0)	0400:0000	67,108,864
16 MHz	32 MHz (0)	4000:0000	1,073,741,824

Note that of the frequencies shown, the 1 MHz, 4 MHz, and 16 MHz points are exact and the other values are all rounded to the nearest LSB, so do not precisely hit the specified frequencies. Also, note that lower frequencies use up more of the FH:FL register, and therefore have better resolution, on lower frequency ranges.

5.1.4. OFSx - Channel DC Offset Registers

Each channel has an OFSn register which allows users to add a DC offset to the waveform output. The register defaults to zero for zero volts of offset. A setting of 0x7FFF adds the maximum positive offset, +5.1198 volts, and 0x8000 applies an offset of -5.12 volts. If the active waveform and the offset sum to over ±5.12 volts, the DAC output will appropriately clip at its maximum output and a channel flag will be set in the CLIPS register. If the D5 control bit is set, scaling the outputs down to ±1.024V fullscale, then the DC offset and clipping ranges are scaled down to ±1.024 as well.

If the channel AMPn register is set to zero, the offset register can be used as a simple DC-output DAC channel.

5.1.5. PHAx - Channel Phase Registers

Each channel has a PHAn register which shifts the phase of the output waveform. The 16-bit register can be treated as an unsigned integer “P” from 0 to 65535, where the waveform is advanced in phase (ie, shifted earlier in time) by an angle of 360*P/65536 degrees; a P setting of 4096 thus shifts the waveform phase ahead by 22.5 degrees. Equivalently, P can also be treated as a signed integer from -32768 to +32767, with the same math.

Phase shifting is usually only meaningful between channels that are operating in a synchronized mode; see section 6.3 for details. Programmed phase shift does not affect the TTL-level SYNC pulses, as the phase rotation occurs downstream of the sync pulse pickoff.

5.1.6. PWMx - Channel PWM Registers

If a channel control register selects a signal source mux code K=1 or K=2, the channel operates in pulse width mode, with its PWMn register setting output duty cycle. In K=1 (Bipolar PWM) mode, the channel high level will be 0x7FFF and the low level will be 0x8001, corresponding to full-scale analog outputs of ±5.12 volts. In K=2 (Unipolar PWM) mode, the active part of the PWM pulse is still 0x7FFF but the low level is 0x0000, so the maximum outputs will be +5.12 and zero volts. These values are scaled by the current setting of the channel amplitude-set register.

This will create a high/low waveform of programmable duty cycle but with 16-bit duty cycle resolution. Pulse width will jitter by one clock, 7.8 ns p-p, unless the programmed frequency is an exact binary fraction of 32 MHz.

The PWMn register content sets the duty cycle of channel “n” from 0 (0x0000) to 99.9985% (0xFFFF.) The PWMn register is ignored in non-PWM modes and is set to 50% (0x8000) at powerup, corresponding to a square-wave output.

In BPWM mode, the effective waveform generated in PWM mode goes to maximum positive voltage (+5.12 max) for the first part of each cycle, and to maximum negative voltage (-5.12 volts) for the rest of the cycle, at the frequency defined by the channel frequency-set register pair. This 10.24 volt p-p waveform can be scaled down or inverted by the channel's AMPn amplitude register, offset by the OFSn register, and phase shifted by the PHAn register. In UPWM mode, the waveform goes positive (+5.12 max) for the first part of the cycle, and zero for the second. Once again, this waveform can be scaled, inverted, and phase shifted. The output voltage is reduced by 5:1 if the channel control D5 bit is set. Rise/fall time is typically below 15 ns.



Typical rise time in PWM mode.

5.1.7. MODx - Channel Modulation Control Registers

On the V346, each channel has a MODn register which controls modulation of that channel...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PW2	PW1	PW0	FR1	FR0	FM2	FM1	FM0		AM2	AM1	AM0		PM2	PM1	PM0

The PM field specifies another channel whose output will phase modulate this channel. If the encoded value is 0, phase modulation is disabled. If the value is 1 through 7, then the named channel will phase modulate this channel.

The AM field similarly specifies a source to amplitude modulate this channel, and the FM field selects a source for frequency modulation. The PW field specifies a source for PWM width modulation, usable only if the target channel is operating in one of its two PWM modes.

Note that channel 0 cannot be used as a source to modulate other channels. Otherwise, there are no restrictions on modulation selections.

The FR bits define four available ranges of FM modulation.

See section 6.2 for a full discussion of modulation. Modulation is not available on the V344.

5.2. Programming Waveforms

There are two different mechanisms in place for programming waveforms on the V344/V346. The MACRO interface is used to modify the 4K point RAM-based wavetable. This is the way that arbitrary waveforms are generated, as well as sine waves, triangle waves, and square waves. Switching to the PWMx controlled pulse waveforms or the bandlimited Gaussian noise use separate hardware which bypasses the wavetable, and is therefore performed by setting the K type bits in the channel control register.

5.2.1. Generating Standard Waveforms

The four standard waveforms available are sine waves, triangle waves, sawtooth waves, and a constant value. These waveforms can be used as-is or as a starting point for arbitrary waveforms. All channels power up with sine waves loaded into their waveform memories; macros are provided to switch to others or to return to sine waves.

To load waveform memories, load macro parameter register PARAM0 with a bitmap naming the channel or channels to be loaded (bits 0 through 7 set will select channels 0 through 7 in any combination.) To set all entries in a channel or channels' wavetable RAM to a constant, write that constant into PARAM1. Once the parameters are written, write the appropriate command into the MACRO register. Each of the waveforms spans the full range of amplitude, -32767 to +32767, equivalent to -5.12 to +5.12 volts, scalable by the channel amplitude register. When the MSB of the MACRO register clears, the load operation is complete.

Code	Operation	Max Time
0x8404	Load sine waves into wavetable RAM	4 ms
0x8405	Load sawtooth waves into wavetable RAM	10 ms
0x8406	Load triangle waves into wavetable RAM	10 ms
0x8407	Load constant into wavetable RAM	4 ms

For example, to load sawtooth waveforms into channels 4 and 5, write 0x0030 to PARAM0 and then load command code 0x8405 into MACRO.

5.2.2. Generating Arbitrary Waveforms

Arbitrary waveforms can be manipulated by reading or writing blocks of 128 signed 16-bit points at a time into and out of the module's BUFFER space. When writing a waveform, the user will write a block of points into the BUFFER, call the write macro, and repeat. To read a waveform back, the read macro is called, and then the BUFFER can be read.

Code	Operation	Max Time
0x840E	Write BUFFER to wavetable RAM	1 ms
0x840F	Read wavetable RAM to BUFFER	1 ms

To use the write macro, write 128 points of the waveform into the BUFFER space. Then load macro parameter register PARAM0 with a bitmap naming the channel or channels to be loaded (bits 0 through 7 set will select channels 0 through 7 in any combination.) Then write the starting index to PARAM1. Generally, this will be a multiple of 128, from 0 to write the first block of waveform RAM to 3,968 to write the last block. Finally, write the write macro code 0x840E into the MACRO register to commit the write. When the MSB of the MACRO register clears, the load operation is complete. As an example, assume a waveform exists in an array X[0] to X[4095], and is to be loaded into channels 2 and 6.

Write 0x0042 into PARAM0, selecting channels 2 and 6

Copy X[0] through X[127] into BUFFER[0] through BUFFER[127]
Write 0 into PARAM1 to write the block starting from address 0
Write 0x840E into MACRO, and then wait for the MSB to clear

Copy X[128] through X[255] into BUFFER[0] through BUFFER[127]
Write 128 into PARAM1 to write the block starting from address 128
Write 0x840E into MACRO, and then wait for the MSB to clear

Copy X[256] through X[383] into BUFFER[0] through BUFFER[127]
Write 256 into PARAM1 to write the block starting from address 256
Write 0x840E into MACRO, and then wait for the MSB to clear

…

Copy X[3968] through X[4095] into BUFFER[0] through BUFFER[127]
Write 3968 into PARAM1 to write the block starting from address 3968
Write 0x840E into MACRO, and then wait for the MSB to clear

To avoid certain internal math errors, any user values of 0x8000 will be loaded to waveform memory as 0x8001, and will read back as 0x8001.

The read macro works in the reverse direction, grabbing 128 points at a time back into the BUFFER space. PARAM1 again points to the start index of the block of points, however, the channel select bitmap in PARAM0 should only have one bit set, since multiple waveforms can't be read at once. With the parameters set, write the read macro code 0x840F into the MACRO register, and wait for the MSB of the register to clear. Then read out the 128 points, and repeat as necessary.

While it is generally advised to always work with start addresses that are multiples of 128 between 0 and 3968, this is not strictly necessary. The V344 and V346 enforce no block alignment on waveform RAM reads or writes, and requests to read addresses above 4095 will wrap back around modulo 4096.

5.2.3. Generating Pulse Waveforms

The PWM generator bypasses the wavetable, and instead generates pulses by directly comparing the phase against the requested duty cycle in the PWMx register. This both improves the available PWM resolution, and allows the PWM duty cycle to be adjusted without having to reprogram the wavetable.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OS	IN	R1	R0	D5	K2	K1	K0		S2	S1	S0	TR	LO	GL	AU
Channel Control Register CTLx															

Kcode	K2	K1	K0	Waveform
0	0	0	0	RAM: Waveform RAM is signal source.
1	0	0	1	BPWM: Use the PWM generator in bipolar mode, with output 0x8001 as "low" and 0x7FFF as "high".
2	0	1	0	UPWM: Use the PWM generator in unipolar mode, 0x0000 "low" and 0x7FFF "high".
3	0	1	1	GAUS: Use the Gaussian noise generator.
4	1	0	0	STEP: Single stepping through waveform RAM is signal source.
5	1	0	1	CNTL: Channel is acting as an Event source rather than a waveform generator (V346 only)
6	1	1	0	(reserved for future use)
7	1	1	1	(reserved for future use)

To generate a PWM waveform, the K field in the channel control register CTLx must be set to either BPWM or UPWM modes. UPWM mode is provided as a convenience to simplify PWM scaling when unipolar PWM signals are required; it simply makes it easier to get a true zero without any rounding errors.

In either mode, the DUTY register controls the positive duty cycle ratio. The value of DUTY is an unsigned 16-bit integer, representing the fraction from 0% to 99.9985%. Some common duty cycles are:

Duty Cycle	DUTY (Hex)	Duty (Decimal)
10%	0x199A	6554
25%	0x4000	16384
50%	0x8000	32768
75%	0xC000	49152

For positive AMPLx and FHx:FLx values, the rising edge of the PWM waveform occurs as the phase accumulator crosses through zero.

5.2.4. Generating Gaussian Noise

Any V344/V346 channel may be programmed to generate band-limited Gaussian noise, by setting its channel control register "K" field to 3; see section 5.1.1.

The channel noise output will be 1.0 volts RMS at the maximum AMPn gain setting, independent of programmed bandwidth, with a nearly Gaussian probability distribution function. The probability distribution does not have the infinite-amplitude tails of truly random noise, so the crest factor is finite, just about 5:1, so that clipping of the channel DAC beyond +-5.12 volts has zero probability.

The usual channel amplitude scaler AMPn, and the D5 attenuation bit, may be used to scale amplitude down from the 1 volt RMS maximum level.

The noise is lowpass filtered with a 3 dB bandwidth that is set in the channel frequency registers FHn:FLn, with the maximum value of 0x7FFF:FFFF specifying a noise bandwidth of 2 MHz. So the noise generator -3 dB frequency is 1/16 of the frequency that the channel would normally generate as a standard sinewave.

Noise is generated from a digital random-number generator, with samples digitally filtered to produce the near-Gaussian distribution and programmed bandwidth. Noise is uncorrelated between channels and has no significant autocorrelations on timescales below the geological.

The noise output of one channel may be used to phase, amplitude, frequency, or PWM modulate another channel. Noise can also be summed into waveforms generated by other channels, with the sum directly output and/or used to modulate still other channels.

If the noise output of one channel is used to phase modulate the waveform of another channel, the maximum phase modulation will be 70.3 degrees RMS. Given the maximum crest factor of just over 5:1, peak phase modulation will be just about +-360 degrees. The AMPn register of the noise-generating channel may be used to scale down the amount of modulation.

If a noise signal is used to phase modulate a target channel that is operating in PWM mode, both the rising and falling edges of the PWM waveform will be modulated (jittered) in time. If the noise bandwidth is low compared to the PWM frequency, both PWM edges will tend to move together, maintaining nearly constant pulse width. If the noise bandwidth is relatively high, each edge will be jittered independently, and pulse width will vary accordingly. Phase modulating a PWM signal with relatively high-frequency noise can produce rising and falling-edge glitches and unusual statistical effects.

5.3. One-Shot Operation

5.3.1. Generating Single Waveform Cycles

Any V344/V346 channel may be programmed to operate in one-shot mode, by setting the OS bit in its channel control register. This will cause the channel phase-accumulator to remain parked at zero until it receives a FIRE trigger. Receipt of this trigger will trigger the output of a single cycle of the waveform, which will stop again at zero and await the next trigger.

If a channel is running when its OS bit is set, it will finish its current sweep through waveform memory and then enter the STOP state with its phase accumulator clear, at which time it will statically output the 0th waveform memory data point, possibly shifted by any PHAn register setting or phase modulation link.

If a channel is held in reset while OS is asserted, or is reset after OS is raised, it will also park in its STOP state with the phase accumulator held clear.

If a channel is armed for one-shot action (OS bit true and STOP state), and a FIRE action is performed on the channel, it will sweep through one pass of waveform memory, generating one cycle of waveform, then STOP. If the channel is already running, FIRE triggers are ignored. If the OS bit is dropped, the channel will resume normal waveform generation.

A FIRE trigger can be invoked from a VME "Fire" macro or from a FIRE Event.

FIRE Source	Scope	Steps
VME Write	Local Module	Write a channel bitmask into PARAM0 to define the channels to be FIREd. Bits 7-0 correspond to channels 7-0; a set bit means to FIRE, a cleared bit means to just keep waiting. Write 0x841D, the “Fire One-Shot Channels” macro, to the MACRO register. Repeat to FIRE again.
TTL Input	Local Module	Set the C field of the TTLCTL register to either 2 for a rising-edge trigger, or 3 for a falling edge. Set the AE bit (accept events) of the CTLx register of each channel that should accept the locally generated FIRE event. Channels with their AE bit clear will ignore the event. Set one or the other of the CAD fields in the ADDRn registers of any channels that ought to respond to the FIRE Event, to an address (AD) between 0 and 254. Set the E field of the TTLEVT register to 0x08, the FIRE event. Set the A field to the same address AD as the channels. Apply the appropriate TTL edge to the TTL EVENT pin (21) of the AUX connector, and repeat to FIRE again.
VME Write	Bussed System	Connect the bussed system, and define system master and slave units in the MODCON registers. Set the AE bit (accept events) of the CTLx register of each channel on each board that should accept the globally generated FIRE event. Channels with their AE bit clear will ignore the event. Set one or the other of the CAD fields in the ADDRn registers of each channel on each board that ought to respond to the FIRE Event, to an address (AD) between 0 and 254. Set the E field (lower 6 bits) of PARARM1 on the system master module to 0x08, the FIRE event. Set the A field (upper 8 bits) to the same address AD as the channels. Write 0x841C, the “Send Global Event” macro, to the MACRO register of the system master module. Repeat to FIRE again.

TTL Input	Bussed System	Connect the bussed system, and define system master and slave units in the MODCON registers. Set the C field of the TTLCTL register on the system master module to either 4 for a rising-edge trigger, or 5 for a falling edge. Set the AE bit (accept events) of the CTLx register of each channel on each board that should accept the globally generated FIRE event. Channels with their AE bit clear will ignore the event. Set one or the other of the CAD fields in the ADDRn registers of each channel on each board that ought to respond to the FIRE Event, to an address (AD) between 0 and 254. Set the E field of the TTLEVT register on the system master module to 0x08, the FIRE event. Set the A field to the same address AD as the channels. Apply the appropriate TTL edge to the TTL EVENT pin (21) of the AUX connector on the system master module. Repeat to FIRE again

5.3.2. Using Single Step Mode

There are tasks for which a free-running DDS generated waveform is ill suited, such as generating static DAC levels coordinated to external events. For these purposes, V346 channels can be placed into the STEP mode, in which each full cycle of the phase accumulator advances to the next step of the wavetable RAM. When the phase accumulator is allowed to run freely, this means that one point will be issued each period, which is the inverse of the programmed frequency.

STEP mode becomes far more useful, however, when combined with the one-shot capability. With the phase accumulator held at zero by the STOP state of the one-shot, the channel will continue outputting the same point. Upon receiving a FIRE trigger, the channel will wait for one period (as the phase accumulator accumulates), and then advance to the next point in the wavetable (as the phase accumulator overflows). This can be used to generate static DAC levels to control other external devices, or in concert with the modulation or summing features to preprogram a sequence of alterations for a different channel, allowing for instance stepping the frequency or DC offset of another channel.

5.4. Channel Errors

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								V7	V6	V5	V4	V3	V2	V1	V0
CLIPS Register															

The CLIPS register provides information about whether or not a channel is clipping. For channels operating without any summing, clipping can be caused only by a combination of amplitude and DC offset that exceed the maximum DAC range. Each time a point must be clipped, the channel's signal sum will saturate to either the negative or positive maximum and the channel's bit will be set in the CLIPS register. When the conditions causing this clipping have been changed, the clipping bit will clear itself after about two seconds.

If this clipping is the expected behavior of the channel, then this may be ignored. Channel clipping may also be caused by summing channels, more information is provided about this in section 6.1.3.

6. Controlling Multiple Channels

6.1. Channel Summing

6.1.1. Summing Channels

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OS	IN	R1	R0	D5	K2	K1	K0		S2	S1	S0	TR	AE		SY
Channel Control Register CTLx															

The outputs of multiple channels can be summed together. This allows for many common tasks to be performed, including adding in harmonics of the original signal and tuning their amplitude and phase, or adding 60-Hz hum or Gaussian noise pickup to a signal to test the robustness of a receiver system

In order to sum two channels, we will introduce the idea of the “source” channel (the one providing the data to be summed) and the “target” channel (the one the data is being summed into. To initiate summing, set the S bits of the CTLx register for the target channel equal to the number of the source channel.

For instance, if we create a 60 Hz sine wave on channel 2, and a 200 Hz sine wave on channel 4, we can sum them by setting the S bits in CTL2 to 4 (i.e. 100 binary). This makes channel 4 the source, and channel 2 the target. The source is unaffected by this process, and channel 4 will continue to output a 200 Hz sine wave. Channel 2 (the target), however, will output the sum of the 60 Hz and 200 Hz sine waves.

Setting the S to 0 (the power-on default) will turn summing off for the target channel. Therefore, channel 0 cannot be a summing source. Also, summing a channel with itself is generally neither productive nor advised.

6.1.2. Cascading Summed Channels

Channel summing may be cascaded all the way to summing all 8 channels. To extend the previous example, if channel 5 had a 1 kHz sine wave output, and the S bits of CTL5 were set to 2, then channel 5 would generate its own 1 kHz output summed with the channel 2 sum of channel 2’s 60 Hz sine wave and channel 4’s 200 Hz sine wave.

Alternatively, if the S bits of CTL5 were set to 4, then channel 5 would output only its 1 kHz output summed with the channel 4 200 Hz.

Each level of summing in a cascade structure will add two clocks (15.6 ns) of delay in the signal path. Much like directly summing a channel with itself, summing a channel with a source channel that is itself summed from the target (i.e. 5 sums channel 2, 2 sums channel 3, 3 sums channel 5) is not advised.

6.1.3. Channel Summing Errors

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								V7	V6	V5	V4	V3	V2	V1	V0
CLIPS Register															

The CLIPS register, as discussed in section 5.4, provides information about whether or not a channel is clipping. For summed channels, this occurs when the total of all of the channels summed and all of their DC offsets exceeds the DAC range. When this condition occurs, the channel's bit in the CLIPS register will be set, and the waveform will saturate at the limit.

If this clipping is the expected behavior of the channel, then this may be ignored. Also, as clipping and saturation are evaluated for each channel, there are some combinations of waveforms, amplitudes, and DC offsets for which summing the channels in one order will clip, but summing them in a different order will not.

6.2. Channel Modulation (V346 only)

Channel modulation is the most powerful feature available on the V346. Some of the possibilities available through modulation include:

- Simulation of random shaft vibration by phase modulation with Gaussian noise
- Misaligned gear detection by amplitude modulation of the tooth pickup signal with a sine wave at the shaft rotation speed.
- Frequency ramps generated by frequency modulating against a slow sawtooth
- DC-DC plant loop testing by pulse-width modulating the switch control at different frequencies.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PW2	PW1	PW0	FR1	FR0	FM2	FM1	FM0		AM2	AM1	AM0		PM2	PM1	PM0
MODx Register															

Modulation for each channel is controlled by the MOD0-MOD7 registers. Setting a given channel's MODx register makes it into a modulation target, the fields in the register specify the modulation source. For any given field, a modulation source of zero indicates no modulation (therefore channel 0 cannot be a modulation source). The fields are:

Field	Meaning
PM	Phase modulation source
AM	Amplitude modulation source
FM	Frequency modulation source
FR	Frequency modulation frequency prescaler
PW	Pulse-width modulation source

When a channel is used as a modulation source, it provides its data after any summing has taken place, but before the conversion to analog. Therefore, if channel 3 uses channel 4 as a summing source, then if channel 2 uses channel 3 as a modulation source, it will be modulated with the sum of channels 3 and 4. The D5 amplitude divider, however, has no effect on modulation.

Modulation is not available on the V344.

6.2.1. Amplitude Modulation Scaling

Assume we wish to amplitude modulate target channel 0 by the output of channel 7. The MOD0 register will be set to 0x0070 to establish the modulation link.

The 16-bit equivalent output of channel 7 is added to the AMP0 register, with the sum applied to the CH0 amplitude multiplier. The channel 7 waveform output is treated as a signed 16-bit value. One might set the AMP0 register to zero when using amplitude modulation; in that case, the scaling of channel 0 outputs would be…

Channel 7 Value	Channel 7 Output	Channel 0 Multiplier
0x7FFF	+5.12V	+0.99997
0x4000	+2.56V	+0.5
0x0000	0V	0
0xC000	-2.56V	-0.5
0x8000	-5.12V	-1

The instantaneous output of channel 0 would then be

V0 = (Wx / 32768) * ((D7+AMP0) / 32768) * 5.12 volts

where Wx is the current channel 0 wave memory output (range +-32767) and D7 is the current channel 7 DAC code, scaled from 32767 (+5.11 volts) to -32768 (-5.12 volts.) Note that if the D7+AMP0 addition exceeds the signed 16-bit range, then the results will overflow and an error flag will appear in the upper byte of the MODS register.

6.2.2. Phase Modulation Scaling

Assume we wish to phase modulate target channel 0 by the output of channel 6. The MOD0 register would be set to 0x0006 to establish the modulation link.

The 16-bit equivalent output of channel 6 effectively added to the PHA0 register, with the sum applied to the CH0 phase rotation adder. If the channel 6 output were 0x4000 (equivalent to +2.56 volts DAC output), the phase of the channel 0 output will be advanced 90 degrees sooner in time; i.e. the channel 0 wave table pointer will be advanced 1024 locations. Thus the modulating input can be treated as a 16-bit unsigned integer in the range 0x0000 to 0xFFFF that scales to 0 to 359.99 degrees of phase lead, or it can be treated as a signed integer from 0x8000 to 0x7FFF that scales from -180 to +179.99 degrees; these views of the situation are mathematically equivalent. The sum of PHA0 and the incoming channel 6 modulation is treated as an angle modulo 360 degrees, with no possible overflow.

6.2.3. Frequency Modulation Scaling

Assume we wish to frequency modulate target channel 0 by the output of channel 5. The MOD0 register will be set to 0x0500 to establish the modulation link. Assume the FR bits are all zero.

The scaled and offset output of the channel 5 waveform generator is treated as a signed 32-bit integer that is added to the programmed frequency of channel 0. Assume that channel 0 is programmed for a frequency of F_0. The correspondences are…

Channel 5 Value	**Channel 5 Output**	**Channel 0 Frequency**
0x7FFE0002	+5.12V	F0 + 15.999023 MHz
0x40000000	+2.56 V	F0 + 8.0000000 MHz
0x0000	0V	F0
0xC0000000	-2.56V	F0 - 8.0000000 MHz
0x80000000	-5.12V	F0 - 16.000000 MHz

where the 0x7FFE0002 is the signed product of the maximum channel 5 wave table entry (0x7FFF) times the maximum AMP5 amplitude scaler (0x7FFF).

So if channel 5 were programmed to generate the standard sawtooth wave (with wave table entries sweeping from 0x8001 to 0x7FFF) and the AMP5 register were set to 0x7FFF, the resulting peak-to-peak FM modulation of channel 0 would be 31.999 MHz. If the channel 0 center frequency Fo were programmed to 16 MHz, the result would be a linear sweep from 0 to just under 32 MHz.

With the scaling noted above, the narrowest sweep that the full-scale sawtooth can make will be when the AMP5 register is set to 0x0001, at which point the sweep will be 976 Hz wide. Narrower span sweeps can be had by setting the FR bits in the MOD register, scaling down the FM range.

FR Code	FR1	FR0	Divisor	Sweep Range
0	0	0	1	32 MHz
1	0	1	16	2 MHz
2	1	0	256	125 kHz
3	1	1	4096	7.8 kHz

Note that the FM deviation is not affected by the frequency range of the target channel, namely the state of the R bits of the channel control register.

Since channel frequency is signed, it is possible to sweep across positive and negative frequencies by sweeping through zero.

Should the sum of the channel's programmed frequency and the scaled frequency modulation signal exceed the range of ±64 MHz, the results will overflow and an error flag will appear in the lower byte of the MODS register.

6.2.4. PWM Modulation Scaling

If a channel is operating in one of its PWM modes, and that channel's PW modulation register field is set to 1 through 7, then the target channel's PWM duty cycle will be controlled by the output of the named source channel, and the target channel's PWMx register will be ignored. The integer value from the modulating channel is mapped such that the scaling is…

Channel 7 Value	Channel 7 Output	Mapped Equivalent	Channel 0 Duty Cycle
0x7FFF	+5.12V	0xFFFF	99.9985%
0x4000	+2.56V	0xC000	75%
0x0000	0V	0x8000	50%
0xC000	-2.56V	0x4000	25%
0x8000	-5.12V	0x0000	0%

For example, suppose channel 7 were programmed to generate a 400 Hz sine wave at full (+-5.12 volts) amplitude. That sine wave would appear on the channel 7 electrical output.

Now suppose we program target channel 2 to operate in PWM mode at 200 KHz, and set its PW modulation bit field to "100", selecting channel 4 to control its pulse width. We could now use the output of channel 2 to control a switchmode power H-bridge, operating at 200 KHz, which will now produce a full-scale, bipolar, 400 Hz sinewave power output. Channel 4 can be programmed for new frequencies, amplitudes, or phases as desired, and the H-bridge output will follow.

The internal scalings within each channel prevent the output of the amplitude scaling multiplier (see fig 3.2) from generating value -32768, 0x8000. So in the above example, target channel 2 will not go to exactly zero duty cycle at the maximum negative swing of PWM source channel 4. To hit zero duty cycle, a small negative offset could be loaded into the OFS4 register to drive channel 4 negative swings all the way to 0x8000.

6.2.5. Channel Modulation Errors

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0	F7	F6	F5	F4	F3	F2	F1	F0
MODS Register															

The MODS register displays mathematical overflow errors associated with channel modulation.

The A7…A0 bits flag mathematical overflow in the amplitude modulation logic of channels 7 through 0 respectively. These bits will set if the AM level end-arounds past + or - full scale, creating a discontinuity. They are not set by the modulator input crossing through zero, as might occur when generating suppressed carrier DSB modulation, where the carrier is regularly inverted in phase.

The F7…F0 bits flag mathematical overflow in FM modulation. Like the AM bits, the overflow is past the extremes of + or - frequency range and does not flag a frequency that passes through zero.

Once the channels are reprogrammed to remove the condition causing these errors, they will self-clear after about two seconds.

Note that neither the PM nor PWM modulation paths can overflow.

6.3. Channel Synchronization

6.3.1. Principles of DDS Synchronization

Because the frequencies of all of the channels on a V344/V346 are derived from the same 128 MHz master clock, two channels programmed to identical frequencies will output at identically the same frequency; the phase relationship between the two channels now and 100 years from now will have not drifted at all. This applies as well to channels programmed to exact integer relationships with one another, allowing a channel programmed to 125 kHz and one programmed to 250 kHz to never drift against one another.

Given a phase relationship capable of persisting for the rest of time, the trick becomes setting it in the first place. In the V344/V346, this is best accomplished by using the phase rotation registers to program the desired phase relationship, then resetting the phase accumulators to zero. For the case of two channels set to the same frequency, after the reset the two phase accumulators (beginning at the same value and incrementing with the same value at the same time) will remain the same, thus making the only phase difference the one programmed into the phase rotation registers. Channels can be reset in several ways, including VME macros, the front panel TTL Reset signal, and the system-wide Event bus, all of which will be described in greater detail in the upcoming sections.

The V344/V346 also allows for channels to be simultaneously updated with new data without resetting. Practically, this tends to be useful only for channels that have already had their phase relationship set with a reset, but future updates do not require further resets. For example, two channels generating 300 kHz sine waves 90° out of phase can be updated together to 400 kHz. When the update takes place, the channels will change frequencies with no phase discontinuity, and will remain 90° apart. In order to do this, the channels must be prevented from automatically loading new parameters when they are written to VME, by placing them into Synchronous Update Mode, described below. They can then receive the update event from either a VME macro or the Event Bus.

6.3.2. Maintaining Phase Relationships

Because the FHn:FLn frequency control registers accept an integer value, there will usually be some rounding error associated with the scaling. While these rounding errors are tiny in terms of absolute frequency accuracy, care must be taken when trying to generate multiple channels with related frequencies. Otherwise, the result can be to take the channels just barely out of an integer relationship, i.e. 9.9999:1 rather than 10:1. Over a large number of cycles, this will cause the channels to walk out of phase alignment with one another. For simulations of many mechanical systems, such as gear trains, this is unacceptable. The correct approach is to generate the frequencies as exact integer multiples **after** the rounding has already occurred, such as in:

```
double fFreq1 = 92.1e3;         /* Driving frequency is 92.1 kHz */
double fMax = 4.0e6;            /* Channels are on 4 MHz range */

signed long iFreq1;       /* 32-bit integer representation of fFreq1
*/
signed long iFreq2;       /* Should be set to _exactly_ 10x Freq1 */

/* The following statements have no relative rounding error. */
iFreq1 = round((fFreq1 / fMax) * double(2^31));
iFreq2 = iFreq1 * 10;
```

This multiplies the frequency of the initial conversion, with the rounding error already included, and thus produces exactly linked frequencies.

6.3.3. Taking Phase Snapshots

It can be useful, especially when generating lower speed waveforms, to capture an instantaneous snapshot of the phases of all of the channels. This can be accomplished by writing the “Snapshot and Read Phases” macro, 0x840C, into the MACRO register. Alternatively, the snapshot could been executed by a Phase Snapshot Event, in which case, the “Read Phases” macro, 0x840D, should be used instead.

Regardless of whether it is sourced by a macro or an Event, snapshotting the phases takes down a record of the phase accumulators of all 8 channels at a single instant, as well as a 16 bit signed cycle count. When the V344/V346 is told to then Read Phases, all this information is written into the BUFFER block.

	0x_0	**0x_2**	**0x_4**	**0x_6**	**0x_8**	**0x_A**	**0x_C**	**0x_E**
0x10_	0	CYC0	PH0	PL0	0	CYC1	PH1	PL1
0x11_	0	CYC2	PH2	PL2	0	CYC3	PH3	PL3
0x12_	0	CYC4	PH4	PL2	0	CYC5	PH5	PL5
0x13_	0	CYC6	PH6	PL6	0	CYC7	PH7	PL7

The snapshots are written, starting at the start of the BUFFER block (0x100) as a 16-bit zero, then the 16-bit cycle count, then the 32-bit phase, from channels 0 up to channel 7. Each 32-bit phase may be treated as an angle from 0 degrees (0x0000:0000) to 359.999… degrees (0xFFFF:FFFF). This data may be used to compute channel-to-channel relative phases.

6.3.4. Synchronous Update Mode

Data loaded into module VME registers must be processed before being installed in the actual channel waveform generation hardware. The act of processing and installing these settings is called Channel Update.

If channels are to be phase coherent, it is necessary to simultaneously clear their phase accumulators and thereafter manage them properly to ensure that phase relationships are maintained. The act of clearing phase accumulators is called Channel Reset.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OS	IN	R1	R0	D5	K2	K1	K0		S2	S1	S0	TR	AE		SY
Channel Control Register CTLx															

If a channel operates in the default Asynchronous Update Mode (SY=0), channel settings in VME registers are applied to channel hardware in a continuous scan loop. Channels are updated automatically with a maximum delay of 250 microseconds, but channel-channel coherency is not observed.

Any channel that has its SY bit set will operate in Synchronous Update Mode. These channels will be excluded from the asynchronous update loop, making it available for coherent operations. Channels will update all of their parameters at once, but must be manually instructed when to do so by the user.

Macros are provided to allow immediate Update, Reset, or Update+Reset operations onto any combination of channels on one board. This is the basic, VME-driven way to synchronize channels in a single-board system.

Events may also be used to allow any grouping of channels on one or multiple boards to be simultaneously updated and/or reset. These events can be local or global, and can be triggered by a TTL signal on pin 21 of the front-panel SCSI connector, a VME command, or a control channel.

6.3.5. Synchronization via VME Macros

If a channel is set for Synchronous Update mode, macro operations can perform coherent operations in one to eight channels simultaneously.

The usual sequence would be…

> Set the AU bits in desired channel control registers to exclude channels from asynchronous updates.
>
> Load initial channel settings.
>
> Execute the UPDATE+RESET macro, using the appropriate channel bit mask, to load and synchronize the channel group. The named channels will start in phase.

Additional channel programming changes can be made to any of the channels in the group, followed by an UPDATE macro, with the same select mask, to update the channels coherently. Note that channel 32-bit frequency settings must be kept equal or in **exact** integer ratios to maintain phase coherence.

Note that such macro operations can be done on independent user-defined groups. For example, two separate groups of three channels can be used to simulate two different 3-phase generators, and can be managed independently.

6.3.6. TTL Events

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		T1	T0		C2	C1	C0								
TTLCTL Register															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0			E5	E4	E3	E2	E1	E0
TTLEVT Register															

When channel updates must be synchronized to external events, the TTL Event mechanism provides a means of accepting an externally generated trigger signal.

The C bits in the TTLCTL register define the sense of the external edge which triggers the Event. Modules that are not system masters should use one of the two Local Event settings. System masters may use the Local Event modes to generate events that are broadcast only to their channels, or the Global Event modes to generate events that are broadcast to all of the boards on the SYS bus.

Code	C2	C1	C0	Action
0	0	0	0	none
1	0	0	1	none
2	0	1	0	Local Event on rising edge of pin 21
3	0	1	1	Local Event on falling edge
4	1	0	0	Global Event on rising edge
5	1	0	1	Global Event of falling edge

Upon receipt of the selected edge on pin 21 (TTL EVENT) of the AUX connector the module will transmit the Event indicated by the TTLEVT register. Channels for which either Channel Address (CAD) matches the Target Address (TAD) called out by the A field of the TTLEVT register, and for which the Accept Events bit is set in their CTLx register, will perform the operation specified by the E field of the TTLEVT register.

Ecode	Event Operation
0	none
1	Update channels: transfers settings from channel latches
2	Reset channels: clears phase accumulators
3	Update and Reset
4	Phase Snapshot
8	Fire one-shot channels

After the Event occurs, the TCOUNT register will be incremented by 1. This allows the user to write the next set of channel parameters in anticipation of the next external edge.

TCOUNT can be reset by writing the “Reset TTL Event Counter” code (0x841F) into the MACRO register.

6.3.7. Control Channel Events

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OS	IN	R1	R0	D5	K2	K1	K0		S2	S1	S0	TR	AE		SY
Channel Control Register CTLx															

By setting the K code of a channel to 6, CNTL mode, a channel can be turned from a waveform channel into a control channel. A control channel, rather than a generator of a signal, is a generator of a sequence of Events at pre-programmed times. The waveform RAM, rather than describing a waveform, is in this case used to describe the Event sequence. Only channels 6 and 7 can be turned into control channels.

Like with the Single Step Mode described in Section 5.3.2, the FHx:FLx frequency register sets the period for stepping through the event sequence, known as the step clock. For example, an entered channel frequency of 1 MHz would correspond to a 1 MHz step clock, which would advance through the table at one step per microsecond.

Commands in the control channel wavetable RAM are defined as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	E5	E4	E3	E2	E1	E0	A7	A6	A5	A4	A3	A2	A1	A0
Generate Local Event															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	E5	E4	E3	E2	E1	E0	A7	A6	A5	A4	A3	A2	A1	A0
Generate Global Event															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Delay For A Time															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Sleep Until A FIRE Trigger															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	A11	A10	A9	A8	A7	A6	A6	A4	A3	A2	A1	A0
Jump to Address															

The two Generate Event commands each take two arguments:

Field	Meaning
E	Event code. Event codes are the same as defined for TTL Events and Global Events.
A	Target address (TAD) to broadcast to.

The Delay command takes a 12-bit long unsigned argument in the D field, corresponding to a delay of D ticks of the step clock, with a D of zero acting as a special case delay of 4,096 ticks. Longer delays can be created by executing multiple Delay commands back to back.

The Jump command jumps to another absolute location in the control channel, and continues execution from that address. The A field corresponds to the address from 0 to 4095. The most useful flavor of the Jump command is the jump to 0 (0x7000), which begins executing the program again from the beginning. In this way, the program can be made to loop over the same commands over and over.

The Sleep command puts the channel to sleep until it is awakened by a FIRE trigger. This FIRE trigger can come from any of the usual sources; the TTL connector, the VME bus, or an event sent in on the SYS bus. This is done by temporarily placing the channel into one-shot mode, therefore the channel will not actually enter the sleeping state until one step clock period after the Sleep command is executed. This means that the next command in the list will fire immediately after the FIRE trigger is received.

Through the use of the Sleep and Restart commands complex sequences can be generated. For instance, a control channel with a 1 kHz step clock (1 ms period) could be programmed as follows:

Entry	Command	Interpretation	Start Time
0	0x6000	Sleep until a FIRE trigger	pre-trigger
1	0x8801	FIRE to CAD 01	0 ms trigger
2	0x0004	Delay 4 ticks	1 ms
3	0x8803	FIRE to CAD 03	5 ms
4	0x8802	FIRE to CAD 02	6 ms
5	0x0009	Delay 9 ticks	7 ms
6	0x8803	FIRE to CAD 03 again	16 ms
7	0x7000	Restart	17 ms

By setting the TTLEVT register to send a FIRE Event to the control channel, this sequence of one-shot pulses can be made to happen upon receipt of an external rising edge. The duration of each channel's pulses can be set on their own respective frequency registers. The timing of the pulses can be manipulated independently by changing the frequency register of the control channel, or by changing the control channel programming. Alternatively, the channel can be kicked off by a VME write, or by an Event generated on the SYS bus by a system master.

7. Controlling the Module

7.1. Using an External Frequency Reference

10 MHz clock sources with excellent accuracy and long-term stability are widely available. For situations in which these qualities are required, the V344/V346 can lock its internal clock to an external 10 MHz reference source in order, turning the native parts per million accuracy into parts per billion or trillion.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										M1	M0				XC

MODCON Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCM							LER						SYN	S10	LOK

CSTAT Register

If the V344/V346 detects the presence of a (roughly) 10 MHz reference signal on the CLOCK connector, it will set the S10 bit in the CSTAT register. In order to lock the module to an external reference, set the XC bit in the MODCON register. This will cause the module to begin attempting to lock. Lock should be acquired within about 2 seconds, at which time the module will set the LOK bit in CSTAT. If a lock cannot be required, the LER lock error bit will be set.

Note that, as global bus synchronization requires that all slave units phase lock to a master unit, 10 MHz reference locking is not available for system slaves, and the XC bit will be ignored. However, the master unit can be locked to a 10 MHz reference, and all of the slaves will track it accordingly with no loss of stability.

7.2. Demonstration Presets

As a quick check of module functionality, the module can be programmed into a set of demonstration waveforms by writing the “Demo Mode” command 0x8411 into the MACRO register.

7.3. Calibration Verification

7.3.1. Calibration Date Registers

The V344/V346, like all equipment, suffers from long-term drift that slightly degrades the accuracy of the unit. Therefore, Highland Technology generally recommends annual recalibration for applications that demand the highest accuracy. The date of the last calibration is stored in the YCAL and DCAL registers. YCAL holds the year of the last recalibration, the high byte of DCAL holds the month, and the low byte holds the day.

7.3.2. Relays, the Calibration Bus, and the Test Connector

Users wishing to verify the system calibration themselves, or wishing to compensate the rest of their systems for drift in the V344/V346, can use the calibration bus and TEST connector to reroute channel output signals to a precision voltmeter and/or frequency counter. This can be done with the calibration relays on the V344/V346 rather than having to disconnect field wiring.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								K7	K6	K5	K4	K3	K2	K1	K0
RELAYS Register															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															TM0
MODE Register															

Setting a bit in the RELAYS register reroutes a channel's output to the calibration bus rather than the normal output connector. Do not set more than one bit of the RELAYS register at a time. Setting the TM0 bit in the MODE register then routes the calibration bus out to the TEST front panel connector. The signal that is seen on the TEST connector is identical to the one that would have come out the normal output connector.

7.3.3. Frequency Counter

The V344/V346 uses two internal crystal oscillators. A 128-MHz oscillator is the basis for synthesized waveforms, and a separate 20 MHz oscillator is used as the microprocessor clock and the time reference for the internal frequency counter and BIST. The main 128 MHz oscillator is factory-set to better than 1 PPM and can be expected to drift less than 2 PPM per year. The 20 MHz oscillator is not adjustable and can be expected to be accurate to 50 PPM long-term.

The internal counter may be selected to measure the frequency of the signal on the internal BIST bus (that is, a selected channel output) or half the frequency of the 128 MHz waveform generator clock, 64 MHz.

The FTIM register controls frequency counter operation:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			CF				X2	G7	G6	G5	G4	G3	G2	G1	G0

The timebase period over which cycles are counted is set by the contents of the G7...G0 bits of the FTIM register, in units of 100 milliseconds.

Users may set the LS byte of FTIM to any value from 1 to 255, corresponding to frequency counter gate times from 100 milliseconds to 25.5 seconds. For example, when measuring very low frequencies, FTIM may be set to 100, for a 10 second timebase, in which case FRHI:FRLO will report frequency in units of 0.1 Hz.

The CF bit selects the source of the signal to measure. Setting the bit measures a 64 MHz internal clock derived from the 128 MHz master clock, while clearing it measures the signal from the calibration bus.

The system normally counts only rising edges of the selected signal. If the user sets the X2 bit, both rising and falling edges are counted, doubling frequency measurement resolution.

At the end of every gate interval, the measured frequency is updated into the register pair FRHI and FRLO, where FRHI is the most significant 16 bits of the 32-bit count and FRLO is the least significant. To ensure skew-free atomic reads, users must read FRHI and then FRLO.

FTIM is set to 0x000A on powerup.

To measure an output channel frequency in Hz, one can...

Program a channel to produce a waveform output that swings from at least 0 to +3 volts.

Route it to the test bus by setting the appropriate bit in the RELAYS register.

Make sure the MODE register is set to zero

Load FTIM with 0x000A (select test bus, 1 second gate)

Wait at least two seconds and read the frequency in FRHI:FRLO.

The PRHI and PRLO register pair reports the frequency input as a 32-bit period, with LSB representing 25 ns. The value is updated once each cycle of the selected frequency-counter input signal and is independent of the selected frequency counter timebase. This period measurement can resolve the frequency of low-frequency inputs faster and with higher resolution than the frequency counter mode. If the input signal stops for more than 1 second, the reported value will jump to 0xFFFF:FFFF. This register pair must be read atomically, PRHI and then PRLO.

If PRHI:PRLO is read as a 32-bit integer P, the signal frequency in Hz is

F = 40e6/P

which has better resolution than a typical frequency-mode measurement for signals in the Hz and low KHz range. The period counter ignores the X2 control bit.

7.3.4. Built-In Self-Test

The V346 features an automatic self-test sequence to allow the user to test the functionality of the unit without external equipment and without the need to disconnect field wiring.

Note: BIST is primarily a functional test and checks only approximate quantitative performance limits. It cannot allow absolute verification of module accuracy, as external NIST-traceable standards are required for formal calibration.

Although the BIST operations can detect most module failures, certain errors can be missed. They include:

- • Failure of a connector pin or associated printed-circuit traces
- • Failure of a channel test relay
- • Low-order DAC bit errors
- Sync output failures

Items tested include...

- BIST a/d converter operation
- Module power supplies
- Synthesizer (128 MHz) clock frequency accuracy
- Channel full-scale AC output and DC offset voltages
- Channel divided-by-5 AC output and offset voltages

- Channel output frequency accuracy
- Filter response

Loading the MACRO register with 0x8410 initiates the module self-test. No parameters are required. The BISS register will display test status and the BERR register displays any errors. The full test takes about 13 seconds.

During the test, the green LED will blink rapidly, and the red LED will come on solid for at least one second if any error is detected. After the self-test, all previous module settings will be restored, except that all channel memories will contain sine waves.

The BISS status register layout is...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								BSY							BAV

The BAV bit indicates that the BIST facility is available. BSY is true while the BIST self-test is in progress.

The BERR register flags BIST errors. Bits are...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADX	CLX	MX						E7	E6	E5	E4	E3	E2	E1	E0

Bits 7...0 flag errors on respective channels. ADX flags an A/D converter error, and CLX indicates that the DDS reference crystal oscillator is failed or excessively off its correct 32 MHz frequency. MX indicates an error in a module power rail.

If any error is detected, a diagnostic log is written to the first 16 words of the BUFFER space", VME registers 128 through 143. The values in these registers may be noted and communicated to Highland to determine the specific error and associated measured values. The register functions are….

Register	Function
128	channel ID bitmask, 0 for global tests
129	BERR pattern at time of error
130:131	D0 lower bound. D0 represents the DC level in 10s of mV, the ADC offset, or the clock frequency, depending on the test.
132:133	Measured D0
134:135	D0 upper bound
136:137	D1 lower bound. D1 represents the RMS AC level in 10s of mV, the ADC slope
138:139	Measured D1
140:141	D1 upper bound
142	Error Code: 1 ADC error 2 128 MHz oscillator error 5 channel frequency error 10 channel error, incorrect full-scale output amplitude 11 channel error, divided by 5 output amplitude 18 channel error, incorrect 32 MHz output 19 channel error, filter check
143	Error Count, incremented by one for each error posted

7.4. Module Resets

Macros are provided to restart the module firmware.

HARD REBOOT (0x8420) resets all the on-board hardware, reconfigures both FPGAs, and loads all registers to their default values. Total time is about 4.8 seconds, and the module disappears from the VME bus for about the first four seconds.

SOFT REBOOT (0x8421) does not reinitialize the FPGAs or other hardware, but sets all registers to their default states. This takes about 16 milliseconds.

Both macros reload all wave memories with sinewaves.

For both reboot macros, the MSB of the MACRO register will stay up until the operation is complete. When MACRO returns to zero, the module is ready for use.

8. Controlling Multiple Modules

8.1. Setting up Master/Slave Systems

The V344/V346 features a dedicated system bus, available on the SYS connector, for connecting and synchronizing multiple modules. This allows any number of modules to be connected together, synchronized to the same clock, and updated simultaneously via Global Events. This SYS bus is fully compatible with that on the T344/T346 embedded waveform generators, and either the VME or embedded modules can be used to control a system containing a mixture of modules.

8.1.1. Overall System Architecture

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										M1	M0				XC
MODCON Register															

Mcode	M1	M0	Module mode	SYS Bus
0	0	0	Standalone	Ignored
1	0	1	Master	Driven
2	1	0	Slave	Locked
3	1	1	Terminating Slave	Locked and 50Ω terminated

Modules are connected by daisy chaining off of a 50Ω synchronization bus. The module physically on one end of the bus (generally the left) should be made the system master, and all others should be made slaves. The module on the far end (generally the right) should be made a terminating slave in order to prevent cable reflections from disturbing the communications.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCM							LER						SYN	S10	LOK
CSTAT Register															

The master module generates an 8 MHz data stream, listened to by all of the slave units. This 8 MHz provides a clocking reference; any module designated a slave will automatically lock its clock to the system master clock, and any errors will be reported in the CSTAT register. When a slave module is properly locked, the SYN bit will be set, indicating the presence of a synchronization signal, and the LOK bit will be set, indicating that lock has been acquired. The LER bit indicates a lock error, and should be clear.

Additionally, the data stream encodes messages known as Global Events which are broadcast to all slave units. All of the units on the bus, master and slave, receive these Global Events and pass them along to all channels. Each channel has both an AE (accept Events) bit in its CTLx register, and a pair of channel addresses (CADs) in its ADDRx register. If the channel is set to accept Events and either CAD matches the target address transmitted as part of the Event it will execute the specified action, otherwise it will simply ignore it.

8.1.2. Cabling and Accessories

Two modules may be connected with any SMB-SMB cable; Highland Technology sells a short one meant to connect two adjacent modules as the J54-1. Up to 16 adjacent modules (128 channels) can be connected with the J346 bussing assembly.

Highland photonic data link products (V720, V730, J720, J724, J730) can be used to synchronize multiple modules over extended distances using fiber optic cabling.

8.2. System-wide Channel Synchronization

8.2.1. Synchronization via VME Global Event Macro

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0			E5	E4	E3	E2	E1	E0
PARAM0 Register as used with Global Event Macro															

Channels on multiple modules can be synchronized through the use of Global Events. In order to send a global event to all of the modules, first write the Global Event code and target address to the PARAM0 register of the master module. The Global Event codes are the same as the TTL Local Event codes.

Ecode	Event Operation
0	none
1	Update channels: transfers settings from channel latches
2	Reset channels: clears phase accumulators
3	Update and Reset
4	Phase Snapshot
8	Fire one-shot channels

With the Event described in PARAM0, write the “Make Global Event” command, 0x841C, to the MACRO register or the master module or the master module. This will transmit the Global Event to all channels that have the AE bit of their CTLx registers set. By using Global Events you can synchronize any number of channels by…

Configure the bus, deciding on which unit will be the system master, and configuring all units’ MODCON registers appropriately.

Confirm via CSTAT that all of the modules have successfully locked.

Program the initial parameters for all of the channels. This includes setting the AE bit to accept global events, and clearing the AU bit to prevent autoupdate.

Send Global Event 3 (Update and Reset) from the master module to load the new channel settings and clear all of the phase accumulators to a known (zero) locked value.

Reprogram all of the channels that need to be changed simultaneously.

Send Global Event 1 (Update) from the master module to load the new channel settings without losing the existing phase.

The ECOUNT register provides a count for all modules of Events that were both received and understood. Only codes listed in the Events table above are understood, others will not increment ECOUNT. Event 0 (No Operation) can be especially handy for confirming that all modules are receiving Global Events properly without making changes to the channels. Each module’s ECOUNT register can be cleared by writing the “Reset Event Counter” command 0x841E to its MACRO register.

8.2.2. Synchronization via Global TTL Events

Just as in the single module case, Global Events can be triggered externally via the TTL EVENT pin (AUX connector pin 21).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		T1	T0		C2	C1	C0								
TTLCTL Register															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0			E5	E4	E3	E2	E1	E0
TTLEVT Register															

Code	C2	C1	C0	Action
0	0	0	0	none
1	0	0	1	none
2	0	1	0	Local Event on rising edge of pin 21
3	0	1	1	Local Event on falling edge
4	1	0	0	Global Event on rising edge
5	1	0	1	Global Event of falling edge

To send Global Events rather than Local Events on a TTL EVENT edge, the C bits in the master module's TTLCTL register must be set to either 4 or 5. Also, the module must be appropriately configured as the system master in MODCON, and all slave units must be configured as slaves.

Upon receipt of the selected edge, the module will transmit the Event indicated by the TTLCTL register to all modules on the SYS bus, both the master and the slaves.

9. Operating Examples

9.1. VME Access

Before programming the V344/V346, basic VME access should be verified. Set the VME address switches as noted in section 3.1, establishing A16 or A24 access mode and setting the module base address. The module is shipped set to base address 0xC000 in the short (A16) address space.

Execute a 16-bit (word) VME read at the module base address, 0xC000 for example. The front-panel blue VME LED should flash and the value read should be 0xFEEE, which is the Highland VXI registered manufacturer's ID. The next register, at base+2 (0xC002 for example) should read back 0x574A, decimal 22346, which identifies the module as a V346, or 0x5748, decimal 22344, which identifies the module as a V344.

9.2. Demo Mode

Writing 0x8411 to the MACRO register will load and run a demo set of waveforms, creating signals on all eight channel output connectors.

9.3. Basic Sine Wave Generation

To make basic sine waves after powerup reset, it is necessary to load only the channel amplitude control (AMPn) and frequency control (FRHn, FRLn) registers. At powerup, all eight amplitude-set registers (AMP0 through AMP7) are set to zero, and the eight channel frequencies are set to 1 KHz through 8 KHz respectively.

After powerup, to make a sine wave on channel 0, write a 16-bit amplitude setting to the word location AMP0, which would be VMEbus address 0xC042 for the default setup. If one writes 0x7FFF to AMP0, the maximum sine wave will be generated, 10.24 volts peak to peak. This 100 KHz sine wave can be measured on C0.

To change the frequency from the default 100 KHz, write to the channel 0 frequency-set register pair FH0 and FL0, as noted in section 5.1.3. This pair of registers must be loaded in order, FH0 first, then FL0. The frequency will change when FL0 is written.

9.4. Loading Other Waveforms

To load triangle waves into a channel's wave memory, set PARAM0 to a bitmask that names the desired channels, then execute the LOAD TRIANGLES macro.

For example, suppose we wanted to change the waveforms of channels 1,3,5, and 7 to be triangles.

Verify that the MS bit of the MACRO register is low

Write bitmask 0x00AA to the PARM0 register (bits 1, 3, 5, and 7 are set)

Write command 0x8406 to the MACRO register

The LOAD SAWTOOTH and LOAD SINEWAVES macros operate similarly.

9.5. PWM Outputs

Each channel may be operated in pulse-width-modulation mode, enabled by setting the PWM bit in that channel's control register. In this mode, the channel outputs a high/low rectangular waveform whose high time is controlled by the value in the channel's PWMn duty-cycle register; see section 5.1.6.

For example, suppose we want channel 4 to generate a TTL-level (0 to 5 volt) pulse that is 10% high and 90% low. We would…

Set the "K" nibble in the CTL4 register to 0x2 to enable unipolar PWM mode

Set channel amplitude register AMP4 to 0x3E80 to set output amplitude to 5 volts

Set channel offset register OFS4 to zero to disable DC offset

Write 0x1999 (6553 decimal) to duty-cycle register DC4.

As the channel frequency is changed, the output will maintain the 10% on/off ratio.

If several channels are used in synchronous mode, the PHA4 register could be used to rotate the phase of the PWM pulse relative to other signals.

9.6. Synchronizing Channels and Phase Control

The default mode of the V344/V346 is for the eight channels to be operated as independent waveform generators. When any channel parameter is changed, such as amplitude or frequency, the internal microprocessor detects the change and loads the appropriate hardware as soon as possible, usually within 250 microseconds, but with no guaranteed timing. In this mode, channel synchronization is not possible and the values in the channel phase-control registers are essentially meaningless.

In order to coordinate channels, it is necessary to place the channels in synchronous update mode, by clearing their AU bits in their channel-control registers. Once a channel is in synchronous mode, changes to its parameters will not be installed until the channel is formally "strobed" by an UPDATE or UPDATE+RESET macro command. The macro allows any combination of channels to be strobed together, allowing phase coherence to be enforced.

For example, suppose we want to generate a 3-phase sine wave set using channels 3, 4, and 5. The sequence would be…

Clear the AU bits in the channel 3, 4, and 5 channelcontrol registers.

Load the identical frequency setting into all three channels. For, say, a 400 Hz system, load FH3 with 0x0001 and FL3 with 0xA36E. Repeat for channels 4 and 5.

Set channel amplitude registers AMP3, AMP4, and AMP5 to the desired values. Writing 0x5863 would set them to 2.5 volts RMS.

Set the channel phase-shift registers. To generate standard 3-phase, set PHA3 to 0x0000 (zero shift), PHA4 to 0x5555 (120 degrees lead) and PHA5 to 0xAAAA (240 degrees lead.)

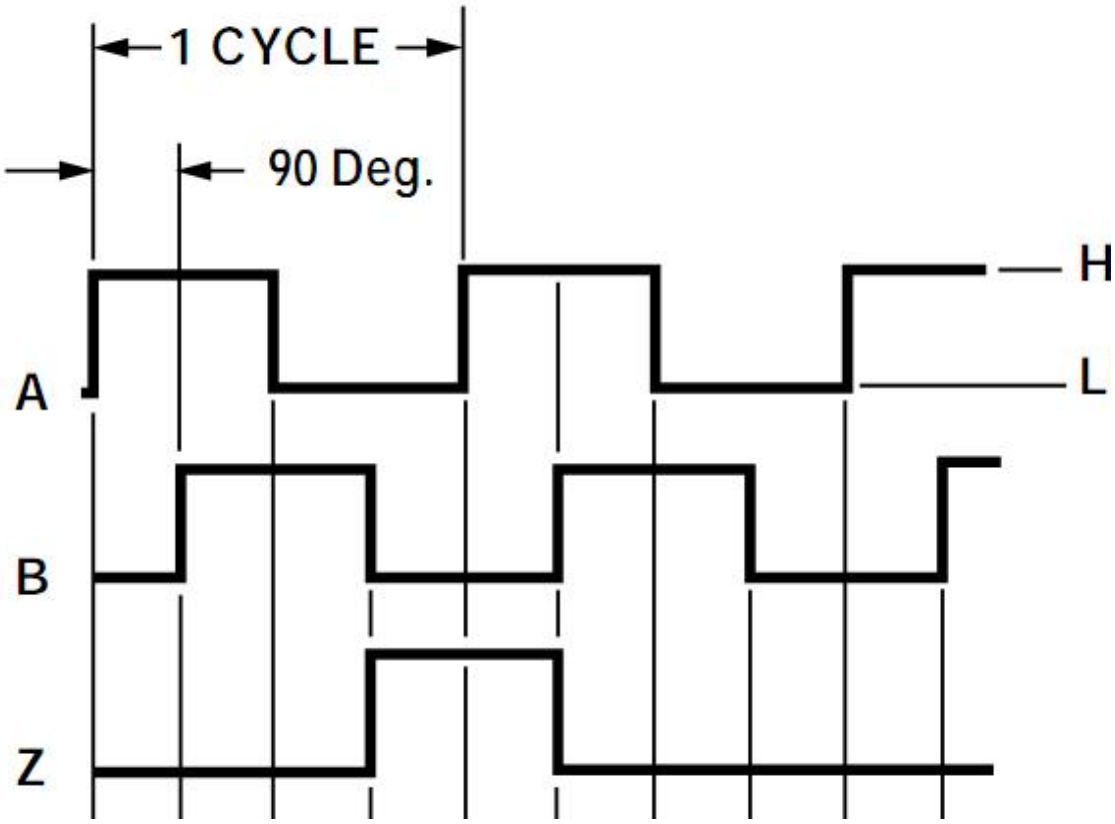
Execute the UPDATE+RESET macro by writing the channel bitmask 0x0038 to the PARM0 register, then writing macro code 0x840B to the MACRO register. Follow the macro handshake procedures noted in section 10.5.

Executing the macro will install the channel settings coherently, setting up the 3-phase waveform set. Later, one can change channel phases, amplitudes, and frequencies and then execute the UPDATE (0x840A) macro, using the same bitmask parameter, to load the new values. Note that the frequencies must always be updated together to maintain phase synchronization.

If a set of channels are to be run at different but synchronized frequencies, proceed as above but load different frequency settings into each channel. To prevent them from slowly drifting in phase, the 32-bit frequency settings, as loaded into the channel's FHn:FLn pairs, must be in mathematically **exact** integer ratios.

If we wanted to run channel 7 at exactly 12 times the frequency of channel 6 while still maintaining phase control, we would operate them in synchronous update mode. We would compute and load the 32-bit FH6:FL6 value for channel 6, and load FH7:FL7 with exactly 12 times that value, then UPDATE+RESET with bitmask 0x00C0 to start them in sync. We could later change the frequencies of channels 6 and 7 by loading a new frequency into channel 6, exactly 12 times that frequency into channel 7, then executing the UPDATE macro with the same bitmask.

Synchronized channels can operate in any waveform or PWM modes.



9.7. Bidirectional Encoder Simulation

The PWM mode can be used to simulate a quadrature encoder. As an example, we could simulate a typical quadrature encoder having 1000 counts per revolution. It would output a pair of quadrature square waves, each making 250 cycles per revolution, and would have a third index output that goes high once a rotation. A typical waveform set is shown below. We could use V346 channels 0 and 1 to make the A and B quadrature signals, and channel 2 to make the Z index pulse. We assume a "half cycle index" as shown below.

We could program the V344/V346 as follows:

Hold channels 0, 1, and 2 reset by setting PARAM0 to 0x0007 to select our three channels, then loading the MACRO register with command 0x8409 to reset. Follow the macro timing rules of section 10.5.

Set the channels to synchronous mode by writing 0x0007 to the SUBS register.

Set the channels to PWM mode by writing 0x0100 to CTL0, CTL1, and CTL2. Set the channels for TTL output levels by writing 0x3E80 to AMP0, AMP1, AMP2, OFS0, OFS1, and OFS2.

Set channels 0 and 1 to 50% duty cycle by writing 0x8000 to PWM0 and PWM1.

The "Z" output (our channel 2) must be high for 1/500 of a rotation for this type of encoder, so set PWM2 to 0x0083, which is decimal 131, namely 65536/500.

Assume we'll start running at 1 revolution per second. Program channel 2, the index, to 1 Hz by setting FH2:FL2 to 0x0000:010C ???. Set the other two channels to exactly 250 times this frequency by setting FH0:FL0 to 0x0001:05B8; repeat for FH1:FL1 ???.

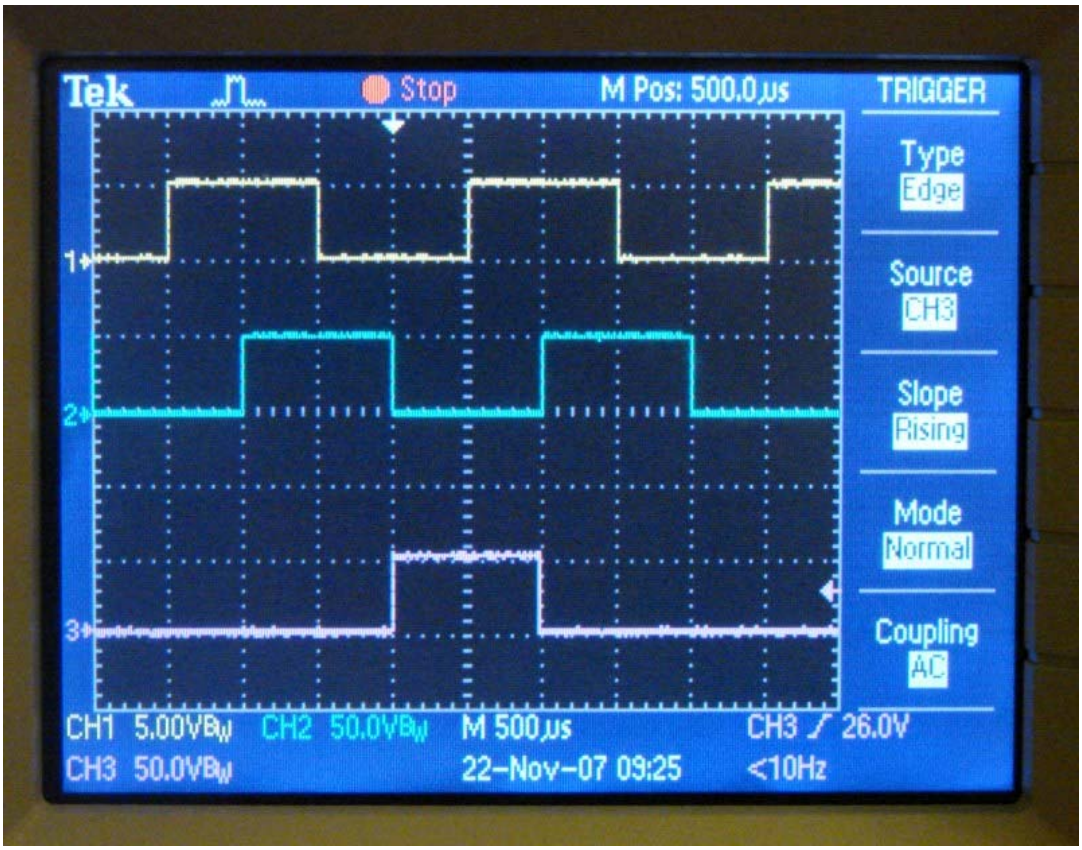
Set the channel phases:

Channel	**Phase**	**Register**	**Value**
2 (Index Z)	0°	PHA2	0x0000
0 (A)	-90° (lag)	PHA0	0xC000
1 (B)	-180° (lag)	PHA1	0x8000

Start the simulation running by writing 0x0007 to PARAM0 (to select our channels again) then writing command 0x840B (UPDATE+RESET) to the Macro register, again following the macro handshake protocol. The encoder will begin at phase angle 0 and simulate clockwise rotation at 1 revolution per second. Speed can be changed, or reversed, by coherently changing the three frequency settings and then executing the UPDATE macro. The frequency control words of channels 0 and 1 must always be numerically exactly 250 times the value of channel 2.

The V344/V346 has no direct mechanism for slewing channel phases to absolute angular positions. Users can implement algorithms which read channel phases, using the phase snapshot macro, and dynamically adjust channel frequencies to converge on and stop at a desired absolute angular position.

The A and B channels could be used in sine wave mode by not setting their PWM control bits. This would simulate an encoder that has quadrature sine outputs.


Tek
Stop
M Pos: 500.0µs
TRIGGER
Type
Edge
Source
CH3
Slope
Rising
Mode
Normal
Coupling
AC
1
2
3
CH1 5.00VBW
CH2 50.0VBW
M 500µs
CH3 ∕ 26.0V
CH3 50.0VBW
22-Nov-07 09:25
<10Hz

10. VME Registers

10.1. Register Map

The V344/V346 implements 256 16-bit VME registers. REG# below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address. The as-shipped default address is 0xC000 in the A16 space.

Registers identified as "RO" should be treated as read-only and should not be written from VME; these registers are periodically refreshed by the module.

The letter "A" in the R/W column indicates that a register pair is atomically locked for 32-bit operations. Atomic pairs must be read or written in the order MS:LS.

Read-write (RW) registers are normally written from VME and, after powerup initialization, are not altered by the internal microprocessor.

Registers tagged RWM can be written by VME or by the internal microprocessor, in accordance with the protocol defined for executing Macro operations.

REG Name	REG#	Offset	R/W	Function
VXI MFR	0	0x00	RO	VXI mfr ID: reads 65262 (0xFEEE)
VXITYPE	1	0x02	RO	Module type: 22344 for V344 22346 for V346
SERIAL	3	0x06	RO	Unit serial number
ROM ID	4	0x08	RO	Firmware ID, typically 22346 decimal
ROM REV	5	0x0A	RO	Firmware revision, typically ASCII "A"
MCOUNT	6	0x0C	RO	Microprocessor IRQ update counter
DASH	7	0x0E	RO	Module version/dash number
TTLCTL	8	0x10	RW	TTL input control
TTLEVT	9	0x12	RW	TTL Event control
RELAYS	11	0x16	RW	Calibration-bus relay controls
ULED	12	0x18	RW	User LED control

MODE	13	0x1A	RW	Module test mode
BERR	14	0x1C	RO	BIST error flags
BISS	15	0x1E	RO	Built-in self-test BIST status
MACRO	16	0x20	RW M	Macro command register
PARAM0	17	0x22	RW M	Macro parameter
PARAM1	18	0x24	RW M	Macro parameter
PARAM2	19	0x26	RW M	Macro parameter
PARAM3	20	0x28	RW M	Macro parameter
PARAM4	21	0x2A	RW M	Macro parameter
PARAM5	22	0x2C	RW M	Macro parameter
YCAL	24	0x30	RO	Calibration date, year
DCAL	25	0x32	RO	Calibration date, month:day
MODCON	26	0x34	RW	Module Control
CSTAT	27	0x36	RO	Clock status
CLIPS	28	0x38	RO	Signal Clipping flags
MODS	29	0x3A	RO	Modulation error flags
ONES	30	0x3C	RO	One-shot complete flags
VZERO	31	0x3E	RO	BIST ADC zero check, 0x0800 nom
CTL0	32	0x40	RW	Ch 0 control register
AMP0	33	0x42	RW	Ch 0 amplitude
FH0	34	0x44	RW A	Ch 0 frequency, MS 16 bits
FL0	35	0x46	RW A	Ch 0 frequency, LS 16 bits
OFS0	36	0x48	RW	Ch 0 DC offset
PHA0	37	0x4A	RW	Ch 0 phase
PWM0	38	0x4C	RW	Ch 0 duty cycle
MOD0	39	0x4E	RW	Ch 0 modulation control (V346 only)

CTL1	40	0x50	RW	Ch 1 control register
AMP1	41	0x52	RW	Ch 1 amplitude
FH1	42	0x54	RW A	Ch 1 frequency, MS 16 bits
FL1	43	0x56	RW A	Ch 1 frequency, LS 16 bits
OFS1	44	0x58	RW	Ch 1 DC offset
PHA1	45	0x5A	RW	Ch 1 phase
PWM1	46	0x5C	RW	Ch 1 duty cycle
MOD1	47	0x5E	RW	Ch 1 modulation control (V346 only)
CTL2	48	0x60	RW	Ch 2 control register
AMP2	49	0x62	RW	Ch 2 amplitude
FH2	50	0x64	RW	Ch 2 frequency, MS 16 bits
FL2	51	0x66	RW	Ch 2 frequency, LS 16 bits
OFS2	52	0x68	RW	Ch 2 DC offset
PHA2	53	0x6A	RW	Ch 2 phase
PWM2	54	0x6C	RW	Ch 2 duty cycle
MOD2	55	0x6E	RW	Ch 2 modulation control (V346 only)
CTL3	56	0x70	RW	Ch 3 control register
AMP3	57	0x72	RW	Ch 3 amplitude
FH3	58	0x74	RW A	Ch 3 frequency, MS 16 bits
FL3	59	0x76	RW A	Ch 3 frequency, LS 16 bits
OFS3	60	0x78	RW	Ch 3 DC offset
PHA3	61	0x7A	RW	Ch 3 phase
PWM3	62	0x7C	RW	Ch 3 duty cycle
MOD3	63	0x7E	RW	Ch 3 modulation control (V346 only)
CTL4	64	0x80	RW	Ch 4 control register
AMP4	65	0x82	RW	Ch 4 amplitude
FH4	66	0x84	RW A	Ch 4 frequency, MS 16 bits

FL4	67	0x86	RW A	Ch 4 frequency, LS 16 bits
OFS4	68	0x88	RW	Ch 4 DC offset
PHA4	69	0x8A	RW	Ch 4 phase
PWM4	70	0x8C	RW	Ch 4 duty cycle
MOD4	71	0x8E	RW	Ch 4 modulation control (V346 only)
CTL5	72	0x90	RW	Ch 5 control register
AMP5	73	0x92	RW	Ch 5 amplitude
FH5	74	0x94	RW A	Ch 5 frequency, MS 16 bits
FL5	75	0x96	RW A	Ch 5 frequency, LS 16 bits
OFS5	76	0x98	RW	Ch 5 DC offset
PHA5	77	0x9A	RW	Ch 5 phase
PWM5	78	0x9C	RW	Ch 5 duty cycle
MOD5	79	0x9E	RW	Ch 5 modulation control (V346 only)
CTL6	80	0xA0	RW	Ch 6 control register
AMP6	81	0xA2	RW	Ch 6 amplitude
FH6	82	0xA4	RW A	Ch 6 frequency, MS 16 bits
FL6	83	0xA6	RW A	Ch 6 frequency, LS 16 bits
OFS6	84	0xA8	RW	Ch 6 DC offset
PHA6	85	0xAA	RW	Ch 6 phase
PWM6	86	0xAC	RW	Ch 6 duty cycle
MOD6	87	0xAE	RW	Ch 6 modulation control (V346 only)
CTL7	88	0xB0	RW	Ch 7 control register
AMP7	89	0xB2	RW	Ch 7 amplitude
FH7	90	0xB4	RW A	Ch 7 frequency, MS 16 bits
FL7	91	0xB6	RW A	Ch 7 frequency, LS 16 bits
OFS7	92	0xB8	RW	Ch 7 DC offset
PHA7	93	0xBA	RW	Ch 7 phase
PWM7	94	0xBC	RW	Ch 7 duty cycle

MOD7	95	0xBE	RW	Ch 7 modulation control (V346 only)
ADDR0	96	0xC0	RW	Ch 0 target address pair
ADDR1	97	0xC2	RW	Ch 1 target address pair
ADDR2	98	0xC4	RW	Ch 2 target address pair
ADDR3	99	0xC6	RW	Ch 3 target address pair
ADDR4	100	0xC8	RW	Ch 4 target address pair
ADDR5	101	0xCA	RW	Ch 5 target address pair
ADDR6	102	0xCC	RW	Ch 6 target address pair
ADDR7	103	0xCE	RW	Ch 7 target address pair
FRHI	112	0xE0	RO A	Frequency counter, MS count
FRLO	113	0xE2	RO A	LS count
FTIM	114	0xE4	RW	Frequency counter timebase/control
PRHI	116	0xE8	RO A	Period measurement, MS
PRLO	117	0xEA	RO A	Period measurement, LS
ECOUNT	118	0xEC	RO	Event counter
BUFFER	128-255	0x100+	RW M	General-purpose data buffer

Registers 128-255 (offset 0x0100 to 0x01FE) are a general-purpose buffer. They are used to load/read waveform memory contents and to deliver channel phase snapshots. Data transfers into or out of the buffer are coordinated by Macro commands; see sections 5.2.2 - Generating Arbitrary Waveforms and 6.3.3 - Taking Phase Snapshots.

10.2. Module Identification/Performance Registers

10.2.1. VXIMFR (0x00)

0xFEEE, Highland Technology's registered VXI ID code.

10.2.2. VXITYPE (0x02)

Module type identifier, either 22346 for a V346 module or 22344 for a V344.

10.2.3. SERIAL (0x06)

Module serial number

10.2.4. ROM ID (0x08)

Firmware version, typically 22346 decimal representing a 22E346 ROM.

10.2.5. ROM REV (0x0A)

ASCII code identifying the revision letter of the firmware, typically 0x41 for “A”.

10.2.6. MCOUNT(0x0C)

The read-only MCOUNT register is an unsigned 16-bit integer which is incremented every microprocessor interrupt, about every 5 ms.

10.2.7. DASH (0x0E)

Module version/dash number, integer 1 for the standard model.

10.3. Function Control Registers

10.3.1. TTLCTL (0x10)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		T1	T0		C2	C1	C0								

This register controls the actions of the two SCSI connector input pins, TTL RESET (pin 20) and TTL EVENT (pin 21).

A transition on the TTL EVENT pin can cause a Local Event or a Global Event. In either case, the event is defined in the low byte, the E0…E7 bits.

The C2..C0 bits determine the operation of the TTL EVENT pin:

Code	C2	C1	C0	Action
0	0	0	0	none
1	0	0	1	none
2	0	1	0	Local Event on rising edge of pin 21
3	0	1	1	Local Event on falling edge
4	1	0	0	Global Event on rising edge
5	1	0	1	Global Event of falling edge

The two T bits determine the effect of the TTL RESET input, connector pin 20.

Tcode	T1	T0	Reset effect
0	0	0	None
1	0	1	None
2	1	0	TTL high on pin 20 holds channels reset
3	1	1	TTL low on pin 20 holds channels reset

Channels recognize this reset input only if they are enabled to accept TTL resets; see 6.12. This operation is local to one module only. The TTL reset function is static, so the channel phase accumulator is held at zero for so long as the reset is in effect.

Note that user writes to the TTLCTL register may take as long as 500 microseconds to become effective.

10.3.2. TTLEVT (0x12)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0			E5	E4	E3	E2	E1	E0

Holds the event to be transmitted when the selected edge is sensed on the TTL EVENT pin. The Event can be sent either just on-board or across a global master/slave system as determined in the TTLCTL register.

The A field, the upper byte of the register, holds the target address (TAD) of the Event. The E field holds the Event Code.

Of the possible 64 Event Codes, the defined operations are…

Ecode	Event Operation
0	None
1	Update channels: transfers settings from channel latches
2	Reset channels: clears phase accumulators
3	Update and Reset
4	Phase Snapshot
8	Fire one-shot channels

10.3.3. RELAYS (0x16)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								K7	K6	K5	K4	K3	K2	K1	K0

If the user sets any bit ON, the corresponding channel test relay will be actuated. The analog output of the associated channel will then be disconnected from its front-panel channel output connector and connected to the internal calibration and testing bus, which may in turn be routed, under control of the MODE register, to the front-panel TEST connector; see section 10.3.5 below.

See section 7.3.2 for discussion of using the TEST connector for verification of module accuracy.

10.3.4. ULED (0x18)

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on. Pattern 0xF000 would result in a blink pattern, 0.5 seconds on and 1.5 seconds off.

10.3.5. MODE (0x1A)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															TM0

The low bit of MODE determines routing of the internal test bus. It is normally zero, which routes the internal test bus to the BIST hardware and disconnects the front-panel TEST connector.

If the user sets test mode = 1 (TM0 bit set) the module's internal test bus is connected to the TEST connector, allowing an external instrument to check the amplitude and frequency of any channel whose test relay is actuated. All channels whose relays are not operated will continue to function normally.

10.4. BIST Status Registers

10.4.1. BERR (0x1C)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADX	CLX							E7	E6	E5	E4	E3	E2	E1	E0

Indicates BIST errors. Bits E7..E0 represent channel errors on channels 7 through 0 respectively, ADX flags an A/D converter error, and CLX indicates that the DDS reference crystal oscillator is failed or excessively off its correct 128 MHz frequency.

10.4.2. BISS (0x1E)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								BSY							BAV

The BAV bit indicates that the BIST facility is available. BSY is true while the BIST self-test is in progress.

10.5. Macro Registers

10.5.1. MACRO (0x20)

Code	Operation	Max Time
0x8400	no operation	250 us
0x8404	Load Sine Waves into channel wave memory	4 ms
0x8405	Load Sawtooth Waves	10 ms
0x8406	Load Triangle Waves	10 ms
0x8407	Load Constant into wave memory	4 ms
0x8408	Hold Channels Reset	400 us
0x8409	Reset Channels	400 us
0x840A	Update Channels	500 us
0x840B	Update+Reset	500 us
0x840C	Snapshot and Read Phases	400 us
0x840D	Read Phases	400 us
0x840E	Write Waveform Memory, 128 words	1 ms
0x840F	Read Waveform Memory, 128 words	1 ms
0x8410	BIST: test module	15 sec
0x8411	Run Demo	50 ms
0x841C	Make Global Event	500 us
0x841D	Fire Channel One-shots	500 us
0x841E	Reset Event Counter	300 us
0x8420	Hard reboot; reloads FPGAs, restarts code; disappears from VMEbus for about 4 seconds	5 sec
0x8421	Soft reboot the module; remains on bus.	20 ms

The macro control register allows invocation of microprocessor service routines. Some macros take or return data in the PARAM0 through PARAM5 registers, or may use the BUFFER space to transfer data. MACRO codes not defined above may be used in factory test and calibration; poking around at them is not advised.

To execute a macro,

Verify that the MS bit (bit 15) of the MACRO register is clear, indicating that the microprocessor is ready to accept a command.

Write any required macro parameters or BUFFER data.

Write a 16-bit macro code to the MACRO register.

Wait until the MS bit again clears, or wait longer than the maximum macro execution time. If any other bits are then set in MACRO, an error has occurred.

Read any returned parameters or BUFFER data.

10.5.2. PARAM0 – PARAM5 (0x22-0x2C)

Macro parameter registers. The use of these depends on the macro that will be executed. See the macro descriptions in the chapters for more details.

10.6. Calibration Date Registers

10.6.1. YCAL (0x30)

Stores the year of the calibration date as an integer, i.e. 2008 (0x07D8) for the year 2008.

10.6.2. DCAL (0x32)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAL MONTH								CAL DAY							

Stores the day of the calibration date as two byte-wide integers, i.e. Feb 29 is 02 (0x02) : 29 (0x1D) is 0x021D.

10.7. System Control Registers

10.7.1. MODCON (0x34)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
										M1	M0				XC

This register is set by users to control module clock and master/slave functions.

If the XC bit is set, the module will lock to an externally-applied 10 MHz clock signal. The CSTAT register reports the state of this lock.

The two M bits select module mode:

Mcode	M1	M0	Module mode	SYS Bus
0	0	0	Standalone	Ignored
1	0	1	Master	Driven
2	1	0	Slave	Locked
3	1	1	Terminating Slave	Locked and 50Ω terminated

If a module is programmed to be a slave, it ignores the XC bit and locks its 128 MHz waveform generator clock to that of the master module.

See section 8.1 for an overview of module synchronization facilities.

10.7.2. CSTAT (0x36)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DCM							LER						SYN	S10	LOK

This read-only register displays the status of several clock-related conditions.

LOK will be true if the module clock is locked to either a 10 MHz reference or to a master module.

The S10 bit will be true if the module senses the presence of an external 10 MHz signal applied to the CLOCK connector.

SYN true indicates the presence of a signal on the SYN connector.

LER is an error flag, true if a lock is expected but not successful.

The DCM bit flags an internal hardware timing error.

10.7.3. CLIPS (0x38)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								V7	V6	V5	V4	V3	V2	V1	V0

Indicates channel saturation errors, caused either by summing channels and DC offsets, or by summing channels with other channels. V7..V0 represent saturation on channels 7 through 0 respectively.

10.7.4. MODS (0x3A) (V346 only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0	F7	F6	F5	F4	F3	F2	F1	F0

Indicates channel modulation overflow errors. A7..A0 represent overflow of the amplitude modulation path for channels 7 through 0, and F7..F0 represent overflow of the frequency modulation path. Always reads 0 on the V344.

10.7.5. ONES (0x3C)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								S7	S6	S5	S4	S3	S2	S1	S0

Indicates one-shot completion on channels 7 through 0.

10.7.6. VZERO (0x3E)

VZERO is a self-test of the BIST analog-to-digital converter. Its nominal value is 2048.

10.8. Channel Control Registers

10.8.1. CTLx (0x40, 0x50, …0xB0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OS	IN	R1	R0	D5	K2	K1	K0		S2	S1	S0	TR	AE		SY

Bit Field	Meaning
OS	Set to enable channel one-shot mode.
IN	Set to enable wavetable linear interpolation.
R	Channel frequency full-scale range: 00 ± 32 MHz 01 ± 4 MHz 10 ± 250 kHz 11 ± 64 MHz
D5	Set to enable analog 5:1 attenuator
K	Channel mode: 000 Wavetable RAM Waveform 001 Bipolar PWM Waveform 010 Unipolar PWM Waveform 011 Gaussian Noise Waveform 100 Wavetable Single Step 101 Control Event Generator (V346 only) 110 reserved 111 reserved
S	Channel summing source: 0 No summing source 1-7 Channels 1-7
TR	Accept AUX connector TTL RESET
AE	Accept Events
SY	Set to disable automatic updates of channel parameters

The CTL0..CTL7 registers are the channel control registers for channels 0-7 respectively. They are explained in greater detail in section 5.1.1.

10.8.2. AMPx (0x42, 0x52, …0xB2)

AMP0..AMP7 are the amplitude registers for channels 0-7. The data is a 16-bit signed fractional, with0x7FFF and 0x8000 representing positive and negative fullscale. This is described more fully in section 5.1.2.

10.8.3. FHx:FLx (0x44:0x46, 0x54:0x56, …0xB4:0xB6)

The FH0:FL0..FH7:FL7 register pairs are the frequency control registers for channels 0-7. The data is a 32-bit signed fractional, with 0x7FFFFFFF and 0x80000000 representing the positive and negative limits of the frequency range defined in the corresponding CTLx register. This is described more fully in section 5.1.3.

10.8.4. OFSx (0x48, 0x58, …0xB8)

The OFS0..OFS7 registers are the DC offset registers for channels 0-7. The data is a 16-bit signed fractional, with0x7FFF and 0x8000 representing positive and negative fullscale. This is described more fully in section 5.1.4.

10.8.5. PHAx (0x4A, 0x5A, …0xBA)

The PHA0..PHA7 registers are the phase rotation registers for channels 0-7. The data is a 16-bit fractional, with 0x0000 representing 0°, 0x4000 representing 90° (or -270°), 0x8000 representing 180° (or -180°), and 0xC000 representing 270° (or -90°). This is described more fully in section 5.1.5.

10.8.6. PWMx (0x4C, 0x5C, …0xBC)

The PWM0..PWM7 registers are the positive duty cycle control register for channels 0-7 when they are operating in PWM mode. The data is a 16-bit unsigned fractional, with 0x0000 representing 0% positive, and 0xFFFF representing 99.9985% positive. This is described more fully in sections 5.1.6 and 5.2.3.

10.8.7. MODx (0x4E, 0x5E, …0xBE) (V346 only)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PW2	PW1	PW0	FR1	FR0	FM2	FM1	FM0		AM2	AM1	AM0		PM2	PM1	PM0

Bit Field	Meaning
PW	Pulse-width modulation source: 0 No pulse-width modulation source 1-7 Channels 1-7
FR	Frequency modulation full-scale range: 00 32 MHz 01 2 MHz 10 125 kHz 11 7.8 kHz
FM	Frequency modulation source: 0 No frequency modulation source 1-7 Channels 1-7
AM	Amplitude modulation source: 0 No amplitude modulation source 1-7 Channels 1-7
PM	Phase modulation source: 0 No phase modulation source 1-7 Channels 1-7

The MOD0..MOD7 registers are the modulation control registers for channels 0-7. They are explained in greater detail in section 6.2. MOD registers are reserved on the V344.

10.9. Channel Address Registers

10.9.1. ADDR0-ADDR7 (0xC0-0xCE)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHANNEL ADDRESS 1								CHANNEL ADDRESS 2							

Stores two channel addresses (CADs) each for channels 0-7. If the channel has the Accept Events bit of the CTLx channel control register set, then it will accept any Event with a target address that matches either of the two CADs. CAD1 and CAD2 are fully interchangeable for all purposes.

10.10. Frequency Measurement Registers

10.10.1. FRHI:FRLO (0xE0:0xE2)

Frequency counter readout. Unsigned 32-bit count of the number of edges that occurred during the time specified by the G field in the FTIM register. See section 7.3.3 for more information.

10.10.2. FTIM (0xE4)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		S1	S0				X2	G7	G6	G5	G4	G3	G2	G1	G0

Bit Field	Meaning
S	Frequency/Period counter source: 0 BIST calibration bus waveform, as per RELAYS 1 Internal 64 MHz clock 2 SYS connector 3 CLK connector
X2	Set to enable frequency counting of rising and falling edges. Clear to count only rising edges.
G	Frequency counter gate time, in 0.1s. 0x01 = 0.1s, 0xFF = 25.5s.

Frequency and period counter control register. Frequency counter is controlled by all fields, period counter is controlled by only the S field. See section 7.3.3 for more information.

10.10.3. PRHI:PRLO (0xE8:0xEA)

Period counter readout. Unsigned 32-bit count of the number of 25ns ticks between rising edges of the signal specified by the CF field of the FTIM register. Periods longer than 1s will be reported as 0xFFFFFFFF. See section 7.3.3 for more information.

10.11. Reporting Registers

10.11.1. ECOUNT (0xEC)

Events count, increments by 1 for each Event recognized. Can be cleared with "Reset Event Counter" macro 0x841E.

10.11.2. BLOG (0xF0-0xFE)

BIST Error log. Shows detailed information on the most recent error detected by the built-in self-test subsystem. See section 7.3.4 for more information.

10.12. Data Buffer

10.12.1. BUFFER (0x100-0x1FE)

Bidirectional data buffer. Used for transferring waveform data, as per section 5.2.2 - Generating Arbitrary Waveforms. Used for retrieving phase snapshot information as per section 6.3.3 - Taking Phase Snapshots.

11. Versions

V344-1 8-channel VME 32 MHz arbitrary waveform generator

V346-1 8-channel VME 32 MHz arbitrary waveform generator w/ complex modulation

12. Customization

Consult factory for information about additional custom versions.

13. Hardware and Firmware Revision History

13.1. Hardware Revision History

Revision C	Dec 2011 Connects K4 and K5 relay signals to FPGA Revision C hardware is slightly slower on the CPU bus than previous revisions
Revision B	Mar 2009
Revision A	Mar 2008 Initial PCB release

13.2. Firmware Revision History

22C346 Revision B	Jan 2012 Removes the clock enables on the address and WE lines to fix a race condition with the falling edge of CS
22C346 Revision A	Apr 2009 Initial channel FPGA release
22E346 Revision C	Jan 2012 Fixes FPGA to compensate for dword accesses to the channel fpga occasionally reading the same word twice, rather than two different words due to slower Revision C hardware

22E346 Revision B	May 2011 Fixes problem with V344 identifying in the module ID register as a V346.22E346
22E346 Revision A	Apr 2009 Initial firmware release for hardware Revision B
22V346 Revision A	Apr 2009 Initial VME FPGA release

14. Accessories

J51	3' shielded-pair 50 pin male SCSI cable
J52	6' shielded-pair 50 pin male SCSI cable
J53	3' SMB to BNC cable
J53-2	6" SMB to BNC cable
J340	50 pin SCSI female BNC termination panel for V34x series digital synchronization outputs
J346-X	SMB trigger bus cable

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