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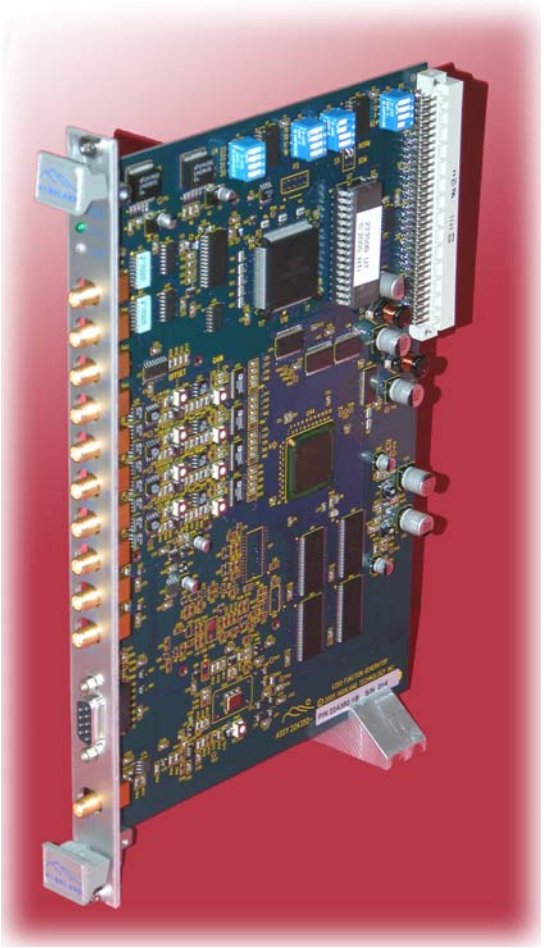
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V350 VME ANALOG/DIGITAL FUNCTION GENERATOR

Technical Manual

May 21, 2011

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1. Introduction

The V350 is a four-channel VME-module analog/digital waveform generator. It is intended for use in the generation of arbitrary waveshapes synchronized with logic-level outputs, as might be used in control system or radar simulation.

The V350 generates waveforms by scanning sequential data points stored in user-loadable memory, with outputs processed by digital-to-analog converters, smoothing filters, and output amplifiers.

Principal features of the V350 include the following:

- Four versatile, command-table-driven waveform generators, each capable of generating one 12-bit analog waveform and up to four digital outputs
- Up to 1M discrete points per waveform at up to 40-MHz clock rate
- Single-shot and looping modes available
- 12-bit waveform amplitude resolution
- Channels may operate independently or may be synchronized within a module or across modules.
- Output stage multiplexing allows flexible configuration.
- Self-test and Demo modes allow quick evaluation and verification.

This manual corresponds to version V350-1B units, Highland assembly 22A350-1B, equipped with firmware version 22350B. See Section 9 for version notes.

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2. Specifications

FUNCTION	4-channel analog/digital waveform synthesis VME module
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16 Implements 128 16-bit registers at switch-selectable addresses in the VME 16- or 24-bit addressing spaces
OUTPUTS	Four channels of arbitrary waveform output, 0:10 volts max, 50 Ω output impedance, 100 mA max Bandwidth 300-KHz full power min Four TTL-level pulse outputs TTL-level waveform sync and pulse sync outputs
INPUTS	One 10-MHz clock input/output Four TTL-level logic inputs
WAVE MEMORY	1M x 16 bits per channel (12 DAC bits, four digital bits)
ACCURACY	Amplitude ±1% Frequency ±1 PPM, lockable to external 10 MHz reference
OPERATING TEMPERATURE	0 to 60° C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies: +5 volts, 1.75 A max +12 volts, 200 mA max (plus load current) -12 volts, 100 mA max
CONNECTORS	SMA female connectors for waveform outputs, pulse outputs, clock D9 female for two sync outputs and four logic inputs
INDICATORS	LEDs indicate processor heartbeat and VME access
PACKAGING	6U single-wide VME module
CONFORMANCE	VMEbus per ANSI/VITA 1-1994 (R2002)

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3. Theory of Operation

3.1 General Architecture

Figure 1 is the overall block diagram of the V350 module.

The module includes the following:

MICROPROCESSOR. A 32-bit Motorola MC68332 embedded CPU supervises module operation. Processor code is stored on a replaceable EPROM chip; this same chip holds the FPGA (gate array) configuration data, allowing hardware and software upgrades in the field.

VME INTERFACE. An FPGA-based interface is used, implementing a bank of 16-bit VME memory locations accessible both from the VME bus and from the internal processor. The module does not use interrupts, and passes all bus grant signals.

WAVEFORM GENERATORS. Four waveform generator Channels A...D are provided.

Each waveform generator includes the following:

A block of VME control registers which provide basic functions and allow access to the channel control RAM.

Channel control RAM, a block of 4096 16-bit words partitioned into 512 control blocks of 8 words each. Each block can initiate and control the execution of waveforms.

A waveform memory holding 1,048,576 16-bit words of stored waveform points. The entire memory is accessible from VME and from the waveform generator.

OUTPUT DACS. Four output DAC/amplifiers DAC1...DAC4 are provided.

Each DAC has a data source multiplexer, allowing any of the four waveform generators A...D to be used to generate the output. Each DAC is followed by a lowpass filter and an amplifier which can provide up to 10 volts peak output.

DIGITAL OUTPUTS. Four digital pulse outputs are provided. Each includes a 16-input multiplexer, allowing any of the available waveform memory “digital” bits to be selected as the logic-level signal source. Thus any digital output may be associated with any waveform. Two additional “sync” outputs are provided, with identical logic.

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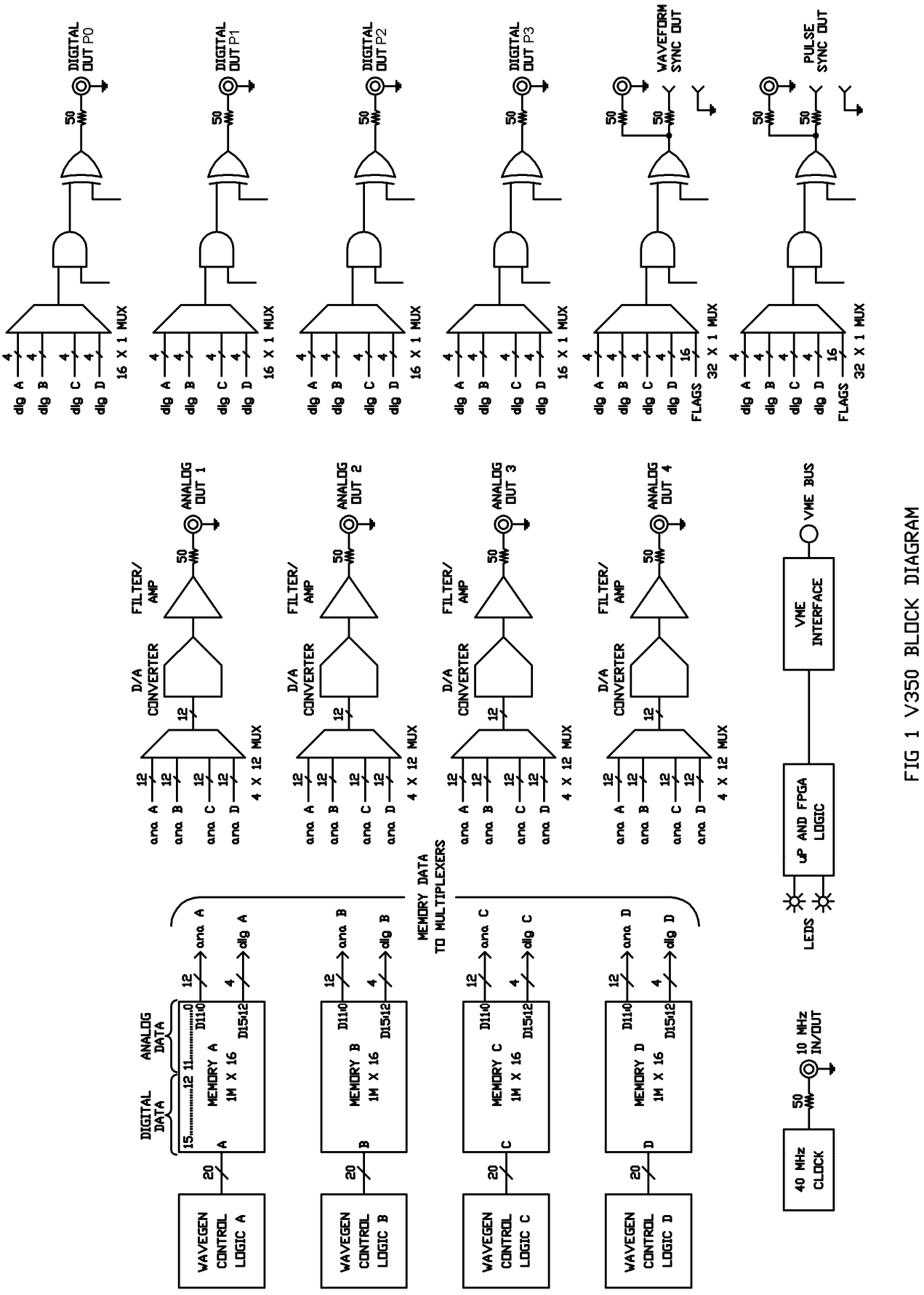


FIG 1 V350 BLOCK DIAGRAM

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OUTPUT CONNECTOR. SMA connectors are provided for all signals, except that a single DB-9 female is used for the two SYNC outputs.

DIGITAL INPUTS. Four TTL-level inputs are provided on the DB-9 connector.

3.2 Nomenclature and Defaults

The four waveform generators are called GENA, GENB, GENC, and GEND, referred to generically as “GENa”. Each has an associated 16-bit waveform memory, “memory a”. The LS 12 bits of memory, namely bits 0…11, are analog waveform data, referred to as “waveform a”. The high 4 bits of memory data are referred to generically as “bitan”, as, for example, “bitC15”, for the MS bit of the C waveform generator memory.

The four DACs are DAC0, DAC1, DAC2, and DAC3, generically referred to as “DAC n”.

The four pulse output channels are P0, P1, P2, and P3, generically “Pn”.

The two sync outputs are WS (waveform sync) and PS (pulse sync).

The four front-panel TTL inputs are called TTL0 through TTL3.

The sixteen global flags are called F0 through F15.

The 12-bit waveform memory data is scaled by the DAC channels as zero volts at waveform data code 0 and 9.99755 volts at code 4095 (0x0FFF)
as measured into a high-impedance load.

The default powerup state is described in Section 6.6.

3.3 Waveform Generators

There are four waveform generators, GENA, GENB, GENC, and GEND. Figure 2 shows the control architecture of one channel.

A waveform is created by writing up to 1,048,576 discrete analog+digital output points into each channel waveform memory, with the memory points being scanned and converted sequentially. The memory output points are processed at a rate determined by the 40-MHz system clock, divided by an individual channel divisor.

Because each channel has its own programmable divisor, channels may be run at integer-fractional speed ratios.

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Each wave generator has a dedicated control memory, consisting of 512 control blocks, each holding eight 16-bit words. Control blocks are "executed" either sequentially or out-of-order via a conditional jump mechanism.

The global VME registers TRIGGER, RESETS, and BUSY each have one bit associated with each wave generator, as described below. Each wave generator has its own block of VME control registers.

The channel DIVISOR register determines the basic clock rate of that wave channel, as a sub-multiple of 40 MHz. If integer “m” is loaded into a divisor, the effective clock rate for that channel is 40 MHz / (m+1).

The read-only wave channel BLOCK register is a pointer to the current 8-word control block in the channel's control RAM. When a channel is reset, the block pointer is cleared, preparing the channel logic to begin execution of Block 0 when a trigger is received.

Wave channel control memory is separated into 8-word executable blocks. Each block includes a control word, wave memory start and stop pointers, a repeat count, a jump address, and a flag control word. Channel control blocks are described in detail below.

3.4 Output DACs

There are four output DAC channels, denoted DAC0, DAC1, DAC2, and DAC3. Each DAC can be selected to use, as its source data, any one of the four waveform generators.

3.5 Digital Outputs

There are six 1-bit digital outputs: P0, P1, P2, P3, WS, and PS.

Each digital output may be programmed to select any of the 16 available waveform memory digital bits, namely BitA12 through BitD15. Each output may also be individually enabled or inverted. The WS and PS outputs may be additionally programmed to output any of the 16 system flag bits.

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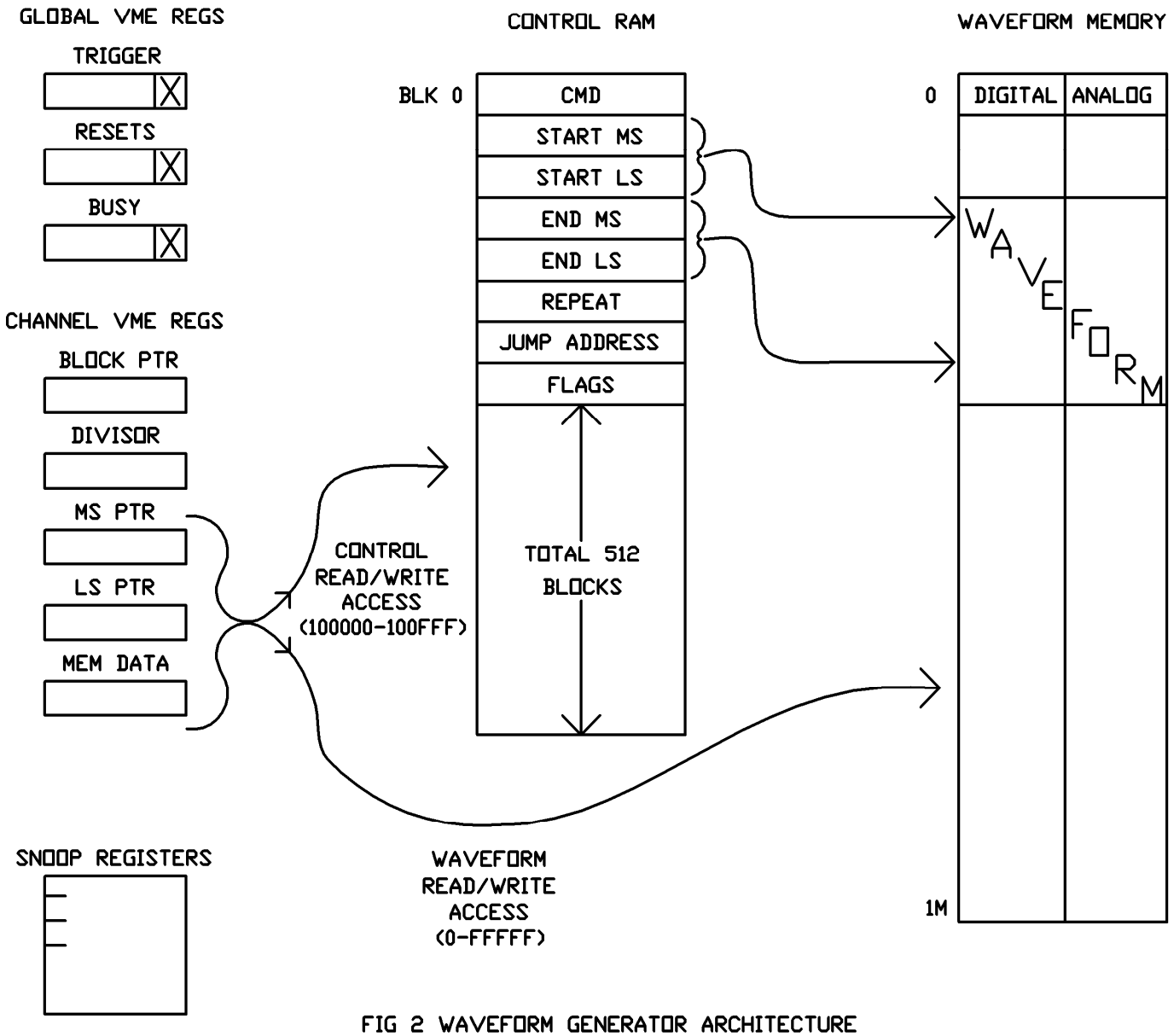


FIG 2 WAVEFORM GENERATOR ARCHITECTURE

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3.6 TTL Inputs

Four TTL logic inputs are provided on the front-panel DB9 connector. These inputs may be used in the following two ways:

They may be read in the TTLS register, as described in Section 5.15.
They may be tested as wave table jump conditions, as noted in Section 3.7.1.
A waveform may be paused until a selected TTL level becomes true.

3.7 Waveform Block Processing

Waveform blocks are resident in each channel's control RAM. Each waveform control block is eight words long; its arrangement is shown in Figure 3.

3.7.1 Block Control Word

The block control word is arranged as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			JM4	JM3	JM2	JM1	JM0	JS	Jmp2	Jmp1	Jmp0	Cmd3	Cmd2	Cmd1	Cmd0

The CMD bits define a block command. There are 16 potential command codes, four of which are currently defined as follows:

0	STOP	Block execution is stopped, and channel BUSY state goes false.
1	PLAY	A waveform is generated from wave ram, from START to STOP pointers, with optional repeat.
2	DELAY	A time delay is executed.
3	WAIT	Hang here until a JUMP condition is met.

When a channel is reset, the current-block counter is set to zero and the waveform point specified by the Block 0 START pointer is output to selected DACs and digital outputs. BUSY will be false until RESET is cleared and a trigger edge is received, at which time BUSY will go true for this channel and Block 0 will begin active execution. Triggers are recognized only when a channel is not busy.

The STOP state freezes the current block address and freezes DAC and digital outputs, and clears the channel BUSY state. The only way out of STOP is a RESET (which jumps to Block 0) or another trigger edge, which reasserts BUSY and causes execution to resume at the block following the STOP.

PLAY will drive DAC and digital outputs from waveform memory points specified in the block START and END pointers. If START equals END and REPEAT is zero, a

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single waveform memory point will be processed and the block will execute for a duration of 25 ns * (D+1) where D is the contents of the channel divisor register. If START is below END, the playback will begin at START, wrap through the end of wave ram (1,048,575 to zero), and end at END.

DELAY is identical to PLAY except that the DAC and digital outputs are not updated. START, END, and REPEAT are thus used only to schedule a time delay. The delay is (END-START+1) * (R+1) * (D+1) clocks long, where a clock is 25 ns, R is the contents of the Repeat parameter, and D is the contents of the channel divisor register. A single block can thus be programmed for a delay of 112e6 seconds, about 3.6 years.

A WAIT block does not update outputs, but hangs until a conditional jump condition is satisfied. Wait is terminated by the jump or by channel reset. Wait always jumps as soon as the specified condition is true, so the FAST/EOB conditions are processed identically.

The three JMP bits define an optional jump operation. Of the eight possible jump actions, three are currently defined as follows:

0	NO: Don't jump.
1	EOB: test and conditional jump at end of block execution.
2	FAST: Conditional jump as soon as selected condition is true.

The JS bit controls the sense of the selected jump condition. If this bit is zero, a jump is enabled if the selected condition is true; if it's a 1, jump is enabled if the condition is false.

The JM (jump mux) bits select a logic level to be tested, namely the jump condition. Selections are as follows:

0..15	System flag bits 0 through 15.
16, 17, 18, 19	Front-panel TTL inputs 0, 1, 2, 3 respectively.
31	Logical "1" bit; allows unconditional jump.

If the JMP mode bits are coded 1 or 2, EOB or FAST, allowing a jump, but the selected jump mux condition is false at the instant it is evaluated, the jump is not taken and the next sequential block is entered.

A common block control word value is 0x1F11. This specifies continuous play of the selected region of waveform memory, with a jump at the end of every pass. Use jump address zero to make this "play" command repeat forever.

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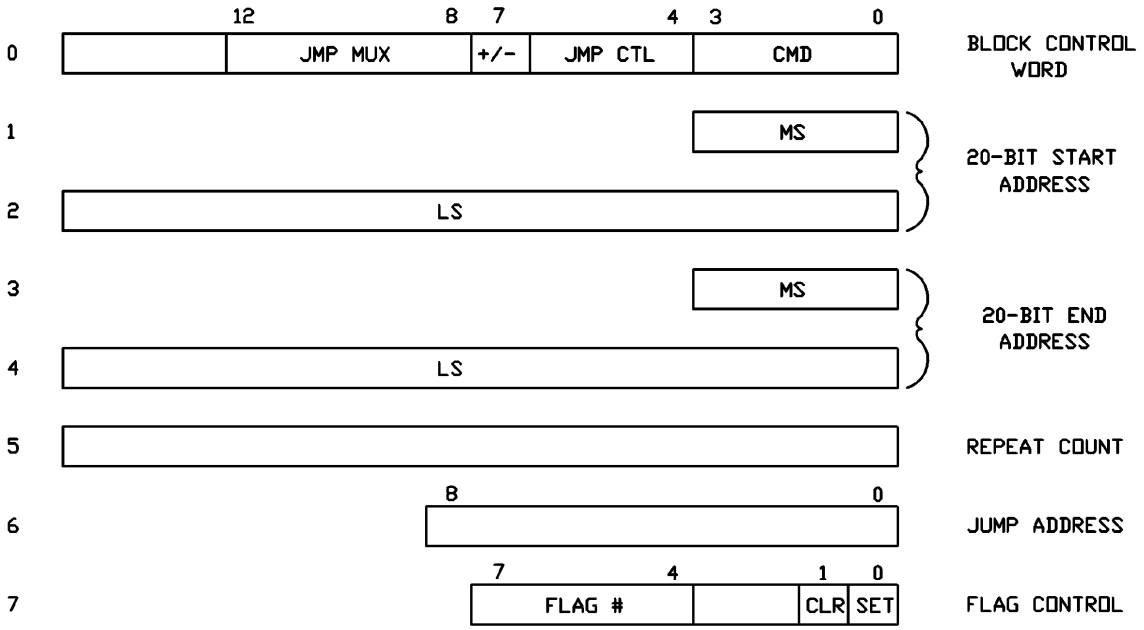


FIG 3 CONTROL BLOCK STRUCTURE

3.7.2 Start Pointer

The START pointer is a 20-bit pointer into waveform memory, presented as 4 MS bits followed by 16 LS bits.

When a block contains the PLAY command, waveform memory points from START to END are scanned, with resulting memory content words available to DACs or digital outputs. If START equals END, a single waveform memory point is played. If START is below END, the playback will begin at START, wrap through the end of wave ram (1,048,575 to zero), and end at END.

3.7.2 End Pointer

The END pointer is a 20-bit pointer into waveform memory, presented as 4 MS bits followed by 16 LS bits.

Note that it is possible to use a PLAY block with an unconditional immediate jump condition programmed to cause only a single waveform memory point (specified by

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START) to be output. For this case, the END value is ignored.

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3.7.4 Repeat Count

The 16-bit REPEAT word specifies that a waveform scan (START to END) be repeated a number of times before this block is done. A value of 0 specifies a single pass, and 65535 specifies 65536 loops. If the parameter is numerically D, the waveform is repeated D+1 times.

3.7.5 Jump Address Word

This word contains the address of the next block to be executed in the case that the control word selects a true jump condition. The 9 LSBs name the next block to be executed. If a jump is not taken, this word is ignored and the next sequential block will be selected.

3.7.6 Flag Control Word

The FLAG word allows this control block to set or clear any one of the 16 global flags in the VME FLAGS register. Coding is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								F3	F2	F1	F0			Clr	Set

The bit specified by the "F" field is either set or cleared, depending on the states of the two LSBs. The set/clear action takes place on the first clock of block execution only, namely when the block execution just begins.

3.8 Some Possible Control Scenarios

A few available waveform control mechanisms include:

Set up waveform channels to use only one control block each, Block 0. Set up each channel's Block 0 to play a region of waveform memory, and to then jump unconditionally to itself at end-of-block time. Now use the VME global RESETS register to reset all channels, and then trigger all channels simultaneously by a write to the global TRIGGERS register. All included wave generators will then start simultaneously and play their waveforms repeatedly until reset.

Assign one wave generator as the master and one or more as slaves. Slaves have their first block programmed as WAIT commands, set up to jump when a system flag goes true. The master channel can include blocks which set system flags, allowing slave waveform to proceed.

Wave generators can include WAIT blocks that suspend wave start until external TTL inputs go true.

See section 8.4 for a basic programming example.

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4. Front-Panel Connectors and LEDs

4.1 Front-panel Connectors

Name	Signal	Connector
DAC0	Analog output 0	SMA
DAC1	Analog output 1	SMA
DAC2	Analog output 2	SMA
DAC3	Analog output 3	SMA
P0	TTL pulse output 0	SMA
P1	TTL pulse output 1	SMA
P2	TTL pulse output 2	SMA
P3	TTL pulse output 3	SMA
WS	TTL waveform sync out	DB9-2 and SMA
PS	TTL pulse sync out	DB9-4 and SMA
TTL0	TTL-level input	DB9-6
TTL1	TTL-level input	DB9-7
TTL2	TTL-level input	DB9-8
TTL3	TTL-level input	DB9-9
CLK	TTL-level 10 MHz	SMA

Pins 1, 3, and 5 of the DB9 female connector are grounded.

The CLK connector may be programmed as an input or an output. As an output, it is a 5-volt CMOS level. As an input, it appears as a 10-MHz bandpass filter with a 1K input impedance. The input filtering makes the phase-lock operation virtually immune to input waveshape and ringing.

4.2 LED Indicators

The module is equipped with two LED indicators.

The green “CPU” LED normally flashes briefly once per second to indicate that the onboard microprocessor program is executing. Possible blink patterns are:

> Brief blink once per second indicates normal operation.
>
> Blinking at 4 Hz indicates a fatal powerup self-test error, namely the failure of the FPGA to properly configure.

The blue “VME” LED flashes whenever the module is addressed from the VME bus.

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5. VME Register Map and Programming

The following is a summary of the VME-accessible registers on the V350 module. A total of 128 16-bit registers are implemented. Switches on the module set the base address, anywhere in the 24-bit or 16-bit VME address spaces.

REG # below is the ordinal register number in decimal. The VMEbus address of a register is

VMEadd = Module base address + REGNUM * 2

The H/S column indicates whether the register is “hard” (FPGA logic) or “soft” (microprocessor serviced). RO, RW, and WO indicate read-only, read-write, and write-only. “WO” registers always read as zero.

REG NAME	REG #	H/S	Function
VXIMFR	0	S RO	VXI vendor ID: always 65262, 0xFEEE
VXITYPE	1	S RO	module type, always 22350, 0x574E
VXISTS	2	S RO	VXI status register
	3	S RO	Unused
ROM ID	4	S RO	firmware ROM ID, typically 22350 decimal
ROM REV	5	S RO	firmware ROM rev, typically ASCII “B”
MCOUNT	6	S RO	microprocessor update counter
ERRH	7	S RO	MS error flag register
ERRL	8	S RO	LS error flag register
MACRO	9	S RW	macro command register
CP0	10	S RW	command parameters
CP1	11	S RW	“
CP2	12	S RW	“
CP3	13	S RW	“
CP4	14	S RW	“
CP5	15	S RW	“
RESETS	32	H RW	Wave channel resets register, 4 lsb's
TRIG	33	H WO	Wave channel “start” triggers, 4 lsb's
BUSY	34	H RO	Wave channel busy flags, read-only
FLAGS	35	H RW	16 flag bits; write bits to set flags
FCLEAR	36	H WO	write bits to clear corresponding flags
CLOCK	37	H RW	10-MHz clock in/out control
TTLS	38	H RO	Shows TTL level states
DAC0	40	H RW	DAC control 0
DAC1	41	H RW	DAC control 1
DAC2	42	H RW	DAC control 2

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REG NAME	REG #	H/S	Function
DAC3	43	H RW	DAC control 3
PMUX0	48	H RW	Pulse output 0 mux
PMUX1	49	H RW	Pulse output 1 mux
PMUX2	50	H RW	Pulse output 2 mux
PMUX3	51	H RW	Pulse output 3 mux
WMUX	52	H RW	Waveform sync mux
PMUX	53	H RW	Pulse sync mux
PTAH	64	H RW	MS pointer into chan A memories
PTAL	65	H RW	LS pointer
DATA	66	H RW	Read/write data, chan A memories
BLKA	67	H RO	Wave generator A current block
DIVA	68	H RW	Wave gen A clock divisor
SNA0	69	H RO	Wave block snoop Block control
SNA1	70	H RO	Wave block snoop Start ptr MS
SNA2	71	H RO	Wave block snoop Start ptr LS
SNA3	72	H RO	Wave block snoop End ptr MS
SNA4	73	H RO	Wave block snoop End ptr LS
SNA5	74	H RO	Wave block snoop Repeat
SNA6	75	H RO	Wave block snoop Flag Control
SNA7	76	H RO	Wave block snoop Jump address
RLAH	77	H RO	Realtime wave location MS
RLAL	78	H RO	Realtime wave location LS
WAVA	79	H RO	Realtime wave memory data
PTBH	80	H RW	MS pointer into chan B memories
PTBL	81	H RW	LS pointer
DATB	82	H RW	Read/write data, chan B memories
BLKB	83	H RO	Wave gen B current block
DIVB	84	H RW	Wave gen clock divisor
SNB0	85	H RO	Wave block snoop Block control
SNB1	86	H RO	Wave block snoop Start ptr MS
SNB2	87	H RO	Wave block snoop Start ptr LS
SNB3	88	H RO	Wave block snoop End ptr MS
SNB4	89	H RO	Wave block snoop End ptr LS
SNB5	90	H RO	Wave block snoop Repeat
SNB6	91	H RO	Wave block snoop Flag Control
SNB7	92	H RO	Wave block snoop Jump address
RLBH	93	H RO	Realtime wave location MS
RLBL	94	H RO	Realtime wave location LS
WAVB	95	H RO	Realtime wave memory data
PTCH	96	H RW	MS pointer into chan C memories

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REG NAME	REG #	H/S	Function
PTCL	97	H RW	LS pointer
DATC	98	H RW	Read/write data, chan C memories
BLKC	99	H RO	Wave gen C current block
DIVC	100	H RW	Wave gen C clock divisor
SNC0	101	H RO	Wave block snoop Block control
SNC1	102	H RO	Wave block snoop Start ptr MS
SNC2	103	H RO	Wave block snoop Start ptr LS
SNC3	104	H RO	Wave block snoop End ptr MS
SNC4	105	H RO	Wave block snoop End ptr LS
SNC5	106	H RO	Wave block snoop Repeat
SNC6	107	H RO	Wave block snoop Flag Control
SNC7	108	H RO	Wave block snoop Jump address
RLCH	109	H RO	Realtime wave location MS
RLCL	110	H RO	Realtime wave location LS
WAVC	111	H RO	Realtime wave memory data
PTDH	112	H RW	MS pointer into chan D memories
PTDL	113	H RW	LS pointer
DATD	114	H RW	Read/write data, chan D memories
BLKD	115	H RO	Wave gen D current block
DIVD	116	H RW	Wave gen D clock divisor
SND0	117	H RO	Wave block snoop Block control
SND1	118	H RO	Wave block snoop Start ptr MS
SND2	119	H RO	Wave block snoop Start ptr LS
SND3	120	H RO	Wave block snoop End ptr MS
SND4	121	H RO	Wave block snoop End ptr LS
SND5	122	H RO	Wave block snoop Repeat
SND6	123	H RO	Wave block snoop Flag Control
SND7	124	H RO	Wave block snoop Jump address
RLDH	125	H RO	Realtime wave location MS
RLDL	126	H RO	Realtime wave location LS
WAVD	127	H RO	Realtime wave memory data

Unassigned registers in the 0-127 range are reserved and should not be written to.

VME Registers are described in detail below. Within each register, bits are numbered 15 (MSB) through 0 (LSB). Bits 7...0 are the LS byte, and bits 15...8 are the MS byte. The V350 allows only 16-bit data writes.

5.1 VXIMFR: VXI Manufacturer's ID

This register displays Highland's VXI-registered manufacturer's ID code. It always reads as 0xFEEE.

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5.2 VXITYPE: Module Type

This register displays the module type. It normally reads as 22350 decimal, 0x574E.

5.3 VXISTS: VXI Status Register

This register implements the VXI-standard status reporting function. Active bits are 2 (PASSED), 3 (READY), and 14 (MODID).

Shortly after powerup, these bits will be set and all other status bits will be zeroes. Note that the module does NOT support the MODID mechanism.

5.4 ROMID: Firmware Version

The microprocessor software version ID is read here, with a typical value of 22350 decimal (0x574E). Other code versions, having different functionality, may have different ID codes.

5.5 ROMREV: Firmware Revision

The revision letter of the firmware may be read at this location, as an ASCII character, “B” (0x42) for the current firmware release.

5.6 MCOUNT: CPU Activity Counter

The MCOUNT register appears as a 16-bit binary counter which is incremented by the microprocessor at about a 512 Hz rate.

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5.7 ERRH, ERRL: Error Reporting Registers

This pair of registers is used by the V350 to report errors which are detected during self-test routines. Any diagnostic routine which detects an error will set its assigned bit. These registers should be all zero after a successful powerup/selftest sequence, or after a requested self-test; any asserted bits flag an error.

Bit assignments are:

ERRL 0	Wave memory A error	ERRH 0	TTL input 0 error
ERRL 1	Wave memory B error	ERRH 1	TTL input 1 error
ERRL 2	Wave memory C error	ERRH 2	TTL input 2 error
ERRL 3	Wave memory D error	ERRH 3	TTL input 3 error
ERRL 4	DAC 0 error	ERRH 4	ADC zero-check error
ERRL 5	DAC 1 error	ERRH 5	VCXO voltage error
ERRL 6	DAC 2 error	ERRH 6	unreasonable temperature
ERRL 7	DAC 3 error		
ERRL 8	P0 digital output error		
ERRL 9	P1 digital output error		
ERRL 10	P2 digital output error		
ERRL 11	P3 digital output error		
ERRL 12	WS digital output error		
ERRL 13	PS digital output error		
ERRL 14	Power supply error		
ERRL 15	Voltage reference error		

In the event of the FPGA failing to configure at powerup, a fatal error, the CPU led will blink rapidly and the microprocessor will attempt to set all 32 error flags.

5.8 MACRO: Macro Command Register

The MACRO register conveys command codes to the microprocessor.
See Section 6 for details of macros and diagnostics.

5.9 RESETS: Reset Control

Bits 3...0, when set from VME, hold wave generators D...A respectively in the reset state. In this state, the generator is stopped, and its divisor counter is initialized. During reset, the wave generator block pointer is held at zero, and the wave generator will statically deliver its first waveform point, which is the point in memory

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specified by the START pointer in waveform control Block 0. When reset is dropped and the channel is subsequently triggered, waveform generation begins from that point.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												RstD	RstC	RstB	RstA

5.10 TRIG: Wave Generator Trigger Register

Bits 3…0, when written as 1's, respectively trigger wave generators D through A. If multiple bits are asserted in a single write operation, the corresponding wave generators will be triggered simultaneously. This register always reads back all zeroes.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												TrgD	TrgC	TrgB	TrgA

5.11 BUSY: Wave Generator Busy Flags

Bits 3…0 when high indicate that the respective wave generator is active.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												BsyD	BsyC	BsyB	BsyA

5.12 FLAGS: Global System Flags

The FLAGS register contains 16 flag bits, named F0 through F15. The flags may be set/cleared from VME or set/cleared/tested by waveform control blocks. To set a flag bit from VME, write a "1" to the appropriate bit in this register. The flags may be read at this address.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	F0

5.13 FCLEAR: System Flags Clear

Writing a "1" to any bit of this register will clear the corresponding bit of the FLAGS register. This register always reads as all zeroes.

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5.14 CLOCK: 10-MHz Clock Control

This register controls the function of the front-panel 10-MHz CLOCK connector.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								Lock						Cin	Cout

If the user sets the Cout bit, the module's internal 10-MHz clock will become a front-panel TTL output. If Cin is set, the connector is an input and the module will attempt to lock its internal crystal oscillator to the external signal. The read-only LOCK bit will go true if the module successfully locks.

5.15 TTLS: TTL Level Monitor Register

This read-only register allow the realtime states of various TTL levels to be read. The low byte displays the front-panel outputs P0 through PS, and the MS byte includes the four front-panel TTL inputs.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
				TTL3	TTL2	TTL1	TTL0			PS	WS	P3	P2	P1	P0

5.16 DACn: DAC Control Registers

Each analog output has an associated D/A converter, with its control register DACn.

15	14	13	12	11	10	9	8	7	6	5	4	2	1	0
													S1	S0

The “S” bits select the source of the 12-bit data that is used by the DAC. Codes are as follows:

0	waveform generator A
1	waveform generator B
2	waveform generator C
3	waveform generator D

Each DAC is unipolar, generating 0…9.99975 volts for DAC codes 0..4095. A hardware option is available for bipolar output.

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5.17 PMUXn, WMUX, PMUX: Digital Output Multiplexer Control Registers

Each of the six digital outputs has an associated control register. Bits are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								FL		INV	Z	M3	M2	M1	M0

The “M” bits select the source (waveform memory and bit) of the digital signal. Assignments are as follows:

M code	**Memory bit**
0	BitA12
1	BitA13
2	BitA14
3	BitA15
4	BitB12
5	BitB13
6	BitB14
7	BitB15
8	BitC12
9	BitC13
10	BitC14
11	BitC15
12	BitD12
13	BitD13
14	BitD14
15	BitD15

If the "INV" bit is set, the digital output will be inverted from the sense of the memory bit that is selected to be the data source. If the "Z" bit is set, the digital output will be held low, and if both INV and Z are set, it will be held high.

For the WMUX and PMUX outputs only, setting FL, bit 7 of this register, enables a system flag to become the logic output, with the M3:M0 bits selecting flag 0 through 15; INV and Z remain operative.

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5.18 Waveform Channel Control Registers

Each of the four waveform generators A, B, C, and D has a block of 16 control registers. The registers for channel A are described below; registers for B, C, and D function identically.

5.18.1 PTAH, PTAL: Memory Read/Write Pointer

PTAH and PTAL constitute a 21-bit pointer. The pointer is loaded by the user to aim at a location in channel control memory or waveform memory.

PTAH:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
											A20	A19	A18	A17	A16

PTAL:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

If A20 is low, the pointer aims at waveform memory (0x000000 - 0x0FFFFF); if it is high, it aims at channel control memory (0x100000 - 0x100FFF). The DATA register is then used to read or write the associated 16-bit memory location, and the pointer auto-increments each time after DATA is accessed. Note that this is a word pointer.

The pointer autoincrements whenever its paired DATA register is read or written. If the pointer is within the waveform segment, autoincrement will roll from 0x0FFFFF to 0x0. If it is in the control space, it will not roll but will hang at 0x100FFF

5.18.2 DATA: Memory Read/Write Data

After the pointer registers are aimed at a memory location, the memory contents may be read or written here.

5.18.3 BLKA: Current Control Block

The low 9 bits of this read-only register indicate the currently-active control block number for this channel. This value will be zero if a waveform generator channel is held reset.

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5.18.4 DIVA: Channel Divisor

A frequency divisor “D” may be loaded into the DIVA register. The effective 40-MHz synthesis rate of waveform generator “A” will be divided by a factor of D+1, allowing division from 1 (D=0) to 65536 (D=65535). The powerup default is D=0, effectively “no division”. If different divisors are used on the various generators, waveforms can be created which simulate gear-ratio couplings. To avoid phase ambiguity, divisors should be loaded while the associated wave generators are held reset.

5.18.5 SNAx: Control Block Snoops

SNA0 through SNA7 are read-only reflections of the 8-word contents of the current waveform control block, namely the block selected by the BLKA register. These are presented for debugging block sequences.

5.18.6 RLAH, RLAL, WAVA: Waveform Snoops

RLAH:RLAL is a read-only, realtime reflection of the 20-bit pointer which is sweeping waveform memory. WAVA is the corresponding waveform memory contents as might be routed to a DAC or a digital output channel. Because these registers may be changing rapidly, reading all three words in succession may not yield a coherent set of values.

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6. Macros and Diagnostics

6.1 Macro Register and Parameters

The MACRO register is used to convey commands to the internal microprocessor. The procedure is...

1. Verify that the low byte of the MACRO register is zero, indicating that the macro processor is not busy.

2. Load the CP0...CP5 registers with any required parameters

3. Load a command code into MACRO. Command are of the form 0x35xx, where the initial "35" is the command "password" and xx is a command code, as noted below.

4. Wait for the low byte of MACRO to clear, indicating the macro has been executed. After execution has completed, the high byte of MACRO will be zero to indicate successful termination; if an error occurred, the high byte will be a nonzero error code.

Following a successful macro operation, values may be returned in the CP0...CP5 registers.

Hex error values, as seen in the MACRO register, are...

0x0000	Macro successfully executed
0x0100	Illegal macro call
0x0200	Bad command parameter
0x0300	Test or data error.

Defined macros are, in hex:

0x3501	Hard Reinitialize
0x3502	Soft Reinitialize
0x3503	Module self-test
0x3504	Run Demo
0x3505	Restore Defaults
0x350B	Read an ADC channel.

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6.2 Macro 3501: Hard Reinitialize

This command causes a hard reset and restart. The FPGA is reset and reconfigured, self-test is run, and the default configuration is installed. This takes about 6.5 seconds to execute, and the module will disappear from the VME bus for most of this time.

6.3 Macro 3502: Soft Reinitialize

This command is similar to the hard reset, except that the FPGA is not reset, so the module remains accessible from VME. Internal variables are cleared, self-test is run, and the default setup is installed. Execution time is below 100 milliseconds.

6.4 Macro 3503: Self Test

This macro performs a basic module self-test; initiate the tests by writing 0x3503 to the MACRO register. After the test, the ERRH and ERRL registers will flag any errors. If any errors are detected, MACRO will return 0x0300 as a summary error indication.

See Section 5.7 for a description of the items tested and the corresponding error flag bits.

Note that this test does a basic check of waveform memories, verifying that all address and data lines are functional and that basic read/write operations function normally. A full memory test would take several minutes to execute from the internal microprocessor, so full-coverage memory diagnostics are best executed from the VME port.

Test of the four TTL inputs verifies that the levels measured by the diagnostic ADC at the input pins are consistent with the levels reported in the TTLS register. TTLs should be unchanging (high or low) during the test. This test cannot guarantee that the TTL data paths are fully functional. Full TTL testing would require that the user toggle the TTL input levels and verify correct indications in the TTLS register.

Loading the DAC outputs will reduce output voltage and may cause errors. Loads down to 5K are acceptable for the self-test.

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6.5 Macro 3504: Run Demo

Writing 0x3504 to the MACRO register invokes demo mode. The default configuration is installed, and then a test pattern is run on all outputs concurrently at about 1-KHz rep-rate.

DAC0 outputs a damped sine waveform.
DAC1 outputs a damped cosine.
DAC2 outputs a 1-cycle sawtooth.
DAC3 outputs a 4-cycle sawtooth.

P0, P1, WS, and PS output a positive pulse at the start of each cycle.
P2 outputs a burst of four pulses.
P3 outputs a burst of 16 pulses.

The DAC0 and DAC1 waveforms will display a spiral on an oscilloscope operating in X-Y mode.

To end the demo, use the Restore Defaults macro.

6.6 Macro 3505: Restore Defaults

This macro places the module in an idle default mode. The setup is…

Wavegen A drives dac 0; bitA15 drives P0 and WS

Wavegen B drives dac 1; bitB15 drives P1 and PS

Wavegen C drives dac 2; bitC15 drives P2

Wavegen D drives dac 3; bitD15 drives P3

All divisors are cleared

All flags are cleared

Channels are reset, then Reset register is cleared

All control ram is cleared

The first location of each waveform ram is cleared

All DAC outputs and TTL outputs are at zero volts.

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6.7 Macro 350B: Read an Analog Value

To read an internal analog value, load CP0 with a channel number (0 to 23 decimal) and then load 0x350B into the MACRO register. After the macro is completed, CP1 will return the analog value. Channels are...

00	P0 DIGITAL OUT
01	P1 DIGITAL OUT
02	P2 DIGITAL OUT
03	P3 DIGITAL OUT
04	PS DIGITAL OUT
05	WS DIGITAL OUT
06	+1.8V FPGA SUPPLY
07	+3.3V LOGIC SUPPLY
08	DAC0 OUT
09	DAC1 OUT
10	DAC2 OUT
11	DAC3 OUT
12	+5A SUPPLY
13	-5A SUPPLY
14	VREF+ (+1.25V)
15	VREF- (-1.25V)
16	TTL0 IN
17	TTL1 IN
18	TTL2 IN
19	TTL3 IN
20	PCB surface temperature
21	VCXO control voltage
22	unused
23	ADC zero check.

Analogs values are presented as a 16-bit signed integer in CP1, with LSB value of one millivolt. Range is at least +-11.5 volts.

Temperature is scaled 100 millivolts, or 100 LSBs, per degree. So temperature in C is CP1/100. Depending on air flow, the reported PCB surface temperature may be roughly 2 to 5 degrees C above ambient. The maximum accurately readable temperature is 75 degrees C.

The VCO voltage should be in the range of 0.5 to 4.5 volts. Values outside this range suggest that the crystal oscillator is near the limits of its adjustment or lock range.

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The ADC zero check should be within +-100 mV.

The DAC outputs are measured at the connector pins. Since the output amplifier has a 50-ohm impedance, external loads will form a voltage divider with this internal impedance and reduce measured voltages.

7. Realtime Considerations

Certain precautions should be taken to avoid unexpected behavior resulting from realtime conflicts in module resource use.

The PTaH/PTaL autoincrement memory pointer registers are shared by the VME host and by the internal microprocessor; these registers increment when their paired DATa register is read or written. Do not write a pointer or access any DATa register during macro execution.

Do not read or write control RAM while a waveform generator channel is busy. The BLKa (current block) and snoop registers may be read at any time.

If waveform memory is read or written during waveform execution, the associated DAC may miss being updated.

Flags may be read, set, or cleared at any time.

It is recommended that divisors be changed while channels are stopped, and that the channel be reset to initialize the divider before running.

The MCOUNT register rolls at about 512 Hz, and pauses during macro execution.

Most macros execute in under 50 milliseconds, except the hard restart, which takes about 6.5 seconds.

Powerup is equivalent to a hard restart. The VME registers are not accessible for about 6.5 seconds, and the default register setups are installed.

Demo mode runs indefinitely after the macro has executed. To stop the demo, execute the Restore Defaults macro or one of the Reinitialize macros.

Unless channel divisors are enabled, control blocks can execute and proceed to the next block (or jump) in a single 25 ns clock. Waveform points are digitized at the 40-MHz rate divided by a programmed divisor.

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8. Setup and Installation

8.1 Safety and Handling Precautions

The V350 module includes static-sensitive components; please observe antistatic procedures when handling the module outside of its antistatic packaging or outside of the VME cardcage.



Do not insert or remove the module with crate power on.
Do not apply any potential to any V350 outputs.

If explosion hazards are possible, connect V350 signals to field wiring through appropriate intrinsic safety barrier devices.

The V350 module has finite failure rates associated with its hardware, firmware, and documentation. Do not apply the V350 in data acquisition or control systems where a failure or defect in the module may result in injury, loss of life, or property damage.

8.2 Switch Setups

8.2.1 A16/A24 Addressing Mode Switch

One DIPswitch position is labeled A16 A24. Press the appropriate side of the switch to permit operation in VME systems which use A16 (16 bit) or A24 (24-bit) addressing. See example in section 8.4.

In A16 mode, the module responds to VME address modifiers 29 and 2D hex. In A24 mode, address modifiers are 39 and 3D hex.

8.2.2 VMEBUS Address Switches

The module VME base address is set by on-board DIPswitches. The switches are labeled A9 through A23. To set an address bit true, press the side of the switch opposite the “OFF” marking. If the module is in A16 mode, only switch positions A9 through A15 are decoded.

Example: to use the module at base address C000 in the A16 space, press the A24/A16 switch section nearest its A16 position, and set the A15 and A14 address switches ON, with all others OFF.

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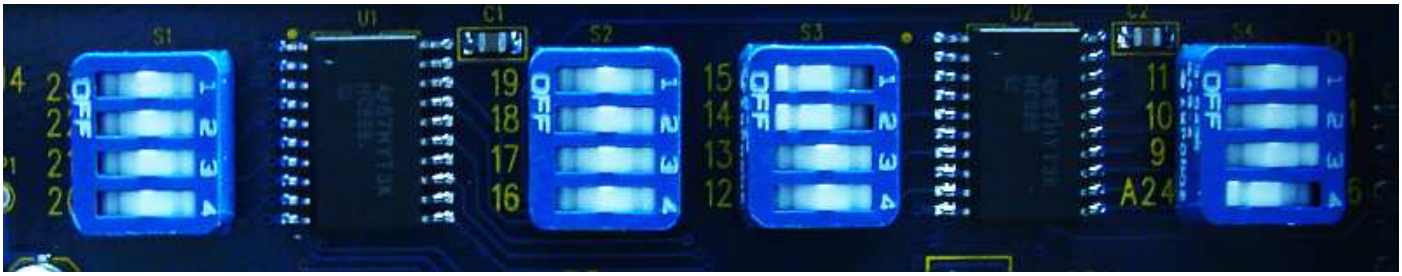
8.3 Installation in a VME Crate

The V350 may be installed in any standard 6U VME backplane. The module connects to the backplane J1 connector only. The standard V350-1 does not use interrupts and passes all interrupt and bus grant signals. Seat the module firmly and secure both front-panel mounting screws before applying power.

8.4 Quickstart Example

The following procedure will generate a simple test waveform on the DAC0 output of the V350.

Install the V350 in a VME crate. For this example, we assume that the dipswitches are set for base address 0xC000 in the 16-bit VME space, as shown:



Power up the crate and run a host program that allows read/write accesses to the short, A16, VME address space.

Read 16-bit module register 0, at address 0xC000. It should read back value 0xFEEE, which is Highland's registered VXI manufacturer's ID code. The front-panel "VME" LED should flash.

Read the next register, register 1, at 0xC002. It should contain decimal 22350, 0x574E, indicating that this module is a V350.

After powerup, the module should be in its default state. To ensure this condition, one may write value 0x3502 to register 9, VME address 0xC012. This is the "soft reset" macro command. Wait at least 100 milliseconds for this to execute.

We will load a simple 5-step staircase waveform into waveform generator A, and output that to DAC0.

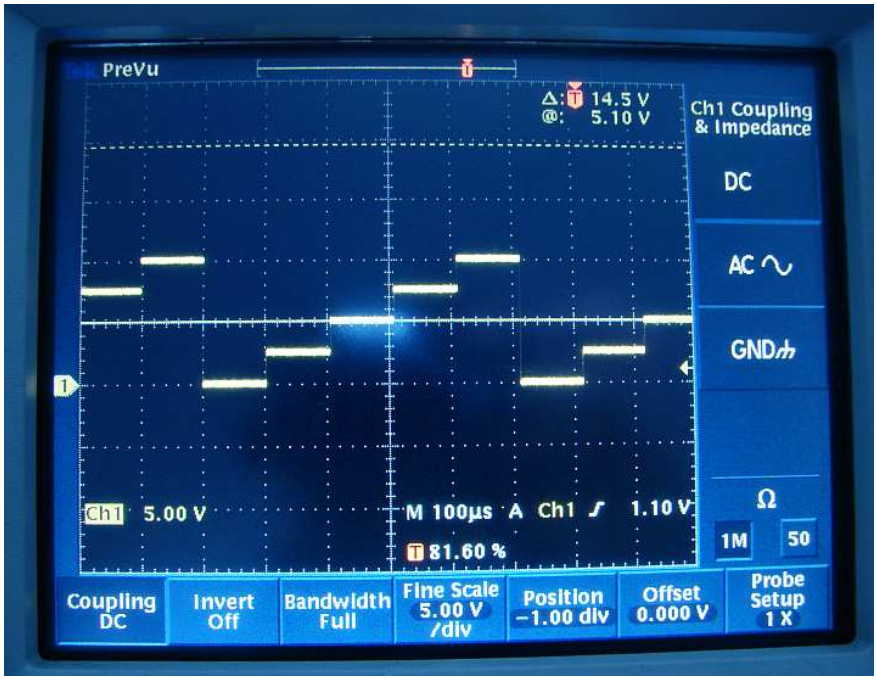
The waveform will repeat at 1953.125 Hz, namely 40 MHz / (4096 * 5)

Now write to module registers in the following sequence:

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Register	Reg #	Address	Write Data	Comment
DIVA	68	0xC088	0x1000	set clock divisor to 4096
PTAH	64	0xC080	0x0000	aim memory pointer to 0,
PTAL	65	0xC082	0x0000	start of waveform memory
DATA	66	0xC084	0x0000	load waveform memory, add 0
DATA	66	0xC084	0x0400	load waveform memory 1
DATA	66	0xC084	0x0800	load waveform memory 2
DATA	66	0xC084	0x0C00	load waveform memory 3
DATA	66	0xC084	0x0FFF	load waveform memory 4
PTAH	64	0xC080	0x0010	aim memory pointer to 0x100000,
PTAL	65	0xC082	0x0000	control block 0
DATA	66	0xC084	0x1F11	block 0 command = continuous run
DATA	66	0xC084	0x0000	waveform start pointer, long,
DATA	66	0xC084	0x0000	= 0
DATA	66	0xC084	0x0000	waveform end pointer, long,
DATA	66	0xC084	0x0004	= 4
DATA	66	0xC084	0x0000	zap repeat count
DATA	66	0xC084	0x0000	Jump address = 0 to repeat block 0
DATA	66	0xC084	0x0000	zap flags
TRIGS	33	0xC042	0x0001	trigger wave generator A

Now the waveform at J5, the DAC0 connector, should look like...



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A few cautions:

We assumed the default setup, which pipes the waveform generator "A" data to DAC0; specifically, the DAC0 register contains zero.

We also assumed that, in the default state, the waveform generators are idle (untriggered) but the RESETS register is clear. In general, to ensure that all generators are idle, one could write to the RESETS register, first 0x000F, then 0x0000.

The multiple writes to the DATA register must indeed write to the same VME bus address, not to successive addresses. Some programming APIs do not allow this in a single call, so multiple write calls may be needed.

The PTAH:PTAL pointer pair autoincrements every time the DATA register is read or written, so extra operations can get the pointers out of the expected sequence.

9. Versions and Firmware

V350 modules are characterized by an assembly part number (22A350), a hardware revision letter, a version dash number, and a firmware version.

The assembly revision letter and dash number appear on the surface of the PC board. Firmware ID is shown on the label on the EPROM chip, and may also be read from the ROM ID and ROM REV registers.

Firmware is incorporated in the form of a plugin EPROM chip that may be upgraded in the field. This chip includes both the microprocessor code and the FPGA configuration file.

Initial units were hardware version 22A350-1A with firmware 22350A. These were prototypes and are not installed in the field.

The first production units were 22A350-1B furnished with firmware version 22350B.

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