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V365

VME

TACHOMETER/

OVERSPEED

MODULE

Technical Manual

August 24, 2010

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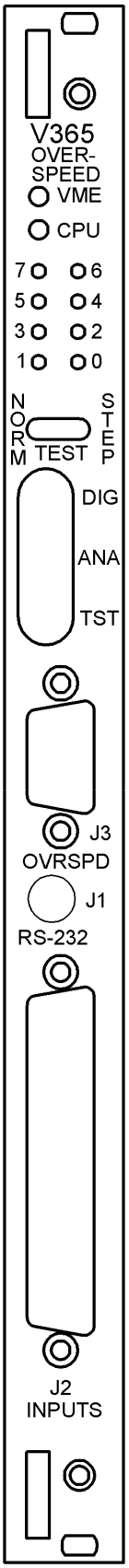
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WARNING: The V365 is a commercial product. It has finite failure rates associated with its design, construction, components, firmware, and documentation. The V365 must not be relied on as the sole protection mechanism for protection of life or property.

Users should make use of all available test mechanisms and redundancy to ensure that the module is operating properly, in order to minimize the likelihood of unexpected behavior.



CAUTION: Please note safety and handling precautions in Section 6.1.

1. Introduction

The V365 is a single-width, 6U height VME module designed specifically to acquire low frequency inputs from industrial speed sensors. The module can measure frequency and period over a wide dynamic range, and is specifically designed to ensure reliable measurement in high-noise industrial environments. It is a superset of the Highland model V360 VME tachometer module.

Features of the V365 include:

Intelligent 8-channel period/frequency/RPM measurement.

Ideal for signal conditioning of magnetic speed pickups, flowmeters, and encoders.

High noise immunity ensures accurate measurement in industrial environments.

Internal signal conditioning accepts direct input from common speed sensors.

Register-based 16-bit VME module, VXI compliant.

Includes four programmable overspeed/underspeed blocks, each with SPDT relay output.

Clean, simple architecture simplifies programming.

Differential signal inputs are signal conditioned, filtered and presented to the inputs of a custom gate array chip which manages period and frequency measurement. An on-board 68000-series microprocessor periodically reads the timer chip, checks and scales data, and loads measured period values into a dual-port memory interfaced to the VMEbus. Users may calculate frequency or RPMs from period.

The input signal conditioners can be connected directly to common transducer types, including…

variable reluctance or hall-effect magnetic speed pickups

AC line voltage or alternator windings up to 150 volts RMS

optical pickups

reed-switches or unconditioned fuel flow meters

contact closures or other special levels.

2. Specifications

FUNCTION	8-channel signal conditioner/tachometer/overspeed module
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16:D08(EO) Implements 32 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
INPUTS	Eight channels, numbered 0 through 7 Each channel has differential inputs, ground, and auxiliary +12 volt source Input impedance is > 60 K to ground on differential inputs Signal level inputs are configurable for standard TTL, open collector, AC generator, and variable reluctance sensor pickups Onboard signal conditioning includes VME-selectable gains, filtering/integration, and trigger levels to accept 10 millivolt to 150 volt RMS signals up to 100 kHz Inputs will tolerate 1000 volt transients for 50 µs
RANGE	32 bit period measurement with 20 ns LSB resolution, approximately 85 seconds maximum period Transparent interlock logic allows skew-free reading of 32-bit period data
ACCURACY	± 0.005% ±1 LSB
RELAY OUTPUTS	Four isolated SPDT over/under speed output relays, Fujitsu type FTR-B3 Contacts rated 1 amp at 30 VDC, 0.3 amps at 120 VAC, resistive loads
RS-232 PORT	9600 baud RS-232 port is provided This provides for monitoring of module performance and permits channel configuration without requiring host CPU programming
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year

POWER	Standard VME supplies: +5 V: 0.5 A +12 V: 0.2 A -12 V: 0.15 A
CONNECTORS	D37 female connector for signal inputs and current-limited +12 volt excitation outputs HD15 female connector provides four SPDT relay contacts for overspeed/underspeed function 2.5 mm stereo phono connector for RS-232 serial port Three SMB signal monitor connectors present analog and digital signal levels of any selected channel and access test frequency signal
INDICATORS	Ten LEDs indicate processor heartbeat, VME access, and individual channel trigger activity
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec

3. Functional Model

3.1 General Architecture

Figure 1 is the block diagram of the V365 VME Tachometer module.

The module provides eight tachometer input channels, numbered 0 through 7. Each input channel includes a differential input amplifier with two user selectable gain settings, and choice of signal conditioner: a programmable second-order lowpass filter (best for conditioned logic-level or switch inputs) or an integrator (best for velocity-type sensors such as variable-reluctance pickups or alternator windings). Each lowpass filter is programmable to have bandwidths of 100 Hz, 1 KHz, 10 KHz, or 100KHz.

Each processed analog signal is compared by two fast precision comparators which define user selectable high and low trigger thresholds.

The digital trigger signals are processed by a custom reconfigurable gate array. For each channel, the gate array implements a programmable divide-by-N prescaler followed by a 32-bit timestamper and an associated pulse edge counter.

For each channel, the comparators provide a pulse for each sensor edge, typically corresponding to one gear tooth, one contact closure, or one AC voltage cycle. The prescaler may be programmed to divide this pulse train by a user-selectable factor between 1 and 255. This feature can reduce measurement jitter when the sensed device does not have perfect rotational symmetry or when noisy signals are processed. For example, if a 20-tooth gear is sensed with a VR pickup and the gear teeth are not precisely identical, a pre-divisor of 20 will ensure that only full shaft rotations are measured, using the same gear tooth to measure each period.

The output of the divide-by-N stage is routed to a per-channel edge counter and edge timestamper, with the timestampers capable of measuring the time-of-pulse-edge to a resolution of 20 nanoseconds.

The processor periodically polls the gate array to read all 8 sets of latched counter data, at about a 1 KHz rate. Each time the processor scans the gate array, it reads the timestamp and edge counts for each channel and computes period. At high input frequencies (above about 1 KHz), the processor will observe multiple edges and thus transparently revert to a multiple-period averaging mode, reducing reported period jitter, and clock quantization. The “last best” period value of each channel is thus computed and posted to VME at the 1 KHz rate.

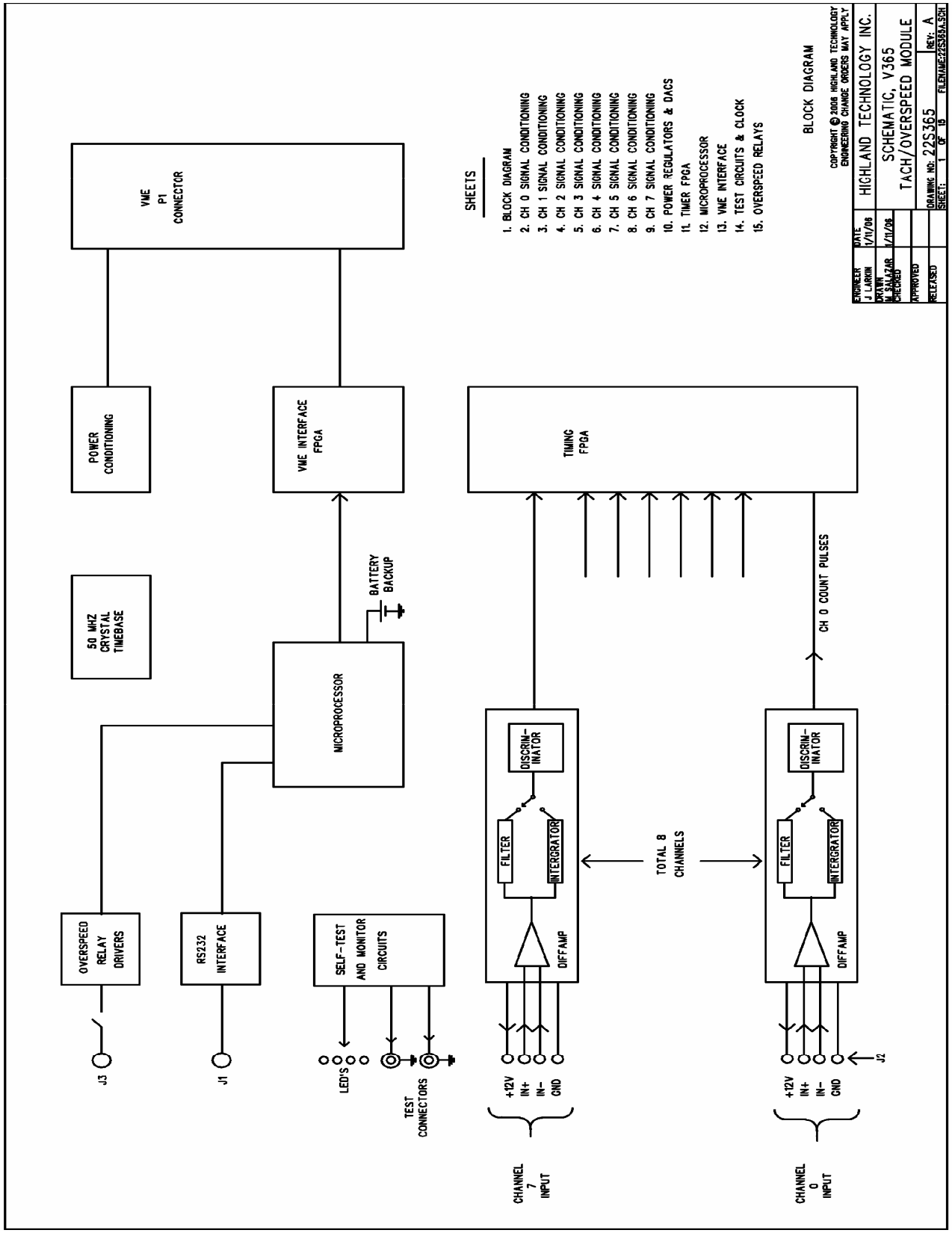


Figure 1. V365 Block Diagram

The microprocessor formats measured periods into 32-bit data words for presentation to a second gate array. This second FPGA includes a 32-bit wide dual-port memory which allows the microprocessor to write period data which is then readable by the VMEbus.

When the VME master reads a period value, it must read the data as two separate 16-bit words. In order to ensure that the read is atomic, the FPGA logic senses when the first word (at the lowest VME address) is read, and coherently saves the second 16-bit word of the 32-bit period value. The user then reads the second word without hazards associated with asynchronous update of period values by the local microprocessor.

The 32-bit period data is always “high endian”, with the most significant 16 bits in the first, lowest, VME address.

Period is reported as a 32-bit value with LSB resolution of 20 nanoseconds, equivalent to a 50 MHz clock. If a channel is prescaled, the reported time is that of “N” input pulses.

Four SPDT relay contacts are provided for overspeed/underspeed use. See Chapter 7 for details of this subsystem.

3.2 Input Signal Conditioning

Each of the eight input channels has an input signal conditioning circuit as illustrated in Figure 2. The channel electronics consists of…

An input resistor network which provides high-voltage withstand capability, high-frequency rolloff, switchable attenuation, and provision for injection of a test signal

±5 volt signal swing clamps;

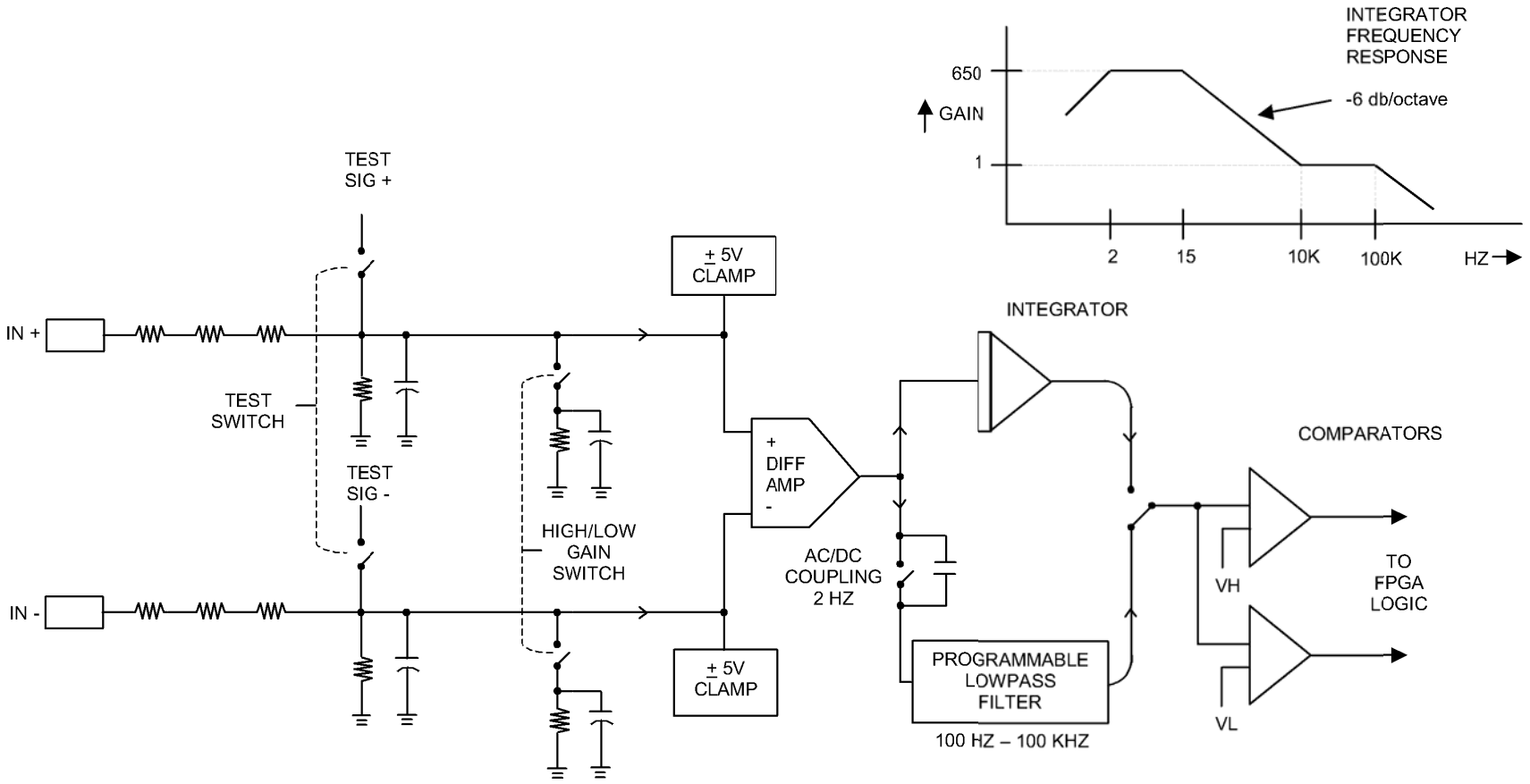
A unity-gain differential amplifier;

A switchable signal path, incorporating either

an AC/DC coupling circuit followed by a switchable-bandwidth lowpass filter, or

an integrator for equalization of rate-type signals;

A dual-level discriminator.



ALL SWITCHES ARE SOLID-STATE PROGRAMMABLE
INPUT ATTENUATOR HAS 100 KHZ LOWPASS
RESPONSE AT ALL GAIN SETTINGS

V360 CHANNEL INPUT
SIGNAL CONDITIONING
FIG 2

3.3 Trigger Discriminators

The conditioned signal, from either the lowpass filter or the integrator, is applied to two precision comparators, each of which has a trigger threshold set by a programmable digital-to-analog converter. The comparators are used in two different modes.

If the input path enables the lowpass filter, both comparators are programmed to have positive thresholds, with one level establishing the “signal high” threshold and the other setting the “signal low” threshold. The difference between these two levels is the trigger hysteresis. Users may select low or high hysteresis levels, which the onboard microprocessor translates into appropriate comparator thresholds.

If the signal is a reasonably symmetric sinusoid or rectangular pulse train, the lowpass filter should be programmed to pass the highest expected input frequency. Filter selections are 100 Hz, 1 KHz, 10 KHz, and 100 KHz. Avoid enabling excessive bandwidth to keep noise and jitter to a minimum.

If the input signal consists of narrow positive pulses, the DC-coupled mode and dual above-zero trip points are appropriate to ensure reliable triggering. In this case, the filter bandwidth should be selected to pass the narrow pulses irrespective of the pulse reprate. The 100 KHz range will pass 10 microsecond or longer pulses, and the 100 Hz range will pass 10 millisecond or wider pulses. If the input is narrow negative pulses, the differential input leads should be reversed to effectively make the pulses positive.

If the input path enables the integrator, the user-furnished thresholds are set symmetrically above and below zero volts, as the “high” and “low” trigger levels. The effective trigger level is then zero volts, with a hysteresis of two times the threshold setting. With the attenuator off, the integrator gain is about 650 from 2 Hz to 15 Hz, falls off at 6 dB/octave to unity gain at 10 KHz, and is flat from 10 K to 100 KHz. This curve is a good match for many velocity-type sensors whose signal level varies linearly with frequency and may be very small at low speeds. The integrator is symmetrically clamped to overload cleanly.

3.4 Period Measurement Algorithms

The algorithm used to measure period is as follows:

Trigger pulses are received from the input signal conditioning logic, one pulse per rising edge of the sensor input.

The pulse train is divided by the programmable divide-by-N prescaler, with division ratio of 1 to 255.

Every resulting pulse edge simultaneously increments an edge counter and snapshots a master timestamp counter. The master timestamp is a 32-bit free-running 50 MHz binary counter.

Every 1.02 milliseconds, the microprocessor reads the latest channel edge count and timestamp. If one or more edges have been counted since the last read, the number of edges and the timestamp are used to compute the signal period.

Each channel may be placed in one of three timing modes:

MODE 0: RUNDOWN. If no count edges are seen by the timing system, it is possible that the pulse train has stopped; this would leave the last-good period measurement in force, falsely implying that the input period remains at the old value. To prevent this error, the processor, when it checks a channel's counters and discovers “no edges”, computes what the period would have been had an edge been sensed. If this value is greater (longer period) than the last real period, the substitute value is posted as the channel period. The net effect is that, if a pulse train abruptly ceases, the reported period will increase smoothly to the maximum (all 1's, 85.899 seconds) value. When the pulse train resumes, a new period will be posted whenever a valid period is sensed.

MODE 1: PERIOD. In this mode, the module reports the last measured full period. After 85.5 seconds of inactivity, the reported period will be set to the maximum value, and two new triggers will be required before a new, valid period can be reported.

MODE 2: USER TIMEOUT. In this mode, the user may specify a no-signal timeout interval of up to 67 seconds. The last valid period will be reported, unless no signal edges have been seen for more than the specified timeout. After the timeout is exhausted, the maximum (all 1's) period is posted.

See Section 5.8.1 for a discussion of channel configuration.

4. Front-Panel Connectors and LEDs

4.1 Connector J1: RS-232 Interface

A female 2.5 mm stereo connector J1 is provided to interface to a PC serial port for configuration settings and test. Use of the RS232 port is purely optional, and is not required for normal operation from the VME bus.

Connection to a typical laptop PC will require an adapter cable, Highland Part Number T565 or equivalent. A drawing of this cable is available from Highland.

4.2 Connector J2: Channel Inputs 0...7

The 8 channel inputs are wired to the female D-37 connector J2. Plus and minus balanced input signals, 12 VDC excitation, and ground pins are provided for each channel as follows:

Pin #	Signal Name
1	VME signal ground
2	VME signal ground
3	+12 excite
4	VME signal ground
5	+12 excite
6	VME signal ground
7	+12 excite
8	VME signal ground
9	+12 excite
10	VME signal ground
11	+12 excite
12	VME signal ground
13	+12 excite
14	VME signal ground
15	+12 excite
16	VME signal ground
17	+12 excite
18	VME signal ground
19	VME signal ground

Pin #	Signal Name
20	VME signal ground
21	channel 7 input -
22	channel 7 input +
23	channel 6 input -
24	channel 6 input +
25	channel 5 input -
26	channel 5 input +
27	channel 4 input -
28	channel 4 input +
29	channel 3 input -
30	channel 3 input +
31	channel 2 input -
32	channel 2 input +
33	channel 1 input -
34	channel 1 input +
35	channel 0 input -
36	channel 0 input +
37	VME signal ground

Note: If an open-collector or switch input is used, the IN-terminal should be connected to ground and the IN+ terminal should be connected to +12V through a pullup resistor; 2.7 K, 1/4 W is suggested.

The +12 volt pins may be used to power external pullups or signal conditioners. All are commoned, and share a single foldback current limiter device from the VME +12 volt supply. Total current drain should not exceed 0.5 amps for all excitation loads. If the load current exceeds 0.5 amps and the current limiter is activated, it may be necessary to remove loads or cycle power to reset the current limiter.

4.3 Overspeed Relay Outputs Connector J3

One female high-density D15 connector J3 is provided to access the four overspeed-trip relays. The connector on the V365 is a Kycon type K66-E-15S-N, a 15-pin VGA-style connector with the DE ("D9") size shell. Pinout is:

Pin #	Signal Name
1	Relay A NC
2	Relay B NC
3	Relay C NC
4	Relay D NC
6	Relay A COM
7	Relay B COM
8	Relay C COM
9	Relay D COM
11	Relay A NO
12	Relay B NO
13	Relay C NO
14	Relay D NO

Unnamed pins are not connected. Since relays are by default de-energized on an overspeed fault, the "fault" condition would have J3-1 continuous to J3-6.

See Section 7 for discussion of overspeed operation.

4.4 SMB Channel Monitor Connectors

The two SMB connectors allow the user to connect a dual-trace oscilloscope to the module to observe the analog input signals and the resulting conditioned digital signal which is used for period measurement. A front-panel-accessible switch selects the channel to be monitored.

SMB connector J6, labeled "Analog", provides for monitoring the selected signal-conditioned analog signal input. This signal is the output of the lowpass filter or integrator. The “raw” input signal may be observed by temporarily reprogramming the channel config register to operate in wideband (100 KHz) filter mode.

SMB connector J5, labeled "Digital", provides for monitoring the actual digital timing trigger of the selected pulse signal input. This is the signal on which period measurement is performed, with the rising edge defining the end of each period. This signal is sampled before the programmable divide-by-N prescaler.

4.5 SMB Frequency Test Connector

SMB connector J4, labeled "Test", is used for self-test of tachometer channels. It can operate as an input or as an output.

The user-loadable TDIV parameter selects the function of this connector, as discussed in Section 5.8.5. If the internal test generator is enabled, users may program a test frequency from 10 Hz to 200 KHz which is applied to the internal test bus, and the TEST connector becomes an output to monitor this frequency. In this case, the output at TEST is a square wave of about 5 volts p-p, AC coupled, with a 100 ohm source impedance. Users should monitor this with a high-impedance oscilloscope or frequency counter.

If the internal test generator is disabled, the connector then becomes an AC-coupled input, with a gain of 1.0 from the connector to the differential test bus, and a bandwidth from 5 Hz to 200 KHz.

Any tach channel that is set to TEST mode will be driven from the test bus signals instead of its normal inputs; see 5.8.1.

A 3-foot SMB-to-BNC coaxial cable is available for connection of a V365 SMB connector to an oscilloscope or signal generator. It is Highland Model Number J53.

4.6 LED Indicators and Test Switch

The module is equipped with 10 LED indicators.

The green “CPU” LED flashes once per second to indicate that the on-board microprocessor program is executing. The blue “VME” LED flashes whenever the module is addressed from the VMEbus.

There are eight amber channel LEDs, labeled “0” through “7”. When the test select switch is in its leftmost NORM position, each LED flashes when the corresponding channel receives active input signal transitions. If prescaling is enabled, the LED flashes are activated from the output of the divide-by-N prescaler.

When the select switch is in the center TEST position, the eight LEDs serve to indicate which channel's signals are routed to the two SMB test connectors. Pressing the test switch to the momentary right STEP position steps through the channel selections, with one amber LED steadily illuminated to indicate which channel is selected. In this case, the conditioned analog channel signal will appear at the ANALOG connector and the discriminated digital signal will appear at the DIGITAL connector.

When the test switch is in its NORM position, the DIGITAL test connector output will be a 5 MHz square wave which may be used to check the accuracy of the internal 50 MHz oscillator.

The position of the TEST switch never affects tach or overspeed functions.

4.7 Connector/Cable Summary

Function	Connector on V365	Required Mate	Notes
Tach inputs	J2 female D37	male D37	Highland # 42027 Shell # 42025
Overspeed relays	J3 female HD15	male HD15	Highland #42024 Shell # 42809
Test connectors	3 ea SMB socket	SMB plug	SMB-BNC cable is Highland J53
RS232 connector	J1 2.5 mm stereo jack	2.5 mm plug	Cable to D9 serial port is Highland T565

5. VME Register Map and Programming

The following is a summary of the VME-accessible registers implemented by the V365 module. The module follows VXI conventions, having 32 each 16-bit registers beginning at the base address. Switches on the module set the base address, anywhere in the 24-bit or 16-bit VME address spaces.

All registers are 16 bits wide. Reg # below is the ordinal register number in decimal; OFFSET is the VMEbus address offset from the module base address, shown in hex. The R/W column indicates whether the register is readable and/or writable from the VMEbus.

Reg Name	Reg #	Offset	R/W	Function
VXI MFR	0	0x00	R	VXI manufacturer ID: always 65262, 0xFEEE
VXITYPE	1	0x02	R	module type, always 22365, 0x575D
MODSTS	2	0x04	R	module status register
OSTAT	3	0x06	R	Overspeed status register
ROM ID	4	0x08	R	firmware ROM ID, typically 22365 decimal
ROMREV	5	0x0A	R	firmware ROM revision, typically ASCII “A” and test-mode flags
MCOUNT	6	0x0C	R	microprocessor update counter
TDIV	7	0x0E	R	test signal frequency divisor
CMD	8	0x10	RW	module command register
PARM1	9	0x12	RW	command parameter 1
PARM2	10	0x14	RW	command parameter 2
PARM3	11	0x16	RW	command parameter 3
PARM4	12	0x18	RW	command parameter 4
PARM5	13	0x1A	RW	command parameter 5
--	14	0x1C	R	unused, always 0
OFOR	15	0x1E	RW	overspeed relay force register
P0HI	16	0x20	R	channel 0 high word period data

Reg Name	Reg #	Offset	R/W	Function
P0LO	17	0x22	R	channel 0 low word period data
P1HI	18	0x24	R	channel 1 high word period data
P1LO	19	0x26	R	channel 1 low word period data
P2HI	20	0x28	R	channel 2 high word period data
P2LO	21	0x2A	R	channel 2 low word period data
P3HI	22	0x2C	R	channel 3 high word period data
P3LO	23	0x2E	R	channel 3 low word period data
P4HI	24	0x30	R	channel 4 high word period data
P4LO	25	0x32	R	channel 4 low word period data
P5HI	26	0x34	R	channel 5 high word period data
P5LO	27	0x36	R	channel 5 low word period data
P6HI	28	0x38	R	channel 6 high word period data
P6LO	29	0x3A	R	channel 6 low word period data
P7HI	30	0x3C	R	channel 7 high word period data
P7LO	31	0x3E	R	channel 7 low word period data

VME Registers are described in detail below. Within each register, bits are numbered 0 (LSB) through 15 (MSB). Bits 0...7 are the LS byte, and bits 8...15 are the MS byte.

5.1 VXI MFR Register: VXI Manufacturer's ID

This register displays the VXI-registered manufacturer's ID code. It always reads as 0xFEEE.

5.2 VXI Type Register: Module Type

This register displays the module type. It normally reads as 22365 decimal, 0x575D.

5.3 MODSTS Register: Module Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
KD	KC	KB	KA	S7	S6	S5	S4	S3	S2	S1	S0	0	0	0	0

Bits 15...12 of this register reflect the realtime state of the relay coil drive to the four overspeed channel relays. If a bit is asserted, the corresponding relay coil is energized.

Bits 4 through 11 reflect the realtime electrical level of the channel 0 through 7 differential inputs respectively, with a high bit corresponding to an electrically positive input level. It is rising edges of these bits which are timestamped to determine channel periods.

This register is reloaded every uP interrupt, every 1024 microseconds.

5.4 OSTAT: Overspeed Status Register

See Section 7.1 for details.

5.5 ROMID Register: Firmware Version

The MC68332 microprocessor software version ID is read here, with a typical value of 22368 decimal (0x5760). Other code versions, having different functionality, may have different ID codes. See Section 9 for a summary of firmware versions.

5.6 ROMREV Register: Firmware Revision

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T7	T6	T5	T4	T3	T2	T1	T0	0	rev	rev	rev	rev	rev	rev	rev

The low byte of this register reflects the revision letter of the module firmware, as an ASCII character. “B” (0x42) denotes the initial production firmware release.

Bits 8-15 reflect the self-test states of tach channels 0 through 7 respectively. If the TEST bit is set in a tach channel control word, its flag bit will be asserted here. Users should check this byte to ensure that no tach channels are inadvertently left in TEST mode, which could invalidate tach and overspeed functions. See Section 5.8.1.

5.7 MCOUNT/TDIV Registers

The MCOUNT register appears as a 16-bit binary counter which is incremented by the microprocessor just after all eight measured period values are refreshed into the VME-readable dual-port memory. Refresh occurs every 1024 microseconds, at 976.56 Hz, and lasts for about 50 microseconds.

TDIV is the 16-bit test oscillator divisor, as discussed in Section 5.8.5.

5.8 CMD Register: Module Command

Certain data transfers are managed using the module COMMAND register and the associated PARAMETER registers. The bits in the COMMAND register are:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERR								DONE	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Bit	Name	Function
6...0	CCODE	command code
7	DONE	set by V365 to indicate operation complete
15	ERR	set by V365 to indicate error

The protocol for executing commands is as follows:

The VME master reads the COMMAND register and waits for the DONE bit to be true.

If DONE is true,

write command parameter registers as desired;

write a command code (bits 0...6 only, other bits OFF) to the COMMAND register.

Wait for the DONE bit to reappear.

Check the ERR bit to see if the command was rejected.

Read any parameter registers if appropriate.

After a command has been executed, the module will simultaneously set the DONE and (if an error) ERR bits. The old command bits 0...6 will be unchanged.

Bits 8...14 of the command register may return error codes or other status information.

Defined commands are as follows:

Command Code Hex	Function
0x8	read module name
0x9	write module name
0x0A	reset module
0x0B	set self-test frequency divisor
0x10	read channel 0 configuration
0x11	read channel 1 configuration
0x12	read channel 2 configuration
0x13	read channel 3 configuration
0x14	read channel 4 configuration
0x15	read channel 5 configuration
0x16	read channel 6 configuration
0x17	read channel 7 configuration
0x18	write channel 0 configuration
0x19	write channel 1 configuration
0x1A	write channel 2 configuration
0x1B	write channel 3 configuration
0x1C	write channel 4 configuration
0x1D	write channel 5 configuration
0x1E	write channel 6 configuration
0x1F	write channel 7 configuration

Command Code Hex	Function
0x20	read channel 0 name
0x21	read channel 1 name
0x22	read channel 2 name
0x23	read channel 3 name
0x24	read channel 4 name
0x25	read channel 5 name
0x26	read channel 6 name
0x27	read channel 7 name
0x28	write channel 0 name
0x29	write channel 1 name
0x2A	write channel 2 name
0x2B	write channel 3 name
0x2C	write channel 4 name
0x2D	write channel 5 name
0x2E	write channel 6 name
0x2F	write channel 7 name
0x30	overspeed commands; see Section 7.

5.8.1 Channel Configuration Command

Each of the eight channels must be configured for the transducer type and measurement options. To configure a channel, load the three command parameter registers and execute the appropriate command, as noted above.

Bits in the configuration registers establish type, gain, filter, threshold, rundown, and hysteresis settings, and engage the self test signal.

When configuring a channel, the parameter register functions are as follows:

PARM1: channel control bits

PARM2: trigger threshold

PARM3: prescaler count

PARM4: mode 2 period timeout

The channel control bits (transferred in PARM1) are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					M2	M1	M0	TEST	FLT1	FLT0	INT	ATTN	HYST	AC	

Bit	Name	Function
0	--	Not used.
1	AC	When set, enables AC coupling of the input signal.
2	HYST	Sets hysteresis HIGH in filter mode.
3	ATTN	Engages the 25:1 signal input attenuator.
4	INT	If set, selects the wide range integrator for velocity-type magnetic pickups. If this bit is off, channel works in filter mode.
5	FLT0	Selects filter cutoff frequency.
6	FLT1	Selects filter cutoff frequency.
7	TEST	Engages self-test override signal to channel input.
8	M0	Channel timing mode.
9	M1	Channel timing mode.
10	M2	Channel timing mode.
11-15	--	Not used.

The three MODE bits establish channel timing mode. Currently-defined modes are:

M2 Bit10	M1 Bit9	M0 Bit8	Timing Mode
0	0	0	Period measurement, rundown enabled.
0	0	1	Period measurement, rundown disabled.
0	1	0	Period with user-specified timeout

The AC bit, when set, enables AC coupling of the signal into the trigger comparators. The low-frequency cutoff point is about 2 Hz. This bit is ignored in integration mode.

The HYST bit is functional only in filter mode. If set, it selects high (50%) hysteresis, and when clear selects low (10%) hysteresis.

The ATTEN bit, when set, activates the channel input-signal attenuator, reducing front-end gain by 25:1. This bit should be set when interfacing with high-level transducers. The inputs are protected to 150 VRMS each regardless of the ATTEN bit setting.

The TEST bit, if set, replaces the input signal with a 2-volt p-p test signal; see Section 5.8.5. The ATTEN bit is inoperative during test.

The INT bit, when set, routes the input signal through the wide-range integrator, and allows the user to set symmetric positive and negative trigger thresholds. Integrator mode should be used for devices that have an analog signal level which is proportional to frequency, such as unconditioned magnetic pickups or alternators. The HYST, AC, and filter-select bits are ignored when in INT mode.

If INT is false, the module works in lowpass filter mode. In this case, the FILT1 and FILT0 bits set the filter bandwidth, as follows:

FILT1	FILT0	Filter Bandwidth
0	0	100 Hz
0	1	1 KHz
1	0	10 KHz
1	1	100 KHz

In filter mode, the Tn bits set the positive trigger threshold, and the HYST bit selects low or high hysteresis.

The trigger threshold is communicated in the low eight bits of PARM2. This value can be considered to be the trigger level, scaled from 0 to 255, corresponding to electrical trigger levels from 0 volts to +5 volts (about 20 millivolts per LSB). If the input attenuator is set to ATTEN mode, the effective (relative to input) trigger level scaling becomes 0 to +125 volts for trigger level codes 0 to 255, about 0.5 volts/LSB.

The count prescaler value is transmitted in the PARM3 register. Legal values may be from 0 to 255. If the value is 0 or 1, the input prescaler is disabled and every input pulse is applied to the period measurement logic. For higher values of PARM3, the input pulse train is divided by the specified value before period measurement is made.

If channel mode 2 is specified, channel parameter 4 must be loaded when the channel is configured. This is a 16-bit unsigned integer which defines the desired no-signal timeout interval. Timing is in units of 1/976 seconds, for a maximum range of 64 seconds.

Example

To set up channel 5, one might do the following:

Read the command register, verify DONE bit true.

Write 0x0044 to PARM1 (DC, no attn, high hysteresys, 10 KHz filter, mode 0).

Write 0x0040 to PARM2 (trigger level 1.25 volts).

Write 0x0024 to PARM3 (prescale divisor = 36).

Write 0x1D to the command register (write channel 5 config).

Read command register; loop till DONE bit true, check for error.

To read back channel setups, execute the appropriate “read config” command code, verify DONE, and then read the four parameter registers.

Since all commands are guaranteed to execute in less than two milliseconds, users may prefer a non-handshake method of executing commands. To do this, the sequence is…

write parameter registers if appropriate,
write command register,
wait at least 2.5 milliseconds,
read parameter registers if appropriate.

Note: The V365.EXE program may optionally be used to assist in configuring modules in two different ways:

1. Modules may be configured by running V365.EXE on a PC which is connected to a V365 module via a serial cable. This allows configuration to be done without the requirement that the VME host deal with the configuration rules.

2. V365.EXE may be run on any PC without connection to a V365, and be used as a “configuration compiler”. One can configure a hypothetical module and save the configuration to a disk file. The readable disk file will summarize the module setup and list a table of hex channel parameters and command codes required to set the module into that configuration. The literal hex values may then be written by the VME host to the actual V365 module.

5.8.2 Set Channel Name Command

The V365 will store a 10-character name for each channel. This may be useful for tracking channel setups, especially when setup is done from the serial port but data readout is via VME.

A name is a 1- to 10-character ASCII string. To write the name, load the five parameter registers with the desired text and execute the appropriate WRITE NAME command. To read back names, execute a READ NAME command, and then read the parameter registers.

By convention, the first character of the name is the MS byte of the first parameter word, and the last character is the LS byte of the fifth parameter word. Factory default names are " Channel 0" through "Channel 7”. If the user writes any control codes (0x1F and below) within the name, the V365 will convert them to spaces.

5.8.3 Set Module Name Command

The module may be assigned a 10-character name, using the associated WRITE MODULE NAME and READ MODULE NAME commands. These commands are similar to the channel name commands discussed above. The default is "V365 Tach”.

5.8.4 Module Reset Command

The module may be reset to a default state by executing the RESET command. To execute this operation, set PARM1 to 0x1129 and then write command code 0x0A to the command register.

All channels will be configured to the default powerup setup, as described in Section 6.6. The V365 will disappear from the VME bus for about two seconds as the reset is executed.

5.8.5 Test Oscillator Set Command

The internal TDIV parameter may be loaded by writing an integer "TDIV" into the PARM1 register and then writing command code 0x0B to the CMD register.

The arrangement of the parameter TDIV is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PRE	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

where PRE is the "prescale" bit and bits 14...0 are interpreted as an unsigned 15-bit integer "D" with value from 0 to 32767.

There are three cases:

A. If parameter TDIV is zero, the test oscillator is disabled and the SMB "Test" connector J4 becomes an input. Users may then apply a signal to J4, and it drives the internal differential test bus.

B. If TDIV is nonzero and the PRE bit is false, the module generates an internal test signal whose frequency is…

   Ftest = 5,000,000 / D

   The legal range of D is from 25 (200 KHz) to 32767 (152.59 Hz).

C. If TDIV is nonzero and the PRE bit is true, the module generates an internal test signal whose frequency is…

   Ftest = 312,500 / D

   Here, the legal range of D is from 25 (12.5 KHz) to 32767 (9.537 Hz).

When the internal generator is active (TDIV is nonzero), connector J4 is an output where users may monitor the internally-generated test signal.

The current value of the TDIV parameter may be read in the TDIV register.

Only tach channels having their TEST bit set in their channel control words will respond to the signal on the internal test bus.

5.8.6 Test Dual-Port Memory Command

A data test pattern may be run on the VME dual-port memory. To invoke this function, load a time interval value “K” into the PARM1 register and load command code 0x0C into the command register. The test pattern will be run for K/976 seconds. During the test interval, the first 16 VME registers will not be modified by the module and are available to the VMEbus master for full read/write testing access. The high 16 registers remain read-only, with preassigned test patterns appearing instead of the normal eight longword time period values.

Each channel period value is alternately written with a defined 32-bit pattern alternating with its complement. The test patterns are:

Channel	Reg #	Offset	Test Pattern
0	16	0x20	0x0123ABCD
1	18	0x24	0x13F634D1
2	20	0x28	0x2C634B71
3	22	0x2C	0x3AA86C4D
4	24	0x30	0x47BA652F
5	26	0x34	0x5D5A4B62
6	28	0x38	0x67C2A551
7	30	0x3C	0x70A53CF2

These patterns may be read and verified as being either the correct test pattern or its complement. This verifies all VME data and address paths and tests the 32-bit “atomic read” logic.

At the end of the test, the channel periods will return to "live" values, and the read-only registers in the low-16 group will resume their normal values. If users alter any of the read/write registers during the test interval, they must take care to restore them to acceptable settings before the test times out.

5.9 OFOR: Overspeed Force Register

See Section 7.2.

5.10 Period Readout Registers

Each channel has a pair of associated period readout registers, named PxHI and PxLO. To ensure coherent data, the PxHI register must be read before reading the PxLO register. When PxHI is addressed, both the HI and LO period data are read from dual-port memory, and the PxLO data is buffered for the subsequent read of the low data.

Each channel has its own low data buffer latch so that, in a multi-tasking environment, one task can read certain time registers and a different task can read others without creating hazards. If multiple tasks must be able to read all registers, another mechanism should be used to ensure that 32-bit period values are correct; double-read-and-compare is suggested.

The 32-bit value reported in any PxHI:PxLO register pair is simply the period of the measured waveform, scaled in units of 20 nanoseconds, equivalent to timing the period using a 50 MHz clock. So if the register pair is treated as an unsigned 32-bit integer P...

P = 50e6 * N / F

or

F = 50e6 * N / P

where F is the tach channel input frequency in Hertz and N is the programmed channel divisor, if any.

So, with no divisor and a 3600 RPM (60 Hz) input,

P = 50e6 / 60 = 833,333

which would appear as hex values 0x000C and 0xB735 in PxHI and PxLO respectively.

6. Setup and Installation

6.1 Safety and Handling Precautions

The V365 module includes static-sensitive components; please observe antistatic procedures when handling the module outside of its antistatic packaging or outside of the VME cardcage.

CAUTION: Do not insert or remove the module from a crate with crate power on. Do not power up the crate unless front-panel mounting screws are secure.

Certain transducers and frequency-signal sources may produce dangerous voltage and energy-level signals. To ensure safety, always observe the following precautions:

CAUTION: Connect only known human-safe and energy-limited signals to the V365.

CAUTION: Route all module wiring as low-voltage signals in conformance with appropriate electrical codes.

CAUTION: Never apply more than 150 volts RMS to any tach channel input, either across a differential input or from any input to ground.

CAUTION: Do not connect signal (VME) ground or the 12-volt excitation signal to any possible external potential sources.

CAUTION: If explosion hazards are possible, connect V365 signals to field wiring through appropriate intrinsic safety barrier devices.

The V365 module is a commercial product which has finite failure rates associated with its hardware, firmware, and documentation. Do not apply the V365 in data acquisition or control systems where a failure or defect in the module may result in injury, loss of life, or property damage.

6.2 Switch Setups

6.2.1 A16/A24 Addressing Mode Switch

One DIPswitch position is labeled A16=/=A24. Press the appropriate side of the switch to permit operation in VME systems which use “A16” (16-bit) or “A24” (24-bit) addressing.

In A16 mode, the module responds to VME address modifiers 0x29 and 0x2D. In A24 mode, address modifiers are 0x39 and 0x3D.

6.2.2 VMEbus Address Switches

The module VME base address is set by on-board DIPswitches. The switches are labeled A06 through A23. To set an address bit true, press the side of the switch nearest the “Axx” legend. If the module is in A16 mode, only switch positions A06 through A15 are decoded.

The as-shipped module base address is 0xC000 in the A16 space. The A24/A16 switch is in its A16 position, and the A15 and A14 address switches are ON, with all others OFF. This configuration is pictured below.

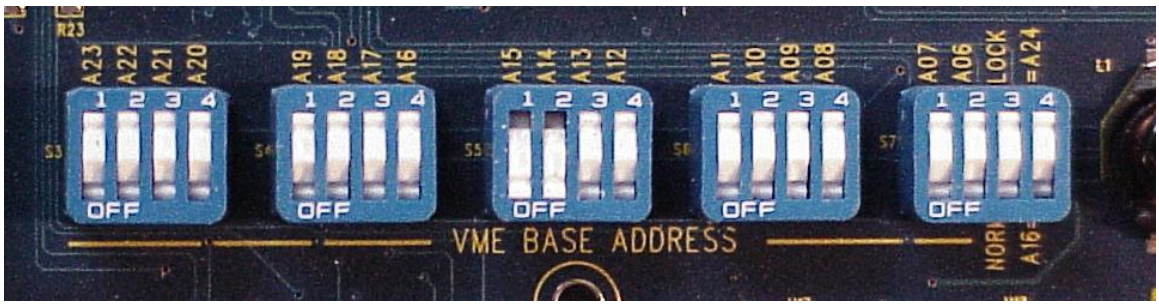


Figure 3. VMEbus Address Switch Configuration: A16 mode, 0xC000.

6.2.3 Lock Mode Switch

The V365 does not support the V360 LOCK mode.

6.3 Installation in a VME Crate

The V365 may be installed in any standard 6U VME backplane. The module connects to the backplane J1 connector only. Seat the module firmly and secure both front-panel mounting screws before applying power.

The module uses the standard VME power supplies:

+5 volts at 700 mA max

+12 volts at 250 mA max

-12 volts at 200 mA max

If external transducer excitation is provided by the V365, the +12 volt current drain will increase, up to the 0.5 amp current limit.

6.4 Installation Verification

Once the module is installed and secured, crate power may be applied. At powerup time the following LED sequence should be observed:

Green LED on; indicates ROM checksum OK,

1 second delay,

blue and green LEDs on; indicates VME FPGA programmed,

1 second delay,

green and blue off; indicates TIMER FPGA programmed,

green now blinks once per second, and blue flashes on VME access.

The TEST switch may now be used to select a channel for test access, or to indicate channel trigger activity via the eight yellow LEDs.

Users may now access the module via the VMEbus. It is recommended that the module MFR ID and MODULE TYPE registers be read and verified correct, ensuring that there are no gross VME access or conflict problems.

6.5 Using the Signal Monitor Features

The front panel of the module is furnished with a test switch, two SMB connectors, and eight channel-monitor LEDs. The switch functions are discussed in Sections 4.3 and 4.4.

During system checkout, it is often convenient to use the test provisions to adjust input signal conditioning and trigger level options. The procedure is:

Setup such as to be able to program channel configurations, either through a VME setup program or by running V365.EXE on a laptop PC connected to the module serial port.

Connect a dual-channel oscilloscope to the ANALOG and DIGITAL front-panel test connectors.

Apply an actual or simulated transducer signal to the channel under test.

Set the TEST toggle switch to its center position, and move it to the right STEP position as required, until the correct channel-select LED is lit.

Adjust channel configuration until both the displayed analog and digital signals are clean and uniform over the range of expected signal levels and frequencies.

6.6 Powerup Defaults

At powerup time or following a module reset command, the V365 self-configures as follows:

All eight tachometer channels are configured as...

Input attenuator	OFF
Filter	100 KHz
Hysteresys	LOW
Mode	0 = rundown
Test Mode	OFF
Trigger Level	+1.25 volts
Divisor	1

All parameters of all four overspeed blocks are zeroed. This results in all four overspeed relays coils being de-energized, so contacts will be positioned as shown in Figure 3.

The TDIV test signal divisor is set to zero, disabling the test generator.

The OFOR overspeed force register is cleared.

The default module and channel names are installed.

7. Overspeed Subsystem

The V365 module provides a four-channel over/underspeed sensing system that operates independently of the normal "V360 mode" tachometer functions.

Figure 4 depicts the overspeed functionality. There are four logical overspeed blocks, called A, B, C, and D. Each consists of...

A 32-bit-wide data multiplexer that selects the period data from any desired tachometer channel 0...7.

Two user-programmable comparators, one that senses overspeed (ie, tach period less than programmed overspeed target) and one that senses underspeed (period greater than underspeed target.)

Two latches that remember momentary overspeed or underspeed conditions.

An OR gate with selection logic, allowing any of the four signals AOL...AUS to be enabled to de-energize the KA relay coil. AOS and AUS are logic levels that indicate static over/underspeed states, and AOL and AUL represent their latched states.

A SPDT output relay. In Figure 4, relays are shown in the de-energized state, which is by default the "error" or "fault" condition.

The failsafe timer provides the power needed to operate the relay coils. It is refreshed regularly by the microprocessor and, should the uP code cease to execute properly, will drop the coil power and de-energize all relays.

Additional provisions are made for reversing the relay coil drive logic, for resetting the latches of any channel, and for monitoring the sixteen diagnostic logic levels from the VME bus. Users may also force the on/off states of any of the relays.

Module commands are provided to set up each of the four available overspeed boxes.

Tach channels are updated every 1.024 millisecond, and reflect fresh speed data if any new tach signal edges have occurred since the last update. Over/underspeed checks are done simultaneously, driving relay coils accordingly. Relay electrical response time is under one millisecond.

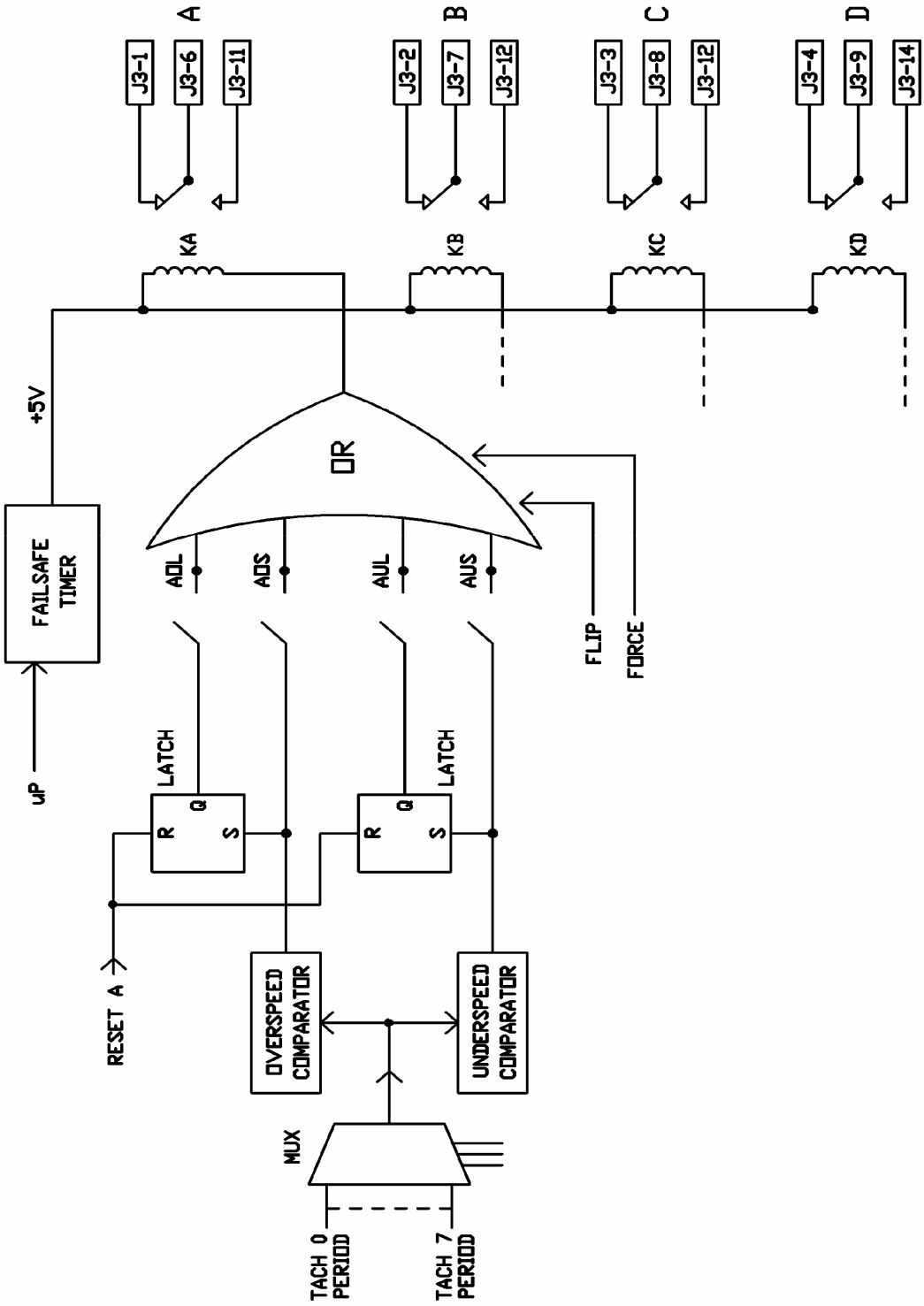


Figure 4. Simplified Overspeed Block Logic

The overspeed logic is summarized as follows:

There are four independent overspeed blocks, A, B, C, and D.

Each block has a SPDT relay output, with contacts brought out to three pins of the front-panel HD15 connector.

Each overspeed block can be assigned to monitor any one of the eight tachometer inputs, tach channels 0...7. Tach channels are unaffected by overspeed programming.

The default state of any relay is ON, coil energized.

A relay will be de-energized if…

The module is powered down.

The V365 firmware fails to refresh either of two internal watchdog timers.

The overspeed block is unprogrammed, namely if all four of its enable bits OS OL US and UL are clear.

The overspeed channel has any of its four flag bits asserted in its associated nibble of the OSTAT register.

The relay would be energized, but its functionality is reversed by the FLIP bit in the overspeed channel control word.

The relay state is overridden by the OFOR relay force register.

Each overspeed block has four enable bits in its control register and four corresponding flag bits in a nibble of the global OSTAT status register. The bits for each block are...

OS overspeed static
OL overspeed latched
US underspeed static
UL underspeed latched.

A flag bit in OSTAT can be true only if it is enabled by its corresponding bit in the channel control word, as established by an overspeed block configuration command.

The static overspeed flag bit OS will go true if enabled by the channel control word and if the selected tach input is overspeed, namely the signal period is less than the programmed overspeed period limit. Similarly, static underspeed flag US will go true if enabled and the period is longer than the underspeed limit.

OL is the latched version of OS, and UL is the latched version of US. Each latched bit is set if enabled and if the corresponding static condition appears, even momentarily. It is not necessary to enable the static bits OS or US in the block control word in order for the latched bits OL and UL to be operative.

The latched overspeed and underspeed bits OL and UL are cleared by the OVERSPEED RESET command or by disabling them in the overspeed block control word.

It is strongly recommended that…

Relays be used in their failsafe mode, namely that de-energizing a relay causes an external overspeed trip.

Multiple overspeed channels be used with redundant overspeed sensors to protect valuable machinery. Relay contacts may be wired in series, or may provide independent trips to external controllers.

Underspeed trips be used to detect failed tachometer signals.

Overspeed trips be tested regularly. Care must be taken to ensure that tach channels are not accidentally left in self-test mode.

Note: On powerup or following a reset command, all overspeed control blocks will be cleared, so all four relay coils will be de-energized.

7.1 OSTAT: Overspeed Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUL	DUS	DOL	DOS	CUL	CUS	COL	COS	BUL	BUS	BOL	BOS	AUL	AUS	AOL	AOS

This read-only register conveys the status flags of all four overspeed blocks. Bits are...

```
 0   AOS   channel A  static  overspeed flag
 1   AOL   channel A  latched overspeed flag
 2   AUS   channel A  static  underspeed flag
 3   AUL   channel A  latched underspeed flag

 4   BOS   channel B  static  overspeed flag
 5   BOL   channel B  latched overspeed flag
 6   BUS   channel B  static  underspeed flag
 7   BUL   channel B  latched underspeed flag

 8   COS   channel C  static  overspeed flag
 9   COL   channel C  latched overspeed flag
10   CUS   channel C  static  underspeed flag
11   CUL   channel C  latched underspeed flag

12   DOS   channel D  static  overspeed flag
13   DOL   channel D  latched overspeed flag
14   DUS   channel D  static  underspeed flag
15   DUL   channel D  latched underspeed flag
```

7.2 OFOR: Overspeed Force Register

The read/write OFOR VME register allows users to take control of any of the four overspeed relays.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								DOF	COF	BOF	AOF	DON	CON	BON	AON

If users set the AON bit, the overspeed A relay coil will be forced on; J3 pins 6 and 11 will be connected. Setting AOF forces the coil off, connecting J3 pins 6 and 1. If both bits are set, the OFF condition dominates. Similarly, bits are provided to control the B, C, and D block relays. These bits unconditionally override the normal speed-based relay control logic.

OFOR may be written directly from the VME bus, or it may be loaded using the 0x41 module command, as noted in Section 7.3.4.

7.3 Overspeed Block Setup Commands

Each of the four logical overspeed blocks is set up with a module command, using the general command protocol outlined in Section 5.8.

Command Code Hex	**Function**
0x30	read overspeed A controls
0x31	write overspeed A controls
0x32	read overspeed B controls
0x33	write overspeed B controls
0x34	read overspeed C controls
0x35	write overspeed C controls
0x36	read overspeed D controls
0x37	write overspeed D controls
0x38	reset overspeed latches
0x39	setup overspeed interrupts
0x40	make interrupt
0x41	write OFOR register

7.3.1 Write Overspeed Controls Commands

The principal overspeed command is WRITE OVERSPEED CONTROLS, with one hex command code assigned to each of the four overspeed blocks A, B, C, and D. To use this command, load all five parameter words and then write the appropriate command (0x31, 0x33, 0x35, or 0x37) to the CMD register. All five command parameters are defined for this command.

PARM1 is the control word for this overspeed block.

PARM2 and PARM3 are the 32-bit overspeed period.

PARM4 and PARM5 are the 32-bit underspeed period.

The PARM1 command word is arranged...

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLIP								UL	US	OL	OS		CH2	CH1	CH0

The CH2...CH0 bits select the tach channel that this overspeed block will monitor, with tach channels 0...7 encoded in the three bits.

If OS is set, the block's associated overspeed relay will be de-energized by a static overspeed, for only so long as the overspeed condition persists.

If OL is set, the relay will be de-energized by the latched overspeed condition.

If US is set, the overspeed relay will be de-energized by a static underspeed, for only so long as the underspeed condition persists.

If UL is set, the relay will be de-energized by the latched underspeed condition.

Each of these bits enables the corresponding flag in the OSTAT register.

Note: If multiple conditions are enabled, any block flag will drop the relay coil current. The relay coil power is also dropped if VME crate power is lost or if the relay failsafe timer times out, so this is the preferred failsafe operating mode.

If none of the four condition-enable bits is set, overspeed checks for this channel will be skipped and the channel relay coil will be kept de-energized.

If FLIP is set, relay coil logic is reversed, and a "safe" condition results in no coil current, whereas any fault will energize the relay coil. This is NOT the preferred failsafe operating mode. The FLIP bit is functional even if no over/under enable

bits are set.

The PARM2:PARM3 register pair specifies the overspeed trip point, scaled identically to the PxHI:PxLO period register format, as described in Section 5.10. If overspeed trip is not enabled, these parameters are irrelevant.

The PARM4:PARM5 register pair specifies the underspeed trip point. If underspeed trip is not enabled, these may be ignored.

7.3.2 Read Overspeed Controls Commands

These commands (0x30, 0x32, 0x34, and 0x36) read back the current settings of the four overspeed blocks. After the command has been executed, the five parameter words will be presented in the format described above.

7.3.3 Reset Overspeed Latches Command

Each overspeed block has overspeed and underspeed latches which remember transient over/under conditions. The RESET LATCHES command allows users to clear these conditions once the machine has reached normal operating speeds.

The PARM1 register specifies which of the eight latches is to be reset:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												RD	RC	RB	RA

If any "R" bit is set in PARM1, this command will clear both "latch" bits in the corresponding overspeed block. If an actual overspeed or underspeed condition still exists when this command attempts to reset latch bits, the latch bit will be immediately re-asserted.

So, writing 0x000F to PARM1, then writing 0x38 to the CMD register will initiate a command which resets all eight over/underspeed latches. If the overspeed/ underspeed functions are used in static (unlatched) mode, this command may be ignored.

7.3.4 Write OFOR Register Command

This command provides an alternate means to write the OFOR overspeed relay force register. Write the desired register contents to PARM1 and then load command code 0x41 into the module CMD register.

7.4 Overspeed Interrupt Setup

A VME interrupt can be caused by the appearance (rising edge) of any of the bits of the OSTAT overspeed status register, as selected by a mask parameter.

The interrupt acts in VME ROAK mode, meaning that the interrupt request on the VME bus is dropped as soon as a successful VME vector operation takes place. Users should be aware that selecting a static overspeed or underspeed bit as an interrupt source can cause a rapid burst of interrupts if a tachometer channel input stays close to an overspeed or underspeed threshold. So it is usually preferable to generate interrupts from latched bits in OSTAT, or to disable interrupts within the interrupt service routine once an exception condition is noted.

To enable interrupts,

Load macro parameter PARM1 with the desired VMEbus interrupt priority level, integer values 1 through 7, with the ENAB bit set to enable interrupts. For example, write 0x9 to this parameter to enable interrupts at priority level 1.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												ENAB	LVL2	LVL1	LVL0

Load parameter register PARM2 with the desired interrupt vector, 0...255. The physical address of the vector in user memory depends on how the system CPU maps VME vectors into the CPU address space.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								V7	V6	V5	V4	V3	V2	V1	V0

Load PARM3 with a bit mask. This mask selects which bits of OSTAT will cause an interrupt on their rising edge.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DUL	DUS	DOL	DOS	CUL	CUS	COL	COS	BUL	BUS	BOL	BOS	AUL	AUS	AOL	AOS

Load the CMD register with macro command code 0x39.

This command must follow the protocol described in Section 5.8.

To disable interrupts, load zero into PARM1 and then execute the 0x39 command.

7.5 Force Interrupt Command

Once interrupts are set up, as described in Section 7.4, a VME interrupt can be forced by executing the 0x40 module command. It is not necessary to enable any OSTAT bit edges in the PARM3 mask of the 0x39 interrupt setup command. One interrupt cycle will be generated immediately after the 0x40 command is executed. No command parameters are required. This command is provided to test user interrupt handlers.

7.6 An Overspeed Programming Example

Suppose we have a turbogenerator which runs at a nominal 3600 RPM. We'll use a variable-reluctance pickup on the main shaft, near a gear with 36 teeth. We will program tach channel 3 to measure this input, and program its divisor to 36 to in effect cancel the frequency increase of the gear teeth.

Assume that we define overspeed to be 3800 RPM and underspeed to be 3000. We then have...

STATE	RPMs	Hertz	PERIOD	HEXHI	HEXLO
Normal	3600	60.0	833,333	0x000C	0xB735
Over	3800	63.3	789,473	0x000C	0x0BE1
Under	3000	50.0	1,000,000	0x000F	0x4240

where "period" equals 50e6/Hertz, and HEXHI:HEXLO is the 32-bit expression of the Period integer.

To allow machine startup, we write 0x0001, the "AON" bit, to the OFOR register; this forces the overspeed "A" relay to be energized, defeating the over/under trips.

Next, we'll load the five command parameters as...

PARAM1	0x0053	use tach channel 3, overspeed static, underspeed static
PARAM2	0x000C	MS part of overspeed period
PARAM3	0x0BE1	LS
PARAM4	0x000F	MS part of underspeed period
PARAM5	0x4240	LS

then write the command code 0x31 to the module CMD register, setting these parameters into the overspeed A block. After the command is executed, it is prudent to clear all the parameter registers and then read back these settings to ensure they are properly loaded.

After overspeed block A is configured, we can start the turbine under manual control, ramping it up to close to normal speed. Once it's in range, we can clear the OFOR register, allowing the block A relay to perform its over/under trip function.

If the machine needs overspeed trip only, we could enable the overspeed feature only, and then wouldn't have to override the relay in order to bring the machine up to speed. If we elected to use latched, rather than static trips, we would have to issue a latch reset command (see 7.3.3) after the machine was up to speed but before we free the overspeed block A relay to operate normally.

Note: Underspeed trip can be valuable for tripping on speed sensor failure as well as true underspeed conditions.

Overspeed block configurations can be changed at any time, even while the machine is running.

Reminder: All command operations must follow the handshake requirements described in Section 5.8.

8. Test Software and Measurement Examples

The V365.EXE program is provided with the V365 module. It will run on a PC under DOS Version 6 or later, or in a Windows DOS box. It can use a number of PC-to-VME interfaces to configure and monitor the V365 module.

V365.EXE also communicates serially to the V365. Connection to a typical laptop PC requires an RS-232 adapter cable, Highland Part Number 28A565 or equivalent. One such cable is furnished with the V365.

Functions supported include:

Display of all module registers, including periods, frequency, and equivalent RPM or other engineering units.

Plotting of frequency/RPM versus real time.

Channel configuration. The program may be used to configure the module in situations where it is undesirable to use the VME host computer to do so. The V365.EXE program will also compute channel configuration register hex values “offline” so that a host system can load these literal values into config registers with a minimum of programming.

The RS-232 display operations may be performed concurrently with normal VME operation. This allows operation to be monitored and allows field-service staff to set up and verify sensor wiring offline, without having to write or run special VME-system programs.

The following figures are typical plots produced by the V365.EXE program.

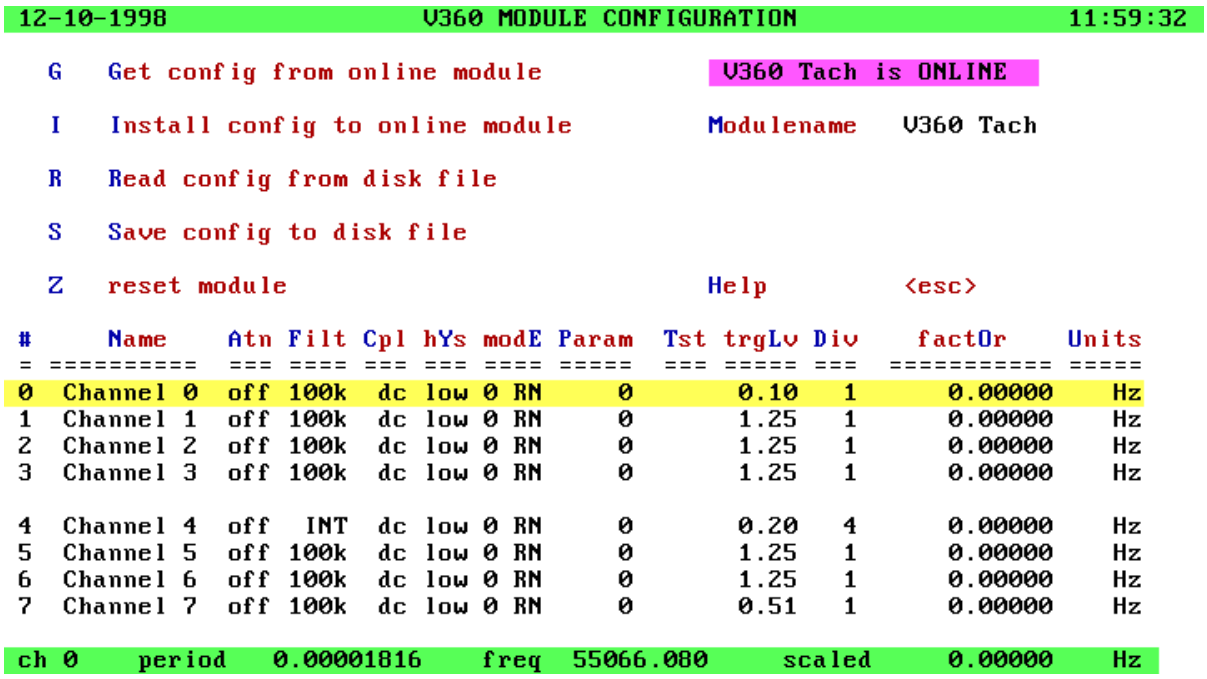


Figure 5. Module Configuration Screen of the V365 Test Program

The V365.EXE test program, which is supplied with the unit, may be run on a laptop PC connected to the V365 RS-232 port, and may be used to configure the module and display/plot channel data.

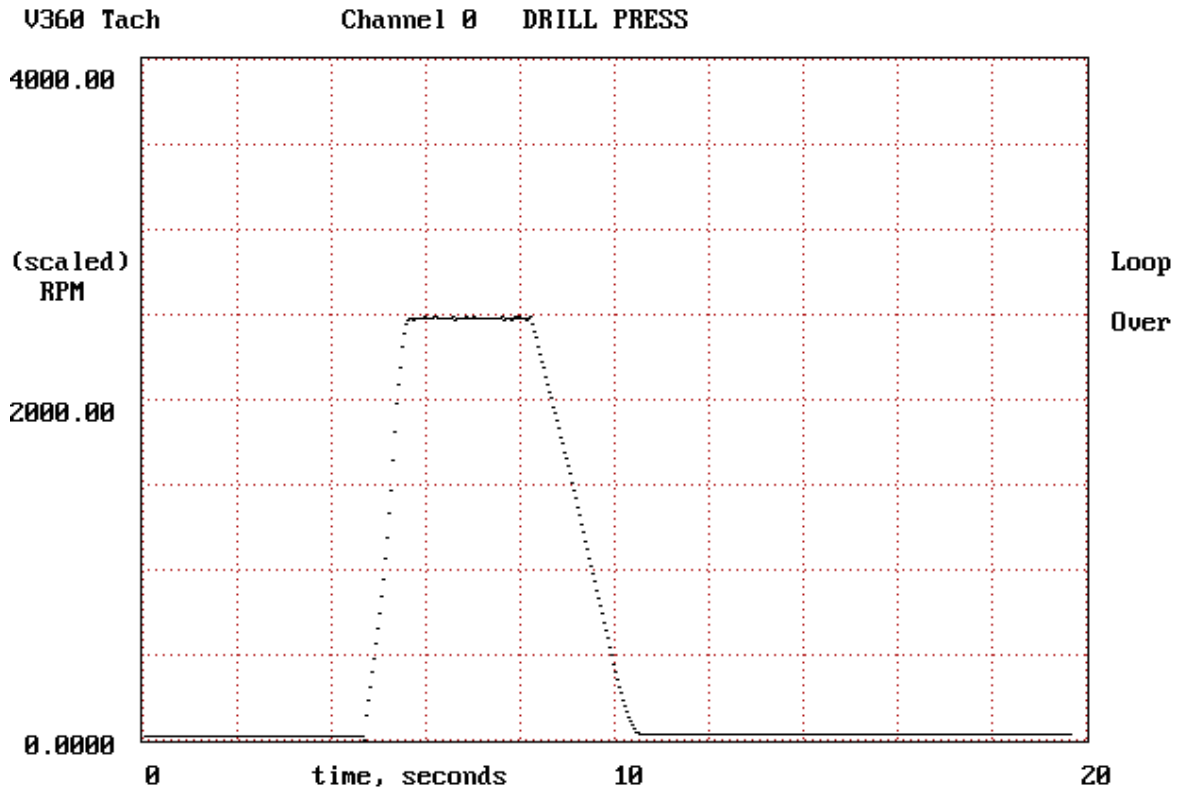


Figure 6. Acceleration-Deceleration Curve of a Drill Press

To measure the acceleration-deceleration curve of a drill press, a magnetic speed sensor was wired to the V365 through 120 feet of unshielded twisted-pair wire run outdoors, on the ground, between buildings.

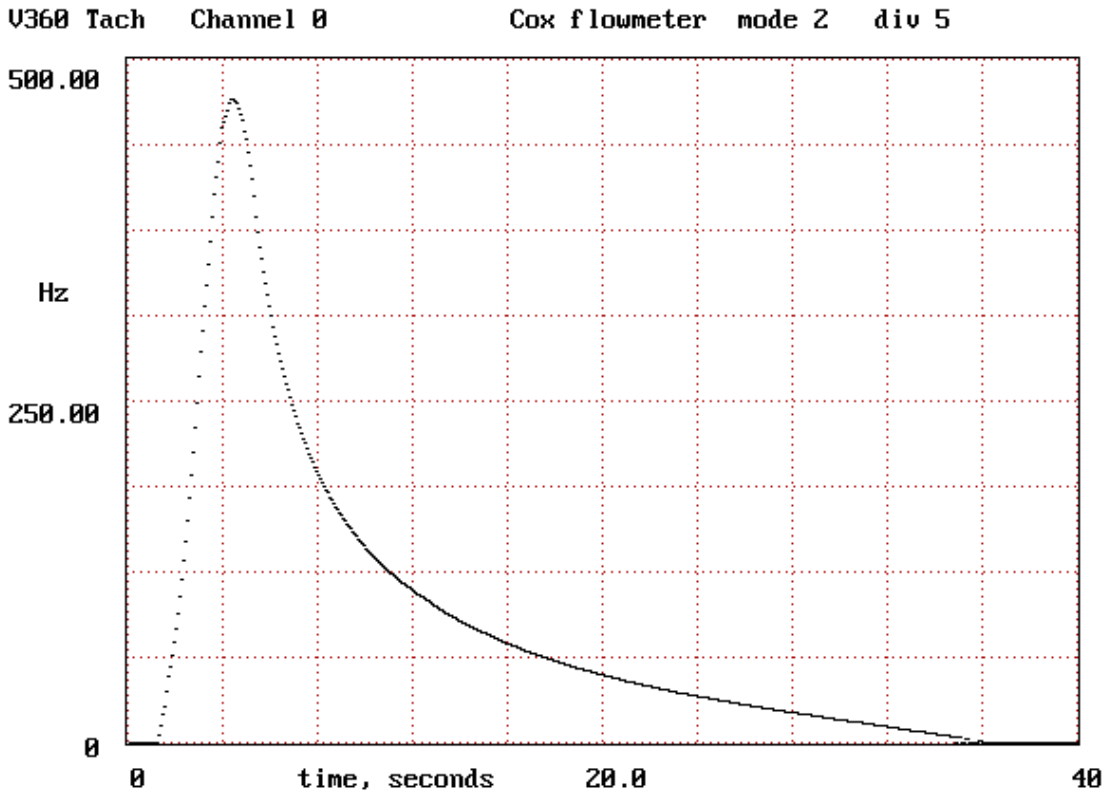


Figure 7. V365 Frequency-Time Plot of Cox Turbine-Type Aircraft Fuel Flow Transducer

A Cox aircraft fuel flow transducer was tested with a compressed air jet.

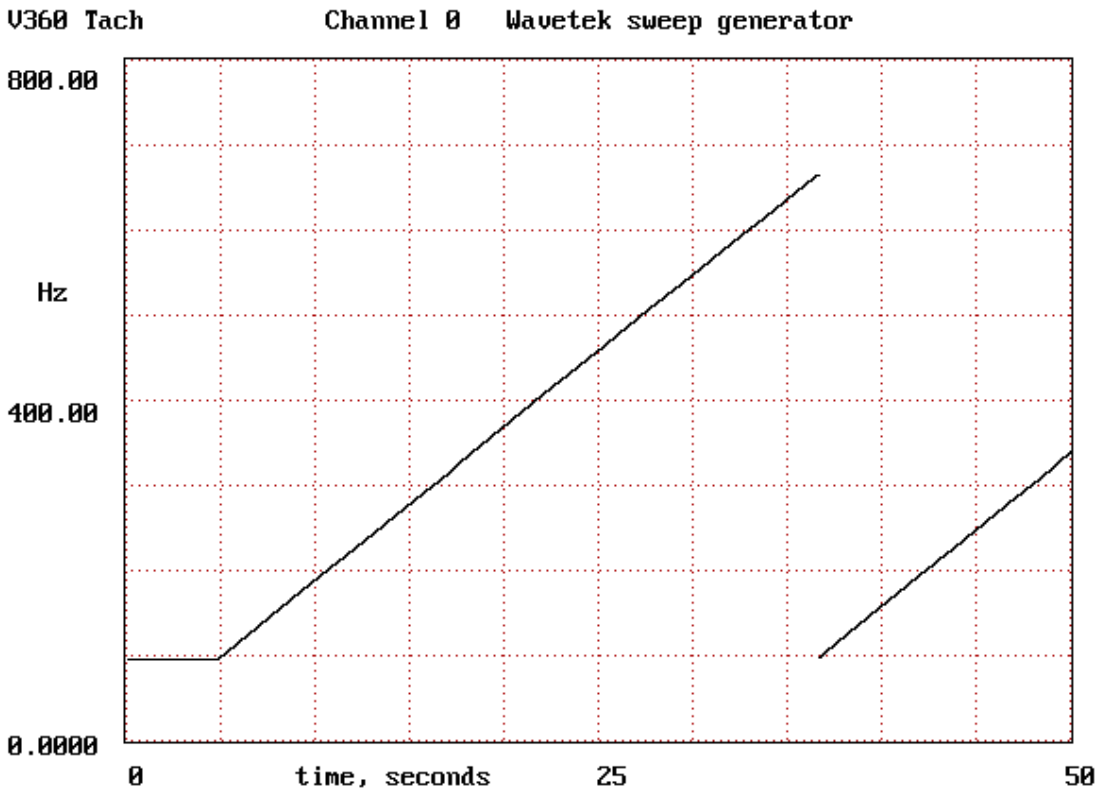


Figure 8. V365 Frequency-Time Plot With Wavetek Sweep Generator as the Signal Source

9. Versions and Firmware

A single plugin ROM chip contains module firmware and the configuration files for the two on-board Xilinx FPGA chips. ROMs may be upgraded in the field, and are identified by a label on the chip as well as by the contents of the ROMID and ROMREV registers.

The standard version of the V365 module is Highland Model V365-1B.

The beta firmware release was 22368-A. All field units have been upgraded to 22368-B.

Firmware version 22368-B was released in early April, 2006. Changes included:

A bug was fixed in the dual-port memory self-test routine.

Eight TEST flag bits were added to the ROMREV register.

The module command register is now initialized to DONE at powerup.

A Prescale bit was added to the test frequency divisor, extending the range of self-test frequencies below 10 Hz.

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