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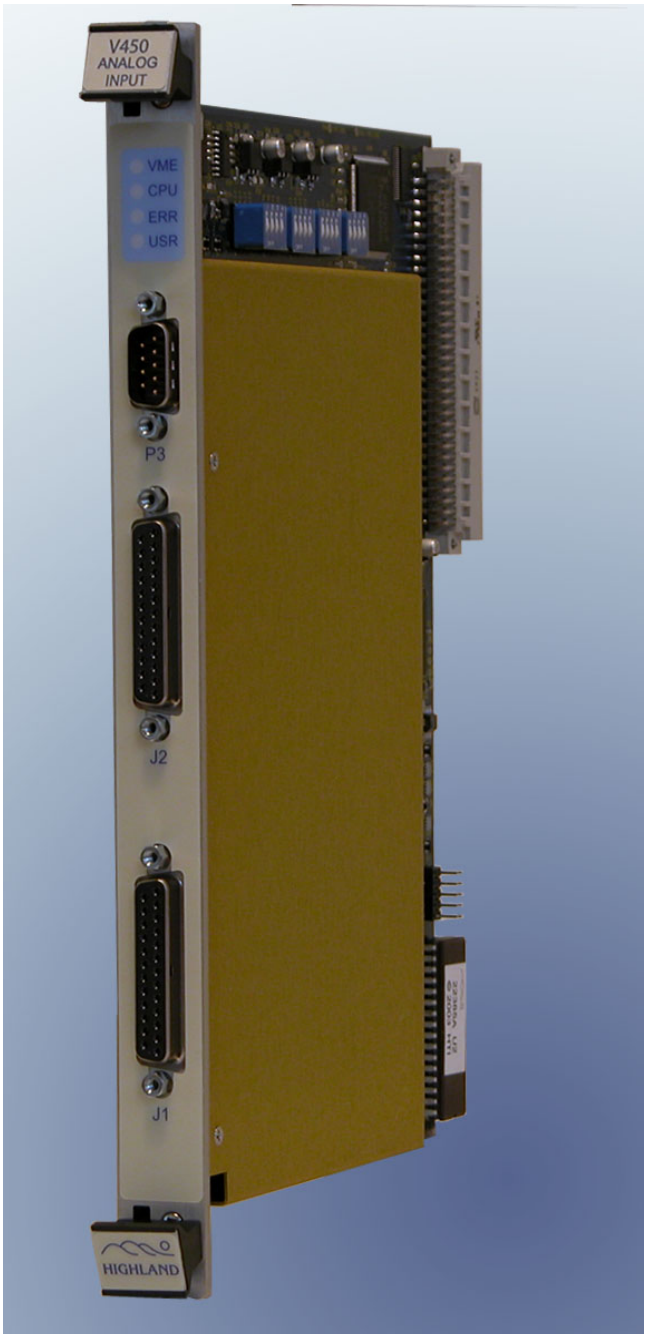
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V450 ANALOG INPUT MODULE

Technical Manual

March 19, 2015

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1 Introduction

This is the technical manual for the Highland Model V450 revision E.

The V450 is a VME 16-channel isolated analog-to-digital converter module which can acquire a wide range of DC voltages, including thermocouple temperatures.

The standard version is Highland Model V450-1. The version of the module with the optional built-in self-test (BIST) facility is the V450-2.

Features of the V450 include:

- 16 channels of fully isolated analog input acquisition. Each channel is independently programmable for mode and input range.
- Voltage mode: input ranges from ± 25 mV to ± 250 volts with 24-bit resolution.
- Thermocouple mode: reports temperature for types J K E T R S B N with $^{1}/_{16}$°C resolution.
- Four precision RTD signal conditioners for reference junction temperature sensing, plus one on-board reference junction sensor. Any thermocouple input channel can be associated with any reference.
- Reports thermocouple loop resistance and detects open thermocouples without inducing offset errors.
- No realtime handshaking is required. Once channel parameters are set up, measurements appear in dual-port memory registers with VMEbus-speed access.
- Separate test connector supports in-crate calibration check.
- Programmable digital filtering and optional plug-in analog anti-aliasing filters.
- Optional built-in self-test (BIST).
- Supports one or two optional 8-channel J470 isothermal junction boxes, each with integral RTD reference junction sensor, or one or two J475 field-wiring interface boards.

2 Specifications: V450 Analog Input Module

2.1 Electrical Characteristics

FUNCTION	16-CHANNEL ISOLATED VOLTAGE/THERMOCOUPLE INPUT
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16 Implements 256 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
CHANNELS	16, programmable functions, galvanically isolated
RANGES	Programmable per channel Voltage: 14 bipolar ranges, ±25 mV, 50 mV, 80 mV, 125 mV, 250 mV, 500 mV, 1.25 V, 2.5 V, 5 V, 12.5 V, 25 V, 50 V, 125 V, 250 V Thermocouples: Types J K E T R S B N
RESOLUTION	Voltage mode, 24 bits Temperature mode, 0.0625°C
SAMPLE RATE	Programmable per channel, 4 to 500 readings/second Default rate of 16/second rejects 50/60 Hz noise
OFFSET ERROR (0-60°C)	Range > 20V ± 10 ppm range ± 250 µV 1V < Range < 20V ± 10 ppm range ± 20 µV Range < 1V ± 10 ppm range ± 2 µV
OFFSET ERROR (-40-80°C)	Range > 20V ± 15 ppm range ± 1000 µV 1V < Range < 20V ± 15 ppm range ± 50 µV Range < 1V ± 15 ppm range ± 5 µV
GAIN ERROR	(15-35°C) ± 300 ppm of measurement ± 30 ppm/°C outside this range
INPUT IMPEDANCE	Range < 1V: 100 MΩ min Range > 1V: 1 MΩ min
PROTECTION	±350 volts differential ±750 volts common-mode ESD to 15 KV, human body model
NOISE REJECTION	> 80 dB rejection of 50/60 Hz noise at default sample rate of 16.7/second
RTD INPUTS	Four non-isolated external reference junction inputs for 4-wire platinum RTD sensor, 100 Ω or 1 kΩ, ISO "385" curve Protected against shorts, ESD

ONBOARD SENSOR	Semiconductor reference junction temperature sensor, ±2°C typical accuracy
OPERATING TEMPERATURE	0 to 60°C; extended -40 to 80°C MIL/COTS range available
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies: +5 V, 1.0 A max +12 V, 5 mA max -12 V, 5 mA max
CONNECTORS	2 D25 female for channels and RTDs D9 male for test
INDICATORS	LEDs indicate VME access, CPU activity, error conditions Additional user programmable LED
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes Thermocouple tables based on NIST/ITS-90 RTD tables per IEC-751 for "385" curve RTDs

2.2 Typical Performance

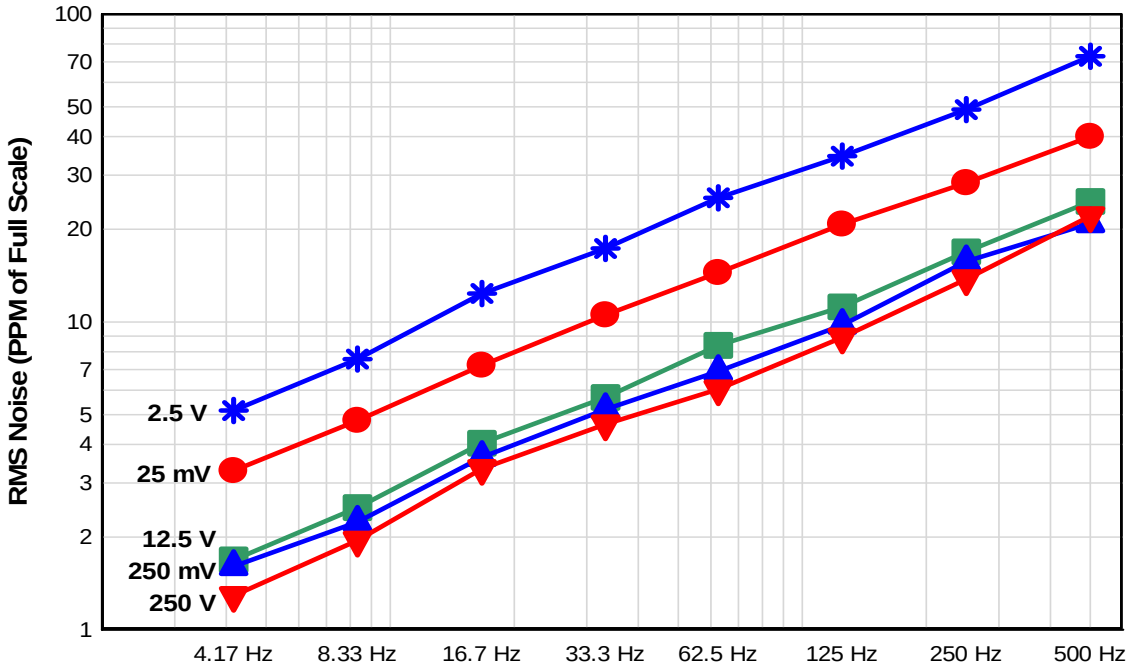


Figure 1. Typical RMS Noise v. Sampling Rate

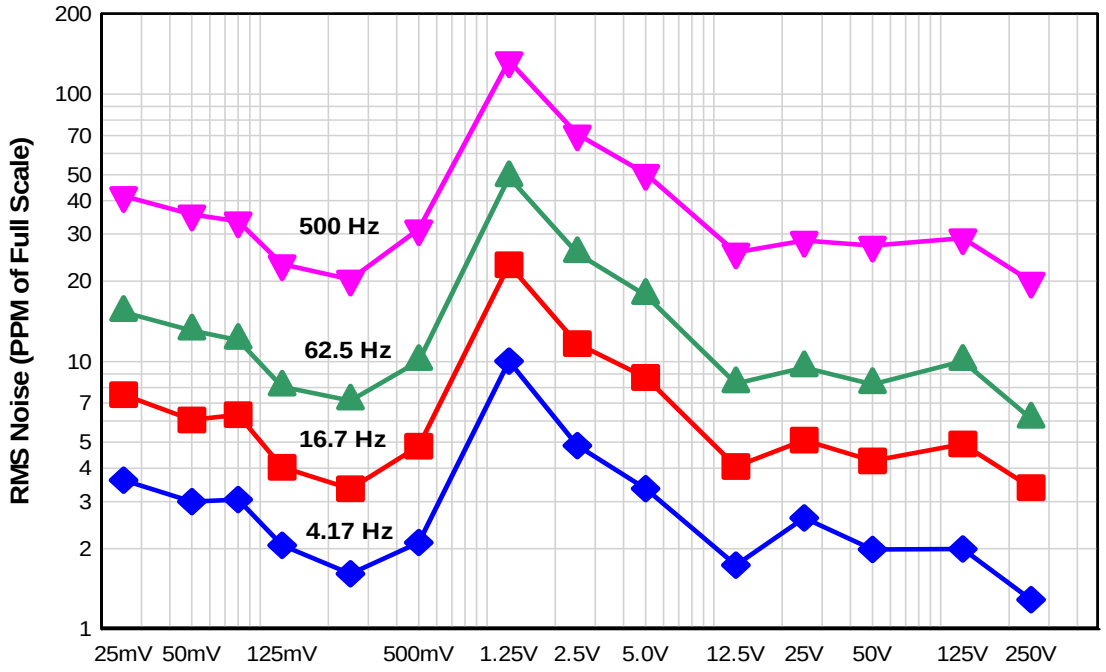


Figure 2. Typical RMS Noise v. Full Scale Range

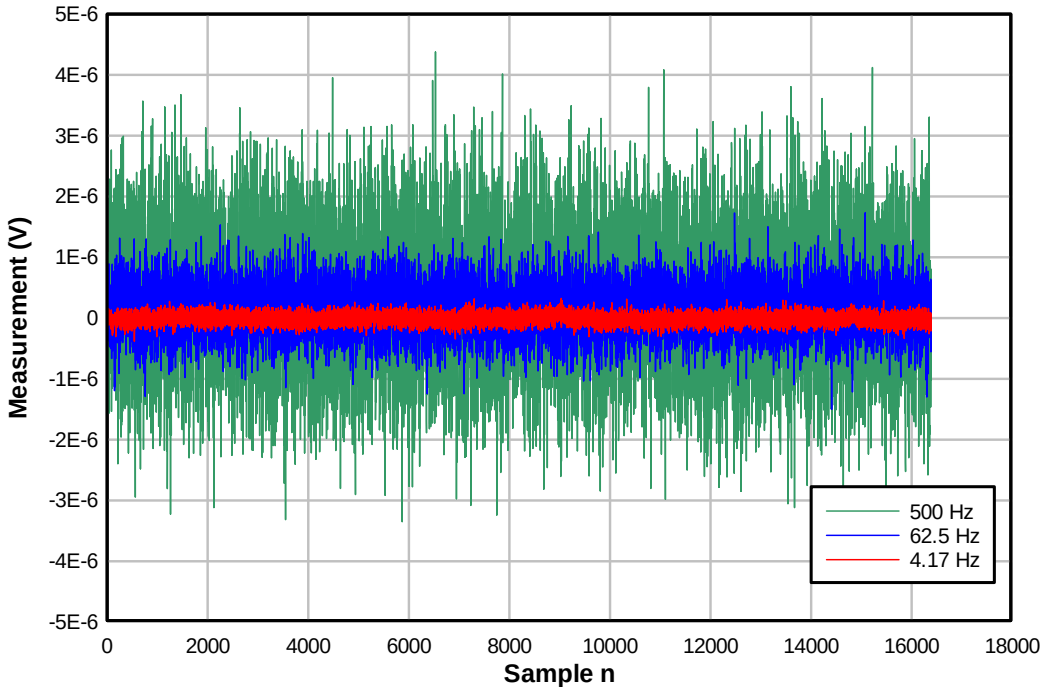


Figure 3. Typical Channel Noise (25 mV Range)

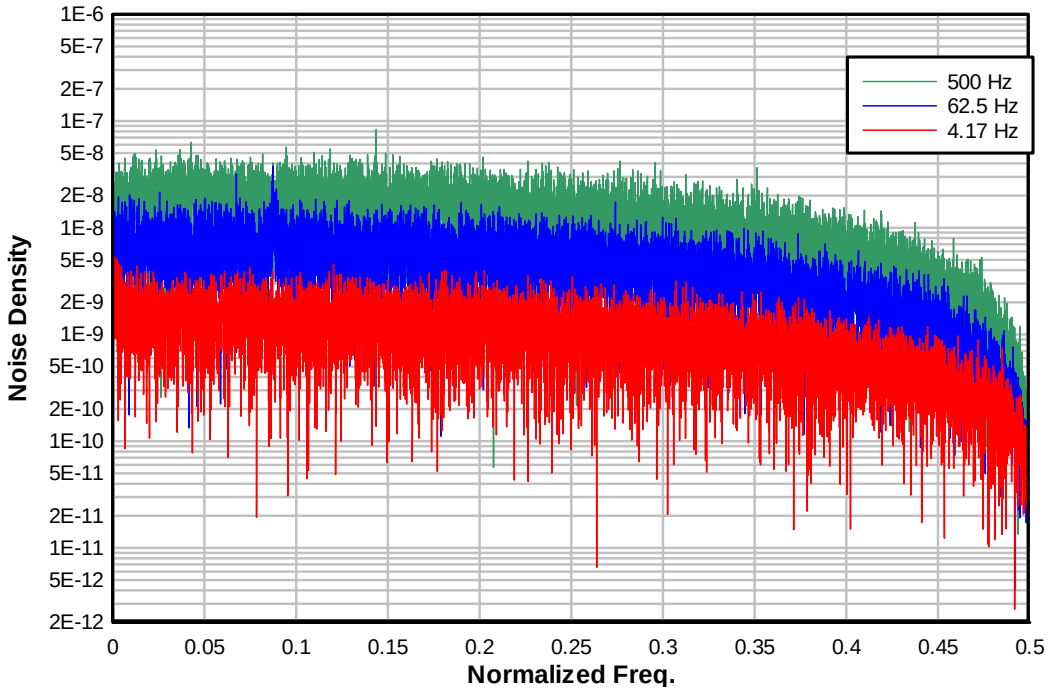


Figure 4. Typical Channel Noise Spectrum (25 mV Range)

3 Overview

The V450 includes 16 independent, isolated channels. Each channel has an isolated DC power supply, A/D converter, signal conditioning, open thermocouple detection, and overvoltage protection circuits.

An internal microprocessor manages all data I/O and communicates with the VMEbus via a transparent, VMEbus-speed dual-port memory.

Each channel may be user programmed to operate in voltage-input or thermocouple acquisition mode, as listed in the specifications section above. In each mode, channel operating parameters, acquired measurements, and status flags are accessible in dedicated VME registers. Data rate/filtering options are provided. Data acquisition is managed autonomously by the processor, so VME masters may set channel parameters or read acquired measurements at any time with no handshaking concerns.

The V450 includes lookup tables for common thermocouple types. Reference junction compensation uses 4-wire platinum RTDs located in the external field wiring, and cold-junction compensation is via reverse lookup of thermocouple potential for the type currently selected. Reference junction temperatures are readable. Provision is made for four reference junction RTDs, and any channel may be assigned to use any RTD. One internal semiconductor reference-junction sensor is also provided.

Thermocouple loop resistance may be measured by user command. Subsequent temperature measurements are automatically compensated for loop resistance/burnout current errors without the errors normally associated with open-thermocouple sensing.

Relays are provided to reroute any input channel to the dedicated D9 test connector for calibration checks without disrupting field wiring.

Thermocouple linearization is based on NIST/ITS-90 polynomials. RTD data is per IEC-751 for "385" curve platinum RTDs. Units are calibrated against a Keithley digital voltmeter accurate to 20 PPM and traceable to NIST.

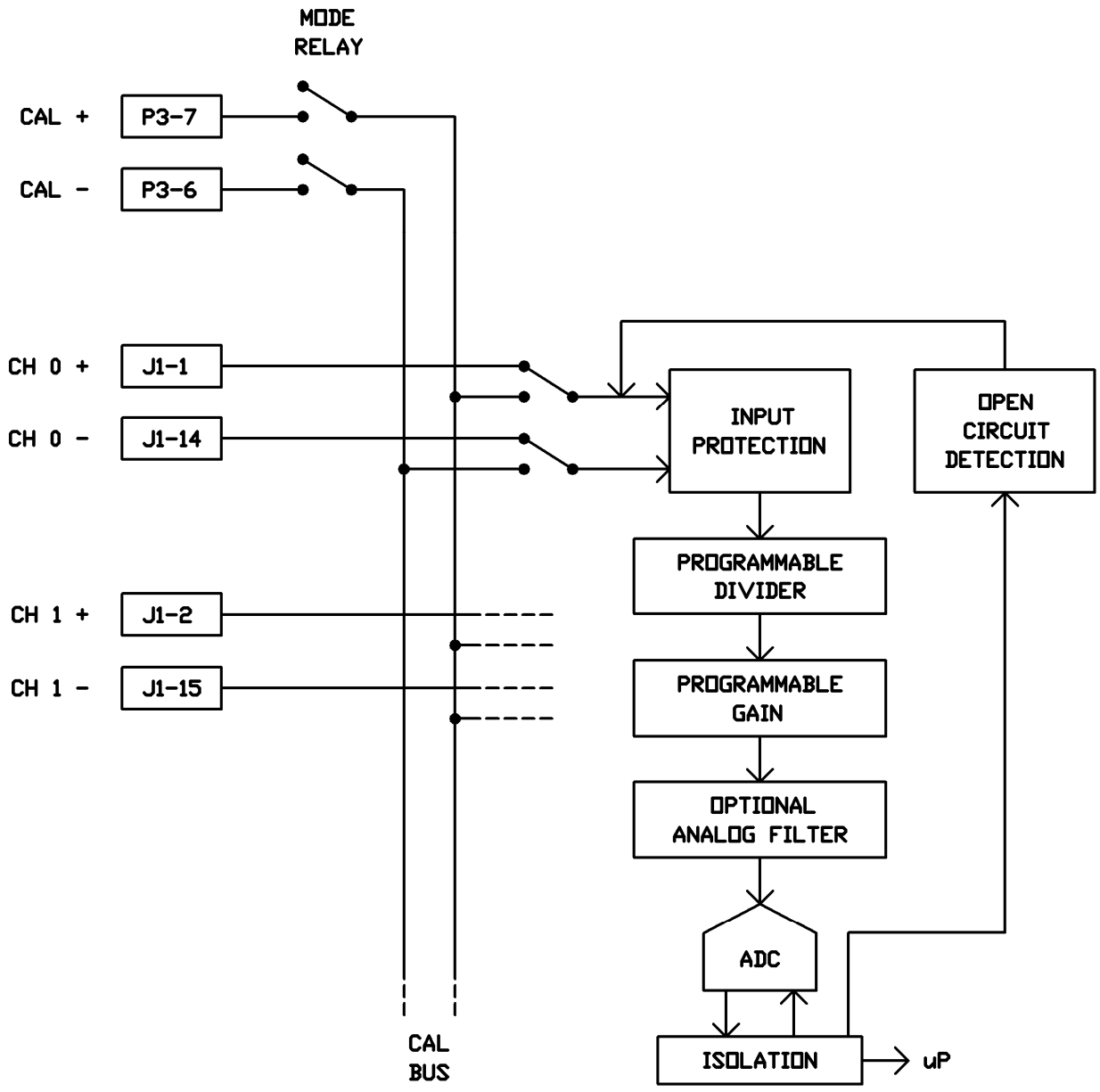


Figure 5. V450 Channel Equivalent Circuit

4 Connectors and Installation

4.1 Address DIP Switches

Four 4-position rocker-type dipswitches are provided near the top edge of the board. They are labeled, left to right, "A23" through "A9" and finally "A24M".

To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its "Axx" lettering. Use a toothpick or paper clip, not a pen or pencil.

The A24M switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A24M switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A9 are active.

Units are shipped with switches A15 and A14 on, all others off, locating the register base at 0xC000 in the A16 space, as shown in the figure below.

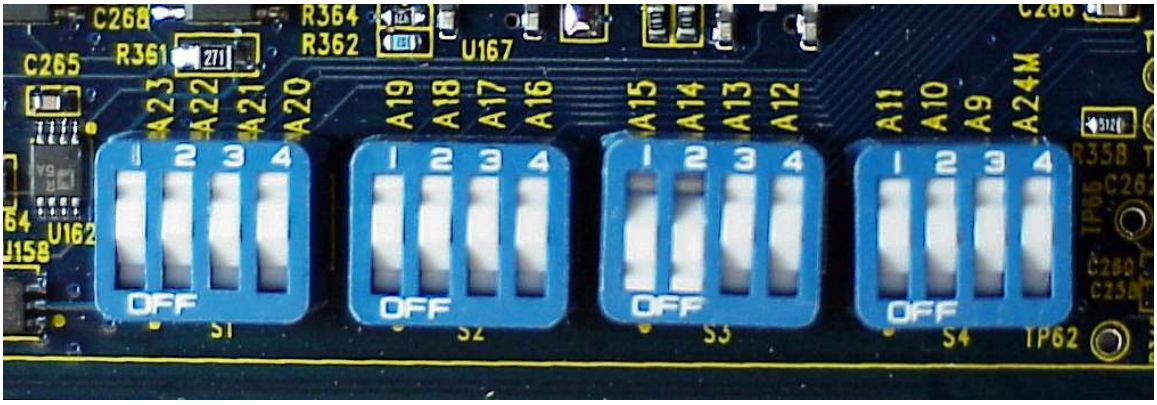


Figure 6. Address DIP Switch Configuration

4.2 Installation

The V450 may be installed in any VME (IEEE 1014) crate, including VME64 variants. It uses only the P1 backplane connector and draws significant current from only the VME +5 volt supply.

The V450 passively passes all interrupt and bus grant signals, so may be used with backplane grant jumpers installed or not installed.



CAUTION: Do not install or remove the V450 with crate power on. VME modules are not hot-pluggable. The V450 will be damaged if hot-plugged.



CAUTION: Fully seat the module and secure front-panel screws before applying power.



CAUTION: Handle the V450 with proper ESD precautions to avoid static damage.

4.3 D25 Input Connectors

Two front-panel female D-25 connectors are provided. Each connector accommodates eight differential inputs and two 4-wire RTD reference junction sensors.

The pinout of the D25 connectors is as follows:

J1 Pin	Function	J2 Pin	Function	Grouping
J1-1	ch 0+	J2-1	ch 8+	
J1-14	ch 0-	J2-14	ch 8-	
J1-2	ch 1+	J2-2	ch 9+	
J1-15	ch 1-	J2-15	ch 9-	
J1-3	ch 2+	J2-3	ch 10+	
J1-16	ch 2-	J2-16	ch 10-	
J1-4	ch 3+	J2-4	ch 11+	
J1-17	ch 3-	J2-17	ch 11-	
J1-5	ch 4+	J2-5	ch 12+	
J1-18	ch 4-	J2-18	ch 12-	
J1-6	ch 5+	J2-6	ch 13+	
J1-19	ch 5-	J2-19	ch 13-	
J1-7	ch 6+	J2-7	ch 14+	
J1-20	ch 6-	J2-20	ch 14-	
J1-8	ch 7+	J2-8	ch 15+	
J1-21	ch 7-	J2-21	ch 15-	
J1-9	RtdA E+	J2-9	RtdC E+	RTD Excitation
J1-22	RtdA E-	J2-22	RtdC E-	
J1-10	RtdA S+	J2-10	RtdC S+	RTD Sense
J1-23	RtdA S-	J2-23	RtdC S-	
J1-11	RtdB E+	J2-11	RtdD E+	RTD Excitation
J1-24	RtdB E-	J2-24	RtdD E-	
J1-12	RtdB S+	J2-12	RtdD S+	RTD Sense
J1-25	RtdB S-	J2-25	RtdD S-	

The RTD E- pins are also VME ground; RTDs should be floating to prevent ground loops.

Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

4.4 D9 Calibration Connector

A male D9 connector is provided for connection to an external precision voltage source. Each input channel incorporates a relay which allows it to be switched, under software control, to this test connector. The internal RTD subsystem check resistor is also switchable to the D9 test connector, allowing the accuracy of the reference junction acquisition circuits to be verified.

Pinout of the D9 is:

P3-7	CalSig+	to external precision voltage source
P3-6	CalSig-	or DVM "input" terminals
P3-9	CalSense+	to external DVM
P3-8	CalSense-	4-wire "sense" terminals
P3-1	Not connected	
P3-2	Not connected	
P3-3	Not connected	
P3-4	Not connected	
P3-5	Not connected	

An external voltage source may be connected to Pins 7 and 6, and a channel relay activated to allow the channel to measure the test source instead of its normal input. Additionally, V450-2 units, featuring BIST, have an on-board voltage source which may be used to drive these pins.

The 4-wire resistance measurement inputs of a precision DVM may be connected to Pins 7-6-9-8, and the resistance of the internal check resistor verified against the value reported in the VME registers.

The RELAYS register is used to control the channel relays; the MODE register controls access to the cal bus and test resistor.

Refer to Section 8 of this manual for a discussion of module calibration verification.

5 Operation

5.1 General Considerations

The V450 occupies 256 16-bit VME registers. DIP switches are provided to set the base address to any 256-word boundary in the A16 or A24 address spaces. All registers are implemented as true dual-port memory which is shared between the VMEbus and the internal microprocessor.

Typical VME access time is under 500 ns, measured from DS* to DTACK*.

The module is normally shipped configured for base address of 0xC000 in the A16 address space.

The V450 does not support single-byte writes from VME.

After powerup, basic module operations can be established with a few VME 16-bit writes:

Write up to four RTD control registers to enable any external RTDs that will be used as reference junction sensors; this is not necessary if the inputs are all voltage-mode or if the internal temperature sensor is to be used (Section 5.9.12).

Write up to 16 channel control registers to select a range and (if in thermocouple mode) desired reference junction for each channel (Section 5.9.17).

Read channel data registers; data will be continuously updated and, after channel setup, may be read at any time.

5.2 Front-Panel LEDs

The blue VME LED will flash whenever the V450 is addressed from the VMEbus.

The green CPU LED will blink once about every two seconds to indicate that the internal firmware is operating normally. If the MODE register is set to be nonzero, the CPU LED will blink twice as a warning that the module is in maintenance mode.

The red ERROR LED will normally be off. Blink patterns are:

One blink	Channel error
Two blinks	RTD acquisition error
Three blinks	RTD system self-check error
Four blinks	Calibration table error
Five blinks	FPGA configuration error
Steady light	Built-in self-test error

The last four blink patterns indicate fatal hardware problems.

The orange USER LED may be programmed from the VMEbus, as described in Section 5.9.6.

5.3 Voltage Measurements

Voltage measurements with the V450 require no reference junction, and therefore the RTDs can be entirely ignored. For each channel CHx, where x is 0 to 15, the V450 provides three 16-bit channel status registers, CTLx, UPCx, and RESx, and a 32-bit measurement register pair DHx:DLx. To begin making voltage measurements with the V450, simply write a channel control word into the CTLx register to tell the V450 the acquisition speed and full scale voltage range of the channel. (Section 5.9.17). For ranges ±500 mV and smaller, the option to use the open circuit detection is also available. The V450 will immediately begin acquiring data, updating the DHx:DLx pair at the requested rate.

The data register pair is scaled as a signed, 32-bit fractional value spanning the selected range.

Example

If the Channel 4 control register CTL4 were set to 10 decimal, selecting the ±12.5 volt range, scaling of the DH4:DL4 register pair would be:

Voltage	**DH:DL Decimal**	**Fractional**	**DH Hex**	**DL Hex**
+12.499...	+32767 : 65535	0.99999...	0x7FFF	0xFFFF
+6.2500	+16384 : 0	0.50000	0x4000	0x0000
+1.0000	+2621 : 28835	0.08000	0x0A3D	0x70A3
0.00000	0 : 0	0.00000	0x0000	0x0000
-2.0000	-5243 : 7865	-0.16000	0xEB85	0x1EB9
-12.500	-32768 : 0	-1.00000	0x8000	0x0000

So if DH4:DL4 is read as a signed 32-bit integer D,

$$V = D * 12.5 / 2^{31}$$

If 16-bit resolution is acceptable, one can read only the DHx word and treat that as a signed 16-bit fractional. So if DH4 is read as a 16-bit signed integer D,

$$V = D * 12.5 / 32768$$

5.4 Thermocouple Measurements

Thermocouples require more processing than raw voltages to measure accurately. In addition to the voltage presented to the V450, the temperature at the junction between the thermocouple wire alloys and copper must be compensated for. (See Appendix A for a background on thermocouples.) Most often this is done by measuring a platinum RTD that is mounted isothermally with the thermocouple-to-copper junctions, and using this temperature to perform the reference junction compensation. The V450 can be configured to transparently perform this task. First, RTDx, where x is A to D, must be configured by writing to the RTDx register, configuring that RTD channel for either 100R or 1000R RTD

types. Then the channel can be configured by writing to the channel control register CTLx, where x is 0 to 15. This control word includes information about desired sampling rate, the type of thermocouple connected, which reference junction to use, and whether or not to use the open thermocouple detection (Section 5.9.17).

If there is no RTD available, thermocouple wire can be run directly into the front panel D25 connectors of the V450 and the on-board temperature reference selected, with some loss of accuracy. Alternatively, if the reference junction temperature is known, perhaps acquired by another system, a thermocouple channel can also be programmed to use one of two user-programmable FAKE reference junction temperatures.

Once both reference junction and channel have been programmed, the V450 will begin acquiring data. Temperatures are always scaled as a signed integer representing temperature in °C times 16, presented in the DHx word. For temperatures, the DLx word is unused and forced to zero. The full-scale range is thus ±2048°C.

Examples

DECIMAL	HEX	TEMP, ºC
+32767	0x7FFF	+2047.93
+16384	0x4000	+1024.00
+00001	0x0001	+0.06250
00000	0x0000	0.00000
-3200	0xF380	-200.00

Resolution is thus $^{1}/_{16}$ (0.0625)°C, equivalent to 0.1125 ºF. If the reference junction is improperly programmed, the V450 will raise a channel error and continue reporting data as if bound to a 0°C reference junction.

The same format is used to report RTD temperatures. If an RTD is disabled or a measurement error is sensed, its temperature will be reported as 0x8000, equivalent to -2048°C.

5.5 Open Circuit Detection

For all thermocouple types, and voltage ranges ±500 mV and less, the V450 allows open circuit detection to be enabled by setting the OT bit in the channel control register (Section 5.9.17). When this bit is set, a current of -0.2 microamperes is injected into the thermocouple circuit.

A channel "open" error is declared if the measured voltage goes below the negative limit of the current ADC range. For thermocouple type channels, this will result in the standard thermocouple out of range result of -2048 C (0x8000). For voltage type channels, this will give the negative full scale reading (0x80000000). In either case, the channel error flag for the channel will be raised.

A request to use open detection on voltage ranges greater than ±500 mV is illegal; a channel error flag will be raised and the burnout current will be disabled. The channel, however, will continue to report the measurement voltage.

While the use of a burnout current is nearly universal among thermocouple measuring instruments, one disadvantage of this scheme is that the current can cause temperature measurement errors.

Example

> Injecting .2 uA into 100 feet of 24 gauge Type K extension wire will change the apparent voltage by about 30 uV, causing a temperature error of nearly a full degree C.

Unlike most thermocouple measuring instruments, the V450 can automatically calculate and subtract out this error if the channel wiring resistance is known. The V450 can measure the resistance (Section 5.6) or users may poke a known loop resistance value into any channel resistance register (Section 5.9.19).

5.6 Loop Resistance Measurements

Under many conditions, the V450 can automatically measure the loop resistance of a channel’s input by using the MEASURE LOOP RESISTANCE macro (Section 5.7.1). For this macro to operate properly the signal applied to the channel must be fairly stable through the three-second measurement interval. Ensure that the temperature of the thermocouple is not changing wildly during this time, or that any voltage signal is mostly stationary.

The content of a VME channel resistance register is used to compensate for open-thermocouple burnout current errors, regardless of whether the resistance value was loaded by the macro or by the user. This compensation will be more

accurate if the V450 is allowed to measure the resistance than if the resistance is entered manually; therefore, manual entry is advised only if the device being measured cannot tolerate the measurement current (20 uA max), or if the voltage stability mentioned above cannot be achieved.

5.7 Macros

During the usual course of operation, registers that are written by the user are never written by the V450 and vice versa. However, there are circumstances in which the V450 is asked to take control of certain user-write registers, such as the channel controls or the channel resistances. The V450 will only write to these registers in response to a user-executed macro.

The macro mechanism provides a means for the user to tell the V450 to perform certain finite duration tasks, rather than the usual operation of the board in which channels continue to return data until told otherwise. Some macros operate over all channels, some operate on the whole board, and others are user selectable as to which channels to apply the macro to.

Most macros that are user selectable expect a channel bitmask in PARAM0. This is a 16-bit word with each bit corresponding to one channel. The MSB corresponds to Channel 15 and the LSB to Channel 0; channels are selected by writing a 1 into their corresponding bit. By setting the PARAM0 register before writing the appropriate macro command code to the MACRO register, any combination of channels can selected.

In order to execute a macro…

- Verify that the MS bit (bit 15) of the MACRO register is clear, indicating that the V450 is ready to accept a command.
- Write the macro parameter, if required, into the PARAM0 register.
- Write into registers 128-143 for certain filter macros
- Write a 16-bit macro code to MACRO.
- Wait until the MS bit again clears. If MACRO is non-zero, an error has occurred.

Execution time will be no greater than the times noted below.

MACRO codes for the V450-1E are as follows:

Code	Operation	Time
0x8400	No operation	1 ms
0x8401	Set all channels to Type J thermocouple at 16.7 Hz, using the onboard reference junction.	1 ms
0x8402	Set all channels to Type K thermocouple at 16.7 Hz, using the onboard reference junction.	1 ms
0x8403	Set all channels to Type E thermocouple at 16.7 Hz, using the onboard reference junction.	1 ms
0x8404	Set all channels to Type T thermocouple at 16.7 Hz, using the onboard reference junction.	1 ms
0x8405	Set all channels to ±12.5 V at 16.7 Hz.	1 ms
0x8406	Set all channels to ±80 mV at 16.7 Hz.	1 ms
0x8407	Set all channels to ±25 mV at 16.7 Hz.	1 ms
0x8408	Program digital filtering (See section 7.)	10 ms
0x8409	Report digital filter setup (See section 7.)	1 ms
0x840B	Report analog filter types. (See section 7.)	0.3 sec
0x840C	Synchronize channels. PARAM0 bitmask specifies channels to sync (Section 5.7.2).	1 ms
0x8418	Measure thermocouple loop resistance. PARAM0 bitmask specifies channels to measure (Section 5.7.1).	3 sec
0x8420	Hard reboot; reloads FPGAs, restarts code; disappears from VMEbus for about 4 seconds (Section 5.7.3).	5 sec
0x8421	Soft reboot the module; remains on bus (Section 5.7.3).	1 sec

The V450-2 provides all of the same macro functionality as the V450-1 as well as additional automatic self-test macros.

Code	Operation	Time
0x8410	Full test sequence. Tests all channels, as well as RTD and temperature sensor subsystems.	80 sec
0x8411	Single channel test sequence. Number from 0 to 15 in PARAM0 specifies the channel to be tested.	50 sec
0x8412	Multiple channel test sequence. PARAM0 bitmask specifies the channels to be tested.	80 sec

See Section 6.2 for descriptions of the self-test macros.

5.7.1 Measure Loop Resistance

To use the MEASURE LOOP RESISTANCE macro, write a channel bitmap into PARAM0, then write 0x8418 to the MACRO register. The macro will take approximately 3 seconds to operate, regardless of number of channels selected, and afterwards all selected channel resistance registers will be updated.
A resistance greater than 16383.75 ohms will be represented as 16383.75 ohms (0xFFFF).

5.7.2 Channel Synchronization

Many data acquisition tasks require multiple measurements to be acquired simultaneously, with the guarantee that sample number *n* on one channel and sample *n* on another were taken at the same time. The V450 provides for this through the SYNCHRONIZE CHANNELS macro. This macro looks to the PARAM0 register for a bitmask of channels to be synchronized.

Upon executing this macro, any channel with its PARAM0 bit set to 1 will be reinitialized to the settings currently loaded into its respective CTL register. If all of the channels requested are set to the same update rate, this will force them into synchronization, and they will all provide updates at the same time. While the channels can also be simultaneously reset to different update rates, this will generally be less useful.

Multiple independent banks of synchronized channels can be created simply by executing the SYNCHRONIZE CHANNELS macro multiple times, changing the selection map in PARAM0. There are no restrictions governing which channels may be synchronized with which other channels.

After synchronization, realtime data of synchronized channels are updated starting with the highest numbered channel, and proceeding backwards towards the lowest. Therefore, watching the update counter of the lowest numbered channel selected for synchronization will reliably notify the user of newly acquired synchronous data and allow coherent reading of data from the entire synchronized group.

5.7.3 Resets

The V450 features two types of reset macros. The soft reset is the faster of the two, and will reset all internal data to power-up values. The hard reset will

temporarily remove the board from the VMEbus while it deconfigures and reconfigures all of the onboard logic.

5.7.4 Analog Filter IDs

The identifier codes for the plug-in analog filters on channels 0-15 can be read by first writing a channel bitmask into PARAM0, then writing 0x840B into the MACRO register. Filter IDs for channels 0-15 will be written into VME registers 128-143 respectively. See section 7.1 for more information about analog filtering.

5.7.5 Digital Filtering Macros

The digital filtering capabilities of the V450 can be controlled by programming the filter settings for channels 0-15 into VME registers 128-143 respectively, then writing 0x8408 into the MACRO register. Likewise, the current filter settings can be read back into these register by writing 0x8409 into the MACRO register. See section 7.2 for more information about digital filtering.

5.8 VME Register Map

The V450 implements 256 16-bit VME registers. REG# below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address.

Registers identified as "RO" should be treated as read-only and should not be written from VME; these registers are periodically refreshed by the uP.

Read-write (RW) registers are written by VME and are not altered by the internal microprocessor.

Read-write + macro registers (RWM) can be written by the user, but may also be changed by the V450 in response to a user executed MACRO command.
A macro handshake protocol is defined in Section 5.7.

32-bit data items are atomically interlocked and must be read in MS:LS word order. The MS word of 32-bit data may be read at any time.

REG Name	**REG#**	**Offset**	**R/W**	**Function**
VXI MFR	0	0x00	RO	VXI mfr ID: reads 65262 (0xFEEE)
VXITYPE	1	0x02	RO	module type, always 22450 decimal
SERIAL	3	0x06	RO	unit serial number
ROM ID	4	0x08	RO	firmware ID, typically 22451 decimal
ROM REV	5	0x0A	RO	firmware revision, typically ASCII "B"
MCOUNT	6	0x0C	RO	microprocessor IRQ update counter
DFILT	7	0x0E	RO	Digital filters active flags
CFLAGS	8	0x10	RO	channel error flags
RFLAGS	9	0x12	RO	RTD and misc. error flags
RELAYS	11	0x16	RW	controls calibration-bus relays
ULED	12	0x18	RW	user LED control
MODE	13	0x1A	RW	module operating mode
CALID	14	0x1C	RO	calibration table status
BISS	15	0x1E	RO	built-in self-test control **

REG Name	REG#	Offset	R/W	Function
MACRO	16	0x20	RWM	macro command register
PARAM0	17	0x22	RWM	macro parameter
PARAM1	18	0x24	RWM	macro parameter
PARAM2	19	0x26	RWM	macro parameter
YCAL	20	0x28	RO	calibration date, year
DCAL	21	0x2A	RO	calibration date, month/day
FAKE1	22	0x2C	RW	user-supplied fake reference temp
FAKE2	23	0x2E	RW	user-supplied fake reference temp
RTDA	24	0x30	RW	RTD A control
TMPA	25	0x32	RO	RTD A temperature
RTDB	26	0x34	RW	RTD B control
TMPB	27	0x36	RO	RTD B temperature
RTDC	28	0x38	RW	RTD C control
TMPC	29	0x3A	RO	RTD C temperature
RTDD	30	0x3C	RW	RTD D control
TMPD	31	0x3E	RO	RTD D temperature
TMPR	32	0x40	RO	onboard ref junction (pcb) temperature
RAHI	34	0x44	RO	RTD A resistance, MS, ohms
RALO	35	0x46	RO	RTD A resistance, LS, fractional ohms
RBHI	36	0x48	RO	RTD B resistance, MS, ohms
RBLO	37	0x4A	RO	RTD B resistance, LS, fractional ohms
RCHI	38	0x4C	RO	RTD C resistance, MS, ohms
RCLO	39	0x4E	RO	RTD C resistance, LS, fractional ohms
RDHI	40	0x50	RO	RTD D resistance, MS, ohms
RDLO	41	0x52	RO	RTD D resistance, LS, fractional ohms
TRHI	42	0x54	RO	test resistor, MS, ohms
TRLO	43	0x56	RO	test resistor, LS, fractional ohms

REG Name	REG#	Offset	R/W	Function
LBHI	44	0x58	RO	BIST loopback **
LBLO	45	0x5A	RO	
DH0	46	0x5C	RO	Channel 0 MS data
DL0	47	0x5E	RO	Channel 0 LS data
DH1	48	0x60	RO	Channel 1 MS data
DL1	49	0x62	RO	Channel 1 LS data
DH2	50	0x64	RO	Channel 2 MS data
DL2	51	0x66	RO	Channel 2 LS data
DH3	52	0x68	RO	Channel 3 MS data
DL3	53	0x6A	RO	Channel 3 LS data
DH4	54	0x6C	RO	Channel 4 MS data
DL4	55	0x6E	RO	Channel 4 LS data
DH5	56	0x70	RO	Channel 5 MS data
DL5	57	0x72	RO	Channel 5 LS data
DH6	58	0x74	RO	Channel 6 MS data
DL6	59	0x76	RO	Channel 6 LS data
DH7	60	0x78	RO	Channel 7 MS data
DL7	61	0x7A	RO	Channel 7 LS data
DH8	62	0x7C	RO	Channel 8 MS data
DL8	63	0x7E	RO	Channel 8 LS data
DH9	64	0x80	RO	Channel 9 MS data
DL9	65	0x82	RO	Channel 9 LS data

REG Name	REG#	Offset	R/W	Function
DH10	66	0x84	RO	Channel 10 MS data
DL10	67	0x86	RO	Channel 10 LS data
DH11	68	0x88	RO	Channel 11 MS data
DL11	69	0x8A	RO	Channel 11 LS data
DH12	70	0x8C	RO	Channel 12 MS data
DL12	71	0x8E	RO	Channel 12 LS data
DH13	72	0x90	RO	Channel 13 MS data
DL13	73	0x92	RO	Channel 13 LS data
DH14	74	0x94	RO	Channel 14 MS data
DL14	75	0x96	RO	Channel 14 LS data
DH15	76	0x98	RO	Channel 15 MS data
DL15	77	0x9A	RO	Channel 15 LS data
CTL0	78	0x9C	RWM	Channel 0 control
UPC0	79	0x9E	RO	Channel 0 update counter
RES0	80	0xA0	RWM	Channel 0 loop resistance
CTL1	81	0xA2	RWM	Channel 1 control
UPC1	82	0xA4	RO	Channel 1 update counter
RES1	83	0xA6	RWM	Channel 1 loop resistance
CTL2	84	0xA8	RWM	Channel 2 control
UPC2	85	0xAA	RO	Channel 2 update counter
RES2	86	0xAC	RWM	Channel 2 loop resistance
CTL3	87	0xAE	RWM	Channel 3 control
UPC3	88	0xB0	RO	Channel 3 update counter

REG Name	REG#	Offset	R/W	Function
RES3	89	0xB2	RWM	Channel 3 loop resistance
CTL4	90	0xB4	RWM	Channel 4 control
UPC4	91	0xB6	RO	Channel 4 update counter
RES4	92	0xB8	RWM	Channel 4 loop resistance
CTL5	93	0xBA	RWM	Channel 5 control
UPC5	94	0xBC	RO	Channel 5 update counter
RES5	95	0xBE	RWM	Channel 5 loop resistance
CTL6	96	0xC0	RWM	Channel 6 control
UPC6	97	0xC2	RO	Channel 6 update counter
RES6	98	0xC4	RWM	Channel 6 loop resistance
CTL7	99	0xC6	RWM	Channel 7 control
UPC7	100	0xC8	RO	Channel 7 update counter
RES7	101	0xCA	RWM	Channel 7 loop resistance
CTL8	102	0xCC	RWM	Channel 8 control
UPC8	103	0xCE	RO	Channel 8 update counter
RES8	104	0xD0	RWM	Channel 8 loop resistance
CTL9	105	0xD2	RWM	Channel 9 control
UPC9	106	0xD4	RO	Channel 9 update counter
RES9	107	0xD6	RWM	Channel 9 loop resistance
CTL10	108	0xD8	RWM	Channel 10 control
UPC10	109	0xDA	RO	Channel 10 update counter
RES10	110	0xDC	RWM	Channel 10 loop resistance
CTL11	111	0xDE	RWM	Channel 11 control
UPC11	112	0xE0	RO	Channel 11 update counter

REG Name	REG#	Offset	R/W	Function
RES11	113	0xE2	RWM	Channel 11 loop resistance
CTL12	114	0xE4	RWM	Channel 12 control
UPC12	115	0xE6	RO	Channel 12 update counter
RES12	116	0xE8	RWM	Channel 12 loop resistance
CTL13	117	0xEA	RWM	Channel 13 control
UPC13	118	0xEC	RO	Channel 13 update counter
RES13	119	0xEE	RWM	Channel 13 loop resistance
CTL14	120	0xF0	RWM	Channel 14 control
UPC14	121	0xF2	RO	Channel 14 update counter
RES14	122	0xF4	RWM	Channel 14 loop resistance
CTL15	123	0xF6	RWM	Channel 15 control
UPC15	124	0xF8	RO	Channel 15 update counter
RES15	125	0xFA	RWM	Channel 15 loop resistance
BIST DAC	127	0xFE	RW	Loopback DAC setting **

Registers tagged ** are reserved for BIST. Registers 128-255 are used as large buffers to interact with both BIST and the Filter macros; see section 7.

Registers 34-77 report data as 32-bit MS:LS register pairs. Each pair is atomically interlocked to avoid the possibility of a collision between a uP update and a VME read, which could result in incoherent data. To guarantee coherent data, the VME user must read the first (MS) word of each pair and then read the second (LS) word of that same variable. If only the MS data is of interest, it may be read at any time.

5.9 Detailed Register Descriptions

5.9.1 Module Overhead Registers

A group of read-only, fixed-value registers identify the module. They include:

VXI MFR: always reads 0xFEEE, Highland's registered VXI ID code.

VXITYPE: always reads 22450 decimal for both the V450-1 and V450-2.

SERIAL: module serial number.

ROM ID: firmware version, typically 22451 decimal

ROM REV: ASCII code identifying the revision letter of the firmware, typically 0x0042, ascii "B"

5.9.2 MCOUNT - Interrupt Count Register

The read-only MCOUNT register is an unsigned 16-bit integer which is incremented every microprocessor interrupt, about 4.096 ms.

5.9.3 CFLAGS - Channel Error Flags

The read-only CFLAGS register displays 16 channel error flags, with bits 0..15 corresponding to input channels 0..15.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

An error flag will be set if a channel is improperly programmed, if a channel is programmed as a thermocouple input and its corresponding RTD is disabled or in an error state, if an input is electrically over-ranged, or if an open thermocouple is detected. Error bits will self-clear once the channel returns to normal operation.

5.9.4 RFLAGS - RTD Error Flags

This register displays error flags for the four external RTD reference-junction temperature sensors and several miscellaneous conditions.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
								LM71	FPGA	CERR	ERRT	ERRD	ERRC	ERRB	ERRA

Bits 0..3 respectively flag errors in acquiring RTD A..D. If an RTD is programmed as "unused" (RT code 0) its error bit will not be active. An RTD error can result from an RTD resistance being out of the legal range (-65 to +150°C equivalent), open or incorrectly phased excitation or sense connections, shorts between wires or to ground, or excessive (over about 25 ohms per leg) leadwire resistance.

The ERRT bit will be high if the onboard self-test resistor appears to be out of range, indicating that the RTD measurement subsystem is not operating normally.

The CERR bit will be up if the module calibration table is corrupted.

If the FPGA bit is set, either the control or VME FPGA chips has a configuration problem. If the VME chip does not configure properly, it is likely that no VME operations can be executed at all.

The LM71 bit will be set if the onboard semiconductor temperature sensor is defective or the board temperature is outside of the range -20 to +80°C.

5.9.5 RELAYS - Calibration Bus Relays Control

The RELAYS register controls actuation of the sixteen channel test relays.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
K15	K14	K13	K12	K11	K10	K9	K8	K7	K6	K5	K4	K3	K2	K1	K0

If the user sets any bit ON, the corresponding channel test relay will be actuated. The analog input of the associated channel will then be disconnected from the front-panel D25 connector and connected to the internal cal bus, which may in turn be routed to the CALSIG+ and CALSIG- Pins (Pins 7 and 6) of the D9 test connector.

More than one relay may be operated at any time, resulting in the outputs of selected channels being connected in parallel to the cal bus. Upon altering the RELAYS register it may take up to 25 milliseconds before all relay contact changes have settled.

See Section 8 for a discussion of using the D9 connector for verification of module accuracy.

5.9.6 ULED - User LED Control

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on. Pattern 0xF000 would result in a blink pattern, 0.5 seconds on and 1.5 seconds off.

5.9.7 MODE - Calibration Bus Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							OFF							M1	M0

Users may set the MODE bits M1:M0 to values 0-3. Zero is the normal operating mode.

M1:M0	**Description**
00	Disconnects the D9 connector from the calibration bus. On V450-2 units with BIST enabled, this also connects the calibration bus to the internal voltage source, controllable by the BIST DAC register. See Section 6.1 for more information about the BIST loopback mode.
01	Connects the D9 connector to the module calibration bus, allowing the connection of a precision external voltage source to test the calibration of the module. All channels whose test relays are not operated will continue to function normally.
10	Connects the D9 connector to allow an external 4-lead DVM to measure the value of the internal self-check resistor, nominally 270 ohms. Its measured value should agree with the value reported in the TRHI:TRLO registers to within 250 PPM. In this mode, external RTD reference junction scanning is suspended and the associated reference junction temperatures frozen.
11	Connects the D9 connector to both the module calibration bus and the BIST DAC voltage source (V450-2 units only). This is similar to mode 01, however the only external equipment required is a DVM, rather than a precision voltage source. (Available on hardware revisions D and above only.)

Setting the OFF bit will disable the isolated power supplies to all 16 input channels. This is intended for factory test only; users whose systems require this feature should further discuss their application with Highland Technology.

5.9.8 CALID, YCAL, DCAL - Calibration Status Registers

The CALID register displays a value which reflects the currently installed calibration table. The normal value for the V450-1 and V450-2 modules is 22450 decimal, 0x57B2. If the factory calibration table is corrupted, the firmware will install the default calibration table, the CALID register will display value 0xDEFC, the CERR bit will appear in the RFLAGS register, and the red LED will flash.

YCAL and DCAL display the last date of module calibration. YCAL is the year, as an integer, such as 2006 decimal. The high byte of DCAL is month 1-12, and the low byte is day 1-31. The recommended factory recalibration interval for the V450 is one year.

5.9.9 FAKE1, FAKE2 - User Reference Junction Controls

The FAKE1 and FAKE2 registers allow the user to manually write reference junction temperatures for thermocouple channels. This allows the V450 to be used in a system where the thermocouple reference junction is measured by some means other than a platinum RTD. The registers take a signed 16-bit number, where one LSB represents $^{1}/_{16}$ of a degree Celsius. For information on binding a thermocouple channel to the FAKE reference junction temperatures, see Section 5.9.17.

5.9.10 BISS - BIST Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH	BCS	ISO	RTF	TSF				BSY							BAV

The BISS register provides status information for BIST enabled V450-2 modules. For the V450-1, lacking BIST, this register will always read zero.

The BAV bit will be true if the BIST option is available. If it is not available, the entire BISS register will read as all zeroes.

BSY will be true while automatic self-tests are running.

BCH will be set if automatic BIST tests discover a "hard" channel error, namely a gross malfunction. BCS will be set if a "soft" error is discovered. A soft error is

defined as an input channel error above ±1500 PPM (±3000 PPM on 25 mV and 250 V ranges), and a hard error is a channel error beyond ±2%.

The ISO bit will be set if electrical leakage is detected from a channel common to module ground.

The RTF bit will be set if an error is detected in the RTD acquisition subsystem.

TSF will be set if an error is detected in the local reference junction temperature sensor.

5.9.11 MACRO, PARAMx - Macro Controls

The macro control register allows the execution of pre-defined macros which perform automatic tasks. Some macros also take a parameter in the PARAM0 register. PARAM1 and PARAM2 are currently unused. See Macros, Section 5.7, for more information.

5.9.12 RTDx - RTD Configuration Controls

There are four RTD temperature sensor channels, each with an associated register block. The RTDs are called RTDA through RTDD, all being external to the V450, either customer supplied or within a J470 termination box. An internal semiconductor temperature sensor is also provided on the module, adjacent to the two D25 input connectors. Any of these sensors may be selected as the reference junction used by any of the 16 input channels when they are operated in thermocouple measurement mode.

Each RTD has a control register RTDx. It is arranged:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														RT1	RT0

where the encoded RT bits declare the RTD type.

RT Code	RTD Type
0	RTD channel is unused
1	100 ohm platinum, ISO 385 curve
2	1K ohm platinum, ISO 385 curve

If any RTD is programmed to be active, an RTD error flag will be reported in RFLAGS if the sensed temperature is out of acquisition range or if a

measurement error is detected. Any analog input channel which references a failed or disabled RTD will also report a channel error in the CFLAGS register.

5.9.13 TMPx, RxHI, RxLO - RTD Information Registers

Each RTD has a realtime temperature reporting register TMPx, which presents temperature in module-standard format, namely degrees C times 16. The V450 is capable of measuring RTD temperatures from -65 to +150°C.

If an RTD is programmed as unused, its temperature will be reported as zero, 0x0000 in the register. If an RTD is programmed as a 100 or 1K ohm type, and a measurement error is sensed in acquiring its temperature, its temperature will be reported as 0x8000, equivalent to -2048°C.

Any thermocouple input channel which references an unused RTD or one having an error will report a channel error flag in CFLAGS and act as if using a 0°C (ice point) reference.

The resistance of each RTD channel is also reported as a 32-bit value, with the MS word being resistance in ohms and the LS being a 16-bit fractional-ohm extension. The RxHI:RxLO register pair would thus contain 0x0064:0x8000 to indicate 100.5 ohms. A reported resistance of 0x8000:0000 indicates a resistance acquisition error.

The RTD resistance registers are interlocked to ensure atomic reads, namely that the VME user never reads mixed old/new data irrespective of when the uP updates the data. To ensure coherence, it is required that any pair of resistance registers be read in the order RxHI:RxLO.

5.9.14 TRHI, TRLO - Test Resistor Status Registers

The TRHI:TRLO register pair contains a reading of the on-board 270-ohm test resistor used to check the calibration of the RTD measurement system. The format is the same as described in Section 5.9.13 above. Test of the RTD subsystem calibration is described in Section 8, Calibration Verification.

5.9.15 LBHI, LBLO - Loopback Expectation Registers

The LBHI:LBLO register pair reports the expected BIST DAC voltage as determined at the time of module calibration. The scaling of the value is the same as that of a channel set to the intended voltage range as described in Section 6.1, Loopback Mode.

5.9.16 DHx, DLx - Channel Data Registers

Acquired voltages are presented in the DHx:DLx register pair as a 32-bit signed fractional relative to the selected voltage range, and temperatures are presented in the DHx register, as a signed temperature in degrees C times 16. Sections 5.3, Voltage Measurements, and 5.4, Thermocouple Measurements, describe the formats in detail.

Many applications can use only the most significant voltage word, DHx, and ignore the LS word. In this case, the DH register can be read at any time and treated as a 16-bit signed fractional. If extended resolution is needed, the DH:DL register pair may be used as a signed 32-bit fractional. In this case, it is mandatory that DH be read first, followed by DL. "High Endian" processors will generally read the pair as a 32-bit value, in the correct order, but if this is not known to be the case, read DH and then DL and merge.

5.9.17 CTLx - Channel Configuration Controls

Each of the 16 isolated input channels has an associated channel control register, CTL0 through CTL15. Users must initialize the control registers of any channels which will be active. The control register arrangement is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RF2	RF1	RF0		RS2	RS1	RS0	OT			RN4	RN3	RN2	RN1	RN0

The RN bits select the input type and range for this channel, with the five RN bits encoded 0 through 31 decimal. Ranges are:

RN Code	Channel Type	Range	Resolution
0	off		
1	voltage	± 25 mv	2.98 nv (approx)
2	voltage	± 50 mv	5.96 nv
3	voltage	± 80 mv	9.53 nv
4	voltage	± 125 mv	14.9 nv
5	voltage	± 250 mv	29.8 nv
6	voltage	± 500 mv	59.6 nv
7	voltage	± 1.25 v	149 nv
8	voltage	± 2.50 v	298 nv
9	voltage	± 5.00 v	596 nv

RN Code	Channel Type	Range	Resolution
10	voltage	± 12.5 v	1.49 uv
11	voltage	± 25.0 v	2.98 uv
12	voltage	± 50.0 v	5.96 uv
13	voltage	± 125 v	14.9 uv
14	voltage	± 250 v	29.8 uv
16	Type J t/c	-210 to 1200°C	0.0625°C
17	Type K t/c	-270 to 1372°C	0.0625°C
18	Type E t/c	-270 to 1000°C	0.0625°C
19	Type T t/c	-270 to 400°C	0.0625°C
20	Type R t/c	-50 to 1768°C	0.0625°C
21	Type S t/c	-50 to 1768°C	0.0625°C
22	Type B t/c	0 to 1820°C	0.0625°C
23	Type N t/c	-270 to 1300°C	0.0625°C

Selection of an undocumented range will result in zero volts reported and will set a channel error flag.

The OT bit, when set, enables open thermocouple detection. See Section 5.5, Open Circuit Detection. Open detection is available only for thermocouple ranges, and voltage ranges ±500 mV and less.

The three RS bits select which sensor is used for reference junction compensation for this channel. These bits apply to thermocouple modes only, and are ignored in voltage input modes.

RS Code	RTD Used	Connector Pins	Notes
0	RTD A	J1 9 10 22 23	External RTD
1	RTD B	J1 11 12 24 25	External RTD
2	RTD C	J2 9 10 22 23	External RTD
3	RTD D	J2 11 12 24 25	External RTD
4	internal	n/a	Internal reference
5	FAKE1	n/a	User-supplied ref temp
6	FAKE2	n/a	User-supplied ref temp
7	none	n/a	0°C (ice point) equivalent

RS code 4 uses the on-board semiconductor temperature sensor as the reference junction temperature. In this case, thermocouple-alloy extension leads should be wired directly to the D25 male connectors which plug into the V450 front panel. Because the front panel and connectors are not a well-controlled isothermal environment, this mode can be expected to be less accurate than using an external isothermal reference junction box with associated RTD sensor.

RS selections 5 and 6 use a temperature specified by the user in the FAKE1 or FAKE2 registers as the effective reference junction temperature, with temperature specified in the module-standard format of °C times 16. This allows other data acquisition systems to acquire and furnish reference junction temperature. These programmed values must be in the range of -65 to +150°C.

Selection 7 simulates using a reference junction at ice point. Millivolt inputs will display temperatures corresponding to the values shown in standard thermocouple tables.

A channel error will result if the selected RTD is disabled or presents a resistance that is out of range.

The three "RF" bits select ADC acquisition speed. The delta-sigma sampling architecture of the ADCs provides automatic digital filtering to reduce noise. Each new element of data also takes the previous into account; as a result step changes in input signal settle to 50% in one sample, then 100% in the next. At the slower sampling rates the V450 also provides notch filters at 50 Hz and 60 Hz in order to reduce the effects of power line hum on the signal.

RF Code	Samples/Second	Settling Time	Notes
0	16.7	120 ms	Good 50/60 Hz rejection
1	4.17	480 ms	Lowest noise; best 50/60 Hz rejection
2	8.33	240 ms	Better 50/60 Hz rejection
3	33.3	60 ms	
4	62.5	32 ms	
5	125	16 ms	
6	250	8 ms	
7	500	4 ms	

In general, the slower the sample rate, the lower the noise level and the better the 50/60 Hz hum rejection. See Figures 1 and 2 in Section 2 for typical RMS noise graphs. See the Analog Devices AD7793 datasheet for details of noise/speed tradeoffs.

5.9.18 UPCx - Channel Update Counter Registers

Each channel has a UPCx register. This is a 16-bit counter that is incremented every time the channel data is updated. The update rate depends on the ADC sample rate, as selected by the "RF" field of the channel control register.

5.9.19 RESx - Channel Resistance Registers

Thermocouple loop resistance may be measured by invoking the MEASURE LOOP RESISTANCE macro. After the macro is executed, loop resistance is presented in the channel's RESn register. The integer value is ohms * 4, with an LSB of 0.25 ohms. Maximum reportable resistance is thus 16383.75 ohms. Users may also measure or calculate loop resistance and write it to any channel resistance register. At powerup, the resistance defaults to zero, so no offset correction is applied.

5.9.20 BIST DAC - BIST Test DAC Control

The BIST DAC register provides manual control over the loopback test DAC, thus allowing a programmable voltage to be placed onto the V450s internal calibration bus. It takes a signed integer from -15 to +15, with zero being 0V, increasingly negative numbers being increasingly negative voltage, and increasingly positive numbers being increasingly positive voltage. For more information about manually-driven self-test, see Section 6.1.

The BIST DAC register is available only on the V450-2, with the built-in self-test feature. The V450-1 variant, lacking this functionality, ignores this register.

5.9.21 DFILT – Digital Filter Summary

Starting with the V450 revision E, onboard digital filtering is supported. While the details of the per-channel digital filter settings are only available through macro requests, the DFILT register provides a quick summary of which channels are currently enabled for digital filtering. The MSB corresponds to channel 15, the LSB to channel 0. A bit set to ‘1’ indicates a channel that has digital filtering enabled, a cleared ‘0’ bit indicates digital filtering is disabled.

See section 7.2 for more information about digital filtering.

6 BIST

The V450-2 features an array of built-in self-test features, both automated and interactive, to allow the user to test the functionality and accuracy of the unit without external equipment and without the need to disconnect from field wiring. Built-in self-test can be invoked at any time and under any conditions with no interaction between the self-test and external connections.

Note: BIST cannot allow absolute verification of module accuracy, as external NIST-traceable standards are required for formal calibration. When BIST is available, the registers in Section 5.8 which are flagged ** are active, and the corresponding BIST macros are available, as noted in Section 5.7.

BIST adds a digital-to-analog converter path that allows the module firmware to drive the internal calibration bus. When a channel's test relay is activated, connecting the channel input to the cal bus, the channel can measure and report the DAC output.

Although the BIST operations can detect most module failures, certain errors can be missed. They include:

- Failure of a connector pin or associated printed-circuit traces.
- Failure of certain RTD multiplexer paths; such failures will, however, probably cause an RTD measurement error to be reported.
- Failure of a channel test relay.

Two self-test facilities are provided for modules having the BIST option: Loopback Mode and Automatic BIST Mode.

6.1 Loopback Mode

Loopback mode is a non-automated BIST function, allowing the user to generate a known output voltage and measure it on the channels.

By setting the MODE register to 0, and the BIST DAC register to a value in the range ±15, a voltage is generated on the internal calibration bus. This voltage is intended to be read by a channel under test on a given range, and the result compared to the expected reading as given in the 32-bit LBHI:LBLO register pair. In MODE 0, the internal test bus is not connected to the D9 test connector.

By setting the MODE register to 3, the voltage output of the BIST DAC is available on the voltage pins of the calibration bus D9 connector (Pins 6 and 7), which is connected to the module calibration bus. While this voltage will no

longer exactly align with the calibrated BIST voltages, it will provide a stable voltage that is available to be read simultaneously by both an external precision DVM and by any channels of the V450 which have been switched to the calibration bus, and can be used to provide an external, traceable secondary calibration.

All BIST DAC voltage steps are calibrated at the factory. As a result the voltages and values actually present on a given board will be slightly different from the nominal values presented in the following table, which should be used only as a rough guide to operation. Users should use the accurate values presented in LBHI:LBLO for actual testing. The nominal voltages generated for the different BIST DAC values are listed in the table on the following page.

Example

> Write `-4` into the BIST DAC register to place approximately -120 mV on the calibration bus. The LBHI:LBLO register pair reports 0x8624DD30, corresponding to a factory calibration voltage of -119.000 mV. Then write `0x0001` into the RELAYS register to connect Channel 0 to the calibration bus. After writing `0x1004` into CTL0 to set Channel 0 to the most accurate sampling rate of 4.17 Hz and the 125 mV range, the DH0:DL0 register pair reports 0x86249A14, or -119.001 mV, a disagreement between the factory calibration and the channel measurement of 1 uV.

BIST DAC	Nominal Voltage	Intended Range	Nominal Reading
-15	-9.99 V	14	FAE2:8F5D
-14	-9.99 V	13	F5C5:1EB9
-13	-9.99 V	12	E66C:CCCD
-12	-9.99 V	11	CCD9:999A
-11	-9.99 V	10	99B3:3334
-10	-4.90 V	9	8280:0000
-9	-2.40 V	8	8500:0000
-8	-1.20 V	7	8500:0000
-7	-488 mV	6	8300:0000
-6	-375 mV	6	A000:5D57
-5	-240 mV	5	8511:BBD8
-4	-120 mV	4	8541:C7AC
-3	-75.1 mV	3	87C4:65E4
-2	-45.1 mV	2	8C93:9504

-1	-20.2 mV	1	98C6:95EA
0	0 V	ALL	0000:0000
1	20.2 mV	1	6739:6A16
2	45.1 mV	2	736C:6AFC
3	75.1 mV	3	783B:9A1C
4	120 mV	4	7ABE:3854
5	240 mV	5	7AEE:4428
6	375 mV	6	5FFF:A2A9
7	488 mV	6	7D00:0000
8	1.20 V	7	7B00:0000
9	2.40 V	8	7B00:0000
10	4.90 V	9	7D80:0000
11	9.99 V	10	664C:CCCC
12	9.99 V	11	3326:6666
13	9.99 V	12	1993:3333
14	9.99 V	13	0A3A:E147
15	9.99 V	14	051D:70A3

6.2 Automatic BIST Mode

Automatic self-tests are provided by means of BIST macro operations, using the MACRO register and associated parameters, and its status and results are reported in the BISS register.

Loading the MACRO register with 0x8410 performs a full module test. The RTD subsystem and the internal reference temperature sensor are checked, each of the 16 channels is tested for an isolation failure and for accuracy. This test takes about 80 seconds.

Macro 0x8411 allows an individual channel to be tested. Load the PARAM0 register with channel number 0..15 before executing the macro. The RTD subsystem and internal temperature sensor are not tested, but channel isolation and accuracy are. This test takes about 50 seconds.

Macro 0x8412 allows multiple channels to be tested. Load the PARAM0 register with a bitfield specifying the channels to be tested before executing the macro. Again, RTD and temperature sensors are not tested, but channel isolation and accuracy are. This test can take up to about 80 seconds.

Any of these tests may be aborted by writing 0xFFFF to the macro register. At the end of the test, the BISS register will indicate if any errors were detected. See Section 5.9.10 for a detailed description of the BISS register bits.

While any channel is being tested, the corresponding channel test relay is operated, disconnecting the input channel from the front-panel D25 connector. When channel tests are finished, the channel is restored to its normal programmed operation.

The green CPU LED will blink rapidly during automatic BIST operations. The red LED will go on solid if any error is detected, and will resume normal operation after the BIST sequence.
If any errors are reported in the BISS register, users may elect to review each error in detail. The block of registers from 128 to 255 are reserved for BIST error reports and are all cleared at the start of execution of any of the BIST macros. If any errors are detected during the automatic BIST operation, each error will generate a 6-word error report in this block of registers, with the first report posted to registers 128-133, and additional errors posted to sequential 6-word blocks, for a maximum of 21 errors.

The six words in each error report block are arranged:

0	Error summary word
1	null
2	MS word of "expected" value
3	LS word of "expected" value
4	MS word of "actual" value
5	LS word of "actual" value

The error summary word is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCH	BCS	ISO	RTF	TSF				ER3	ER2	ER1	ER0	EC3	EC2	EC1	EC0

where EC3..EC0 specify a channel, 0..15.

The ER3..ER0 range field applies to input channel errors and specifies the range on which the error was detected, encoded as:

1	±25 mV
2	±50 mV
3	±80 mV
4	±125 mV
5	±250 mV
6	±500 mV

7	±1.25 V
8	±2.5 V
9	±5.0 V
10	±12.5 V
11	±25 V
12	±50 V
13	±125 V
14	±250 V

The BCH...TSF bits specify an error condition; they are the same as for the BISS register described in Section 5.9.10.

An error summary word that is all zeroes indicates that no more errors have been posted.

A nonzero error summary word is followed by a zero word then four "value" words. The first two words are the expected value, as a 32-bit fractional, and the last two are the actual (measured) value.

For isolation errors, the value is the current through a sense resistor, with the "expected" value being zero. The full-scale range of the 32 bit measured value is ±100 mA.

If the error condition RTF is reported, the "expected" value is 270 ohms, and "actual" is the measured value of the on-board precision test resistor. Both are expressed as an MS word of integer ohms and LS word of fractional ohms.

If the error condition TSF is posted, the "expected" value is 25°C (400 decimal in the LS "expected" word) and the "actual" value is the internal reference junction sensor temperature, in the LS "actual" word only, in degrees C times 16.

When the “full test” or “multiple test” macros are executed, a maximum of four errors are reported per channel. For any of the BIST macros, a maximum of 21 errors are posted in the reporting space, VME words 128-253. In either case, all programmed tests are actually performed and the appropriate error flags are set in the BISS register.

VME register 254 increments each time the BIST system moves on to a new stage of the test, and location 255 displays the total number of errors detected.

The BSY bit, Bit 7 of the BISS register, will be set high while tests are being performed, and will clear to indicate completion.

7 Analog and Digital Filtering

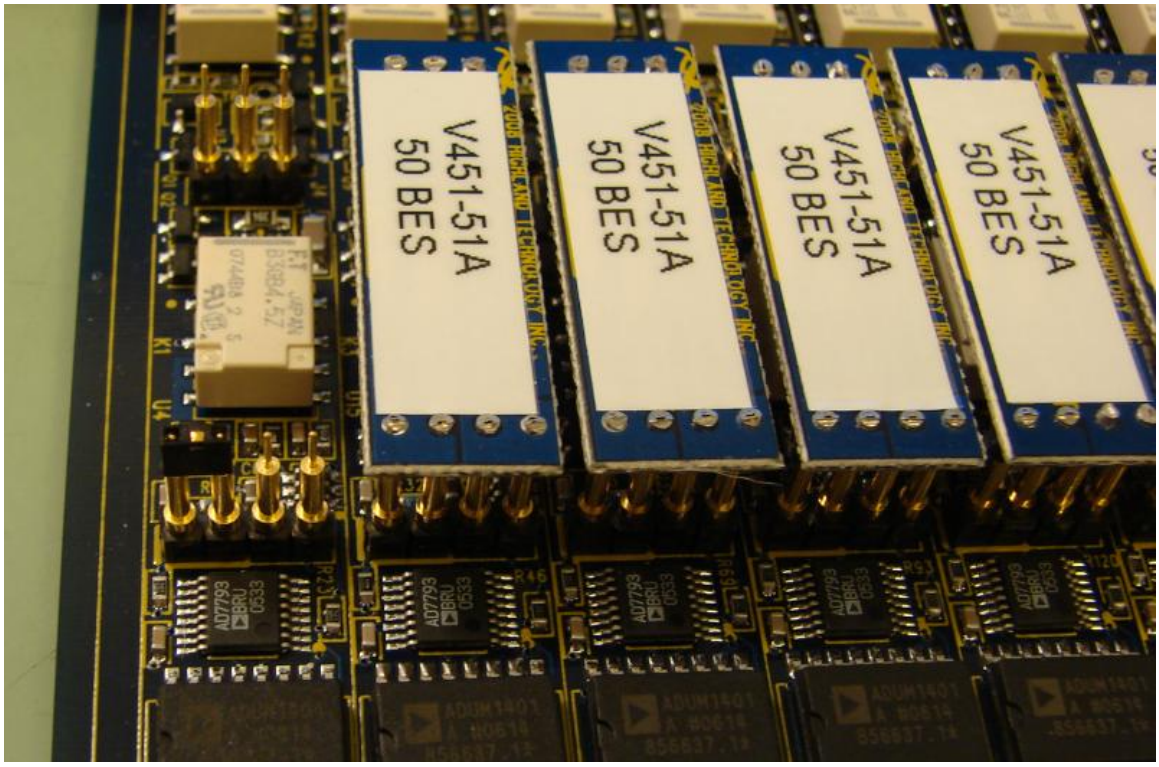
Starting with module revision E, the V450 includes user-programmable digital filtering and provision for plug-in analog lowpass filters.

Digital filtering is implemented in an on-board FPGA. Both voltage and temperature data is lowpass filtered, and the results posted to VME, at about a 2 KHz rate. Users may read channel data at any time and get the latest filter output. One application of digital filtering is to remove noise beyond the range of interest. Another use is to smooth out the steps associated with the inherent sample rate of the ADCs.

7.1 Analog Filters

The V450 has provision for per-channel plug-in 6-pole analog lowpass filters. If a filter is not installed on any given channel, a jumper shunt must be used to ensure signal continuity. These jumpers are included on the standard V450-1E and V450-2E modules.

The photo below shows filters installed, with a jumper on channel 0 in place of a filter. The "50 BES" on each filter indicates 50 Hz Bessel rolloff.



Filters are Highland part number V451-xx, where dash number "xx" defines the filter shape and 3 dB cutoff frequency. Currently available filters are...

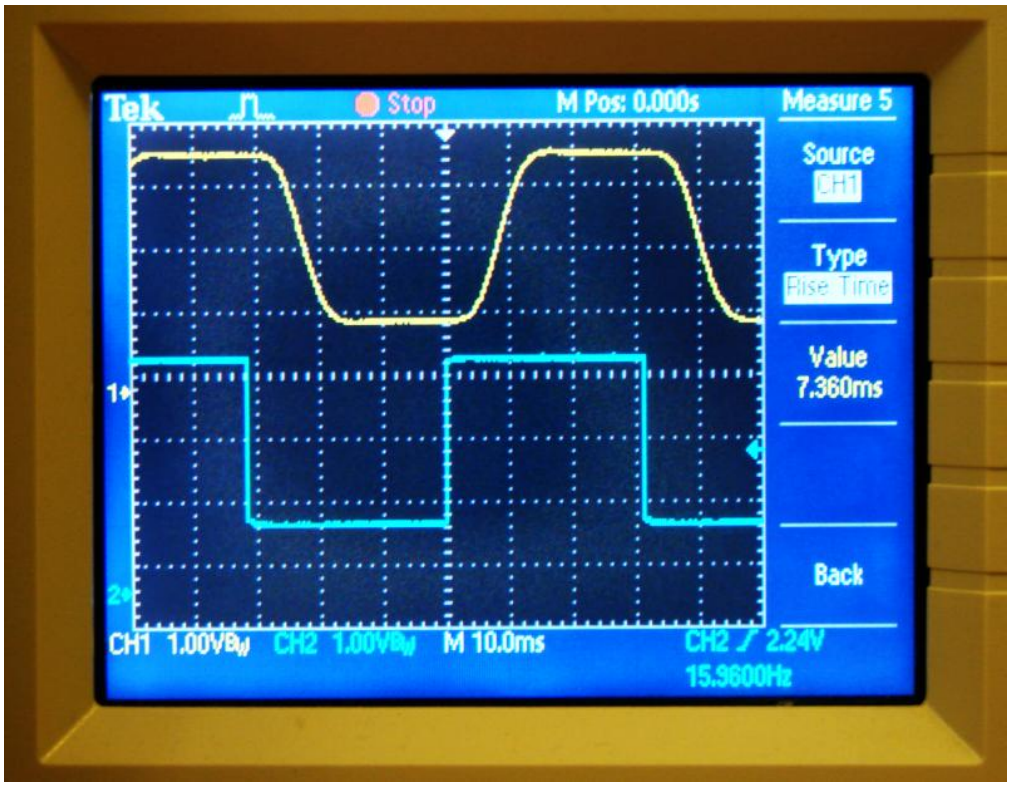
V451-50 50 Hz Butterworth

V451-51 50 Hz Bessel

If a V450 is factory-equipped with all 16 filters, the VME module part number is extended to specify the filter type. So a standard V450-1 becomes a V451-150 with 16 type 50 filters, or V450-251 for a V450-2 (BIST option) with type 51 filters.

Filters are preferably installed and tested at the factory. Users may install or replace filters in the field, by removing the module cover and removing an existing jumper or filter and plugging in a new filter. The filter module typically adds a small DC offset in the range of +3 to +7 microvolts; this offset is calibrated out when filters are factory installed.

The step response of the 50 Hz Bessel filter is shown below. Input is the blue trace, and filter output is yellow. Rise time is about 7.3 milliseconds.



A macro command is available to identify the presence and types of installed analog filters. Writing command 0x840B into the MACRO register will initiate a scan to determine installed filter types on channels specified by a bitmask in the PARAM0 register (0xFFFF to check filter IDs on all channels). Execution time is about 300 ms, during which time the channels will not report measurement data, and after which the MACRO register should clear to indicate completion. After the macro has run, VME registers 128 through 143 will present the dash number of filters installed on channels 0 through 15 respectively, zero if no filter is installed, or 0xFFFF if the filter appears to be an unknown type.

7.2 Digital Filters

The V450 rev E also includes programmable digital filtering. By switching the digital filters, the frequency response of the channels can be changed from software, without requiring changes to the V450 hardware itself.

When digital filtering is enabled, filter outputs are posted to the regular channel data registers about 4000 times per second, providing a pseudo-continuous input response that can be read at any time. Each new ADC sample is fed into the input of the filter at the programmed sample rate and appears as a step change. As opposed to channels with no digital filtering, filtered channels show the best performance with the sampling rate turned up to the maximum of 500 samples/sec.

The available digital filters on the V450 rev. E are:

F	Filter Type
0	Digital Filtering disabled
1	1 Hz 16-pole Butterworth
2	2 Hz 16-pole Butterworth
3	5 Hz 16-pole Butterworth
4	10 Hz 16-pole Butterworth
5	20 Hz 16-pole Butterworth
6	50 Hz 16-pole Butterworth
7	100 Hz 16-pole Butterworth
11	1 Hz 16-pole Bessel
12	2 Hz 16-pole Bessel
13	5 Hz 16-pole Bessel
14	10 Hz 16-pole Bessel
15	20 Hz 16-pole Bessel

16 50 Hz 16-pole Bessel
17 100 Hz 16-pole Bessel

To set up digital filtering, write the desired F values for all 16 channels into VME registers 128 through 143, corresponding to channels 0 to15. Then write 0x8408 to the MACRO register. After about a 2 millisecond delay, MACRO will clear, or it will return error code 0x0100 if an undefined F-code was selected. Undefined F codes will result in that channel being set to F=0, disabling digital filtering on that channel.

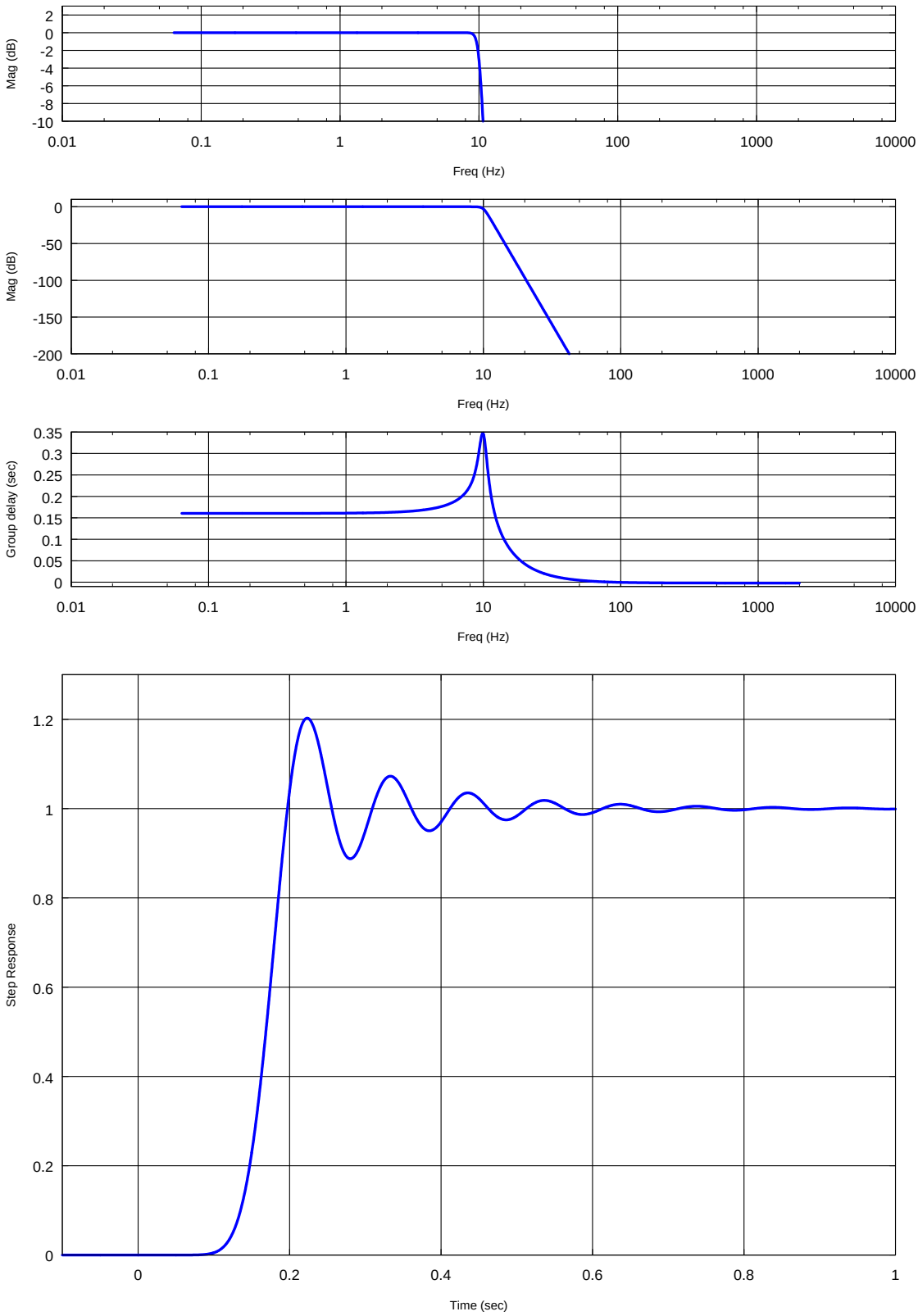
To read back digital filter selections, execute macro 0x8409. After macro completion, registers 128-143 will display the current F-codes for the 16 channels.

The DFILT register is a bitmap indicating those channels which have digital filtering enabled.

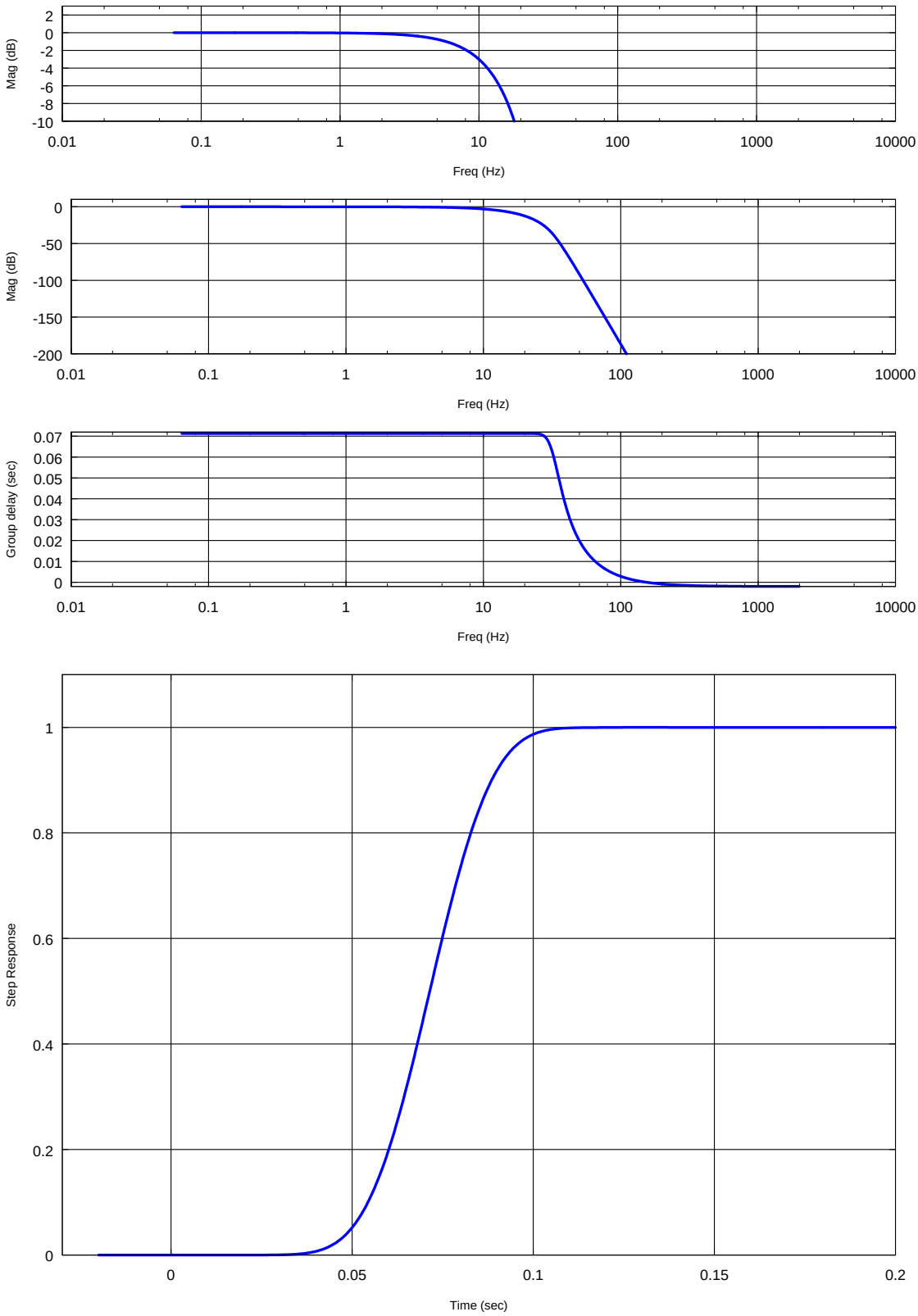
Example: channels could be equipped with 50 Hz analog anti-aliasing filters, programmed to operate at the maximum 500 Hz sample rate, and be enabled to use 20 Hz digital filtering. The resulting channel data would closely resemble a classic sampling-type ADC preceded by a 20 Hz analog lowpass filter, and the 500 Hz sampling steps of the delta-sigma ADCs would be smoothed into continuous-time appearing data. The digital filtering would buy back much of the resolution and s/n ratio that would normally be lost by programming the ADCs to their maximum rates.

As with conventional analog filters, the tradeoff between the Butterworth and Bessel filters is a trade between increased frequency selectivity and a clean transient response. The Butterworth filter, also known as a maximally flat filter, features very little frequency rolloff below the corner frequency, turning quickly into very sharp attenuation of frequencies above the corner, at the expense of a transient response featuring a roughly 20% overshoot that rings for quite a while before being fully damped. The Bessel filter, on the other hand, has a much more rounded frequency corner and less high frequency attenuation, but has no overshoot and settles out with no ringing. Additionally, for a given cutoff frequency the Bessel filter has roughly half the time delay that the Butterworth has.

The following pages show the 10 Hz Butterworth and Bessel filters for comparison. Filters of other frequencies will show the same response shapes, scaled in time and frequency accordingly.



10 Hz Butterworth Filter (F=4) Frequency and Step Responses



10 Hz Bessel Filter (F=14) Frequency and Step Responses

8 Calibration Verification

The calibration of one or more V450 modules may be verified in their operating VME crate.

To verify input channel accuracy, the V450 module or modules should be connected to a precision voltage source; wire source positive to P3 Pin 7 and negative to P3 Pin 6. Apply a known, stable voltage, activate one or more channel relays, select module MODE = 1, and read the channel data. This voltage can be produced by either a programmable precision voltage source or by a non-precision programmable source verified simultaneously with a precision DVM.

The V470-2 variant, with built-in self-test functionality, provides a verifiable programmable source on board, freeing the user from having to provide one separately. This source can be programmed by writing to the BIST DAC register as described in Section 6.1, and can be made available for measurement on P3 Pins 7 and 6 by setting MODE = 3. These pins can then be connected to a precision digital voltmeter, such as a Keithley 2000 or equivalent with the following connections.

P3 PIN	DVM Connection	Function	
P3-7	INPUT HI	CalSig+	test voltage +
P3-6	INPUT LO	CalSig-	test voltage -
P3-9	SENSE HI	Disconnected by V450	
P3-8	SENSE LO	Disconnected by V450	

Note: The channel ±25 mV range is used for thermocouple types T, R, S, and B, and the ±80 mV range is used for Types J, K, and E. Type N uses the ±50 mV range.

The RTD measurement subsystem can be verified using the same DVM connections as the voltage test by placing the DVM into four-wire resistance measurement mode. The required connections are:

P3 PIN	DVM Connection	Function	
P3-7	INPUT HI	CalSig+	test resistor excitation
P3-6	INPUT LO	CalSig-	test resistor excitation
P3-9	SENSE HI	CalSense+	test resistor sense
P3-8	SENSE LO	CalSense-	test resistor sense

Operate the module normally (MODE = 0) and note the resistance reported in the TRHI:TRLO 32-bit register pair. Then set the MODE register to 2 and use the DVM to make a 4-wire resistance measurement of the module's internal test resistor. The reading of the DVM should be 270 ohms ±0.25% and should agree with the reported TRHI:TRLO value to within 250 PPM, equivalent to an RTD temperature measurement error of 0.0625°C. Clear the MODE register to resume normal operation.

One may assume that, if voltage-mode measurements are accurate and if the RTD subsystem is also accurate, then thermocouple measurement will be correct.

The D9 connector pins of multiple Highland modules (such as the V450 Analog Input, V470 Analog Output, V420 Resistance Simulator, and V340 Waveform Generator) may be bussed in parallel to a single precision DVM, provided that only one module is switched to the test bus at any one time.

9 Quick Start Guide

The V450 ships with the address DIP switches set to address 0xC000 in A16 space. See Figure 6 in Section 4.1 to confirm that these switches are in fact in their default setting. Plug the V450 in, and power up the VME crate.

Read VME address 0xC002 in A16 space. This should read the number 22450 and the blue LED on the V450 front panel will briefly light, indicating VME access (Figure 7). This indicates that the V450 is functional. See Section 5.8 for a full register map.

Connect the positive terminal of a 9-volt source to Pin 1 of J1 (a 9-volt battery will work quite well). Connect the negative terminal to Pin 14 of J1. The 9 V is now connected to Channel 0. Write 0x000A into VME address 0xC09C, the CTL0 register. This activates Channel 0, sampling 16.7 times per second with a ±12.5 V full scale range. See Section 5.9.17 for a full description of the CTL0-CTL15 registers.

Any time more than 100 ms after writing the CTL0 register, you can now read VME address 0xC05C, the DH0 register, to get the 16 most significant bits of the acquired data.



Figure 7. VME Activity Light

To turn the data into volts, divide the contents of the register by 32,768 to get a fraction of full scale between -1 and +1, then multiply this fraction by 12.5 V, the full scale that Channel 0 is currently set to. If DH0 is 23,986, this corresponds to 0.7320 of full scale, or 9.15 V. See Section 5.3 for more information on making voltage measurements.

10 Sample Applications

10.1 VME Power Monitor

GOAL: Monitor the power supply of a mission-critical VME crate to be able to raise a user alarm in the event of unexpected power conditions. The power supply generates the following voltages: +5 V at 75A max, +12 V at 10A max, and -12 V at 10A max. The system must be able to detect a problem with the power within 10 ms of its occurrence.

SOLUTION: We will monitor the three supply voltages, the currents through each, and the temperature of the power supply, using half of a V450, a J470 termination box, and three 50 mV, 100 A current shunts. First, connect the current shunts between the supply voltages and the VME backplane. Ensure that any voltage sense connections for the supply are connected at the backplane side of the shunts to ensure proper voltage regulation. Also, tape, bolt, or weld a K-type thermocouple to the heat sink of the supply.

As shown in Figure 8, connect the V450 through a D25 cable to the J470 box. From the J470, wire the positive sides of Channels 0-2 to the supply voltages at the backplane. Wire the negative sides of these channels to VME ground, preferably close to the power connections. Connect Channel 3 across the current shunt on the +5 V supply, and Channels 4 and 5 across the current shunts on the ±12 V supplies. Because of the fully floating inputs of the V450, the common-mode voltages on these high-side current sensing shunts have no impact on the ability to measure the signals. Finally, connect the thermocouple to Channel 6. The floating inputs prevent a ground loop from occurring between the V450 and the chassis' grounded heat sink.

The V450 takes two samples to respond to a step change in input voltage. Therefore, in order to meet the requirement of a 10 ms response time, we must sample the data no slower than every 5 ms, and so we will set all of our voltage and current measurements to the 250 Hz rate, updating every 4 ms. The thermocouple itself responds to changes far more slowly than this, and so we will use the 16.7 Hz rate for it.

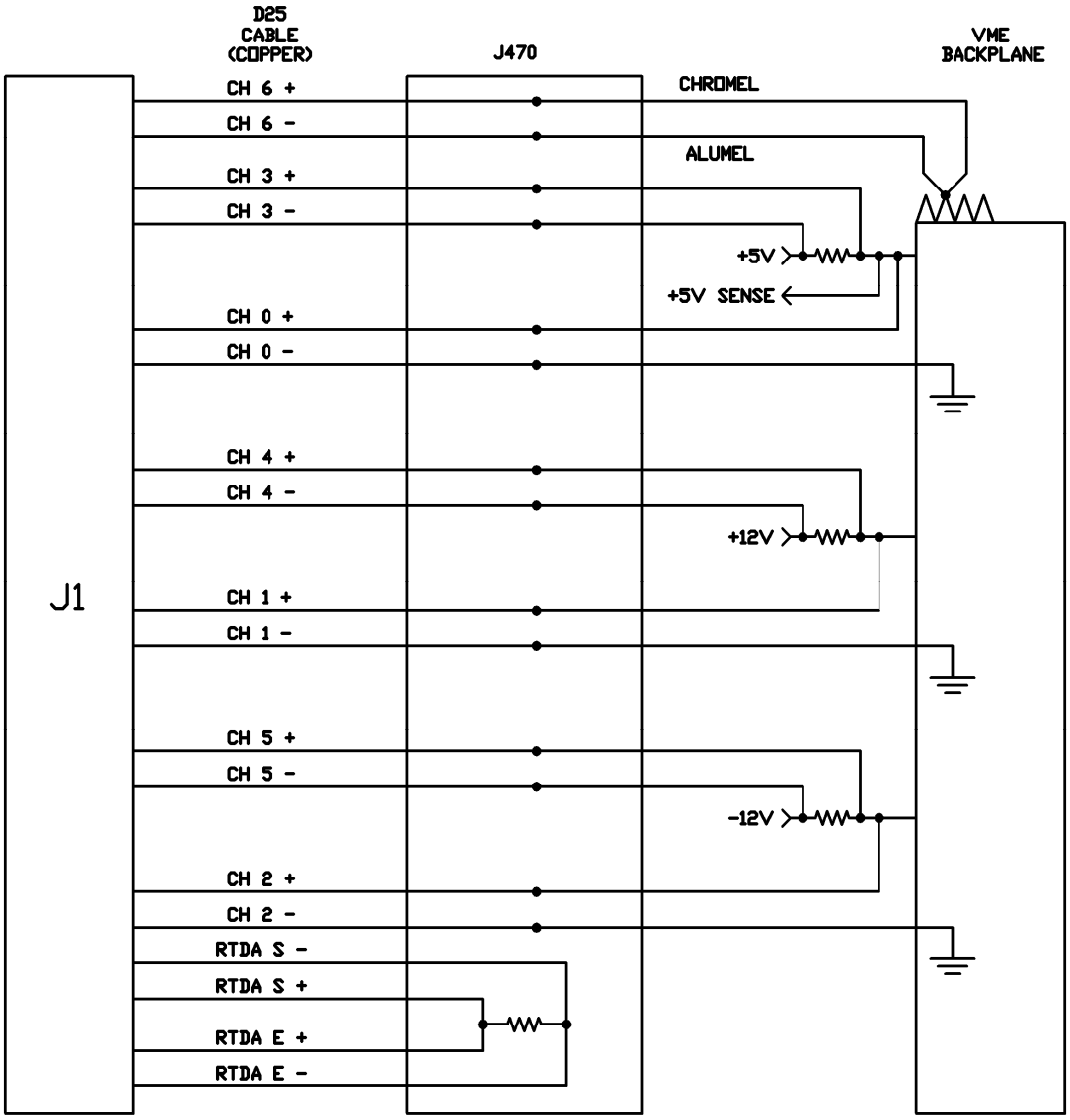


Figure 8. Connections for Monitoring a VME Power Supply

Power up the VME crate containing the V450. Program CTL0 through CTL2 to `0x600A`, which sets channels 0-2 to measure on the ±12.5 V range at 250 Hz. Program CTL3 to `0x6082`, the ±50 mV scale with open detection. Program CTL4 and CTL5 to `0x6081`, the ±25 mV scale with open detection. This allows maximum resolution on the current shunts while still allowing some headroom in the measurements. Program RTDA to `0x0001` to correctly read the 100R RTD buried in the J470. Then program CTL6 to `0x0091` to set it up as a Type K thermocouple, compensated by RTDA, with open detection. Finally, in order to properly compensate for the measurement errors introducted by the open detection on channels 3-6, write `0x0078` into PARAM0, then `0x8418` to

MACRO to execute a resistance measurement. Knowledge of the loop resistances of the low voltage channels now allows the V450 to make error-free measurements of these signals while providing notification should a break occur in the wiring.

After completion of the macro, the V450 will begin providing measurements of voltage, current, and temperature. The voltages are scaled to ±12.5 V full scale; therefore multiply 32-bit values DH0:DL0, DH1:DL1. and DH2:DL2 by (12.5×2^{-31}) to turn them into actual voltages. On the current shunts, 50 mV represents 100A; therefore Channel 3, set to 50 mV, is scaled out of ±100 A full scale; get the +5 V current by multiplying DH3:DL3 by (100×2^{-31}) for current in amperes. Channels 4 and 5, on 25 mV ranges, are only ±50 A full scale; multiply DH4:DL4 and DH5:DL5 by (50×2^{-31}) for the current on the ±12 V supplies. Finally, the thermocouple temperature is obtained by dividing DH6 by 16. The most current data will be continually posted, and so the monitoring software has only to read these values as often as desired.

10.2 Temperature Data Logger

GOAL: Map the temperatures across a device at 16 different points. Data will go to generate an animation where the temperature gradients across the device are shown changing over time, with each frame of video representing 120 ms steps.

SOLUTION: Attach 16 Type-K thermocouples to the device at key points. Connect these thermocouples to two J470s, one connecting Channels 0-7, the other Channels 8-15. Connect the J470s to the V450 by way of two D25 cables.

Write `0x2091` to CTL0-CTL7 to set them to 8.33 Hz sampling rate, Type-K thermocouples, with open circuit detection, referenced to RTD A. Write `0x2291` to CTL8-15 to set them similarly, but referenced to RTD C. This matches each set of 8 thermocouples to the buried RTD reference in its respective J470. Measure the loop resistances on all the channels by writing `0xFFFF` into the PARAM0 register, then `0x8418` into MACRO. Wait three seconds or so for the macro to finish; the most significant bit of the MACRO register will clear to indicate completion.

Once the resistances are known, the channels must be synchronized; otherwise the data in the video would be out of time-alignment with each other. Write `0xFFFF` into PARAM0 again, and then write `0x840C` into MACRO. This resets all the channels, forcing them into a synchronized state after the macro completes.

To read the data out, begin polling the UPC0 register. Every time it advances, all of the synchronized data has been updated. Therefore, the next synchronized

data set can be read by rapidly reading DH0-DH15 and grabbing all of the measurements. DL0-15 will be all zero on thermocouple measurements, and thus can be ignored. To avoid missing data, care should be taken to ensure that all data registers are read in less than 100 ms.

With the data read, turn the temperature data into degrees Celsius simply by dividing the values from DHx by 16. This data of temperature over time may be combined with CAD views of the device being monitored to create false-color video to show temperature gradients, thermal flows, and hotspots.

11 Versions

Standard versions of the V450 include:

V450-1: 16-channel VME analog input module

V450-2: 16-channel VME analog input module with BIST

V450-151: 16-channel VME analog input module with pre-installed V451-50 50 Hz 6-pole analog bessel filter option

V450-181: 16-channel VME analog input module with pre-installed V451-80 200 Hz 6-pole analog bessel filter option

V450-251: 16-channel VME analog input module with BIST and pre-installed V451-50 50 Hz 6-pole analog bessel filter option

V450-281: 16-channel VME analog input module with BIST and pre-installed V451-80 200 Hz 6-pole analog bessel filter option

12 Customization

Consult factory for information about additional custom versions.

13 Hardware and Firmware Revision History

13.1 Hardware Revision History

Revision G	Mar 2015 Fixes channel isolation problem in Revision F
Revision F	Jan 2015 Functionally equivalent to Revision E Revision F hardware is not shippable
Revision E	Nov 2008
Revision D	Aug 2006
Revision C	May 2006
Revision B	Feb 2006
Revision A	Dec 2005 Initial PCB release

13.2 Firmware Revision History

22451 Revision F	Mar 2015
22451 Revision E	Sep 2014 For Rev E and Rev F hardware, supports BIST and digital and analog filters Code rev E changes the BIST zero-check limits
22451 Revision D	Oct 2010 For Rev E hardware, supports BIST and digital and analog filters
22451 Revision C	May 2009 For Rev E hardware, supports BIST and digital and analog filters Fixes a problem where the MACRO register was not cleared during a soft reset, thus leading to an endless loop of soft resets in 22451B
22451 Revision B	May 2009

	For Rev E hardware, supports BIST and digital and analog filters
22451 Revision A	Sep 2006 For Rev D hardware, supports BIST
22450 Revision C	Sep 2006 For Rev B and Rev C hardware, supports BIST
22450 Revision B	Apr 2006 For Rev B hardware, supports BIST BIST erroneously registers isolation errors if the BIST DAC had been manually programmed to output a large negative voltage prior to initiating automatic BIST
22450 Revision A	Mar 2006 For Rev B hardware, does not support BIST

14 Accessories

J470	8-channel D25 female isothermal termination box
J475-1	8-channel D25 female Din rail termination panel
J475-2	8-channel D25 female Din rail termination panel w/ reference junction sensor
J55	6' shielded D25 male to D25 male cable
J56	10' shielded D25 male to D25 male cable
J71	Dual D9 male to Agilent 34104A cable
J75-1	D9 male to two(2) dual banana plug cable
J76	D9 OpenCVA busing cable
V451-50	V450 Plug-In Filter, 50 Hz Bessel version (factory installation only)
V451-80	V450 Plug-In Filter, 200 Hz Bessel version (factory installation only)

15 Appendix A: Thermocouple Theory and Notes

A thermocouple is a pair of dissimilar-alloy wires used to measure temperature. Any metallic alloy can be thought of as having an intrinsic energy level or voltage that is a nonlinear function of temperature. This voltage is usually in the range of about 5 to 40 microvolts per degree C.

The figure below illustrates a Type "K" thermocouple. Since the chromel and alumel alloys have different thermocouple voltage versus temperature functions, a voltage appears at the ends of the leads that depends on the temperature gradients along the wires. If we want to measure the junction temperature, we connect a voltmeter to the ends of the thermocouple leads

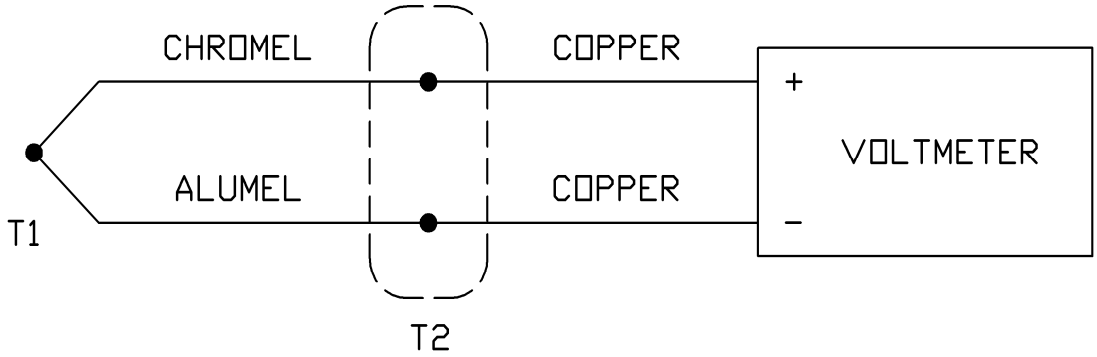


Figure 9. Type “K” Thermocouple

In this case, T1 is the temperature to be measured and T2 is called the "reference junction temperature". NIST publishes thermocouple temperature/voltage tables which assume that the reference junction is kept at ice point, zero degrees C. If the reference junction cannot be maintained at zero C, its temperature can be measured and a correction factor applied to the indicated voltmeter reading, so the ice-point-based lookup tables can then be used.

Note: Because the thermocouple effect is nonlinear, the voltmeter reading is not an accurate function of the temperature difference between T1 and T2: it is more correctly a function of the difference in thermocouple potentials at T1 and T2.

Many thermocouple instruments apply a linear correction to the measured voltage, as a function of reference junction temperature, but this is only an approximation. Ideal thermocouple reference junction compensation corrects the voltmeter reading by the actual, nonlinear thermocouple potential at point T2, which is the technique used in the V450.

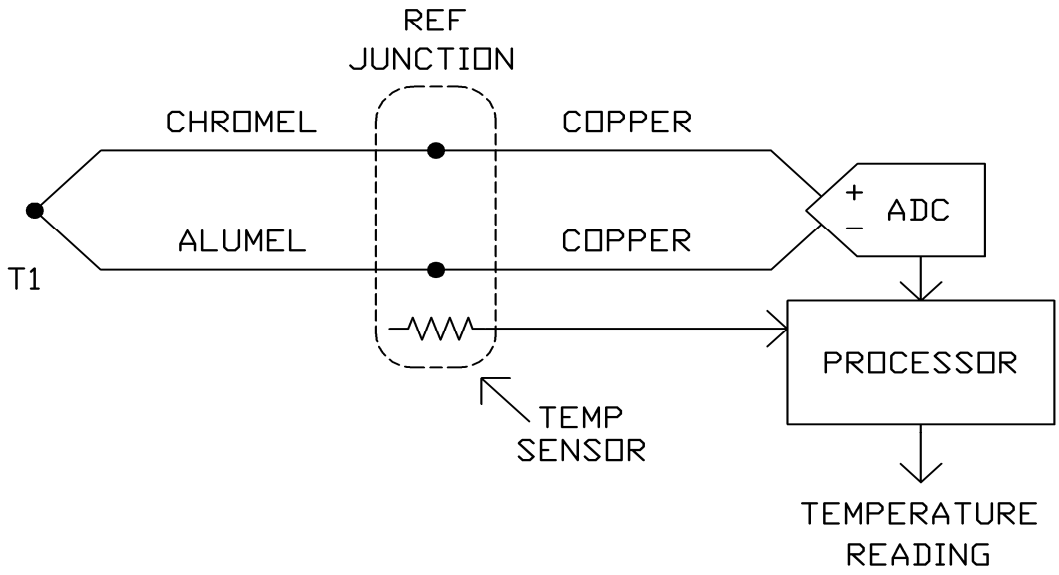


Figure 10. Type “K” Thermocouple with Temperature Sensor

Here, the microprocessor is given a thermocouple type and also reads a temperature sensor at the reference junction temperature T2. Within the reference junction box are screw terminals where the transition is made from copper-copper leads to the actual thermocouple alloys. It is important that both screw terminals and the temperature sensor be at the same temperature in order for the compensation to be accurate.

Given that the entire junction box is isothermal, the temperature sensor eading can be converted to the appropriate nonlinear offset voltage for the thermocouple type, and this offset applied to the voltage measured across the thermocouple.

The V450 includes the capability to measure up to four platinum RTD temperature sensors to perform the reference junction math. Any of the 16 input channels may be assigned to use any one desired reference junction sensor. The module assumes that the RTDs are calibrated to 100 or 1000 ohms at zero degrees C, and that they follow the standard ISO "385" nonlinearity curve. RTDs are connected as 4-wire devices to eliminate errors caused by the resistance of connection wires from the V450 to the reference junction.

The cabling from the front panel of the V450 to the reference junction can be ordinary connectors and copper wiring. Appropriate connector shells should be in place to ensure that all pins within the mating connector are reasonably isothermal and protected against air currents and thermal transients. Shielded wiring is preferred, with the shield bonded to the connector shell, which is VME front-panel and chassis frame ground.

If the internal temperature sensor of the V450 is to be used, the thermocouple wires should be extended all the way to the front panel of the module, soldered or crimped into the pins of the mating connector to J1 or J2. Program the channel control register to specify the internal sensor, RS code 4. Because the sensor is on the printed-circuit board but the reference junction is effectively within the mating connector, isothermal conditions will be poor and errors on the order of several degrees C may be expected.

There are many potential sources of error in thermocouple measurement:

- Imperfection in the reference-sensing RTD and the V450 RTD acquisition subsystem.
- Non-isothermal reference junction.
- Voltage drop in thermocouple wires.
- Imperfect thermocouple wire chemistry.

A V450 using the J470 termination box will typically have errors below ±0.2°C over the full Type "K" range. Type K thermocouples are available with standard accuracy limits of ±2.2°C or 0.75% of temperature, whichever is greater; "Special limit" thermocouples are available with errors of about half that. So the V450 will usually not be a significant error contributor compared to inherent thermocouple accuracy.

16 Appendix B: Thermocouple Types

Type	± Alloys	Range °C	uV/°C	USA Colors	IEC Colors
J	Iron/Constantan	210 to 1200	50	white/red	black/white
K	Chromel/Alumel	-270 to 1372	39	yellow/red	green/white
E	Chromel/Constantan	-270 to 1000	59	violet/red	violet/white
T	Copper/Constantan	-270 to 400	39	blue/red	brown/white
R	Pt-13Rh/Platinum	-50 to 1768	5	black/red	orange/white
S	Pt-10Rh/Platinum	-50 to 1768	5	black/red	orange/white
B	Pt-30Rh/Pt-6Rh	0 to 1820	10	grey/red	grey/white
N	Nicrosil/Nisil	70 to 1300	26	orange/red	pink/white

Note: The negative wire is always red in the USA/ANSI color code, and always white for the IEC colors.

Type B has a near-zero thermal coefficient at room temperature, so is often used without a reference junction sensor, namely programmed to use a simulated ice point reference.

17 Appendix C: Accessories

The J470 is an enclosed 8-channel isothermal termination box with integral 100R RTD reference-junction sensor connected to RTDA. Terminals are provided for four-wire connection to an off-board RTDB if desired. It is recommended for connections to thermocouples, voltage sources, or combinations of the two. It may be located up to 300 feet from the V450, and can be connected using standard "RS232" type shielded 25-pin copper-wire cable assemblies. One or two J470's may be connected to each V450.

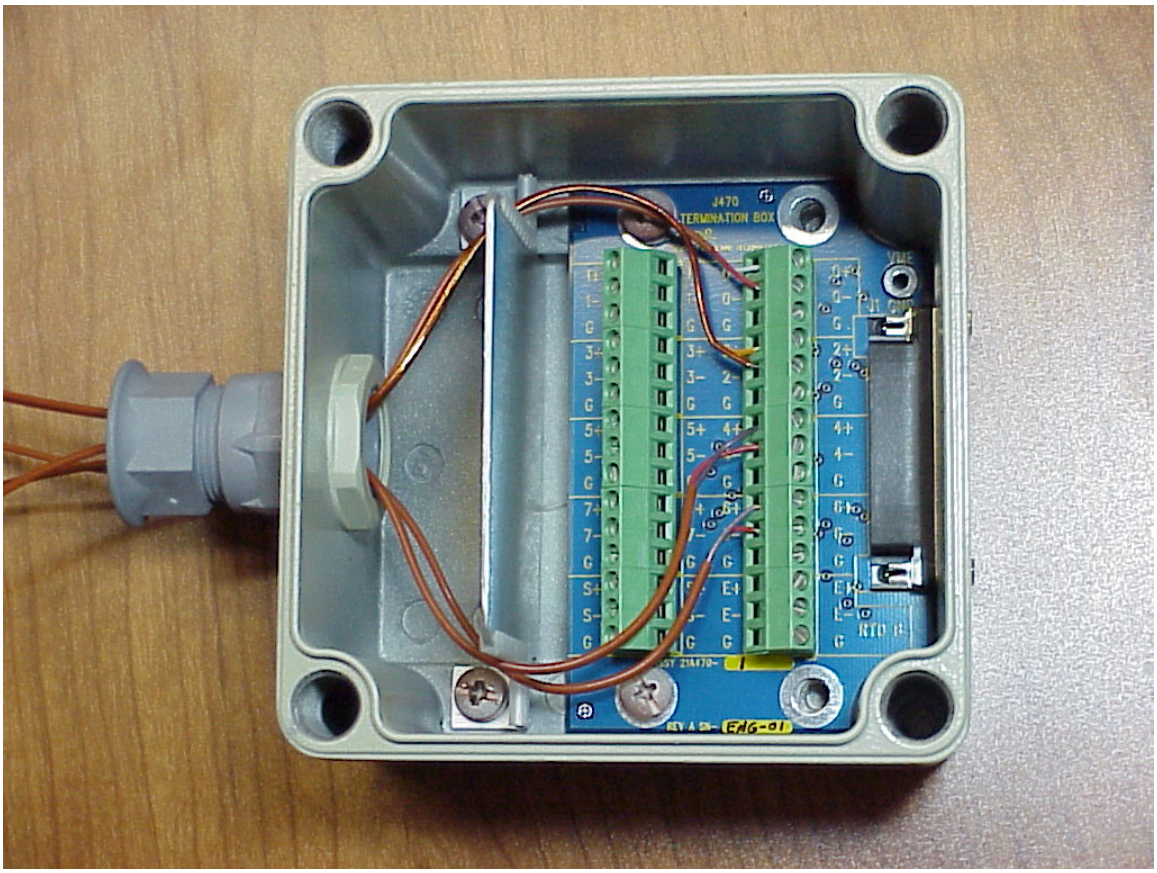


Figure 11. Model J470 8-channel Isothermal Termination Box

The J475 is a DIN-rail mountable 8-channel PC-board termination panel that transitions from a D25 connector to screw terminals. As provided it is recommended only for voltage sources; the J475 does not include a built-in reference junction sensor. Terminals are provided for four-wire connection to an off-board RTDB if desired. It may be located up to 300 feet from the V450, and can be connected using standard "RS232" type shielded 25-pin copper-wire cable assemblies. One or two may be connected to each V450.

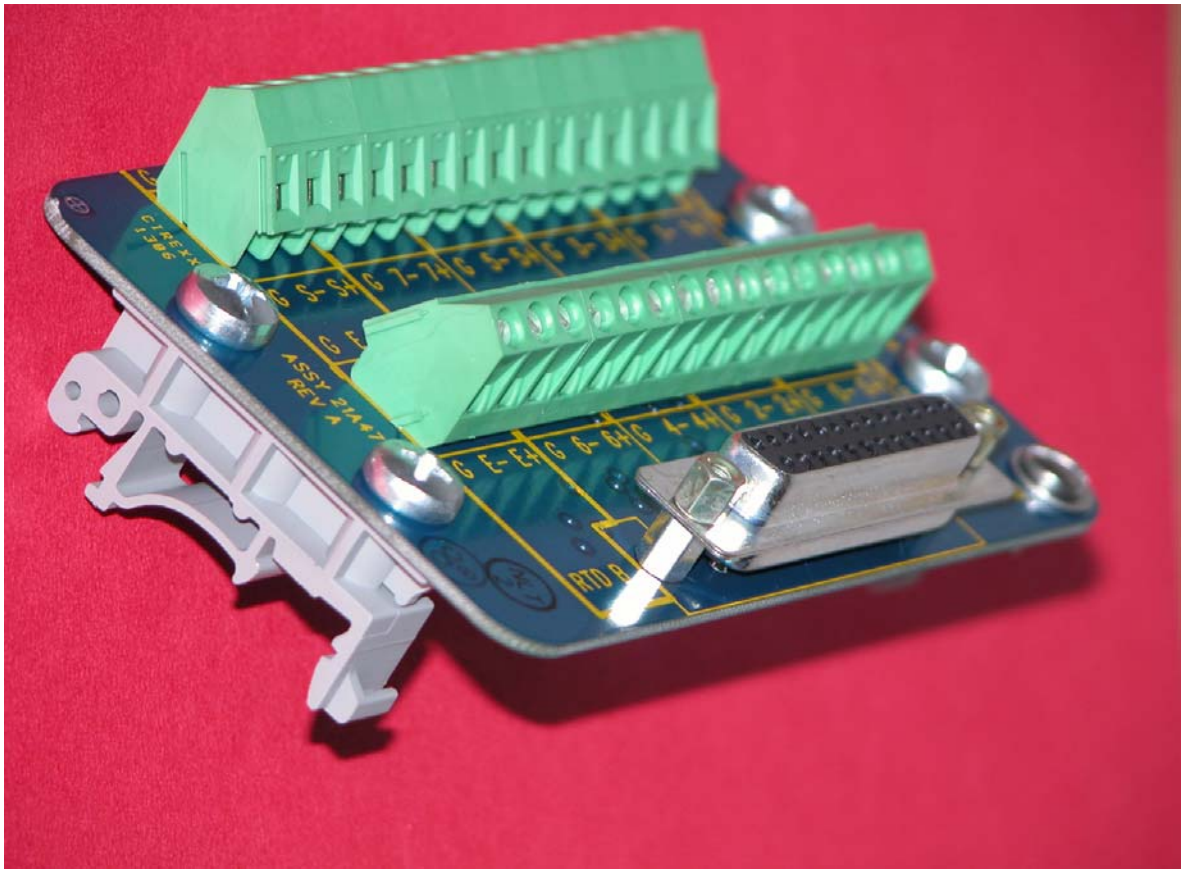


Figure 12. Model J475 8-channel DIN-rail Panel

18 Appendix D: Module Versions

The standard version of the V450 is the Model V450-1E, Highland Part Number 22A450-1E. It incorporates firmware version 22451D. Module revision E added programmable digital filtering and provision for plug-in analog lowpass filters.

The V450 is also available as Model V450-2E, incorporating built-in self-test features. It is Highland Part Number 22A450-2E, and incorporates firmware version 22451D.

The plug-in analog filter assembly is model V451-xx, where dash number "xx" specifies the filter response; see section 7

If a unit is factory-provisioned with 16 type "xx" filters, the xx is appended to the base module number, so a V450-2E becomes a V450-251E if all 16 type 51 filters are installed.

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