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V545
24 - CHANNEL VME SYNCHRO / LVDT / ACQUISITION MODULE

Technical Manual

February 15, 2019

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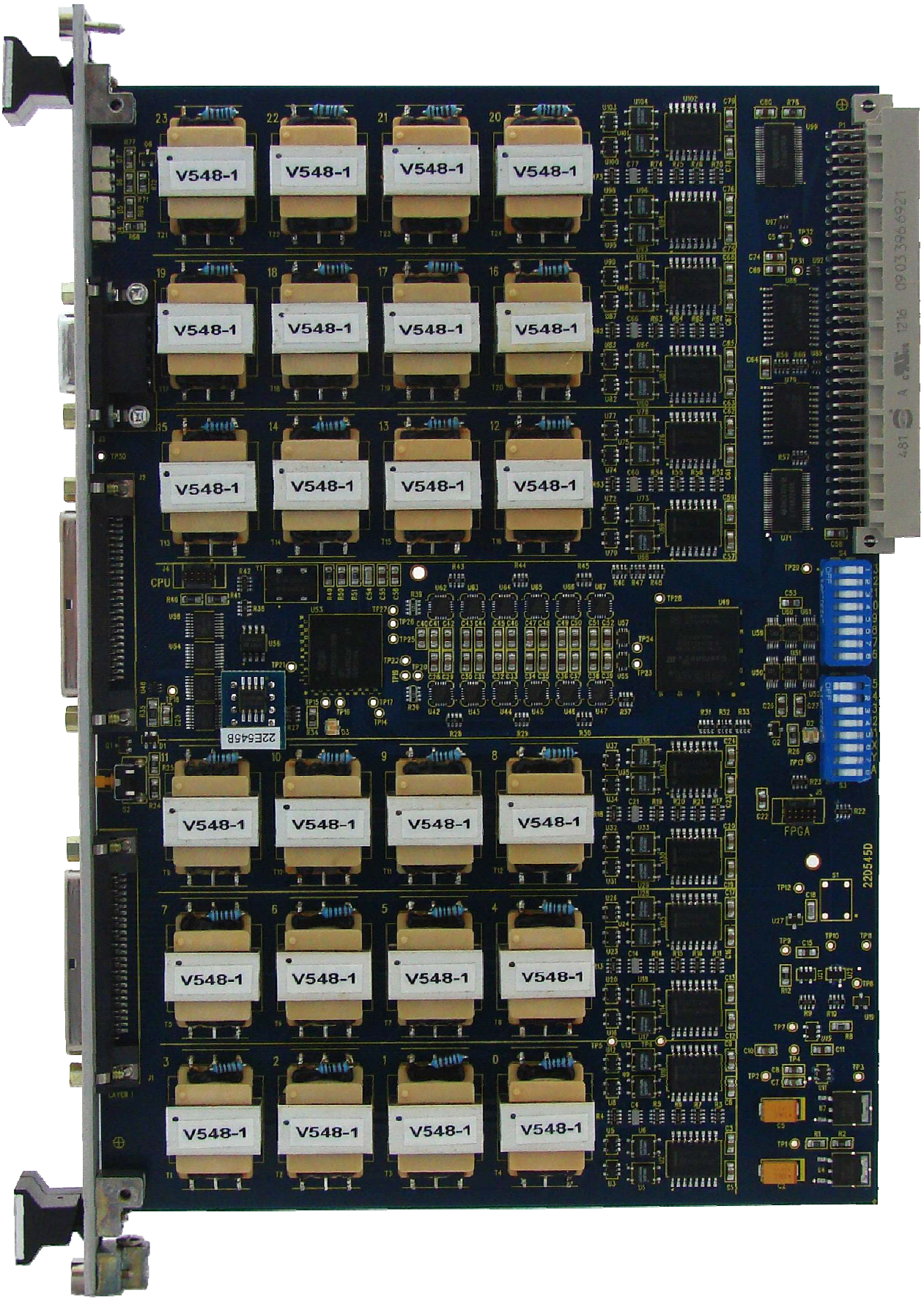
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V548-1
CPU
FPGA

1. Introduction

This is the manual for the V545, a 24 channel synchro/resolver/LVDT/RVDT measurement/simulation VME module.

Features of the V545 include:

- 24 transformer-isolated AC sinewave generator/acquisition channels
- Generalized ADC-DAC-DSP architecture
- Programmable functions include:
    - LVDT/RVDT acquisition, with internal or external excitation
    - LVDT/RVDT simulation, with internal or external excitation
    - Synchro/resolver acquisition, with internal or external excitation
    - Synchro/resolver simulation, with internal or external excitation
    - Poly-phase sine wave generation from 250 Hz to 20 KHz
    - True RMS voltage measurement
    - Synchronous detection
    - Frequency measurement
- Realtime voltage and frequency measurement, all signals in all modes
- 16 bit ADC and DAC resolution
- Internal ARM9 CPU performs macro functions
- Generalized function block capability
- Clearly labeled dipswitches set VME address; no jumpers, headers, or trimpots

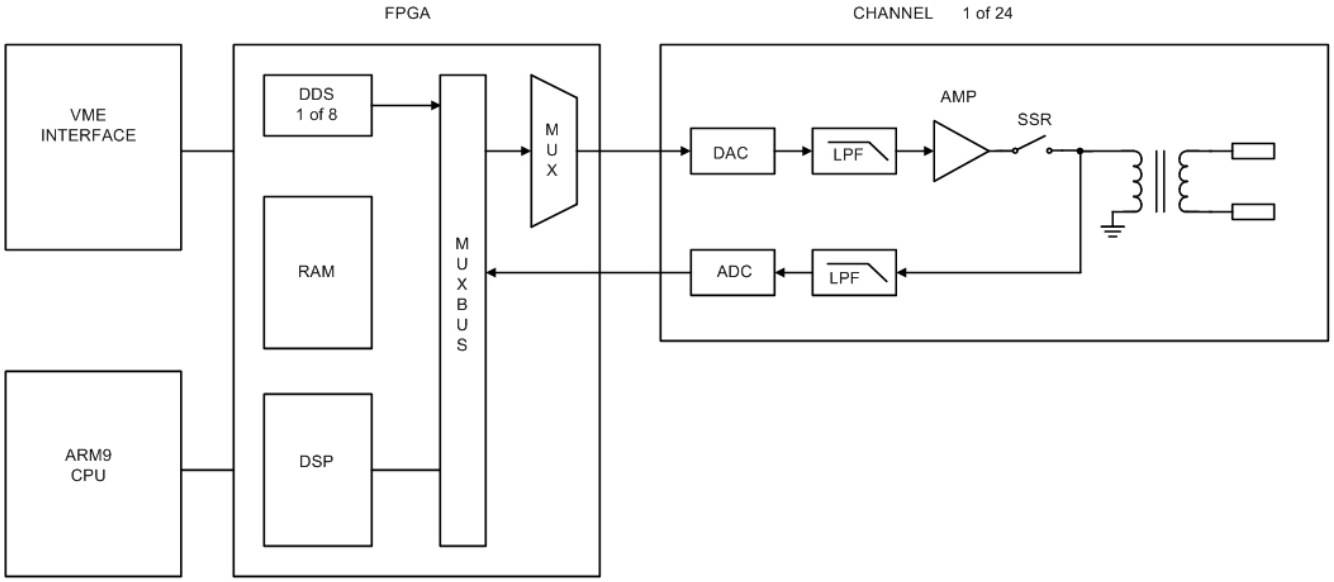
2. Specifications: V545 LVDT/Synchro Simulation Module

FUNCTION	24-channel LVDT/synchro simulator
DEVICE TYPE	16-bit VME register-based slave: A24:A16:D16; Implements 1024 16-bit registers at switch selectable addresses in the VME 16 or 24 bit addressing spaces
I/O CHANNELS	24, transformer isolated, programmable input/output Nominal 100 ohm output impedance with 1:1 transformers
RANGES	± 10.24 volts peak using 1:1 transformers ± 54.27 volts peak using 5.3:1 transformers
RESOLUTION	16 bits
SAMPLE RATE	250 ksps/channel
FREQUENCY RANGE	250 Hz to 20 KHz
OPERATING TEMPERATURE	0 to 60°C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	Two years
POWER	Standard VME supplies: + 5 volts, 500 mA max +12 volts, 2 A max -12 volts, 2 A max
CONNECTORS	Two female D25 connectors, one female D9 connector
INDICATORS	LEDs indicate VME access, CPU activity, error conditions Additional LED is user programmable
PACKAGING	6U single-wide VME module

ACCURACY	
VOLTAGE GENERATION	± 0.50% full scale at 300 Hz to 500 Hz
RMS VOLTAGE MEASUREMENT	±1% full scale at 300 Hz to 500 Hz
FREQUENCY MEASUREMENT	0.05%
FREQUENCY GENERATION	0.05%
SYNCHRO/ RESOLVER ACQUISITION	±0.2 degrees at 300 Hz to 500 Hz, with dash-6 transformers
SYNCHRO/ RESOLVER SIMULATION	±0.2 degrees at 300 Hz to 500 Hz, with dash-6 transformers.
LOGIC I/O	
INPUTS	Four TTL/CMOS/contact inputs on D9 connector Pullup 1k-Ohm to 3.3V 0/5V Max
OUTPUTS	Two open-drain outputs on D9 connector 100mA / 24V / 0.35W max
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec; does not support byte writes

3. Overview

The basic block diagram of the V545 is shown below.



The user interface is presented in 1024 VME registers, in six major groups:

Module overhead and supervision registers

Eight DDS sine wave signal generators. These are the signal sources for optional internal excitation of LVDT and synchro type devices.

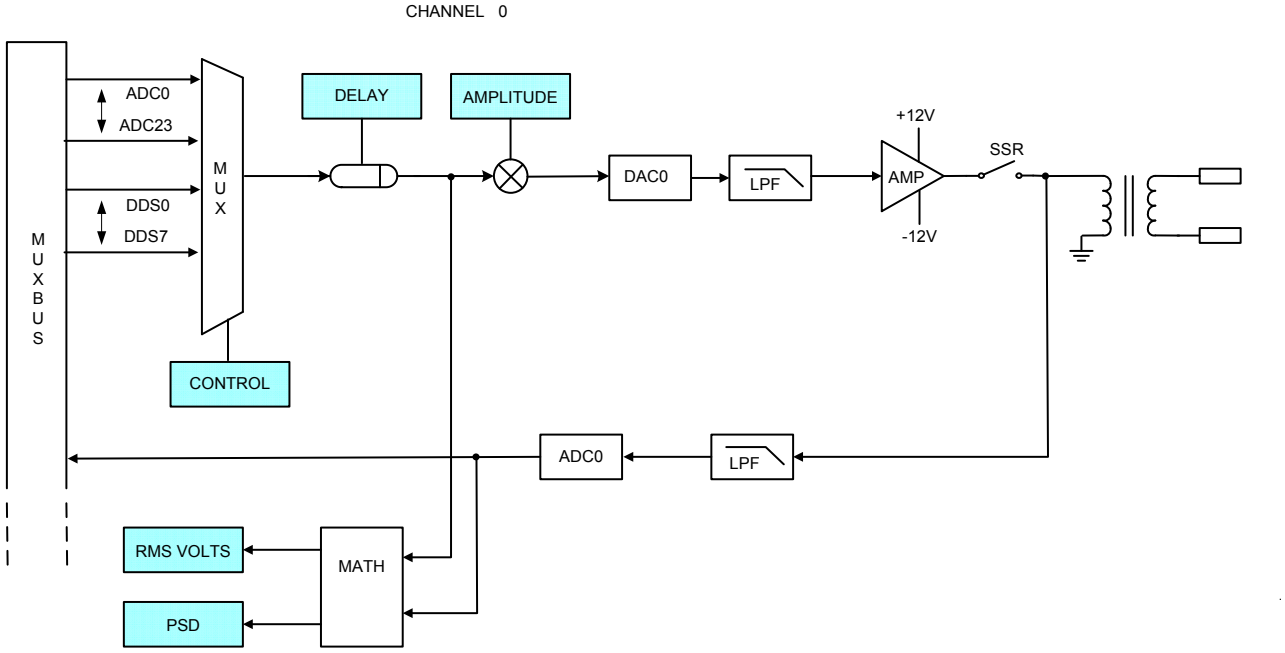
Twenty-four channel interface blocks for the transformer-isolated I/O channels. Each block can be programmed as an output or as an input.

Twelve Function Blocks which do higher-level operations using multiple I/O channels

Four Override Blocks which can sense switches or watchdog timeouts

A 64-word register file for use with Override Blocks and macros

The configuration of a typical I/O channel, channel 0, logic is shown in detail below:



The shaded blocks depict VME registers. The CONTROL register selects which bus signal drives the channel DAC, controls the SSR, and sets filtering and other options.

The DELAY register allows phase shift to be added in the signal path, to simulate real-world electrical phase shifts. The AMPLITUDE registers scales the DAC data over the range of +1 to -1.

The MATH block computes the true RMS voltage based on ADC samples, and reports it in the RMS register. A phase-sensitive detector and filter are provided, with results reported in the PSD register.

Each of the 24 channels can be programmed to be an input or an output.

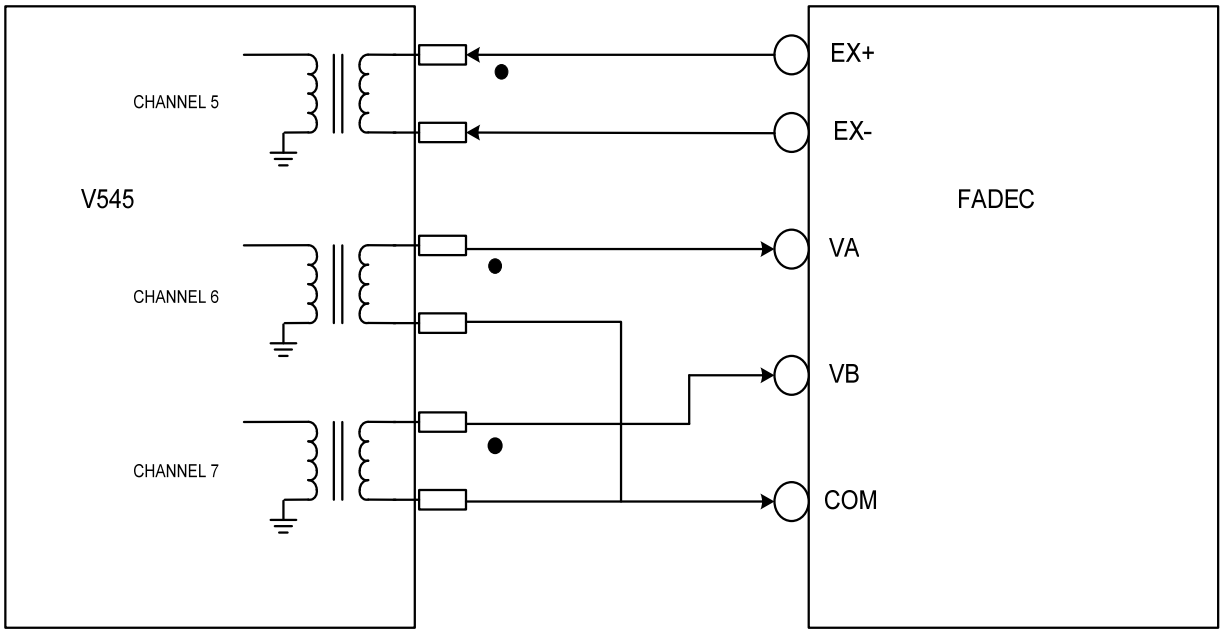
As an input, with the SSR open, the ADC digitizes the signal applied from the field into the connector side of the transformer. This could be an external excitation supply, or an output winding from an LVDT or synchro. The sampled ADC data is presented to the data bus, available as a resource for other channels, and is available for computation. The computed RMS voltage and PSD phase detector outputs are also available. The channel MUX output, optionally delayed, is used as the phase-sensitive detector reference.

As an output, the SSR is closed, allowing the DAC and amplifier to drive the transformer and an external load. The channel multiplexer selects the signal source to drive this channel's DAC. Available MUXBUS sources include all 24 channel ADCs and any of the eight DDS sinewave generators.

Both the ADC and DAC are clocked at 250 KHz. If one channel acquires a sine wave from an external source, and that data is piped to the DAC of another channel, the nominal transport delay is 8 microseconds. The ADC and DAC anti-aliasing filters are designed to process sine waves up to 20 KHz.

The basic channel architecture is directly accessible through the 24 Channel Control Blocks of registers. The V545 also provides twelve Function Blocks which can each use multiple lower-level Channel Blocks to perform complex LVDT and synchro/resolver functions; the Function Blocks are essentially one level of abstraction above the individual Channel Control Blocks.

A basic application example is simulation of a 5-wire, externally excited LVDT to a FADEC engine-control computer. The FADEC provides 2-wire sinewave excitation at 4 volts RMS and 5 KHz, and expects to receive a 3-wire signal from an LVDT secondary. The setup might look like the following:



Channel 5 of the V545 is programmed as an input, and digitizes the excitation signal generated by the FADEC. Channels 6 and 7 are programmed as outputs, with both data-select multiplexers programmed to select the data from channel 5. The amplitude registers of channels 6 and 7 can be loaded to simulate the outputs of an LVDT. The delay function of channels 6 and 7 could be used to simulate phase shift associated with cable capacitance loading of the LVDT.

4. Connectors and Installation

4.1 Address DIP Switches

The V545 appears as 1024 16-bit registers in the VME 16 or 24-bit addressing spaces. The base address of the module registers is set by dip switches.

Two rocker-type dip switches are provided near the center right corner of the board. They are labeled, top to bottom, "23" through "11", then X, Y, and finally "A".

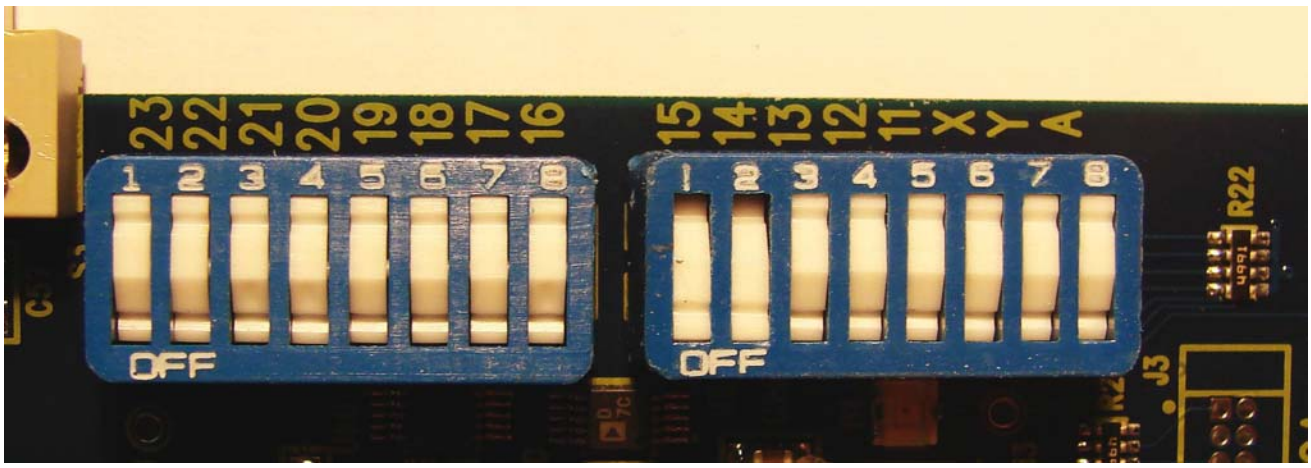
To set a switch to the logical "1" or "ON" position, press the side of the switch nearest its lettering. Use a toothpick or paper clip, not a pen or pencil.

The numbered switches represent address bits A23-A11 respectively.

The A switch, when set, allows the board to operate in the VME 24-bit (A24) address space; in this case, all address switches are active and the board responds to VME address modifier codes 0x39 and 0x3D.

If the A switch is off, the module resides in the A16 space and responds to address modifiers 0x29 and 0x2D. In this case, only address switches A15 through A11 are active. The X and Y switches are currently unused.

Units are shipped with switches A15 and A14 on, all others off, setting the register base to 0xC000 in the A16 space, as shown below.



4.2 Installation

The V545 may be installed in any standard 6U VME crate, including VME64 variants. It supports 16-bit data transfers using the P1 connector.

The V545 passes all interrupt and bus grant signals, and may be used with backplane grant jumpers installed or not installed.



CAUTION: Do not install or remove the V545 with crate power on. VME modules are not hot-pluggable. The V545 will be damaged if hot-plugged.



CAUTION: Fully seat the module and secure front-panel screws before applying power.



CAUTION: Handle the V545 with proper ESD precautions to avoid static damage.



CAUTION: V545 channels are transformer coupled. Do not apply DC voltages, or apply AC voltages to channels programmed to be outputs.

4.3 Front-Panel D25 Connectors

Two front-panel female D-25 connectors are provided. Pinout is as follows:

J1 Pin	Function	J2 Pin	Function
J1-1	ch 0+	J2-1	ch 12+
J1-14	ch 0-	J2-14	ch 12-
J1-2	ch 1+	J2-2	ch 13+
J1-15	ch 1-	J2-15	ch 13-
J1-3	ch 2+	J2-3	ch 14+
J1-16	ch 2-	J2-16	ch 14-
J1-4	ch 3+	J2-4	ch 15+
J1-17	ch 3-	J2-17	ch 15-
J1-5	ch 4+	J2-5	ch 16+
J1-18	ch 4-	J2-18	ch 16-
J1-6	ch 5+	J2-6	ch 17+
J1-19	ch 5-	J2-19	ch 17-
J1-7	ch 6+	J2-7	ch 18+
J1-20	ch 6-	J2-20	ch 18-
J1-8	ch 7+	J2-8	ch 19+
J1-21	ch 7-	J2-21	ch 19-
J1-9	ch 8+	J2-9	ch 20+
J1-22	ch 8-	J2-22	ch 20-
J1-10	ch 9+	J2-10	ch 21+

J1 Pin	Function	J2 Pin	Function
J1-23	ch 9-	J2-23	ch 21-
J1-11	ch 10+	J2-11	ch 22+
J1-24	ch 10-	J2-24	ch 22-
J1-12	ch 11+	J2-12	ch 23+
J1-25	ch 11-	J2-25	ch 23-
J1-13	VME GROUND	J2-13	VME GROUND

Connector shells are bonded to the VME front panel, which connects to the crate frame through the module securing screws.

On V545 revision C and above, a switch closure connector J3 is provided. This is a female D9. Pinout is:

J3-1	GROUND	VME GROUND
J3-2	SWIN0	INPUT
J3-3	SWIN1	INPUT
J3-4	SWIN2	INPUT
J3-5	SWIN3	INPUT
J3-6	SWOUT0	OUTPUT
J3-7	SWOUT1	OUTPUT
J3-8	NC	NOT CONNECTED
J3-9	GROUND	VME GROUND

The SWIN input pins are normally switch closures to ground or TTL inputs referenced to ground; each has a 1K pull-up to +3.3 volts. Their levels are readable in the SWIN register and may be used by Override Blocks to gate override functions.

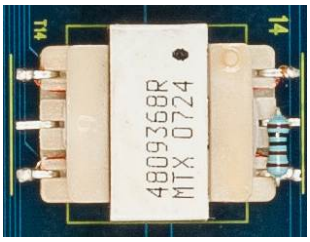
The SWOUT pins are open-collector outputs, controlled by the SWOUT register.

4.4 Transformer Types

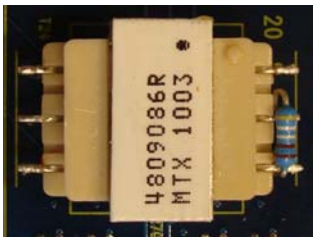
Each of the 24 I/O channels has a plugin coupling transformer. Transformer types are sensed and reported in the channel **STS** registers. Available transformers are:

Model	Ratio	max volts p-p	max volts RMS	Z out nom	STSn ID code
V548-1	1.00	20.48	7.241	100 ohms	1
V548-6	5.30	108.54	43.44	1.5K ohms	6

The V548-1 is commonly used with LVDTs, and V548-6 is generally used for 400 Hz synchros.



Type 1 V548-1



Type 5 V548-6

"Z out" in the table above is the approximate signal source impedance when a channel is programmed to be an output. Transformer outputs generally have adequate drive to simulate LVDT and synchro/resolver signals to electronic controls but may require external amplification to drive the reference windings of physical synchro type devices.

The V545-1 is furnished with 24 type 1 transformers suitable for LVDT acquisition and simulation.

The V545-6 is furnished with 24 type 6 transformers suitable for acquisition and simulation of 26-volt 400Hz synchros and resolvers.

5. Operation

5.1 LEDs

There are four front-panel LED indicators.

The blue VME led flashes whenever the module is accessed from the VME bus.

The green CPU led flashes about once a second to indicate CPU activity

The red ERR led will flash to indicate errors:

Red LED Pattern	Error
One blink	Upgrade application exists, but checksum failed. Factory application is running instead.
Two blinks	Calibration table error. Default calibrations are in use.
Three blinks	Power supply error.
Four blinks	FPGA error. Module may not respond to the VME bus
One-second toggle	Failure to boot application.

The orange USR led displays a user-defined blink pattern. See section 7.3.

There is an additional LED on the PCB surface which illuminates green when the FPGA is properly configured.

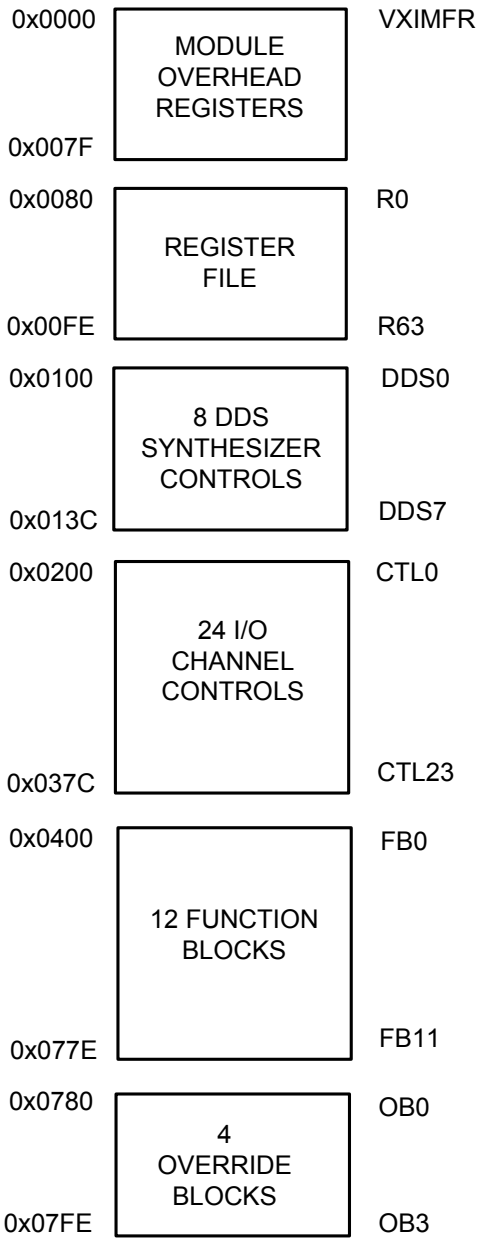
6. VME Registers

The V545 implements 1024 16-bit VME registers. OFFSET is the hex VMEbus offset from the module base address.

Registers identified as "RO" should be treated as read-only and should not be written from VME; these registers are periodically refreshed by the internal microprocessor.

Read-write (RW) registers are written and read back by VME and, after powerup initialization, are not altered by the internal microprocessor.

The overall register map is:



6.1 VME Register Map

Reg Name	Offset	R/W	Function
Module Control and Status Registers			
VXI MFR	0x000	RO	Highland ID: reads 65262, 0xFEEE
VXI TYPE	0x002	RO	V545 module ID, 22545
SERIAL	0x006	RO	unit serial number
ROM ID	0x008	RO	firmware ID, typically 22545 decimal
ROM REV	0x00A	RO	firmware revision, typically ASCII "B"
MCOUNT	0x00C	RO	microprocessor IRQ counter
DASH	0x00E	RO	module version (dash) number
STATE	0x014	RO	module state
ULED	0x016	RW	user LED control
BISS	0x018	RO	BIST status register
CALID	0x01A	RO	calibration table status
YCAL	0x01C	RO	calibration date: year
DCAL	0x01E	RO	calibration date: month/day
SWIN	0x020	RO	J3 D9 input state
SWOUT	0x022	RW	J3 D9 output state
MACRO	0x030	RW	macro command register
PARAM0	0x032	RW	macro parameter
PARAM1	0x034	RW	macro parameter
PARAM2	0x036	RW	macro parameter
R0	0x080	RW	64-word register file
R1	0x082	RW	
	...		
R63	0x0FE	RW	

Reg Name	Offset	R/W	Function
DDS Synthesizer Control Blocks			
DFR0	0x100	RW	DDS source 0 frequency
DPH0	0x102	RW	DDS source 0 phase
DAM0	0x104	RW	DDS source 0 amplitude
DFR1	0x108	RW	DDS source 1 frequency
DPH1	0x10A	RW	DDS source 1 phase
DAM1	0x10C	RW	DDS source 1 amplitude
DFR2	0x110	RW	DDS source 2 frequency
DPH2	0x112	RW	DDS source 2 phase
DAM2	0x114	RW	DDS source 2 amplitude
DFR3	0x118	RW	DDS source 3 frequency
DPH3	0x11A	RW	DDS source 3 phase
DAM3	0x11C	RW	DDS source 3 amplitude
DFR4	0x120	RW	DDS source 4 frequency
DPH4	0x122	RW	DDS source 4 phase
DAM4	0x124	RW	DDS source 4 amplitude
DFR5	0x128	RW	DDS source 5 frequency
DPH5	0x12A	RW	DDS source 5 phase
DAM5	0x12C	RW	DDS source 5 amplitude
DFR6	0x130	RW	DDS source 6 frequency
DPH6	0x132	RW	DDS source 6 phase
DAM6	0x134	RW	DDS source 6 amplitude
DFR7	0x138	RO	DDS source 7 frequency fixed 400 Hz
DPH7	0x13A	RO	DDS source 7 phase fixed 0
DAM7	0x13C	RO	DDS source 7 amplitude fixed max

Reg Name	Offset	R/W	Function
I/O Channel Control Blocks			
CTL0	0x200	RW	channel 0 control
STS0	0x202	RO	channel status
AMP0	0x204	RW	channel amplitude
DLY0	0x206	RW	channel delay
RMS0	0x208	RO	channel RMS voltage
PSD0	0x20A	RO	channel phase-sensitive detector
FRQ0	0x20C	RO	channel signal frequency
CTL1	0x210	RW	channel 1 control
STS1	0x212	RO	channel status
AMP1	0x214	RW	channel amplitude
DLY1	0x216	RW	channel delay
RMS1	0x218	RO	channel RMS voltage
PSD1	0x21A	RO	channel phase-sensitive detector
FRQ1	0x21C	RO	channel signal frequency
CTL2	0x220	RW	channel 2 control
STS2	0x222	RO	channel status
AMP2	0x224	RW	channel amplitude
DLY2	0x226	RW	channel delay
RMS2	0x228	RO	channel RMS voltage
PSD2	0x22A	RO	channel phase-sensitive detector
FRQ2	0x22C	RO	channel signal frequency
CTL3	0x230	RW	channel 3 control
STS3	0x232	RO	channel status
AMP3	0x234	RW	channel amplitude
DLY3	0x236	RW	channel delay
RMS3	0x238	RO	channel RMS voltage
PSD3	0x23A	RO	channel phase-sensitive detector
FRQ3	0x23C	RO	channel signal frequency

Reg Name	Offset	R/W	Function
CTL4	0x240	RW	channel 4 control
STS4	0x242	RO	channel status
AMP4	0x244	RW	channel amplitude
DLY4	0x246	RW	channel delay
RMS4	0x248	RO	channel RMS voltage
PSD4	0x24A	RO	channel phase-sensitive detector
FRQ4	0x24C	RO	channel signal frequency
CTL5	0x250	RW	channel 5 control
STS5	0x252	RO	channel status
AMP5	0x254	RW	channel amplitude
DLY5	0x256	RW	channel delay
RMS5	0x258	RO	channel RMS voltage
PSD5	0x25A	RO	channel phase-sensitive detector
FRQ5	0x25C	RO	channel signal frequency
CTL6	0x260	RW	channel 6 control
STS6	0x262	RO	channel status
AMP6	0x264	RW	channel amplitude
DLY6	0x266	RW	channel delay
RMS6	0x268	RO	channel RMS voltage
PSD6	0x26A	RO	channel phase-sensitive detector
FRQ6	0x26C	RO	channel signal frequency
CTL7	0x270	RW	channel 7 control
STS7	0x272	RO	channel status
AMP7	0x274	RW	channel amplitude
DLY7	0x276	RW	channel delay
RMS7	0x278	RO	channel RMS voltage
PSD7	0x27A	RO	channel phase-sensitive detector
FRQ7	0x27C	RO	channel signal frequency
CTL8	0x280	RW	channel 8 control

Reg Name	Offset	R/W	Function
STS8	0x282	RO	channel status
AMP8	0x284	RW	channel amplitude
DLY8	0x286	RW	channel delay
RMS8	0x288	RO	channel RMS voltage
PSD8	0x28A	RO	channel phase-sensitive detector
FRQ8	0x28C	RO	channel signal frequency
CTL9	0x290	RW	channel 9 control
STS9	0x292	RO	channel status
AMP9	0x294	RW	channel amplitude
DLY9	0x296	RW	channel delay
RMS9	0x298	RO	channel RMS voltage
PSD9	0x29A	RO	channel phase-sensitive detector
FRQ9	0x29C	RO	channel signal frequency
CTL10	0x2A0	RW	channel 10 control
STS10	0x2A2	RO	channel status
AMP10	0x2A4	RW	channel amplitude
DLY10	0x2A6	RW	channel delay
RMS10	0x2A8	RO	channel RMS voltage
PSD10	0x2AA	RO	channel phase-sensitive detector
FRQ10	0x2AC	RO	channel signal frequency
CTL11	0x2B0	RW	channel 11 control
STS11	0x2B2	RO	channel status
AMP11	0x2B4	RW	channel amplitude
DLY11	0x2B6	RW	channel delay
RMS11	0x2B8	RO	channel RMS voltage
PSD11	0x2BA	RO	channel phase-sensitive detector
FRQ11	0x2BC	RO	channel signal frequency
CTL12	0x2C0	RW	channel 12 control
STS12	0x2C2	RO	channel status

Reg Name	Offset	R/W	Function
AMP12	0x2C4	RW	channel amplitude
DLY12	0x2C6	RW	channel delay
RMS12	0x2C8	RO	channel RMS voltage
PSD12	0x2CA	RO	channel phase-sensitive detector
FRQ12	0x2CC	RO	channel signal frequency
CTL13	0x2D0	RW	channel 13 control
STS13	0x2D2	RO	channel status
AMP13	0x2D4	RW	channel amplitude
DLY13	0x2D6	RW	channel delay
RMS13	0x2D8	RO	channel RMS voltage
PSD13	0x2DA	RO	channel phase-sensitive detector
FRQ13	0x2DC	RO	channel signal frequency
CTL14	0x2E0	RW	channel 14 control
STS14	0x2E2	RO	channel status
AMP14	0x2E4	RW	channel amplitude
DLY14	0x2E6	RW	channel delay
RMS14	0x2E8	RO	channel RMS voltage
PSD14	0x2EA	RO	channel phase-sensitive detector
FRQ14	0x2EC	RO	channel signal frequency
CTL15	0x2F0	RW	channel 15 control
STS15	0x2F2	RO	channel status
AMP15	0x2F4	RW	channel amplitude
DLY15	0x2F6	RW	channel delay
RMS15	0x2F8	RO	channel RMS voltage
PSD15	0x2FA	RO	channel phase-sensitive detector
FRQ15	0x2FC	RO	channel signal frequency
CTL16	0x300	RW	channel 16 control
STS16	0x302	RO	channel status
AMP16	0x304	RW	channel amplitude

Reg Name	Offset	R/W	Function
DLY16	0x306	RW	channel delay
RMS16	0x308	RO	channel RMS voltage
PSD16	0x30A	RO	channel phase-sensitive detector
FRQ16	0x30C	RO	channel signal frequency
CTL17	0x310	RW	channel 17 control
STS17	0x312	RO	channel status
AMP17	0x314	RW	channel amplitude
DLY17	0x316	RW	channel delay
RMS17	0x318	RO	channel RMS voltage
PSD17	0x31A	RO	channel phase-sensitive detector
FRQ17	0x31C	RO	channel signal frequency
CTL18	0x320	RW	channel 18 control
STS18	0x322	RO	channel status
AMP18	0x324	RW	channel amplitude
DLY18	0x326	RW	channel delay
RMS18	0x328	RO	channel RMS voltage
PSD18	0x32A	RO	channel phase-sensitive detector
FRQ18	0x32C	RO	channel signal frequency
CTL19	0x330	RW	channel 19 control
STS19	0x332	RO	channel status
AMP19	0x334	RW	channel amplitude
DLY19	0x336	RW	channel delay
RMS19	0x338	RO	channel RMS voltage
PSD19	0x33A	RO	channel phase-sensitive detector
FRQ19	0x33C	RO	channel signal frequency
CTL20	0x340	RW	channel 20 control
STS20	0x342	RO	channel status
AMP20	0x344	RW	channel amplitude
DLY20	0x346	RW	channel delay

Reg Name	Offset	R/W	Function
RMS20	0x348	RO	channel RMS voltage
PSD20	0x34A	RO	channel phase-sensitive detector
FRQ20	0x34C	RO	channel signal frequency
CTL21	0x350	RW	channel 21 control
STS21	0x352	RO	channel status
AMP21	0x354	RW	channel amplitude
DLY21	0x356	RW	channel delay
RMS21	0x358	RO	channel RMS voltage
PSD21	0x35A	RO	channel phase-sensitive detector
FRQ21	0x35C	RO	channel signal frequency
CTL22	0x360	RW	channel 22 control
STS22	0x362	RO	channel status
AMP22	0x364	RW	channel amplitude
DLY22	0x366	RW	channel delay
RMS22	0x368	RO	channel RMS voltage
PSD22	0x36A	RO	channel phase-sensitive detector
FRQ22	0x36C	RO	channel signal frequency
CTL23	0x370	RW	channel 23 control
STS23	0x372	RO	channel status
AMP23	0x374	RW	channel amplitude
DLY23	0x376	RW	channel delay
RMS23	0x378	RO	channel RMS voltage
PSD23	0x37A	RO	channel phase-sensitive detector
FRQ23	0x37C	RO	channel signal frequency
Function Blocks			
FB0	0x400	RW	function block 0 32 words
...	**...**		
FB1	0x440	RW	function block 1
...	**...**		

Reg Name	Offset	R/W	Function
FB2	0x480	RW	Function Block 2
...	...		
FB3	0x4C0	RW	Function Block 3
...	...		
FB4	0x500	RW	Function Block 4
...	...		
FB5	0x540	RW	Function Block 5
...	...		
FB6	0x580	RW	Function Block 6
...	...		
FB7	0x5C0	RW	Function Block 7
...	...		
FB8	0x600	RW	Function Block 8
...	...		
FB9	0x640	RW	Function Block 9
...	...		
FB10	0x680	RW	Function Block 10
...	...		
FB11	0x6C0	RW	Function Block 11
...	...		
Override Blocks			
OB12	0x700	RW	Override Block 12 32 words
...	...		
OB13	0x740	RW	Override Block 13
...	...		
OB14	0x780	RW	Override Block 14
...	...		
OB15	0x7C0	RW	Override Block 15
...	...		

7. Detailed Register Descriptions

7.1 Module ID Registers (RO)

A number of read-only overhead registers are provided.

VXI MFR always reads 0xFEEE, Highland's registered VXI module ID code

VXITYPE always reads 22545 decimal to identify a V545 module

MODREV module hardware revision number, typically 0x0045, ASCII “E”.

SERIAL module serial number

DASH module version (dash) number, 1 for the standard V545-1

ROM ID firmware version, typically 22545 decimal

ROM REV Bits 7-0 are an ASCII code identifying the revision letter of the firmware. Bits 15-8 are a binary draft number, or zero for final release versions.

MCOUNT a 16-bit counter that is incremented by the internal microprocessor at about 1 KHz

7.2 Module State Register (RO)

STATE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						RF	FF			K1	K0				

The onboard flash memory contains a boot loader, a factory-installed firmware image, and storage for a field-reflashed upgrade firmware image. The encoded K bits indicate which code is currently running:

1 factory operating firmware

2 upgrade firmware

If the FF bit is set, a valid factory code image is available in flash memory. If RF is set, a valid upgrade image is available.

Macros are provided to manage the primary or upgrade firmware images.

7.3 ULED - User LED Control (RW)

An orange LED is provided on the front panel for user application. The ULED register allows user flash patterns to be loaded. An internal shift register is periodically loaded from the contents of the ULED register, and the MS bit of this register operates the orange LED. The shift register is left-shifted every 125 milliseconds, and the register is reloaded every 16 shifts, namely every 2 seconds.

ULED pattern 0x0000 turns the user LED off. Pattern 0xFFFF turns it steady on.

7.4 CALID, YCAL, DCAL - Calibration Status Registers (RO)

The CALID register displays a value which reflects the currently installed calibration table. The normal value is 22545 decimal. If the factory calibration table is corrupted, the firmware will install the default calibration table, the CALID register will display value 0xDEFC and the red LED will flash two times every few seconds..

YCAL and DCAL display the last date of module calibration. YCAL is the year, as an integer, such as 2012 decimal. The high byte of DCAL (bits 15..8) is month 1-12, and the low byte (bits 7..0) is day 1-31.

7.5 D9 Connector Switch Closure Registers

SWIN (RO)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
												SWIN3	SWIN2	SWIN1	SWIN0

The SWIN register displays the state of the inputs on the D9 switch closure. ‘1’ represents a TTL high state and ‘0’ represents a closed or TTL low state. The contents of this register are undefined for V545 modules with hardware revision “B” or earlier.

SWOUT (RW)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
														SWOUT1	SWOUT0

The SWOUT register controls the open-collector outputs on the D9 switch closure. ‘1’ pulls and output low and ‘0’ causes high impedance output. The default state of this register is 0x0000. If the module’s hardware revision is “B” or earlier, writes to this register have no effect.

7.6 BISS Register (RO)

Eight signals are read by the on-board processor for self-test. The BISS register reports a bitmask of these signals. A bit value of '1' means that the signal is out of tolerance. Bits 8 to 15 are unused.

Bit	Signal
0	DAC reference
1	+2.5V Power
2	+3.3V Power
3	VMID – ADC "COM" input
4	VAMP – ADC Reference
5	+1.2V Power
6	Ground
7	+3V analog reference

These can be checked with the macro to read power supplies. See section 8.

7.7 MACRO, PARAMx - Macro Controls (RW)

The macro control register allows the execution of microprocessor routines which perform calibration and test tasks. Some macros also take or return parameters in the PARAM registers.

To execute a macro, verify that the MS bit (bit 15) of the MACRO register is clear, then write any required parameters and then write a macro code to the MACRO register. Wait until the MS bit of MACRO self-clears. See section 8. , "Macros and Program Management".

7.8 DDS Frequency Synthesizer Registers (RW)

There are eight Direct Digital Synthesizer (DDS) control blocks. Each generates a sinewave data stream which is applied to the MUXBUS, and is available to all channels. The generators are called DDS0 through DDS7, and each has a block of registers.

DDS0 through DDS6 are programmable. The DDS7 generator is fixed to operate at 400 Hz and maximum amplitude. It is the default source for basic synchro functions. All DDS7 registers are read-only.

The DFRn register sets the DDS frequency; the LSB is 0.5 Hz. The maximum recommended value is 40000, equivalent to 20 KHz.

The DPHn register shifts the phase of the synthesizer. This value is meaningful only if it is coordinated with the phases of other DDS blocks. They are synchronized using the Reset Macro (see section 8). Values 0...65535 correspond to 0 through 359.994 degrees lead.

The DAMn register is an unsigned fractional that scales the amplitude of the synthesized sinewave. Its powerup default value is 0xFFFF, which means that it normally generates a "full amplitude" sinewave, effectively ±10.24 volts peak as seen by an output channel DAC.

7.9 Channel Registers

Each of the 24 I/O channels has a block of 16-bit registers. They are:

CTLn (RW) Channel Control
STSn (RO) Channel Status
DLYn (RW) Channel Delay
AMPn (RW) Channel DAC Amplitude
RMSn (RO) Channel RMS Voltage
PSDn (RO) Channel Phase-Sensitive Detector Voltage
FRQn (RO) Measured signal frequency

Users can perform flexible, fundamental analog signal acquisition and output by programming individual channels and groups of channels. Function Blocks can also be used to abstract common LVDT and synchro/resolver operations; see section 11.

7.9.1 Channel Control Registers (RW)

Each of the 24 I/O channels has a read-write channel control register, CTL0 through CTL23.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	M6	M5	M4	M3	M2	M1	M0		2X	F2	F1	F0		DL	SSR

The SSR bit, when set, enables the solid-state relay to connect the channel's post-DAC amplifier to the output transformer. This makes the channel an output. Before changing a channel from an output to an input, make sure its AMP register is zero.

The DL bit controls the phase reference used by the phase-sensitive detector. If DL is zero, the detector will use the undelayed MSB of the mux data as the phase reference. If DL is set, the delayed version will be used.

The “F” bits set the period over which the channel’s phase-sensitive detector averages data, as a number of cycles of the reference signal.

F	Cycles		F	Cycles
0	1		4	256
1	4		5	1,024
2	16		6	4,096
3	64		7	16,384

See section 7.9.6 for discussion of the PSD.

If the "2X" bit is set on an output channel, the gain of the channel DAC is doubled.

If an input ADC channel is programmed to drive an output channel, and if the output channel 2X bit is low, and the output channel has its AMPn register set to max, the electrical voltage gain from input to output will be 1.00. Some LVDTs have secondary output voltages that are greater than the excitation winding inputs (ie, step-up ratios) so these require gain above 1, as supported by the 2X bit. Channel outputs are still limited to ± 10.24 volts peak swing, so high gain cannot be used with high ADC channel inputs. Optional step-up transformers are available if higher output voltages are needed.

The "M" bits drive the DAC multiplexer to select the MUXBUS source to drive this channel's DAC and phase-sensitive detector. Selections are:

M	**DAC/PSD Source**
0...23	ADC data from I/O channels 0 through 23
24-31	DDS frequency synthesizers 0 through 7
32-up	reserved

7.9.2 Channel Status Registers (RO)

Each of the 24 channels has a read-only status register, STS0 through STS23.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CL												X3	X2	X1	X0

The CL bit indicates that the ADC has clipped at least once in the last second, suggesting that the peak input amplitude is too high, or that the signal has noise spikes.

The "X" nibble identifies the type of transformer installed in this channel.

X value	**Transformer**	**Ratio**	**Notes**
0	none		
1	V548-1	1.00	typically for LVDTs
2	V546-1	1.00	special
6	V548-6	5.30	typically for synchros/resolvers

7.9.3 Channel Delay Registers (RW)

Each of the 24 input channels has a writable channel delay register, DLY0 through DLY23. The low 9 bits specify a time delay in units of 4 microseconds, with a range of 0 to 2.044 milliseconds. This allows phase shift to be added to the DAC data path. Note that inverting the sinewave amplitude can effectively add 180 degrees, doubling the potential delay range.

7.9.4 Channel Amplitude Registers (RW)

Each of the 24 input channels has a writable channel amplitude register, AMP0 through AMP23. Data from the channel multiplexer and delay line are scaled by this register.

The relationship is:

AMPn Hex	AMPn Decimal	Scaler
0x7FFF	+32767	+ 0.999969
0x0000	0	0
0x8000	-32768	-1.000000

For example, channel 5 might be an input, with its SSR bit off. It would be connected to an external sinewave generator which is also being used to excite a number of LVDTs. Suppose this external voltage level is 4 volts RMS.

Channels 6 and 7 could both be programmed to be outputs, with their SSR bits set. Both would have their "M" bits set to 5, so both are getting data from the reference sine wave.

If AMP6 and AMP7 are both set to 0x4000 (16384 decimal, 0.5 fractional) then both channels will output 2.0 volts RMS, in phase with the excitation, which might simulate an LVDT at nominal center position. To simulate an off-center position, AMP6 could be increased and AMP7 decreased by equal amounts.

Negative values of AMP6 or AMP7 would electrically invert the phase of the sinewave outputs relative to the channel 5 excitation input.

Setting the 2X bit in a channel's CTLn register doubles its output voltage, which is still electrically limited to ± 10.24 volts peak.

If an output channel is set up to select a sine wave source from an internal DDS generator (M codes 24 through 31) then the AMPn register scales the transformer output signal. If AMPn is set to 32767, the full DDS amplitude is used, 10.24 volts peak, or 7.241 volts RMS. AMPn of -32768 produces the same 10.24 volts peak sinewave, but phase inverted.

If the DDS source is set to less than the default full-scale amplitude, the actual peak voltage output will be

$$Vpeak = G * 10.24 * (DAMn / 65536) * (AMPn / 32768)$$

where DAMn is an unsigned integer and AMPn is a signed integer. *G* is 1.00 if the channel control register 2X bit is low, and 2.00 if 2X is high. Vpeak is electrically limited to slightly over ± 10.24 volts peak.

7.9.5 Channel RMS Voltage Registers (RO)

Each of the 24 input channels has a read-only RMS voltage register. When the channel is programmed as an input, the value in its RMSn register will be nominally 0 with no input voltage, and is calibrated at 1 KHz to report 23,170 when the transformer input, at the D25 connector, is 10.24 volts peak, or 7.241 volts RMS. This corresponds to 3200 codes/V RMS.

Transformer		**RMS Scaling**	
V548-1	1.0:1	0.3125mV/LSB	16,000 at 5 volts RMS
V548-6	5.3:1	1.875mV/LSB	16,000 at 26.5 volts RMS

If a channel is programmed to be an output, the RMSn value nominally reflects the voltage that will appear at the channel's D25 connector pins, with some error caused by transformer loadings.

7.9.6 Channel Phase-Sensitive Detector Register (RO)

Each of the 24 input channels has a phase-sensitive detector and a corresponding read-only PSDn voltage register. The PSD function is used on channels that are programmed to be inputs, and the channel's DAC multiplexer is used to select the phase reference.

The voltage scaling is +32767 for +10.24 volts peak (7.241 volts RMS) and -32768 for -10.24 volts, where a minus value corresponds to the signal and reference being out of phase.

The channel ADC samples are multiplied by the MSB of the channel MUX output, namely the sign of the usual DAC data stream. The product of ADC samples and the ±1-valued MSB is averaged over a programmable number of cycles of the phase reference, as noted in section 7.8.1. The result is presented in the PSDn register. This allows any input channel to be used as a phase-sensitive detector, with the phase reference being any other input channel or any DDS synthesizer. The reference signal selected by the channel DAC MUX setting should be the equivalent of at least 0.5 volts RMS for proper PSD operation.

Users can select a low number of averaged cycles for fast response, or a larger number for lower noise. It is suggested that the number of cycles, as programmed in the channel's CTLn register, result in an integration time of at least 2 milliseconds, corresponding to averaging at least 500 ADC samples.

If the DL bit is low in CTLn, the phase-sensitive detector will use the undelayed MSB from the DAC-select MUX. If DL is set, the delayed phase reference will be used.

7.9.7 Channel Frequency Measurement Register (RO)

Each of the 24 input channels has a frequency measurement register FRQn. It measures signal zero crossings for channels operating as inputs or outputs. The value is updated

once per second, and the LSB is 0.5 Hz. A signal of at least 10% of the channel's full range is required for reliable frequency measurement.

8. Macros and Program Management

The macro control register allows invocation of microprocessor service routines. Some macros take or return data in the PARAM0 through PARAM2 registers. Values not listed in the sections below are reserved for HTI calibration/maintenance and should not be used.

To execute a macro:

Verify that the MS bit (bit 15) of the MACRO register is clear, indicating that the microprocessor is ready to accept a command.

Write any required macro parameters.

Write a 16-bit macro code to the MACRO register.

Wait until the MS bit again clears. If any other bits are then set in MACRO, an error has occurred.

Read any returned parameters.

If the MS bit of the MACRO register clears but the MACRO register does not equal zero, an error has occurred. This may have been caused by an execution error (such as a flash timeout), a parameter error, an invalid macro, or a macro that was called out of order (for example if the Flash Write macro was called without calling the Flash Unlock macro first).

8.1 NOOP Macro – 0x8400

The MACRO register will clear when the V545 detects this macro.

8.2 Reset Macro – 0x8407

Force a hard reset. V545 processor will reboot its code and reset the FPGA. The V545 will disappear from the VME bus for about four seconds.

This macro should be processed within five seconds.

8.3 Flash Unlock Macro – 0x8408

Enable write accesses to the flash memory. This macro exists as a redundant measure to prevent accidental/unintended flash accesses.

This must be executed before any flash programming operations. It remains active until a reboot. See section 14 about re-flashing firmware.

8.4 Flash Erase Macro – 0x8409

Erase the user-upgrade region of the flash memory. The Flash Unlock macro must have been executed first.

This takes up to 25 seconds. While the flash is erasing, PARAM0 will be updated with the sector number (16 to 31) of the flash that is being erased.

If the module is subsequently power cycled or reset, the original factory code will be run.

See section 14 about re-flashing firmware.

8.5 Flash Write Macro – 0x840A

Write to the user-upgrade region of the flash memory. The Flash Unlock macro must have been executed first.

PARAM0 should contain the number of the 128-byte page, indexed from zero.

Registers R0 to R63 should contain the data to write, in *little endian format*. For example, if the first six bytes to write into a page of the flash are {0x01, 0x02, 0x03, 0x04, 0x05, 0x06}, then R0 should be 0x0201, R1 should be 0x0403, and R2 should be 0x0605.

Do not use this macro when using an Override Function Block.

See section 14 about re-flashing firmware.

8.6 Checksum Flash Macro – 0x840B

Checksum the images stored in the flash. The results are stored in the PARAM0 and PARAM1 registers:

PARAM0 result:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						FP1	FP0							FF1	FF0

PARAM1 result:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						UP1	UP0							UF1	UF0

Bit fields are:

FP Factory FPGA

FF Factory Firmware

UP Upgrade FPGA

UF Upgrade Firmware

The field values for all fields are:

00 Image not present

01 Checksum okay

10 Checksum fail

11 Undefined

This macro is useful for determining the success of a re-flash operation before resetting the V545. See section 14 about re-flashing the firmware.

This macro should be processed within five seconds.

8.7 Reset PSD Macro – 0x840C

Synchronously reset Phase-Sensitive Detectors, time-aligning them. PARAM0 is a bitmask of PSDs 0 to 15. PARAM1 is a bitmask of PSDs 16 to 23. The upper 8 bits of PARAM1 are unused. A bit value of '1' causes the PSD to reset; a value of '0' has no effect on the PSD. Be careful when setting up these parameters; PARAM1 is not long-word aligned.

This is used for synchronizing PSDs when multiple channels are used for calculations.

8.8 Read Flash Macro – 0x8410

Read 128 bytes out of the upgrade portion of the flash.

PARAM0 should hold the 128-byte page number. (This is the same parameter value that would be used for the Flash Write macro.)

The results will be printed to registers R0 to R63, in *little-endian format*. For example, if R0 is 0x0102, then the first byte of the requested flash page is 0x02 and the second byte of the page is 0x01.

This macro is useful for verifying that a page was correctly written with the Flash Write macro. See section 14 about re-flashing the firmware.

Do not use this macro when using an Override Function Block.

8.9 Read Power Supply Macro – 0x8411

Display self-test voltages in millivolts in the first eight registers of the register file, R0 to R7.

Register	Signal	Ideal value (mV)
R0	DAC reference	4500
R1	+2.5V Power	2500
R2	+3.3V Power	3300
R3	VMID – ADC “COM” input	2150
R4	VAMP – ADC Reference	1792
R5	+1.2V Power	1200
R6	Ground	0
R7	+3V analog reference	3000

8.10 Reset DDS Macro – 0x8414

Synchronously reset Direct Digital Synthesizers, time aligning them. PARAM0 is a bitmask of DDS’s. A bit value of ‘1’ causes the DDS to reset. A bit value of ‘0’ has no effect. The upper eight bits of PARAM0 are ignored.

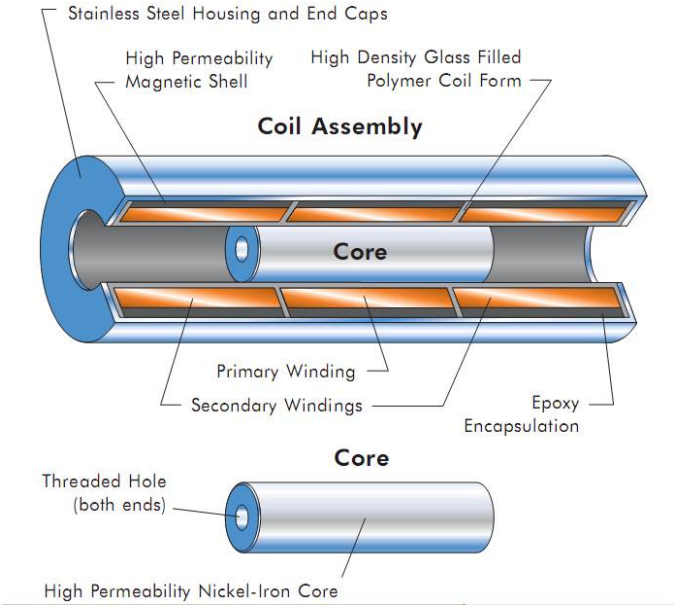
This is used when phase alignment is needed for multiple DDSs.

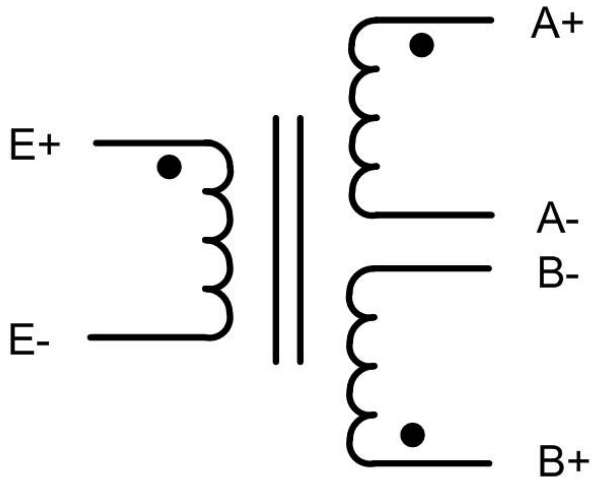
9. LVDTs

9.1 LVDT Theory and Types

An LVDT is a Linear Variable Differential Transformer, a linear position sensor based on varying the coupling of magnetic coils based on the physical position of a movable magnetic core.

The basic LVDT has three coils wound sequentially on a support bobbin.





In normal operation, an AC sine wave is connected into the primary winding, the E+ and E- terminals. Voltage is induced into the "A" and "B" secondary windings. The E+, A+, and B+ voltages are electrically in phase, and the A and B voltages are equal when the core is centered. As the core moves off-center, the A and B voltages change, with one increasing and the other decreasing within the working range of displacement.

LVDT primary excitation is typically a few volts RMS, commonly in the 2-10 KHz range.

There is a wide range of conventions and variations among available LVDTs. They may present three, four, five, or six wires, with varying nomenclature and color coding.

9.2 LVDT Simulation with Channel Control Blocks

LVDTs can be simulated using the basic channel tools. Higher level tools are discussed in section 11.4.

An example is the Lucas/Schaevitz model 050HR, a six-wire, free-core, short-stroke LVDT. Characteristics are:

Recommended excitation: 3 volts RMS at 2.5 KHz

Nominal secondary voltage: 4.25 volts RMS, core centered

Motion range: ± 0.050 inches from center position.

Primary DC resistance: 41 ohms

Primary inductance: 21.6 mH with core centered, 8.7 mH with no core

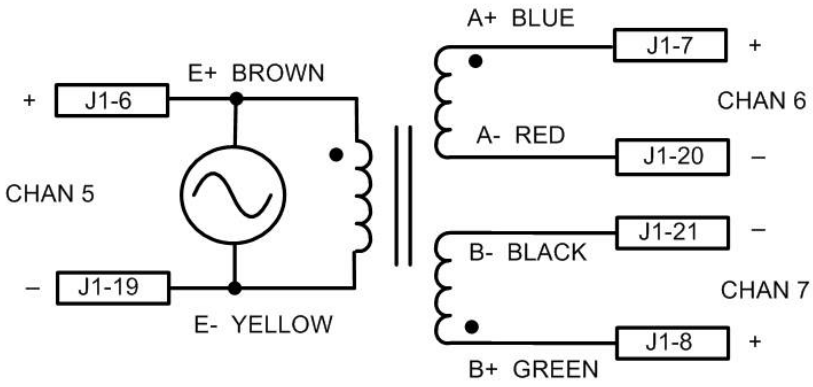
Secondary DC resistance: 765 ohms

Secondary inductance: 139 mH with core centered, 71 mH with no core.

Sensitivity: 17.2 mV RMS per mil, A+ to B+

Type 1 transformers would be used, 1:1 ratio.





To simulate such an LVDT, assume that the V545 will receive the nominal excitation from an external source, using the connections shown above. The three "-" signals may be grounded if desired. The external 3 volt RMS excitation is accepted on channel 5, and channels 6 and 7 are the simulated secondary outputs.

The channels would be programmed as follows:

CTL5	0x0000	Input
CTL6	0x0541	Output, Gain = 2X, MUXbus source channel 5
CTL7	0x0541	Output, Gain = 2X, MUXbus source channel 5

The channel 6 and 7 output gains are set to 2X, since this LVDT has a step-up ratio of about 1.4. The output channels could then generate a maximum of 6 volts RMS, based on a 3 volt excitation signal received on channel 5.

To simulate the core at center, the channel 6 and 7 outputs should both be 4.25 volts RMS. Since the output channel gains are set to 2X, the AMP6 and AMP7 amplitude registers should be set to 4.25 / (3.00 * 2), which is 0.708 fractional, 23210 decimal, 0x5AAA, which values simulate the core at mid position.

To simulate 1 mil of travel, we need to increase the channel 6 output by 8.6 mV and decrease the channel 7 output by the same amount. Since the full-scale output voltage of 6.00 volts RMS corresponds to 1.00 fractional, 32768 LSBs, 8.6 mV is 0.001433 fractional, or 46.96 LSBs. So add 47 LSBs to AMP6 and subtract the same amount from AMP7 to simulate 1 mil of travel.

We are assuming here that the sum of the secondary voltages is constant over the range of travel, and that the voltage difference is linear on core position, namely that

$$\text{Position} = K * (VA-VB) / (VA+VB)$$

This is often true for LVDTs, especially short-stroke units, but not always so. VA+VB may not be constant, and the relation may be nonlinear.

The source impedance of either actual LVDT secondary winding would be about 2300 ohms. If a cable had 15 pF of capacitance per foot, 50 feet of cable would present a load of 750 pF, which has a reactance of about 84K ohms. This is not a significant load to the 2300 ohm reactance, so this much cable loading on a real LVDT would be small, and we can ignore it in this simulation and leave the DLY6 and DLY7 registers zero. To emulate long cable runs with this LVDT, cable phase shifts and resonance amplitude effects could be added to the simulation.

9.3 LVDT Acquisition with Channel Control Blocks

LVDTs can be acquired using the basic channel tools. Higher level tools are discussed in section 11.3.

Using the Lucas/Schaevitz example from the previous section, this time the V545 is wired such that the middle of the previous example's figure represents an actual LVDT and the laterals of the figure represent the V545. Channel five is connected to an actual "E" winding, channel 6 is connected to an actual "A" winding, and channel 7 is connected to an actual "B" winding.

If providing the excitation voltage, set channel 5 to be an output, and use a DDG. The DDG and excitation channel would be programmed as follows:

DFR0	0x1388	2.5 kHz
DAM0	0xFFFF	Full amplitude
CTL5	0x1F01	Output, MUXbus source DDG 0
AMP5	0x3508	3 volts RMS, 41.4% full range

The A and B channels would be programmed as follows:

CTL6	0x0500	Input, MUXbus source channel 5
CTL7	0x0500	Input, MUXbus source channel 5

After channels are set up, synchronize the phase-sensitive detectors to time-align the data (using the Reset PSD macro and pertinent bitmask in the PARAM registers – see section 8.7). This is not necessary if the channel control register's "F" value is 1.

Now read the phase-sensitive detector inputs, and use the displacement formula:

$$\text{Position} = K * (VA-VB) / (VA+VB)$$

This is often true for LVDTs, especially short-stroke units, but not always so. VA+VB may not be constant, and the relation may be nonlinear.

10. Synchros and Resolvers

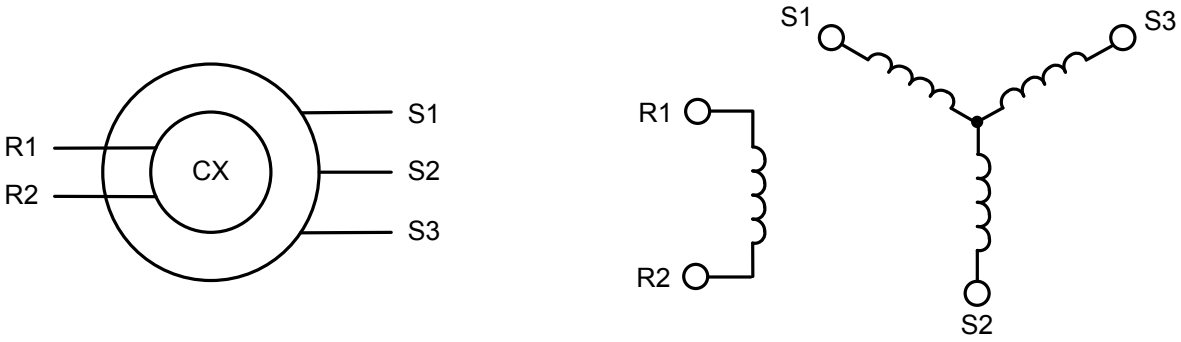
A synchro is a rotary transformer that can sense angular position.



The synchro family of devices includes...

10.1 Synchro Transmitter CX

The synchro transmitter couples its rotor winding, the reference, to three secondary windings. An AC reference voltage is applied to the rotor, and it induces voltages into the three stator secondaries, with the magnitude of the coupled secondary voltages changing as a function of the angular position of the shaft.



An excitation sine wave is applied to R1:R2, namely high on R1 and low on R2. The resulting output AC voltages are:

$$V(S3:S1) = K * V(R1:R2) * \sin(\Theta)$$

$$V(S2:S3) = K * V(R1:R2) * \sin(\Theta + 120°)$$

V(S1:S2) = K * V(R1:R2) * sin (Θ + 240°)

where a negative sin() value corresponds to phase inversion of the secondary voltage waveform compared to the reference. K is a coupling factor, typically around 0.4 to 0.8.

Voltage S3:S1 is zero at Θ = 0, and increases in-phase with R1:R2 as the angle is initially increased. The convention is that positive angle is CCW (rotation left) as viewed looking at the shaft.

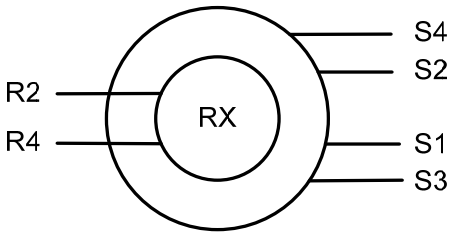
The induced voltages are nominally in phase electrically with the AC reference voltage, or inverted if the sin() expression is negative. The angular information is expressed in the relative amplitudes of the three AC secondary voltages. In practice, there will be some electrical phase shift, typically 5-20 degrees lead for an unloaded synchro, but that may become lag if a large amount of cable capacitance is present.

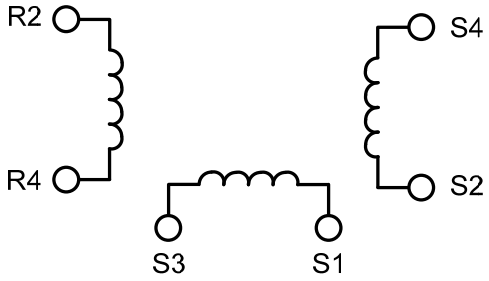
A common excitation voltage for aerospace synchros is 26 volts RMS at 400 Hz, inducing a maximum of 11.8 volts into a secondary pair. The large Navy type synchros usually operate with reference voltages of 115 RMS at 60 Hz, inducing about 90 volts max into a secondary pair. V545 transformer options can be selected to match the expected voltages.

A V545 channel may not have sufficient power output capacity to directly excite a synchro or resolver.

10.2 Resolver Transmitter RX

The resolver transmitter is similar to the synchro transmitter except that it has two secondary windings 90 degrees apart.



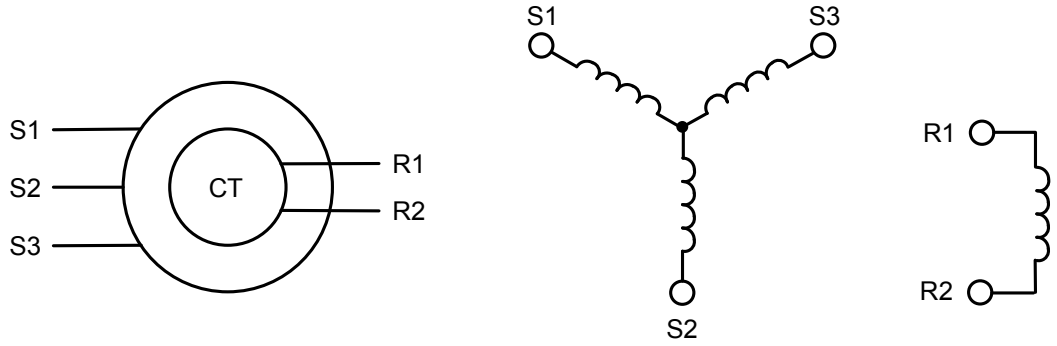


V(S1:S3) = K * V(R4:R2) * sin (Θ)

V(S4:S2) = K * V(R4:R2) * cos (Θ)

10.3 Synchro Receiver/Control Transformer CT

The synchro receiver is physically identical to a synchro transmitter, but it accepts inputs on the S1-S2-S3 terminals and outputs on R1:R2. The magnitude and phase of the R1:R2 signal is a function of the difference between the shaft and the angle expressed by the S1-S2-S3 signals. A CT is generally used as the position error sensor in a position servo system.

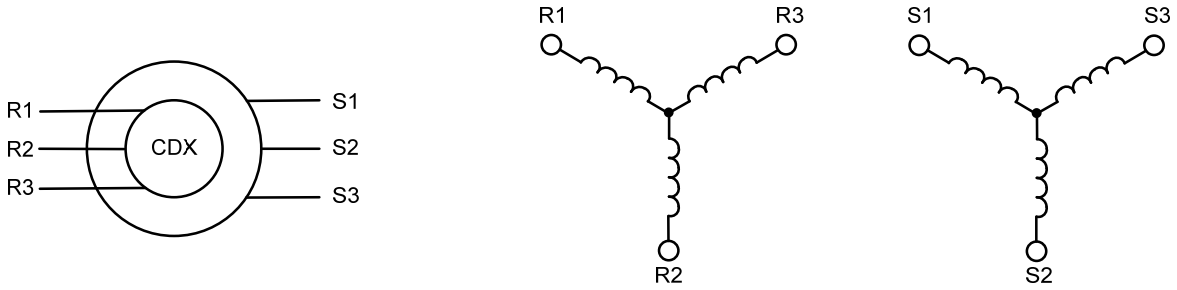


10.4 Resolver Receiver/Control Transformer RC

The resolver receiver is physically identical to a resolver transmitter, but it accepts inputs on the S1-S4 terminals and outputs on R1:R2. The magnitude and phase of the R1:R2 signal is a function of the difference between the shaft and the angle expressed by the S1-S4 signals.

10.5 Control Differential Transformer CDX

The control differential transformer has two a 3-wire input and a 3-wire output. The output is a synchro signal that is the input signal rotated by the shaft angle.



10.6 Synchro/Resolver Simulation with Channel Control Blocks

Synchros and resolvers can be simulated using the basic channel tools, and several of the common types can also be simulated using the Function Blocks described in section 11.2

For a simulation with external excitation, select a channel to receive the excitation signal and program that channel it to be an input. For internal excitation, program one DDS signal generator to be the sinewave source and program a channel to be an output and accept this DDS source.

Then select two or three channels to be outputs, as needed to simulate a resolver or a synchro. Two channels could be used to simulate the three synchro signals, but the drive would be asymmetric; best synchro accuracy uses three channels wired in a triangle hookup.

Program the output channels to accept the DDS generator as their multiplexed signal source (for internal excitation cases) or to accept the reference channel as their multiplexed signal source (for external excitation) and program the channel amplitudes per the synchro or resolver equations above. Channel delay registers may be used to simulate electrical phase shifts.

10.7 Synchro/Resolver Input with Channel Control Blocks

Synchro and resolver positions can be acquired using the basic channel tools, and several of the common types can also be acquired using the Function Blocks described in section 11.1

For acquisition with external excitation, select a channel to receive the excitation signal and program that channel it to be an input. For internal excitation, program one DDS signal generator to be the sinewave source and program a channel to be an output and accept this DDS source. (Note that a V545 channel using a DDS may not sufficiently drive the excitation for some models of synchro or resolver receivers. The output channel's signal should be amplified externally before it is connected to the receiver windings. Some phase lag may result from this.)

Then select two or three channels to be inputs, as needed to measure a resolver or a synchro respectively.

The input channels will use their phase-sensitive detectors to acquire the incoming sinewave signals. The "M" field of the channel control registers should be loaded to select the DDS or the reference receiver channel, which selects the demodulation reference for the phase-sensitive detectors. The channel control F bits can be selected for the number of cycles to be acquired: use 1 for fastest acquisition and larger values for slower acquisition with better noise rejection.

After channels are set up, synchronize the phase-sensitive detectors to time-align the data (using the Reset PSD macro and pertinent bitmask in the PARAM registers – see section 8.7). This is not necessary if the channel control register's "F" value is 1.

Now read the phase-sensitive detector outputs. For resolvers, the shaft angle is the arctangent of the Y-axis PSD value divided by the X-axis PSD value. Necessary operations include checking for reasonable voltages, divide-by-zero checking, and quadrant decoding. The c-library "atan2" function accepts Y and X values and does the full 2pi transformation.

For synchros, a "Scott-tee" transformation must be done with the 3-channel data to reduce it to Y-X resolver equivalent.

11. Function Blocks

Twelve 32-word Function Blocks are provided in the V545 register map. These provide higher-level math operations than the direct approach using the Channel Control Blocks discussed in chapters 9 and 10. They simulate and acquire LVDTs, RVDTs, synchros, and resolvers. Every millisecond, the chain of twelve Function Blocks is executed, from FB0 to FB11.

Each Function Block takes control of one or more of the twenty-four I/O channels from their Channel Control Blocks. Function Blocks do not control shared resources, such as DDS signal generators and reference I/O channels. These must be set up by users before Function Blocks are initialized. When a function block controls an I/O channel, the channel's control registers will be ignored. Function Blocks do not update the R/W registers in the channel blocks; their behavior is transparently overruled behind the scenes. When a Function Block is cleared, control over the I/O channels will be returned to the Channel Control Block's registers.

All function blocks have a function register **FUN** at offset 0x00 from their register base, an operation register **OPR** at offset 0x02 from their register base, and a status register **STS** at offset 0x06 from their register base.

Writing a function number to the FUN register enables the function block. If a function block is enabled, users should always clear it by writing zero to FUN and waiting for STS to clear before using the function block for a different function. Changes from one function to another without clearing the function block results in undefined behavior.

FUN value	Function
0	None; function block is free
1	***DEPRECATED***: Synchro/Resolver Acquisition
2	***DEPRECATED***: Synchro/Resolver Output/Simulation
3	LVDT/RVDT Input
4	LVDT/RVDT Output/Simulation
5	Synchro/Resolver Acquisition
6	Synchro/Resolver Output/Simulation

The setup procedure common to all functions is:

- Clear FUN and OPR
- Write the function number to FUN
- Write setup registers (described for each function in the subsections that follow)
- Write 0x01 ("Initialize") to OPR
- Wait for OPR to self-clear

When OPR has cleared, setup is complete for the Function Block. STS will either report successful initialization by setting bit 0 (0x0001), or it will report a configuration error by setting bit 12 (0x1000). It is considered a configuration error if any of the setup registers have improper values, or if the Function Block's channels do not have matching

transformer ratios, except for the reference/excitation channel. Other error flags in STS are described for each function in the subsections that follow.

IMPORTANT NOTE ABOUT FUNCTION BLOCKS 1 AND 2:

Function blocks 1 and 2 are deprecated, due to a phase discrepancy in previous firmware's resolver function blocks. End users should use function blocks 5 and 6 in their place. Proper operation of these function blocks is still possible with intentional "miswiring," so they remain in the firmware for backwards-compatibility with existing end-users' systems.

The following documentation is the same for function block 1 as for function block 5, and the same for function block 2 as for function block 6, with the following major exceptions regarding resolvers:

- The channel pointers' R bits represent R4:R2 for function blocks 1 and 2.
- Function block 1 calculates angle as if the Y channel is 180 degrees out of phase.
- Function block 2 simulates the Y channel 180 degrees out of proper phase.

11.1 Synchro/Resolver CX/RX Acquisition Function Block

A synchro/resolver input Function Block initializes two or three stator/secondary I/O channels and subsequently digitizes their voltages and processes their signals into an angular position. This block does not initialize the reference I/O channel or its optional DDS sine wave source.

The register layout is below. "Offset" is relative to the Function Block start address. The R/W registers marked with a single asterisk (*) will be read only during Function Block initialization.

Reg Name	**Offset**	**R/W**	**Function**
FUN	0x00	RW	Function Code = 0x05
OPR	0x02	RW	Operation
FLG	0x04	RW*	Setup-time flags
STS	0x06	RO	Real-time status
OVR	0x08	RO	Override control
	. . .		
CP01	0x10	RW*	Channel pointers 0, 1
CP23	0x12	RW*	Channel pointers 2, 3
CP45	0x14	RW*	Channel pointers 4, 5
CP67	0x16	RW*	Channel pointers 6, 7
	. . .		
SRP	0x1A	RW*	Phase Shift
	. . .		
	0x20		reserved
AP	0x22	RO	Actual Position
	0x24		reserved
FP	0x26	RO	Filtered Position
FV	0x28	RO	Filtered Velocity
	. . .		
MSV	0x30	RO	Measured secondary voltage

When setting up this Function Block, the recommended sequence is:

Program an I/O channel to generate or to accept the reference voltage.

Clear the FUN, OPR, and FLG words.

Write all operating parameters, including channel pointers and phase shift.

Write the Flags word FLG.

Write the function code 0x01 to FUN.

Write the "initialize" command 0x01 to the Operation Register OPR.

Offsets 0x32 to 0x3E may be used for scratch registers after the function block has been set up.

11.1.1 FUN Register (RW)

Load the FUN with function code 0x05 to enable synchro/resolver acquisition.

11.1.2 FLG Register (RW)

The flags word FLG should be loaded by the user before loading FUN.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									F2	F1	F0	T3	T2	T1	T0

The T3...T0 nibble specifies the device type. 0x00 is a standard 3-secondary synchro, and 0x01 is a 2-secondary resolver. Other codes are reserved.

The F2...F0 bits specify filtering speed for the measured angle.

F value	**Cutoff Frequency (turns/sec)**
0	No filtering
1	1 (slowest)
2	2
3	5
4	10
5	20
6	50
7	100 (fastest)

11.1.3 OPR Register (RW)

The Operations Register OPR accepts action commands.

Write 0x01 to OPR to initialize the Acquisition Block. This will:

Set up the two or three I/O channels which acquire resolver or synchro secondary signals.

Set the AP and FP and FV words to zero.

Set the Status Register STS to 0x01, "initialized"

Clear the Operations Register OPR

Begin angular position acquisition.

11.1.4 STS Register (RO)

The read-only Status Word STS reflects real-time acquisition status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SE	EE	CE				OR								IN

The IN bit indicates that the Acquisition Block has been initialized and is operating.

OR will be set if the block is in Override mode, namely if the override register OVR is nonzero. In this case, the actual synchro/resolver position is not acquired and an override position is loaded into Actual Position AP. For input blocks like this type, override is mainly used for testing.

The upper nibble is error flags. They are:

CE Configuration Error

EE Excitation Error; this bit is set if the excitation voltage is too low, specifically less than 1 volt RMS using 1:1 transformers.

SE Signal Error; this bit is set if the measured secondary voltage is below 100 mV or if there is an ADC clipping error on one of the function block's secondary channels.

11.1.5 OVR Register (RO)

The Override Word OVR is loaded by an Override Block.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B3	B2	B1	B0						R6	R5	R4	R3	R2	R1	R0

If the R field is nonzero, R6:R1 is an index to a word in the Rnn register file that defines the override position. Normal acquisition is suspended and the Rnn value is loaded into position register AP**.** The index R6:R0 is the byte offset from R0 (0x80) to the override position word. Bit 0 should always be 0. The filtered position FP will follow the AP value.

The B field identifies which Override Block loaded OVR. Since four Override Blocks (OB12 to OB15) are defined, the value will be 12 to 15.

Overrides are mainly used by "position output" type Function Blocks, but are available on input Function Blocks for testing or special applications.

11.1.6 Channel Pointer Registers (RW)

Resolvers use the CP01 and CP23 channel pointer words to name three I/O channels.

Note: A V545 channel using a DDS may not sufficiently drive the excitation for some models of synchro or resolver receivers. If the “R” channel described below is used as an output, its signal should be amplified externally before the signal is connected to the receiver windings. Some phase lag may result from this, which can be adjusted by the SRP register.

CP01 for resolvers is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			R4	R3	R2	R1	R0								

Where the R bits are encoded 0 through 23 to assign the reference I/O channel, the channel that generates the reference voltage (for internal excitation) or that accepts the reference (for external excitation.) The resolver rotor leads R2:R4 are connected to this I/O channel.

CP23 for resolvers is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			Y4	Y3	Y2	Y1	Y0				X4	X3	X2	X1	X0

Where the Y bits are encoded 0 through 23 to assign the Y-axis input, namely the I/O channel that is wired to the resolver sine (S1:S3) secondary. The X bits assign the channel that is wired to the resolver cosine (S4:S2) secondary.

Synchros use CP01 and CP23 to name four I/O channels.

CP01 for synchros is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			R4	R3	R2	R1	R0				A4	A3	A2	A1	A0

Where the R bits are encoded 0 through 23 to assign the reference I/O channel, the channel that generates the reference voltage (for internal excitation) or that accepts the reference (for external excitation.) The synchro rotor leads R1:R2 are connected to the I/O channel.

The A bits assign the I/O channel that is connected to the S3:S1 secondary of the synchro.

CP23 for synchros is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			B4	B3	B2	B1	B0				C4	C3	C2	C1	C0

Where the B bits are encoded 0 through 23 to assign the I/O channel that is wired to the synchro S2:S3 secondary. The C bits assign the I/O channel that is wired to the S1:S2 secondary.

11.1.7 SRP Register (RW)

The SRP register programs the delay in the two (resolver) or three (synchro) input Channel Control Blocks. This uses the same scale and units as the DLYn register. Note, however, that this does not change the contents of the DLYn register. When the function block is cleared the channel's delay will return to the value set by its DLY register.

11.1.8 Position and Velocity Registers (RO)

The AP register reports the fast (unfiltered) angular position of the synchro or resolver. The scaling is 0x0000 for zero degrees and 0xFFFF for 359.995 degrees. The MS bit represents 180 degrees and the LS bit represents about 0.0055 degrees, or about 0.33 minutes. Users may treat the AP register as signed, covering the range of -180 to +179.995 degrees.

The FP register is the filtered version of AP. It responds slower than AP and reduces angular position noise. The response speed is selected by the F field in FLG.

FV is the signed Filtered Velocity Register. Positive values represent CCW rotation.

11.1.9 MSV Register (RO)

MSV is the measured secondary voltage. For a resolver, it is the square root of the sum of the squares of the two secondary voltages. For a synchro, it is the equivalent after the Scott-t transform. The scaling is 1 millivolt per LSB. The MSV register does not calculate the transformer ratio.

11.2 Synchro / Resolver CX/RX Simulation Function Block

A synchro/resolver output Function Block initializes two or three stator/secondary I/O channels as outputs and subsequently drives their signals to simulate an angular position. This block does not initialize the reference I/O channel or its optional DDS sine wave source.

The register layout is below. "Offset" is relative to the block start address. The R/W registers marked with a single asterisk (*) will be read only during function block initialization.

Reg Name	**Offset**	**R/W**	**Function**
FUN	0x00	RW	Function Code = 0x06
OPR	0x02	RW	Operation
FLG	0x04	RW*	Setup-time flags
STS	0x06	RO	Real-time status
OVR	0x08	RO	Override Word
	. . .		
CP01	0x10	RW*	Channel pointers 0 (MS byte) , 1 (LS byte)
CP23	0x12	RW*	Channel pointers 2, 3
CP45	0x14	RW*	Channel pointers 4, 5
CP67	0x16	RW*	Channel pointers 6, 7
SRK	0x18	RW*	K amplitude scalar
SRP	0x1A	RW*	Phase Shift
HS1	0x1C	RW*	Min hard stop
HS2	0x1E	RW*	Max hard stop
	. . .		
AP	0x22	RO	Actual Position
	. . .		
TP	0x26	RW	Target Position
TV	0x28	RW	Target Velocity
BRK_A	0x2A	RW	Coil error simulation register
BRK_B/BRK_Y	0x2C	RW	Coil error simulation register
BRK_C/BRK_X	0x2E	RW	Coil error simulation register

When setting up this Function Block, the recommended sequence is:

Program an I/O channel to generate or to accept the reference voltage.

Clear the FUN and OPR registers. Wait at least one millisecond.

Write all operating parameters, including channel pointers, flags, phase shift, and initial TP value.

Write the function code 0x02 to function register FUN.

Write the "initialize" command 0x01 to the operation register OPR.

Wait for OPR to clear and check that there are no error flags in the status register STS.

Write the desired 'runtime' operation (2 through 5) to the operation register OPR; simulated output will begin.

11.2.1 FUN Register (RW)

Load FUN with function code 0x06 to enable synchro/resolver simulation. Write zero to FUN to end synchro/resolver simulation.

11.2.2 FLG Register (RW)

The Flags Word FLG should be loaded by the user before loading FUN.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		S1	S0									T3	T2	T1	T0

The T3...T0 nibble specifies the device type. 0x00 is a standard 3-secondary synchro, and 0x01 is a 2-secondary resolver. Other codes are reserved.

The S1:S0 bits specify the smallest time interval for processing TV and TP register inputs. By default, this is every millisecond. These bits apply to units with firmware revision D or later. Units with earlier firmware will ignore these bits.

S value	**Smallest Time Interval**	**TV LSB (deg. per sec.)**
0 (default)	1 ms	5.49316
1	10 ms	0.54932
2	100 ms	0.05493
3	reserved	Reserved

11.2.3 OPR Register (RW)

The Operations Register OPR accepts action commands to initialize the function block and to set operating mode. In brief, the OPR codes are:

OPR	Operating mode	Description
0	IDLE	Do nothing; do not output angular position
1	INITIALIZE	Initialize and reset to IDLE when finished
2	MOVE_SIGNED	Ramp to value in TP register at speed determined by signed value of TV register
3	MOVE_SHORTEST_PATH	Ramp to value in AP register at speed determined by absolute value of TV register
4	SPIN_SIGNED	Spin continuously at speed determined by signed value of TV register
5	MOVE_HARD_STOP	Ramp to value in TP register at speed determined by absolute value of TV register, but do not pass through cut-out region defined by HS1 and HS2.

A simulation function block must be initialized by writing '1' to OPR before any of the operating modes can be used.

The normal usage of the OPR register is to write '1' to initialize the function block, wait for OPR to self-clear (enter IDLE mode), and then write a 'runtime' operation (2 through 5) to OPR. After a function block has been initialized, it can be re-initialized at any time by writing a '1' back into the OPR register. Angular output will cease when re-initializing a function block.

Although a VME user can change OPR from one runtime mode one to another, this is not the function block's ordinary design purpose. It will only read its channel pointers, flags, hard stop registers, and SRP and SRK registers while in INITIALIZE mode.

A VME user may change TP or TV at any time. During one of the runtime OPR modes (2 through 5), the function block will respond to changes in these registers within the number of milliseconds determined by the "slow" S bits in the FLG register.

The OPR codes are discussed individually below.

11.2.3.1 **IDLE (OPR = 0)**

Users are not expected to set an initialized function block into IDLE mode directly, except before writing the FUN register. This mode is set automatically by the self-clearing INITIALIZE mode.

While in IDLE mode, the function block waits for OPR to be set to a runtime operation. No simulated output will occur at any angle, and overrides will not be processed.

11.2.3.2 INITIALIZE (OPR = 1)

Write 1 to OPR to initialize the simulation block. This will:

Set up the two or three I/O channels which generate simulated resolver or synchro secondary signals.

If SRK is zero, set SRK to 0x8000

Copy TP to AP

Set the “Initialized” IN bit in the STS register

Clear OPR to ‘0’

Initialization is complete when OPR self-clears to 0, and successful if the IN bit is set in STS. If there are no error flags in the STS register, a user may then write a ‘runtime’ operating mode (2 through 5) to the OPR register to begin angular output. The first simulated angle is the value of TP that was saved at initialization time.

Warning: Behavior is undefined if a VME user changes the function block’s registers between start and end of INITIALIZE mode. Always wait until INITIALIZE mode completes before writing to the function block’s registers.

11.2.3.3 MOVE_SIGNED (OPR = 2)

When OPR is 2, the simulated position will move towards the target position TP at the specified target velocity TV. The MSB of TV may be considered a sign bit in this case. A value of 0xFFF0 in TV, for example, will cause the simulated output to move at the same rate as 0x0010, but in the opposite direction.

11.2.3.4 MOVE_SHORTEST_PATH (OPR = 3)

When OPR is 3, the sign of TV (its MSB, indicating 180 degrees) will be ignored. The simulated output will approach the angle at TP using the direction of the shortest path. A value of 0xFFF0 in TV, for example, will cause the simulated output to move at the same rate as 0x0010, but the direction depends on the distance from AP to TP. If TP is exactly 180 degrees (0x8000) away from AP, then the path will default to the counter-clockwise direction.

11.2.3.5 SPIN_SIGNED (OPR = 4)

When OPR is 4, the actual simulated output will increment continuously at the signed target velocity TV, applying the same TV rules as MOVE_SIGNED. TP will be ignored.

11.2.3.6 MOVE_HARD_STOP (OPR = 5)

When OPR is 5, the simulated position will move towards the target position TP in whichever direction causes the simulated position to not pass through the cut-out region defined by HS1 and HS2 (see section 11.2.11, Hard Stop registers).

The velocity is the absolute value of TV. A value of 0xFFF0 in TV, for example, will cause the simulated output to move at the same rate as 0x0010, but the direction depends on the hard stops.

Handling of invalid TP

If the *initial* position is in the cut-out region, the function block will not simulate an angle and the STS register will report a configuration error. TP must be changed to a valid position before angular output will begin.

If TP is set to an invalid angle after angular output has begun, then the simulated output angle will not move and the STS register will report a configuration error, until a valid TP is entered. *This is true for invalid override positions as well.* VME users should be careful to never use an invalid override position for a function block in MOVE_HARD_STOP mode, or the simulated output will not move to the override position.

If TP is equal to either HS1 or HS2, it is at the *boundary* of the cut-out region but not inside it. TP is considered valid in this case.

11.2.4 TV Register (RW)

TV represents the 16-bit fraction of a circle that is added to AP to ramp toward the target position TP.

When in MOVE_SIGNED or SPIN_SINGED, the full 16-bit value is used. The MSB, which represents 180 degrees, can be thought of as a sign bit in this case; 350 degrees will in fact be -10 degrees. If TV is positive, the direction is CCW; if TV is negative the direction is CW.

When in MOVE_SHORTEST_PATH or MOVE_HARD_STOP mode, the sign bit is ignored. The largest velocity in this mode will not exceed 180 degrees.

The TV value is applied every millisecond, every ten milliseconds, or every hundred milliseconds, depending on the S bits in the FLAG register. The maximum positive value of 0x7FFF scales to 179.994 degrees of CCW rotation in one millisecond, so the when the S bits are zero (every millisecond), the LSB corresponds to 5.493 degrees per second.

CAUTION: it is possible for a programmed movement to go "the wrong way." The MOVE_SIGNED mode will take the long way around if programmed to go from 2 degrees to 1 degree with a positive velocity. The MOVE_SHORTEST_PATH move from +10 to -10 degrees might hit a mechanical stop at 0 degrees. Use extreme care

in planning ramped moves in safety-critical systems. The MOVE_HARD_STOP mode was designed for this purpose.

11.2.5 TP Register (RW)

The TP register is the target position. The value of TP during INIITIALIZE mode will be the first angle output when entering a runtime mode. In the 'move' modes (MOVE_SIGNED, MOVE_SHORTEST_PATH, MOVE_HARD_STOP), the simulated output AP will proceed towards the angle in TP following the rules of the specific operating mode. SPIN_SIGNED mode ignores TP.

11.2.6 STS Register (RO)

The read-only status register STS reflects real-time simulation status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		EE	CE				OR								IN

The IN bit indicates that the Simulation Block has been initialized.

OR will be set if the block is in Override mode, namely if the OVR register is nonzero.

The upper nibble holds error flags. They are:

CE Configuration Error

EE Excitation Error; this bit is set if the excitation voltage is too low, specifically less than 1 volt RMS using 1:1 transformers.

11.2.7 OVR Register (RO)

The OVR Override Word is loaded by an Override Block; see section 12. The VME CPU should not try to write this register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B3	B2	B1	B0						R6	R5	R4	R3	R2	R1	R0

If the R field is nonzero, R6:R1 is an index to a pair of words in the Rnn register file that define the override position and override velocity, in that order. The simulated position AP ramps to the override position at the override velocity. The index R6:R0 is the byte offset from R0 (0x80) to the override position word. Bit 0 will always be read as '0'.

The B field identifies which Override Block loaded OVR. Since four Override Blocks (OB12 to OB15) are defined, the value will be 12 to 15. Thus, any non-zero OVR value indicates an override condition.

Direction of override path

During an override condition, the direction towards the override position will follow the same rules as the function block's current OPR mode. If, for example, the function block is in MODE_HARD_STOP during an override, the override path will be in the direction that avoids the cutout region determined by HS1 and HS2. If the function block is in a signed-path mode during an override, the sign of the override velocity will be used for override direction, not the sign of TV.

11.2.8 Channel Pointer Registers (RW)

Resolvers use the CP01 and CP23 channel pointer words to name three I/O channels. The F bits in the CP registers described below apply to units with firmware revision D or later. Units with earlier firmware revisions will ignore these bits.

CP01 for resolvers is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			R4	R3	R2	R1	R0								

Where the R bits are encoded 0 through 23 to name the reference I/O channel, the channel that generates the reference voltage (for internal excitation) or that accepts the reference (for external excitation.) The resolver rotor leads R2:R4 are connected to the I/O channel.

R values 0 through 23 select the ADC input of an I/O channel, whether the channel is an input (digitizing an external reference voltage) or an output (generating the reference signal from a DDS generator.)

CP23 for resolvers is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FY			Y4	Y3	Y2	Y1	Y0	FX			X4	X3	X2	X1	X0

Where the Y bits are encoded 0 through 23 to name the Y-axis input, namely the I/O channel that is wired to the resolver sine (S1:S3) secondary. The X bits name the channel that is wired to the resolver cosine (S4:S2) secondary. If set, the FY and FX bits flip the polarity of the Y and X channels, respectively, effectively shifting their phase 180 degrees.

Synchros use CP01 and CP23 to name four I/O channels

CP01 for synchros is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			R4	R3	R2	R1	R0	FA			A4	A3	A2	A1	A0

Where the R bits are encoded 0 through 23 to name the reference I/O channel, the channel that generates the reference voltage (for internal excitation) or that accepts the

reference (for external excitation.) The synchro rotor leads R1:R2 are connected to the I/O channel.

The A bits name the I/O channel that is connected to the S3:S1 secondary of the synchro. If set, the FA bit flips the polarity of the A channel amplitude, effectively shifting its phase by 180 degrees.

CP23 for synchros is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FB			B4	B3	B2	B1	B0	FC			C4	C3	C2	C1	C0

Where the B bits are encoded 0 through 23 to name the I/O channel that is wired to the synchro S2:S3 secondary. The C bits name the channel that is wired to the S1:S2 secondary. If set, the FB and FC bits flip the polarity of the B and C channels, respectively, effectively shifting their phase by 180 degrees.

11.2.9 SRK Register (RW)

The SRK register scales the reference voltage to the two or three simulated secondary voltage outputs. For example, a common 400 Hz synchro uses a reference voltage of 26 RMS and has a maximum secondary voltage of 11.8 RMS, a K-factor of 0.453. Load SRK with the fractional equivalent of 0.453, namely 65536*0.453 = 29743 = 0x742F. SRK should be loaded before initializing the Function Block.

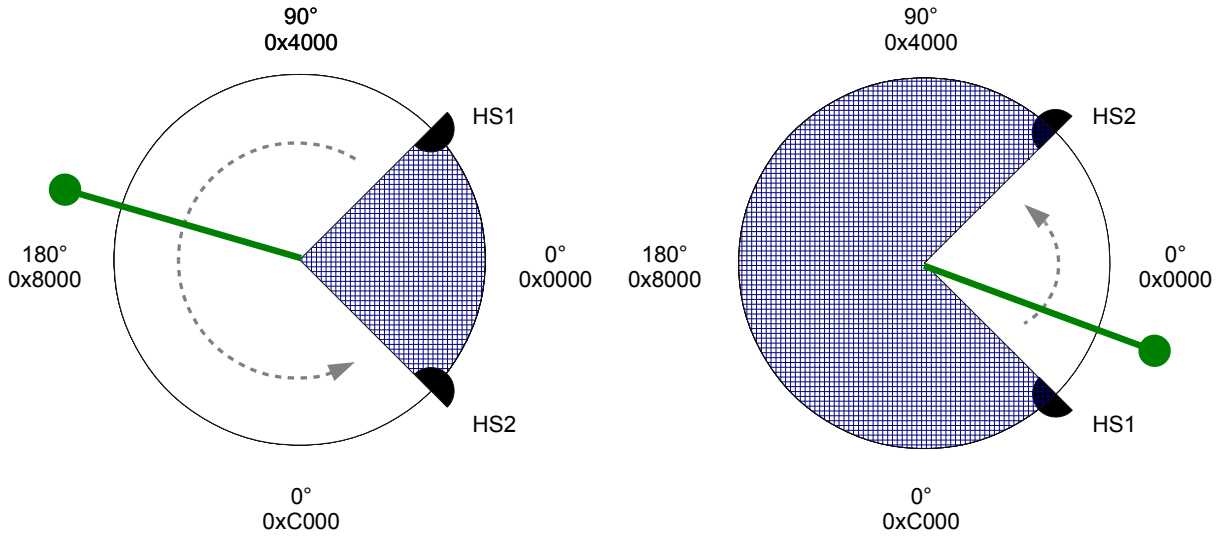
11.2.10 SRP Register (RW)

The SRP register programs the delay of the two (resolver) or three (synchro) output channels. This uses the same scale and units as the DLYn register. Note, however, that this does not change the contents of the DLYn register. When the function block is cleared the channel's delay will return to the value set by its DLY register.

11.2.11 Hard stop registers HS1 and HS2 (RW)

The hard stop registers define a single cut-out region for the function block wherein angles will not be simulated. These hard stops will only be implemented while the function block is in MOVE_HARD_STOP mode. HS1 and HS2 are read only during initialization.

The cut-out region is the region in which HS2 is clockwise from HS1, using the convention that "clockwise" is the direction of decreasing angles. In the two figures below, the cut-out region is shaded in. While the function block is in MOVE_HARD_STOP mode, the actual position will not pass through the shaded cut-out region. See section 11.2.3.6.



In the special case that TP is the same value as a hard stop register, it is at the *boundary* of the cut-out region but not inside it; AP will reach TP in this case.

If HS2 and HS1 are equal, the cut-off region has a size of zero. In this case, every value of TP is considered valid, but AP will use the direction that does not cross over the hard-stop position.

The scaling for HS2 and HS1 is the same as with the other positional registers: 0x0000 is for zero degrees and 0xFFFF is for 359.995 degrees. The MS bit represents 180 degrees and the LS bit represents 0.0055 degrees. Users may treat these registers as signed, covering the range of -180 to +179.995 degrees.

11.2.12 AP Register (RO)

The AP register displays the current simulated angular position of the synchro or resolver. If the function block is in INITIALIZE or IDLE mode, then AP displays what the first simulated angular position will be upon entering a MOVE_* or SPIN_* mode. The scaling is 0x0000 for zero degrees and 0xFFFF for 359.995 degrees. The MS bit represents 180 degrees, and the LS bit represents about 0.0055 degrees, or about 0.33 minutes. Users may treat these registers as signed, covering the range of -180 to +179.995 degrees.

11.2.13 BRK Registers (RW)

A function block can simulate a “broken” coil by dividing a channel’s output by values determined by the BRK registers. If the MSB of a BRK register is set, then its 17 LSBs will be read as an unsigned scalar value from zero to 10000. Each count is 0.01 percent; 10000 is 100 percent. If the value is greater than 10000 then 100 percent will be used.

If the MSB of a BRK register is not set, then it will be ignored.

For a synchro function block, the BRK_A register is for the A channel, the BRK_B register is for the B channel, and the BRK_C register is for the C channel. For a resolver function block the BRK_Y register is for the Y channel and the BRK_X register is for the X channel.

The BRK_n registers are available in Firmware revision E and later.

11.3 LVDT/RVDT Acquisition Function Block

A LVDT/RVDT input Function Block is aimed at a reference I/O channel and at one or two LVDT/RVDT secondary signal acquisition I/O channel. It is similar in most respects to a synchro/resolver acquisition Function Block. It initializes one or two stator/secondary I/O channels and subsequently digitizes their voltages and processes their signals into a linear/angular displacement. This block does not initialize the Reference I/O channel or its optional DDS sine wave source.

The register layout is below. "Offset" is relative to the Function Block start address. The R/W registers marked with a single asterisk (*) will be read only during function block initialization.

Reg Name	**Offset**	**R/W**	**Function**
FUN	0x00	RW	Function Code = 0x03
OPR	0x02	RW	Operation
FLG	0x04	RW*	Setup-time flags
STS	0x06	RO	Real-time status
OVR	0x08	RO	Override control
	. . .		
CP01	0x10	RW*	Channel pointers 0, 1
CP23	0x12	RW*	Channel pointers 2, 3
CP45	0x14	RW*	Channel pointers 4, 5
CP67	0x16	RW*	Channel pointers 6, 7
	. . .		
SRP	0x1A	RW*	Phase Shift
	. . .		
AD	0x22	RO	Actual Displacement
	. . .		
FD	0x26	RO	Filtered Displacement
	. . .		
MSV	0x30	RO	Measured Secondary Voltage

When setting up this Function Block, the recommended sequence is:

Program an I/O channel to generate or to accept the reference voltage.

Clear the FUN, OPR, and FLG words.

Write all operating parameters, including channel pointers and phase shift.

Write the Flags word FLG.

Write the function code 0x03 to FUN.

Write the "initialize" command 0x01 to the Operation Register OPR.

Offsets 0x32 to 0x3E may be used for scratch registers after the function block has been set up.

11.3.1 FUN Register (RW)

Load FUN with function code 0x03 to enable LVDT/RVDT acquisition.

11.3.2 FLG Register (RW)

The flags word FLG should be loaded by the user before loading FUN.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
									F2	F1	F0	T3	T2	T1	T0

The T3...T0 nibble specifies the device type.

T value	**LVDT/RVDT type**
0x0	ratiometric LVDT/RDVT
0x1	open-wiring LVDT/RVDT
All others	Reserved

The F2...F0 bits specify filtering speed for the measured angular position. If the F value is zero, no filtering occurs for the position, and a 100 turn-per-second cutoff frequency will be used for velocity.

F value	**Cutoff Frequency (Hz)**
0	--
1	1
2	2
3	5
4	10
5	20
6	50
7	100

11.3.3 OPR Register (RW)

The Operations Register OPR accepts action commands.

Write 0x01 to OPR to initialize the Acquisition Block. This will:

Set up the one or two I/O channels which acquire LVDT or RVDT secondary signals.

Set the AD and FD words to zero.

Set the Status Register STS to 0x01, "initialized".

Clear the Operations Register OPR.

Begin acquisition.

11.3.4 STS Register (RO)

The read-only Status Word STS reflects real-time acquisition status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SE	EE	CE				OR								IN

The IN bit indicates that the Acquisition Block has been initialized and is operating.

OR will be set if the block is in Override mode, namely if the override register OVR is nonzero. In this case, the actual LVDT/RVDT displacement is not acquired and an override displacement is loaded into Actual Displacement AD. For input blocks like this type, override is mainly used for testing.

The upper nibble is error flags. They are

CE Configuration Error

EE Excitation Error; this bit is set if the excitation voltage is too low, specifically less than 1 volt RMS using 1:1 transformers.

SE Signal Error; this bit is set if the measured secondary voltage is below 100 mV or if there is an ADC clipping error on one of the function block's secondary channels.

11.3.5 OVR Register (RO)

The Override Word **OVR** is loaded by an Override Block.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B3	B2	B1	B0						R6	R5	R4	R3	R2	R1	R0

If the R field is nonzero, R6:R1 is an index to a word in the Rnn register file that defines the override displacement. Normal acquisition is suspended and the Rnn value is loaded into displacement register AD**.** The index R6:R0 is the byte offset from R0 (0x80) to the override displacement word. Bit 0 should always be 0. The filtered displacement FD will follow the AD value.

The B field identifies which Override Block loaded OVR. Since four Override Blocks (OB12 to OB15) are defined, the value will be 12 to 15.

Overrides are mainly used by "position output" type Function Blocks, but are available on input Function Blocks for testing or special applications.

11.3.6 Channel Pointer Registers (RW)

LVDT/RVDT Function Blocks use the CP01 and CP23 channel pointer words to assign their I/O channels.

CP01 is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			R4	R3	R2	R1	R0								

Where the R bits are encoded 0 through 23 to name the reference I/O channel, the channel that generates the reference voltage (for internal excitation) or that accepts the reference (for external excitation.) The excitation winding leads are connected to this I/O channel.

CP23 for ratiometric LVDTs/RVDTs is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			A4	A3	A2	A1	A0				B4	B3	B2	B1	B0

Where the A bits are encoded 0 through 23 to name the A-channel input, and the B bits name the B channel. “A” and “B” channels are as described in section 9.1.

CP23 for open-wire LVDTs/RVDTs is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			A4	A3	A2	A1	A0								

Where the A bits are encoded 0 through 23 to name the single-channel input.

11.3.7 SRP Register (RW)

The SRP register programs the DLYn delay of the one or two input channels. This uses the same scale and units as the DLYn register. Note, however, that this does not change the contents of the DLYn register. When the function block is cleared the channel’s delay will return to the value set by its DLY register.

11.3.8 Displacement Registers (RO)

The AD register reports the fast (unfiltered) displacement of the LVDT or RVDT. The scaling is fractional, in the range of 0x8000 (-1 times maximum displacement) to 0x7FFF (+0.99997 times the maximum displacement).

For a ratiometric LVDT, the AD register reports maximum displacement in a direction when an input channel's amplitude is zero and the other channel's input amplitude is double its zero-displacement amplitude. AD reports a positive displacement when the A channel's amplitude is greater than the B channel's amplitude.

The FD register is the filtered version of AD. It responds slower than AD and reduces displacement noise. The response speed is selected by the F field in FLG.

11.3.9 MSV Register (RO)

MSV is the measured secondary voltage. For a ratiometric LVDT, it is the sum of the A-channel plus the B-channel input voltages. For an open-wire LVDT, it is the A-channel voltage. The scaling is 1 millivolt per LSB. The MSV register does not calculate the transformer ratio.

11.4 LVDT/RVDT Simulation Function Block

A LVDT/RVDT output Function Block is aimed at a reference I/O channel and at one or two LVDT/RVDT secondary signal output I/O channel. It is similar in most respects to a synchro/resolver simulation Function Block. It initializes one or two stator/secondary I/O channels as outputs and subsequently drives their signals to simulate an angular displacement. This block does not initialize the Reference I/O channel or its optional DDS sine wave source.

The register layout is below. "Offset" is relative to the Function Block's start address. The R/W registers marked with a single asterisk (*) will be read only during function block initialization.

Reg Name	**Offset**	**R/W**	**Function**
FUN	0x00	RW	Function Code = 0x04
OPR	0x02	RW	Operation
FLG	0x04	RW*	Setup-time flags
STS	0x06	RO	Real-time status
OVR	0x08	RO	Override Word
	. . .		
CP01	0x10	RW*	Channel pointers 0 (MS byte) , 1 (LS byte)
CP23	0x12	RW*	Channel pointers 2, 3
CP45	0x14	RW*	Channel pointers 4, 5
CP67	0x16	RW*	Channel pointers 6, 7
SRK	0x18	RW*	K amplitude scalar
SRP	0x1A	RW*	Phase Shift
	. . .		
AD	0x22	RO	Actual Displacement
	. . .		
TD	0x26	RW	Target Displacement
TV	0x28	RW	Target Velocity
	. . .		
BRK_LA	0x2C	RW	Coil error simulation register
BRK_LB	0x2E	RW	Coil error simulation register

When setting up this Function Block, the recommended sequence is:

Program an I/O channel to generate or to accept the reference voltage.

Clear the FUN, OPR, and FLG words

Write all operating parameters, including channel pointers, flags, phase shift, and initial TP position

Write the function code 0x04 to function register FUN

Write the "initialize" command 0x01 to the Operation Register OPR

Wait for OPR to clear and check that there are no error flags in the status register STS.

To start simulated displacement, write 2 to OPR.

11.4.1 FUN Register (RW)

Load FUN with function code 0x04 to enable LVDT/RVDT simulation.

11.4.2 FLG Register (RW)

The Flags Word FLG should be loaded by the user before loading FUN.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		S1	S0				X2					T3	T2	T1	T0

The T3...T0 nibble specifies the device type.

T value	**LVDT/RVDT type**
0x0	ratiometric LVDT/RVDT
0x1	open-wiring LVDT/RVDT
All others	Reserved

The X2 bit, if set, enables the output DACs for the channels simulating A and B windings to be scaled by a multiple of 2. This can be used with the SRK register to simulate stepping up the secondary voltage.

The S1:S0 bits specify the smallest time interval for simulating the slew operation (see sections on OPR register and TV register, below). These bits apply to units with firmware revision D or later. Units with earlier firmware will ignore these bits.

S value	**Smallest Time Interval**	**TV LSB (amount of full span per second)**
0 (default)	1 ms	0.0152587
1	10 ms	0.0015259
2	100 ms	0.0001526
3	reserved	reserved

11.4.3 OPR Register (RW)

The Operations Register OPR accepts action commands.

The Operations codes are:

0x00	IDLE	Do nothing; do not output displacement
0x01	INITIALIZE	Initialize and reset to IDLE when finished
0x02	MOVE	Track target displacement

A LVDT/RVDT simulation function block must be initialized by writing ‘1’ to OPR before the MOVE operating mode can be used.

The normal usage of OPR register is to write ‘1’ to initialize the function block, wait for OPR to self-clear (enter IDLR mode), and then write ‘2’ to put the function block into MOVE mode. Normally OPR may be left alone after putting a function block into MOVE mode; however, it can be re-initialized at any time by writing a ‘1’ back into OPR. Simulated displacement will cease while re-initializing a function block.

IDLE (OPR = 0)

Users are not expected to set an initialized function block into IDLE mode directly, except before writing the FUN register. This mode is set automatically by the self-clearing INITIALIZE mode.

While in IDLE mode, the function block waits for OPR to be set to MOVE. No simulated output will occur at any displacement, and overrides will not be processed.

INITIALIZE (OPR = 1)

Write 0x01 to OPR to initialize the Simulation Block. This will:

Set up the one or two I/O channels which generate simulated LVDT or RVDT secondary signals.

If SRK is zero, set SRK to 0x8000.

Set the Status Register STS to 0x01, "initialized".

Clear OPR.

MOVE (OPR = 2)

Writing 0x02 to OPR will cause the AD simulated displacement to slew towards the target displacement TD at the specified target velocity TV. The operation command code will remain in OPR. A VME user can write TD and TV any time. The function block will process changed values within the number of milliseconds determined by the “slow” S bits in the FLG register.

MOVE mode is not self-clearing.

11.4.4 STS Register (RO)

The read-only Status Word STS reflects real-time acquisition status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		EE	CE				OR								IN

The IN bit indicates that the Simulation Block has been initialized and is operating.

OR will be set if the block is in Override mode, namely if the OVR register is nonzero.

The upper nibble is error flags. They are:

CE Configuration error

EE Excitation error, this bit is set if the excitation voltage is too low, specifically less than 1 volt RMS using 1:1 transformers.

11.4.5 OVR Register (RO)

The OVR Override Word is loaded by an Override Block; see section 12.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B3	B2	B1	B0						R6	R5	R4	R3	R2	R1	R0

If the R field is nonzero, R6:R1 is an index to a pair of words in the Rnn register file that define the override position and override velocity in that order. The simulated displacement AD ramps to the override displacement at the override velocity. The index R6:R0 is the byte offset from R0 (0x80) to the override displacement word. Bit 0 should always be 0.

The direction of override motion depends on the values of the override displacement and the current displacement. The override velocity is unsigned and the simulated output will not cross the -1/+1 threshold.

The B field identifies which Override Block loaded OVR. Since four Override Blocks (OB12 to OB15) are defined, the value will be 12 to 15.

11.4.6 Channel Pointer Registers (RW)

LVDT/RVDT Function Blocks use the CP01 and CP23 channel pointer words to assign their I/O channels. The F bits in the CP registers discussed below apply to units that have firmware revision D or later. Units with earlier firmware revisions will ignore these bits.

CP01 is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			R4	R3	R2	R1	R0								

Where the R bits are encoded 0 through 23 to assign the reference I/O channel, the channel that generates the reference voltage (for internal excitation) or that accepts the reference (for external excitation.) The excitation winding leads are connected to this I/O channel.

CP23 for ratiometric LVDTs/RVDTs is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FA			A4	A3	A2	A1	A0	FB			B4	B3	B2	B1	B0

Where the A bits are encoded 0 through 23 to name the A-channel input, and the B bits name the B channel. These correspond to the “A” winding and “B” winding discussed in section 9.1. If set, the FA and FB bits flip the output polarity of the A and B channels, respectively, effectively offsetting their phase 180 degrees.

CP23 for open-wiring LVDTs/RVDTs is:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FA			A4	A3	A2	A1	A0								

Where the A bits are encoded 0 through 23 to name the single-channel secondary. If set, the FA bit flips the polarity of the A channel, effectively offsetting its phase 180 degrees.

11.4.7 SRK Register (RW)

The SRK register scales down the reference voltage to the simulated secondary voltage outputs. For example, you can simulate the 3:4.25 step-up ratio of the Lucas/Schaevitz model discussed in section 9.2 by setting the X2 bit in the FLG register and then setting the SRK register to 0xB333 (derived from 65536 * 4.25V / (2 * 3V)). SRK should be written before initializing the Function Block.

11.4.8 SRP Register (RW)

The SRP register programs the delay of the one or two output channels. This uses the same scale and units as the DLYn register. Note, however, that this does not change the contents of the DLYn register. When the function block is cleared the channel’s delay will return to the value set by its DLY register.

11.4.9 Displacement Registers (RW)

The TD register sets the simulated displacement of the LVDT or RVDT. The scaling is fractional, in the range 0x8000 (-1 times the maximum displacement) to 0x7FFF (+0.99997 times the maximum displacement).

For a ratiometric LVDT, a “maximum displacement” means that one secondary outputs zero volts and the other secondary outputs double its zero-displacement voltage. For positive displacement, the Simulation Block will increase the A channel and decrease the B channel.

The AD register holds the current simulated displacement. It has the same units as the TD register.

TV represents the unsigned 16-bit value that is added to AD to ramp toward the target displacement TD, when the OPR register is set to 0x0002. The output path will not cross the -1/+1 boundary as with the synchro/resolver Function Block, so the direction is determined already by the values of AD and TD.

TV has the same units as its corresponding register in the synchro/resolver Function Block, except that it is always unsigned, and the MSB is always used. A value in TV that is larger than the difference between TD and AD has the same effect of an instantaneous jump in position. As with the Synchro/Resolver Function Blocks, the TV register’s LSB is affected by the S bits in the FLAG register.

11.4.10 BRK Registers (RW)

A function block can simulate a “broken” coil by dividing a channel’s output by values determined by the BRK register. If the MSB of a BRK register is set, then its 17 LSBs will be read as an unsigned scalar value from zero to 10000. Each count is 0.01 percent; 10000 is 100 percent. If the value is greater than 10000 then 100 percent will be used.

If the MSB of a BRK register is not set, then it will be ignored.

The BRK_LA register is for the LVDT A channel and the BRK_LB register is for the LVDT B channel.

The BRK_n registers are available in Firmware revision E and later.

12. Override Blocks

There are four Override Blocks, OB12 to OB15, each 32 words long. An Override Block can be programmed to sense a switch closure or a watchdog timer rundown and load the OVR override word registers of up to twelve Function Blocks.

Override Block OB12 has the lowest override priority and Override Block OB15 has highest priority.

All four Override Blocks are executed periodically if enabled. When a block is run, its specific input condition (a switch or a watchdog timeout) is tested. If the exception condition is true, the block is "tripped" and the OV0...OV11 list of twelve override values is scheduled for loading into the OVR override word registers of the twelve respective Function Blocks.

After all four Override Blocks are evaluated, the actual OVR words of the Function Blocks are loaded. If more than one Override Block tries to load OVR in a given Function Block, the highest priority Override Block prevails. If none of the four Override Blocks specifies a nonzero override value, the relevant Function Block OVR word is cleared.

The register layout of an Override Block is below. "Offset" is relative to the Override Block's start address.

Reg Name	**Offset**	**R/W**	**Function**
FUN	0x00	RW	Function Code
OPR	0x02	RW	Operation
FLG	0x04	RW	Flags
STS	0x06	RO	Status
	. . .		
DOG	0x0C	RW	Watchdog Timer
TRG	0x0E	RW	Software override
	. . .		
OV0	0x20	RW	Override value for Function Block 0
OV1	0x22	RW	Override value for Function Block 1
OV2	0x24	RW	Override value for Function Block 2
OV3	0x26	RW	Override value for Function Block 3
OV4	0x28	RW	Override value for Function Block 4
OV5	0x2A	RW	Override value for Function Block 5
OV6	0x2C	RW	Override value for Function Block 6
OV7	0x2E	RW	Override value for Function Block 7

Reg Name	Offset	R/W	Function
OV8	0x30	RW	Override value for Function Block 8
OV9	0x32	RW	Override value for Function Block 9
OV10	0x34	RW	Override value for Function Block 10
OV11	0x36	RW	Override value for Function Block 11

12.1 FUN Register (RW)

To enable an Override Block, load FLG and optionally DOG, then load a function code into the FUN register. The function codes are:

0x00 Block is unused

0x11 Watchdog timer override

0x12 Switch input override

Do not use the "switch input" type Override Block for V545 modules with hardware revision earlier than "C".

12.2 OPR Register (RW)

Write 0x01 to OPR to clear the LAT bit, which cancels latched overrides. OPR will self-clear when this operation is done.

12.3 FLG Register (RW)

Load the FLG register before enabling the Override Block. Fields are:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					TG	INV	LEN					A3	A2	A1	A0

For switch inputs (**FUN** code 0x12) the "A" field is a bitmask that selects which switches are used to trigger an interrupt. A '1' selects the switch.

A code	SWITCH	J3 PIN
A0	SWIN0	2
A1	SWIN1	3
A2	SWIN2	4
A3	SWIN3	5

The override is tripped if the switch is open, namely the pullup voltage at the J3 pin is high. If the INV bit is set, the override is tripped if the switch is closed and the J3 pin is at ground.

If the latch enable LEN bit is set, an override trip will latch. A momentary activation of the override switch, or timeout of the watchdog timer, will set the LAT bit in STS, and LAT will stay true until cleared by the Unlatch operation.

If the TG bit is set, then a non-zero value in the TRG register will force an override condition.

12.4 STS Register (RO)

The read-only STS word reflects real-time Override Block status.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		EE	CE				LAT	TRP							IN

The IN bit indicates that the Override Block is enabled.

TRP indicates that the selected override condition is tripped. That is the case for a switch-type override if the switch closure is in the override state, or if the watchdog has timed out for a watchdog timer type block.

LAT is the latched version of TRP. The LAT bit in STS can go high only if the LEN latch enable bit in the FLG register is high.

If either TRP or LAT is true, the Override Block is tripped and the values of the OVn registers are written to their corresponding Function Block's OVR registers.

To clear the LAT bit, write 0x01 to the OPR register. OPR will self-clear when the unlatch operation is done.

12.5 DOG Register (RW)

The watchdog DOG register is a 16-bit down counter that is used in watchdog-type Override Blocks. It decrements every 4 milliseconds and stops at zero. Before enabling the Override Block by writing watchdog function code 0x11 to FUN, the VME computer should first load this register with a timeout value.

If the DOG word is zero, the TRP bit will be set in the STS register. If the latch-enable LEN bit is set in FLG, the LAT bit will also be set in STS and the timeout trip state will be latched even if the VME computer resumes refreshing DOG.

For example, for a one-second watchdog timeout, the VME computer should regularly write 250 to DOG.

12.6 TRG Register (RW)

If the TG bit in the FLG register is set, then a nonzero value in the TRG register will force an override condition regardless of switch or watchdog state. This register will self-clear after the override is triggered. Use the LEN bit in the FLG register to latch this override.

This register will be ignored if the TG bit in the FLG register is not set.

12.7 OVn Registers (RW)

Each Override Block has twelve Override Values, OV0 through OV11. They correspond to the twelve Function Blocks, FB0 to FB11. If an Override Block is tripped and has, for example, an OV7 value of *X*, then value *X* will be copied into the OVR override register of Function Block number 7, at address 0x05C8.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B3	B2	B1	B0						R6	R5	R4	R3	R2	R1	R0

The meaning of an override word is discussed in greater detail in sections 11.2 and 11.4. In summary, a nonzero override word will cause a Function Block to simulate an override position and velocity while an override condition exists. The override position and velocity are stored in the R0…R63 register file, as pointed to by the R field. The B bits store the Override Block number 12 to 15, to determine priority (but see note below).

All four Override Blocks may try to load the same OVR override word in any Function Block. The highest-numbered Override Block has write priority. If none of the four Override Blocks specifies a nonzero value for a given OVR, that word is cleared.

Any nonzero value of OV*n* will result in OV*n* being copied to Function Block *n*'s OVR register. Since the B field ranges from 12 to 15 instead of 0 to 3, a value of zero for the R bits – pointing to the first register R0 in the Register File – may be used for an override condition.

Note: If OV*n* is nonzero but its B field is incorrect – not the same as the Override Block number – then the correct value of B will be copied instead of OV*n*'s B field, and the correct priority will still be used. The B field is a way of making an OV*n* register non-zero, in case the R field needs to be zero. The R field is never considered invalid.

CAUTION: It is possible for a programmed override to go "the wrong way." The signed-velocity override motion will take the long way around if programmed to go from 2 degrees to 1 degree with a positive velocity. A shortest-path move from +10 to -10 degrees might hit a mechanical stop at 0 degrees. Use extreme care in planning overrides in safety-critical systems. The synchro/resolver Function Block's MOVE_HARD_STOP operating mode was designed for this purpose.

13. Upgrade Procedure

V545 modules with firmware rev. “B” or later can field-reflash using the MACRO and PARAM registers and the register file R0…R63. This is not supported by rev. “A” firmware.

Highland will furnish a file named in the style of “22E545B_upgrade.bin” for field program upgrade.

See section 8 for a detailed description of the macros discussed below. The upgrade is performed using the MACRO and PARAMn registers, and the R0…R63 register file. Throughout the following procedure, the MACRO register should be checked for an error (non-zero) value each time its MS bit clears after executing a macro.

Execute the Flash Unlock macro (0x8408) and wait for the MS bit of the MACRO register to clear.

Execute the Flash Erase macro (0x8409) and wait for the MS bit of the MACRO register to clear. This may take up to 25 seconds.

Once the upgrade region is erased, perform the following loop:

Read a 128-byte page from the binary file and write it sequentially into the R0 to R63 registers, in little-endian format (see section 8.5).

Write the page number to the PARAM0 register. Write zero for the first page of the file, incrementing by one for each pass of this loop.

Write the Flash Write macro (0x840A) to the MACRO register and wait for the MS bit to clear.

Optional: verify that the page was correctly written. With the same page number in the PARAM0 register, execute the Read Flash macro (0x8410), wait for the MS bit of the MACRO register to clear. R0…R63 now hold data read back out of the flash, in little-endian format (see section 8.8). Compare this data to the data that you intended to write.

Repeat the loop for each page of the binary file, incrementing PARAM0 for each 128-byte page, until the end of the binary file is reached. It is okay if the final page does not equal 128 bytes; write it anyway.

Optional: execute the Checksum Flash macro (0x840B) to determine if the re-flash procedure was successful. The UP and UF fields of the PARAM1 register (see section 8.6) should both be 01 binary, “checksum okay”. If not, the re-flash procedure has failed. A reset will result in the factory image being loaded. If you choose to restart this procedure, the flash must be erased again with the Flash Erase macro before writing to it.

Execute the Reset macro (0x8407) for the upgrade to be complete. After resetting, the STATE register (see section 7.2) will show upgrade status.

14. Versions

V545-1	24-channel VME synchro/LVDT simulation/acquisition module with 1:1 transformers
V545-6	24-channel VME synchro/LVDT simulation/acquisition module with 1:5.3 transformers

15. Customization

Consult factory for information on additional custom versions.

16. Hardware and Firmware Revision History

16.1 Hardware Revision History

Revision E Jun 2017
Improved manufacturability
Functionally equivalent to Revision D

Revision D Feb 2014
Made D9 connector thru-hole

Revision C Jul 2013
Added TTL D9 connector for contact closure I/O capability
Modified front panel

Revision B Mar 2012
Improved channel filters and fixed silkscreen
Shipped with firmware 22E545A

Revision A Feb 2012
Initial PCB release
Shipped with firmware 22E545A

16.2 Firmware Revision History

Standard firmware is 22E545.

Revision F Feb 2017
Fixed bug in calibration.

Revision E Jan 2017
Added hard stops and additional functionality to synchro/resolver simulation function blocks.
Added function blocks 5 and 6 to replace function blocks 1 and 2.
Corrected phase handling in LVDT function blocks.

Revision D Aug 2014
Added S bit to simulation function block FLG registers; added F bits to simulation function block CP registers.

Revision C Aug 2014
Fixed bug that incorrectly implemented negative amplitudes.

Revision B Nov 2013
Added support for re-flashing, function blocks, override blocks, and D9 switch enclosure
Added macros for flash access and synchronizing PSD's and DDS's

Revision A	Mar 2012 Initial firmware release For revision A and B hardware only

17. Accessories

Additional transformers can be purchased to replace supplied transformers. Factory recalibration is recommended if transformers are replaced.

V548-1 small signal 1:1 730MH plugin transformer

V548-6 small signal 1:5.3 750MH plugin transformer

Changes

June 7, 2013: Defined filter steps, sec 10.1

August 26, 2013: Modified D9 connector description, section 4.3. Removed mention of Channel Error, sec. 5.1. Added SWIN/SWOUT to register map, sec. 6.1 & 7.5. Extended MACRO documentation, chapter 8. Removed the otherwise undocumented STATE register from function block register map, chapter 11 & 12. Documented filter cutoffs, chapter 11. Moved upper-byte channel pointer's LSB from 9 to 8, chapter 11. Added chapter on reflashing, chapter 14

October 1, 2013: Added description of the LVDT/RVDT function blocks. Added documentation for the READ FLASH macro. Cleaned up formatting, spelling, unclear statements, etc. Corrected chapter 10 in the table of contents.

October 3, 2013: Rearranged chapters 8 and 14 so that chapter 8 discusses macros all in one place, and chapter 14 focuses on reflash procedure.

October 8, 2013: Reformatted headings, tables, etc., to take after HTI's template for manuals. Rewrote the part of 4.3 concerning J3, the D9 switch enclosure. Changed 60-Hz lower frequency limit to 250 Hz. Started new final chapter on Module Versions, separate from upgrade procedure.

October 25, 2013: Corrected errors, renamed AOUT to SWOUT, embellished use of channel control blocks for LVDT acquisition, added documentation of dash 6 transformers, added hardware versions and history.

November 25, 2013: Changed specifications page to reflect tests run on dash 6 transformers. Corrected statements about dash 6 transformers; they are calibrated to have a 5.3:1 ratio. Removed incorrect statement about channel pointers; they may only directly reference channels, not DDS's.

January 16, 2014: Revised versions, customization, hardware and revision history, and accessories. Added wiring diagrams to section 9.2.

March 26, 2014: Clarified some contents based on customer recommendations; some alterations in section 11's section numbers have resulted from this. Corrected small mistakes in function block register descriptions, in particular that they do not affect contents of channel control block R/W registers. Changed the pin-out of the D-9 connector to reflect rev. D hardware change.

May 12, 2014: Added RW/RO to end of register detailed descriptions. Mentioned need for amplifier for output excitation channels. Added dash-6 qualifier for accuracy specification.

August 6, 2014: Added slow bits and flip bits to the simulation function blocks.

September 8, 2014: Fixed out-of-date J3 table on page 70. Clarified A bits in the override block's flag register.

September 11, 2014: Large changes to 11.2 and 11.4, simulation function blocks; added hard stops to synchro/resolver function blocks.

September 16, 2014: Made corrections to section 11.2 regarding invalid TP; removed hard-stop limitations; corrections to introduction; expanded the general introduction to Function Blocks at the start of section 11.

October 28, 2014: Added description of macro to read power supplies; defined BISS register.

February 5, 2015: Added BRK register description.

February 13, 2015: Embellished meaning of signal error in function block STS registers.

March 12, 2015: Added TRG register and FLG register's TG bit in override block.
May 21, 2015: Added BRK_n registers to the simulation function blocks.
January 6, 2017: Added function blocks 5 and 6, deprecated function blocks 1 and 2, removed menion of unused BISS register, made corrections to channel pointer registers.
January 23, 2017: Corrected -6 transformer Zout, preparing as V545MAND3
February 7, 2017: Added Rev F firmware in revision history.
February 15, 2019: Changed delay information: "The low 10 bits...range of 0 to 4.095" was changed to say "9 bits" instead of "10 bits" and "2.044" instead of "4.095". Updated for Rev E hardware.

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