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HIGHLAND TECHNOLOGY, INC.

MODEL V660
12-CHANNEL VME TIME-TO-DIGITAL CONVERTER
TECHNICAL MANUAL

September 22, 2010

Highland Technology, Inc, 18 Otis Street, San Francisco, CA 94103 USA
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1. Introduction

The V660 is a 12-channel time-to-digital converter VME module. It accepts digital logic level inputs and measures the time-of-edge of each input. It is capable of independent timestamping of all 12 channels

The V660 captures events to 32-bit resolution. The basic time measurement unit is 24.4140625 picoseconds, the equivalent of measuring events using a 40.96 GHz clock, for a maximum time span of 104.8 milliseconds. Users may elect to reduce resolution in steps to as coarse as 1.5625 nanoseconds, extending the maximum time range to as much as 6.71 seconds.

The architecture of the V660 is quite flexible, with all logic being implemented in two Xilinx FPGA chips. Custom versions can be designed to extend time ranges, provide event logic, or implement special gating or processing procedures.

The main VME board includes the 12 time stampers and event processing logic. User inputs are processed by a mezzanine board. The mezzanine provides input connectors, input signal conditioning, fast gating and routing, and other application-specific functions. Various mezzanines are available for specific applications.

This manual applies to versions...

V660-1 Highland part number 22A660-1B, equipped with differential ECL mezzanine

V660-2 Highland part number 22A660-2B, equipped with optical-input mezzanine



1 V660-1



V660-2

2. Specifications

Unless noted, the following specifications refer to the V660-1 version.

FUNCTION	12 channel VME TDC/timestamp module.
PACKAGING	Single-wide, 6U VME module.
VME MODES	A24:A16:D32:D16:D08(EO). Address mode and bus address are dipswitch selectable. Responds to hex address modifiers 29 and 2D in 16-bit mode, or 39 and 3D in 24-bit mode. VME cycle response time (DS* to DTACK*) averages 150 ns.
INPUTS	V660-1 version: 12 logic-level front-panel inputs; channels are named T0 through T11. The V660-1 accepts differential ECL positive-edge triggers, and terminates 100 ohms differentially. One differential ECL Gate input. One TTL Gate input. One general-purpose TTL logic I/O. V660-2 version: Eight ST-connectorized 850 nm optical inputs, timestamp channels 1-5 and 7-9. Two TTL/CMOS timestamp inputs, channels 10 and 11 One TTL gate input
TIMING	Measures time-of-edge of each of the 12 timing inputs. User-selectable LSB values are: 24.4140625 ps (40.96 GHz clock equivalent) 97.65625 ps (10.24 GHz) 390.625 ps (2.56 GHz) 1562.5 ps (0.64 GHz) with 32-bit range (effective clock speeds of 40.96, 10.24, 2.56, and 0.640 GHz). Times are reported as absolute timestamps relative to the MCH:MCL master counter. The master timestamp counter may be read and reset from the VME bus. The V660 will timestamp all edges on any given channel if separated by at least 160 ns. Average event rate is limited by VMEbus unload of event FIFO memory. Alternate mezzanine modules provide for other signal levels, multihit and

	pingpong modes, fast gating, and other features. Jitter is defined as the statistical variation of times measured as the difference between two timestamps on a single channel or across channels. Jitter is below (0.75 LSB + 65 ps + timebase jitter) RMS, where timebase jitter is a function of the measured time interval. Channel-channel skew is below 200 ps. Statistical linearity is better than 0.25 LSB.
MEMORY	Each channel includes a 256-sample FIFO memory. An associated control/status register indicates number of samples in each FIFO, overrun status, and allows FIFO management. Per-channel FIFO data may be read from a single address or from a block of 256 longwords/channel, allowing sequential-read block transfers.
CLOCK	Internal TCXO timebase, ±1 PPM accuracy. Timebase jitter is below (2e-9 x measured delay RMS. The module includes provision for phase-locking to another V660 or to an external 10 MHz reference.
LOGIC	Internal logic is implemented with a reprogrammable FPGA, allowing field-upgradeable customization of functions and interface. The V660 may also be used to trigger external events and generate associated time-acquisition gates.
RAM	The V660 is optionally available with up to eight megabytes of fast static RAM usable for histogramming, event buffering, or construction of 2-d images from delay-line detectors.

3. Theory of Operation

3.1 General Architecture

Figure 1 is the overall block diagram of the V660 TDC module.

The V660 module includes the following:

1. MICROPROCESSOR — A 32-bit Motorola MC68332 embedded CPU supervises module operations. Embedded processor code is stored on a replaceable EPROM chip; this same chip holds the FPGA (gate array) logic chip configuration data, allowing hardware and software upgrades in the field.
2. VME INTERFACE — An FPGA-based interface is used, implementing a bank of 32-bit VME memory locations accessible both from the VME bus and from the internal logic.
3. MAIN FPGA — A Xilinx XC2S400 chip performs timestamp processing and FIFO buffering.
4. CLOCKS — An internal 40 MHz crystal oscillator is the internal clock source. Long-period time measurements are limited in accuracy by the phase noise and drift of this oscillator. The oscillator may be phase-locked to an external 10 MHz source, and one V660 may be used as the master to which other modules are locked.
5. TIME STAMPERS — The V660 uses 12 front-end timestamp circuits to acquire incoming events. Incoming rising edges are accepted from the signal-conditioning mezzanine board and applied to the clock input of a d-type flipflop. The enable of this flipflop is derived from the gating logic for this channel, such as to allow inputs to be qualified by external conditions.

   When the 'hit' flipflop is triggered, it enables a vernier time-measurement circuit which measures the time difference from the nearest 40 MHz clock edge; this difference is passed to the timing FPGA, which applies calibration factors and concatenates the result onto the coarse (40 MHz, 25 ns) time value generated by the master counter. The result is a 42-bit time stamp with 24.4140625 ps LSB resolution, equivalent to a 40.96 GHz clock; the user-selected 32 bits of this value are the reported timestamp.

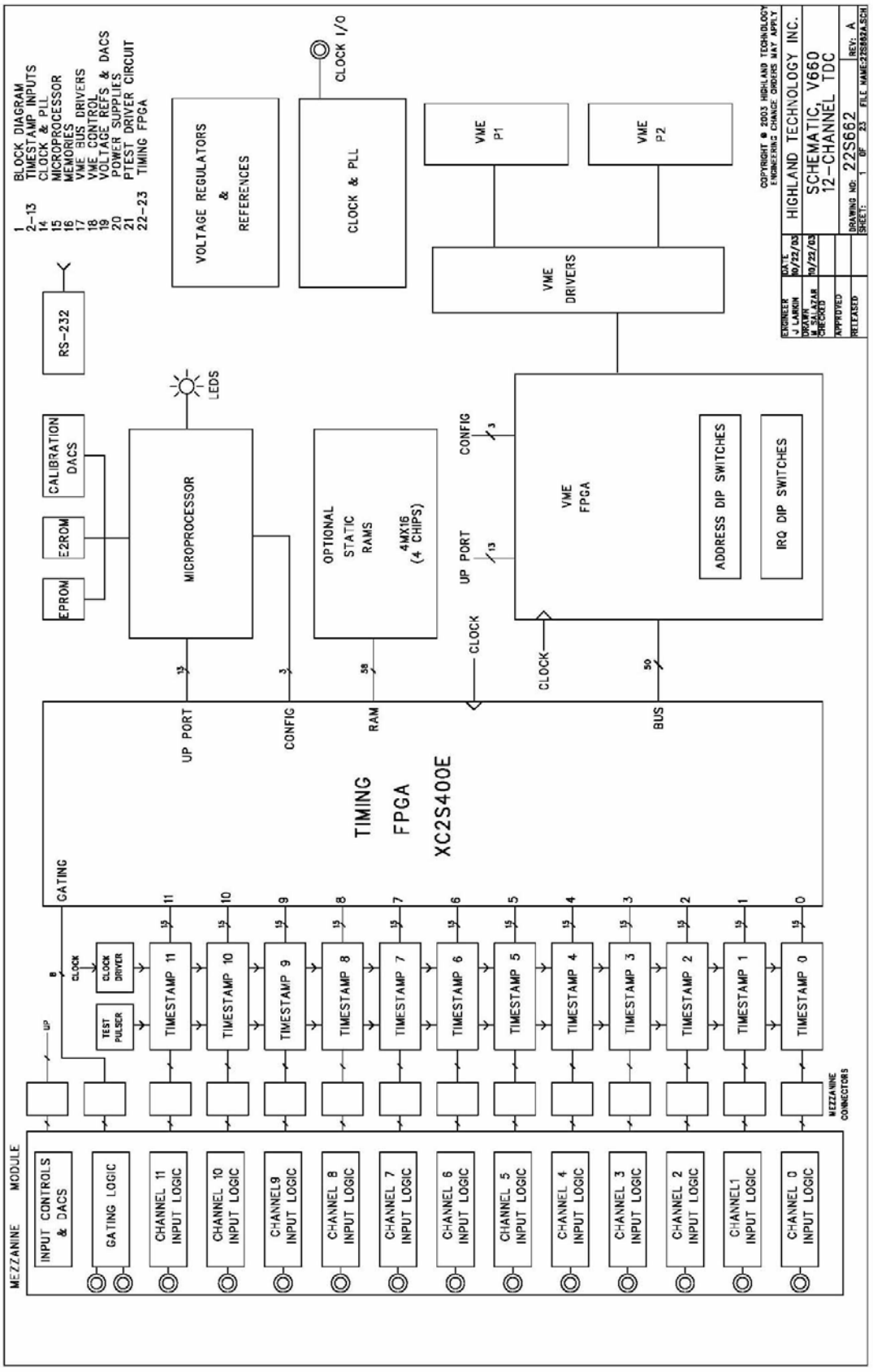
   The FPGA logic resets the hit flipflop and vernier measurement circuit, and re-arms for the next event, within 160 ns.
6. POWER SUPPLIES — The V660 incorporates a number of linear regulators that condition standard VME power supply voltages for internal use. These regulators generate heat, which could degrade time measurement accuracy. The module is designed so that proper VME slot airflow, from bottom to top along the full length of the module, will ensure proper heat transfer.

7. MEZZANINE MODULE

The V660-1 incorporates the V664-1 input mezzanine module, capable of accepting differential ECL inputs. This mezzanine may be optionally configured for LVDS signal levels, as the V660-3

The V660-2 is the optical input version.

Figure 1


BLOCK DIAGRAM
1 TIMESTAMP INPUTS
2-13 CLOCK & PLL
14 MICROPROCESSOR
15 MEMORIES
16 VME BUS DRIVERS
17 VME CONTROL
18 VOLTAGE REFS & DACS
19 POWER SUPPLIES
20 PTEST DRIVER CIRCUIT
21 TIMING FPGA
22-23
RS-232
VOLTAGE REGULATORS & REFERENCES
CLOCK & PLL
CLOCK I/O
VME P1
VME P2
VME DRIVERS
LEDS
CALIBRATION DACS
E2ROM
EPROM
MICROPROCESSOR
OPTIONAL STATIC RAMS 4MX16 (4 CHIPS)
CONFIG
UP PORT
VME FPGA
ADDRESS DIP SWITCHES
IRQ DIP SWITCHES
CLOCK
CLOCK
UP PORT
CONFIG
RAM
BUS
GATING
TIMING FPGA XC2S400E
UP
CLOCK
TEST PULSER
CLOCK DRIVER
TIMESTAMP 11
TIMESTAMP 10
TIMESTAMP 9
TIMESTAMP 8
TIMESTAMP 7
TIMESTAMP 6
TIMESTAMP 5
TIMESTAMP 4
TIMESTAMP 3
TIMESTAMP 2
TIMESTAMP 1
TIMESTAMP 0
MEZZANINE MODULE
INPUT CONTROLS & DACS
GATING LOGIC
CHANNEL 11 INPUT LOGIC
CHANNEL 10 INPUT LOGIC
CHANNEL9 INPUT LOGIC
CHANNEL 8 INPUT LOGIC
CHANNEL 7 INPUT LOGIC
CHANNEL 6 INPUT LOGIC
CHANNEL 5 INPUT LOGIC
CHANNEL 4 INPUT LOGIC
CHANNEL 3 INPUT LOGIC
CHANNEL 2 INPUT LOGIC
CHANNEL1 INPUT LOGIC
CHANNEL 0 INPUT LOGIC
MEZZANINE CONNECTORS
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ENGINEERING CHANGE ORDERS MAY APPLY
HIGHLAND TECHNOLOGY INC.
SCHEMATIC, V660
12-CHANNEL TDC
DRAWING NO: 22S662
REV: A
SHEET: 1 OF 23
FILE NAME:22S662A.SCH

4. Front-Panel Connectors and LEDs

4.1 V660-1 ECL Input Version

4.1.1 Timestamp Input Connector

All 12 timestamp inputs are accepted at J1, a 50-position "SCSI II" female connector located on the mezzanine module. The connector used internal to the V660 mezzanine module is the Kycon K77-50S-WL or equivalent. A typical input cable assembly might be the SPC Corp. SPC10516.

J1 pinout is as follows:

CHANNEL	+ INPUT	- INPUT
0	24	49
1	22	47
2	20	45
3	18	43
4	16	41
5	14	39
6	12	37
7	10	35
8	8	33
9	6	31
10	4	29
11	2	27
GATE2	1	26

All inputs are differential ECL. A 100-ohm line-to-line terminator is provided on each input pair, but no ECL pulldowns are provided. Event time is defined as the rising edge of a "+ INPUT" pin.

The GATE2 input may be used as an enable for the 12 event inputs; see Section 5.13.1.

All other pins on this connector are grounded to the VME circuit ground. The shield/shell of J21 is grounded to the module front panel.

4.1.2 Clock I/O

A front-panel SMB connector is provided for clock I/O. It may be user-programmed as a 10 MHz output, a 10 MHz input, or may be disabled.

When used as an output, a 10 MHz TTL signal is provided at the CLOCK connector. This is 1/4 of the internal 40 MHz clock frequency.

When used as an input, the CLOCK connector accepts a 10 MHz sine, square, or TTL input of at least 1 volt p-p, and locks the module 40 MHz oscillator to this input. The input must be 10 MHz ±4 PPM to ensure lock. See section 5.7 regarding clock control register bits.

4.1.3 Gate1 Input

A front-panel SMB connector accepts a TTL-level gate input. Any timestamp channel can be programmed to use this as a trigger qualifier. This input is terminated in 50 ohms to ground, and has a nominal threshold of about +1.4 volts.

4.1.4 LEDs

The V660-1 has a single front-panel LED, labeled VME. It flashes whenever the module is accessed from the VME bus.

Three additional LEDs are located on the PCB surface. A red led blinks at about 1 Hz as the CPU 'heartbeat'. A green LED indicates that the VME FPGA is successfully configured, and an amber LED indicates that the timing FPGA is configured.

4.2 V660-2 Optical Input Version

4.2.1 Optical Timestamp Input Connectors

Eight optical pulse inputs are provided on the front panel. The connectors are multimode ST fiber types, intended for use at 850 nm with optical power levels in the 1 mW range. The module timestamps the rising edge of a light pulse on timestamp channels 1, 2, 3, 4, 5, 7, 8, and 9.

Optical trigger threshold is set by the OPTO THR trimpot on the top of the mezzanine board. Test point TP12 indicates the threshold setting, scaled 1 volt per milliwatt. The factory setting is 300 mV at the test point, corresponding to a threshold of 300 uW, the preferred trigger level for optical inputs in the 800 uW-1.2 mW range.

4.2.2 Electrical Timestamp Input Connectors

Two electrical inputs are also provided, timestamped on channels 10 and 11. Each input is positive-edge triggered, with threshold set by the ELEC THR pot and measurable at test point TP9. These inputs are terminated with 50 ohms to ground. Standard connectors are SMB types.

Timestamp channels 0 and 6 are not used on the V660-2 version, but are present on the main board and operate in PTEST self-test mode.

4.2.3 Gate Input Connector

One GATE input is provided. This is a TTL/CMOS level, as described in section 4.1.3.

5. VME Register Map and Programming

The following is a summary of the VME-accessible registers on the V660-1 module; registers are shown as 16-bit unless otherwise noted. Thirty-two bit values are high-endian, with the most significant data at the lowest bus address.

The module occupies 512 bytes in the VME address space, and may be used in the user-selectable "bigmap" mode, expanding the address space to 16 Kbytes. Bigmap mode allows fast readout of timestamp FIFO data using sequential-read operations.

Switches on the module set the base address, anywhere in the 24-bit or 16-bit VME address spaces.

REG # below is the ordinal register number in decimal; OFFSET is the hex VMEbus offset from the module base address.

REG NAME	REG#	OFFSET	FUNCTION
VXI MFR	0	0x00	VXI manufacturer ID : always 65262, FEEE hex.
VXITYPE	1	0x02	Module type, always 22660, 5884 hex.
VXI STS	2	0x04	VXI status register.
ROM ID	4	0x08	Firmware ROM ID, typically 22660 decimal.
ROM REV	5	0x0A	Firmware ROM revision, typically ASCII 'A'.
MCOUNT	6	0x0C	Microprocessor update counter.
SETUP	8	0x10	Basic module control/setup register.
RESETS	9	0x12	Channel resets register.
FLAGS	10	0x14	Channel hit flags.
ENABLES	11	0x16	Channel VME enables.
MCH	12	0x18	Master counter, MS 16 bits.
MCL	13	0x1A	LS 16 bits.
FHIT	16	0x20	FIFO hit (not empty) flags.
FHALF	17	0x22	FIFO half-full flags.
FHIGH	18	0x24	FIFO 3/4 full flags.
FOVER	19	0x26	FIFO overflow flags.
FZAP	20	0x28	FIFO resets.

ICTL	24	0x30	Interrupt control.
IEN	25	0x32	Interrupt enable bits.
IFLG	26	0x34	Interrupt flags.
IVEC	28	0x38	Interrupt vector.

Channel 0 Registers

CC0	32	0x40	Channel control.
FC0	33	0x42	FIFO control/status.
TH0	34	0x44	Time stamp MS 16 bits.
TL0	35	0x46	Time stamp LS 16 bits.
FH0	36	0x48	FIFO output MS 16 bits.
FL0	37	0x4A	FIFO output LS 16 bits.
CAL0	47	0x5E	Channel offset calibration (read-only).

Channel 1 Registers

CC1	48	0x60	Channel control.
FC1	49	0x62	FIFO control/status.
TH1	50	0x64	Time stamp MS 16 bits.
TL1	51	0x66	Time stamp LS 16 bits.
FH1	52	0x68	FIFO output MS 16 bits.
FL1	53	0x6A	FIFO output LS 16 bits.
CAL1	63	0x7E	Channel offset calibration.

(Etc., Channels 2-11, spaced 16 registers, 0x20 bytes, apart.)

UCMD	240	0x1E0	Microprocessor command register.
UP0	241	0x1E2	Command parameters.
UP1	242	0x1E4	
UP2	243	0x1E6	
PTEST	255	0x1FE	Self-test pulse register.

Unassigned registers in the 0-255 range are reserved and should not be written to. Read of unassigned registers will result in extended (not to exceed 500 ns) DTACK responses and unpredictable data.

VME Registers are described in detail below. Within each register, bits are numbered 15 (MSB) through 0 (LSB). Bits 7..0 are the LS byte, and bits 15…8 are the MS byte. For 32-bit items, bits are numbered 31 through 0, with 31-16 in the first (MS) word and 15-0 in the second (LS) word.

5.1 VXIMFR: VXI Manufacturer's ID

This register displays Highland's VXI-registered manufacturer's ID code. It always reads as 0xFEEE.

5.2 VXITYPE: Module Type

This register displays the module type. It normally reads as 22660 decimal, 0x5884.

5.3 VXISTS: VXI Status Register

This register implements the VXI-standard status reporting function. Active bits 2 (PASSED), 3 (READY). and 14 (MODID) will be high.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ID											RDY	PAS		

Shortly after powerup, these bits will be set and all other status bits will be zeroes. Note that the module does NOT support the MODID mechanism.

5.4 ROMID: Firmware Version

The microprocessor software version ID is read here, with a typical value of 22660 decimal (0x5884). Other code versions, having different functionality, may have different ID codes.

5.5 ROMREV: Firmware Revision

The revision letter of the firmware may be read at this location, as an ASCII character, 'A' (0x41) for the initial firmware release.

5.6 MCOUNT: CPU Activity Counter

The MCOUNT register appears as a 16-bit binary counter which is incremented by the microprocessor at about a 25 Hz rate.

5.7 Setup Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					LCK	PLL	CLK				BIG			R1	R0

The user-set R1:R0 bits select the time resolution of all reported timestamp data as follows:

R1	R0	LSB, ps	time range, s	effective clock, GHz
0	0	24.4140625	0.1048576	40.96
0	1	97.6562500	0.4194304	10.24
1	0	390.6250000	1.6777216	2.56
1	1	1562.5000000	6.7108864	0.64

The BIG bit, when set by the user, expands the memory map from the default 512 bytes to 16K bytes, allowing DMA-style block reads of FIFO data. See Section 5.15.

If the user sets the CLK bit, the V660 drives its front-panel CLOCK connector with a 10 MHz square wave derived from its internal clock oscillator.

If the user sets the PLL bit, the module accepts an external input applied to this same CLOCK connector and phase-locks its oscillator to it. The read-only LCK bit is a flag that indicates successful phase locking. The LCK bit will typically rise about two seconds after pll mode is enabled and a valid external reference is applied. Do not set both the CLK and PLL bits.

5.8 Resets Register

Bits 0-11, when user set, respectively hold channels 0-11 in the reset state. When a channel is held reset, its input hit flipflop is held clear, its ENABLE bit is held clear, and its FIFO is cleared until the RESETS bit is cleared by the user. Channel gate control bits are not affected by these resets.

5.9 Enables Register

Bits 0-11 are the respective Channel 0-11 enable bits; this register is read/write from VME. Each channel ENABLE bit is read/write accessible in this register and also in the respective channel control register. Since all 12 ENABLE bits must be accessed together from this register, some timing control strategies (especially single-hit operation) are better managed if the enables are handled independently via the channel-control registers.

Other gates may be additionally required to allow input events to be accepted, as specified in individual channel control registers. These ENABLES bits are effectively ANDed with other conditions to enable channel hit flipflops.

Individual ENABLES bits will be cleared by the module if the associated channel is in single-shot mode and a hit is received; see section 5.13.

5.10 Flags Register

Bits 0-11 of this register are read-only flags indicating that channel time registers contain valid time stamps. These bits are only meaningful in single-shot (non-FIFO) mode.

5.11 Master Counter

The MCH:MCL 32-bit register is the master timestamp counter. The counter clocks continuously at 40 MHz, and may be read as a 32-bit longword, or coherently using separate 16-bit reads if MCH is read first. A 32-bit channel timestamp is a concatenation of N bits of clock interpolation data and 32 – N bits of this counter. For 24 ps resolution, N=10.

Any write that accesses the MS byte will clear this 32-bit counter. Although it is not necessary to ever clear the master counter, it may be useful to clear it just before a burst of time stamps to avoid dealing with the math associated with timestamp rollover.

5.12 FIFO Control Registers

Each of the 12 timestamp channels has a first-in/first-out (FIFO) memory capable of storing up to 256 32-bit time stamps. The following registers present status and provide control of the FIFOs, with bits 0-11 of each register being associated with channels 0-11.

FHIT	FIFO hit (not empty) flags	This register presents an asserted bit for any FIFO that contains any valid timestamps.
FHALF	FIFO half-full flags	Identifies FIFOs that are at least half full, containing 128 or more timestamps.
FHIGH	FIFO 3/4 full flags	Identifies FIFOs that are 3/4 full or more.
FOVER	FIFO overflow flags	Flags FIFOs that have lost input data because they were full. Resetting a FIFO (via RESETS or FZAP) will clear its overflow bit.

FZAP	FIFO resets	This register contains 12 writable bits; the act of writing a '1' to any bit resets the corresponding FIFO; this clears all FIFO flags, empties all data, and resets the FIFO fill count to zero. It is not necessary to clear these bits after a write.

5.13 Channel Control Registers

Each of the 12 timestamp channels has a block of control registers.

5.13.1 CCn Channel Control

A channel control register is arranged as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							ENA	SSM					G2	G1	G0

The three 'G' bits control channel trigger gating. A channel will ignore incoming logic edges if its gating permissive is not true. The three G bits select a gate signal, and that signal is ANDed with the ENA bit; the result enables the input event hit flipflop.

G2	G1	G0	
0	0	0	Channel off: cannot be triggered.
0	0	1	Channel on: ignores gate inputs.
0	1	0	External GATE1 level high enables.
0	1	1	External GATE1 level low enables.
1	0	0	External GATE2 level high enables.
1	0	1	External GATE2 level low enables.

The ENA bit, when asserted, allows triggers to be accepted. This bit is read/write from both the channel control register and the ENABLES register.

If the user sets the SSM bit, the channel works in single-shot mode: the ENA bit (both here and in the ENABLES register) will be cleared immediately after accepting the next time stamp. The timestamp data will then appear in the TH:TL registers and no more triggers will be accepted until ENA is again asserted.

5.13.2 FCn Channel FIFO Control

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	ERR		OVR	DAT	3/4	1/2	C8	C7	C6	C5	C4	C3	C2	C1	C0

The nine Cx bits are a count of how many timestamps are in the channel data FIFO. The count may range from 0 (empty) to 256. Whenever a properly gated trigger pulse arrives, it is timestamped and pushed into the FIFO and the count is incremented. Whenever data is read from the FIFO, the count is decremented.

The DAT bit indicates that there is at least one timestamp in the FIFO. The 3/4 bit indicates that the FIFO is 3/4 full, and 1/2 indicates half full.

The OVR bit indicates that at least one time stamp was lost because the FIFO was full when it arrived. A FIFO reset will clear this flag.

The RST bit, when written to “1”, will reset the FIFO. The data count and all flag bits will go to zero. This bit always reads back as a 0. This reset function is a duplicate of the action performed by the RESETS register.

5.13.3 THn, TLn : Channel Time Stamp

This pair of 16-bit registers contains the last timestamp for this channel. They may be read coherently by a single 32-bit read, or by two 16-bit reads, TH first; do NOT read them in reverse (LS first) order. This value may change at any time in normal operation, and is frozen after one hit in single-shot mode, i.e., when the ENA bit is low.

Hex value 0x80000000 is reserved as the 'empty' flag (a 'true' timestamp value of 0x80000000 is reported as 0x80000001 so that the data point is not lost.) The 'empty' value will be read if the channel has been reset and has not received a hit, or if the channel has been enabled in single-shot mode but has not yet been triggered.

5.13.4 FHn, FLn : Channel FIFO Data

This pair of registers delivers FIFO-buffered time stamps. Data format and readout rules are identical to the TH:TL registers. Hex value 0x80000000 will be reported if the FIFO is empty when read.

If the FIFO data is read using 16-bit VME transactions, always read the FH register first, then read FL.

5.14 PTEST Register

Any write to the PTEST register will fire all 12 timestampers. Channel enable registers should be set to 0x101 to enable the channels to accept the hits. The operation may take up to 2 μsec, and there will be an approximate 100 ps per-channel time skew between channels, with Channel 11 being fired first. This is primarily a factory maintenance function, but may be used to force timestamps to be generated for software test.

5.15 BIGMAP Mode

In BIGMAP mode, each channel is assigned a 1 Kbyte (256 32-bit samples) memory space associated with its FIFO output. Even word locations within each channel block are identical to the channel's FH register, and odd words are equivalent to FL. This allows a single 12K block transfer, performed in either 16 or 32-bit modes, to read out all FIFOs.

Setting the BIG bit in the SETUP register enables bigmap mode.

The space for each channel contains 256 sample locations, but not all samples will generally be valid, as a FIFO is typically unloaded when it is perhaps 1/2 or 3/4 full. Accordingly, the specific timestamp value 0x80000000 is reserved as an 'invalid' flag, meaning that it represents a read of an empty FIFO datum.

The BIGBLOCK address assignments, relative to the module base address, are as follows:

```
Channel 0     0x0400 – 0x07FF
Channel 1     0x0800 – 0x0BFF
Channel 2     0x0C00 – 0x0FFF
Channel 3     0x1000 – 0x13FF

Channel 4     0x1400 – 0x17FF
Channel 5     0x1800 – 0x1BFF
Channel 6     0x1C00 – 0x1FFF
Channel 7     0x2000 – 0x23FF

Channel 8     0x2400 – 0x27FF
Channel 9     0x2800 – 0x2BFF
Channel 10    0x2C00 – 0x2FFF
Channel 11    0x3000 – 0x33ff
```

5.16 Clock Trim Commands

The crystal oscillator on the V660 is factory-set to better than 0.5 PPM accuracy, but will drift with age and temperature. For highest precision, the module timebase should be locked to an external precision 10 MHz clock.

Users may wish to trim the internal oscillator frequency to maintain accuracy when an external reference is not available. An oscillator trim factor XTRIM is stored within the module; commands are available to read, write, and save XTRIM. XTRIM is an unsigned 10-bit integer, ranging in value from 0 to 1023, with nominal center value of 512.

To monitor clock frequency, set the CLK bit in the module setup register, and connect a high-quality frequency counter to the front-panel CLOCK connector.

To read the current XTRIM value, verify that the UCMD register is zero, then write value 0x3039 to UCMD; within 5 milliseconds, UCMD will clear itself and the current value of XTRIM will be available in the UP0 register.

To set XTRIM, verify that UCMD is clear; write the new XTRIM value to the UP0 register, then write 0x3517 to UCMD. UCMD will clear when the oscillator factor is installed, within 5 milliseconds.

To permanently save the current XTRIM value to the nonvolatile EEPROM memory, verify that UCMD is zero, then write 0xFA1E to UCMD. The EPROM write will take about 350 milliseconds, after which UCMD will clear.

5.17 ICTL: Interrupt Control Register

Modules which use the 22660B firmware support interrupts.

The ICTL register is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IEN				IRQ CLR	IFLAG CLR			FIFO OVR	FIFO 3Q	FIFO 1/2	FIFO HIT		IRQ LVL 2	IRQ LVL 1	IRQ LVL 0

IRQ LVL *0-2* — These bits are used to set the VME IRQ. 1 to 7 are valid binary values.

FIFO HIT — Set this bit to enable VME interrupts to occur when the channel FIFOs are not empty.

FIFO 1/2 *FIFO half-full* — Set this bit to enable VME interrupts to occur when the channel FIFOs are half full.

FIFO 3Q *FIFO 3/4 full* — Set this bit to enable VME interrupts to occur when the channel FIFOs are 3 quarters full.

FIFO OVR *FIFO overflow* — Set this bit to enable VME interrupts to occur when the channel FIFOs overflow.

IFLAG CLR — Set & Clear this bit to reset all the channel Interrupt flags.

IRQ CLR — Set & Clear this bit to re-enable VME interrupts after a VME interrupt has occurred. (This is implemented to stop continuous VME interrupts.)

IEN — Set this bit to enable VME interrupts.

5.18 IEN: Interrupt Enables Register

Bits 0-11 are the respective Channels 0-11 enable bits for interrupts. This register is read/write.

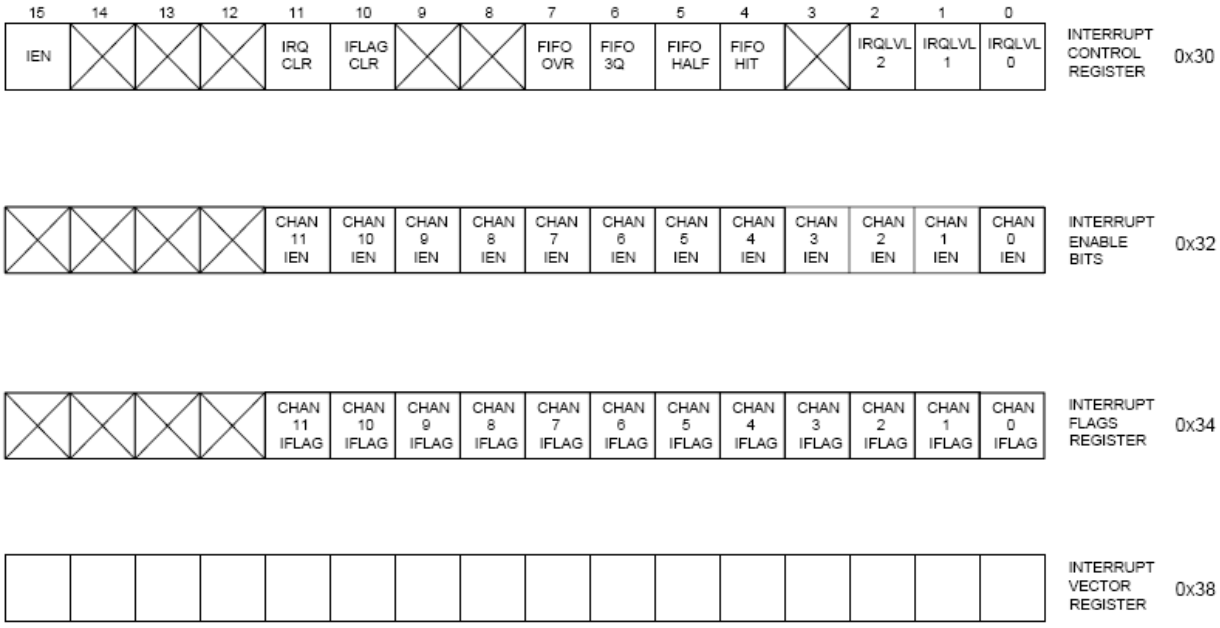
5.19 IFLG: Interrupt Flags Register

Bits 0-11 are the respective Channel 0-11 interrupt flag bits. This register is read only

5.20 IVEC: Interrupt Vector Register

The 8 or 16-bit Interrupt vector (or status word) that is written to the VME bus during an interrupt acknowledge cycle. This register is read/write.

The V660 supports the ROAK (Release-On-Acknowledge) interrupter.



6. Setup and Installation

6.1 Safety and Handling Precautions

The V660 module includes static-sensitive components; please observe antistatic procedures when handling the module outside of its antistatic packaging or outside of the VME cardcage.

Do not insert or remove the module from a crate with crate power on. Powerup the module only when both front-panel screws are tightened to secure the module into the VME crate.

Do not apply any potentials to any V660 outputs.

If explosion hazards are possible, connect V660 signals to field wiring through appropriate intrinsic safety barrier devices.

Do not use pen or pencil points to operate the address DIPswitches. Use a paper clip or other clean implement.

The V660 module has finite failure rates associated with its hardware, firmware, design, and documentation. Do not apply the V660 in data acquisition or control systems where a failure or defect in the module may result in injury, loss of life, or property damage.

6.2 Switch Setups

Four DIPswitches are provided near the VME P1 connector.

6.2.1 A16/A24 Addressing Mode Switch

One DIPswitch position is labeled A16 A24. Press the appropriate side of the switch to permit operation in VME systems, which use “A16” (16-bit) or “A24” (24-bit) addressing.

In A16 mode, the module responds to VME address modifiers 29 and 2D hex. In A24 mode, address modifiers are 39 and 3D hex.

6.2.2 VMEBUS Address Switches

The module VME base address is set by on-board DIPswitches. The switches are labeled “9” through “23”, corresponding to bus address bits. To set an address bit true, press the side of the switch nearest the number legend. If the module is in A16 mode, only switch positions 9 through 15 (S1 and S2 only) are decoded.

Example: to use the module at base address C000 in the A16 space, set the A24/A16 switch to its A16 position, and set the “15”and “14” address switches ON, with all others OFF. This is the factory default.

If BIGMAP mode is to be used, the module address must be set to a multiple of 16K; this requires that dipswitch address bits 13 through 9 all be set OFF.

6.3 Installation In A VME Crate

The V660 may be installed in any standard 16- or 32-bit 6U VME backplane. The module connects to the backplane J1 and J2 connectors. Seat the module firmly and secure both front-panel mounting screws before applying power.

7. Examples

7.1 Minimum Timestamp Setup

A basic module setup procedure might be as follows:

1. Set the module address DIPswitches as described in Section 6.2. The factory default is A16 mode, address 0xC000. Install and power up as described in Section 6.
2. Read the base module address (0xC000 here) as a 16-bit register. Verify that the blue VME LED flashes, and that the register reads 0xFEEE.
3. Leave the SETUP register clear to use the default 24 ps timing.
4. Write 0x0101 to all 12 of the CCx channel control registers
5. Write 0x0FFF to the RESETS register, then clear it.

The V660 will now accept triggers and load the channel FIFOs with the acquired timestamps. If no inputs are available, one or more writes to the PTEST register will create test timestamps.

8. Typical Performance

Figure 2 is a 24-hour plot of the time accuracy and RMS jitter of a typical channel. This setup uses Channel 11 as the 'start' channel, and Channel 6 as the 'stop' channel, for a group of time interval measurements stepped from 160 ns to 100 ms. The V660 was phaselocked to a precise external clock source to give stable timestamps for the longer time measurements. The central plot is time errors averaged over 250 shots per time step, and the small green and grey dots are the extreme minimum and maximum time errors. The RMS error points are each the standard deviation of a group of 250 shots. The rise at the right end of the curve is caused by timebase errors in the V660 vs the test generator.

Figure 3 is a plot of time-error vs. time delay for all 12 channels superimposed. Again, all channel time measurements were relative to Channel 11, so the Channel 11 data became simple period measurements.

Figure 4 is the same as Figure 3, but only the V660 internal clock was used, and data was plotted for 24 hours. The fishtail beginning at about 8 msec results from accumulated timebase errors, driven mainly by ambient temperature changes in an uncontrolled office environment. The extremes indicate about an 20 PPB peak-to-peak timebase oscillator drift.

Figure 2

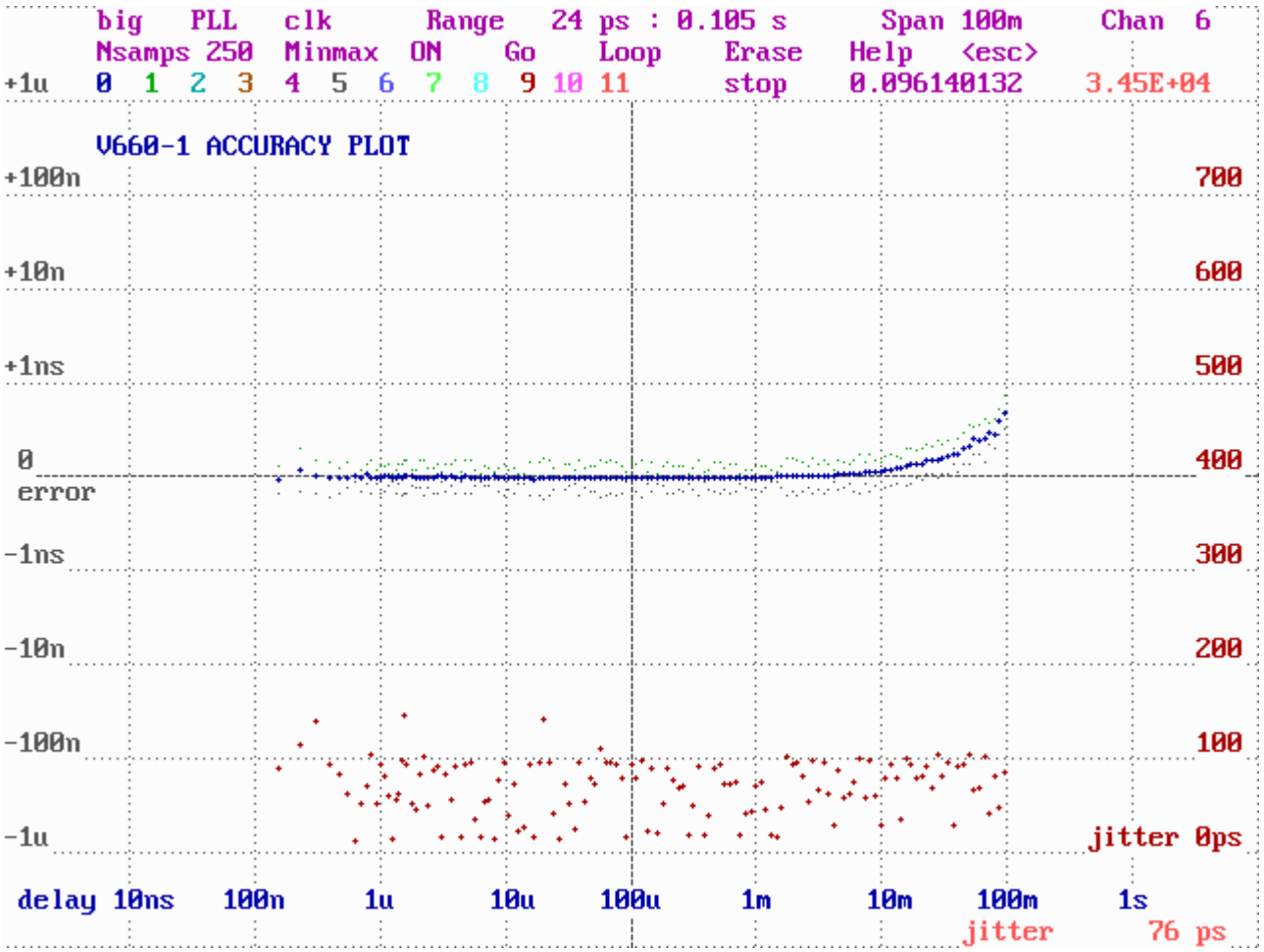


Figure 3

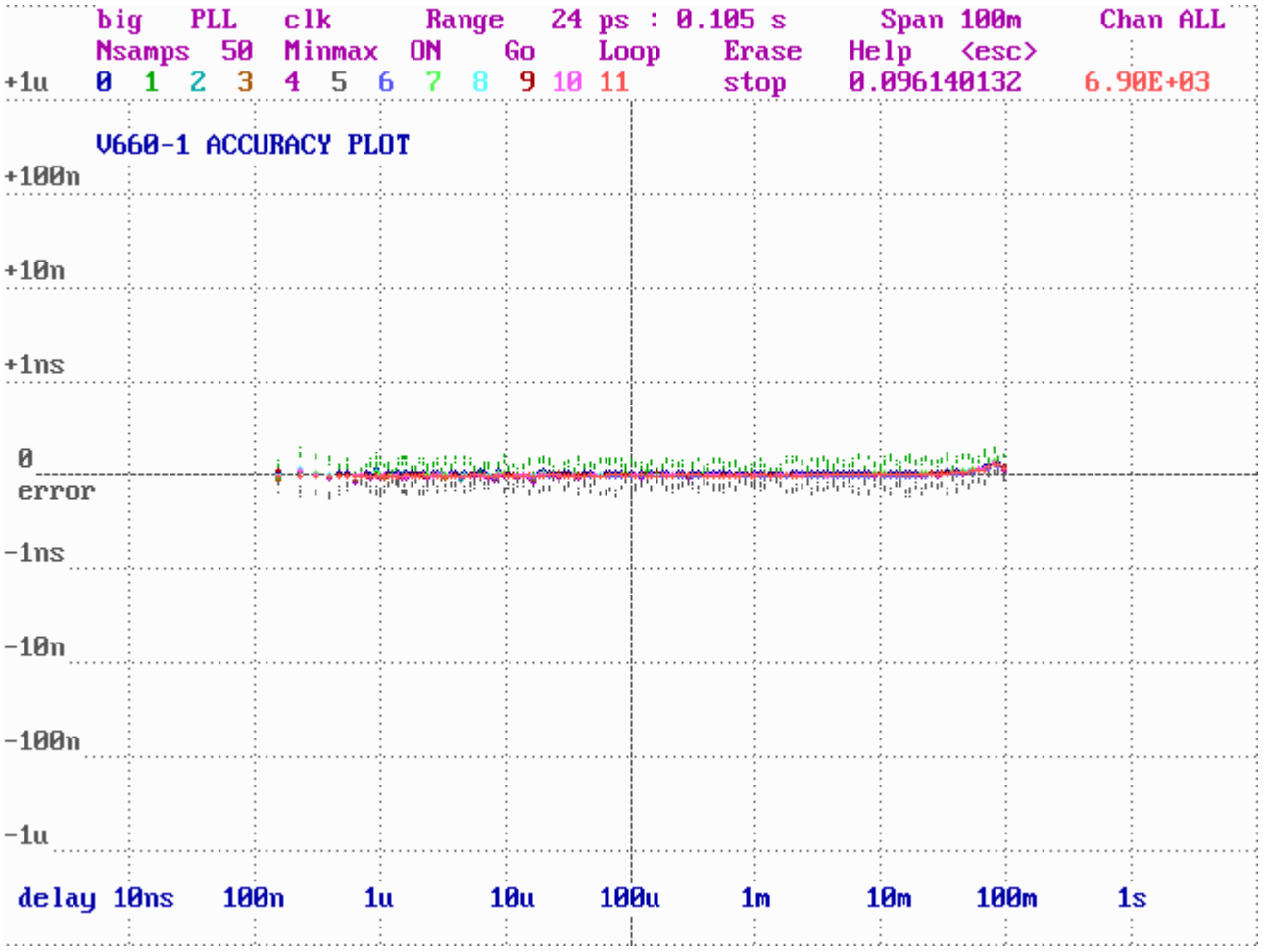
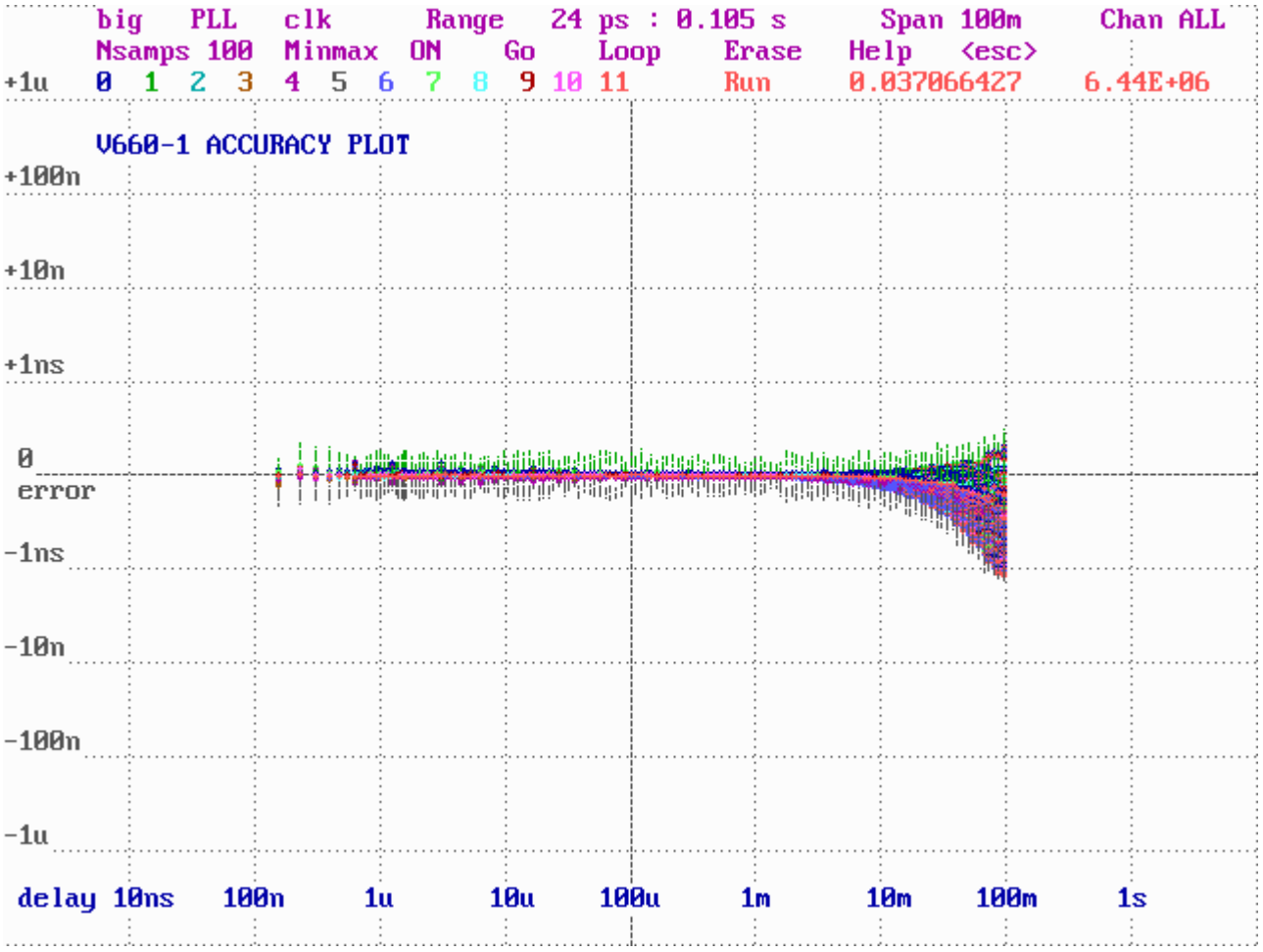

big PLL clk Range 24 ps : 0.105 s Span 100m Chan ALL
Nsamps 50 Minmax ON Go Loop Erase Help <esc>
+1u 0 1 2 3 4 5 6 7 8 9 10 11 stop 0.096140132 6.90E+03
V660-1 ACCURACY PLOT
+100n
+10n
+1ns
0
error
-1ns
-10n
-100n
-1u
delay 10ns 100n 1u 10u 100u 1m 10m 100m 1s

Figure 4


big PLL clk Range 24 ps : 0.105 s Span 100m Chan ALL
Nsamps 100 Minmax ON Go Loop Erase Help <esc>
+1u 0 1 2 3 4 5 6 7 8 9 10 11 Run 0.037066427 6.44E+06
V660-1 ACCURACY PLOT
+100n
+10n
+1ns
0
error
-1ns
-10n
-100n
-1u
delay 10ns 100n 1u 10u 100u 1m 10m 100m 1s

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