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HIGHLAND TECHNOLOGY



V860 SIX-CHANNEL PULSE AMPLIFIER VME MODULE

Technical Manual

September 3, 2010

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1. INTRODUCTION

This document is the technical manual for the series V860 pulse amplifier. The V860 is a 6-channel digital pulse amplifier packaged as a single-width VME module. The V860 may be used as a fast pulse amplifier, laser driver, FET driver, or trigger fanout.

The module provides six independent amplifier channels, each with input and output connectors. All channels share a common input threshold and output voltage level. One common GATE input is provided to disable all outputs. Channel inputs may be clustered to allow the module to be used as a trigger fanout.

Available versions are...

Six channels, SMB connectors	model V860-1	assembly 22A860-1
Six channels, LEMO connectors	model V860-2	assembly 22A860-2
Six channels, SMA connectors	model V860-3	assembly 22A860-3

This manual applies to revision 'C' units.

2. SPECIFICATIONS : MODEL V860 PULSE AMPLIFIER

FUNCTION	Multichannel digital pulse amplifier
INPUTS	Six logic inputs, threshold from -2.5 to +2.5 volts, common trimpot adjustment, factory set to +1.25 volts Maximum safe input is ± 4 volts Per-channel switches are provided to select input polarity and input termination, 50Ω to ground or high impedance Factory setting is positive, terminated Channel inputs may be cascaded such as to drive multiple outputs from one input One common TTL-level GATE input disables all outputs when pulled low
OUTPUTS	Six positive pulses, active pullup, passive pulldown; customer termination to ground is required Pulse amplitude is adjustable from +4 to +10 volts into a 50Ω load, with common adjustment for all channels Factory set to +5 volts Pullup output impedance is 2Ω nominal; pulldown is 500Ω nominal Output current limit is 300 ma peak, 80 ma average Risetime 500 ps max; falltime 5 ns max
PROPAGATION DELAY	Rising edge, 3.5 ns typical; falling edge, 10 ns typical
JITTER	Rising edge, less than 5 ps RMS added jitter Falling edge, less than 25 ps RMS added jitter

OPERATING TEMPERATURE	0 to 60° C; extended MIL/COTS ranges available
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies: +5 volts, 200 mA max +12 volts, 360 mA max (plus load current) -12 volts, 150 mA max
CONNECTORS	V860-1 SMB V860-2 LEMO V860-3 SMA
PACKAGING	Single-wide 6U VME module
CONFORMANCE	VMEbus per ANSI/VITA 1-1994 (R2002) The module does not interface to the VME data bus, and passes all VME grant lines

3. INSTALLATION AND OPERATION

CAUTION : THE V860 USES HIGH-SPEED SILICON AND GALLIUM ARSENIDE SEMICONDUCTORS. THESE PARTS ARE HIGHLY STATIC SENSITIVE AND MAY BE DAMAGED BY STATIC DISCHARGE OR ELECTRICAL OVERLOAD.

USE FULL STATIC CONTROL PROCEDURES WHEN HANDLING AND USING THESE MODULES. ENSURE THAT ALL INPUTS AND OUTPUTS ARE NOT SUBJECT TO OVERLOAD, AND THAT ALL COAXIAL CABLE CENTER CONDUCTORS ARE DISCHARGED BEFORE BEING CONNECTED.

DO NOT APPLY MORE THAN +-4 VOLTS TO INPUTS. DO NOT DRIVE OUTPUTS.

3.1 SWITCH SETUP

Before installing a V860 in a VME crate, the various rotary switches should be set up for the intended application.

The amplifier channels are numbered 0 through 5. Each channel has dedicated **HI/50** (termination select) and **+ / -** (signal polarity) switches. Channels and switches are clearly labeled on the PC board surface.

For each channel, set its termination select switch to **50** to terminate the input signal with 50 ohms to ground, or to **HI** for high impedance input. Set the polarity switch to **+** for non-inverting operation, or **-** for inversion.

Channels 1 through 5 also have cascade select switches, located just to the left of the termination select switches. These switches are labeled **NORM** and **INx**, where 'x' is the current channel number minus 1. When these switches are in their **NORM** positions, each channel will act independently, accepting its input from its dedicated input connector. These channels may also accept its input from the input of the previous channel. For example, the CH1 cascade switch may be set to its **IN0** position, in which case the Channel 1 amplifier will receive its input from the Channel 0 input signal, with the Channel 1 connector being unused. 'Chains' may be built by continuing this cascade; for example, Channels 0 through 3 may all be driven from the CH0 input if the Channel 1, 2, and 3 cascade switches are set to accept inputs from the respective previous channels.

When two or more channels are used in a cascade group, only the last (highest-numbered) channel should be terminated.

3.2 VME CRATE INSTALLATION

The V860 may be installed in any slot of a standard VME crate. The module receives only power from the crate, and does not connect to the VME data lines. The module passes all bus grant signals.

DO NOT INSERT OR REMOVE THE V860 WHEN CRATE POWER IS ON.

TO AVOID STATIC DAMAGE, INSTALLERS SHOULD GROUND THEMSELVES TO THE CRATE FRAME BEFORE ALLOWING THE MODULE TO CONTACT THE CRATE.

3.3 SETTING THRESHOLD AND OUTPUT VOLTAGE ADJUSTMENTS

After the module switches are set and the module is inserted in the VME crate and powered up, but before inputs and outputs are connected, the two front-panel trimpots should be set.

Connect a voltmeter from VME common to the VTH test point on the front of the module, and adjust the VTH pot for the desired logic input threshold voltage. For minimum jitter, set the threshold to the point on the input waveform which has the highest volts/nanosecond slope; this is generally near the midpoint of the input signal swing.

Connect the voltmeter to the VOUT test point and set the VOUT pot for the desired output signal high voltage value. This is adjustable in the range of +4 to +10 volts.

4. OPERATING NOTES AND LIMITATIONS

Outputs are DC coupled, but have limited drive capability, due to both GaAs FET thermal limits and VME connector pin current limits. Should average output current exceed about 100 ma for any single channel, that channel will current limit and output amplitude will drop below the value set by the **VOUT** adjustment. Control pulse duty cycle such as to limit output current to 80-milliamp average.

All outputs should be terminated in 50 ohms to ensure specified performance, but the output drivers will not be damaged by any resistive load, open, or short. When driving LEDs or lasers, it is best to add series resistance at the load to create an approximate 50-ohm termination, reducing reflections and ensuring clean edges.

Circuits will be damaged by input voltages exceeding +-4 volts. Always set the input threshold level to the correct value before connecting input signals.

If the GATE input is grounded, all outputs will be forced off (low). This input is TTL/CMOS compatible, and is pulled up to +5V through a 1K resistor. Response time is in the 10 ns range.

5. JITTER CONSIDERATIONS

The V860 is capable of amplifying pulses with added jitter of a few picoseconds RMS. To achieve minimum rising-edge jitter, observe the following precautions:

1. The input signal should be as large in amplitude as possible (at least a 1 volt transition is preferred) and must have a high slew rate, preferable several volts per nanosecond. Set the V860 input threshold to the highest-slope point of the input waveform.

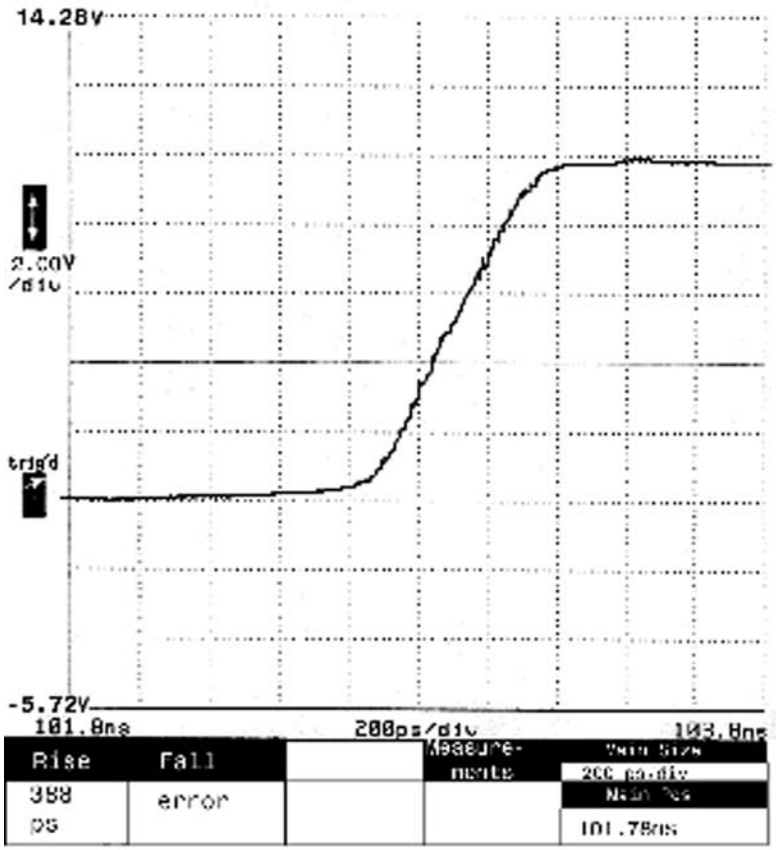
2. Avoid introducing noise, hum, or ground loop potentials between system assemblies. Millivolts of hum or RF noise can contribute substantial jitter to a slow input trigger edge; a standard TTL signal, slewing at about 0.3 volts/ns, will demonstrate about 3 ps added jitter for each millivolt of noise. DC blocks can sometimes be used to remove 60 Hz hum and low-frequency noise from inputs.

3. Use short, low-loss coaxial cables to interconnect system components. Use SMA connectors if possible.

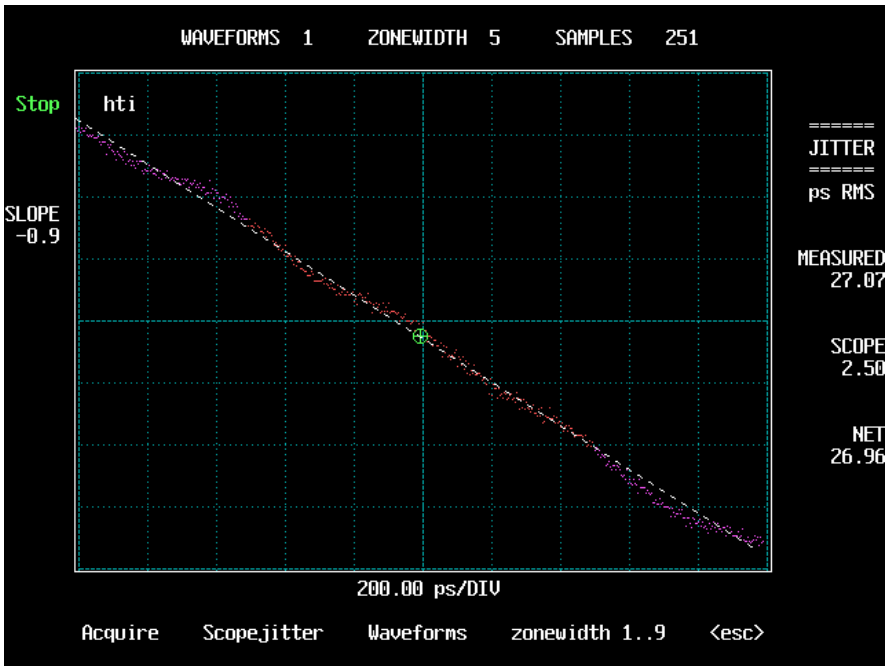
4. Ensure that the VME crate power supplies meet the noise requirements of the IEEE 1014 VME spec. For minimum jitter, transient crate loads (such as computers and disk drives) should not be present in the crate with the V860, as they tend to introduce power supply transients and contribute to ground-loop noise.

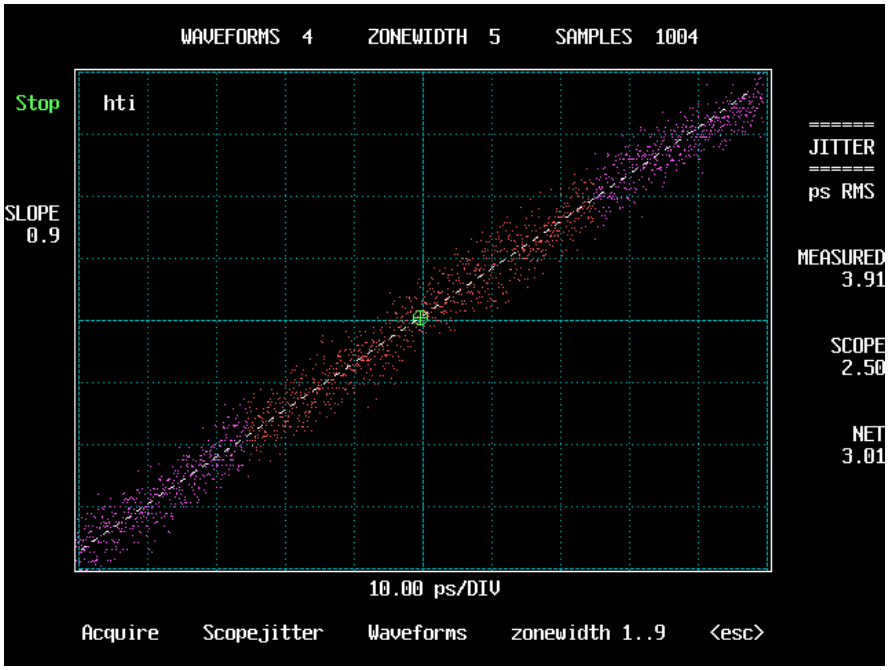
6. TYPICAL PERFORMANCE

The following figures represent typical performance of the V860.



Typical Output waveform





Waveforms were acquired using a Tektronix model 11801 sampling oscilloscope with an SD24 (20 GHz) sampling head. A 20 dB (10:1) attenuator was used at the sampling head input.

To generate a low-jitter scope pretrigger, a standard pulse generator was used to drive the CH0 and CH1 channels in cascade mode. This generated two 5-volt

outputs; one output was used to trigger the scope, and the other was delayed 80 ns by a low-loss coaxial cable and used as the input to the channel under test, CH2, whose output was displayed on the scope. Measured jitter is thus a combination of the jitter introduced by three separate V860 channels. The sampling scope has an internal jitter of about 2.5 ps RMS.

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