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HIGHLAND TECHNOLOGY



V880
SYSTEM TIMING
VME MODULE

TECHNICAL MANUAL

September 2, 2010

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1. SCOPE AND OVERVIEW

This is the technical manual for the Highland Model V880 System Timing Module, Highland part number 22A880, Revision B.

The V880 is an 8-channel precision system timing VME module. It accepts a fiberoptic 155-MHz serial data stream, which the module uses to synchronize its internal low-jitter clock and from which a realtime data payload is recovered. The payload defines repetitive time epochs and single-shot system events which the V880 can decode. Eight independent pattern recognition channels are provided, each equipped with a high-resolution, low-jitter digital delay generator and output driver stage. A ninth non-delayed reference channel is included for testing purposes.

The V880 is intended for use in systems where large numbers of devices must be triggered at precise times, and where the client devices are typically distributed over a physically large facility.

The V880 Timing Module is capable of generating system triggers with 1-picosecond settability, and has combined RMS jitter and drift which is typically below 10 picoseconds.

Several versions of the module are available, distinguished by suffix dash numbers. There are two accuracy classes, "Standard" and "Precision," and modules are available with electrical and/or optical outputs in units of four channels. Versions are...

MODEL	ACCURACY	OUTPUTS	NIF VERSION
V880-1	Standard	8 electrical	type A
V880-2	Precision	8 electrical	type D
V880-3	Standard	8 optical	type B
V880-4	Precision	8 optical	type C
V880-5	Standard	4 ele, 4 opt	--
V880-6	Precision	4 ele, 4 opt	--

Module Revision B incorporates the following changes:

Temperature and optical power compensation has been added to the Reference pulse output, and Reference timing has changed slightly.

The nonvolatile calibration table and serial number are now stored in redundant EEPROM memory tables; battery backup is eliminated. The module status register has associated new bits, and calibration procedures have been changed.

The OC-3 phase-locked loop now has automatic acquire and lock modes for faster lock and reduced jitter.

Several changes were made to reduce the temperature coefficient of delay.

The OC-3 temperature sensor was deleted.

The Rev B module is compatible with Rev A in normal operating modes.

2. PRODUCT SPECIFICATIONS

Specifications noted are for Precision modules; values in brackets are for Standard modules.

FUNCTION	8-channel digital timing generator
DEVICE TYPE	16-bit register-based VME slave; A16:D16 Implements 256 16-bit registers in the VME 16-bit addressing space
INPUTS	Primary timing input: 155.52 Mbps, biphase-encoded data stream, 1310 or 1550 nm, -20 to -28 dBm, APC/SC bulkhead connector Electrical test trigger, +1 V nominal threshold, 50Ω termination, SMB connector
OUTPUTS	Reference timing pulse, +1.75 V nominal into external 50Ω load, 180 ns nominal width, 700 ps nominal rise/fall, SMB connector Test output, sample of software-selected output channel pulse; +1 V nominal into 50Ω, SMB connector Eight channel outputs, 180 ns pulse each, available as electrical or optical outputs in groups of four channels Electrical outputs are +4 V nominal into 50Ω, transformer isolated, 750 ps nominal risetime, SMB connectors Optical outputs are 850 nm, 500 µW nominal, 500 ps max risetime, ST 62/125 µm multimode connectors
DELAYS	Eight channels; each channel includes a VME-programmable 128-bit pattern match array, a 128-bit pattern mask array, and a 0 to 3 second range digital delay generator with 1 ps LSB resolution Each channel is triggered when its programmed pattern match aligns with the time data fields in the master fiberoptic input signal A ninth reference channel is provided, with pattern match capability but no programmable delay
ACCURACY	Jitter is below 15 [25] ps RMS measured over 10 seconds or less Delay accuracy is ±250 [500]ps; resolution 1 ps; monotonicity 40 [100]ps Insertion delay is 96.0 ns relative to the end of frame sync Reference pulse delay is 63 ns ±450 [750]ps Temperature drift is below 1 [2.5]ps/°C Optical power sensitivity is below 15 [50]ps/db, -20 to -28 dBm

OPERATING TEMPERATURE	10 to 35°C
CALIBRATION INTERVAL	One year
POWER	Standard VME supplies: +5 V: 1.75 A +12 V: 0.4 A −12 V: 0.6 A
INDICATORS	LEDs indicate VME access, channel trigger, and phaselock
PACKAGING	6U single-wide VME module
CONFORMANCE	ANSI/VITA 1-1994 (R2002) VMEbus spec

3. FUNCTIONAL DESCRIPTION

3.1 OVERALL ARCHITECTURE

The V880 block diagram is shown as Figure 1. The module includes...

A. Power conditioning to provide various filtered and regulated supply voltages as needed.

B. A front-end optical signal receiver, phase-locked loop, and serial data recovery section.

C. A Control FPGA, which manages data deserialization and checking, pattern matching, channel triggers, VME interface, and includes the central 256-word by 16-bit 4-port memory.

D. A Timer FPGA which performs coarse (12.86ns resolution) channel delay generation.

E. Eight channel delay verniers which perform fine (1ps resolution) channel delays.

F. An internal microprocessor system which manages module configuration, operation, and calibration.

3.2 OPTICAL DATA STREAM

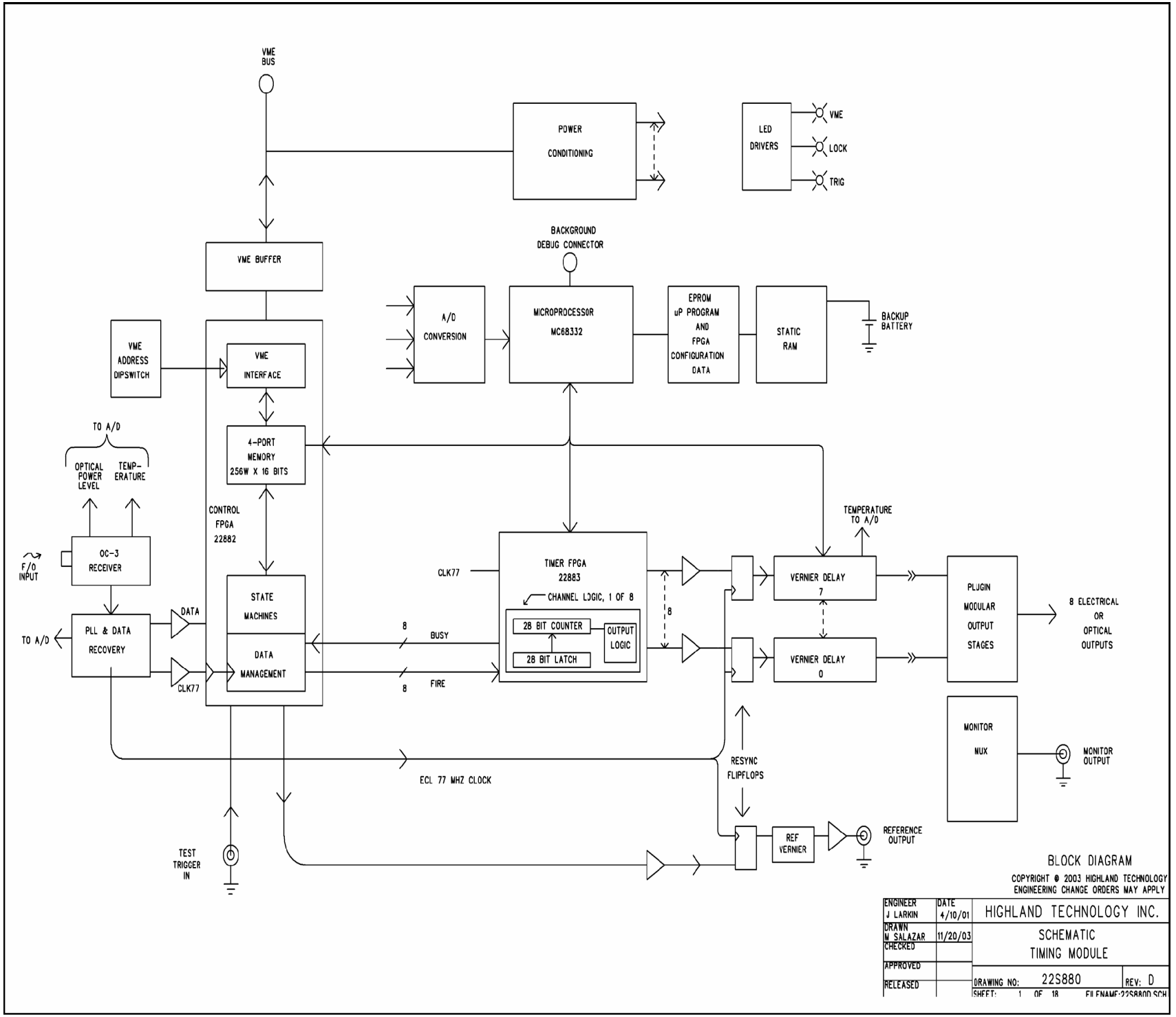
The V880 accepts a 155.52Mbaud biphase-encoded optical datastream via an APC/SC bulkhead feedthrough, using 9-micron singlemode fiber.

The data content of the optical datastream is described in Section 6.

3.3 PHASE-LOCKED LOOP

The module uses a commercial OC-3 fiberoptic receiver module to recover the biphase data from the optical signal. A phase-locked loop synchronizes an internal low-jitter ECL crystal oscillator to the data output of the receiver, aligning rising edges of data to rising edges of the local clock. The PLL will lock onto data streams at 155.52Mbaud ±10PPM, about ±1.5KHz from the ideal center frequency. Lock time is under one second.

The phaselocked 155.52MHz clock is divided by two to create the 77.76MHz module master timing clock CLK77.



BLOCK DIAGRAM

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ENGINEER J LARKIN	DATE 4/10/01	HIGHLAND TECHNOLOGY INC.
DRAWN M SALAZAR	11/20/03	SCHEMATIC TIMING MODULE
CHECKED		
APPROVED		
RELEASED		DRAWING NO: 22S880 REV: D
		SHEET: 1 OF 18 FILENAME:22S880D.SCH

3.4 DATA RECOVERY CIRCUITS

The module has a fast (ECL-based) serial data recovery circuit which uses the CLK77 signal to decode the biphase serial data stream. The recovered data stream is applied to the Control FPGA chip, which then processes the stream as follows:

A. The logic waits for a stream of at least 256 sequential '1' bits as confirmation of the 'fill' state, then...

B. Waits for the next '0' bit, then deserializes the 160-bit data payload. The initial '0' is assumed to be the first bit of the frame sync word. The payload contents are written into the VME-accessible multiport memory. If snapshot mode is active, a second copy of the payload is written to memory and the snapshot request flag cleared.

C. If the framesync pattern is correct, channels which were previously armed will be triggered at the end of the framesync word.

D. After all payload words are received, the framesync and CRC words are checked; if both are correct, the pattern-match microengine is triggered to run.

3.5 PATTERN MATCH MICROENGINE

Following a good payload, the pattern-match microengine is run. This is an FPGA-resident state machine which determines which of the nine output channels should be armed for trigger at the next framesync. The microengine makes repeated accesses to the multiport memory, comparing the just-received timing payload to the 16 words of pattern match and pattern mask associated with each channel. If the 128-bit-wide logical operation

Yn = (PAYLOAD XOR MATCHn) OR MASKn

results in Yn = all 1's, Channel n will be armed to trigger. PAYLOAD here refers to the 128 timing bits embedded in the optical data stream, MATCHn is the VME-loaded 8-word match array associated with Channel n, and MASKn is the VME-loaded 8-word 'don't care' array for Channel n.

3.6 DELAY GENERATORS

If any channel is armed by the microengine and is not currently busy, its delay generator will be triggered at the next framesync, starting the channel delay generator. Each channel has a separate digital delay generator, having a 3-second maximum delay and 1-picosecond delay resolution. Each delay generator consists of a programmable down-counter operating at the CLK77 rate, followed by an analog time vernier circuit. The onboard microprocessor continuously computes and applies optical power and temperature error corrections to all vernier delays.

At the end of the channel delay, a 180ns one-shot is fired to drive the channel output stages. Note that the reference channel has no DDG, and acts as if it had zero programmed delay. The reference has no delay delay generator, but does apply corrections for optical power and temperature influences.

3.7 OUTPUT STAGES

Delay generators 0 through 7 drive final output stages. The output drivers are modular in groups of four, and may be configured for electrical or optical outputs.

3.8 VME INTERFACE

The V880 implements a standard 16-bit VME interface, with the entire 256-word multiport memory being read/write accessible via the VME port.

3.9 MICROPROCESSOR

An internal MC68332 microprocessor performs the following functions:

A. At powerup time, configures the RAM-based Control and Timer FPGA chips and recovers the calibration table from EEPROM.

B. Scans internal analog points, including internal temperatures, optical power level, VCO parameters, and output stage monitors.

C. Continuously updates various module status words in the multiport, VME-accessible 256-word memory.

D. Services global module commands.

E. Services individual channel commands which alter channel trigger setups or delay times.

F. Provides calibration services, including storage and implementation of channel calibrations and compensations for variations in optical power level and temperature.

3.10 TIMING NOTES

All V880 timings are referenced to the plane of the module front panel.

Output times are measured at the half-amplitude point of any electrical or optical output, and are always referenced to the end of the frame sync word of the incoming optical data stream. In order for a channel to fire, a pattern match must have occurred in the **previous** payload.

'End of frame sync' is defined as one clock (6.430ns) after the mid-bit transition of the last biphase bit of the 16-bit frame sync word. This is a rising (light-on) edge. This is equivalent to 31 clocks (199.331ns) after the rising mid-bit transition of the first '0' bit of the frame sync word.

If any normal channel is programmed for zero delay, its output edge will rise 96.0ns after the end of frame sync.

The reference channel rising edge will occur 63.00ns after the end of frame sync.

The front-panel monitor output is delayed about 1.0ns from the selected output which is being monitored.

OC3 CLOCK RATE	155.52MHz	period = 6.43004ns
BIPHASE BIT RATE	77.76MHz	period = 12.86008s
WORD LENGTH	16 bits	205.7613ns
PAYLOAD LENGTH	10 words	2.057613µs
FRAME LENGTH	3240 bits	41.66666µs

Section 6 discusses the payload structure in detail.

4. VME REGISTER MAP AND PROGRAMMING

The following is a summary of the 256 VME-accessible registers implemented by the V880 timing module. All registers are located in the short (16-bit) VME addressing space and generally follow the VXI register use conventions. The module base address is selected via the on-board VME ADDRESS DIPswitch, allowing the base to be set to any multiple of 200 hex within the VME 16-bit space. The module responds to VMEbus address modifiers 2D and 29 hex. Modules are usually shipped set to hex address C000.

All V880 registers are 16 bits wide, and may be byte- or word-addressed according to VME specifications. REG # below is the ordinal register number in decimal; OFFSET is the VMEbus address offset from the module base address, shown in hex. The R/W column indicates whether the register is intended to be readable and/or writable from the VMEbus. Since all registers are located in a dual-port RAM structure, all are in fact readable and writable by both the VME port and module internal hardware; register read/write privileges are determined by convention.

REG NAME	REG#	OFFSET	R/W	FUNCTION
VXIMFR	0	00	RO	VXI manufacturer ID: always 65262, FEEE hex
VXITYPE	1	02	RO	module type, always 22880, 5960 hex
VXISTS	2	04	RO	VXI status register, always FFFF hex
MSTAT	3	06	RO	module status register
CTRL	4	08	RW	module CONTROL register
TRIGS	5	0A	RW	TRIGGERS register
TMUX	6	0C	RW	test multiplexer register
SERIAL	7	0E	RO	module serial number
CAL	8	10	RW	calibration control register
CODE	9	12	RO	firmware version number
REV	10	14	RO	firmware revision letter
CSTAT	11	16	RO	calibration status register
GFRAME	12	18	RO	good frame counter
BFRAME	13	1A	RO	bad frame counter
INIT	14	1C	RW	module initialization register
CREF	15	1E	RW	reference channel control register
C0	16	20	RW	channel 0 control register
H0	17	22	RW	channel 0 MS time delay register
M0	18	24	RW	channel 0 mid time delay register
L0	19	26	RW	channel 0 LS time delay register
C1	20	28	RW	channel 1 control register
H1	21	2A	RW	channel 1 MS time delay register
M1	22	2C	RW	channel 1 mid time delay register
L1	23	2E	RW	channel 1 LS time delay register
C2	24	30	RW	channel 2 control register
H2	25	32	RW	channel 2 MS time delay register
M2	26	34	RW	channel 2 mid time delay register
L2	27	36	RW	channel 2 LS time delay register

REG NAME	REG#	OFFSET	R/W	FUNCTION
C3	28	38	RW	channel 3 control register
H3	29	3A	RW	channel 3 MS time delay register
M3	30	3C	RW	channel 3 mid time delay register
L3	31	3E	RW	channel 3 LS time delay register
C4	32	40	RW	channel 4 control register
H4	33	42	RW	channel 4 MS time delay register
M4	34	44	RW	channel 4 mid time delay register
L4	35	46	RW	channel 4 LS time delay register
C5	36	48	RW	channel 5 control register
H5	37	4A	RW	channel 5 MS time delay register
M5	38	4C	RW	channel 5 mid time delay register
L5	39	4E	RW	channel 5 LS time delay register
C6	40	50	RW	channel 6 control register
H6	41	52	RW	channel 6 MS time delay register
M6	42	54	RW	channel 6 mid time delay register
L6	43	56	RW	channel 6 LS time delay register
C7	44	58	RW	channel 7 control register
H7	45	5A	RW	channel 7 MS time delay register
M7	46	5C	RW	channel 7 mid time delay register
L7	47	5E	RW	channel 7 LS time delay register
X0A	48	60	RW	match pattern, ch 0 (msb == 1st payload bit)
X0B	49	62	RW	match pattern, ch 0
X0C	50	64	RW	match pattern, ch 0
X0D	51	66	RW	match pattern, ch 0
X0E	52	68	RW	match pattern, ch 0
X0F	53	6A	RW	match pattern, ch 0
X0G	54	6C	RW	match pattern, ch 0
X0H	55	6E	RW	match pattern, ch 0 (lsb == last pl bit)
K0A	56	70	RW	mask pattern, ch 0 (msb == 1st payload bit)
K0B	57	72	RW	mask pattern, ch 0
K0C	58	74	RW	mask pattern, ch 0
K0D	59	76	RW	mask pattern, ch 0
K0E	60	78	RW	mask pattern, ch 0
K0F	61	7A	RW	mask pattern, ch 0
K0G	62	7C	RW	mask pattern, ch 0
K0H	63	7E	RW	mask pattern, ch 0 (lsb == last pl bit)

8-word mask and match pattern blocks repeat for channels 1-7 and the reference channel, as follows:

REG NAME	REG#	OFFSET	R/W	FUNCTION
X1A-X1H	64-71	80	RW	match pattern, channel 1
K1A-K1H	72-79	90	RW	mask pattern, channel 1
X2A-X2H	80-87	A0	RW	match pattern, channel 2
K2A-K2H	88-95	BO	RW	mask pattern, channel 2
X3A-X3H	96-103	C0	RW	match pattern, channel 3
K3A-K3H	104-111	D0	RW	mask pattern, channel 3
X4A-X4H	112-119	E0	RW	match pattern, channel 4
K4A-K4H	120-127	F0	RW	mask pattern, channel 4
X5A-X5H	128-135	100	RW	match pattern, channel 5
K5A-K5H	136-143	110	RW	mask pattern, channel 5
X6A-X6H	144-151	120	RW	match pattern, channel 6
K6A-K6H	152-159	130	RW	mask pattern, channel 6
X7A-X7H	160-167	140	RW	match pattern, channel 7
K7A-K7H	168-175	150	RW	mask pattern, channel 7
X8A-X8H	176-183	160	RW	match pattern registers, reference channel
K8A-K8H	184-191	170	RW	mask registers, reference channel
FSYNC	192	180	RO	realtime frame sync word
PATA	193	182	RO	realtime first payload pattern word
PATB	194	184	RO	
PATC	195	186	RO	
PATD	196	188	RO	
PATE	197	18A	RO	
PATF	198	18C	RO	
PATG	199	18F	RO	
PATH	200	190	RO	realtime last payload pattern word
CRC	201	192	RO	realtime CRC

REG NAME	REG#	OFFSET	R/W	FUNCTION
LFSYNC	208	1A0	RO	latched frame sync word
LPATA	209	1A2	RO	latched first payload pattern word
LPATB	210	1A4	RO	
LPATC	211	1A6	RO	
LPATD	212	1A8	RO	
LPATE	213	1AA	RO	
LPATF	214	1AC	RO	
LPATG	215	1AE	RO	
LPATH	216	1B0	RO	latched last payload pattern word
LCRC	217	1B2	RO	latched CRC
OPL	224	1C0	RO	received optical power, nanowatts
OCTEMP	225	1C2	RO	unused (was OC3 receiver temperature)
PCTEMP	226	1C4	RO	PC board surface temperature
VCXO	227	1C6	RO	PLL VCXO control voltage
SCAN	228	1C8	RO	microprocessor service loop counter
CALSUM	229	1CA	RO	calibration table checksum
RXVX	230	1CC	RW	control FPGA test mux
RXTX	231	1CE	RW	timer FPGA test mux
TTC	232	1D0	RO	pcb temperature:time correction
OPC	233	1D2	RO	optical power:time correction
OPX	234	1D4	RO	unscaled optical power level
VC0	235	1D6	RO	maintenance: ch 0 VCODE
DC0	236	1D8	RO	maintenance: ch 0 DCODE
RE0	237	1DA	RO	maintenance: ref dac
AN0	238	1DC	RO	output 0 monitor
AN1	239	1DE	RO	output 1 monitor
AN2	240	1E0	RO	output 2 monitor
AN3	241	1E2	RO	output 3 monitor
AN4	242	1E4	RO	output 4 monitor
AN5	243	1E6	RO	output 5 monitor
AN6	244	1E8	RO	output 6 monitor
AN7	245	1EA	RO	output 7 monitor
INH	246	1EC	RW	calibration inhibits
PAD	252	1F8	RW	ram peek address
PHI	253	1FA	RO	peek ms data
PLO	254	1FC	RO	peek ls data

Registers are described in detail below. Within each register, bits are numbered 0 (LSB) through 15 (MSB).

See Section 7 for discussion of calibration-related registers CAL, CSTAT, INH, and CALSUM.

4.1 VXIMFR: VXI MANUFACTURER'S ID REGISTER

This register displays the VXI-registered manufacturer's ID code for Highland Technology. It always reads as FEEE hex.

4.2 VXITYPE: MODULE TYPE REGISTER

This register displays the module type. It normally reads as 22880 decimal, 5860 hex; special-function modules may display different codes.

4.3 VXISTS: VXI STATUS REGISTER

This register always reads all 1's (FFFF hex).

4.4 MSTAT: MODULE STATUS REGISTER

This read-only register summarizes the module status. Bits are...

BIT	NAME	FUNCTION
7	HIPRES	if set, the module is a Precision version
8	ALT	indicates that alternate (backup) EEPROM cal table is in use (primary table is corrupted)
9	CRCERR	CRC error flag
10	CALERR	high if calibration table is corrupt
11	CALDEF	true if default calibration table is installed
12	ALARM	true if optical power is out of legal range
13	MLOCK	true if PLL is marginally locked
14	NOLOCK	true if PLL is not locked
15	PFAIL	true following powerup; cleared by any channel control register operation

CRCERR is a realtime indication of the state of the hardware CRC checker.

CALERR will go true if the internal calibration table has a bad checksum.

CALDEF will be true if the default calibration table is installed. This table will generally have a bad checksum.

The ALARM bit will go high if the received optical power is not in the acceptable range. Alarm limits are about -17 and -31dBm.

The MLOCK bit will go high if the VCO signal to the local crystal oscillator is near the pull limit of the oscillator. This indicates that the oscillator has aged or other factors have forced the lock to near the frequency limit of the

local oscillator.

The NOLOCK bit will go true if the PLL is not locked.

PFAIL is set whenever the module powers up or is reinitialized. It is cleared by any channel command execution.

4.5 CTRL: MODULE CONTROL REGISTER

Bits in the CTRL register establish module operating and maintenance modes. Bits are...

Bit 0: NOCRC. When set, forces the CRC checker to the CRCOK state.

Bit 1: DSTOP. If this bit is set, the incoming OC3 data stream receiver will be disabled. The internal pattern-compare microengine may be tested by asserting DSTOP, poking 'fake' payload data into the memory, and triggering the microengine via the KICK bit in the TRIGS register. The channel MATCH bits will then show pattern match results.

Bit 2: OUT. When asserted, applies power to the optical or electrical output modules. OUT is cleared at powerup or by REINIT. If this bit is off, no channel output pulses can be generated.

4.6 TRIGS: TRIGGER REGISTER

The TRIGS register allows certain fast triggers to be generated within the module. This register appears to be a static read/write word location, but triggers are fired by the act of writing a "1" to each named bit.

Bit 0: VMETRIG. Writing a "1" to this bit fires timer channels which are programmed for VME triggers.

Bit 1: KICK. Writing a "1" to this bit kicks off a microengine pattern-compare run. After about a 22µsec delay, the nine channel-fire permissive flipflops (MATCH bits) will be asserted or cleared depending on the match between the payload data and the channel match/mask patterns. This is a maintenance function only.

Bit 2: SNAP. Writing a "1" to this bit requests that the next data payload be recorded in the snapshot region of the dual-port memory.

Bit 3: CCLEAR. When set, both the 'good' and 'bad' frame counters are cleared.

4.7 TMUX: TEST MULTIPLEXER REGISTER

The three LSBs of the TMUX register select the channel (0...7) whose output pulse signal is routed to the front-panel MONITOR output. Note that the OUT bit must be set for the output pulses to be active.

4.8 SERIAL: SERIAL NUMBER REGISTER

SERIAL displays the module serial number as an unsigned integer. The serial number is loaded into the module as part of the module calibration table.

4.9 CODE and REV: FIRMWARE ID REGISTERS

CODE displays the module firmware version, typically as decimal integer 22880; REV displays the revision letter, as an ASCII character in the LS byte, "B" typically. The combination of CODE:REV also uniquely defines the configuration of the two onboard FPGA chips.

4.10 GFRAME and BFRAME: FRAME COUNTERS

GFRAME and BFRAME are unsigned 16-bit counters. GFRAME counts good payloads, those with a proper fill, frame sync, and CRC. BFRAME counts bad frames, defined as fill followed by a "0" bit which is not the beginning of a good frame. Frames having correct framesync but bad CRC will be counted as good if the NOCRC bit is set.

'Bad Frame' will count at up to 10KHz if incoming frames occur at less than this rate. The 'bad frame' counter will be held clear for about 15 seconds after powerup or reinitialization to flush errors associated with achieving initial phaselock.

4.11 INIT: MODULE INITIALIZATION REGISTER

Writing hex value BAD1 to this register will reinitialize the module. This is equivalent to a powerfail/restart sequence.

4.12 CHANNEL CONTROL REGISTERS

Each timing channel has a dedicated control/status register. These registers are named C0 through C7. CREF is the corresponding control register for the reference channel. Bit functions are...

BIT	NAME	FUNCTION	M1	M0	
0	M0	trigger mode	0	0	off
			0	1	electrical trigger
1	M1	trigger mode	1	0	VME trigger
			1	1	normal (optical) trigger
2	RUN	enables continuous-mode triggering			
3	OS	oneshot: enables one trigger only			
7	CFLAG	command handshake bit			
8	ARMED	channel enabled to trigger			
9	BUSY	channel timer is running			

10	MATCH	true if microengine detects pattern match
11	OPTO	true if channel is configured for optical output
12	ELEC	true if channel is configured for electrical output

About 950 times per second, the internal processor will service the command register associated with each channel. The service logic is:

The internal microprocessor reads the channel command register

If CFLAG is true,

the channel is reset and disabled

the delay time specified in the three channel registers is read and installed into the channel counter and vernier

if RUN or OS are set, the channel is re-armed appropriately

the LS byte of the command register is written back with the OS and CFLAG bits false

end if

The MS byte of the command register is updated

Users should NOT write to the command register if the CFLAG bit is true, but should wait until the current command has been serviced.

The MS byte of the command register will be rewritten periodically, regardless of the command service outcome. This will update the realtime state of the status bits in the MS byte, but will not alter the LS command byte.

The VME master should preferentially use byte write operations on the LS command byte, and observe the CFLAG handshake protocol, and should not write to the MS byte of the command register. If the VME master does write to the MS byte, the channel status bits will be invalidated until refreshed by the next channel scan.

The two trigger mode bits select the trigger source for the channel.

Mode 0, OFF, prevents channel triggers, but any channel which has already been triggered will complete its current delay and output pulse.

Mode 1, Electrical Trigger, allows the channel to be triggered by the front-panel electrical trigger input.

Mode 2, VME trigger, allows a channel to be triggered by a write to the VMETRIG bit of the TRIGS register.

Mode 3 is the normal operating mode, in which triggers are generated by pattern matches with the OC-3 data stream.

The RUN bit allows the channel to trigger whenever a valid trigger is recognized.

The OS bit, if set, enables the channel to fire only once, at the next valid trigger event. This bit will self-clear when the command is executed. The OS bit is ignored if RUN is true.

The read-only OPTO bit will be set if an optical output module is installed for this channel, and ELEC will be true if the channel is configured for electrical output. Both bits will be false if...

The CONTROL register OUT bit is false, disabling power to the output modules.

An output subassembly module is not installed.

An output pulse transformer or laser diode has failed to open.

The ARMED bit will be true if RUN is asserted, or if a one-shot request was issued but the channel has not yet triggered.

The BUSY bit will be true while a channel timer is running (i.e., after a valid trigger but before the output pulse).

MATCH will be true if the last run of the pattern-match microengine has determined that the channel has a valid pattern match. This is useful primarily in DSTOP test mode.

4.13 CHANNEL TIME DELAY REGISTERS

Each of the eight timing channels has three delay-set registers, named "Hn", "Mn", and "Ln". The concatenation of these three registers represents a 48-bit channel time delay with an LSB value of 1 picosecond and a range of 3 seconds max. The "H" register represents the 16 most significant bits.

To load a new channel time delay, write the 48-bit time value to the three delay registers, then write the desired trigger select pattern and operating mode (RUN or ONE-SHOT) into the channel command register low byte, with the command register CFLAG bit set.

When a new time is recognized, the microprocessor will reset the delay channel, possibly aborting a pending output pulse; disable triggers for this channel; install the new time-delay values; and re-enable channel operation as permitted by the channel control register.

A few hex time-set examples are...

TIME	Hn	Mn	Ln
0	0000	0000	0000
1ns	0000	0000	03E8
1µs	0000	000F	4240
1ms	0000	3B9A	CA00
1s	00E8	D4A5	1000
3s	02BA	7DEF	3000

4.14 CHANNEL PATTERN REGISTERS

Each channel has eight pattern-match registers (named XnA-XnH) and eight pattern-mask registers (named KnA-KnH). A channel will trigger its delay generator at the next frame sync time if the previous frame data pattern matches the channel match words, masked by the channel mask words.

4.15 PAYLOAD FRAME BUFFER

The FSYNC through CRC words are the realtime received serial data payload. The PatA through PatH words are those used to qualify the channel match and mask patterns to determine when a channel is to be triggered. These words are written to VME-accessible memory registers as they are received. The MS bit of FSYNC is the first zero bit received following the detection of the all 1's 'fill' interval. For a normal data frame, FSYNC will contain 7FE2 hex.

In microengine test mode (DSTOP set in the module control register) it is possible to write to the frame buffer to simulate a serial data payload to the pattern-match logic.

4.16 PAYLOAD SNAPSHOT BUFFER

The LFSYNC through LCRC are a frozen snapshot of the realtime frame buffer, latched at the end of the first payload received following the assertion of the SNAP bit by the VME master. Users may wish to write all 1's to the LFSYNC word prior to requesting the snapshot; when the LFSYNC word changes to any other value (normally the frame sync pattern), the snapshot operation is complete.

4.17 OPL, TTC, OPC, OPX REGISTERS

The OPL register contains an unsigned binary number proportional to the realtime received optical power level, with LSB value of approximately 1nW; -20dBm (10 microwatts average power) will display about 10000 decimal. This word saturates at 65535, about -11.8dBm.

TTC is the time correction factor computed from the PC board surface temperature; it is a signed integer with LSB of 0.196ps. TTC is applied to the eight output channels and to the reference channel to correct for temperature drift.

OPC is the time-error corrector computed from the current optical power level; this is applied to all eight time verniers and the reference channel to adjust channel delays for optical power variations. It is a signed integer with LSB value of 0.196 picoseconds.

OPX is the raw ADC data corresponding optical receiver PIN diode current; it is used in module calibration. The LSB is roughly 2nw.

4.18 PCTEMP REGISTER

The PCTEMP register displays the realtime temperature of the printed-circuit board surface. The value is a signed integer with LSB of 0.01 degrees C. A typical value is 3200 (32.00 degrees C), which is about 12degC above ambient,

depending on air flow.

4.19 VCXO REGISTER

This register displays the realtime VCO control voltage at the input of the phase-lock crystal oscillator. It is a signed integer with LSB value of one millivolt. Normal range is -1 to -4 volts.

4.20 SCAN REGISTER

The SCAN register is a 16-bit counter which increments each time the channel command-service loop is executed. The average count rate is 949.21875Hz, the 155.52MHz clock rate divided by 163,840.

4.21 RXVX and RXTX REGISTERS

These registers control the FPGA test-point multiplexers; they do not affect normal operation.

4.22 CHANNEL MONITOR REGISTERS AN0...AN7

The channel monitor registers display the analog voltage at the drain of the power GaAsFets which drive the eight channel outputs. Scaling is 1mV per LSB. If the channel is configured for electrical output, the nominal value will be +5100, corresponding to +5.1 volts. If an optical output is installed, the indicated voltage will be about +3.5 volts. The indicated values will be nominally zero if the outputs are not enabled.

4.23 OTHER REGISTERS

Other registers are reserved for module maintenance functions, but writes to these registers will not affect module operation. Register 255 will never be written by the module (excepting powerup clear) so may be used as a read/write register for VMEbus data integrity testing, public flag storage, etc.

5. MODULE INSTALLATION AND TURNON

5.1 HANDLING AND INSTALLATION PRECAUTIONS

The V880 uses high-speed semiconductors which are static sensitive. Always use static protection in handling the module, and always transport it in the conductive antistatic bag furnished with the module.

5.2 INSTALLATION IN A VME CRATE

Install the V880 in a standard 6U VME crate.

NEVER INSTALL OR REMOVE THE MODULE WITH VME POWER ON.

ALWAYS SECURE THE FRONT-PANEL LOCKSCREWS BEFORE APPLYING POWER.

The V880 does not use interrupts and jumps all interrupt and bus request grant lines. VME backplane IRQ and grant jumpers may be left in place or removed without affecting downstream modules.

5.3 POWERUP

At powerup, both the LOCK and TRIG indicators will light. In about one second, the LOCK LED will go off, VME will blink briefly, then all LEDs will go out, indicating that the powerup initialization and FPGA configuration sequences are complete. After this powerup interval, the module begins normal operation. LOCK will then illuminate when solid data frames are received.

If the SX DIPswitch is set ON, the module will not execute its normal functions and will not access the VME register file. In this state, one may run read/write memory diagnostics on the VME register set. When SX is set to OFF, all registers are cleared and normal module operation resumes.

At powerup, all channel control registers, pattern match registers, and channel delays are zeroed, and the output stage power supply is turned off.

At powerup, the V880 will read the primary calibration table from the onboard serial EEPROM memory. If this table appears to be intact, it is installed as the active calibration table. If not, the second (backup) copy is read from EEPROM; if the backup looks correct, it is used and the ALT bit set in the module status register. If neither table is correct, the default cal table is installed and the DEFAULT bit is set in the status register. The unit serial number will show as 100 if the default table is used.

6. OPTICAL DATASTREAM DESCRIPTION

The V880 accepts a 155.52Mbaud serial datastream which is compatible with physical-level OC-3 fiberoptic transmitter and receiver components.

The serial stream is biphase encoded at a bit rate of 77.76MHz. A "1" is defined as a high:low (light:dark) squarewave cycle of 12.86ns duration, and a "0" is a low:high cycle.

Data is organized into repetitive frames; a frame consists of a block of 'fill' (all 1's) followed by a payload. The standard frame is 405 bytes, 3240 bits, and is 41.666 microseconds in duration.

The dataframe consists of 3080 fill bits followed by 160 payload bits. The payload is divided into ten 16-bit words, named Framesync, time pattern words PatA through PatH, and CRC. Each word is expressible as a 4-character hex value, with the MSB transmitted first in time.

Framesync is hex pattern 7FE2. The eight time-pattern words are 128 bits of time flags which may be used arbitrarily to define periodic time (counter) fields, single-event triggers, or in any other structure that is of experimental significance.

The CRC is the polynomial checksum of the eight pattern words, beginning with PatA, using the CRC-16 polynomial X^16 + X^15 + X^2 + 1.

A typical payload with correct CRC is, in hex,

Fsync	PatA	PatB	PatC	PatD	PatE	PatF	PatG	PatH	CRC
7FE2	53B5	5B88	812E	D02F	3710	B477	9AED	354B	B63D

The V880 will trigger a delay channel at the end of the Framesync word, provided that the previous payload had a good framesync, a good CRC, and that the channel had a pattern match against the eight payload pattern words. 'Pattern match' means the 128-bit logical test...

(Pat xor Match) or Mask = all 1's

where Match is this channel's 128-bit match pattern delivered by the VME port, and Mask is the channel's 128-bit 'don't care' pattern, also from VME.

7. MODULE CALIBRATION

7.1 CALIBRATION OVERVIEW

In order to meet specifications for accuracy and stability, each V880 must be individually calibrated. A 176-word calibration table must be present in the module's volatile (runtime) memory for normal operation.

Two copies of the cal table are created during factory calibration and are stored in nonvolatile EEPROM. At module powerup time, the first table is loaded into working RAM, checked for validity, and used if valid. If the primary table is corrupted, the backup is tried and, if it is also corrupt, the EPROM-resident default cal table is used. The module status register indicates the calibration status.

The calibration table contains the following data items:

1. Calibration status word, indicating calibration state. Defined states are Final, Default, and Partial.

2. Calibration type: Standard or Precision.

3. Calibration date and time.

4. Unit serial number. This integer is the source of the VME-readable serial number.

5. A temperature:delay compensation factor.

6. For each of the eight internal delay generators, a pair of cal factors which adjust channel time offset and delay vernier slope.

7. A 129-element lookup table which corrects module delay as a function of incoming optical power level. The module measures actual optical power level and interpolates between table entries to correct for optical receiver delay errors.

8. Offset, optical power, and temperature correction factors for the Reference channel.

9. A 16-bit cal table checksum.

A test and calibration program V880C.EXE is available to assist in module calibration, and the Model V888 optical pattern generator is available to generate the optical payloads and time-sync pulses required for module calibration.

7.2 CAL: CALIBRATION CONTROL REGISTER

The CAL register is used to manage module calibration.

For normal operation, this register should be left at its powerup value of zero.

To enter calibration mode, write hex value CA02 to the CAL register. The module will reset all timing channels, load the current cal table into the VME buffer space, and clear the low byte of CAL to indicate done. CAL will then be CA00

hex, indicating cal mode.

CAL mode commands are requested by loading a command code CAxx into the CAL register and waiting for the V880 to respond. The V880 will set CAL to CA00 when a command is finished. To exit cal mode, clear the CAL register, wait at least 10 milliseconds, then reload channel parameters as desired.

CAL command codes are...

```
    CA00  -------      COMMAND DONE STATE
    CA01  DEFAULT      INSTALL DEFAULT CAL TABLE
    CA02  READ         COPY CAL TABLE TO VME, STARTING AT REG 16
    CA03  WRITE CAL    COPY FROM VME TO CAL TABLE IN RAM
    CA04  GET  EE1     COPY EEPROM BLOCK 1 TO CAL TABLE AND VME
    CA05  GET  EE2     DITTO EE BLOCK 2
    CA06  SAVE EE1     SAVE CAL TABLE TO EEPROM BLOCK 1
    CA07  SAVE EE2     DITTO EE BLOCK 2
```

7.3 CSTAT: CALIBRATION STATUS REGISTER

This register presents calibration status:

```
   10FC hex: final calibration table loaded
   1001 hex: partial calibration
   10DF hex: default cal table is loaded
```

7.4 CALSUM: CALIBRATION CHECKSUM REGISTER

This register displays the 16-bit checksum of the calibration table.

7.5 INH: CALIBRATION INHIBIT REGISTER

This register can selectively inhibit the application of various internal calibrations.

Individual calibrations may be inhibited by writing hex value 41xx to the INH register, where the LS bits "xx" are...

```
  bit 0: if set, inhibits optical power level corrections
  bit 1: inhibits PCB surface temperature corrections
  bit 2: inhibits vernier offset and slope corrections
  bit 3: inhibits periodic (about 1/sec) vernier refresh operations
  bit 4: inhibits reference channel compensations
```

This register should normally be left clear.

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