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HIGHLAND TECHNOLOGY

MODEL V680 8-CHANNEL VME TIME-TO-DIGITAL CONVERTER MODULE TECHNICAL MANUAL

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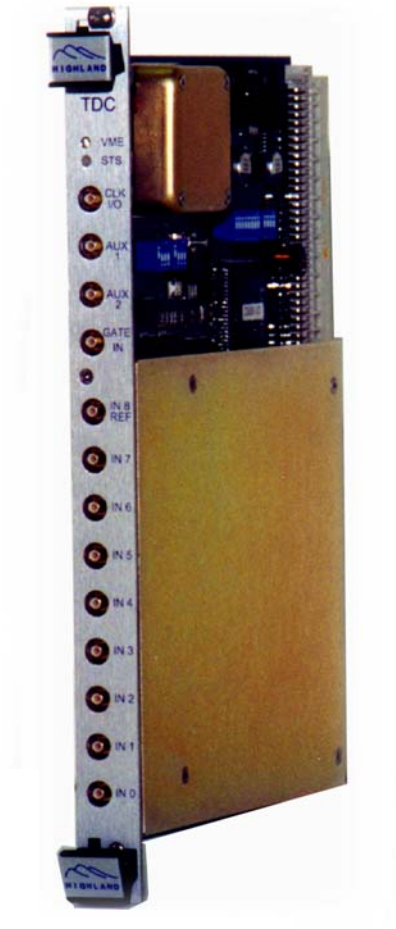
1. Introduction

The V680 is an eight-channel time measurement module packaged as a single-width, 6U, 16-bit VME module.

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V680 8-CHANNEL TIME -TO –DIGITAL CONVERTER VME MODULE



FEATURES

- 8-channel, 48-bit, 48-picosecond resolution TDC.
- Measures events up to 6800 seconds before or after common trigger, or 0 to +13,700 seconds after trigger.
- Adjustable trigger levels and edge polarity.
- Usable as a 9-channel independent time-stamper.
- Fast readout available 200 ns after events.
- Jitter typically below 40ps RMS.
- Ultrastable, ovenized quartz crystal timebase may be locked to an external source.
- Optional custom internal microengine can qualify and analyze timing events.

The V680 is an 8-channel time-to-digital converter used to record the time of occurrence of eight independent electrical pulse inputs, each measured relative to a single, common reference input. Each input channel can time its event "hit" with 48.82-picosecond resolution and 48-bit dynamic range.

The module has provisions for adjustable input logic levels, selectable input edge polarity, and selectable termination.

The V680 employs a highly linear interpolation technique which requires a minimum of adjustments. Data is available within 200 ns of the completion of the measured time intervals, and the module may be cleared and rearmed in less than one microsecond. All features are switch selectable.

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SPECIFICATIONS: MODEL V680 8-CHANNEL TDC

CONFORMANCE:	Complies with ANSI/IEEE 1014-1987 VMEbus specification. Meets the VXIC specification, Revision 1.4.
DEVICE TYPE:	Register based slave: A16:D16:D08(EO).
PACKAGING:	Single-width, 6U VME, B-size VXI module.
POWER REQUIRED:	+5 : 2.8 A max ; +12 : 1.1A max (start-up), 600 mA max after warm-up; -12 : 1.4 A max(start-up), 800 mA after warm-up.
INPUTS:	One common reference input (T8). Eight individual event inputs (T0-T7). One external input (GATE) enables event channels. Two inputs (AUX) support custom control logic. One clock I/O (CLK).
INPUT LEVELS:	The thresholds of the event inputs are adjustable as a group in the range of ±2.5 V. Their impedance (high-Z or 50 ohms) and polarity (rising or falling edge) can also be selected individually. The GATE input has a separate threshold level adjustment. Its impedance (high-Z or 50 ohms) and polarity (high or low) are also selectable. The AUX inputs are TTL-compatible.
OUTPUTS:	AUX1 normally indicates that module is armed and ready to accept an event.
RESOLUTION:	48.828125 ps, equivalent to 20.48 GHz clock.
RANGE:	$\pm 2^{47}$ counts (±6871 seconds) for bipolar mode.
JITTER:	Less than (75 ps + 2×10^{-9} x measured time) RMS.
LINEARITY:	±0.25 LSB.
TIMEBASE:	Internal ovenized crystal oscillator. Accuracy is 0.01 ppm/deg C; aging < 1 ppm/year. Internal phase-lock-loop allows utilization of an external 10 MHz timebase.
INDICATORS:	LEDs indicate VME access and acquisition/readout mode status.
CONNECTORS:	Standard SMB; optional LEMO.

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2. Specifications

FUNCTION	8-channel time-interval measurement module. Times-of-trigger of eight input channels are measured relative to time-of-trigger of the reference channel input. In timestamp mode, all nine inputs independently report trigger timestamps.
CONFORMANCE	Conforms with ANSI/IEEE 1014-1987 VMEbus specifications. Meets VXIC VXI specifications. Rev 1.4 for B-size VXI module.
PACKAGING	Single-wide 6U Eurocard.
DEVICE TYPE	16-bit VME register-based slave: A16:D16:D08(EO); implements 32 16-bit registers at or above C000h in the VME short addressing space.
INPUTS	Nine channels; 0...7 are standard inputs, Ch 8 is reference. One GATE input. One CLOCK input/output. Two special-purpose TTL-level AUX inputs/outputs.
LEVELS	Time inputs 0...8, switch selectable as a group for TTL, ECL, NIM, or user-set thresholds; GATE input is switchable for TTL/ECL/NIM/User. All inputs are switchable for polarity (±) and termination (50 ohms to GND or Hi-Z). AUX1, AUX2, CLOCK: TTL/HCMOS compatible.
RESOLUTION	48.828125 picoseconds/LSB; equivalent to 20.48GHz clock.
RANGE	48 bits; ±6871 seconds bipolar or +13,743s unipolar.
JITTER	<75ps + timebase jitter, RMS. Internal timebase jitter is less than 2E-9 * measured time.
LINEARITY	Integral, <0.5LSB; differential, <1%.
TIMEBASE	Internal ovenized crystal oscillator. TC below 2E-9/degC, aging below 1PPM/year; lockable to external 10MHz TTL reference or to another V680 or V850 module.
CONNECTORS	LEMO or SMB.

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3. Functional Model

The V680 time interval counter module functions as follows:

There are nine input channels, numbered 0 through 8, with Channel 8 being considered the reference channel for relative-time measurements. Each channel includes an input discriminator, a 'hit' flip-flop, and a 48-bit time latch.

A single 'master' 48-bit counter drives the inputs of all nine-channel time latches. When any channel recognizes a valid trigger event, its hit flip-flop is set and the value in the master counter is copied into the channel latch register and saved as the timestamp of the channel trigger event. The state of the nine hit flip-flops may be read in the hit register to indicate which, if any, channels have valid timestamps frozen in their latches.

The master counter consists of a 38-bit, 20MHz physical counter. Time interpolation circuits extend the counter to its full 48-bit dynamic range, with the counter LSB having a weight of 48.828125 picoseconds, corresponding to an equivalent count rate of 20.48GHz. The full range of the counter is about 13,743 seconds.

The module may be used in either of two timing modes: standard mode and timestamp mode. In standard mode, the event time associated with a hit on Channel 8 is considered to be the module reference time, and the time of all hits on Channels 0...7 are reported relative to this reference time. The value reported for Channels 0...7 is the difference between the channel timestamp and the reference timestamp, in the range of ±6871 seconds, with a positive difference indicating that the channel trigger happened after the channel 8 reference event. If the Channel 0...7 hits are known to happen after the Channel 8 trigger, the time difference may be interpreted as a positive value from 0 to 13,742 seconds.

In timestamp mode, the actual timestamp of each channel is reported as the channel's time-of-hit, with all nine channels behaving identically. Here, time is relative to the last time that the master counter was cleared. When each channel is triggered, its hit flag may be observed as an indication that the channel has fresh data; the data may then be read and the channel cleared and rearmed in preparation for a new event.

A positive-only mode is selectable; in this mode, triggers on Channels 0...7 are ignored until after a hit is sensed on Channel 8. The minimum measurable 'positive only' time is typically 4 nanoseconds.

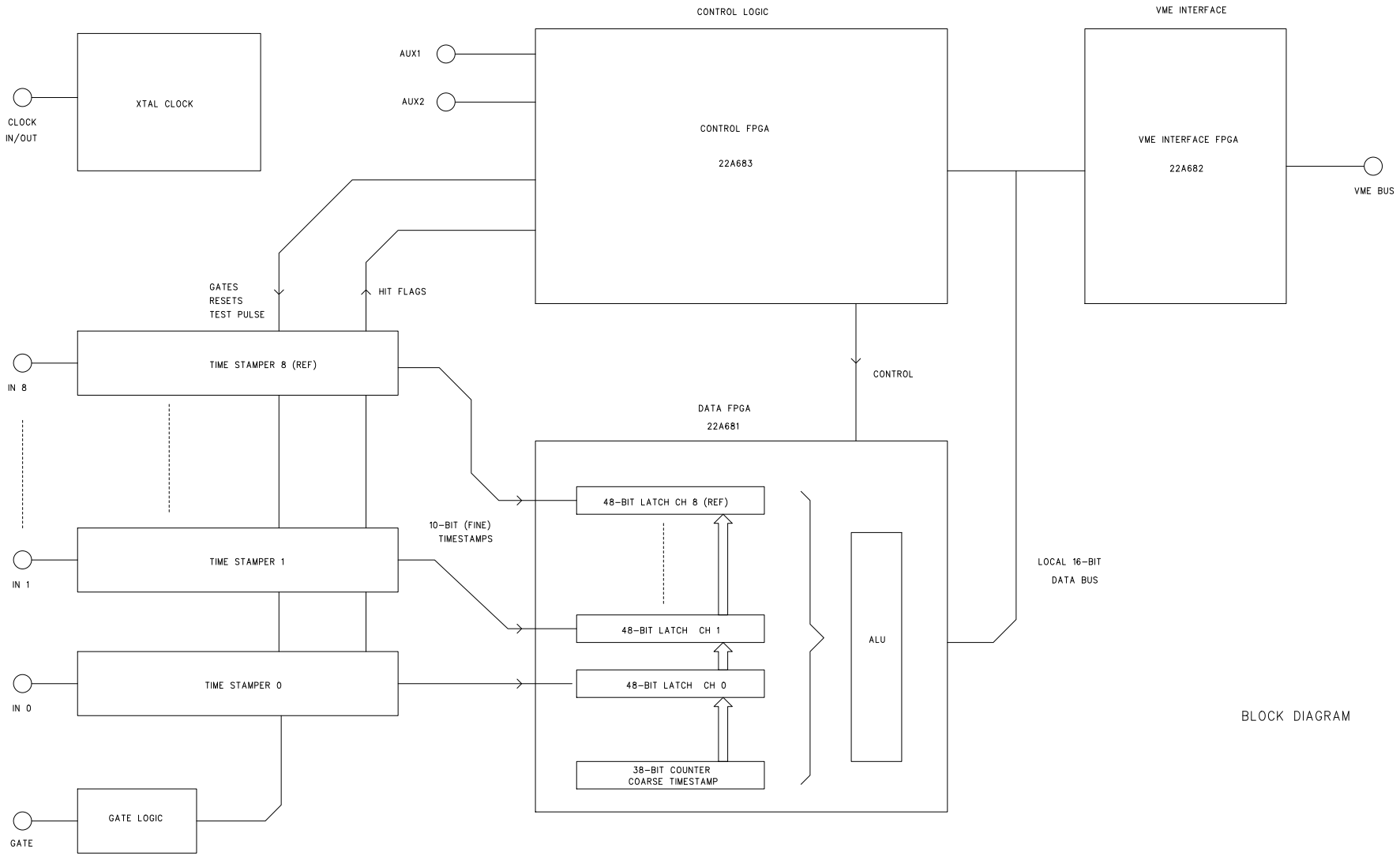
A double-hit register is provided to indicate when a second active trigger edge is sensed on any input channel while the gate is still true. The time of the first hit is always reported. Double-hit resolution is typically 3 nanoseconds.

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The master counter and time interpolators are driven by an on-board precision 40MHz ovenized crystal oscillator. This oscillator may be phase-locked to an external 10MHz system reference clock, to another V680, or to a V850-series digital delay generator, permitting accurate interval or timestamp measurement across any number of modules and channels. Because of the inherent time uncertainty associated with clearing the master counter in any given module, absolute timestamps between modules may differ considerably. For accurate multi-module time measurements, standard (e.g., channel-8-relative) timing mode should be used, with a common external trigger applied to Channel 8 of all modules to synchronize their time references to sub-nanosecond precision.

Timestamp mode can be used for accurate period measurements of up to nine independent signals, or may be used to perform up to four independent bipolar start-stop measurements using paired channels.

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BLOCK DIAGRAM

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4. Electrical Inputs

The V680 has 12 front-panel input connectors, optionally SMB or LEMO coaxial types. Inputs are as follows:

8/REF	Reference (Channel 8) input.
0…7	Eight channel inputs.
GATE	Hit enable gate.
CLK	Clock in/out.
AUX1	Auxiliary TTL input/output.
AUX2	Auxiliary TTL input/output.

4.1 Channel Inputs

The REF and 0...7 channel connectors connect to the nine input channel discriminators.

A switch is provided to set the thresholds of Channels 0...8 as a group to TTL, ECL, or NIM levels (+1.25, -1.25, and -0.4 volts respectively).

Each input is individually switch selectable to be a high impedance or 50-ohm-to-ground termination, and each has a selector switch for positive- or negative-edge input.

4.2 Gate Input

The GATE input, when asserted, enables the nine channel inputs to accept trigger edges. Switches are provided to select gate termination, threshold level, and polarity. The GATE input may be forced into the 'enable' state by the software FGATE bit.

When the GATE input polarity switch GP is switched to the '+' position, a positive GATE input enables hits.

The GATE input may be individually selected for TTL/ECL/NIM and user-set threshold levels.

4.3 Clock Input/Output

CLK is a TTL-compatible signal. When the module is in internal clock mode, this is a 10MHz output. When the module is in external clock mode, this is an input, and the internal crystal oscillator will phaselock to a 10MHz TTL signal applied to this connector. A switch is provided to select clock mode.

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When the module is used in internal clock mode, the CLK connector is an output. The signal is a 10MHz square wave at HCMOS levels, source-terminated at 50 ohms. It may be run through a 50-ohm coaxial cable directly to a terminated or unterminated oscilloscope or frequency counter input to verify the presence and frequency of the internal clock. The clock output of one V680 may also be used to drive up to four additional V680 units which are operating in external clock mode, such that the four 'slave' units will phase-lock to the single 'master' clock. Total cable length from the master unit to the last slave should not exceed three feet; if cables need to be longer or drive more loads, a buffer amplifier (such as the Model V860 Pulse Amplifier Module) will be required.

If an external 10MHz clock is used to drive one or more V680 units, the signal may be daisy-chained through up to four V680s, with the signal source- or end-terminated.

4.4 Aux Input/Outputs

The AUX connections are discussed in Section 6.4.

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5. VME Register Map and Programming

The following is a summary of the VME-accessible registers implemented by the V680-series modules. The module follows VXI conventions, having 32 16-bit registers located in the high 4K of the short VME address space. A DIPswitch on the module sets the base address, beginning at C000 hex.

All registers are 16 bits wide. REG # below is the ordinal register number in decimal; OFFSET is the VMEbus address offset from the module base address, shown in hex. The R/W column indicates whether the register is readable and/or writable from the VMEbus.

Reg Name	Reg#	Offset	R/W	Function
VXI MFR	0	00	R	VXI manufacturer ID: always 65262, FEEE hex.
VXI TYPE	1	02	R	Module type, always 22680, 5989 hex.
VXI STS	2	04	R	VXI status register, always FFFF hex.
VECTOR	3	06	RW	VME interrupt vector register.
CONTROL	4	08	RW	Module CONTROL register.
HIT	5	0A	R	Channel HIT flags register.
DBLHIT	6	0C	R	Channel double hit flags register.
IRQMASK	7	0E	RW	Interrupt enable mask register.
RESETS	8	10	W	Channel/module reset bits.
SELECT	9	12	RW	Data readout select register.
T0	10	14	R	MS 16 bits of time.
T1	11	16	R	Mid 16 bits of time.
T2	12	18	R	LS 16 bits of time.

Registers 13-31 are reserved for future use.

Registers are described in detail below. Within each register, bits are numbered 0 (LSB) through 15 (MSB).

5.1 VXI MFR Register: VXI Manufacturer's ID

This register displays the VXI-registered manufacturer's ID code. It always reads as FEEE hex.

5.2 VXI TYPE Register: Module Type

This register displays the module type. It normally reads as 22680 decimal, 5898 hex; special-function modules may display different codes.

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Register Map

Reg #	Hex Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
0	C000	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	VXI MFR ID	ALWAYS FEEE HEX
1	C002	0	1	0	1	1	0	0	0	1	0	0	1	1	0	0	0	VXI TYPE	22680 DECIMAL, 5898 HEX
2	C004	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	VXI STS	ALWAYS FFFF HEX
3	C006	0	0	0	0	0	0	0	0	V7	V6	V5	V4	V3	V2	V1	V0	IRQ VECTOR	
4	C008						uENGINE ENABLE	GATE STS		THTEST	GTTEST	ET8	SYNC TEST	IRQ FLAG	POS TIME MODE	FORCE GATE	GATE	CONTROL	
5	C00A						uENG FLAG	GATE FLAG	HIT 8	HIT 7	HIT 6	HIT 5	HIT 4	HIT 3	HIT 2	HIT 1	HIT 0	HIT	
6	C00C								DBL HIT 8	DBL HIT 7	DBL HIT 6	DBL HIT 5	DBL HIT 4	DBL HIT 3	DBL HIT 2	DBL HIT 1	DBL HIT 0	DOUBLE HIT	
7	C00E						uENG IE	GATE FLAG IE	IE 8	IE 7	IE 6	IE 5	IE 4	IE 3	IE 2	IE 1	IE 0	INTERRUPT ENABLES	
8	C010					CLRCTR	uENGINE RESET	GATE FLAG RESET	RESET 8	RESET 7	RESET 6	RESET 5	RESET 4	RESET 3	RESET 2	RESET 1	RESET 0	RESETS	
9	C012						uA2	uA1	uA0				DS1	DS0	CH2	CH1	CH0	READOUT SELECT	
10	C014	T47															T32	T0 MS TIME	
11	C016	T31															T16	T1 WID TIME	
12	C018	T15															T0	T2 LS TIME	
13	C01A	T47															T32	U0 MS uENG TIME	
14	C01C	T31															T16	U1 MID uENG TIME	
15	C01E	T15															T0	U2 LS uENG TIME	

NOTE: HEX ADDRESSES ASSUME MODULE BASE ADDRESS IS SELECTED AS C000 HEX.

uENGINE FUNCTIONS ARE OPTIONAL.

READOUT SELECT CODES ARE AS FOLLOWS:

DS1	DS0	CH2	CH1	CH0	ITEM SELECTED
0	0	N	N	N	RELATIVE TEIM, CHANNEL N
0	1	N	N	N	TIMESTAMP, CHANNEL N
1	0	0	0	0	CHANNEL 8 TIMSTAMP
1	1	0	0	0	TIMSTAMP COUNTER

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5.3 VXI STS Register: VXI Status Register

This register always reads all 1s (FFFF hex).

5.4 Vector Register

This user-loaded register determines the VMEbus vector asserted during interrupt cycles. Only the low eight bits are active. The appropriate value must be loaded before enabling interrupts.

5.5 Control Register

Bits in this register establish module-operating modes.

Bit	Name	Function
0	GATE	Gate/enable bit for inputs 0…8.
1	FGATE	Forces GATE state true.
2	POS	Forces positive time measurement mode.
3	IRQFLG	True if interrupt is requested by module.
4	SYNC	If set, the ET8 test is synchronous to local clock.
5	ET8	Triggers the self-test chain; write-only.
6	GTEST	Tests the gate threshold detector.
7	TTEST	Tests threshold detectors 0…8.
9	GSTAT	Realtime state of the GATE input.

Channel hits are enabled if the GATE bit is set and the external GATE input is true. If FGATE is set, the external gate input is forced true. Setting GATE and FGATE enables triggers unconditionally.

If the POS bit is set, Channels 0...7 can be triggered only AFTER the reference channel, Channel 8, is triggered. This ensures that measured relative times are always positive. Channels 0...7 are enabled about 3 nanoseconds after Channel 8 is triggered.

Bits 4, 5, 6, and 7 are used for module testing. If the module gate is enabled and all channel inputs are in the inactive state, writing a '1' to the ET8 bit will 'fire' all nine channel inputs in sequence, with a channel-to-channel separation of about 1 nanosecond. This trigger is asynchronous to the internal clock so it may be used to measure and adjust channel jitter. If the SYNC bit is set, the ET8trigger is synchronous to the internal clock; this can be useful for certain signal-probing applications.

If the channel threshold and gate threshold DIPswitches are both set to their NIM positions, all thresholds will be programmed to -0.4 volts. Then, if the GTEST bit is set, the gate threshold will change to +0.4 volts; similarly, TTEST will change the channel thresholds to +0.4 volts. These bits may be used to test the gate and channel input discriminator circuits.

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Bit 9 indicates the immediate state of the GATE input; a '1' indicates that timing channels are enabled to accept hits. FGATE can force this bit high. Note that GSTAT indicates the logical gate state, not the electrical state; that is, if the gate polarity is switch-selected as negative, hits are enabled when the electrical gate input is negative.

5.6 Hit Register

Bit	Name	Function
0…8	HITn	Status of HIT flip-flops for Channels 0…8; a '1' indicates that the associated channel has been triggered at least once since last channel reset.
9	GATEFLAG	This bit is asserted at the fall of the GATE state, whether GATE was asserted by an external GATE input or by the FGATE control register bit. It is cleared by the GATE FLAG RESET bit in the RESETS register.

5.7 Doublehit Register

Bit	Name	Function
0…8	DHITn	Status of DOUBLEHIT flip-flops for Channels 0…8; a '1' indicates that the associated channel has been triggered two or more times while the GATE state was true.

5.8 IRQ Mask Register

Bits 0...8 of this register are channel interrupt-enable bits. A VME interrupt request will be generated if

```
(HITn .and. MASKn) <> 0
```

that is, if any channel has a hit (indicated by a '1' in the HIT register) and the corresponding mask bit is set, an IRQ will be requested.

Bit 9 enables interrupts at the end of the GATE state, namely when the GATE FLAG bit is true.

Bit 10 enables optional microengine interrupts.

5.9 Reset Register

Bits 0...8 of this register, when written as 1s, clear Channels 0...8 respectively. Writing a '1' to any bit clears the HIT and DOUBLEHIT flip-flops for that channel and prepares the channel to accept a new event trigger.

Writing a '1' to bit 9 clears the GATE FLAG.

Writing a '1' to bit 10 clears the optional microengine.

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Writing a '1' to bit 11 clears the master 48-bit timestamp counter. If the module is used in standard mode, the counter need not ever be cleared. In timestamp mode, users may wish to clear the master counter just prior to expected trigger events such as to keep returned 48-bit timestamp values small, or to avoid dealing with possible 13,743-second timestamp rollovers.

The RESET bits do not latch, and always read back as 0s.

5.10 Select Register

The five low bits of this register select the data to be presented in the three time-readout registers.

Bit select patterns are as follows:

4	3	2	1	0		
DS1	DS0	CH2	CH1	CH0	Hex	Data selected for readout
0	0	0	0	0	00	Relative time, Channel 0
0	0	0	0	1	01	Relative time, Channel 1
0	0	0	1	0	02	Relative time, Channel 2
0	0	0	1	1	03	Relative time, Channel 3
0	0	1	0	0	04	Relative time, Channel 4
0	0	1	0	1	05	Relative time, Channel 5
0	0	1	1	0	06	Relative time, Channel 6
0	0	1	1	1	07	Relative time, Channel 7
0	1	0	0	0	08	Timestamp, Channel 0
0	1	0	0	1	09	Timestamp, Channel 1
0	1	0	1	0	0A	Timestamp, Channel 2
0	1	0	1	1	0B	Timestamp, Channel 3
0	1	1	0	0	0C	Timestamp, Channel 4
0	1	1	0	1	0D	Timestamp, Channel 5
0	1	1	1	0	0E	Timestamp, Channel 6
0	1	1	1	1	0F	Timestamp, Channel 7
1	0	0	0	0	10	Timestamp, Channel 8
1	1	0	0	0	18	Master Counter

5.11 Time Readout Registers: T0, T1, T2

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The T0, T1, and T2 registers contain time data for the item named in the SELECT register. The three 16-bit registers contain a 48-bit time value, with T0 being the most significant 16 bits and T2 being the least significant. For relative times (select codes 0...7h), this data represents the time DIFFERENCE between the channel's hit time and the hit time of Channel 8, the reference time channel. The data is valid only if the selected channel AND Channel 8 both have their 'hit' flags set.

For select codes 08...10h, the data represents the timestamp value for Channels 0...8. This data is valid only if the selected channel has a hit.

Select code 18h selects the timestamp counter. The 10 LSBs will always read as zeroes, and the remaining bits will count in real time.

5.12 Reading Time Registers

The SELECT register is used to select which channel is read out in the Tn registers, and whether the data is an absolute time stamp (available for all nine channels) or a relative time (Channels 0...7 only).

If a single channel 0...7 has its 'hit' flag set in the STATUS register, its timestamp value may be read in the T0:T1:T2 registers by writing the proper channel timestamp SELECT code. If the reference (Channel 8) hit is also asserted, then the channel's relative time value may also be read in T0:T1:T2, after asserting the appropriate SELECT code.

To read a time value for Channels 0...7, first check the STATUS register to see if the channel has its HIT flag set. If it is desired to read relative values, verify that the Channel 8 HIT flag is set as well. Next, write the proper code into the SELECT register, then read the three 'T' registers. After data is read, the channel may be cleared and rearmed by writing the appropriate RESET register bits.

The 3-word (48-bit) 'Tn' value represents either the value in the 48-bit master timestamp counter, effective the instant that the channel was triggered, or, if relative time is selected for readout, the 3-word value is the time of Channel 0...7 trigger relative to the time of the Channel 8 trigger. The net value of a timestamp or relative time is as follows:

```
T = ((T0 * 65536) + T1) * 65536 + T2
```

where the 'Tn' words are considered to be unsigned 16-bit integers, and the net LSB value is 48.828125 picoseconds. Note that the counter overflows every 2^48 counts, about every 13,743 seconds. For time in seconds, just multiply the computed 'T' value by 48.828125E-12. When measuring relative times, counter overflow may be ignored.

If the channel triggers may occur before or after the reference, the relative time data in the Tn registers must be interpreted as a 48-bit, 2s complement signed integer. Use the formula above, but if the MSB of the result is set (e.g., if T exceeds +140,737,488,355,327), then subtract 281,474,976,710,656 from the computed value). Again, the result is in units of 48.8ps, but here the corrected 'T' represents a time from -6871 to +6871 seconds relative to the reference hit.

To maintain full accuracy within application programs, the 3-word time values should be handled as 64-bit integers or as double-precision floating-point values.

If it is certain that a relative time interval will not exceed 209 milliseconds (±104 ms in bipolar cases), then the MS time register value (namely the T0 register) can be ignored, and the T1:T2 register pair can

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be processed as a signed or unsigned 32-bit value.

The reprate of time measurements is limited only by VMEbus access speed.

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The following PowerBasic code fragment reads Channel 5 relative time and converts the data into double-precision floating-point time values TU# (unsigned time) and TS# (signed), both in seconds.
The program assumes that the VME registers are directly accessed as elements of the V( ) array, as unsigned integers. All program variables are unsigned 16-bit integers except '&&' types which are 64-bit signed integers and '#' types which are double-precision floaters.

```
DIM ABSOLUTE V(32767) AT VSEG       'THROW V() ARRAY ONTO VME SPACE

BASE = &HC000/2                     '= MODULE BASE ADDRESS, AS WORD

T0 = BASE + 10                      'DEFINE TIME REGISTERS RELATIVE
T1 = BASE + 11                      'TO MODULE BASE ADDRESS, NOTE THAT
T2 = BASE + 12                      'THESE ARE *WORD* ADDRESSES!
RD = BASE + 9                       'DEFINE READOUT SELECT REG, TOO

V(RD) = 5                           'SELECT CHANNEL 5, RELATIVE TIME

T0D = V(T0)                         'READ MS TIME,
T1D = V(T1)                         'MID TIME,
T2D = V(T2)                         'AND LS TIME AS UNSIGNED 16S

T&& = T0D                           'MAKE A COMPOSITE TIME VARIABLE
SHIFT LEFT T&&, 16                  'T&&' IN V680 LSB'S
T&& = T&& + T1d                     '
SHIFT LEFT T&&, 16                  '(DATA IS 48 BITS, SO WE MUST
T&& = T&& + T2D                     'DO QUAD-WORD 64-BIT MATH)

TU# = 4.8828125E-11 * T&&           'FLOAT THAT, IN SECONDS
                                    'AS UNSIGNED TIME

S&& = T&&                           'COPY 48-BIT STUFF
                                    'AND
IF(S&& AND &H400000000000) THEN     'SIGN EXTEND
S&& = (S&& OR &HFFFF400000000000)   '48-TO-64 IF REQUIRED
END IF

TS# = 4.8828125E-11 * S&&           'FLOAT THAT, IN SECONDS
                                    '(LSB IS WORTH 48.8 PICOSECONDS)
                                    'THIS IS 'SIGNED TIME IN SECONDS'
```


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5.13 Interrupts

The V680 uses the RORA (reset on register access) VME interrupt mechanism. Internal to the module, all bits of the INTERRUPT ENABLE register are logically ANDed with corresponding bits of the HIT register. If any bit pair ANDs to 1 (e.g., any pair of bits is 1:1) then the IRQ state is true. If interrupts are enabled by the IRQ DIPswitch, the IRQ state asserts and holds one of the seven available VME interrupt request lines until the IRQ state is cleared by the user's interrupt service routine. Note this is a static (rather than an edge-triggered) interrupt system.

The GATE FLAG may be enabled to generate interrupts by setting bit 9 of the interrupt enable register. In this case, an interrupt will be requested at the end of the channel-enable gate.

To enable interrupts, proceed as follows:

1. Set the IRQ DIPswitch to the desired interrupt level, 1 to 7. Selecting level 0 will disable interrupts. If level 7 is an NMI to the host processor, it should not be used here.
2. Write the desired IRQ vector number into the VECTOR register.
3. Assert the desired bits in the INTERRUPT ENABLES register.

An interrupt service routine must run at a priority level sufficiently high that it cannot be re-interrupted by the module. The ISR must take actions to clear the interrupting condition (typically, it reads out and resets channels having hits) before exiting.

5.14 Microengine

The V680 has a optional custom microengine capability that may be useful in high data rate applications. An internal programmable gate-array may be configured to perform simple internal sequencing, data routing, and buffering operations. The microengine can qualify or discard certain events, automatically reset channel hits, and store and buffer 'good event' data. Contact the factory for more information on the capabilities of this option.

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6. Input and Output Connections

6.1 Channel Inputs 0...8

Use high-quality, low-loss coaxial cables to connect to the channel trigger inputs. Note that long lengths (ten feet or more) of high-loss cable can seriously degrade risetimes and increase apparent jitter. For minimum jitter, input signals should have a high rate-of-rise, on the order of 1V/ns, and not be contaminated by noise or 60Hz ground loops. To avoid input damage, ensure that peak input potentials cannot exceed ±5 volts, and that the cable signal conductor is not charged to a higher potential.

6.2 Gate Input

The GATE input is electrically similar to the channel inputs.

6.3 Clock Input/Output

The CLOCK input is a TTL/HCMOS compatible input/output. It is discussed in Section 4.2.

6.4 AUX1, AUX2, and LEDs

Two front-panel LEDs are provided. The blue VME LED flashes whenever the module is accessed from the VME bus.

The STS LED will light up as follows:

GREEN	When the module is armed, gated, and ready to accept a reference channel hit.
RED	When a reference channel hit has occurred.
OFF	Otherwise.

The AUX1 output is a TTL level which goes high when the module is armed, gated, and ready to accept a REF channel pulse (e.g., when the STS LED is green). AUX2 is currently unused. If the module is not powered, both AUX signals will be pulled low (via internal CMOS protection diodes to the +5V supply).

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7. Setup and Installation

7.1 Handling Precautions

The V680 uses high-speed silicon and gallium arsenide surface-mount components which may be damaged by electrostatic discharge or by mechanical abuse. **Handle the module carefully.** Do not place the module in a rack or on a surface, or hand it to another person, without first touching that object or person to ensure that the transfer is equi-potential (i.e., the V680 is not a static discharge path).

When inserting or removing the module into/from a VME cage, take care not to damage the solder-side trimpots and switches.

Never insert or remove the V680 when the VME card cage is powered up.

7.2 Switch Setups

Before installation, the following switches should be set up:

- **VME ADDRESS** The VME ADDRESS DIPswitch (S2) selects the module base address. Only bus address bits 6 through 13 are switchable, as the V680 always resides in the high 4K of the short VME addressing space, in conformance with VXI module rules. Set the switch sections to the indicated '1' or '0' positions as desired. All sections '0' is address C000 hex.
- **IRQ LEVEL** The IRQ LVL DIPswitch (S3) has three sections labeled '1', '2', and '4'. If all three are set to their '0' positions, the module will not interrupt. In any other positions, the combined setting determines the IRQ priority level. Note that the actual vector is set in the IRQ VECTOR register.
- **TRIGGER LEVELS** One DIPswitch (S4) is provided to set the trigger level for the nine channel inputs, and another switch sets the level for the GATE input. The CH0:8 switch sets channel input thresholds; it is labeled TTL/VT/NIM/ECL to select TTL, user-settable, NIM, and ECL threshold levels. Set only one switch section to the ON position. The TTL level is +1.25 volts; NIM is -0.4 volts; and ECL is -1.25 volts. If 'VT' is selected, the VT trimpot sets trigger levels from -2.5 to +2.5 volts, measurable at the VT test point. Similarly, the GATE switch sets the GATE threshold, using the VG pot and test point.
- **CLOCK** A slide switch (S1) is provided to select the clock source. In the INT position, the internal crystal clock is used, and the front-panel CLOCK connector is an output. In internal mode, the CLOCK TRIM pot fine-tunes the on-board ovenized oscillator. If the switch is set to EXT, the front-panel CLOCK connector is an input, and the internal oscillator will lock to an external 10MHz ±10PPM source.
- **TERMINATIONS** There are 10 termination switches, all located on the solder side of the board near the input connectors. They are labeled T0 T1 T2 T3 T4 T5 T6 T7 T8 and GT, and are associated with the nine input channels and the GATE input. If a switch is rotated clockwise to the 'HI' position, its input is unterminated; if it is rotated CCW to the '50' position, the input will be terminated in 50 ohms to ground.

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- **POLARITIES** Ten switches are associated with the nine input channels and the GATE input. The channel switches are labeled P0 through P8. When any of these is rotated CCW, the corresponding channel triggers on the positive edge of an input pulse; conversely, CW rotation selects the negative (falling) edge for time measurements. The GP switch selects the GATE polarity. If GP is set CCW to the '+' position, then a high input at the GATE connector will enable time hits. If the GATE function is not used, set the gate threshold to ECL, set GP to '+', and set the gate terminator GT switch to its 50-ohm position. Alternately, software may use the FORCE GATE option to ignore the gate input.

7.3 Adjustments

A CLOCK TRIM trimmer is provided to set the crystal clock frequency. To trim the clock, allow the V680 to warm up for at least 30 minutes, then use a precision counter to measure the frequency at the front-panel CLOCK connector; adjust the TRIM pot for a clock frequency of 10MHz ±Hz. The oscillator will age most when the unit is new, so should be checked after 6 months and then annually to maintain 1PPM accuracy.

Trimpots are provided to adjust time interpolator calibration. These are factory-set and sealed, and should not be field adjusted. Misadjustment of these pots will cause channel-to-channel time skew and excess jitter.

7.4 Installation in a VME Crate

After setting module switch options, install in any standard 6U VME crate. Be careful not to damage components when inserting or removing the module. If the module is to be used in its interrupt mode, remove any backplane IRQ jumpers at its slot. The module provides on-board bus grant jumpering, so backplane BG jumpers may be removed or left in place.

Never insert or remove the module with power on, and always secure the front-panel tiedown screws before powering up. Ensure that the slot used has at least 200 LFPM air-flow over the board surface.

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8. Test Software

A test/display program, V680.EXE, is available. It is a DOS application and requires a memory-mapped PC-to-VME interface in order to access the VME module; Bit3, Xycom, and VMIC interfaces are supported.

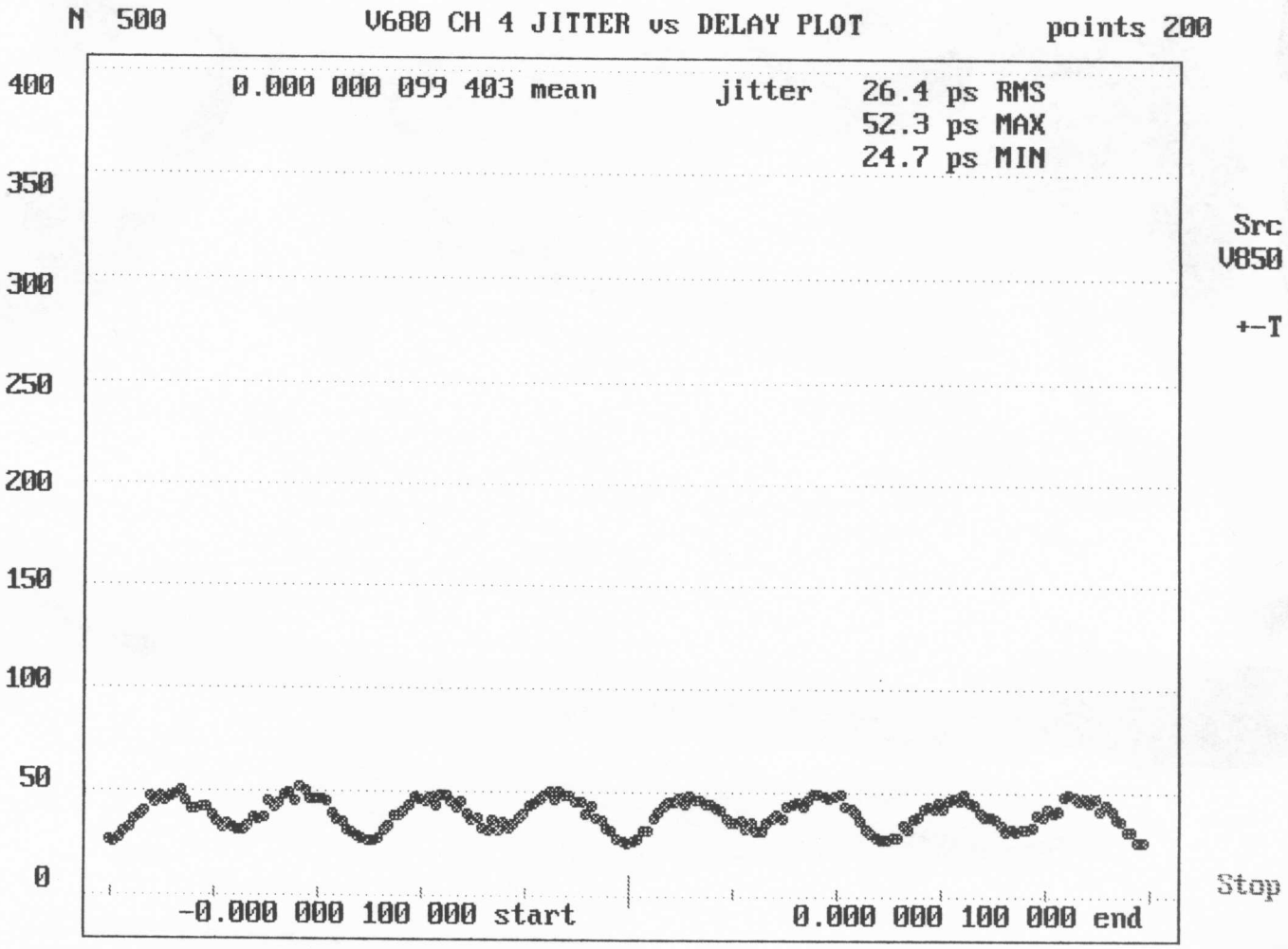
The program can test the module, make time measurements, make time histograms, and measure jitter. The source program, coded in PowerBasic, is also available.

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9. Typical Performance

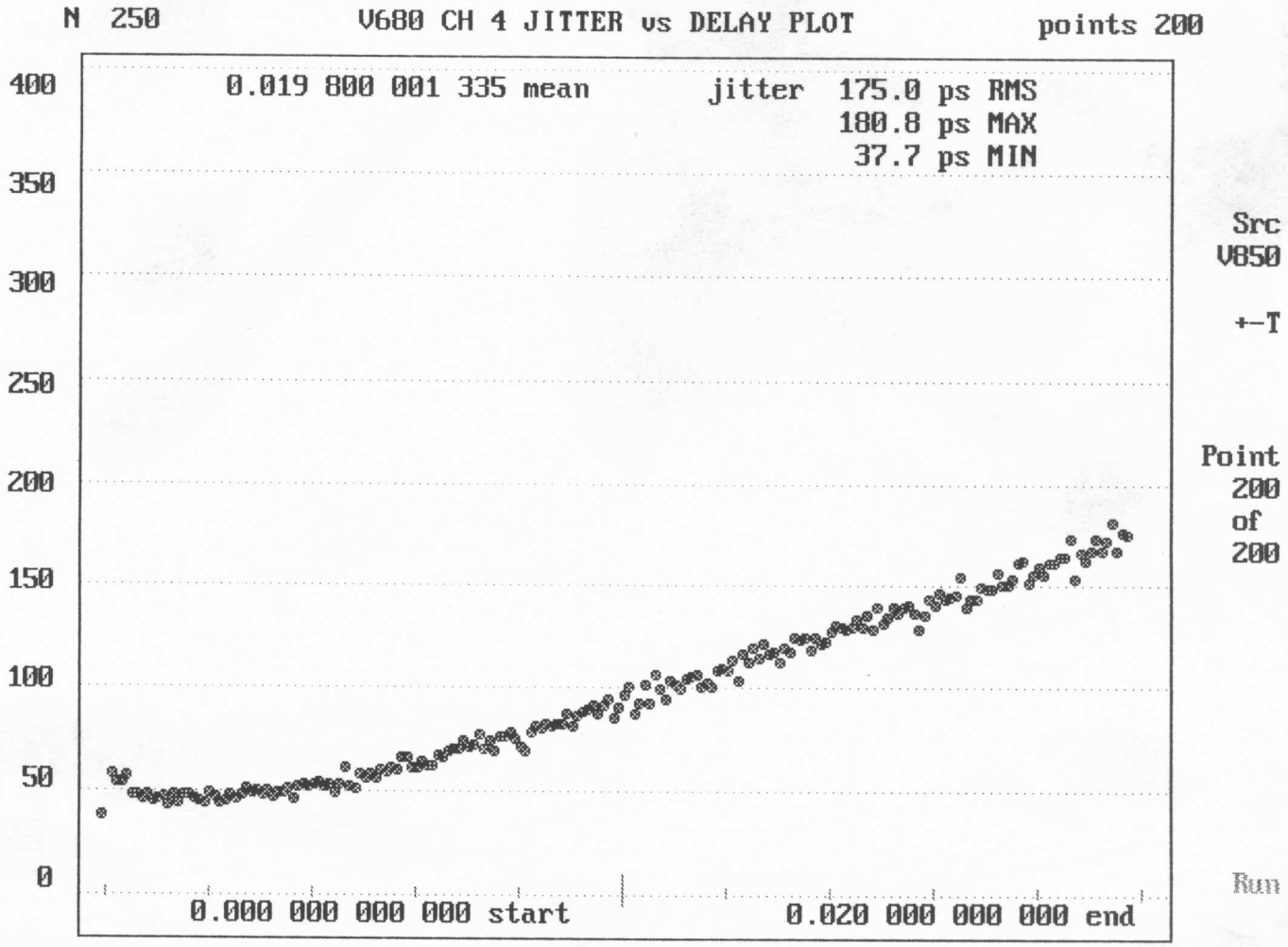
The following graphs illustrate the performance of a typical, factory-calibrated V680 module. The module was used with a Model V850 VME digital delay generator, so the indicated jitter includes contributions from both units.

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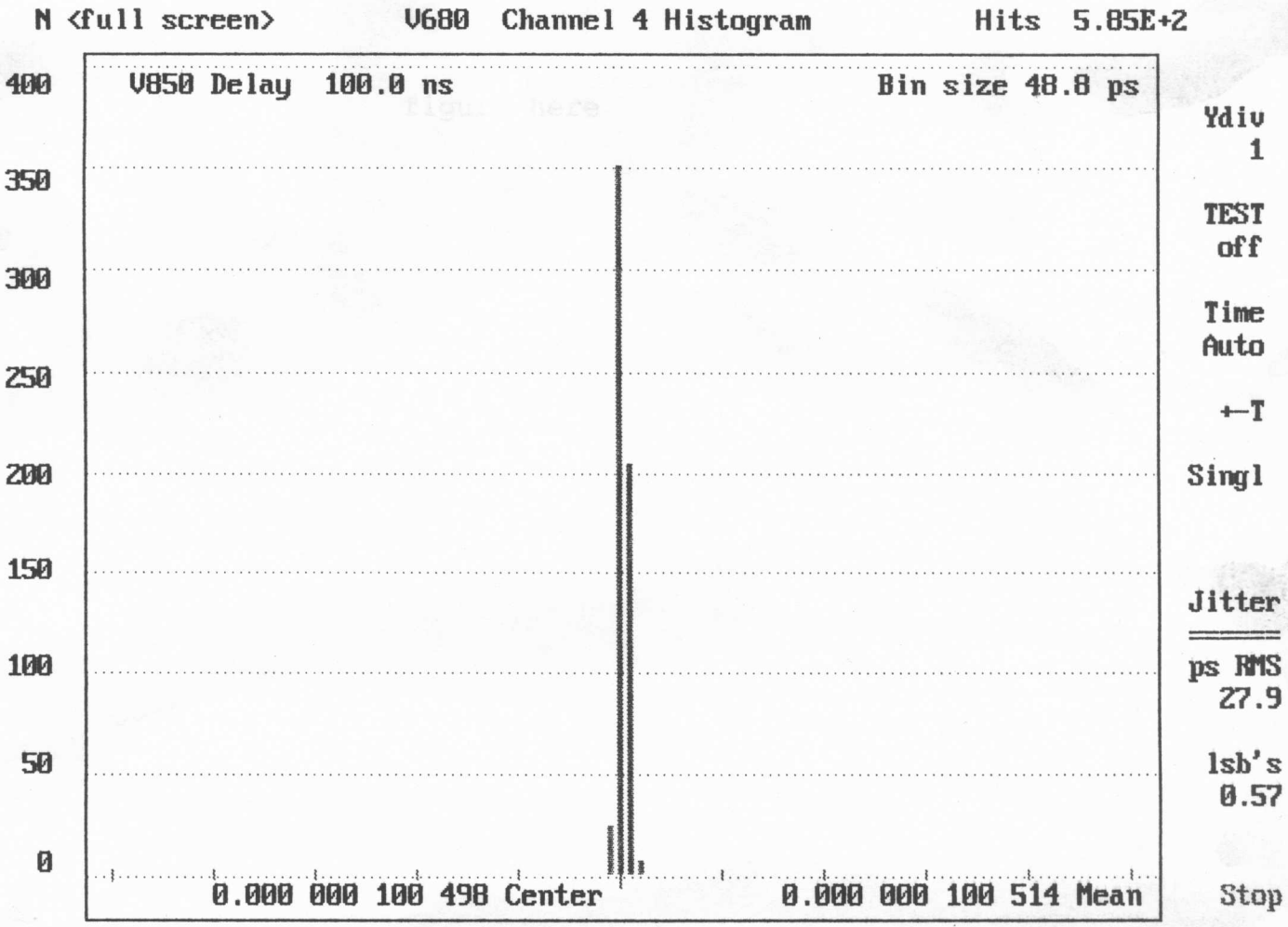
Graph of RMS jitter in picoseconds as a function of measured time, with delay ranging from -100 to +100 ns. This pattern is typical of short delays. For delays in the millisecond range, clock oscillator phase noise (in both the V680 and in the V850 test source) will increase jitter.

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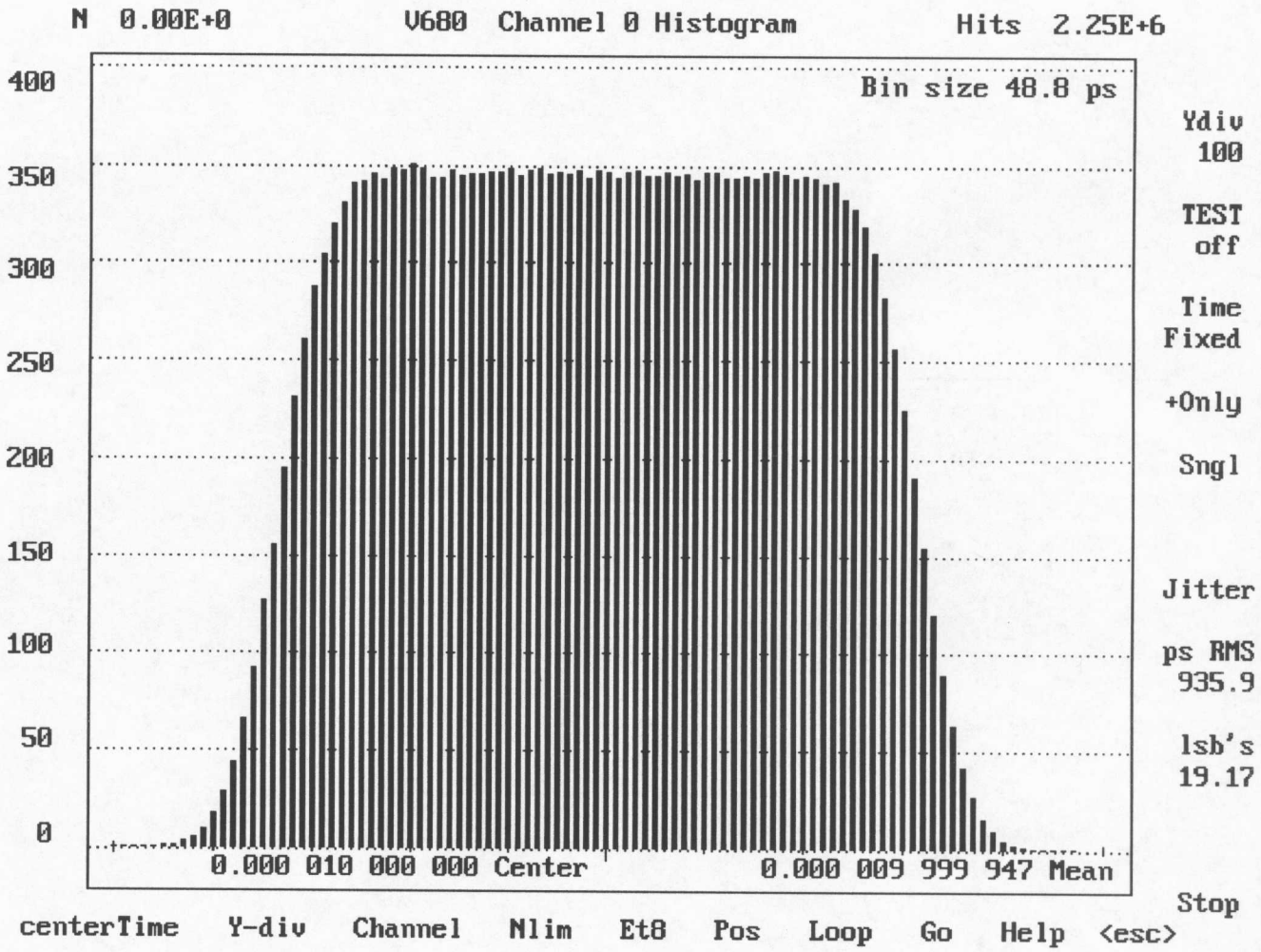
Graph of RMS jitter in picoseconds as a function of measured time, with delay ranging from 0 to +20 ms. The jitter increase starting at about 5 ms is caused by the phase noise of the V680 and V850 (test source) crystal oscillators.

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Histogram of a group of time measurements. Histogram bin size is 1 LSB, 48.8 picoseconds.

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Histogram illustrating differential linearity. The V850 delay source was time-swept by an asynchronous triangle wave, producing a nearly-flat time-density profile. Bin size is 1 LSB, 48.8 ps. Bin-to-bin height variations are essentially statistics-limited.

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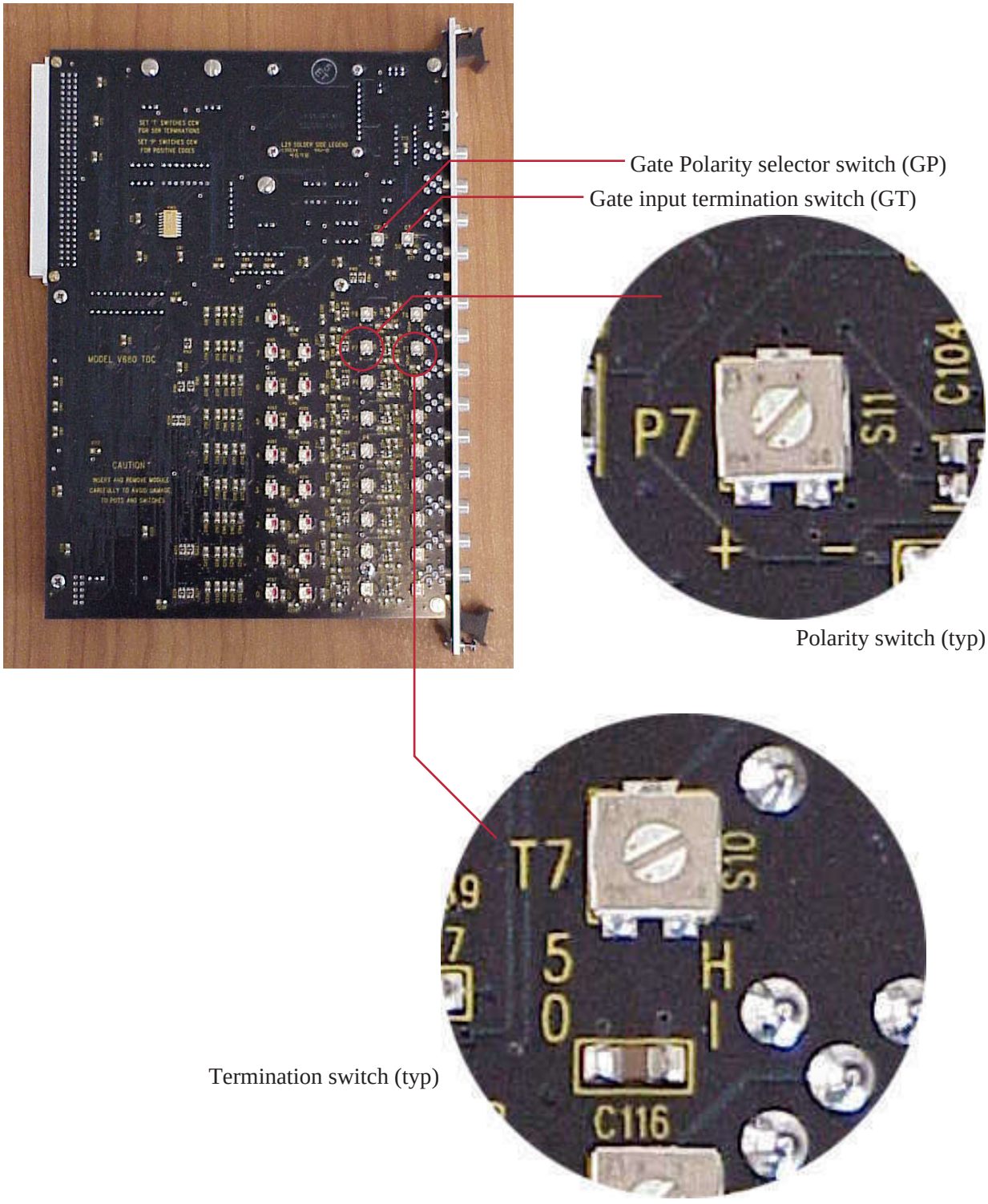


Fig. 2 Termination switches (T0- T8, GT) and polarity switches (P0 - P8, GP) are located on the solder side of the V680 Module

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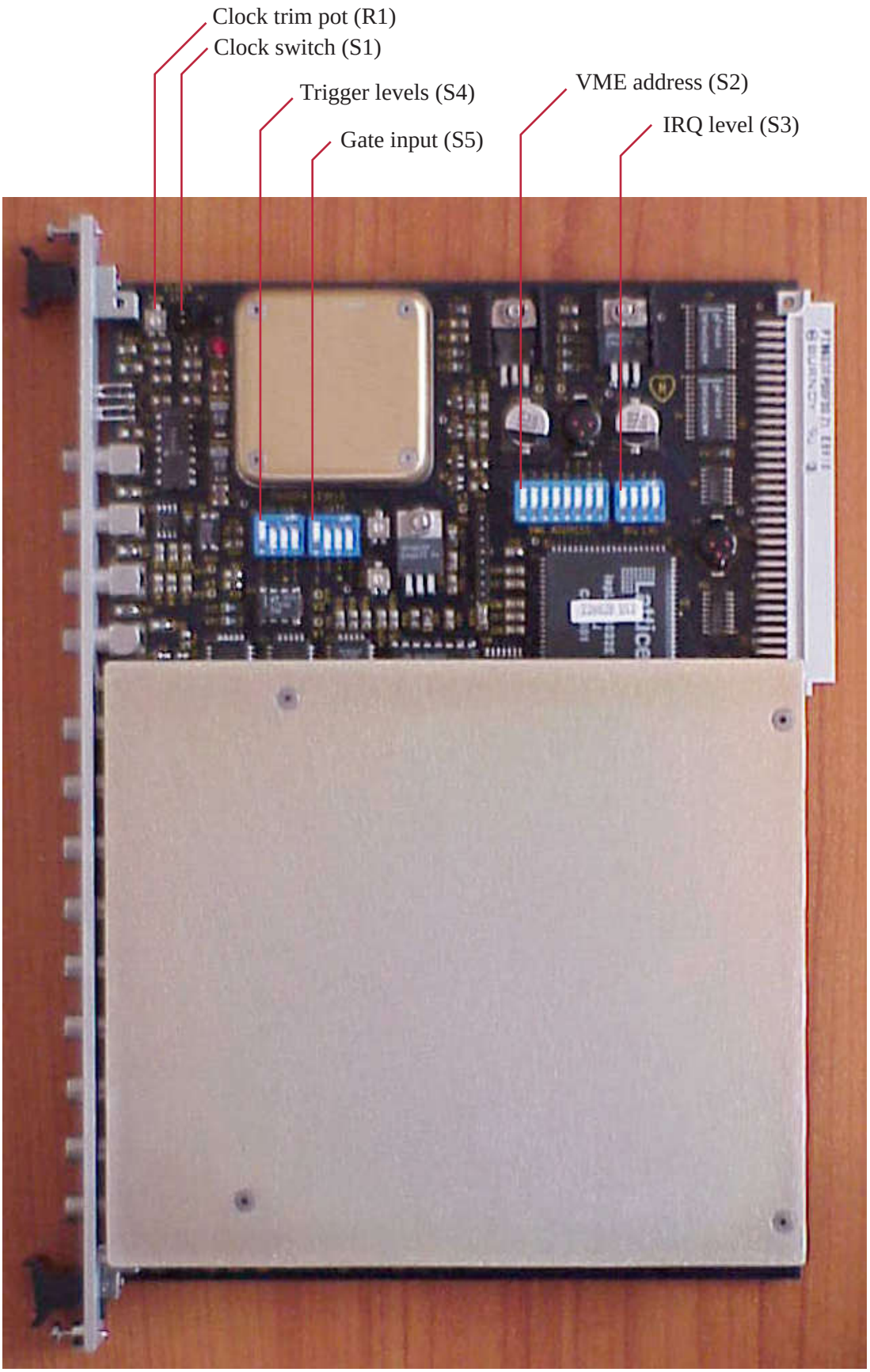


Figure 1: Set on-board switches (component side of board) to configure the V680 before installation

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