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HIGHLAND TECHNOLOGY

MODELS V850 AND V851
VME DIGITAL DELAY GENERATOR
TECHNICAL MANUAL

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1. Introduction

The V850-series is a group of versatile VME-packaged digital delay generators. The V850 is a 4-channel DDG, and the V851 provides six channels. Each is available with various connectors, and the V851 may be ordered with NIM logic-level outputs in addition to the six programmable-level delay outputs.

A V850-series module mounts in a standard 6U-size VME card cage, and operates as a slave module to any VME bus master. The V850 is triggered by an external pulse or an internally-generated single or repetitive pulse train. After receipt of a trigger, the module generates a 'T0' reference pulse and delayed pulse outputs T1 through T4 (or T6 for the V851). The delay associated with the Tn outputs may be programmed via the VME bus to be zero to 167.77 milliseconds with 32-bit resolution (39.0625 picosecond least significant bit). Each of the time outputs may be programmed to generate a variety of waveforms, and all output high and low voltage levels may be programmed as a group.

Features of the V850-series include the following:

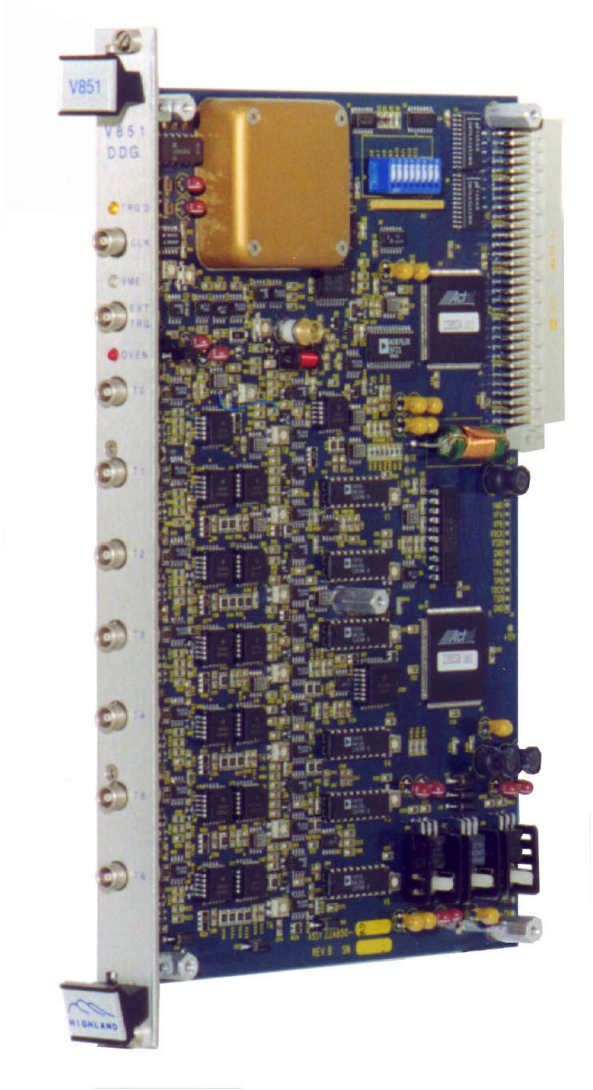
- Four or six delay channels in a 6U VME module.
- VXI compliant as a size "B" module.
- Resolution of 39.0625 picoseconds, range of 167.7 milliseconds.
- Typical accuracy better than 250 picoseconds absolute.
- Typical delay jitter below 30 ps RMS, external-trigger-to-output.
- Low, calibrated 25-nanosecond insertion delay; rep-rates to 2.5 MHz.
- All channel timings may be updated coherently, on-the-fly, without timing errors; smooth delay 'sweeps' are possible.
- Ovenized crystal oscillator timebase with phaselock provisions.

Standard versions of the V850-series include the following:

V850-1	Four channels, SMB connectors.
V850-2	Four channels, LEMO connectors.
V850-3	Four channels, LEMO connectors, auxiliary NIM outputs.
V851-1	Six channels, SMB connectors.
V851-2	Six channels, LEMO connectors.
V851-3	Six channels, LEMO connectors, auxiliary NIM outputs.
V851-4	Six channels, LEMO connectors, 15-ohm outputs.
V851-5	Six channels, LEMO connectors, Mode 6 disabled.

This manual applies to Revisions 'A' and 'B' of these products.

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FEATURES

- 6-channel digital delay generator in a 6U, register-based VME module.
- Delay and width modes.
- 40 (39.0625) picosecond LSB resolution with 32-bit (167.8 ms) full-scale delay range.
- Jitter typically less than 25 ps RMS.
- Adjustable trigger threshold and output levels.
- Insertion delay of 25 ns.

The Model V851 is a single-width, 6U VME module. It accepts a single trigger input and generates six separately programmable delay outputs. The six channels of delay may be combined in sequences to create three delay-and-width outputs. The module features a 32-bit dynamic range, 40-ps resolution, low jitter, and high rep-rate capability.

All channels are triggered simultaneously, and the module generates a "T0" edge 25 ns after the trigger, and six following delays (1 through 6) each programmable from 0 to 167.8 ms.

The outputs can also be configured to generate widths. This uses two channels, 1 and 2, to generate a pulse whose incidence is determined by Channel 1's timing value and whose termination is determined by Channel 2's timing value. Similarly, Channels 3 and 4, as well as 5 and 6, can be combined to operate in the width mode.

The V851 delay parameters may be programmed on-the-fly at VME-bus speeds without any generation of erroneous delays. All six delay channels can be updated coherently.

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CONFORMANCE	Complies with ANSI/IEEE 1014-1987 VMEbus specification. Meets the VXIC specification, Revision 1.4.
DEVICE TYPE	Register based slave: A16:D16:D08(EO) capability.
POWER REQUIRED	+5: 3.0A max; +12: 1.5A max at startup, 825mA max after warm-up; -12: 1.1A max at startup, 550mA after warm-up.
PACKAGING	Single-width, 6U VME, B-size VXI module.
TIMING CHANNELS	Six timing channels (1 through 6). In DELAY mode, the V851 produces six independent delays. In WIDTH mode, channels 1 and 2 (as well as 3 and 4, 5 and 6) allow the generation of pulses with programmable delay and duration.
TRIGGERING	Triggers can be selected from front panel EXT TRG, internal source, or VMEbus command trigger.
REP RATE	Up to 2.5 MHz.
INSERTION DELAY	25 ns.
RESOLUTION	39.0625 ps LSB (equivalent to a clock rate of 25.6 GHz).
RANGE	32 bits allows a full scale range of 167.7722 ms on all channels.
JITTER	Less than (50 ps + 1E-9 x programmed delay) RMS.
ACCURACY	± (500 ps + timebase stability).
TIMEBASE	Ovenized oscillator. Temperature coefficient <10 ppB/° C; aging below 1ppM/year. Oscillator may be phase locked to a 10 MHz external reference via the front panel CLOCK I/O connector.
INPUTS	EXT TRG: Adjustable threshold level ±2.5V, slope, and termination (Hi-Z, 50 ohms to ground).
OUTPUTS	One fixed position marker (T_0) and six delay (1, 2, 3, 4, 5 and 6) outputs. In the DELAY mode, a given timing channel is routed to the similarly numbered output. In the WIDTH mode, the width waveform generated timing channels 1 and 2, are routed to output 2, with 3 and 4 routed to output 4, and, for the V851, 5 and 6 routed to 6. All outputs are commonly adjustable for a baseline of 0 to -2.5 volts and amplitude of 0 to +5 volts. The slew rates are better than 2V/ns.
CONNECTORS	Standard: SMB. Options: LEMO or LEMO with independent NIM outputs.

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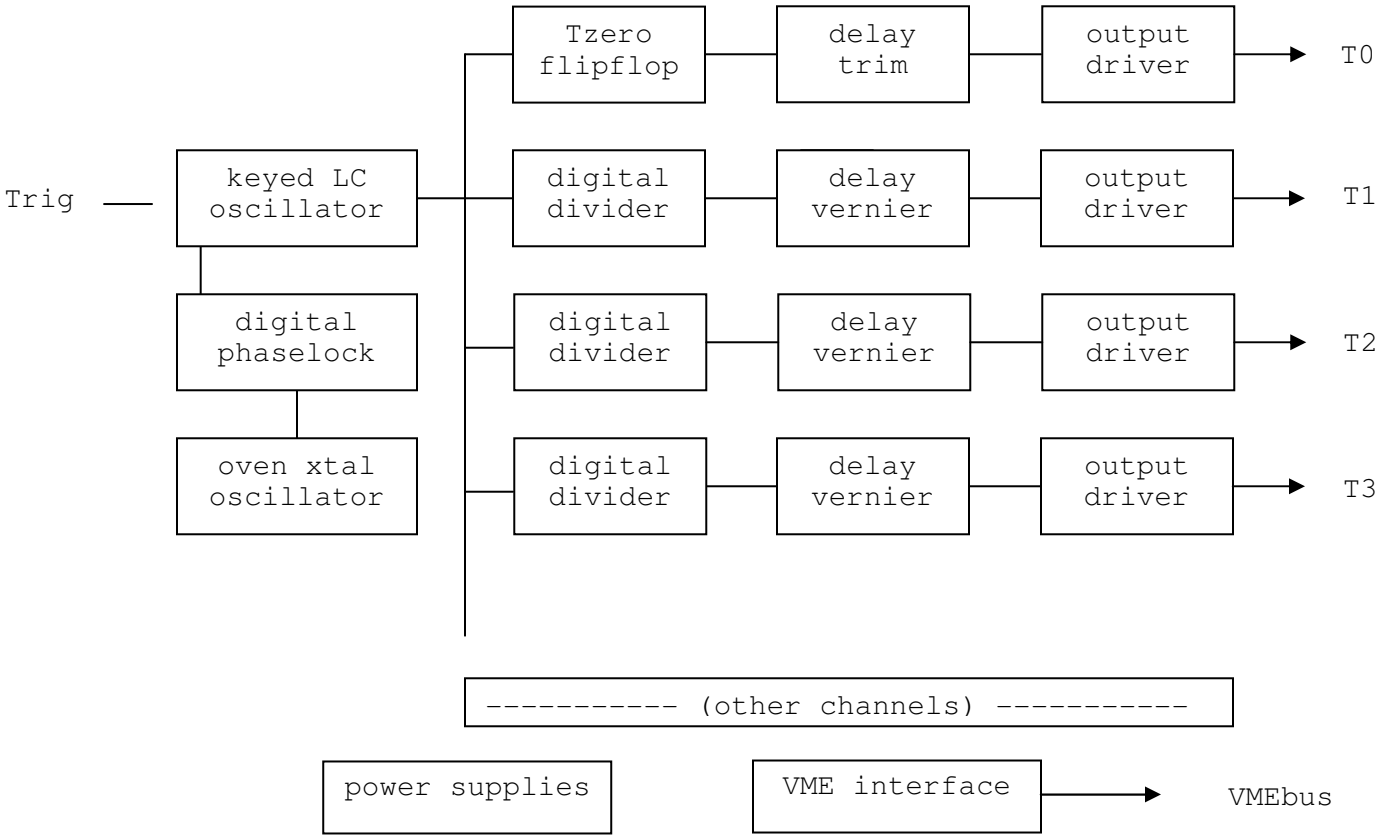
3. Theory of Operation

3.1 Block Diagram

A simplified block diagram of the V850-series DDGs is shown in Figure 1. When a trigger is detected - from an internal or external source – a precision 50 MHz LC oscillator is keyed; this oscillator drives individual channel digital downcounters to count off precise delays. Time vernier circuits add small additional delays to interpolate between the counts of the digital dividers. A DSP-based phaselock circuit forces the LC oscillator to have the same long-term precision as that of the internal ovenized crystal timebase.

The module provides a 'T0' output which occurs 25 nanoseconds after trigger, and four (or six) 'Tn' outputs, one associated with each delay channel. The Tn timing values are measured relative to the T0 edge.

Figure 1



The module may be triggered from an external (user-supplied) signal, from an internal programmable reprate generator, or via VME command.

Per-channel delays are determined by loading 32-bit delay value registers from the VME bus. Resolution is 39.0625 picoseconds per LSB, with a maximum delay range of 167.772 milliseconds. The precision crystal oscillator timebase may be phase-locked to another V850-series module or to an external 10 MHz clock.

The output stages are programmable (as a group) to output high levels of 0 to +5 volts and low levels of 0 to -2 volts behind 50 ohms. The external trigger level is programmable from -2.5 to +2.5 volts.

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3.2 Output Waveform Logic

Each output stage may be programmed to generate one of a number of waveforms. Channels may be used individually, combined with the T0 signal, or paired with a neighboring channel to create delay/width combinations. A set of new delay values can be loaded into a V850 and simultaneously 'installed', guaranteeing that all new delays are effective simultaneously. For example, pulse delays and widths may be swept smoothly, or pulses programmed arbitrarily, without error.

Possible channel waveforms are listed and illustrated below. 'T0' represents the module reference time, 'Tn' is the programmed 'channel n' time delay, and 'EOD' is the cycle end-of-delay time; EOD is declared when all channels have timed out, or when the module is force-reset.

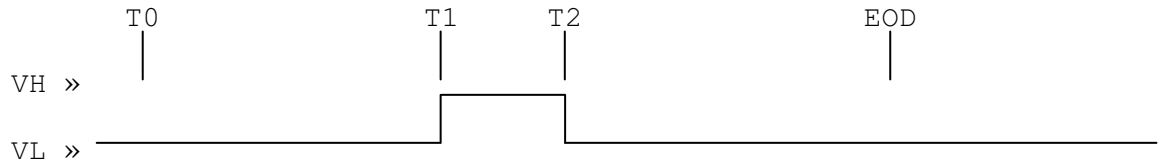
```
MODE 0: DELAY +  Positive edge at programmed delay time. Level is
                 maintained until End-Of-Delay (EOD).
```



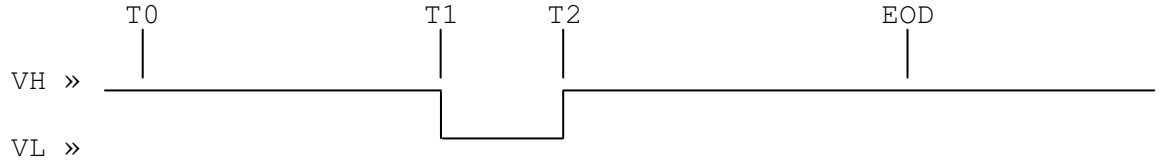

```
MODE 1: DELAY -  Negative edge at programmed delay time. Level is
                 maintained until EOD.
```




```
MODE 2: WIDTH +  Two channels are paired (1/2, 3/4, or 5/6). The output
                 goes high when the ODD channel delay is reached, and
                 returns low when the EVEN channel times out. For
                 Channels 1 and 2, this signal is   OUT = (T1 * !T2).
```

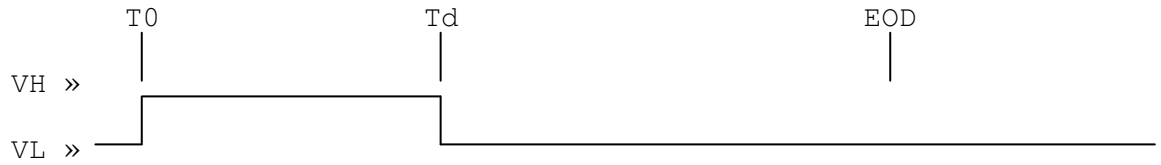



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MODE 3: WIDTH -  Same as mode 2, but output polarity is inverted.
```



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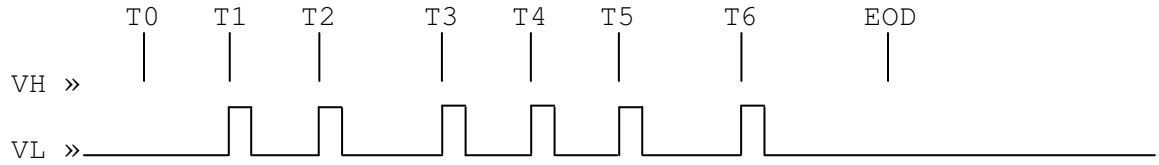
MODE 4: T0/delay + Output goes high at trigger time, and returns low when channel times out.



MODE 5: T0/delay – Same as mode 4, but output polarity is inverted.

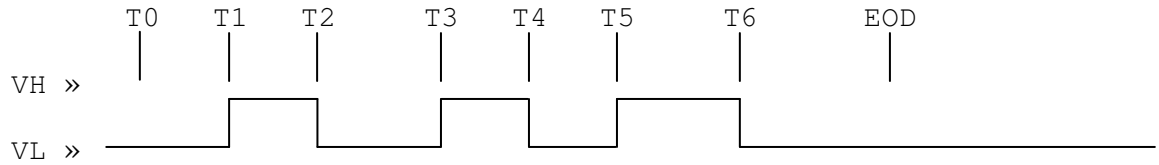


MODE 6: OR-ALL Logical OR of all timing channels (1...4 or 1...6); output is active high. Used primarily when all channels are in ONESHOT mode, as shown here:



Note: In the V851-5 optional version, Mode 6 OR-ALL is OFF.

MODE 7: OR-WIDTHS Logical OR of all widths, active high. Logically, this is OUT = (T1 * !T2) + (T3 * !T4) + (T5 * !T6).



3.3 About Width Modes

Note that when a pair of channels is combined to generate a delay/width output, the ODD channel sets the LEADING edge time and the EVEN channel sets the TRAILING edge time. Either channel (or indeed both channels) can be used in delay/width mode, and its paired delay channel can be used in any other mode. Do not set the ONESHOT attribute on either channel used in a delay/width pair.

For example, Channel 1 could be operated in any desired mode, with time set to 10 µsec, and Channel 2 could be programmed to operate in WIDTH+ mode, with time set to 12 µsec. Then Channel 1 would operate normally in its programmed mode, and Channel 2 would generate a positive pulse starting 10 µsec after the trigger, and lasting 2 µsec.

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3.4 Oneshot Mode

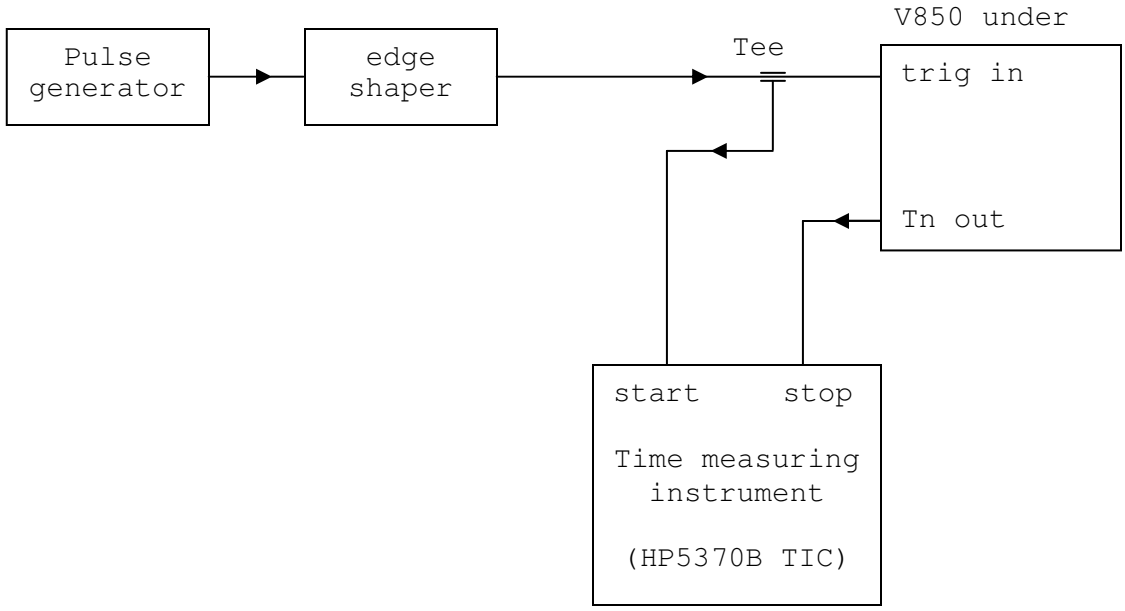
Any delay channel may be programmed to operate in Oneshot mode. In Oneshot mode, the channel output is a short pulse at the end of the programmed time interval. Oneshot pulse width can vary from 40 to 80 ns depending on the channel time setting. The leading edge of the Oneshot pulse will always occur at the programmed time.

Do not enable Oneshot mode on either channel used in a Delay/Width pair.

3.5 Measurement Reference Conditions

Note that the V850 module is tested, and accuracy specified, using the following reference setup:

Figure 2



The V850 is externally triggered at 1 KHz, using a fast edge-rate generator or a TTL-speed generator and a V858-1 edge shaper. The trigger pulse should be -2 to +2 volts behind 50 ohms, with a risetime of 100 ps nominal.

The trigger pulse is connected to a short Tee junction at the V850 front panel, and the trigger signal is continued to the time measuring device. The DDG output to be measured is routed to the other time measuring device input. The recommended time measuring instrument is the HP Model 5370B time-interval counter (TIC). High-quality 50-ohm matched-length coaxial cables should be used between the V850 and the TIC. TIC inputs should be set for 50 ohms, zero threshold, and positive slope.

The V850 under test should be programmed for the following:

TRIGGER	External, +slope, 0 V threshold, high-z.
OUTPUTS	-2 to +2 volts.
CLOCK	Internal.
CHANNEL MODES	Positive delay (waveform mode 0).

Note: When measuring jitter, the jitter reported by the TIC instrument is the trigonometric sum of the DDG jitter and the inherent jitter of the TIC itself. The V850 jitter is similar to that of the HP5370B.

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4. Application

4.1 VME Rack Installation

A V850-series module may be installed in any VME (ANSI/IEEE standard 1014) VME card cage. The module requires only the standard +5, +12, and -12 volt DC power and engages only the upper (P1) VMEbus connector. The V850 does not use interrupts or bus request lines and passes all grant lines.

Before installing the unit, set its desired bus address, as described in Section 5.2.

The front-panel holddown screws should be securely engaged before powering up the VME crate. Note that the V850 front panel will be grounded to the VME frame by these screws, and the VME frame must be connected to a secure earth ground to ensure safety and minimize EMI. Note that the V850 front panel is NOT connected to VME common within the module.

The V850 requires a minimum of 200 LFPM forced-air flow over the surface of the printed-circuit card. The DDG is equipped with a shielding plate, and it may not operate properly with the plate removed.



CAUTION: The VME cardcage must be properly grounded. Always turn off VME crate power before inserting or removing any VME modules. Damage to the module or to other modules in the crate may result from installing or removing modules with power on. The small-geometry high-speed semiconductors used in the V850 are sensitive to static discharge damage. Ground all cables and discharge inner conductors before connecting to the DDG connectors.

4.2 Trigger Input

If external triggering is required, connect the trigger source to the TRIGGER connector using a shielded, 50-ohm coaxial cable. The trigger source should have a maximum signal level of ±5 volts peak to avoid damage to the DDG. An internal slide switch is provided to select whether the V850 provides a high impedance to the trigger source or terminates it in 50 ohms.

For safety reasons, the trigger source should be grounded to VME common, which itself is generally tied to earth ground.

For minimum jitter, the trigger should have a high amplitude, high slew rate, and minimum noise. Note that both high-frequency noise (arcs, SCR impulses, nearby RF equipment) and low-frequency noise (unstable source amplitudes, 60-Hz ground loops) can dither the trigger threshold and induce jitter. For testing purposes, a step-recovery-diode edge shaper (such as the Model V858) can be used to enhance the edge of a standard pulse generator into the 20 V/nsec range.

4.3 Clock In/Out

The V850-series modules include low-drift, low phase-noise, ovenized crystal oscillators as their internal timebases. When used in internal clock mode, the front-panel CLOCK connector provides a TTL-level, 10 MHz output. This output may be used to verify the accuracy of the internal oscillator, or it may serve as the timebase for other equipment, including other V850's, or series 600 time-to-digital converters.

When a DDG is programmed to use an external clock, the CLOCK connector becomes an input. An external 10 MHz source can be applied to the DDG, and the V850 will phase-lock its internal oscillator to that source. The external clock must be 10 MHz ±1 PPM (±10 Hz) and must be TTL level.

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4.4 T0 Output

A reference time output T0 is provided on the module front panel. The T0 output goes high 25 nsec after a trigger is recognized and remains high until EOD time; see Section 5.4.3 for EOD details. This T0 delay is the 'module insertion delay' and is factory adjusted to be 25 ± 0.25 nsec.

T0 is the time reference for all channel (T1...T6) time outputs. If a channel is programmed to have a 10 ns delay, its output will transition 10 ns after the T0 rising edge.

The electrical high/low levels of the T0 output (and of the Tn channel outputs) are programmable, as described in Sections 5.3.4 and 5.3.5.

4.5 Channel Outputs

Four-channel (or six-channel) output connectors are provided, named T1...T6. Each has a programmable waveform, as described in Section 3.2, and programmable high/low voltage levels common with the T0 levels. Each output has a 50-ohm source impedance and edge rates of about 2.5 volts/ns.

4.6 Optional NIM Outputs

Modules may be furnished with optional NIM-level outputs. Such modules have four or six additional output connectors, and provide NIM outputs which go true (electrically, -18 mA) when the corresponding channel outputs go true. On an oscilloscope, the NIM outputs will look like inverted versions of the waveforms shown in Section 3.2. NIM signals typically occur 700 picoseconds before the main outputs, as measured under reference conditions.

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5. Programming

5.1 General

The V850-series modules are register-based VME slave devices capable of performing 8 or 16-bit data transactions, formally 'A16:D16:D08(EO)'.

In general, the sequence of programming is as follows:

1. Set the on-board DIPswitch to select the module base address.
2. Install and power up the module.
3. Read the VXI MFR and VXITYPE registers to verify module presence.
4. Write the desired control register pattern; set DISARM if required to avoid generating output pulses during setup.
5. Write the VOUT HI and VOUT LO output-level registers.
6. Write the TRG LVL trigger level register (for external triggers) or the INTRATE register for inter periodic triggers.
7. Write the three WAVE registers to select desired waveforms.
8. Write the DLY registers to load channel time delays.
9. Write the XFR bit in the ACTIONS register to 'install' the delays.
10. Rewrite CONTROL with DISARM low if required to enable triggers.

5.2 VME Address Selection

A DIPswitch is provided on the DDG module for selection of the VME bus module base address; bits are clearly labeled on the switch. The switch is accessible without removing the module cover. *Note*: In accordance with VXI standards, the module occupies 32 words (64 bytes) in the high 4K of the 16-bit addressing space, namely the address range C000 - FFC0. Modules should not be switched to have base address FFC0 (all switches set to '1') as that might interfere with automatic module address assignment in certain VXI systems.

The V850 responds to hex address modifier codes 29 and 2D.

V850 modules are normally shipped with all address switches set to '0', establishing a base address of C000 hex.

5.3 VME Register Map

The following is a summary of the VME-accessible registers implemented by the V850-series modules. All registers are 16 bits wide. REG # is the ordinal register number in decimal; OFFSET is the VMEbus address offset from the module base address, shown in hex. The R/W column indicates whether the register is Read-only or Write-only from the VMEbus.

Reg Name	Reg#	Offset	R/W	Function
VXI MFR	0	00	R	VXI manufacturer ID; always 65262, FEEE hex.
VXITYPE	1	02	R	Module type, always 22851, 5943 hex.
VXI STS	2	04	R	VXI status register.
----	3	06	-	Unused.

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Reg Name	Reg#	Offset	R/W	Function
VOUT LO	4	08	W	Channel and T0 low voltage level.
VOUT HI	5	0A	W	Channel and T0 high voltage level.
ACTIONS	6	0C	W	Module action command bits.
TRG LVL	7	0E	W	External trigger level set.
CONTROL	8	10	W	Module control bits.
INTRATE	9	12	W	Internal trigger reprate divisor.
----	10	14	-	Unused.
----	11	16	-	Unused.
----	12	18	-	Unused.
----	13	1A	-	Unused.
----	14	1C	-	Unused.
----	15	1E	-	Unused.
DLY1 HI	16	20	W	Delay 1 MS 16 bits.
DLY1 LO	17	22	W	Delay 1 LS 16 bits.
DLY2 HI	18	24	W	Delay 2 MS 16 bits.
DLY2 LO	19	26	W	Delay 2 LS 16 bits.
DLY3 HI	20	28	W	Delay 3 MS 16 bits.
DLY3 LO	21	2A	W	Delay 3 LS 16 bits.
DLY4 HI	22	2C	W	Delay 4 MS 16 bits.
DLY4 LO	23	2E	W	Delay 4 LS 16 bits.
DLY5 HI	24	30	W	Delay 5 MS 16 bits **see caution note.
DLY5 LO	25	32	W	Delay 5 LS 16 bits **in Section 5.3.10.
DLY6 HI	26	34	W	Delay 6 MS 16 bits ** ".
DLY6 LO	27	36	W	Delay 6 LS 16 bits ** ".
WAVE 12	28	38	W	Waveform programming, Channels 1/2.
WAVE 34	29	3A	W	Waveform programming, Channels 3/4.
WAVE 56	30	3C	W	Waveform programming, Channels 5/6. **
----	31	3E	-	Unused.

Within each register, bits are numbered 0 (LSB) through 15 (MSB). Detailed descriptions appear in the following sections:

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5.3.1 VXI MFR Register: VXI Manufacturer's ID

This register displays the VXI-registered manufacturer's ID code. It always reads as FEEE hex.

5.3.2 VXITYPE Register: Module Type

This register displays the module type. It always reads as 22851 decimal, 5943 hex.

5.3.3 VXI STS Register: Status Register

This register contains two active readable bits. Bit 8 reads high if a timing cycle is in progress, and bit 9 reads high during the EOD interval. All other bits read high, except the MSB (bit 15) which is always low.

5.3.4 VOUT LO Register: Output Low Voltage Level

This register sets the low level output voltage for the T0...T6 outputs. The MS byte of this register (bits 15...8) controls the 8-bit low-level DAC. Byte value 0 sets the output level to 0 volts, and byte value 255 (FFh) sets the low level to -2.0 volts.

If 'R' is considered to be the unsigned 16-bit integer value in this register, then for VLOW in volts:

```
R  =  (- VLOW) * 32640
```

5.3.5 VOUT HI Register: Output High Voltage Level

This register sets the high level output voltage for the T0...T6 outputs. The MS byte of this register (bits 8...15) controls the 8-bit high-level DAC. Byte value 0 sets the output level to 0 volts, and byte value 255 (FFh) sets the high level to +5 volts.

If 'R' is considered to be the unsigned 16-bit integer value in this register, then for VHIGH in volts:

```
R  =  VHIGH * 13056
```

5.3.6 ACTIONS Register: Module Immediate Actions

Writing active-high bits into this register will trigger immediate module actions. Bits are as follows:

Bit	Name	Function When Written To '1'
0	FEOD	Forces end-of-delay; terminates any timing cycle in progress; if set with XFR, jam-loads timing registers.
2	CAL	Initiates a phase-locked-loop recalibration.
7	XFR	Causes newly-written timing values to be queued for loading into timing registers at the next EOD.
15	FIRE	Triggers the DDG if module is in VME trigger mode.

5.3.7 TRG LVL Register: External Trigger Level

The MS byte of this register (bits 15...8) sets the trigger level voltage for external trigger inputs. Hex codes 0000 through FF00 correspond to trigger levels +2.5 and -2.5 volts respectively, and code 8000 hex corresponds to zero level.

If the value in this register is considered to be unsigned 16-bit integer 'R', then, for trigger level 'TL' in volts:

```
R  =  (2.5 - TL) * 13107
```

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5.3.8 CONTROL Register: DDG Control

Bits in this register establish module operating modes as follows:

Bit	Name	Function
8	SLOPE	Selects external trigger slope; '1' = negative edge.
9	VTRIG	When set, module is triggerable by the FIRE action bit.
10	ITRIG	When set, internal rate generator triggers the DDG. (If VTRIG and ITRIG are both low, external triggers are enabled.)
11	PRESCL	When set, prescales the internal rate generator by 100.
12	LDNOW	When set, writes to the INTRATE register will immediately load the internal rate divisor. When this bit is clear, data written to INTRATE will be loaded into the divisor when the next internal trigger occurs.
13	CCAL	When set, forces the module into CAL mode; this function is intended for maintenance only.
14	EXTB	When clear, the front-panel CLOCK connector is a 10 MHz output; when set, CLOCK is an input, and the module will phase-lock to an external 10 MHz source.
15	DISARM	When set, the DDG will not trigger.

5.3.9 INTRATE Register: Internal Trigger Reprate Divisor

When the module is used in internal trigger mode, the level of the PRESCL bit and the value written to the INTRATE register together determine the trigger rate. If PRESCL is low, the internal trigger rate is as follows:

```
RATE = 5 MHz / INTRATE
```

and, if PRESCL is true:

```
RATE = 50 KHz / INTRATE.
```

Note: The V850 should not be triggered at a rate above 2.5 MHz.

5.3.10 DLYn HI and DLYn LO: Delay Registers

Each DDG channel has a pair of 16-bit registers, which determine the channel delay time. Delay is considered to be a 32-bit unsigned integer with LSB weight of 39.0625 picoseconds. The 32-bit value is written to the module as two 16-bit values, with the DLY HI registers being the most significant 16 bits and the DLY LO registers being the 16 least significant bits.

Values loaded into the DLY registers are held in 'assembly' latches. When the XFR action bit is set, the assembly-register time values are transferred together into to an array of delay registers. The delay-register values are loaded into actual timing downcounters at the next EOD interval.



CAUTION: Although the V850 version DDG does not implement the T5 or T6 outputs, the DLY5 and DLY6 register sets remain present and functional on the internal Timer chip. These registers should be loaded with all 0's to avoid possible extension of timing cycles and delay of the EOD event.

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5.3.11 WAVE 12 Register: Waveform Select, Channels 1 and 2

Two nibbles of this register select the waveform modes for delay Channels 1 and 2. Bits are as follows:

bit	7	6	5	4	3	2	1	0
name	OS2	S2c	S2b	S2a	OS1	S1c	S1b	S1a

Bits 7...4 control Channel 2, and bits 3...0 control Channel 1. The OS bits, when set, put the corresponding channel into one-shot mode. Bits <c...a> select the channel waveform mode 0 through 7, as described in Section 3.2.

5.3.12 WAVE 34 Register: Waveform Select, Channels 3 and 4

Two nibbles of this register select the waveform modes for delay Channels 3 and 4. Bits are as follows:

bit	7	6	5	4	3	2	1	0
name	OS4	S4c	S4b	S4a	OS3	S3c	S3b	S3a

5.3.13 WAVE 56 Register: Waveform Select, Channels 5 and 6

Two nibbles of this register select the waveform modes for delay Channels 5 and 6 (V851 only). Bits are as follows:

bit	7	6	5	4	3	2	1	0
name	OS6	S6c	S6b	S6a	OS5	S5c	S5b	S5a

5.4 Realtime Considerations

5.4.1 Register Buffering

V850 registers may be categorized into two classes: buffered and unbuffered. Writes to unbuffered registers take effect immediately. These include the ACTIONS, VOUT HI, VOUT LO, TRIG LVL, CONTROL, and the three WAVESELECT registers. The INTRATE register may be used in buffered or unbuffered mode, under control of the LDNOW control bit. The DLY time-setting registers are usually used in their default double-buffered mode, but buffering can be overridden when required.

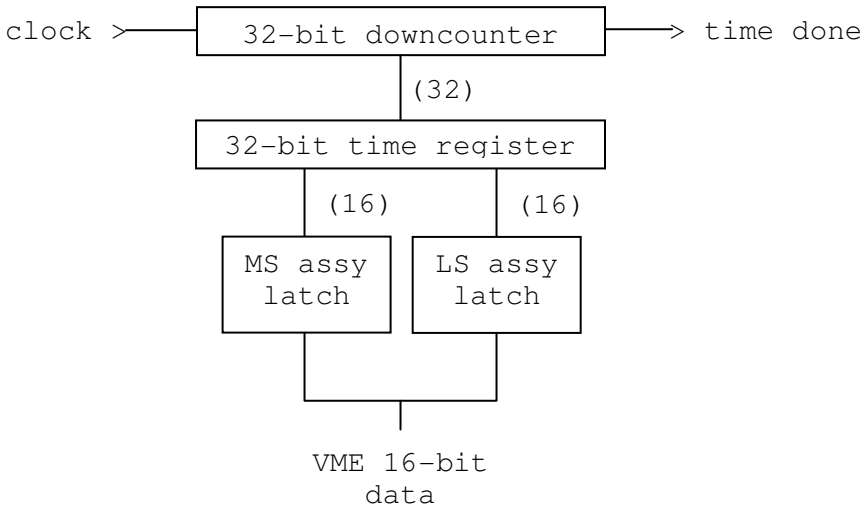
5.4.2 Time Update Modes

The V850 time-count data path is shown below. For each timing channel, two user-writable 16-bit 'assembly' registers are provided to accept the most-significant and least-significant halves of the 32-bit channel time delay value. The VME-accessible assembly registers may be written at any time and in any sequence without affecting module operation. Once a new set of times is loaded, asserting the XFR action bit will cause all assembly registers (of all channels) to be simultaneously transferred to the 32-bit time registers.

At the end of any DDG cycle (i.e., at EOD time), the contents of all the 32-bit time registers are loaded into the respective channel downcounters in preparation for the next trigger. When the module is subsequently triggered, the downcounters are used (along with their associated time verniers) to generate the desired delays. Anti-collision logic is active during the EOD interval to ensure that all counters are correctly loaded for any possible timing of the XFR event.

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Figure 3



The V850 is commonly used in two distinct environments:

1. The DDG is continuously triggered by a source, which is not observable to the controlling computer or occurs at a rate sufficiently high that the computer cannot synchronize its software to triggers.
2. The trigger events occur infrequently or are effectively single-shot experiments. The control software is aware that the DDG is not triggered and knows the desired timing values for the very next expected trigger event.

In case one (1), the controlling computer may, at any time, write a new set of time values to some or all of the DLY registers and, when done, set the XFR action bit. The new times will become effective at the END of the next timing cycle (or at the end of the current timing cycle if XFR is executed while timing is active).

In case two (2), it is generally undesirable to wait until the end of a timing cycle to install new time values, since the event to be timed may be expensive and occur only once. In this case, the user may load a new time-value set into the DLY registers, then assert both the FEOD and XFR action bits in a single write to the ACTION register. This will abort any timing sequence currently in progress, force the EOD logic to sequence, and immediately load all new times into both the time registers and the actual downcounters. The very next trigger will then use the new time delay set.

If aborting an in-progress timing cycle is undesirable, you can set the DISARM control bit, wait for the current timing cycle to finish, and then perform any desired reprogramming, including the XFR+FEOD operation.

5.4.3 EOD Logic

After the DDG is triggered and all four (or six) timing channels have completed their programmed delays, EOD is declared. The EOD interval lasts about 200 nanoseconds. During EOD, the input trigger recognizer is held reset, all outputs are returned to their 'off' states, and the timing downcounters and associated time verniers are reloaded from their 32-bit time buffer registers.

Setting the FEOD bit in the ACTION register forces EOD, terminating any ongoing timing cycle.

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5.4.4 Internal Rate Generator Notes

The function of the internal rate generator is described in Section 5.3.9. The rate generator is a downcounter; every time it counts down to zero, it creates a DDG trigger and is reloaded to the latched value written to the INTRATE register from the VME bus. If a new INTRATE value is loaded, the downcounter will continue to time out its current period until it reaches zero; it will then install the new time divisor value for the next cycle.

If the LDNOW bit is set in the CONTROL register, writes to the INTRATE register will immediately force-load the rate generator downcounter, beginning a new interval down-count regardless of the completion state of the previous cycle.

5.5 Self-Calibration

As described in Section 3.1, the V850 uses a precision, temperature-compensated LC oscillator to generate time delays, and the LC oscillator is phase-locked to a precision ovenized quartz crystal oscillator for long-term stability. At powerup time, and any time the DDG is triggered, the LC oscillator center frequency is retuned to align it with the crystal oscillator. An explicit recalibrate function is also available, invoked by setting the CAL bit in the ACTION register. If this bit is written as a '1', the module will execute an oscillator realignment sequence, taking about 300 microseconds to complete. Explicit recalibration is not normally required. Recalibration is appropriate only in situations where the DDG has not been triggered for an extended interval (hours or days), the ambient temperature may have changed significantly during this time, and maximum precision is demanded on the next expected trigger event.

5.6 The V850.EXE Program

An MS/DOS-based program is available for use with the V850 family of delay generators. The program can be used, with a PC-to-VME interface, to directly set up and control DDG modules. Even if a hardware interface is not available, the program may be used to set up a virtual DDG, and then display, print, or save register contents as an aid to programming.

The V850 program includes extensive HELP screens and is useful in evaluating the capabilities of the V850 family of products.

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