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IPC 620 Programmable Controller

Model IPC 620-25 and 620-35

User Manual

Form 620-8984
Rev. B
Effective: 2/88
Supersedes: 1/87

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USER MANUAL CROSS REFERENCE FOR IPC 620-25/35 PROCESSORS

MANUAL:	MATERIAL COVERED:
IPC 620-25 and 620-35 Processor User Manual Form No. 620-8984	Detailed hardware description; 620-25 and 620-35 system configurations (processor and I/O); modes of operation; processor diagnostics; instruction set and opcodes.
IPC 620 Installation User Manual Form No. 620-8996	620 system overview; system configuration for all processor models, parallel and serial I/O; addressing; rack assembly mounting; module settings (jumpers and DIP switches); module installation; cable and conduit routing; wiring; reference information on superseded model numbers.
IPC 621 I/O Specifications User Manual Form No. 620-8995	I/O system overview; detailed module descriptions (digital input, digital output, special function); serial I/O system; fuse and battery requirements.
IPC 623-51 Loader/Terminal User Manual Form No. 623-8999	Hardware description; installation; modes of operation; programming instructions and examples; editing and display functions; documentation and tape functions; trouble-shooting and maintenance; codes and error messages.
IPC 623-60 MS-DOS Loader User Manual Form No. 623-8993	Product description and requirements; installation and configuration; system start-up and menus; IPC 620 instruction set; edit and display functions; program editing instructions; documentation; utility functions.
IPC 620 Control Network Introduction/User Manual Form No. 620-8994	Control Network overview; hardware description; modes of operation; CNM communications; diagnostics; configuration; DIP switch settings; addressing; installation.
IPC 620 Redundant Control System User Manual Form No. 620-8983	Redundant Control System overview; detailed hardware description; installation; configuration; applications considerations; modes of operation; theory of operation; DIP switch settings.
IPC Data Collection Modules User Manual Form No. 620-8980	Overview of 620-0048 and 620-0052 modules; detailed hardware descriptions; theory of operation; instruction set, opcodes and descriptions; installation; wiring; Asynchronous Byte Count Protocol; DIP switch settings.
IPC Communications Interface Module Form No. 620-8986	Overview of the 620-0043 CIM; hardware description; configuration; installation; wiring; instruction set; DIP switch settings.
IPC Hiway Interface Module User Manual Form No. 620-8981	Overview of the 620-0081 HIM; hardware description; functional description; configuration; operation; diagnostics; DIP switch settings.
Network Guide, Form No. 74-WS-29-01 Gateway User Manual, Form No. 82-50-10-16	Information on the 620-0044 CIM.

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INTRODUCTION

The IPC 620 Programmable Controller System fulfills three important factory automation requirements:

* Control
* Communications
* Monitoring

The 620 System consists of a choice of five control processors, a Universal I/O system, two programming devices, an industrial microcomputer plus, related software products, motion control products, monitoring products, and communication systems.

This manual covers the use of the 620-25 and 620-35 processors. Other 620 system products— the 623-51 Loader/Terminal, 627-70 Microcomputer, motion control products, 620 Control Network, 626 Support Controller, software products, and the other 620 processors are supported by their own literature. The User Manual Cross Reference Table summarizes the material covered in other 620 user manuals referenced in this manual.

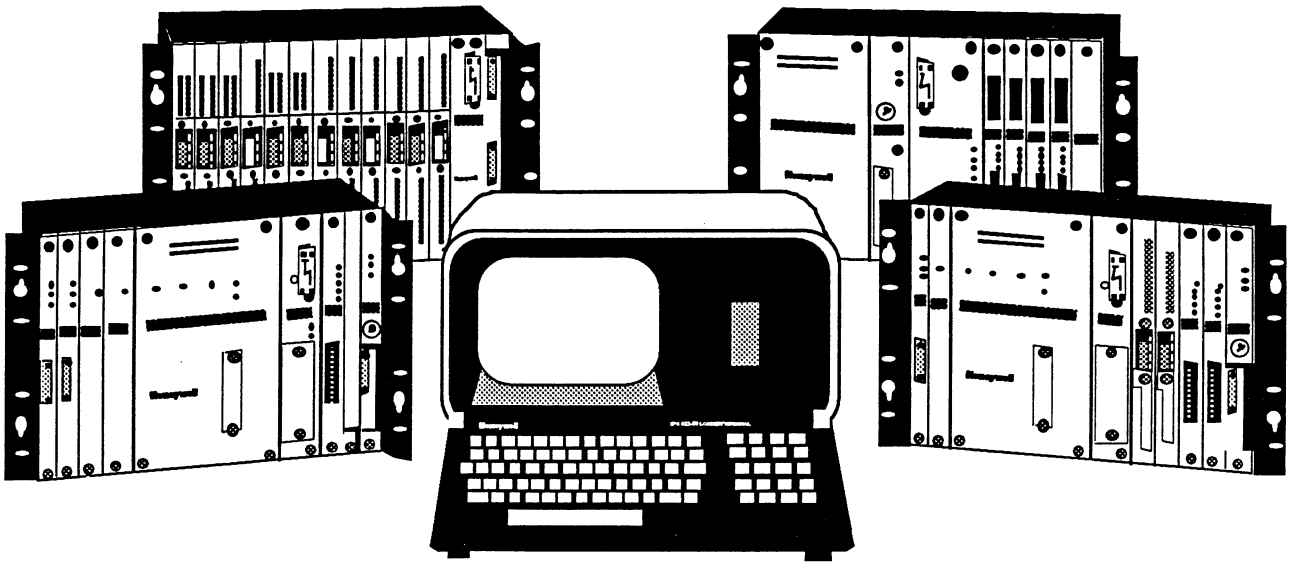


FIGURE 1 - 620-25 AND 620-35 SYSTEM

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SYSTEM SPECIFICATIONS

AC VOLTAGE *.....115/230± 15% **
FREQUENCY *.....47 to 63 Hz

DC VOLTAGE *.....20 to 28VDC

NORMAL LOAD *.....115 Watts

SURGE CURRENT *.....15A 1 cycle from cold start

POWER FAIL LEVEL *.....115VAC - 85VAC
230VAC - 190VAC
24VDC - 19VDC

POWER FAIL DELAY *.....11.5ms (115VAC)
7.0ms (24VDC)

OPERATING TEMPERATURE *.....0 to 60° C

STORAGE TEMPERATURE *.....-40 to 85° C
(-40 ° to 70° C with battery)

RELATIVE HUMIDITY *.....5% to 95% (non-condensing)

HEIGHT *.....10.7in (27.2cm)

WIDTH *.....19in (48.3cm)
[I/O Half rack 10in (25.4cm)]

DEPTH *.....7.5in (19.1cm)

I/O CAPACITY.....2048 max.

CONTROL RELAY CAPACITY.....2048 or 4096

DATA REGISTERS.....2048 - 4096

REGISTER SIZE.....17-Bit
(16-bit plus sign bit)

MEMORY SIZES.....2K, 4K, 8K, 16K, 24K, 32K words

MEMORY TYPE.....Read/Write CMOS

BATTERY BACKUP.....1.5 years minimum

BATTERY.....Size D Lithium (629-3001)
(located in Power Supply Module)

MEMORY USAGE.....One word per ladder diagram element

SCAN RATE.....2.5ms per K (Relay only)***
6.05ms per K (Nominal Mix)***
8.88ms per K (Math intensive)***

* Also applies to the 621 I/O system.

** 250VAC maximum (fuse rating).

*** Based on analysis of actual user programs for machine control

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620-25 AND 620-35 PROCESSOR COMPONENTS

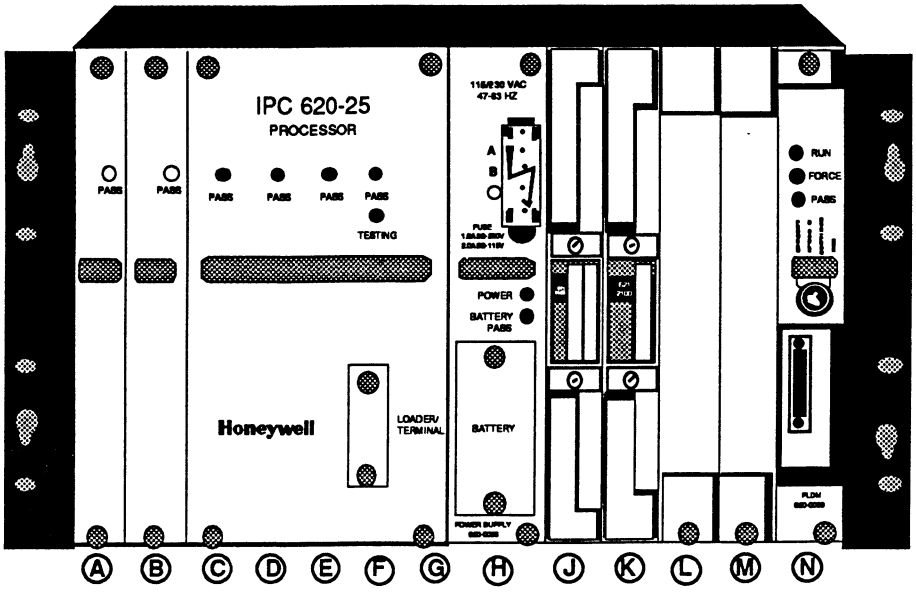
The 620-25 or 620-35 processor systems may be ordered as individual components or as a processor system package. Refer to the 620 System Configuration Guide and the Price List for detailed ordering information. Figures 2 and 3 show processor rack configurations. A basic processor is assembled from the components listed in Table 1.

The 620-25/35 processors can also include various option modules. There are four slots in the 620-35 (two in the 620-25 processor rack) to accommodate optional modules. Option slots that are not used are enclosed with blank coverplates. Empty SLM slots are enclosed with coverplates which are ordered separately. Table 2 shows which option modules can be incorporated into the basic processors.

TABLE 1 - BASIC 620-25 AND 620-35 COMPONENTS

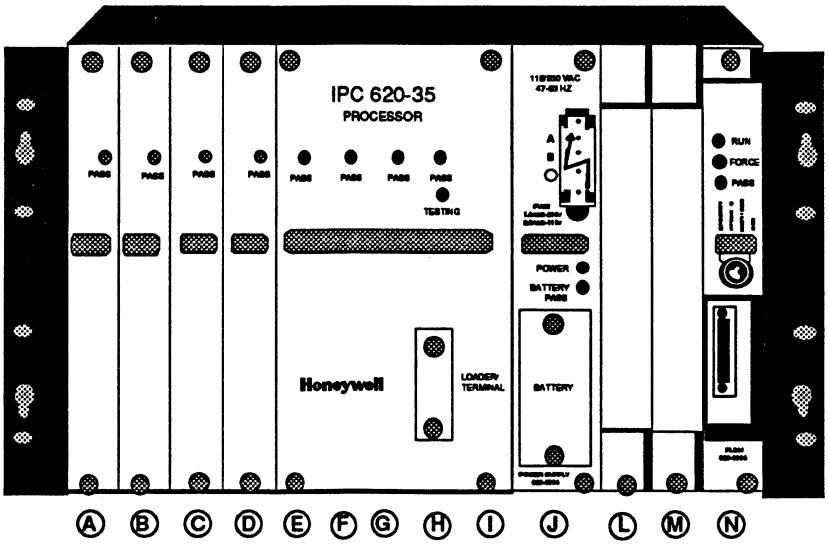
COMPONENT	MODEL NO.
620-25 Processor Rack	620-2590
620-35 Processor Rack	620-3590
620-25/35 Processor Module	620-0080
620-25/35 System Control Module	620-0054
Memory Module (2K)	620-0025
Memory Module (4K)	620-0026
Memory Module (8K)	620-0027
Memory Module (16K)	620-0023
Memory Module (24K)	620-0024
Register Module (2K X 2K)	620-0055
Register Module (4K X 4K)	620-0056
512 I/O Control Module	620-0057
1024 I/O Control Module	620-0058
2048 I/O Control Module	620-0085
Power Supply Module (115/230VAC)	620-0036
Power Supply Module (24VDC)	620-0047
Parallel Link Driver Module	620-0086
Serial Link Module	621-9939

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A Blank slot for optional module
B Blank slot for optional module
C Memory Module
D Register Module
E System Control Module
F Processor Module
G I/O Control Module
H Power Supply Module
J I/O *
K I/O *
L I/O or Serial Link Module *
M I/O or Serial Link Module *
N Parallel Link Driver Module

FIGURE 2 - 620-25 RACK CONFIGURATION



A Blank slot for optional module
B Blank slot for optional module
C Blank slot for optional module
D Blank slot for optional module
E Memory Module
F Register Module
G System Control Module
H Processor Module
I I/O Control Module
J Power Supply Module
L Serial Link Module
M Serial Link Module
N Parallel Link Driver Module

FIGURE 3 - 620-35 RACK CONFIGURATION

* Refer to TABLE 4 - INPUT/OUTPUT MODULE for a selection of available I/O and to FIGURE 12 - PARALLEL I/O CONFIGURATION, and FIGURE 13 - REMOTE SERIAL I/O CONFIGURATION for more information. The 620-25 Processor Rack does not accommodate I/O modules that use PUSH/PULL interface or 32-point I/O modules.

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PROCESSOR RACK
Model No. -- 620-2590 (620-25)
620-3590 (620-35)

The processor racks include the chassis, backplane, and frontplates. The processor modules are vertically positioned in the racks with component side toward the left. Backplane connectors are offset to prevent inserting a module upside down. Card slots (labeled A through N) and the modules which they accommodate are shown in Table 3.

The rack fits into an 8-inch NEMA 12 enclosure, or a 19-inch instrumentation rack. The rack conforms to the European "HE" standard. Reversible mounting brackets allow the rack to be panel mounted. When the brackets are attached to the rack front, it mounts in a standard 19-inch rack. When the brackets are rotated 180° and mounted to the rear, the rack can be panel mounted.

TABLE 2 - OPTION MODULES IN PROCESSORS

MODULES	SYSTEM QUANTITY	
	620-25	620-35
Control Network Module (620-0038)	1 - 2	1 - 4
Communications Interface Modules (620-0044, 620-0043)	1 - 2	1 - 4
Data Collection Module (620-0048, 620-0052)	1	1
Hiway Interface Module (620-0081)	1	1
Redundancy Control Module (620-0059)	1	1

TABLE 3 - RACK SLOTS ASSIGNED TO PROCESSOR MODULES

MODULE	RACK SLOT ASSIGNMENT	
	620-25	620-35
Optional Modules (Blank coverplates provided with rack)		
Control Network Modules	A & B	A - D
Communication Interface Modules	A & B	A - D
Data Collection Module	A & B	A - D
Highway Interface Module	A & B	A - D
Redundancy Control Module	A & B	A - D
Memory Module	A - C	A - E
Register Module	D	F
System Control Module	E	G
Processor Module	F	H
I/O Control Module	G	I
Power Supply Module	H & I	J & K
I/O Modules *	J, K, L & M	----
Serial Link Modules	L & M	L & M
Parallel Link Driver Module	N	N

* The 620-25 Processor Rack does not accommodate I/O modules which use the PUSH/PULL interface.

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MEMORY MODULE (MM)

Model No. - 620-0025 (2K, 2048 words)
620-0026 (4K, 4096 words)
620-0027 (8K, 8192 words)
620-0023 (16K, 16,384 words)
620-0024 (24K, 24,576 words)

The Memory Module stores the user control program. The green status LED, labeled PASS, located on the front of the module energizes after successful completion of the module self-test. The memory module is positioned in cardrack slot C in the 620-25 and E of the 620-35.

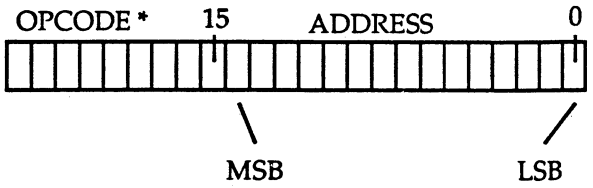
Additional memory modules can be inserted in option slots A - B in the 620-25 or slots A - D in the 620-35 to increase memory capacity to 32K. The memory starting address must be set for each module, forming contiguous memory space in order for a complete memory scan to occur during operation.

A 4-position DIP switch, located on the front, sets the starting address for the module. Setting a switch ON adds that switch's value to the starting address. The starting address is set at zero in systems using a single memory module. Each additional memory module's starting address is set to the total amount of memory in the system less the capacity of the additional memory module. (e.g. A system contains 20K of memory. The first memory module is 16K and the starting address is 0. The second memory module is 4K and the starting address is 16K.)

The front DIP switch has the following values:

SWITCH NO.	SWITCH VALUE OFF	ON
1	0	2K
2	0	4K
3	0	8K
4	0	16K

Each memory word contains 24 bits. Memory word organization is as follows:



* See the Appendix for an OPCODE list.

REGISTER MODULE (RM)

Model No. - 620-0055 (2K x 2K)
(2048 I/O, 2048 Registers)

620-0056 (4K x 4K)
(4096 I/O, 4096 Registers)

The Register Module contains the system's I/O Data Table. The data table is divided into three areas; the I/O Status Table, System Status Table, and the Register Tables.

The I/O Status Table contains either 2048 (2K x 2K) or 4096 (4K x 4K) continuous single bit storage locations which have a starting address of 0. In the 2K x 2K Register Module 2048 single bit locations are available for real I/O status or internal coils. In the 4K x 4K Register Module 2048 locations are available for real I/O status or internal coils, and an additional 2048 locations are available for internal coils.

Timer and counter preset and accumulated values are stored in the register area. Other numerical data may be stored in the bit or register area (see Figure 4). The register area is 16 bits wide plus a sign bit. The 17th bit is normally used to indicate the sign of the data contained in the register. In certain operations it will indicate overflow conditions.

The System Status Table stores processor diagnostic information that can be accessed by the Loader/Terminal or by the PULL instruction in the control program. The System Status Table consists of memory locations 8 bits wide. The table is divided into three sections: System Diagnostics, System Hardware Status, and System Identification. The contents of the System Status Table are defined in Appendix A.

The Data Table is battery-backed to ensure data retention during system power outages. All register addresses are cleared to 0 when a total memory clear operation is executed.

The Register Module is installed in slot D in the 620-25 and slot F in the 620-35. The green LED labeled PASS energizes after successful completion of the module self-test.

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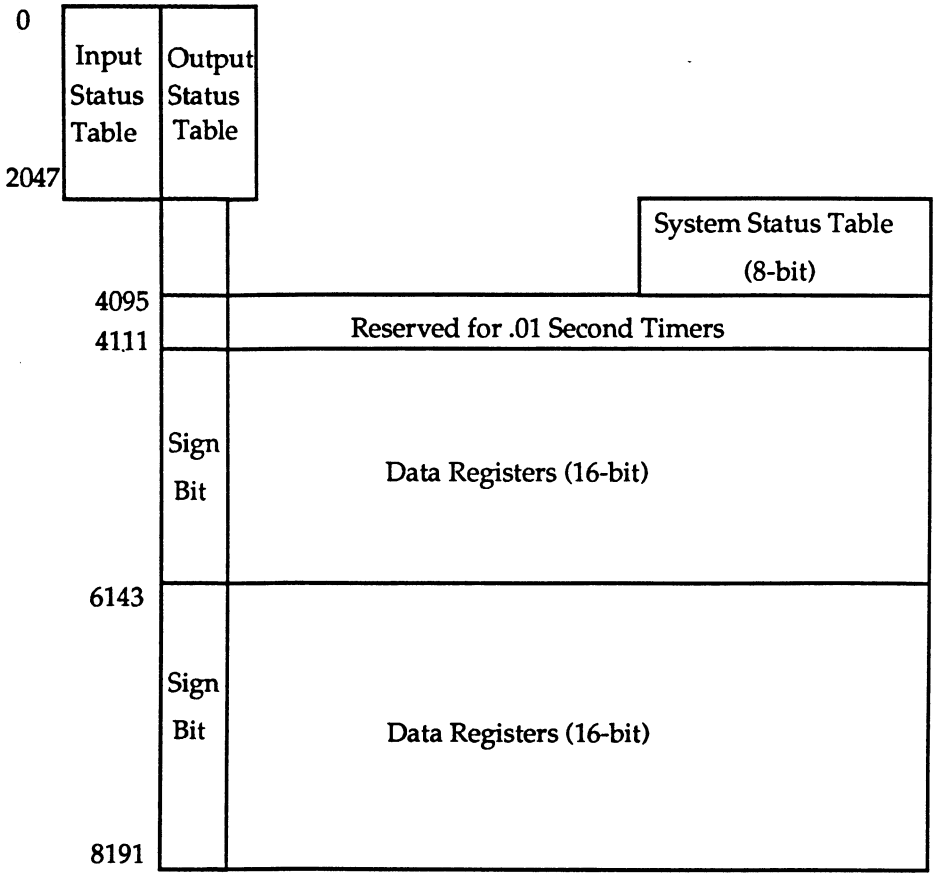


FIGURE 4 - REGISTER MEMORY MAP

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SYSTEM CONTROL MODULE (SCM)

Model No. -- 620-0054

The System Control Module, a functional extension of the Processor Module, coordinates the interaction of all the modules in the processor. The SCM also contains a single-bit processor that solves all relay logic in the control program.

The SCM is installed in rack slot E in the 620-25 and slot G in the 620-35. A status indicator is located on the front panel of the SCM. The green LED labeled PASS energizes after successful completion of the self-test.

PROCESSOR MODULE (PM)

Model No. -- 620-0080

The Processor Module executes the program stored in the memory module and handles arithmetic computation and data movement instructions.

The Processor Module is installed in slot F in the 620-25 and slot H in the 620-35. Two status indicators are located on the front of the PM. The green LED labeled PASS energizes when the module passes its self-test. The red LED labeled TESTING energizes when the series of diagnostic tests are initiated on system power-up. The TESTING LED appears to remain energized as long as the processor is scanning since a short series of diagnostics, which occurs at the beginning of each scan, continually activates it. The port labeled Loader/Terminal connects to the 623-51 Loader/Terminal and is protected by a removable coverplate.

I/O CONTROL MODULE (IOCM)

Model No. -- 620-0057 (512 I/O)
620-0058 (1024 I/O)
620-0085 (2048 I/O)

The Input/Output Control Module coordinates communications between the processor and the 621 I/O system and formats the data flowing between the I/O system and the processor. It also monitors individual I/O module fault diagnostics. The IOCM works in conjunction with the Parallel Link Driver Module and/or Serial Link Module to control data flow to I/O. The IOCM is installed in slot G in the 620-25 and slot I of the 620-35.

POWER SUPPLY MODULES (PSM)

Model No. -- 620-0036 (115/230VAC)
620-0047 (24VDC)

The Power Supply Module provides power to operate the processor. The PSM is installed in slot H in the 620-25 and J in the 620-35. The module occupies the space of two processor rack slots - H and I in the 620-25 and J and K in the 620-35.

A battery compartment in the PSM contains a lithium battery which provides backup power to the memory and register modules. The PSM is shipped with the battery installed.

NOTE

An insulating wafer prevents battery discharge during shipment and storage and must be removed before the system is operated. A figure showing how to remove the wafer is shown under Module Installation in the 620 Installation Manual (Form No. 620-8996).

The PSM provides a maximum of 15 Amps of +5DC power for use by the processor rack modules. It also supplies 300mA of ±12VDC for optional modules requiring those voltages.

Two status indicators are located on the front of the PSM. A green LED labeled POWER indicates that power is being applied to the module. A green LED labeled BATTERY PASS remains energized as long as the battery is in good condition and power is applied.

Model No. -- 620-0036 (115/230VAC)

Terminals on the front panel are labeled A (Line or L1), B (Common or L2), and GND for connecting AC power wiring. The 620-0036 operates on user-selected voltage of 115VAC or 230VAC. The yellow shorting board located inside the side cover at the top rear edge sets the AC voltage.

The 620-0036 contains a front-accessible fuse holder. The module is shipped with a 2 Amp SLO-BLO fuse installed for 115VAC operation. A 1 Amp SLO-BLO fuse for 230VAC is also shipped with the PSM.

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Model No. -- 620-0047 (24VDC)

Terminals on the front panel are labeled +, -, and GND. The 620-0047 operates on 20-25VDC voltage.

The 620-0047 contains a front accessible fuse holder. The module is shipped with an 8 Amp SLO-BLO fuse.

PARALLEL LINK DRIVER MODULE (PLDM)

Model No. -- 620-0086

The Parallel Link Driver Module works with the IOCM module to control I/O communications. The PLDM also controls system status by the mode keyswitch, and it determines I/O response to system faults and various operating parameters. The PLDM is installed in slot N in both the 620-25 and 620-35 processors.

The front panel of the PLDM contains three LED status indicators, a processor mode keyswitch, and a D connector that interfaces the processor with the I/O system.

The green LED labeled RUN energizes while the processor is scanning the ladder diagram program and is operating correctly. The red LED labeled FORCE energizes when at least one address in the program is in the forced state. The green LED labeled PASS energizes when the PLDM has passed its self-test.

The processor keyswitch has four positions for selecting processor mode of operation. The positions are labeled PROGRAM, DISABLE, RUN/PROG, and RUN.

Two DIP switch banks are located on the top edge of the PLDM. The banks are labeled SW 1 (four switches) and SW 2 (eight switches). The switches select the I/O response to system faults and various operating parameters.

This module replaces the 620-0033. The two modules are the same physically and functionally.

SERIAL LINK MODULE (SLM)

Model No. -- 621-9939

The SLM frontplate has five LED's indicating the status of the module. The operating states of the SLM are shown by the status of the front panel LED's. These states are shown in Table 11 in Appendix A.

The green active light indicates that data is being transmitted properly. The normal state of the light is ON during transmission. There is one of these LED's for each channel.

There is a yellow link fault LED for each channel. It indicates that a rack fault or a communication fault has occurred on the channel. The normal state is OFF. When a link fault occurs, this LED turns ON. It remains ON as long as the problem exists, unless power is cycled at the SLM or the serial system in which the fault exists is reset by shorting the reset terminals at the SLM.

After the SLM has been reset or had power cycled, the serial system re-initializes. This includes the drops taken off-line, except those that have been manually powered down because of the fault, and the link fault LED is turned OFF. The LED remains ON if the faulted racks are restarted by a means other than resetting or cycling power at the SLM.

A DIP switch, SW1, located near the top edge of the circuit board configures the SLM. The switch settings are shown in Table 9 in Appendix A.

This module must be used with SIOM 621-9938 or 621-9940. Also, this module replaces the 621-9936 which is described in Appendix B and must be used with SIOM 621-9935.

COMMUNICATIONS INTERFACE MODULES (CIM)

Model No. -- 620-0044
620-0043
620-0048
620-0052

The Communications Interface Modules are optional in the 620-25/35 processor. They provide interface to the 627-70 COP microcomputer or other serial devices. See the respective documentations for further information. The contents of the user manuals for these products are listed in the User Manual Cross Reference Table.

CONTROL NETWORK MODULE (CNM)

Model No. -- 620-0038

The 620 Control Network is an easy-to-use, high speed peer-to-peer communication network, providing peer-to-peer communication between a maximum of eight 620 processors. Installing a CNM in the 620-25/35 enables the processor to communicate with as many as seven other 620 processors,

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transferring I/O status bits or register data between processor systems which are interconnected on a multi-drop twisted-pair serial link. Two CNM's may be installed in the 620-25 and four CNM's in the 620-35 enabling the processors to communicate with as many as two or four separate Control Networks respectively. The CNM may be installed in any of the option slots A or B in the 620-25 and A through D in the 620-35. See CNM documentation for further information. The contents of the CNM User Manual are listed in the User Manual Cross Reference Table.

HIWAY INTERFACE MODULE (HIM)

Model No. -- 620-0081

The HIM acts as an interface between an IPC 620 Processor and Honeywell's TDC-3000 Data Hiway. The HIM provides a service facility for higher order devices in the system, such as computers and operator stations to interface with the IPC 620 Processor.

The HIM is a single-slot option module that can be installed in any IPC 620 Processor rack. It provides redundant BNC connectors that attach directly to the Data Hiway. The module has the same functional capacity as up to four Data Hiway Port (DHP) modules. It also implements the same point structure as the DHP from the Data Hiway. See the HIM User Manual for further information.

REDUNDANCY CONTROL MODULE (RCM)

Model No. -- 620-0059

The Redundancy Control Module is the primary component in the Honeywell IPC 620 Processor Redundancy System. The high-availability control system requires minimal hardware and installation effort. It operates with the IPC 620-25 or 620-35 Processors. The system consists of two identically configured processors, each containing an RCM. Both processors are connected to a common I/O system. The RCM's are connected to each other by a data cable. Redundant systems can be configured using parallel, serial or both types of I/O. See Redundant Control System User Manual for more information.

621 I/O SYSTEM

The I/O system consists of I/O full or half racks, Power Supply Modules, Parallel or Serial I/O Modules, and various digital, analog and special function I/O modules.

621 I/O FULL RACK

Model No. -- 621-9990

The 621 I/O full rack is identical in size to the 19-inch 620 processor racks. It is designed for installation in 8-inch NEMA 12 enclosures or 19-inch instrumentation racks. It holds a maximum of 12 I/O modules, either a Parallel or Serial I/O Module, and a Power Supply Module.

Model No. -- 621-9992

The 621-9992 augmented I/O rack is identical to the 621-9990 I/O rack in size and function. It contains an additional upper bus on the backplane to facilitate communication between modules within the I/O rack . This rack is used with modules which require dual bus communication (ie. Servo Modules).

621 I/O HALF RACK

Model No. -- 621-9991

The half rack is approximately one half the width of a full rack. It accommodates a maximum of six I/O modules, a Parallel or Serial I/O Module and a Power Supply Module. The half rack is useful for installation in narrow enclosures such as motor control centers.

I/O RACK POWER SUPPLY MODULES (PSM)

Model No. -- 621-9932 (8A, 24VDC)

The 621-9932 I/O Rack Power Supply provides 8 amps of +5VDC for the I/O logic circuitry in the rack. It also supplies 600mA of ±15VDC power. Refer to the 620 Installation Manual for individual module power requirements.

The maximum power consumption of the 621-9932 Power Supply is 96VA. A cold start surge of this power supply requires a maximum of 40 amps.

The required input is 20-28VDC with a 24VDC nominal input. The Power Supply Module offers a front-accessible fuse holder and is shipped with an 8A Fast-blo fuse. A green LED labeled 5V PASS is energized when the 5VDC power is present.

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Model No. -- 621-9933 (15A, 115/230VAC)

The 621-9933 I/O Rack Power Supply is a double-wide module that provides 10 to 15 amps of +5VDC for the I/O logic circuitry in the rack. It also supplies 1.3 to 2 amps of ±15VDC. The graph in Figure 5 shows the relationship of current loads between the ±15VDC source and the ±5VDC source. If, for example, the ±15VDC source requires 2 amps, the 5VDC can draw a maximum of 10 amps. If the ±15VDC requires 1.3 amps, the ±5VDC can draw a maximum of 15 amps. Refer to the 620 Installation Manual or individual module specifications for module power requirements.

The maximum power consumption of the 621-9933 Power Supply is 110VA. A cold start surge requires a maximum of 20 amps for one cycle.

The input is selectable for 115 or 230VAC by the position of a toggle switch located under the component cover of the Power Supply. The 115VAC selection allows a voltage range of 85 to 132VAC. The 230VAC allows a 170 to 250VAC operation. The frequency for both ranges is 47 to 63 Hz. The Power Supply Module offers a front-accessible fuse holder. It is shipped with a 4.0A SLO-BLO fuse installed for 115VAC operation. The 230VAC 2.0A SLO-BLO fuse is also shipped with the module. One green LED, labeled 5VDC, is energized when the 5VDC power is present.

NOTE
Be sure to match the 115/230VAC toggle switch with the module fuse.

Model No. -- 621-9934 (8A, 115/230VAC)

The 621-9934 I/O Power Supply provides 8 amps of +5VDC power. This module also provides 600mA of ± 15VDC power for the operation of some special function I/O and analog I/O modules. The power supply is selectable for 115/230VAC operation, 47- 63Hz.

A terminal block at the top of the module front coverplate is labeled with an A (Line or L1), a B (Common or L2), and a ground symbol for AC input wiring termination. A front-accessible fuse holder houses a 2 amp SLO-BLO fuse for 115VAC operation. A 1 amp SLO-BLO fuse for 230VAC operation is also shipped.

PARALLEL INPUT/OUTPUT MODULE (PIOM)
Model No. -- 621-9937

The PIOM is located in the N slot in the full I/O rack or the H slot in the I/O half rack. This module acts as the interface to the processor Parallel Link Driver Module and to other PIOMs. The PIOM has two 50-pin D-type connectors. The male plug (top) is the IN port and the female plug (bottom) is the OUT port. The green LED, labeled ACTIVE, indicates proper communication from a preceding rack.

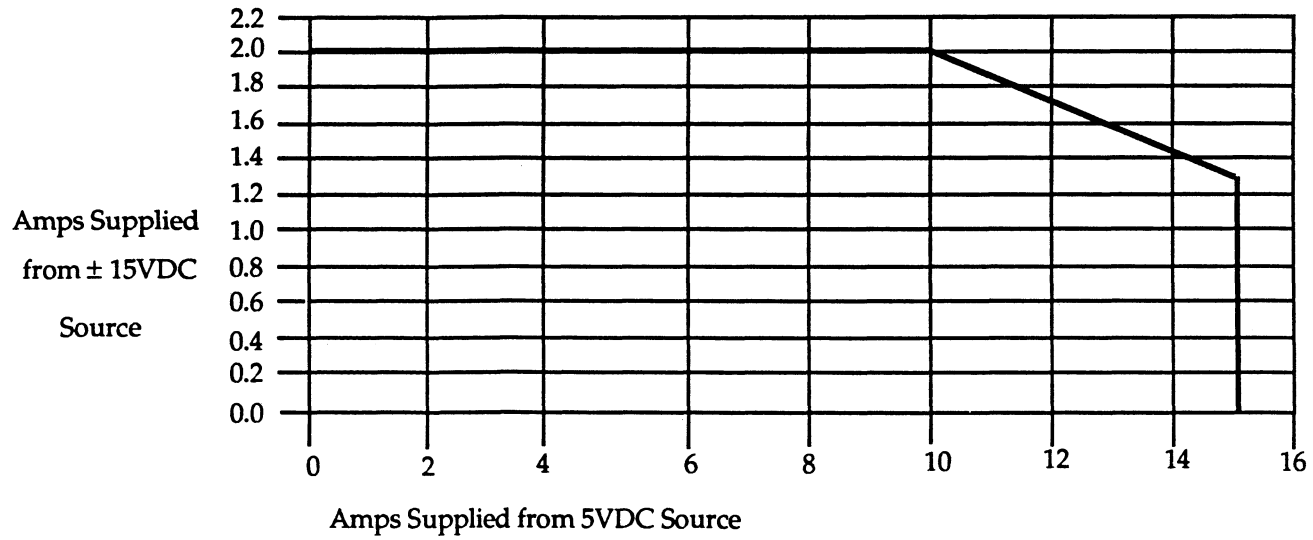


FIGURE 5 - RELATIONSHIP BETWEEN ±15VDC AND ±5VDC SOURCE CURRENT LOADS (MODEL 621-9933)

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Two DIP switch banks, SW1 and SW2, select rack configuration and output handling. Three DIP switch banks, SW3, SW4, SW5 set the number of I/O points used in each I/O rack slot.

The 621-9937 replaces the 621-9930. See Appendix B for information on the 621- 9930.

SERIAL INPUT/OUTPUT MODULE (SIOM)
Model No. -- 621-9938, 621-9940

The 621-9938 has two serial ports and the 620-9940 has one. The 621-9938 is used in redundant applications which require communication with redundant processors. The 621-9938 frontplate has six LED's for indicating the module status and the 621-9940 has three. The green active LED indicates that the associated port is transmitting and receiving data properly. The light is ON when transmitting.

The green pass LED indicates the SIOM has successfully completed its self-test which occurs on power-up and when the SIOM reset terminals are closed. The normal state is ON.

The yellow rack fault LED indicates that an output module data fault has occurred. The LED is normally OFF.

The green lead LED indicates that the port is connected to the lead processor in a redundant configuration and is successfully communicating with the lead processor's SLM. The normal state is ON for the port connected to the lead processor and OFF for the port connected to the backup processor. Only one LED is ON at a time.

The statuses of the front panel LED's show the operating state of the SIOM. These statuses are shown in Table 12 in Appendix A.

Five banks of DIP switches, located near the top edge of the circuit board, set how the rack is configured and how outputs are handled, and the number of I/O points used in each I/O rack slot. The functions of these switches are shown in Table 10 in Appendix A.

INPUT/OUTPUT MODULES

The 621 Universal I/O System offers a variety of 8-, 16- and 32- point digital modules, analog, and special function module types. Figure 6 shows typical I/O modules and Table 4 provides a complete list of 621 I/O modules.

Double swing terminal blocks that attach to the rack chassis fit over 8- and 16- point modules, splitting the field wiring into two small bundles. One terminal block swings down, closing from the top of the rack, the other swings up, closing from the bottom, both fitting over the installed I/O module. The terminal blocks lock open for easy installation or removal of the module without disconnecting the field wiring.

The 8-point terminal block models are factory jumpered at T1 and T2 and B1 and B2. The 16-point terminal block models are factory jumpered at T1, T2, and T3 and B1, B2, and B3. These terminals are field power and return connections and the jumpers select the number of points per common. See Figure 8.

The 32-point I/O modules use two removable connectors that attach to the front of the module. The field wiring is installed in the front of the module using set screws that can be accessed without removing the connector from the module. If a connector must be removed, metal connector bars eject the connectors from the module. See Figure 9.

623-51 LOADER/TERMINAL

The 623-51 Loader/Terminal is a programming, monitoring and documentation tool used with the 620-25/35 processors as well as the other 620 processors, the 627-70 COP Industrial Microcomputer, and other ASCII peripheral devices. The 623-51 Loader/Terminal may also be used as a stand alone 620 program development system. Refer to the Loader/Terminal User Manual 623-8999 for detailed programming and operating information.

IPC 623-60 MS-DOS LOADER

The 623-60 MS-DOS Loader is a software/hardware package that gives any MS-DOS operating system personal computer the capability to program and monitor all IPC 620 programmable controllers. The MS-DOS Loader consists of two 5 1/4-inch floppy disks, one 3 1/2 floppy disk and a board to interface to the IPC 620 PLC or a PC/PLC adapter. The easy-to-use software is menu-driven and includes a comprehensive series of help screens. The Loader integrates programming and documentation. Editing is simple because the link between ladder logic and documentation is maintained during editing.

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TABLE 4 - INPUT/OUTPUT MODULES

621 I/O COMPONENT MODEL NUMBER DESCRIPTIONS		
COMPONENT GROUP	MODEL NUMBER	DESCRIPTION
INPUT MODULES	621-0000	Analog Input, 8 channels*
	621-0009	Simulator Input Module
	621-0014	Thermocouple/mV Input Module*
	621-1100	115VAC/DC, 8-pt.
	621-1101	115VAC/DC Isolated, 6-pt.
	621-1151	115VAC, 16-pt.
	621-1175	115VAC, 32-pt.
	621-1200	230VAC/DC, 8-pt.
	621-1201	230VAC/DC Isolated, 6-pt.
	621-1500	24VAC/DC, 8-pt.
	621-1550	24VAC/DC, 16-pt.
	621-3300	5VDC Sink, 8-pt.
	621-3450	12VDC Sink, 16-pt.
	621-3500	12-24VDC Sink, 8-pt.
	621-3502	12-24VDC Sink Fast Response, 8-pt.
	621-3550	24VDC Sink, 16-pt.
	621-3552	24VDC Sink Fast Response, 16-pt.
	621-3575	24VDC Sink, 32-pt.
	621-3600	48VDC Sink, 8-pt.
	621-3650	48VDC Sink, 16-pt.
	621-4300	5VDC Source, 8-pt.
	621-4350	5V TTL, 16-pt.**
	621-4500	12-24VDC Source, 8-pt.
	621-4502	12-24VDC Source Fast Response, 8-pt.
	621-4550	24VDC Source, 16-pt.

* Uses PUSH/PULL interface exclusively and does not function in the 620-25 Processor Rack.

** Uses PUSH/PULL interface, but not exclusively. PUSH/PULL interface does not function in the 620-25 Processor Rack.

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TABLE 4 - INPUT/OUTPUT MODULES (CONT.)

621 I/O COMPONENT MODEL NUMBER DESCRIPTIONS		
COMPONENT GROUP	MODEL NUMBER	DESCRIPTION
OUTPUT MODULES	621-0007	Reed Relay, 6-pt.
	621-0010	Analog Output, 4 channels *
	621-2100	115VAC, 8-pt.
	621-2101	115VAC Isolated, 6-pt.
	621-2102	115VAC Source Self-Protected, 8-pt.
	621-2150	115VAC, 16-pt.
	621-2175	115VAC, 32-pt.
	621-2200	230VAC, 8-pt.
	621-2201	230VAC Isolated, 6-pt.
	621-2500	24VAC, 8-pt.
	621-2550	24VAC, 16-pt.
	621-6300	5VDC Source, 8-pt.
	621-6350	5V TTL, 16-pt. **
	621-6450	12VDC Source, 16-pt.
	621-6500	12-24VDC Source, 8-pt.
	621-6501	12-24VDC Source Self-Protected, 8-pt.
	621-6550	24VDC Source, 16-pt.
	621-6551	24VDC Low Power Source, 16-pt.
	621-6575	24VDC Source, 32-pt.
	621-6600	24VDC Source, 8-pt.
	621-6650	48VDC Source, 16-pt.
	621-6700	120VDC Source (0.5A), 8-pt
	621-6701	120VDC Source (2A), 8-pt.
SPECIAL FUNCTION MODULES	621-0004	System Diagnostic Module**
	621-0006	BCD Converter*
	621-0008	Pulse Input Module**
	621-0012	ASCII Communications Module**
	621-0016	Controller Access Module**
	621-0018	Absolute Encoder Module**
	621-0306	High Speed Counter**

* Uses PUSH/PULL interface exclusively and does not function in the 620-25 Processor Rack.

** Uses PUSH/PULL interface, but not exclusively. PUSH/PULL interface does not function in the 620-25 Processor Rack.

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627-70 COP MICROCOMPUTER

The 627-70 is a stand-alone industrial microcomputer. When interfaced with a programmable controller, the unit is capable of reading and writing inputs, outputs, registers and program memory. The flexibility of the BASIC09 programming language allows the COP to use programmable controller data to provide an efficient machine-to-human interface by communication with color graphic displays, printers, touch panels, card readers, etc.

The COP is available in several configurations. One configuration offers 32K for BASIC09 programming. Other configurations use RAM memory to emulate a disk drive. This COPRAM disk system offers up to 144K of RAM. The large memory enables the COP to perform sophisticated data handling functions. It includes two RS232/422 compatible ports that can be expanded to a total of eight ports, providing extensive high speed data transfer between programmable controllers (ICD and other manufacturers) and ASCII devices. Specific information pertaining to the 627-70 COP Industrial Microcomputer is contained in the 627-70 User Manual.

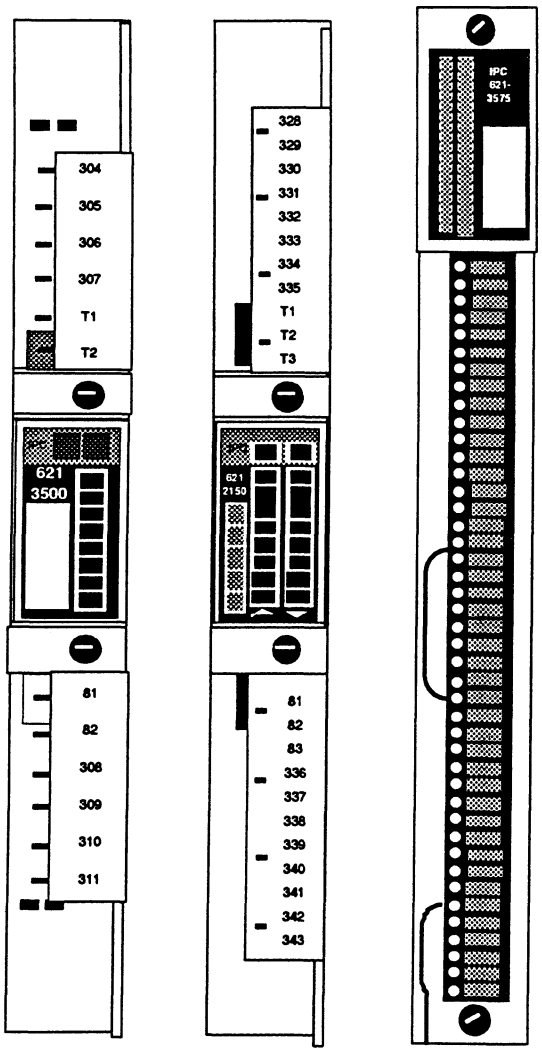


FIGURE 6 - TYPICAL DIGITAL I/O MODULES

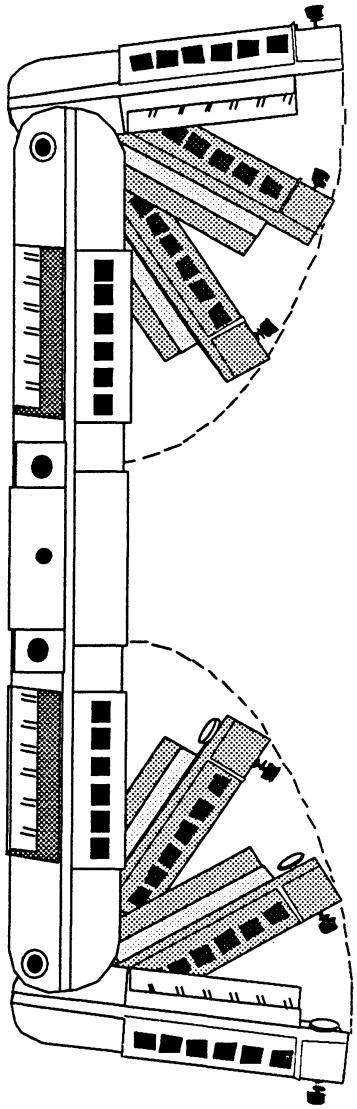


FIGURE 7 - DOUBLE SWING TERMINAL BLOCKS

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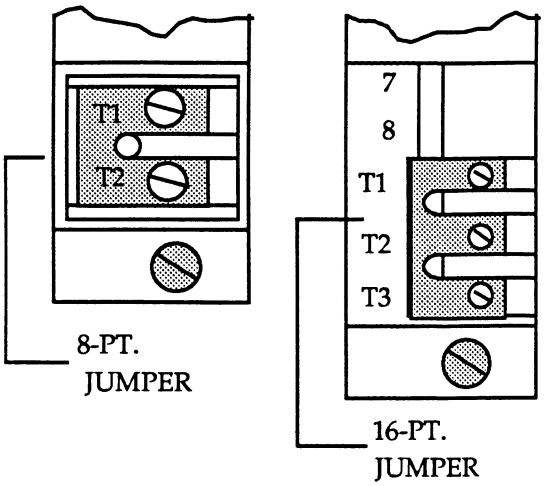


FIGURE 8 - 8- AND 16-POINT TERMINAL BLOCK JUMPERS

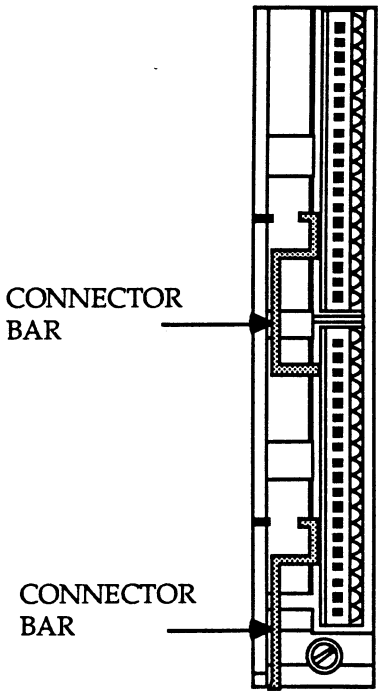


FIGURE 9 - 32-POINT I/O CONNECTORS

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LOCAL PARALLEL I/O

The Parallel I/O Configurations are designed for those applications in which long distances between 621 I/O racks and the processor are not required. A maximum data cable length of 100 feet is allotted for parallel I/O within a 620- 25/35 system.

The Parallel Link Driver Module, housed within the 620 processor rack provides a 50-pin D connector. This connector is cabled to one of the two ports on a Parallel I/O Module (PIOM) within the 621 I/O rack. Additional racks may be connected via the PIOM port in a daisy-chain fashion. The 620-25/35 offers a maximum of 2048 I/O points.

ADDRESSING

The starting address must be set for each I/O rack in a parallel I/O system, and each I/O slot must be set for 0, 8, 16, or 32 addresses. Normally, the starting address of the first I/O rack is zero. Additional I/O rack starting addresses are set at 1 plus the ending address of the previous I/O rack.

Each I/O slot is normally set for the type of I/O module to be installed in the slot (i.e. 8 addresses assigned to a slot that will contain an 8-point I/O module). Slots can be set for more addresses than the installed module (i.e. 32 addresses assigned to a slot that will contain a 16-point module). Zero can be assigned to a slot when necessary for double width modules.

SETTING PIOM 621-9937 SWITCHES

PIOM switch locations are shown in Figure 10. SW1 switches 1 - 8 set the rack starting address. These switch values are assigned in increments of 8. Closing a switch adds that value to the starting address. When I/O modules are installed in the 620-25 processor rack, their addressing begins with 0 and ends with 31 or 63 depending on whether 8 or 16 points per slot are selected on the PLDM. 32-point I/O modules cannot be used within the four I/O slots of the 620-25 Processor rack.

SW2 switches 1 and 2 determine rack output states if an output fault occurs.

SW3, SW4, and SW5 switches set the number of I/O addresses assigned to each rack slot. Each pair of switches, beginning with SW5 switches 1 and 2, set each slot A - L for 0, 8, 16 or 32 I/O points. Slots may be set for 0 points when they are occupied by multi-slot special function modules which may not require I/O addresses.

Figure 11 shows PIOM SW3, SW4, SW5 switch selections. Figure 12 shows an example parallel I/O configuration.

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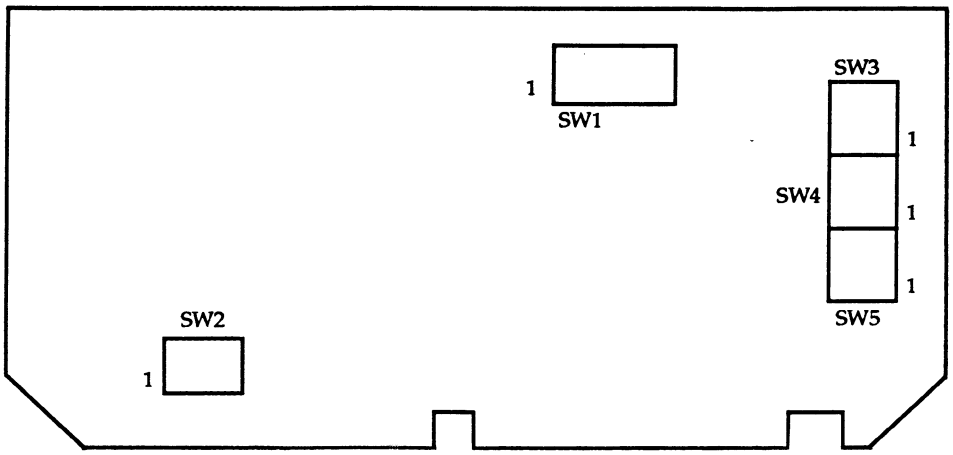


FIGURE 10 - PIOM DIP SWITCH LOCATIONS

(621-9937)

Example:
- Slot A, 16-pt. Module
  - SW5 1 ON
  - 2 OFF
- Slot B, 8-pt. Module
  - SW5 3 OFF
  - 4 ON
- Slot K, 32-pt. Module
  - SW3 5 OFF
  - 6 OFF

I/O POINTS	SWITCH PAIR	
	LOWER	HIGHER
0	CLOSED/ON	CLOSED/ON
8	OPEN/OFF	CLOSED/ON
16	CLOSED/ON	OPEN/OFF
32	OPEN/OFF	OPEN/OFF

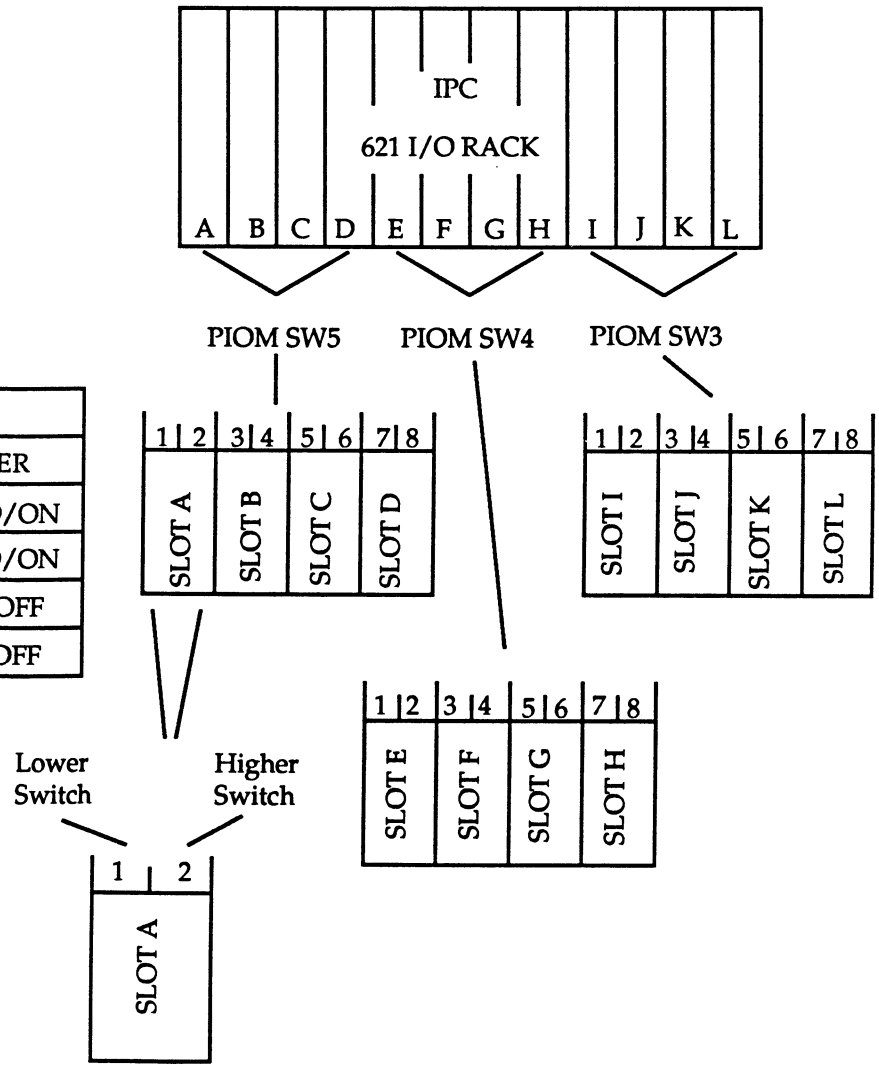


FIGURE 11 - PIOM (621-9937) SW3 - SW5 SWITCH FUNCTIONS

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RACK	RACK STARTING ADDRESS	RACK ENDING ADDRESS	I/O POINTS PER SLOT											
			A	B	C	D	E	F	G	H	I	J	K	L
1	0	223	8	8	8	8	16	16	16	16	32	32	32	32
2	224	367	8	8	8	8	16	16	16	16	32	8	0*	8

* Slots D and H are reserved for future use. Eight addresses are allowed for slot D and 16 addresses are allowed for slot H. Slots J and K of rack 2 are used for a double-wide special function module. Slot K is set for 0 since the module plugs into slot J.

	SW5								SW4								SW3							
SLOT	A		B		C		D		E		F		G		H		I		J		K		L	
SWITCH	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8	1	2	3	4	5	6	7	8
RACK 1		▒		▒		▒		▒	▒		▒		▒		▒									
RACK 2		▒		▒		▒		▒	▒		▒		▒		▒					▒	▒	▒		▒

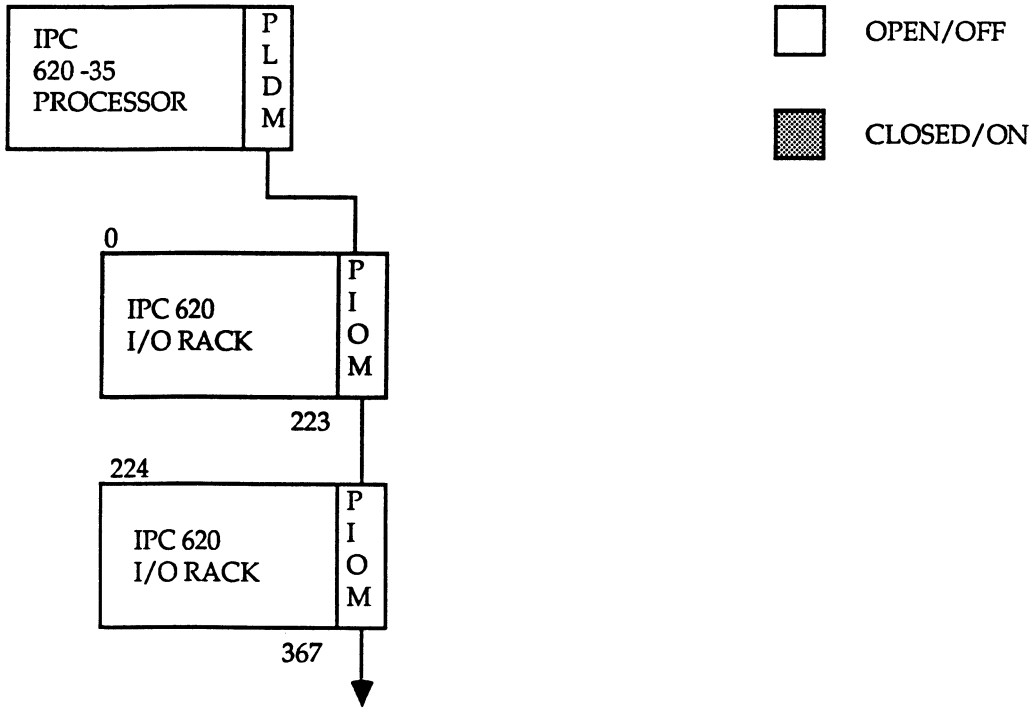


FIGURE 12 - EXAMPLE PARALLEL I/O CONFIGURATIONS

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REMOTE SERIAL I/O

NOTE

The serial I/O system described in this section supersedes the system covered in previous versions of this manual. This serial system uses Serial Link Module (SLM) 621-9939 and Serial I/O Module (SIOM) 621-9938 or 621-9940. The two systems are not compatible. Information pertaining to the superseded system, which is not obsoleted, is included in Appendix B.

SERIAL I/O SPECIFICATIONS

DATA
TRANSFER MEDIUM.....Serial 4-wire full duplex (asynchronous to processor scan)

DATA RATE.....115.2K baud

ELECTRICAL FORMAT.....RS422

SERIAL CHANNEL
SCAN RATE.....Depends on the number of racks per link, number of discrete points per link, number of racks containing PUSH/PULL cards and the number of PUSH/PULL cards updated per scan (all or 1 per scan).

MAXIMUM DROPS
PER CHANNEL.....16

MAXIMUM I/O
PER CHANNEL.....2040

MAXIMUM CHANNEL
LENGTH.....4000ft. (Belden 9729, using 200 ohm terminating resistor)
10,000ft. (Belden 9182, using 300 ohm terminating resistor)

ERROR CHECKING.....Cyclical redundancy check plus data receive time out.

Serial I/O allows I/O racks to be mounted close to the machine or process being controlled rather than at the processor. This eliminates the high cost of installing long wire runs. The 620-25/35 processor rack provides two slots, L and M, for Serial Link Modules. Two channels are operated by one SLM.

Serial I/O Modules (SIOM) which are installed in each I/O rack connect to the serial channel in a multi-drop arrangement. This allows an I/O rack to be disconnected while communication to the other remote I/O racks on the link is maintained.

The SLM operates independently of the processor, and processor scan time is not affected by remote serial I/O channels.

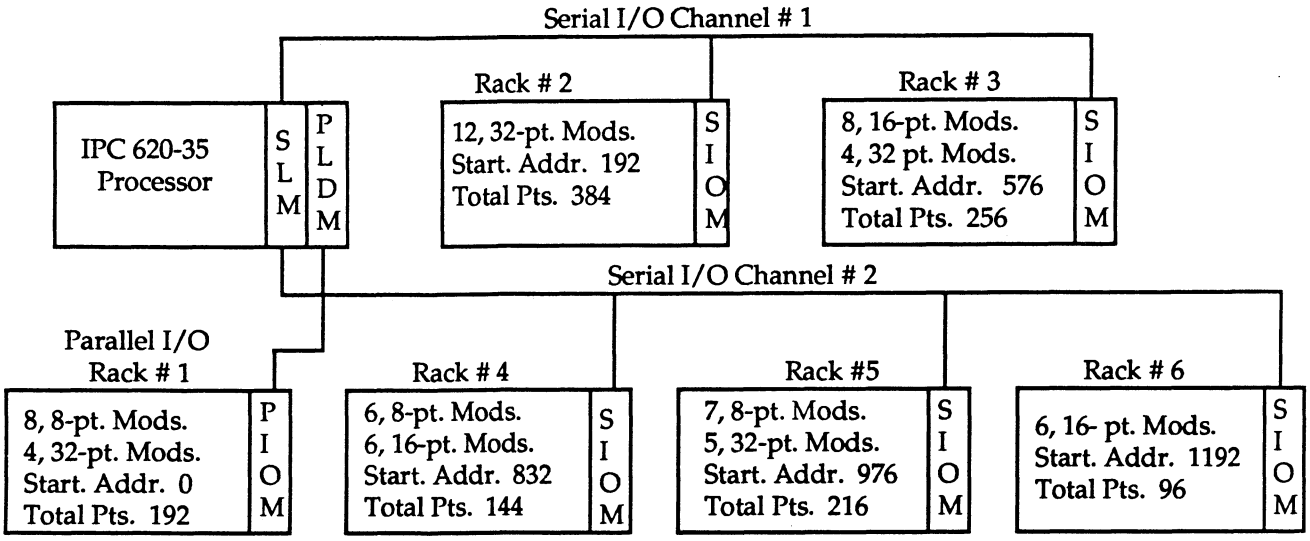
SERIAL ADDRESSING

Any mix of -0, -8, -16 and -32 point I/O modules may be used in a serial I/O rack. Setting an 8-position DIP switch establishes the starting address for each rack. Also, a pair of switches identifies each I/O slot within a rack for 0, 8, 16 or 32 points. Table 10 in Appendix A shows the switches for selecting rack addresses and identifying the number of points for I/O slots. Rack addresses are set in multiples of 8 by setting the appropriate DIP switches to the CLOSED/ON position and adding their values.

For example, in Figure 13, the starting address of the first serial I/O rack (rack # 2) is 192. Switches 4 and 5 (64 + 128 = 192) are set CLOSED/ON to assign a starting address of 192. Since rack # 2 has 384 I/O points, the starting address of rack # 3 is 576 (192 + 384 = 576). Switches 4 and 7 (64 + 512 = 576) are CLOSED/ON to asssign a starting address of 576. Starting addresses may not overlap. Serial racks may not share the same starting address or have overlapping addresses. In the example, the serial racks are shown with consecutive adresses; however this is not necessary. Real I/O addresses may be skipped between racks or the first rack on the link may have a higher starting address than the second rack, provided addresses do not overlap. Because of this feature, serial racks may be laid out to accommodate future expansion or the physical layout of the plant.

DIP switches SW3, SW4 and SW5 are set to designate the number of I/O points per slot. Each pair of switches from these banks designates the number of I/O points for an individual slot. Starting with slot A (leftmost slot) and assuming a 16-point I/O module, switches 7 and 8 of SW5 are CLOSED/ON to identify a 16-point module in slot A. This same procedure is used to set the remaining I/O slots for the corresponding point configuration. The maximum number of points per rack is 384 (32 pts. x 12 slots = 384).

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RACK	I/O MODULES		I/O PTS. PER RACK	STARTING ADDRESS	ENDING ADDRESS
	NO.	PTS.			
1	8	8	192	0	191
	4	32			
2	12	32	384	192	575
3	8	16	256	576	831
	4	32			
4	6	8	144	832	975
	6	16			
5	7	8	216	976	1191
	5	32			
6	6	16	96	1192	1287

FIGURE 13 - EXAMPLE OF PARALLEL AND SERIAL I/O ADDRESSING CONFIGURATION

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CONTROL NETWORK CONFIGURATION

A Control Network is a high speed peer-to-peer communications system in which as many as eight programmable controllers can share I/O status over a serial channel. Installing the CNM in a 620-25/35 option slot enables the processor to communicate with as many as seven other 620 processors which are connected by a multi-drop, single twisted pair half-duplex link. Each CNM on the network can transmit either 32 or 64 discrete I/O points or two or four 16-bit registers onto the network.

All processors on the Control Network operate asynchronously. The network is fast enough to provide real time control. The trunk line can extend a maximum of 8000 feet. The transmission distance can be extended with the use of modems.

Two types of Control Network configurations are possible. Typically, each processor on the network will contain only one CNM. It is optional though to install a maximum of four CNM's in the 620-25/35 processor enabling it to pass information from one network to another or to collect information from different networks. In such applications each CNM in the processor has a unique module number and a unique transfer table. Figure 14 illustrates a Control Network configuration.

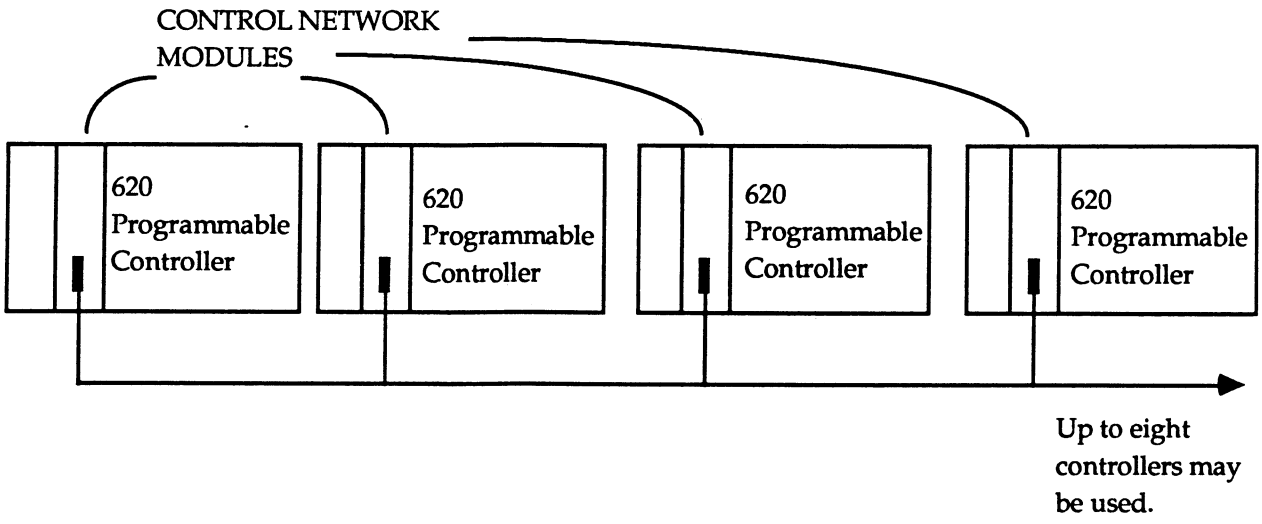


FIGURE 14 - EXAMPLE OF CONTROL NETWORK CONFIGURATION

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PROCESSOR MODES OF OPERATION

The four-position keyswitch on the front panel of the Parallel Link Driver Module determines the processor mode of operation. The 620-25/35 features four modes of operation: PROGRAM, RUN, RUN/PROGRAM, and DISABLE.

PROGRAM MODE

The system may be placed in the PROGRAM mode by the front panel keyswitch. The Processor Module does not execute the control program.

The RUN LED on the Parallel Link Driver Module (PLDM) is OFF when the system is in the PROGRAM mode. When the processor is in the PROGRAM mode, a signal is transmitted to the I/O System which allows individual I/O racks to be selected to freeze or clear outputs. Contacts may be forced if the Force Enable Switch (SW2 switch 4) on the PLDM is CLOSED/ON. Timer/counter data stored in the Register Module may be changed regardless of the state of the Data Change Enable Switch (SW2 switch 5) since the processor is already in the PROGRAM mode.

Switching the keyswitch to another processor mode removes the processor from the PROGRAM mode. If the system has been placed in the PROGRAM mode by the Loader/Terminal or a CIM, the software PROGRAM mode request must be removed from the processor causing the system to return to the mode of operation specified by the position of the keyswitch.

SOFTWARE PROGRAM MODE

The system can be placed in the Software PROGRAM Mode by the Loader/Terminal or a CIM. The programmable controller must be in the RUN/PROGRAM or DISABLE mode, and the on-line programming function enabled according to SW2 switch 6 on the PLDM. The system enters the Software PROGRAM mode only after the scan being executed is completed. When the Loader removes the Software PROGRAM Mode request, the processor leaves the software PROGRAM mode and returns to the original mode, after the system successfully executes the retentive scan and self-diagnostics.

Software PROGRAM mode changes are made through the LOADER/TERMINAL Mode change auxiliary menu. This function is particularly useful in the program debug stage for extensive changes. The user may monitor program execution, find a bug, change it, and execute the program from the keyboard.

RUN MODE

The system is in the RUN mode when the front panel keyswitch is in the RUN or RUN/PROGRAM position. The RUN mode is the main control mode for the processor.

The system executes a retentive scan when it first enters the RUN mode. During the retentive scan all nonretentive outputs from 0 to 4095 are turned OFF. The retentive outputs retain the state they were in during the last scan executed prior to being removed from the RUN mode.

After the retentive scan is complete, the user program scan begins by verifying that an Input Status Scan (ISS) instruction is located in the first memory location of the user program. While input status is being collected from the I/O system, the processor examines the card fault interrupt. If any card faults are detected in the I/O system, the fault information is inserted in the System Status Table.

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The processor then does a program memory scan by reading the second location in the Memory Module and continues through the user program until it encounters a Return to Beginning of Program or End of Memory instruction. Either of these instructions causes the scanning sequence to repeat, beginning with a new ISS. In this instance, a Return to Beginning of Program is an optional instruction programmed by the user. The End of Memory instruction is automatically deposited in the Memory Module by the device that loaded the program into memory.

Scan-Loss Timer

A scan-loss timer is reset on each scan. This timer performs a diagnostic function by timing each scan. If a scan runs beyond the scan-loss timer's setting, the timer times out. When this happens, the processor stops scanning through the user program and clears or freezes outputs in the I/O system depending on the position of PIOM SW2 switch 1. A time out causes the RUN LED to turn off. If the scan-loss timer has not reached its timeout setting before the end of the scan, the processor continues with the next scan, resetting the timer.

Some valid ladder logic programming causes the scan timer to exceed the time-out setting. This type of programming requires the scan-loss timer to be disabled. Closing SW1 switch 1 on the Parallel Link Driver disables the scan-loss timer.

CAUTION

Some of the processor's built-in diagnostic ability is disabled when the scan-loss timer is disabled.

Program Execution Sequence

Using the sample program in Figure 15, represented by the following logic lines, the program execution would be as follows:

```
  101        67                 32
---] [--------] [----------------(  )---------
   32       342                384
---] [--------] [----------------(  )---------
```

1. The first instruction (-] [- 101) is brought from memory causing a logical OR to be performed on the bits stored at address 101 of the Input and Output Status Tables of the Register Module. Assuming that input 101 was ON at input status scan, a binary 1 is stored in the Input Status Table at address 101. All output status table bit addresses are cleared to zeros during retentive scan, so the OR operation will result in a 1 (contact 101 CLOSED).

2. The next instruction, (-] [- 67) is brought from memory and a logical OR performed on the Input and Output Status Tables at address 67. Assuming that input contact 67 is closed, a binary 1 is stored in the Input Status Table at address 67.

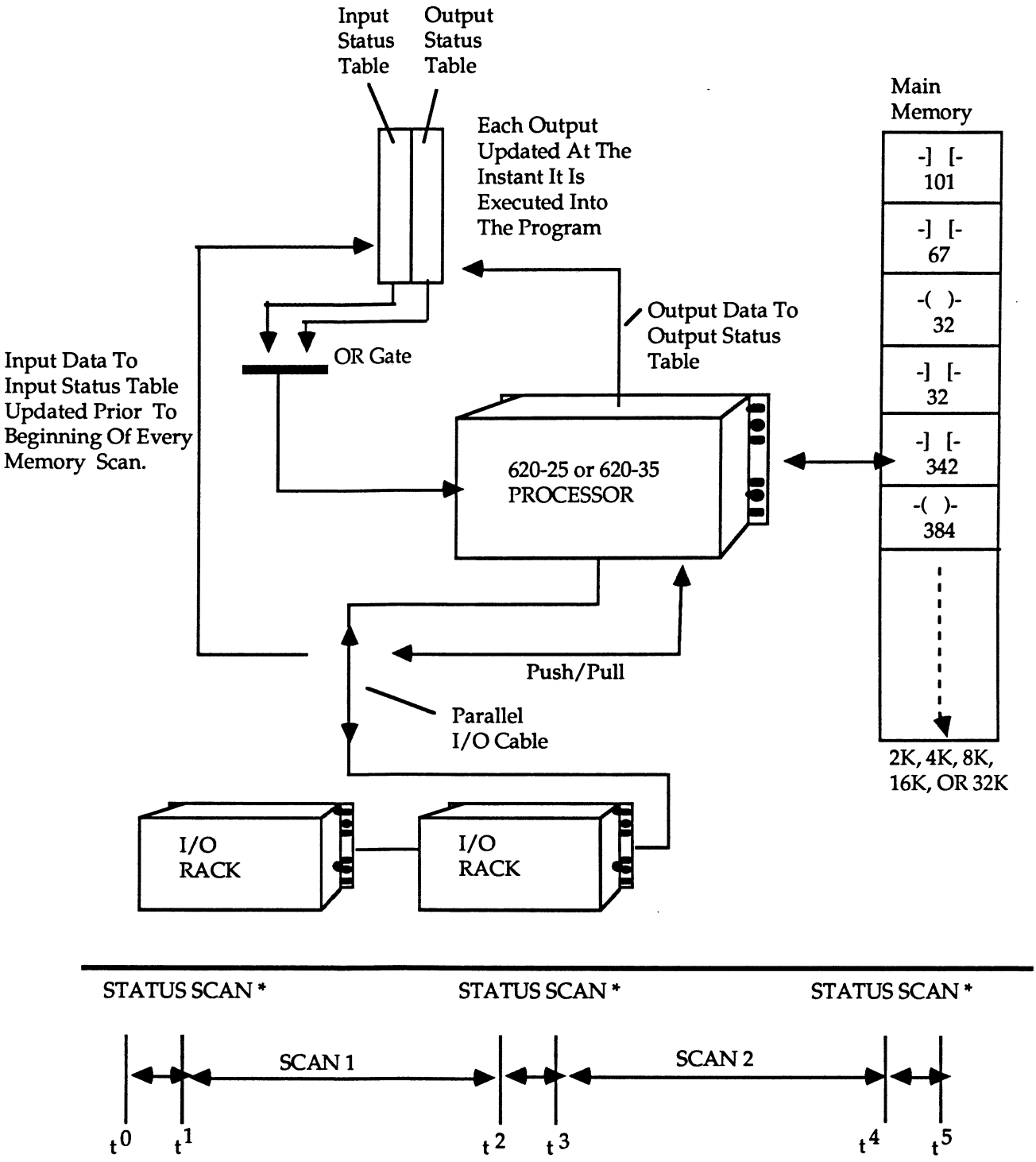
3. The next instruction, (-] [32) is brought from memory. The processor recognizes that output 32 must be turned ON since both input contacts 101 and 67 are closed. The processor transmits a signal via the field I/O bus to energize output 32 and also posts a binary 1 in address 32 of the Output Status Table.

4. The next instruction (-] [- 32) is brought from memory and a logical OR performed on the Input and Output Status Tables at address 32. Bit address 32 in the Input Status Table contains a 0, because no input module is in that position, but a binary 1 was just posted at address 32 in the Output Status Table as a result of the previous instruction. The result of the logical OR is a binary 1 (contact 32 closed).

5. The next instruction (-] [- 342) is brought from memory, and a logical OR performed on the Status Tables at address 342. Assuming that input contact 342 is OPEN, 0 is stored in the Input Status Table at address 342.

6. The next instruction (-( )- 384) is brought from memory. The processor recognizes that contact 32 is CLOSED, but contact 342 is OPEN, therefore, output 384 must be de-energized. The processor transmits the signal via the field I/O bus to de-energize output address 384 and posts a 0 in bit address 384 of the Output Status Table.

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t = TIME

* For IOCM Model 620-0057 - 771.00µs + 1-2ms for diagnostics and option slot test.
* For IOCM Model 620-0058 - 1.2ms + 1-2ms for diagnostics and option slot test.
* For IOCM Model 620-0085 2.06ms + 1-2ms for diagnostics and option slot test.

FIGURE 15 - 620-25/35 PROGRAM EXECUTION

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7. The remainder of the instructions are executed until the End of Memory instruction is reached. The EOM returns the program execution sequence to the first memory word of the program (the input status scan).

Run Mode Status

The RUN LED located on the Parallel Link Driver Module (PLDM) is energized when the system is in the RUN mode. The scan loss timer on the PLDM is enabled to time out after the time base has elapsed (determined by switches SW1 switch 2 through SW1 switch 4 on the PLDM). If the scan loss timer times out, the processor stops scanning through the user program and may or may not clear outputs in the I/O system, depending on the setting of PLDM SW2 switch 7. The internal run flag resets to run and the 0.01 second timer time base interrupt is enabled as long as the system is in the RUN mode.

PLDM switches control the following machine status options:

SW2 switch 4	Enable/Disable Force command
SW2 switch 5	Enable/Disable data change

The RUN mode offers the following options. Contacts may be forced if the force enable switch (SW2 switch 4) on the PLDM is CLOSED/ON. Timer/Counter preset and accumulated values, sequencer register values, and constant values may be changed if the data change enable switch (SW2 switch 5) on the PLDM is CLOSED/ON. Outputs in the I/O system may be cleared when the scan loss timer times out if the scan loss outputs switch (SW2 switch 7) on the PLDM is CLOSED/ON.

The processor can be removed from the RUN mode by switching the keyswitch to another position or by entering a PROGRAM mode request command from the Loader/Terminal or a CIM. This is only applicable if the processor keyswitch is in the RUN/PROGRAM or DISABLE position. When the processor receives a PROGRAM mode request, it enters the PROGRAM mode after the scan returns to the first location in the Memory Module. The processor stays in the PROGRAM mode until the requesting device removes it. Note, however, that the Loader/Terminal security code must be entered before the Loader/Terminal actually performs a processor mode change.

RUN/PROGRAM MODE

When the programmable controller system is in the RUN/PROGRAM mode the system operates identically to the RUN mode with the added capability of making program changes. The user's program is executed as it is in the RUN mode. The RUN LED on the Parallel Link Driver Module (PLDM) is energized while the keyswitch is in the RUN/PROGRAM mode.

RUN/PROGRAM mode enables the scan loss timer on the PLDM to time out after the time specified by the scan loss timer set point switches on the PLDM has elapsed. The scan loss timer does not time out if an input status scan is executed within the time specified by the scan loss timer set point switches. When a Loader/Terminal requests a program change to be made, the RUN light remains energized, and the scan loss timer remains enabled.

The RUN/PROGRAM mode permits the following functions: element status may be forced by the Loader/Terminal if the force enabled switch (SW2, switch 4) on the PLDM is closed; and preset and accumulated values of timers and counters, sequencer register values, and constant values may be changed by the Loader/Terminal if the data change enable switch (SW2, switch 5) on the PLDM is closed. Augmented RUN Mode Programming is allowed if the on-line programming switch (SW2, switch 6) on the PLDM is closed.

The PLDM switches control the following machine status options in the RUN/PROGRAM mode:

SW2 switch 4	Enable/Disable Force function
SW2 switch 5	Enable/Disable data change function
SW2 switch 6	Enable/Disable on-line programming

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AUGMENTED RUN MODE PROGRAMMING (ARMP)

The capability to make program changes while in the RUN/PROGRAM mode has been refined with the introduction of Augmented RUN Mode Programming (ARMP). This feature allows users to make control program additions and selections while in the RUN/PROGRAM mode with no adverse affect on system operation, other than temporarily increasing scan time (20 ms max.).

ARMP is included with all 620-25 and -35 processors that have a firmware revision of 48 or greater. Earlier firmware versions can be upgraded to ARMP status by ordering upgrade kit 220-007 (compatible with Processor Module 620-0080).

To perform ARMP operations, the 623-51 Loader/Terminal must also be compatible with the ARMP level of firmware. ARMP - compatible loaders have a firmware revision level of E-98 or greater. Earlier versions of the L/T can be upgraded by means of one of the following upgrade kits:

* 223-0007 623-51 Upgrade Kit (English)
* 223-0008 623-51 Upgrade Kit (German)
* 223-0009 623-51 Upgrade Kit (French)
* 223-0010 623-51 Upgrade Kit (Spanish)

The 623-50 L/T is not ARMP compatible and must be updated to a 623-51 by installing one of the following upgrade kits:

* 223-0001 623-50 Upgrade Kit (English)
* 223-0002 623-50 Upgrade Kit (German)
* 22300003 623-50 Upgrade Kit (French)
* 223-0004 623-50 Upgrade Kit (Spanish)

ARMP Programming Changes

Augmented RUN Mode Programming is possible only when the L/T is in the PROGRAM mode, the Processor keyswitch is in the RUN/PROGRAM position, and the processor on-line programming DIP switch is enabled.

Under these conditions, when the L/T is placed in the PROGRAM mode, this message is displayed:

620 IN RUN MODE:
CAUTION: RUN MODE PGM ENABLED

EDITING A LINE - An existing program line can be edited as usual. When the changes are complete, press LINE and ENTER. This message appears:

CAUTION:
RUN MODE PROGRAM SELECTION ENABLED.
DEPRESS LOAD TO EXECUTE/
ANY KEY TO CANCEL

An additional message is displayed during a delete or line enter function:

WARNING:
LOADER IS NOT MONITORING LINE STATUS!
OUTPUT BIT(S) WILL REMAIN IN LAST STATE
IF DELETED OR ADDRESS CHANGED.
DO NOT DEPRESS LOAD IF DANGER EXISTS.
SEE USER MANUAL.

Press LOAD to complete the process. A "busy" message flashes when the line edit function is being executed. When this message disappears, line monitoring resumes.

INSERTING AND LOADING A LINE - A new logic line can be inserted between existing lines (LINE, INSERT) or at the end of the program (LOAD). These operations are similar to the edit line process, except the warning message is not displayed.

DELETING A LINE - The currently displayed line can be deleted from the program by pressing LINE, DELETE, LOAD. The caution and warning messages mentioned before are displayed. Be sure that the line terminator, if it's a coil, is OFF prior to the delete operation to avoid real outputs remaining ON. A Send Out, likewise, should be set to zero.

SEQUENCERS - Sequencers of 80 steps or fewer can be inserted, loaded, or deleted using normal RUN mode methods. Sequencers with more than 80 steps cannot be deleted as a whole. The only way to delete such sequencers is to delete individual steps until there are 80 steps or less, at which time the entire sequencer can be deleted. Multiple step editing of sequencers greater than 80 steps is also prohibited.

To edit a sequencer in the RUN mode, press SHIFT-SEQUENCER (both keys simultaneously), which leads to this menu item:

F5 = Edit Seq.
Program Seq.

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Press the F5 key to toggle between editing the sequencer and programming the line. The difference is this: in edit mode, you only need to enter a value and press the down arrow key to insert, delete or overwrite a sequencer value. In program mode, all sequencer changes are stored until the LINE, ENTER, LOAD or LINE, INSERT, LOAD operations are performed, and the line is entered in program memory.

AUTO ENTER MODE - the L/T, when selected for the Auto-Enter, will not monitor line status. To resume line monitoring, you must exit Auto-Enter and the line is redisplayed by moving up or down one rung.

Programming Rules

When making RUN mode changes, the following rules should be followed:

1. Set the watchdog timer preset to allow for up to 20msec of extra scan time.

2. Care should be taken when performing ARMP operations with subroutines and certain types of NSKR instructions:

   * When adding new subroutines, add the SUB instruction first, then the JSR. Likewise, when adding new jumps, add the EOS first, then the NSKR.

   * When deleting subroutines, delete the JSR first, then the SUB. When deleting jumps, delete the NSKR first, then the EOS.

   * Do not overwrite a SUB or EOS with another SUB or EOS. The old instructions should first be deleted before the new instruction is added.

   * Judge carefully the consequences of adding or deleting sequencer steps. For example, adding a step before the active step makes the sequencer appear to be moving back a step. Deleting a step before the active step makes the sequencer appear to be moving forward a step. The step number register must be adjusted to agree with the new number of steps.

   * If Load or Unload Sequencer instructions are used, care should be taken if the target sequencer is deleted. In this case, the Load/Unload instruction would operate on the next sequencer in the program.

3. If a power loss occurs during a RUN mode programming operation, it could cause a "write in progress" failure. This causes the controller to shut down, and the only way to recover is to reload memory. In most cases a full recovery is possible, however the line being programmed may or may not be changed.

Compatibility Concerns

623-51 loaders with ARMP firmware (Rev E-98 or higher) are compatible with non-ARMP processors except for RUN mode programming operations. The loader will perform the old RUN mode program procedure (i.e. Request Softwware PROGRAM mode, perform the function, then return to RUN mode).

623-51 loaders without ARMP firmware are compatible with ARMP processors except for RUN mode programming operations. In this case, neither ARMP nor present RUN mode programming procedures are available. If a RUN mode operation is attempted, the loader displays the message "Invalid Command".

623-50 loaders with the old RUN mode programming capability are compatible with ARMP processors except for RUN mode programming operations. In this case, the 623-50 will perform the old RUN mode programming procedure (Request software PROGRAM mode, etc.).

DISABLE MODE

The system may be placed into the DISABLE mode by the front panel keyswitch or by the absence of any other mode. If the system does not detect a selected mode, it enters the DISABLE mode by default.

When the system is in the DISABLE mode the processor scans through the user's program, executing the instructions as it would for normal machine control operation. This involves collecting field input status, solving the ladder logic program and posting the outputs in the Output Status Table. As outputs are updated in the Output Status Table, they are sent to the I/O Control Module to update field outputs. At the same time, the hardware on the Parallel Link Driver Module sends a power fail signal to the I/O system. Outputs are cleared or held in the last state in the DISABLE mode, depending on the PIOM or SIOM setting for each rack. The outstrobe for updating the I/O is held disabled, preventing I/O output updating.

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PARALLEL I/O THEORY OF OPERATION

The 621 Parallel I/O System consists of one or more I/O racks connected to the PLDM in the processor rack in a point-to-point (daisy-chain) configuration. Communication takes place over a parallel bus of multiconductor cables connecting the PLDM in the processor rack and the PIOM's in the I/O racks. Bus activity between I/O racks and the PLDM in the processor rack is controlled by the processor through the IOCM andPLDM.

PARALLEL OPERATIONAL SEQUENCE

1. The Input Status Scan (ISS) instruction is automatically inserted in the first word of memory and can also be user programmed at other points in the control program. During ISS the processor momentarily stops solving the control program to update the Input Status Table.

2. During ISS the processor systematically generates I/O module address data which is transmitted to all PIOM's on the parallel channel.

3. The PIOM's decode the address data and in turn generate card selects to all I/O cards in the I/O rack.

4. After an input module receives the card select, the data present at each input is latched on the input module.

5. Immediately after the card select is received, an in-strobe is generated to the module that allows the information to be transmitted to the processor Input Status Table.

6. Each I/O module is successively selected and then strobed. All output modules strobed during input status scan are read as zero or OFF. At this point, output modules are queried for card faults. The processor can store the location of up to eight card faults. The most significant address of the faulted I/O module is stored in the System Status Table.

7. By the end of the Input Status Scan, the status of all inputs is recorded in the Input Status Table. All outputs are recorded as zero or OFF in the Input Status Table.

8. The processor then commences program execution. As output instructions are solved, the processor posts the status of the output module into the output status table.

9. The processor also generates the address data and output status to the I/O system. The PIOM's decode the address information and generate a card select to the appropriate output module.

10. After the output module is selected, a specific output command is sent to the module followed by the outstrobe command that allows the output to turn ON or OFF depending on the output command.

11. The 620-25/35 processor also performs a diagnostic function with every output command. When an output is solved, not only is the address data and output status sent to the I/O system, but also the complement of the output status information. These two groups of data are transmitted to appropriate output modules on separate data lines. At the output module, a comparison between the data and its complement is made. If a miscompare occurs, signifying a module or I/O bus fault, the output module sets a fault flag. This flag is read by the processor during Input Status Scan. The address of the faulted module is then posted in the System Status Table.

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PARALLEL SHUTDOWN

The Parallel I/O System will halt operation under the following conditions:

1. The processor, in the PROGRAM or DISABLE Mode (Scan Loss) sends a power fail signal to all PIOM's located in the I/O racks. The PIOM's upon receiving the power fail, either turn off all outputs or hold outputs in their last state (as selected by PIOM DIP switch settings) until the power fail signal is removed.

2. When any I/O rack power supply detects that the AC supply falls below 85 volts in 115VAC operation or 190 volts in 230VAC operation for a time period greater than 11.5ms, that power supply sends a power fail signal to all other I/O racks as well as to the processor. This causes the PIOM's to clear or freeze outputs and causes the processor to halt operation.

3. When the processor rack Power Supply detects a low AC line voltage. A power fail signal is sent to the I/O system and the processor. The processor halts operations and the PIOM's clear or freeze outputs in their racks.

4. PIOM's can be individually selected to recognize output module faults occurring in their racks. If faults are to be recognized or acted upon, the PIOM will clear or freeze outputs in its rack only.

SERIAL I/O THEORY OF OPERATION

POWER-UP

The remote serial I/O is serviced asynchronously from the processor scan. Each SLM operates as the master for the I/O racks connected to it. The SLM derives its power from the processor rack backplane to ensure orderly power-up and power-down sequences for the SLM and each channel that it operates.

When power is applied to the system, each SLM clears its I/O status tables, serial I/O status table, PUSH/PULL data and card faults. The SLM then queries each SIOM to determine channel addressing. The SLM's read the SIOM input, output, PUSH and PULL data, and determine the selected I/O responses to system mode changes and system faults.

The SLM's and SIOM's also perform a self-diagnostic check at this time. A status ready bit is set in the SLM serial I/O status table when all the input/PULL data has been received from the SIOM's. An SLM will not transmit output data to a SIOM until all input data has been received. When the status ready bit is set, the SLM permits SIOM's to write their I/O data to the SIOM backplanes, commencing normal service of each I/O channel.

NOTE

It is possible for the processor to power up and begin operation before the serial link has finished its configuration process. For this reason it is suggested that the IPC 620 be powered up in the PRGM mode and then switched to the RUN mode once the serial system is operating. Or, two lines of ladder logic can be added as the first lines in the ladder logic program to monitor the input/PULL data ready bits from the serial I/O table. This will cause the program to return to the beginning of program (RBP) if the input/PULL data ready bits have not been set. See serial I/O status table and programming considerations.

SYSTEM OPERATION

The normal sequence of operation of a serial channel is as follows:

1. The SLM output RAM's are continuously updated by the processor during the processor scan.

2. The SLM input RAM's are read by the processor during the input status scan.

3. The SLM services each I/O rack in the order of their addresses on the link by transmitting the rack's output/PUSH data to the SIOM.

4. Each SIOM (non-redundant 621-9940) responds to its message from the SLM by immediately transmitting its rack input/PULL data to the SLM.

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5. The SIOM writes its output/PUSH data to the I/O backplane.

6. The SLM writes the SIOM input/PULL data to its input RAM's.

SERIAL I/O STATUS INFORMATION

SIOM on-line, off-line and link status is continually updated and maintained at the SLM. This serial I/O status information is accessed by using the PULL instruction for addresses 2040 to 2047 in the IPC 620-25/30/35 processor. This feature precludes the use of any PUSH/PULL or discrete I/O card in the I/O slot occupied by addresses 2040 to 2047. The processor must also be a 2K system in order to obtain the serial status information. Table 5 shows register addresses and corresponding bit locations for the available serial status information. A description for the serial I/O status information is as follows:

SIOM Off-Line Flag

This bit is OFF (0) when all SIOM's are on-line. When a SIOM is taken off-line this bit is turned ON (1). The bit remains set until all off-line SIOM's have been brought back on-line or the SLM has been reset or rack power has been cycled.

Input/PULL Data Ready

This bit is used during power-up and switchover to show that each link's input and PULL data has been collected at the SLM or when all of the data has been collected. This bit is ON during normal operation. When the input and PULL data is not available, this bit is OFF. On power-up or when a link is shutdown, causing a switchover, this bit is cleared and remains cleared until all of the data is retrieved.

TABLE 5 - SERIAL I/O STATUS INFORMATION

REGISTER ADDRESS	NUMBER OF BITS	CHANNEL	DESCRIPTION
2040	0 -15	1 -4	Status Bits
	0	1	SIOM Off-Line Flag
	1	1	Input/PULL Data Ready
	2	1	Reserved
	3	1	All SIOM's Active on Redundant Link
	4 - 7	2	Status Bits Channel 2
			See Bits 0 - 3 Channel 1
	8 - 11	3	Status Bits Channel 3
			See Bits 0 - 3 Channel 1
	12 - 15	4	Status Bits Channel 4
			See bits 0 - 3 Channel 1
2041	0 -15	1	Starting Address of SIOM Off-Line
2042	0 -15	2	Starting Address of SIOM Off-Line
2043	0 -15	3	Starting Address of SIOM Off-Line
2044	0 -15	4	Starting Address of SIOM Off-Line
2045	0 -15	1	Number of SIOM's On-Line
2046	0 -15	2	Number of SIOM's On-Line
2047	0 -7	3	Number of SIOM's On-Line
	8 -15	4	Number of SIOM's On-Line

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All SIOM's Active on Redundant Link

This bit is used with redundant processor systems to indicate the status of the backup link. It is ON when all the SIOM's are on-line and communicating on the backup link. It turns OFF when one or more SIOM's drop off-line on the backup side. This bit does not cover SIOM's which are already off-line on the lead port or on both the lead and backup ports. See the Redundancy User Manual (620-8983) for more information.

Starting Address of SIOM Off-Line

This register contains the starting address of the rack for a SIOM which has gone off-line. When more that one SIOM is off-line only the first SIOM to go off-line is posted. When it is brought back on-line, the next off-line SIOM address is reported. This register contains a valid address only when the SIOM off-line flag bit is ON.

Number of SIOM's On-Line

This register contains the number of SIOM's currently on-line.

System Restart/Reset

The IPC 621 remote serial I/O design allows the user to permit (via DIP switch selections) that any drop of a multidrop configuration can be taken off-line (intentionally or unintentionally) without interrupting the operation of the remaining drops on the serial link. Several restart options are available to restart a drop that has been taken off-line.

The serial I/O system can be restarted by cycling power at the processor or by shorting the reset terminals on the SLM. Either of these actions will cause the SLM to perform a power-up procedure including self-test and link configuration.

The user may elect to only restart an off-line drop by one of the following methods:

* Shorting the SLM restart terminals starting all off-line SIOM's. Communication with on-line links will continue uninterrupted.

* Start the off-line SIOM only by shorting its reset terminals.

* Start the off-line SIOM only by cycling the SIOM power. It could take several seconds before the SIOM is brought on-line, depending on when during the serial I/O scan a rack (SIOM) is restarted.

If the entire serial I/O system is shutdown, the recommended reset procedure is to cycle processor power or short the SLM reset terminals. Either of these methods will initiate the self-diagnostic start-up routines. This ensures a complete system reset.

System Fault Detection

The IPC 621 serial I/O system employs several on-line fault routines to ensure proper link operation. These routines are performed after all SLM's and SIOM's have successfully passed their self-diagnostic tests. Refer to Table 9 and 10 for user selectable fault responses.

Each SIOM (in conjunction with any output modules housed in the I/O rack) diagnose I/O rack backplane output card faults or bus faults. The SIOM transmits the fault information to the SLM. The SLM enters the most significant I/O card address for the faulted address into the I/O card fault table. The user can elect to clear or freeze I/O at the rack (through DIP switch settings) if a card fault occurs.

Each message transmitted by an SLM or SIOM contains a Cyclic Redundancy Check Character(CRCC) to ensure transmission validity. If an error is detected in the message initiated by the SLM the following actions take place:

* The SIOM aborts its response to the SLM.

* The SLM recognizes the SIOM failure to respond and re-sends the message to the SIOM.

* If the re-sent SLM message is accepted, the SIOM responds with a new input and PULL data message.

* If the re-sent SLM response contains an error, the SIOM again aborts its response to the SLM. The SLM ceases communication with the affected SIOM and sends a message to the next SIOM on the link. The affected SIOM takes itself off-line and its input/PULL data is cleared from the SLM status table. The SLM link fault will illuminate.

Once SLM/SIOM communication has been established, if an SLM does not receive a message from a polled SIOM in the allotted time period, the SLM will time-out. If the CRCC comparison reveals an error in a SIOM transmitted message, or the SLM times-out, the following responses occur:

* The SLM will re-send the message to the SIOM.

* The SIOM will respond to the retry message by transmitting its input and PULL data message.

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* If the SIOM response is accepted by the SLM, the SLM proceeds to send the next message to the next SIOM on the link.

* If the second response contains an error, or the SLM times-out a second time, the SLM ceases communication with the affected SIOM and sends a message to the next SIOM on the link. The affected SIOM takes itself off-line, and its input/ PULL data is cleared from the SLM status table. The SLM fault LED will illuminate.

For data communication errors the SLM immediately attempts to retry communications with the affected SIOM as explained above. If the data communications to or from a SIOM is corrupted on both the initial and retry communication attempts, the associated SIOM is shut down. Depending on the number of racks (SIOM's) per link, the following number of retries are permitted per each I/O scan before the link is shut down:

NUMBER OF RACKS	ALLOWABLE RETRIES
1	1
2	2
3 - 16	2

Programming Considerations

* The serial I/O scan is asynchronous to the processor scan.

* Send Outs to real serial I/O addresses must be on a 16-point I/O address boundary (i.e. 15, 31, 47, etc.)

* Serial I/O status information is available from addresses 2040 - 2047. The information can be used in the following ways:

1. Input/PULL data ready bit can be used on powerup to ensure the ladder logic program does not begin execution until the serial I/O system has been configured and is operating. This can be done with the lines of logic in Figure 16.

2. The SIOM off-line flag can be used as an alarm to indicate a SIOM (rack) has gone off-line. Once this bit is set the address of the off-line SIOM can be determined from registers 2041 - 2044.

3. Registers 2045 - 2047 indicate the number of SIOM's on-line. This can be used to indicate the number of on-line and off-line SIOM's. Only one address is posted in the starting address of the SIOM off-line register. It is possible to determine the number of SIOM's off-line by comparing the number of racks on each link with the number posted in the Number of SIOM's On-line Register.

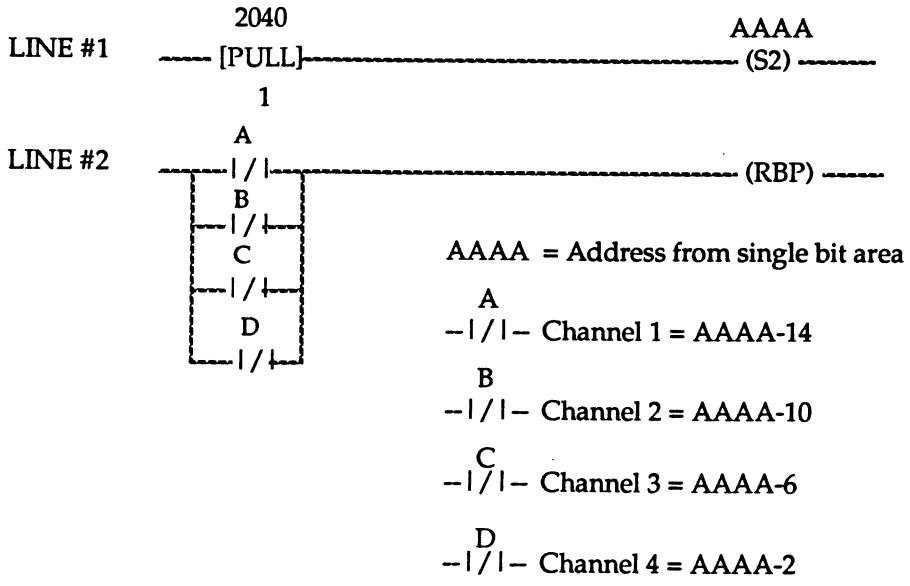


FIGURE 16 - LADDER LOGIC FOR INPUT/PULL DATA READY

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DIAGNOSTICS

The 620-25/35 self-diagnostics enable the user to locate system faults at the module level. LED indicators alert the user if system faults occur and direct the maintenance person to fault locations. Most system faults can be repaired by replacing a single module.

The self-diagnostic tests are conducted in a series beginning with the Processor Module, which is the core of the system, and proceeds through the processor backplane, other processor modules, the I/O bus, individual I/O racks, and individual I/O modules. The Processor Module thoroughly tests itself before proceeding with the self-diagnostics to assure the validity of the testing. The PM executes functional and comprehensive memory location tests. The functional test assures that hardware paths, control functions and system registers are operational. The memory location test ensures the ability of the memory to receive and retain stored information.

The diagnostics discussion is broken into three categories: power-up diagnostics, on-line diagnostics, and monitoring diagnostics with the Loader/Terminal.

SYSTEM POWER-UP SELF-TEST

The Processor Module (PM) begins executing the self-diagnostic test program stored in the executive ROM. The red LED labeled TESTING energizes, indicating the initiation of diagnostic testing. This LED remains energized until the diagnostic testing procedure is complete.

1. Test data flow through microprocessor and operation of microprocessor register.
2. Compute checksum of executive ROM.
3. Test read/write ability of processor module working memory.
4. Test bus operation.
5. Test program memory address register on system control module (SCM).
6. Test processor module control and contact data flow in register module.
7. Test control logic unit (CLU) on system control module (SCM).
8. Test address register on memory module (MM) and data flow through MM.
9. Test register data flow through the register module.
10. Test single bit output transmission on the input/output control module (IOCM).
11. Test sendout output status transmission on IOCM.
12. Test IOCM and parallel link driver module (PLDM) for correct system configuration.
13. Test system mode. The system mode keyswitch is examined. The diagnostic tests continue with test 14 if the keyswitch is in PROGRAM. The diagnostic tests end if the keyswitch is in the RUN, RUN/PROGRAM or DISABLE mode. The results of the diagnostic tests are stored in the System Status Table.
14. Test memory module and register module. Comprehensive test of every location in the MM and RM. Processor executes a series of read, write, complement procedures comparing the data stored in every memory and register location. The results of the diagnostic tests are stored in the System Status Table.

PROGRAM MEMORY CHECK

The user program memory integrity is checked through a comparison of checksum calculations. If any on-line changes occur, the initial checksum is recalculated. This is valid for Processor Module 620-0080 with Firmware Revision 50 (V.R. 2.2). The checksum calculation and comparison check occurs in the 620-0080 processors with Firmware Revision 50 (V.R. 2.2) as follows:

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1. The processor calculates the initial checksum of the user program during the retentive scan.

2. The processor calculates a second checksum of user program while program is running by reading six memory words per scan. If any on-line changes occur, flag bits are set to cause the processor to start over by recalculating the initial checksum.

3. If the two checksum calculations match the process starts over since no error has been detected.

4. If the two checksum calculations do not match, the processor sets the error flag (refer to Table 5) and is forced to the PROGRAM mode. The Loader/ Terminal will display a PC Diagnostics Fail message. The recovery procedure for a checksum error is to reload program memory. The 623-51 will display "program checksum error" when the processor is placed in PRGM mode.

Table 6 describes the function of System Status Table registers involved in the checksum calculation and comparison procedure.

ON-LINE CHECKS

On-line checks are functional tests performed before contacts are collected at the beginning of every scan. These tests are abbreviated versions of the diagnostics performed at system power-up:

1. Check processor backplane
2. Check System Control Module
3. Check main memory
4. Check integrity of Memory Module
5. Check Contact Logic Unit on System Control Module
6. Check Parallel Link Driver Module
7. Check program checksum

The processor immediately goes into self-diagnostics if any of these tests are unsuccessful.

I/O SYSTEM TEST

The 620-25/35 processor also performs a diagnostic function with every output command. Output modules have diagnostic circuitry that receives data over two different routes on the data bus. When an output is solved, not only is the address data and output status sent to the I/O system, but also the complement of this information. These two groups of data are transmitted to appropriate output modules on separate data lines. At the output module, a comparison between the data and its complement is made. If a miscompare occurs, signifying a module or I/O bus fault, the output module sets a fault flag. This flag is read by the processor during Input Status Scan. The address of the faulted module is then posted in the System Status Table. The output module data fault LED energizes if a miscompare is detected.

MONITORING DIAGNOSTICS

The 623-51 Loader/Terminal allows the user to examine the results of the processor diagnostics. Programmable Controller hardware and software status may be accessed and monitored using the Loader/Terminal CRT. Descriptions of the CRT displays follow.

1. The HARDWARE STATUS display provides the user with data concerning various programmable controller DIP switch settings and other processor information.

2. The second display is SELF-TEST, which indicates pass/fail status of the individual hardware elements involved in the self-test routine.

3. The I/O MODULE STATUS display offers the total I/O module faults at any given time and lists the most significant addresses of eight modules at fault. The displayed faults are cleared and additional faults are displayed if more than eight faults occur at one time.

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TABLE 6 - FUNCTIONS OF CHECKSUM REGISTERS

REGISTER	CONTENT	FUNCTION
2395	Checksum (MSB)	These registers store the calculated user program memory checksum.
2394	Checksum (LSB)	
2393	Checksum	The most significant bit (MSB) is 0 when no error is detected. The MSB is 1 when an error is detected.
2392	0	Not used.
2391	Initial Flag	System use only.
2390	Initial Pass	The most significant bit (MSB) is 0 when the initial checksum is being calculated. The MSB is 1 when the checksum is complete.

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APPENDIX A

DIP SWITCH SETTINGS

TABLE 7 - PLDM (620-0086) SWITCH SETTINGS

SWITCH	STATE	FUNCTION
SW1		
1	CLOSED/ON	Disables processor scan loss function
	OPEN/OFF *	Enables processor scan loss function
2	CLOSED/ON *	Adds 20ms
	OPEN/OFF	Adds 0ms
3	CLOSED/ON *	Add 40ms — Set to minimum value in excess of processor scan time.
	OPEN/OFF	Add 0ms
4	CLOSED/ON *	Add 80ms
	OPEN/OFF	Add 0ms
SW2		
1**	CLOSED/ON *	Disables processor I/O. Zero starting address located in I/O rack.
	OPEN/OFF	Enables processor I/O. Zero starting address located in processor rack.
2**	CLOSED/ON	Processor set for 16-point operation.
	OPEN/OFF *	Processor set for 8-point operation.
3	CLOSED/ON	I/O racks clear or freeze outputs according to PIOM or SIOM freeze/clear setting when the Software PROGRAM mode is used.
	OPEN/OFF	When in the Software PROGRAM mode, all outputs remain in their last state regardless of PIOM or SIOM freeze/clear setting.
4	CLOSED/ON *	Enables FORCE function.
	OPEN/OFF	Disables FORCE function.
5	CLOSED/ON *	Enables following data changes in RUN mode: timer/counter preset and accumulated values; sequencer register values; and constant values.
	OPEN/OFF	Disables the above data changes in the RUN mode.
6	CLOSED/ON *	Enables on-line programming in RUN/PROG mode.
	OPEN/OFF	Disables on-line programming in RUN/PROG mode.
7	---	Not used.

* Factory Setting

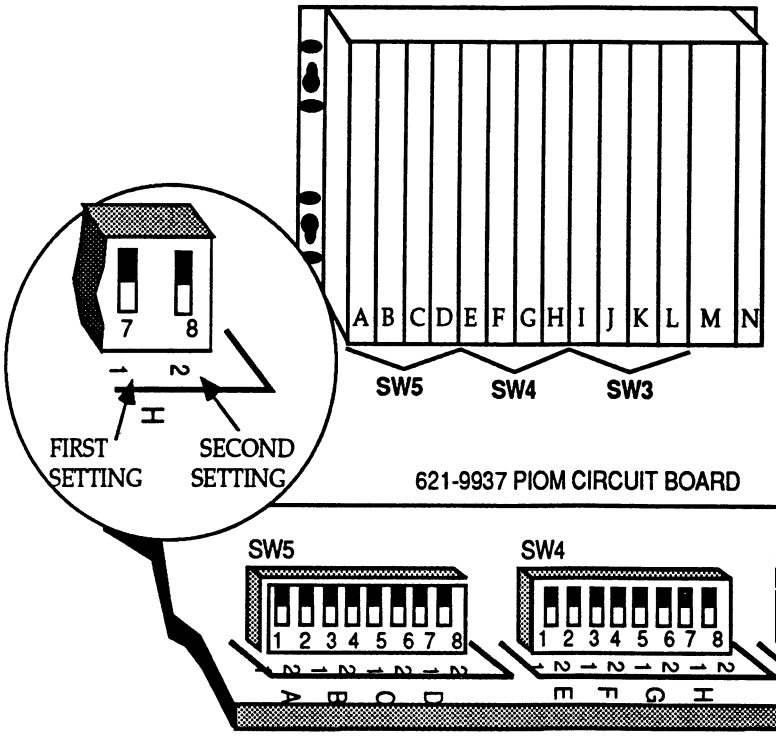
** SW2 switches 1 and 2 apply only to the 620-25 Processor, since the 620-35 Processor rack does not have I/O slots. When using the 620-35 Processor, set SW2, switch 1 CLOSED/ON.

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TABLE 8 - PIOM (621-9937) SWITCH SETTINGS

SWITCH	POSITION	STATE	SWITCH VALUE	
SW1	1	Closed/ON	8	Determines starting address for the parallel I/O rack (e.g. closing positions 2, 4, and 6 yields a starting address of 16+64+256=336)
		Open/OFF*	0	
	2	Closed/ON	16	
		Open/OFF*	0	
	3	Closed/ON	32	
		Open/OFF*	0	
	4	Closed/ON	64	
		Open/OFF*	0	
	5	Closed/ON	128	
		Open/OFF*	0	
	6	Closed/ON	256	
		Open/OFF*	0	
	7	Closed/ON	512	
		Open/OFF*	0	
	8	Closed/ON	1024	
		Open/OFF*	0	
SW2	1	Closed/ON*	Clear outputs with 1) switch 2 closed and I/O fault occurs, 2) external cable disconnect, 3) external power failure, 4) processor in PROGRAM or DISABLE modes	
		Open/OFF	Outputs remain the same; with the above conditions	
	2	Closed/ON	Recognize an output module fault	
		Open/OFF*	Ignore an output module fault	
	3	Not used		
	4	Not used		

* Factory setting



SLOT CONFIGURATION SELECTION

MODULE TYPE	SETTING	
	FIRST	SECOND
0-Point	Closed/ON	Closed/ON
8-Point	Open/OFF	Closed/ON
16-Point	Closed/ON	Open/OFF
32-Point*	Open/OFF	Open/OFF

*Factory Setting for all switches

Example:

Slot C with a 16-point module
SW5, position 5 - ON
SW5, position 6 - OFF
Slot G with an 8-point module
SW4, position 5 - OFF
SW4, position 6 - ON

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TABLE 9 - SLM (621-9939) SWITCH SETTINGS

SWITCH STATE		FUNCTION
1 and 3	2 and 4	(SHUTDOWN RESPONSE)
Open/OFF*	Open/OFF*	Channel continues to operate if a channel fault occurs**
Closed/ON	Closed/ON	Channel ceases operation if a channel fault occurs**
Open/OFF	Closed/ON	Both channels on SLM cease operation if a channel fault occurs**
Closed/ON	Open/OFF	Both SLM channels shutdown plus CLROL line on I/O bus is set - resetting parallel I/O and causing a second SLM (if present) to have its corresponding SIOM's clear or freeze their data depending on SIOM DIP switch settings**

SWITCH	STATE	FUNCTION
5	Closed/ON	Service one PUSH/PULL card per I/O rack each scan
	Open/OFF*	Service all PUSH/PULL cards per I/O rack each scan
6	Closed/ON	Identify SLM as #2 in rack
	Open/OFF*	Identify SLM as #1 in rack (must select if only one SLM in rack)
7	Closed/ON	Redundant serial I/O system
	Open/OFF*	Non-redundant serial I/O system
8	Closed/ON	Auto-test enabled
	Open/OFF*	Auto-test disabled (normal operation)

* Factory setting

** A channel fault is defined as a SIOM being taken off-line for any of the following reasons:

1) power failure
2) serial link timeout
3) two consecutive serial data receive errors

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TABLE 10 - SIOM'S (621-9938, 621-9940) SWITCH SETTINGS

SW1 SWITCH STATE	SWITCH							
	1	2	3	4	5	6	7	8
	SWITCH ADDRESS VALUE							
Open/ OFF *	0	0	0	0	0	0	0	0
Closed/ ON	8	16	32	64	128	256	512	1024

SW2 SWITCH	STATE	FUNCTION
1	Closed/ON *	Clear outputs and PUSH data with 1) SW2 switch 2 closed and I/O fault occurence 2) loss of SLM communications 3) external power failure 4) processor in PRG or DISABLE mode (CLROL low)
	Open/OFF	Freeze outputs and PUSH data with conditions above
2	Closed/ON	Recognize I/O card fault and respond according to SW2 switch 1 setting
	Open/OFF *	Ignore an output module fault
3		Not Used
4	Closed/ON	Auto-test
	Open/OFF *	Normal Operation

CONTROLLING SWITCH			SELECTION SWITCH	NUMBER OF I/O POINTS PER SLOT			
SW5	SW4	SW3		0	8	16	32 *
I/O SLOT				SWITCH STATE			
D	H	L	1 (2)	Closed/ON	Closed/ON	Open/OFF	Open/OFF
			2 (1)	Closed/ON	Open/OFF	Closed/ON	Open/OFF
C	G	K	3 (2)	Closed/ON	Closed/ON	Open/OFF	Open/OFF
			4 (1)	Closed/ON	Open/OFF	Closed/ON	Open/OFF
B	F	J	5 (2)	Closed/ON	Closed/ON	Open/OFF	Open/OFF
			6 (1)	Closed/ON	Open/OFF	Closed/ON	Open/OFF
A	E	I	7 (2)	Closed/ON	Closed/ON	Open/OFF	Open/OFF
			8 (1)	Closed/ON	Open/OFF	Closed/ON	Open/OFF

* Factory Setting

Switch selection in parentheses denotes the silkscreen labelling on the SIOM pc board.

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FRONT PANEL LED'S

The operating states of the SLM and the SIOM's can be determined from the status of the front panel LED's. These states are shown in Tables 11 and 12.

TABLE 11 - OPERATING STATES SHOWN BY SLM LED'S

MODULE STATE		LED STATE		
DEFINITION		PASS	LINK FAULT	ACTIVE
1	Power Up/Reset	OFF	ON	OFF
2	Self-test - The SLM is performing the self-test.			
3	Configure Link- The SLM is establishing communications with ready SIOM's.	ON	OFF	ON
4	Normal Operation - The serial link is working.			
5	Link Fault - A fault has occurred on the serial link. It is necessary to restart or reset to return to state 4.		ON	ON - The link is still operating. OFF - The link is not operating.

TABLE 12 - OPERATING STATES SHOWN BY SIOM LED'S

MODULE STATE		LED STATE			
DEFINITION		PASS	LEAD	RACK FAULT	ACTIVE
1	Power-Up/Reset	OFF	ON	ON	OFF
2	Self-test - The SIOM is performing self-test.				
3	Configure Link - The SIOM is waiting to establish communications with the SLM.	ON	OFF	OFF	
4	Normal Operation - The serial link is working.		ON - Lead port OFF - Back-up port		ON
5	Rack Fault - A card fault has occurred in this rack. Cycle power or reset to return to state 4.			ON	ON - The link is still operating. OFF - The link is not operating.
6	Link Fault - A fault has occurred on the serial link. Restart or reset at the SLM to return to state 4.		OFF	ON - Rack fault Off - No rack fault	OFF

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SYSTEM STATUS TABLE

The System Status Table consists of memory locations 8 bits wide. It stores processor system diagnostic information. This information is accessed through the Loader/Terminal by using a four-digit decimal address and a PULL instruction in the control program. The three categories of information stored in the System Status Table are: System Diagnostics, System Hardware Status, and System Identification.

The most useful four-digit decimal addresses and register contents are:

DECIMAL ADDRESS	REGISTER CONTENTS
2413	Scan Loss/Battery
2415	Card Fault Count
2417	Card Fault Address 7
2419	Card Fault Address 6
2421	Card Fault Address 5
2423	Card Fault Address 4
2425	Card Fault Address 3
2427	Card Fault Address 2
2429	Card Fault Address 1
2431	Card Fault Address 0
2287	Software Request for Program
2291	Scan Time
2297	Memory Used
2299	Memory Size

OPCODES

The opcode for each instruction in the 620-25/35 system is listed in Table 13. Bits 0 - 15 contain the instruction address where it is required. Bits 20 and 21 are history bits used to indicate forced status or previous scan status where required.

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TABLE 13 - OPCODES FOR 620-25/35 INSTRUCTIONS

INSTRUCTION	BITS								EXECUTION (microseconds)	
	23	22	21	20	19	18	17	16	MIN.	MAX.
Normally Open Contact	1	1	Force		1	0	0	0	1.83	1.83
Normally Closed Contact	1	1	Force		1	1	0	0	1.83	1.83
Transition ON Contact	0	1	Force		0	0	1	1	9.80	14.80
Transition OFF Contact	0	1	Force		1	0	1	1	9.80	14.80
Branch (three internal instru)										
Down Branch	1	1	0	0	0	0	0	1	1.83	1.83
Double-Down Branch	1	1	0	0	0	0	1	0	1.83	1.83
Up Branch	1	1	0	0	0	0	1	0	1.83	1.83
Output	1	1	Force		0	1	0	0	4.27	6.10
Retentive Output	1	1	Force		0	1	0	1	4.27	6.10
Latch Output	1	1	Force		0	1	1	0	4.27	6.10
Unlatch Output	1	1	Force		0	1	1	1	4.27	6.10
ON Delay timer										
Word 1: (.01 sec)	0	1	1	0	1	0	0	0	39.04	51.24
(.1 sec)	0	1	1	0	1	0	0	1	27.45	32.23
(1 sec)	0	1	1	0	1	0	1	0	27.45	37.21
Word 2:	1	1	Force		0	1	0	0	4.27	6.10
OFF Delay Timer										
Word 1: (.01 sec)	0	1	1	0	0	0	0	0	43.31	62.83
(.1 sec)	0	1	1	0	0	0	0	1	29.28	41.48
(1 sec)	0	1	1	0	0	0	1	0	29.28	41.48
Word 2:	1	1	Force		0	1	0	0	4.27	6.10
Retentive ON Delay Timer										
(.1 sec)	0	1	1	0	1	1	0	1	23.79	35.38
(1 sec)	0	1	1	0	1	1	0	0	23.79	35.38
Up/Down Counter	0	1	1	1	1	1	1	1	34.50	51.50
Not Skip and Retain	0	1	Force		0	1	1	0	21.90	31.72
Not Skip and De-energize	0	1	Force		0	1	1	1	10.40	24.00
End Of Skip	0	0	1	1	0	1	0	0	3.00	15.00
Jump	0	1	Force		0	1	1	0	(B)	(B)
Return to Beginning of Program	0	0	Force		0	1	0	1	3.60	5.20
Bring In	1	0	0	0	1	0	0	0	12.70	16.00
Send Out (Registers)	0	0	Force		0	1	1	1	15.00	15.00
Send Out (Control)	0	0	Force		0	1	1	1	18.00	86.00 (C)

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TABLE 13 - OPCODES FOR 620-25/35 INSTRUCTIONS (CONT.)

INSTRUCTION	BITS								EXECUTION (microseconds)	
	23	22	21	20	19	18	17	16	MIN.	MAX.
Pull From I/O	1	0	0	0	0	0	0	0	(A)	(A)
Pull From Status Table	1	0	0	0	0	0	0	1	(A)	(A)
Pull From Registers	1	0	0	0	0	0	1	0	(A)	(A)
Push To I/O	1	0	0	0	0	1	0	0	(A)	(A)
Push To Registers	1	0	0	0	0	1	1	0	(A)	(A)
Constant	1	0	0	0	1	0	1	1	11.60	11.60
Addition	0	0	0	0	1	1	1	0	25.45	25.45
Subtraction	0	0	0	0	1	1	0	1	27.45	27.45
Multiplication	0	0	0	0	1	1	0	0	34.43	34.43
Division	0	0	0	0	1	0	1	1	43.45	43.45
Equality Comparison	0	0	0	0	1	0	0	0	14.45	16.45
Less Than Comparison	0	0	0	0	1	0	0	1	15.45	16.45
Greater Than Comparison	0	0	0	0	1	0	1	0	14.45	16.45
Test For Zero	1	0	Force		1	1	0	1	11.50	17.25
Sequencer									55.00	55.00
Word 1	1	0	0	0	1	0	1	0	---	---
Word 2	1	0	0	0	1	1	0	0	---	---
Word 3	1	0	0	0	1	0	1	1	---	---
Control Output Addr.	0	0	0	0	0	1	1	1	15.00	86.00
Load Sequencer	0	1	0	0	0	1	0	0	3.60	55.00
Unload Sequencer	0	1	0	0	0	1	0	1	3.60	89.00
Input Status Scan	1	0	0	0	1	1	1	1	(D)	(D)
Indirect Bring In	1	0	0	0	1	0	0	1	13.51	23.00
Indirect Sendout Register	0	0	0	0	0	1	1	0	16.00	86.00 (C)
Control	0	0	0	0	0	1	1	0	20.00	89.00 (C)
Jump To Subroutine (JSR)	0	0	0	0	0	1	0	0	19.60	67.00
Subroutine (SUB)	0	0	1	0	0	1	0	0	3.10	11.60
Return To Subroutine (RTS)	0	0	0	1	0	1	0	0	3.10	37.50

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TABLE 13 - OPCODES FOR 620-25/35 INSTRUCTIONS (CONT.)

INSTRUCTION	BITS								EXECUTION (microseconds)	
	23	22	21	20	19	18	17	16	MIN.	MAX.
Matrix									See individual operator times	
Operator	1	0	1	0	1	1	1	0		
Size	1	0	0	0	1	0	0	0		
Source Matrix	1	0	0	0	1	0	0	0		
Reference Matrix	1	0	0	1	1	1	1	0		
Destination Matrix	1	0	1	1	1	1	1	0		
INSTRUCTION	BITS								MIN.	MAX.
	7	6	5	4	3	2	1	0		
Matrix Operations of 8 (real I/O)										
Move	0	0	0	0	0	0	0	0	14.00	980.00
Invert	0	0	0	0	0	0	1	0	14.00	1000.00
Or	0	0	0	0	0	1	0	0	14.00	1170.00
And	0	0	0	0	0	1	1	0	14.00	1170.00
Exclusive Or	0	0	0	0	1	0	0	0	14.00	1170.00
Set 0	0	0	0	0	1	0	1	0	14.00	810.00
Set 1`	0	0	0	0	1	0	1	0	14.00	810.00
Compare	0	0	0	0	1	0	1	1	14.00	1240.00

A.

PULL I/O	1 word = 57.00 + 27.5/additional word
PULL Register	1 word = 27.57 + 9.60/additional word
PULL Status	1 word = 32.50 + 15.00/additional word
PUSH I/O	1 word = 48.00 + 21.00/additional word
PUSH Register	1 word = 36.00 + 13.00/additional word

B. 44.00 microseconds when NSKR is enabled
9.60 microseconds when NSKR is disabled
43.50 microseconds when EOS is enabled
12.00 microseconds when EOS is disabled

C. Maximum time for consecutive sendouts. Minimum time is acheived when logic execution time, after sendout and before next line terminator, equals the difference between minimum and maximum time.

D. 512 I/O -- 771.00 microseconds
1024 I/O -- 1.2 milliseconds
2048 I/O -- 2.06 milliseconds

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INSTRUCTION SET

The 620-25/35 Processor provides a powerful instruction set including math functions. A brief definition of the instructions follows.

RELAY LOGIC INSTRUCTIONS

Normally Open Contact - Examines an input for an ON condition; examines an output for an energized condition.

Normally Closed Contact - Examines an input for an OFF condition; examines an output for a de-energized condition.

Transition On Contact - Acts as a one-shot; ON for one scan when its address energizes and OFF thereafter.

Transition Off Contact - Acts as a one-shot; ON for one scan when its address de-energizes and OFF thereafter.

Branch - Creates parallel branch circuits in a logic line.

Output - Energizes when preceding ladder logic is true.

Retentive Output - Logic status is retained ON or OFF when power is removed. At program power-up all retentive outputs assume their last state before the power-down.

Latch Output - Energizes when preceding logic is true and remains energized regardless of logic changes. Must be unlatched to be de-energized.

Unlatch Output - De-energizes a latch output with an identical address when preceding logic is true. Remains unlatched regardless of logic changes.

TIMER AND COUNTER INSTRUCTIONS

All timer instructions increment from zero towards the preset value.

On Delay Timers (.01, .1, 1 second) - Begin to time when the preceding logic is true. The output turns ON when the accumulated value equals the preset value. Timer is reset to zero when the preceding logic is false.

Off Delay Timers (.01, .1, 1 second) - Begin to time when preceding logic is false. The output turns OFF when the accumulated value equals preset.

Retentive On Delay Timer (.1 and 1 second) - Separate timer RUN and RESET inputs. When the RUN input is false, the timer will not run and the accumulated value is retained. When the RESET input is false, the timer is reset.

Up/Down Counter - Counts from - 65535 to + 65535 transferring an ON signal to the output status table and I/O system when the accumulated value equals the preset value.

SKIP INSTRUCTIONS

Not Skip and Retain - When preceding logic is false, all following logic line terminators are skipped, retaining their terminators present status, until a matching End of Skip instruction is encountered.

Not Skip and De-energize - When preceding logic is false, all following logic line terminators are skipped and their terminators de-energized until an End of Skip instruction is encountered.

End of Skip - Marks the point where memory scan terminates skipping and resumes executing lines following Not Skip and Retain or Not Skip and De-energize instructions.

Jump - When preceding logic is false, all following logic is jumped and not executed until a matching end of jump instruction is encountered.

Return To Beginning of Program - Instructs program scan to return to the beginning of the program.

DATA MANIPULATION INSTRUCTIONS

Bring In - Transfers 16 bits of data from the I/O Status Table or 16 bits plus sign bit from the Register Table, to the processor for use within the logic line.

Send Out - Transfers 16 bits of data from the preceding instructions to the I/O system and the Output status or 16 bits plus sign bit to the Register Table.

Pull - Transfers multiple 16-bit groups of data from the I/O modules (with PUSH/PULL capability) or the Register Table, to the processor.

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Push - Transfers multiple 16-bit groups of data from preceding logic to I/O modules (with PUSH/PULL capability), or to the Register Table.

Indirect Bring In - Transfers 16 bits of data from the address pointed to by the Indirect Bring In address in the I/O Status or Register Table. Allows multiplexing of input data.

Indirect Send Out - Transfers 16 bits of data from the preceding data instructions, to an address pointed to by the Indirect Send Out address. Allows multiplexing of data.

Constant - Transfers a number between 0 and 65,535 from the user memory to the processor.

ARITHMETIC INSTRUCTIONS

Addition - adds two 16-bit signed numbers.

Subtraction - Subtracts two 16-bit signed numbers.

Multiplication - Multiplies two 16-bit signed numbers.

Division - Divides a 32-bit signed dividend by a 16-bit signed divisor to yield a 16-bit signed quotient and a 16-bit remainder.

Equality Comparison - Compares for equality between two signed data values.

Less Than Comparison - Compares for less-than condition between signed data values.

Greater Than Comparison - Compares for greater-than condition between signed data values.

Test For Zero - Processor tests specify Register or 15 consecutive I/O status table locations for a zero condition. If a zero condition is detected, the contact will be ON.

SEQUENCER INSTRUCTIONS

Sequencer - allows processor to store up to 1024 16-bit groups of user-defined data in main memory. The data may be used to control repetitive operations or for bulk data storage.

Load Sequencer - Allows data to be transferred to sequencer tables.

Unload Sequencer - Allows data to be transferred from sequencer tables before the sequencer table is executed.

MATRIX INSTRUCTIONS

Move - Transfers data stored in a specified area of the I/O Status Table or Register Table to another area.

Invert - Inverts and transfers data stored in a specified area of the I/O Status Table or Register Table to another area.

Set Zero - Sets every bit of a matrix to zero.

Set One - Sets every bit of a matrix to one.

Or - Performs an OR of the contents of two matrices and transfers the results to a third matrix.

Exclusive Or - Performs an Exclusive OR of the contents of two matrices and transfers the result to a third matrix.

And - Adds the contents of two matrices and transfers the result to a third matrix.

Compare - Compares two matrices for equality and stores the addresses of miscompares in a third matrix.

SUBROUTINE INSTRUCTIONS

Subroutine - Allows the processor to execute defined portions of the program on command.

Jump to Subroutine - Causes the processor to jump immediately to an identified subroutine in the program and begin executing the subroutine program.

Return from Subroutine - Identifies the end of a subroutine.

MISCELLANEOUS INSTRUCTIONS

Input Status Scan - Temporarily suspends program execution in order to allow the Input Status Table to be updated.

No Operation - A place-holding instruction that facilitates on-line program changes.

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APPENDIX

SUPERSEDED COMPONENTS

Appendix B contains information on 620-25/35 System components which have been superseded by other components. Those components are covered in the main content of the manual. The superseded components may still be used in some applications and are covered in this Appendix.

MODULE/SYSTEM COMPATIBILITY

Table 18 lists the following information:

1. the modules compatible with the processor systems - 620-20, 620-30 620-25, and 620-35,
2. the processor racks with which the modules are compatible, and
3. information on module replacement.

MEMORY MODULES (MM)

Model No. 620-0020 (2K)
Model No. 620-0021 (4K)
Model No. 620-0022 (8K)

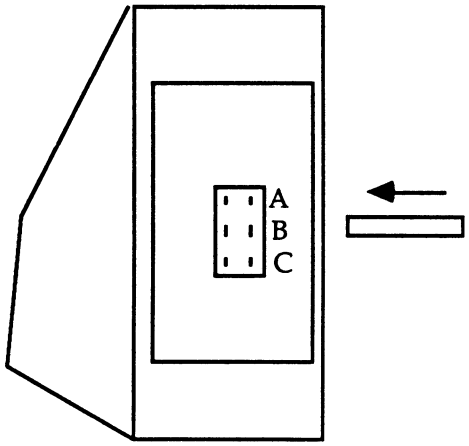
The Memory Module stores the user control program. The green status LED labeled PASS, located on the front of the module energizes after successful completion of the module self-test. The memory module is positioned in cardrack slot C in the 620-25 and slot E of the 620-35.

Two additional Memory Modules can be inserted in option slots A or B in the 620-25 or A - D in the 620-35. The total memory capacity is divided into three 8K segments. Each memory segment must contain 8K before another MM is added, to ensure complete memory scan during operation. A four position shorting board extends from the lower portion of the module front. The position of the shorting board sets the starting address for the Memory Module. See Table 14 for Memory Module configurations and shorting board positions.

TABLE 14 - MEMORY MODULE CONFIGURATIONS (620-0020, -0021, -0022)

SYSTEM MEMORY SIZE	MODULE LOCATIONS			
	E	D	C	B
2K	2K	--	--	--
4K	4K	--	--	--
8K	8K	--	--	--
10K	8K	2K	--	--
12K	8K	4K	--	--
16K	8K	8K	--	--
18K	8K	8K	2K	--
20K	8K	8K	4K	--
24K	8K	8K	8K	--
32K	8K	8K	8K	8K
SHORTING BOARD POSITION	A	B	C	D

SHORTING BOARD



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PARALLEL LINK DRIVER MODULE
Model No. 620-0033

This module has been replaced by the 620-0086. The two modules are the same physically and functionally.

COMMUNICATIONS INTERFACE MODULE (CIM)
Model No. 620-0042

The 620-0042 has been replaced by the 620-0048.

I/O RACK POWER SUPPLY MODULE (5A, 115/230VAC)
Model No. 621-9931

The 621-9931 provides 5.0 amps of +5VDC power for each I/O rack. This module also provides 500mA of ±15VDC power for the operation of analog I/O modules. The PSM is selectable for 115/230VAC operation 47-63 Hz. The yellow shorting board located inside the side cover at the top rear edge of the PSM selects the AC voltage.

The 621-9931 has a fused AC input line. A terminal block at the top of the module frontplate is labeled A (Line or L1), B (Common or L2), and GND for AC input wiring termination. A green LED indicates 5VDC output from the power supply. The front-accessible fuse holder houses a 1.25 Amp SLO-BLO fuse for 230VAC is also shipped with the module. The fuse rating is printed beneath the fuse housing. The I/O rack power supply is installed in slot H of the full rack and slot G of the half rack.

PARALLEL INPUT/OUTPUT MODULE (PIOM)
Model No. 621-9930

The PIOM is located in slot N of the full I/O rack or slot H of the I/O half rack. This module acts as the interface to the processor Parallel Link Driver Module and to other PIOMs. The PIOM has two 50-pin, D-type connectors. The male plug (top) is the IN port and the female plug (bottom) is the OUT port. The green LED, labeled ACTIVE, indicates proper communication from a preceding rack.

Two DIP switch banks located on the pc board are labeled SW1 and SW2. SW1 (switches 1 through 8) selects the I/O rack starting address. Closing a switch (ON) adds that switch position value to the starting address. SW2 (switches 1 through 4) selects rack configuration (all 8-pt. or 16-pt. I/O) and output handling.

Table 15 shows PIOM (621-9930) DIP switch settings.

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TABLE 15 - PIOM (621-9930) SWITCH SETTINGS

SWITCH SW1	STATE	SWITCH VALUE
1	CLOSED/ON	16
	OPEN/OFF *	0
2	CLOSED/ON	32
	OPEN/OFF *	0
3	CLOSED/ON	64
	OPEN/OFF *	0
4	CLOSED/ON	128
	OPEN/OFF *	0
5	CLOSED/ON	256
	OPEN/OFF *	0
6	CLOSED/ON	512
	OPEN/OFF *	0
7	CLOSED/ON	1024
	OPEN/OFF *	0
8	CLOSED/ON	2048
	OPEN/OFF *	0
SWITCH SW2	**STATE**	**SWITCH FUNCTION**
1	CLOSED/ON *	Clear outputs if: SW2 switch 2 is closed and an I/O fault occurs, the external cable disconnects, the external power fails, or the processor is in PROGRAM or DISABLE.
	OPEN/OFF	Freezes outputs with the above conditions.
2	CLOSED/ON	Recognizes an output module fault and acts according to SW2 switch 1.
	OPEN/OFF *	Ignores an output module fault.
3	CLOSED/ON *	Rack set for 8-point operation.
	OPEN/OFF	Rack set for 16-point operation.
4		Not used.

* Factory Setting

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ON-LINE EDITING AND PROGRAMMING IN PROCESSORS WITHOUT AUGMENTED RUN MODE PROGRAMMING (ARMP)

620-25 and 620-35 Processors with firmware revision of 35 or less allow on-line programmable controller changes, through on-line editing or on-line programming while the processor is in the RUN/PROGRAM mode. The following procedures explain how to perform this function. Note that these procedures apply only to Non-Augmented Run Mode Programming Processors shipped prior to November, 1987.

ON-LINE EDITING

To perform on-line editing the programmable controller keyswitch must be in RUN/PROG. The 623-51 Loader/Terminal must be in the PROGRAM mode, and the on-line programming function enabled according to SW2 switch 6 on the PLDM. During on-line editing the programmable controller continues to operate in the RUN mode while the Loader/Terminal changes one or more memory locations. When a program command is transmitted, the Processor Module makes the program changes after the scan being executed is completed.

Changes in a line are accomplished by overwriting elements while in the ENTER mode. Elements cannot be deleted, but they can be overwritten by NOP instructions (which occupy a memory word but do not affect program execution). Elements cannot be inserted, but they can overwrite existing NOP's. For this reason, planning must go into the initial program development to accommodate future on-line element additions (by careful placement of NOP's).

ON-LINE PROGRAMMING

To perform on-line programming the processor keyswitch must be in the RUN/PROG mode, the Loader/Terminal must be in the PROGRAM mode and the on-line programming function enabled according to SW2 switch 6 on the PLDM. It is possible to insert and delete elements from a line and to add new lines to a program. This type of change briefly places the processor in Software PROGRAM mode, makes the change, then returns to RUN mode. See Software Program Mode in the main body of the manual for more information.

CAUTION

Changing the number of elements in a line while in the RUN/PROGRAM mode causes the programmable controller to enter the Software PROGRAM mode for up to two seconds. A retentive scan is performed when returning to the RUN mode. During retentive scan all non-retentive output coils are turned OFF and non-retentive timers (TON's and TOFF's) are reset. Be extremely careful to analyze the affect of the retentive scan on program operation before using on-line programming.

Real Output Response to On-line Programming

In the parallel I/O system there are two switches which control output responses during PROGRAM or Software PROGRAM mode. They are PLDM (620-0033) SW2 switch 3 and PIOM (621-9937 and 621-9930) SW2 switch 1. PLDM SW2 switch 3 freezes outputs during the Software PROGRAM Mode and overrides the PIOM switch which controls output responses. To prevent outputs in the parallel I/O system from momentarily clearing during an on-line program change, set PLDM SW2 switch 3 to the OPEN/OFF position.

In the serial I/O system SW1 switch 6 on the SIOM is the only switch controlling output responses during on-line programming. This switch must be set to freeze outputs to prevent outputs from momentarily clearing during on-line programming.

Outputs must be in the OFF state when deleted to avoid real outputs remaining ON.

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SUPERSEDED SERIAL I/O SYSTEM

The superseded serial I/O system uses SLM 621-9936 and SIOM 621-9935.

SERIAL LINK MODULE (SLM)
Model No. 621-9936

The 621-9936 controls serial I/O data transfer to and from remote I/O. The processor can accommodate two SLM's, one installed in each of rack slots L and M in both the 620-25 and 620-35 processors. The SLM is a separate processor with its own data table and operates asynchronously from the Processor Module. A 12-pole connector provides connection for both serial channels. Each channel can be extended a maximum of 8,000 feet and each channel is capable of operating a maximum of 384 I/O or 8 racks.

There are five status indicators on the front of the SLM. The green LED's labeled ACTIVE energize during proper data transmission and reception. Two yellow LED's labeled LINK FAULT energize when a fault occurs on their respective channels. The green LED labeled PASS energizes after successful completion of the module self-test.

There are two eight-position DIP switches located on the printed circuit board of the SLM. Each switch sets the starting address and shutdown responses for one channel. Switch bank SW1, switches one through eight, selects the starting address and shutdown responses for channel one. Switches one through eight on switch bank SW2 select the starting address and shutdown repsonses for channel two. The starting addresses are set in increments of 48. Closing a switch (ON) adds that switch value to the starting address. The settings for the switches are shown in Table 16.

SERIAL INPUT/OUTPUT MODULE (SIOM)
Model No. 621-9935

The SIOM is located in the N slot in the full I/O rack or the H slot in the half rack. This module is the interface to the processor Serial Link Module (621-9939). The SIOM controls the remote I/O rack and communicates with the SLM.

Three LED indicators provide module and I/O status information. The green LED labeled PASS energizes after successful completion of the module self-test. The green LED labeled ACTIVE energizes as long as the module is receiving valid data over the serial channel. The amber LED labeled RACK FAULT turns ON if an output module fault is detected.

DIP switch bank SW1 (switches 1 through 8) located on the circuit board selects I/O starting addresses and control operation of the SIOM. The settings for these switches are shown in Table 17.

REMOTE SERIAL I/O CONFIGURATION

Serial I/O allows I/O racks to be mounted close to the machine or process being controlled rather than at the processor. There is no need for long wire runs to field devices. The 620-25/35 processor rack provides two slots, L and M, for Serial Link Modules. Two channels are operated by one SLM.

The maximum length for each channel is 8,000 feet. The serial channels are full duplex allowing simultaneous data transmission and reception.

Serial I/O Modules (621-9935) which are installed in each I/O rack connect to the serial channel in a multi-drop arrangement. This permits disconnecting an I/O rack without affecting the channel operation. The SIOM has a detachable connector to accomplish this function.

The SLM operates independently of the processor, and processor scan time is not affected by remote serial I/O channels. Serial channel scan rate is calculated by adding the individual update times incurred by each I/O rack. The update times are as follows:

48-point rack.....4.0ms
96-point rack.....5.0ms
192-point rack.....7.8ms

If one or more PUSH/PULL type cards are used on a channel, the update time for that channel will be increased by 6.1ms.

Addressing

SLM's installed in the processor rack determine the starting address for each serial channel. Each SLM has two 8-position DIP switches to set the starting address for each channel. The first six switches on each bank assign the starting address in multiples of 48. Closing a switch adds that switch value to the starting address.

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In the example in Figure 17, Rack 1 an 8-point parallel I/O rack, is assigned a starting address of 0 and ends with address 95. This is accomplished by setting the PIOM SW1 switches 1 through 8 OPEN/OFF. At this point, the starting address of channel one on the Serial Link Module must be assigned. This starting address for channel one is 96 because 96 is the closest higher number to 95 which can be set via the channel one I/O addressing DIP switches (SLM DIP switch 2). The total number of I/O operated on channel one is 240. Therefore, the starting address of channel two is 336 (96 - starting address of channel one, plus 240 - number of I/O on channel one = 336). This is accomplished by closing switches 1, 2 and 3 on the SLM channel two set of DIP switches.

After the serial channel starting addresses have been determined, each serial I/O module (SIOM) is assigned a starting address relative to the SLM starting address. This SIOM starting address ranges from 0 to 383 in increments of 48. This relative starting address is added to the SLM channel starting address in order to determine the actual starting address for each I/O rack on the channel. Closing a switch adds that switch value to the SIOM relative starting address.

For example, the first remote serial I/O rack in Figure 17 (Rack 2) is assigned the relative starting address of 0. This added to the channel starting address of 96 gives I/O rack 2 an actual starting address of 96 (96 + 0 = 96).

After the I/O rack starting address is determined, the rack is selected for 8 or 16-point I/O operation and half or full I/O rack operation. These two selections determine how many addresses are allocated to each I/O rack. This information is used to determine the starting addresses for other I/O racks on the channel. For example, the SIOM starting address for I/O Rack 2 is 0 and it operates 96 I/O points. Therefore, the relative starting address for I/O Rack 3 is 96 (0 + 96 = 96). The real starting address for Rack 3 is 192 (96 - the channel starting address, plus 96 - the relative starting address = 192). This procedure is repeated for Rack 4.

As stated, the real starting address for channel two is 336. The relative starting address for Rack 5 is 0. Rack 5 contains six 8-point I/O modules, allowing 48 addresses. Therefore, the real addresses for Rack 4 are 336 to 383. The relative starting address for rack 6 is 48 (0 + 48 = 48). The real starting address for rack 6 is 384 (336 - the channel starting address, plus 48 - the relative starting address = 384).

Notes on Selecting Addresses

The following rules must be observed when using the Bring In and Send Out instructions that are addressed to I/O modules located in the Serial I/O System:

1. The Send Out address plus 1 must be evenly divisible by 16 (e.g. 479 is a valid Send Out address since 479 + 1 is divisible by 16). Therefore, the most significant address of a 16-point I/O module is a valid Send Out address. The most significant address of every other 8-point I/O module in a rack (slots A, C, E etc.) is a valid Send Out address.

2. Bring In instructions may use any 16 consecutive addresses in the Serial I/O System. If 8-bit integrity is desired, the Bring In address plus 1 must be divisible by 8.

The Serial I/O System maintains 16-bit data integrity for Send Out, PUSH and PULL instructions.

When planning address assignments for the Serial I/O System, note that the channel starting address can only be assigned in increments of 48.

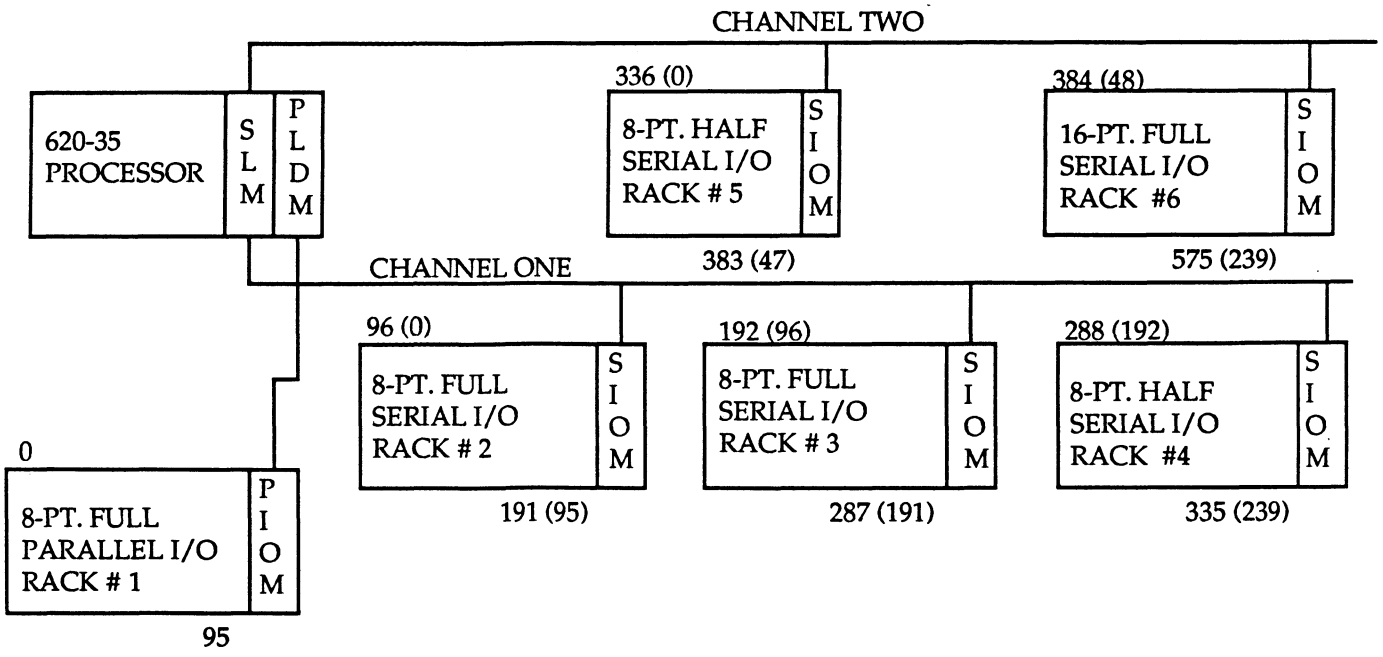
SLM SWITCH POSITION VALUES

SLM SWITCH CLOSED/ON	VALUE
1	48
2	96
3	192
4	384
5	768
6	1536

SIOM SWITCH POSITION VALUES

SIOM SWITCH	VALUE
1	48
2	96
3	192

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NOTE: ( ) indicate relative address.

RACK	RACK STARTING ADDRESS	I/O MODULES		I/0 PTS. PER RACK	RACK ENDING ADDRESS	DIP SWITCHES SET CLOSED/ON		
		NO.	PT.			PIOM	SLM	SIOM
1	0	12	8	96	95	SW2, 3	—	—
2	96	12	8	96	191	—	SW1, 2	—
3	192	12	8	96	287	—	—	SW1, 2
4	288	6	8	48	335	—	—	SW1, 3 SW1, 4
5	336	6	8	48	388	—	SW2, 1 SW2, 2 SW2, 3	SW1, 4
6	384	12	16	192	575	—	—	SW1, 1 SW1, 5

FIGURE 17 - EXAMPLE OF SUPERSEDED PARALLEL AND SERIAL ADDRESSING I/O CONFIGURATION

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SERIAL I/O
THEORY OF OPERATION

The 621 Serial I/O System allows the 620-25/35 processor to control 621 I/O that is remotely located as far as 8,000 feet from the processor. The 621 Serial I/O System consists of SLM's (621-9936) and SIOM's (621-9935) that operate asynchronously from the 620 processor program scan. The SLM and SIOM modules are microprocessor based utilizing the Motorola 6809E MPU. These intelligent modules perform all of the serial link operating tasks including diagnostics and rely on the 620 processor only to obtain certain control signals and I/O data exchange.

The SLM may be viewed as a master control module. The SLM actually resides on the processor rack I/O bus allowing the SLM to exchange data with the processor and monitor control signals from the processor for system startup and shutdown procedures. The SLM contains a data table for storing all I/O data from racks connected to the SLM's two serial ports.

The SIOM module, located in each serial I/O rack, operates the remote I/O rack. SIOM's may be viewed as slave modules to the SLM in that the SIOM's respond only to tasks issued by the SLM.

System Start-Up

The 621 serial I/O depends on the 620 processor for orderly start-up procedures. Applying power to the 620 processor or exiting the PROGRAM mode causes the serial I/O system to initiate the following start-up procedure:

1. The SLM and connected SIOM's perform a self-test of their ability to properly receive and transmit data.

2. The SLM clears its I/O Status Table to OFF.

3. The SLM queries all connected SIOM's that have passed the self-test for the following information:

   a. I/O rack relative starting address.
   b. I/O rack size.
   c. I/O module type (8- or 16- point)
   d. Location of I/O modules utilizing the PUSH or PULL instruction.
   e. Position of freeze or clear I/O DIP switch.
   f. Copy output status into SLM Data Table.

NOTE

The SIOM DIP switch settings determine the rack configuration and output response data required by the SLM. See Appendix Table 10 for switch settings.

The SIOM response data allows the SLM to allocate its Data Table addresses to the configuration of each serial channel, and allows the SLM I/O Status Table to freeze or clear according to the I/O rack's selected output response (freeze or clear) during processor mode change and system fault conditions.

The serial I/O system start-up procedure is accomplished while the 620 processor is also peforming its self-test. The serial I/O system will always have correct input data to present to the processor before the first processor program scan.

NOTE

If the SLM fails the self-test the SLM must be restarted by either exiting processor PROGRAM mode or cycling processor power.

If a SIOM fails the self-test, it will not respond to future SLM commands and must be restarted by shorting the reset terminals located on the SIOM or by cycling SIOM I/O rack power. The SIOM will then be brought on-line automatically by the SLM after successful completion of the SIOM self-test.

Serial Channel Operation

When the 620 processor is in the RUN mode, the SLM operates the serial channels in the following manner:

1. The SLM output status table is updated as each output and PUSH instruction is solved during the processor program scan.

2. The processor collects input status from the SLM data table during the processor input status scan. PULL data is collected from the SLM data table when the PULL instruction is executed in the processor program scan.

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3. The SLM services each SIOM in the order in which they are addressed, from the least to the most significant starting address. The SLM transmits output data to the selected SIOM. The SIOM updates its outputs at that time and also begins transmitting the input data back to the SLM.

4. I/O modules using the PUSH or PULL instructions are serviced by the SLM after all SIOM's on the channel are serviced. The SLM services only one of these modules per channel scan. Thus "N" number of PUSH or PULL modules located in a serial channel will require "N" serial channel scans to be serviced. Analog input or output modules are examples of modules using PUSH or PULL instructions. The SLM always performs a PUSH and PULL from locations containing these modules.

The serial I/O operation in the PROGRAM mode is the same as in the RUN mode except that the SIOM's do not update output modules located in the I/O rack. The SIOM does continue to transmit and PULL data to the SLM while the processor is in the PROGRAM mode.

System Error Checking

The 621 Serial I/O System performs several on-line checks.

1. Each message transmitted by an SLM or SIOM includes a Cyclic Redundancy Check Character (CRCC) to detect data errors. If two consecutive messages directed to a particular SIOM are received with CRCC errors, that SIOM will go off-line and wait for a restart procedure. An SLM receiving two consecutive CRCC errors from a SIOM will allow that SIOM to go off-line by not transmitting new data to the SIOM.

2. If a SIOM stops receiving data for any reason it will go off-line and wait for a restart procedure.

3. All SIOM's operate a local I/O rack diagnostic routine to all output modules using fault detection circuitry similar to that in the Parallel I/O System (see I/O System Test). The SIOM, if selected to recognize output module faults, will freeze or clear rack outputs but will continue to transmit input and PULL data to the SLM.

4. Most common I/O rack backplane data faults detected by the SIOM will cause the SIOM to go off-line.

Monitoring Serial I/O System Operation

The 621 Serial I/O System operates independently from the 620 processor. The 620 processor and parallel I/O will operate even though one or more SIOM's are not on-line. In order to detect that SIOM's are off-line the user should consider installing a Model 621-0004 System Diagnostic Module (SDM) in serial I/O racks. This module may be monitored in the control program so that if a SIOM is taken off-line appropriate action can be taken by the program.

An additional benefit of the SDM is that it has a relay that may be wired to remove power to rack output modules, if this feature is desired. If the user elects not to use the SDM, the control program should monitor an input that is always ON, at each serial I/O rack. If that input is OFF, indicating that a SIOM is off-line, appropriate action can be taken by the control program.

The serial channel can be selected to automatically shutdown for serious faults. This is described in the Serial I/O Shutdown section.

Serial I/O Shutdown

The 621 Serial I/O System will initiate a shutdown procedure when processor power is removed or when the processor is placed in the PROGRAM mode.

When the processor power is removed, the SLM ceases transmitting new data. The SIOM's effect a data receive timeout and freeze or clear SIOM rack outputs according to the SIOM DIP switch selections.

When the processor is placed in the PROGRAM mode the serial I/O system continues operations, however SIOM rack outputs are cleared or frozen as described in the Serial Channel Operation section.

Serial I/O racks may be taken off-line without affecting serial channel operation if desired. When a SIOM is taken off-line the SLM recognizes that the SIOM is no longer transmitting new data. The SLM then clears all Data Table input and output addresses associated with that SIOM to OFF. The SIOM rack outputs however, may be selected to be cleared or held in the last state.

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When a SIOM fault is recognized, the SLM can be selected to perform various shutdown procedures. The SLM shutdown response is determined by positions 7 and 8 on SLM DIP switch SW1. See Appendix Table 16. The shutdown responses to a SIOM going off-line are as follows:

1. The channel continues operation.
2. The channel containing the off-line SIOM shuts down.
3. Both channels on the SLM shutdown.
4. All I/O connected to the processor (parallel and serial) shutdown.

If the SLM is selected to shutdown, the SLM may only be restarted by cycling processor power or by going from the PROGRAM to the RUN mode.

Serial I/O System Restart

The 621 Serial I/O System initiates a total restart procedure as described in the System Start-up section by cycling power to the processor or by exiting processor PROGRAM MODE. These operations cause the Serial I/O System to reconfigure, and those SIOM's that do not pass the self-test are not brought on-line.

The procedure for restarting off-line SIOM's is:

1. Shorting the restart terminals located on the SLM connector restarts all SIOM's that have passed self-test and are off-line due to a data receive timeout or data receive error.

2. SIOM's with recognized output module faults can only be restarted by shorting the SIOM reset terminals or by cycling SIOM rack power. This also applies to SIOM's that are off-line due to a detected rack backplane fault.

3. If the SLM is selected to shutdown due to a SIOM fault, change the processor from PROGRAM to RUN mode or cycle processor power to restart the serial link. The SLM restart terminals do not restart the serial channel.

NOTE

When restarting off-line SIOM's it is recommended to attempt the restart via the SLM restart terminals or the SIOM reset terminals. Cycling processor power or exiting processor PROGRAM mode will cause the Serial I/O System to initiate a system start-up procedure that includes link configuration. Faulted SIOM's that do not respond during link configuration will not be brought on-line and the SLM fault LED's will remain OFF.

Serial I/O System Fault Recognition

Status LED's located on the SLM and SIOM can be used to identify Serial I/O System faults as follows:

<u>SLM</u>

1. The green PASS LED must be ON before operating the serial I/O channels. If this LED is OFF, it indicates that the SLM is not functional. Attempt a restart of the SLM via a processor mode change or processor power cycling before replacing the module.

2. The two green ACTIVE LED'S indicate that the SLM is transmitting data on the serial channels. When OFF, this indicates that the SLM has shut down due to a SIOM fault or inoperable SLM.

3. The two amber SLM link fault LED's, if ON, indicate a faulted SIOM due to:

   a. a data receive error,
   b. a data receive timeout,
   c. a SIOM hardware fault, or
   d. an output module fault.

<u>SIOM</u>

1. The SIOM green PASS LED must be ON before operating the SIOM on the serial channel. If this LED is OFF the SIOM did not pass its self-test. Attempt a reset of the SIOM before replacing the module. A flashing PASS LED indicates that channel addressing capacity has been exceeded by this rack.

2. The green ACTIVE LED indicates that the SIOM is on-line and transmitting data. If the LED is OFF, it indicates that the SIOM is off-line due to:

   a. a data receive error,
   b. a data receive timeout,
   c. a SIOM rack backplane fault, or
   d. a SLM link shutdown procedure.

3. The amber rack fault LED will be ON when an output module fault is detected. This LED will also be ON when the SIOM detects most common rack backplane faults.

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TABLE 16 - SLM (621-9936) SWITCH SETTINGS

SWITCH	STATE	SWITCH VALUE
SW1		
1	CLOSED/ON	48
	OPEN/OFF *	0
2	CLOSED/ON	96
	OPEN/OFF *	0
3	CLOSED/ON	192
	OPEN/OFF *	0
4	CLOSED/ON	384
	OPEN/OFF *	0
5	CLOSED/ON	768
	OPEN/OFF *	0
6	CLOSED/ON	1536
	OPEN/OFF *	0

SWITCH/STATE		SWITCH FUNCTION
7	8	
OPEN/OFF *	OPEN/OFF *	Channel continues to operate if a channel fault occurs **
CLOSED/ON	CLOSED/ON	Channel with fault ceases operation. **
OPEN/OFF	CLOSED/ON	Both channels on SLM cease operation if a channel fault occurs. **
CLOSED/ON	OPEN/OFF	All I/O (parallel and serial) cease operation.

* Factory Setting.

** A channel fault is defined as the SIOM being taken off-line by a power failure or a card fault (if selected).

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TABLE 17 - SIOM (621-9935) SWITCH SETTINGS

SWITCH	STATE	SWITCH VALUE/FUNCTION
SW1		
1	CLOSED/ON	48
	OPEN/OFF *	0
2	CLOSED/ON	96
	OPEN/OFF *	0
3	CLOSED/ON	192
	OPEN/OFF *	0
4	CLOSED/ON *	Designates I/O half rack operation.
	OPEN/OFF	Designates I/O full rack operation.
5	CLOSED/ON	Sets I/O rack for 16-point operation.
	OPEN/OFF *	Sets I/O rack for 8-point operation.
6	CLOSED/ON	Freeze I/O if a serial communication fault occurs.
	OPEN/OFF *	Clear I/O if a serial communication fault occurs.
7	CLOSED/ON *	Recognize I/O card fault and act according to SW1 switch 6 setting.
	OPEN/OFF	Ignore I/O card fault.
8		Not used.

* Factory Setting

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TABLE 18 - 620-20, 620-30, 620-25, AND 620-35 MODULE/RACK COMPATIBILITY

SYSTEM	620-20	620-30	620-25	620-35	
Rack Model No.	(620-2090)	(620-3090)	(620-2590)	(620-3590)	
MODULE					COMMENTS
629-0020 2K MM	x	x	x	x	
620-0021 4K MM	x	x	x	x	
620-0022 8K MM	x	x	x	x	
620-0023 16K MM		x	x	x	
620-0024 24K MM		x	x	x	
620-0025 2K MM	x	x	x	x	Replaces 620-0020
620-0026 4K MM	x	x	x	x	Replaces 620-0021
620-0027 8K MM	x	x	x	x	Replaces 620-0022
620-0030 SCM	x	x			
620-0031 2K RM	x	x			
620-0036 PSM	x	x	x	x	
620-0038 CNM	x	x	x	x	
620-0039 4K RM		x			
620-0043 CIM	x	x	x	x	
620-0044 CIM					
620-0047 PSM	x	x	x	x	
620-0048 DCM	x	x	x	x	Replaces 620-0042
620-0052 DCM	x	x	x	x	Replaces 620-0042
620-0054 SCM			x	x	
620-0055 2K RM	x	x	x	x	
620-0056 4K RM		x	x	x	
620-0057 512 IOCM			x	x	
620-0058 1024 IOCM			x	x	
620-0059 RCM			x	x	
620-0080 PM			x	x	
620-0081 HIM	x	x	x	x	
620-0085 2048 IOCM		x	x	x	
620-0086 PLDM	x	x	x	x	Replaces 620-0033
620-2030 PM	x				
620-2032 IOCM	x				
620-2033 PM	x				Replaces 620-2030
620-3032 2048 IOCM		x			
620-3033 PM		x			Replaces 620-3030
621-9936 SLM	x	x	x	x	
621-9939 SLM	x	x	x	x	

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