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User Manual for the
HE700GEN100,
HE700GEN200

uGENI VME Interface Module

Third Edition
20 July 2000

MAN0105-02

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PREFACE

This manual explains how to use the Horner APG uGENI VME Interface module. This manual should be used in conjunction with GE Fanuc's **GFK-0073 "Genius™ I/O GENI Board**-User's Manual".

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ABOUT PROGRAMMING EXAMPLES

Any example programs and program segments in this manual or provided on accompanying diskettes are included solely for illustrative purposes. Due to the many variables and requirements associated with any particular installation, Horner APG cannot assume responsibility or liability for actual use based on the examples and diagrams. It is the sole responsibility of the system designer utilizing uGENI VME Interface Module to appropriately design the end system, to appropriately integrate the uGENI VME Interface Module and to make safety provisions for the end equipment as is usual and customary in industrial applications as defined in any codes or standards which apply.

Note: The programming examples shown in this manual are for illustrative purposes only. Proper machine operation is the sole responsibility of the system integrator.

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Revisions to This Manual

This version (MAN0105-02) of the **uGENI VME Interface Module User Manual** contains the following revisions, additions and deletions:

1. Converted manual into Word format.

2. Changed company name from Horner Electric, Inc. to Horner APG, LLC.

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CHAPTER 1: INSTALLATION

This chapter discusses the installation of an HE700GEN100/200 uGENI VME Interface Module into a VME rack.

1.1 Module Placement

The HE700GEN100/200 is considered a single slot generic VME module. If the interrupt capabilities of this board are to be used, it must be placed in the interrupt chain. If not, it should be placed after all modules that are utilizing VME interrupts.

1.2 Wiring Considerations

Normally, a GE Fanuc programmable controller runs the network, through a PLC module called a Genius Bus Controller (GBC). The HE700GEN100/200 has the ability to replace or exist in conjunction with a Genius Bus Controller. Up to 32 devices are wired in a daisy chained fashion. Network devices support four communications terminals, Serial 1, Serial 2, Shield In and Shield Out. The network is terminated at each end with an appropriate terminating resistor. The value of the resistor should be chosen to match the characteristic impedance of the cable. Refer to GE Fanuc Automation publication **GFK-90486** for help in selecting an appropriate cable type for your application. Note: If the characteristic impedance of the cable is unknown, 120 ohm terminating resistors should be used.

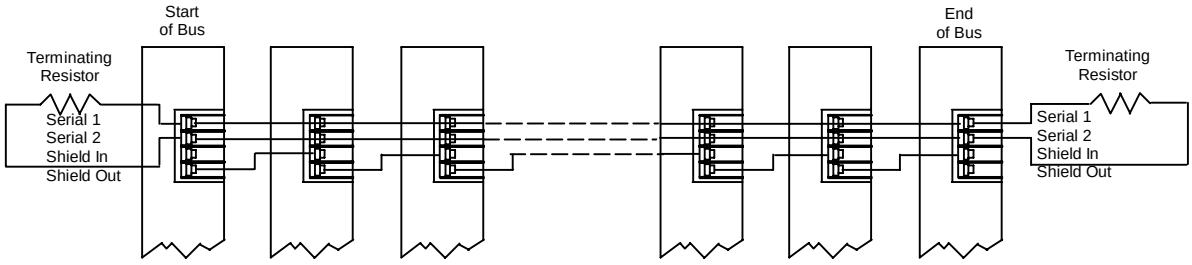


Figure 1.1 – A Typical Genius Network

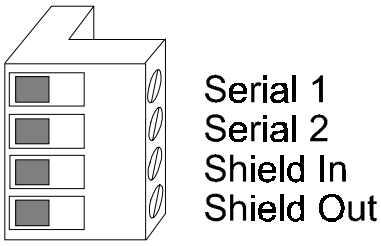


Figure 1.2 – The pinout for the HE700GEN100/200 Genius connector

Each of the (up to) 32 devices on the network is assigned a Genius Bus Address ranging from 0 to 31. Bus Controllers are most typically assigned a Genius Bus Address of 31. In applications with redundant bus controllers, the “backup” bus controller is address 30. Bus address 0 is normally reserved for the Genius Hand Held Monitor.

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1.3 Dip Switch Location

There are several switches on the HE700GEN100/200 board that are used to configure the Genius Interface, I/O addresses, Interrupts and User Mode. Figure 1.3 shows the location of these switches.

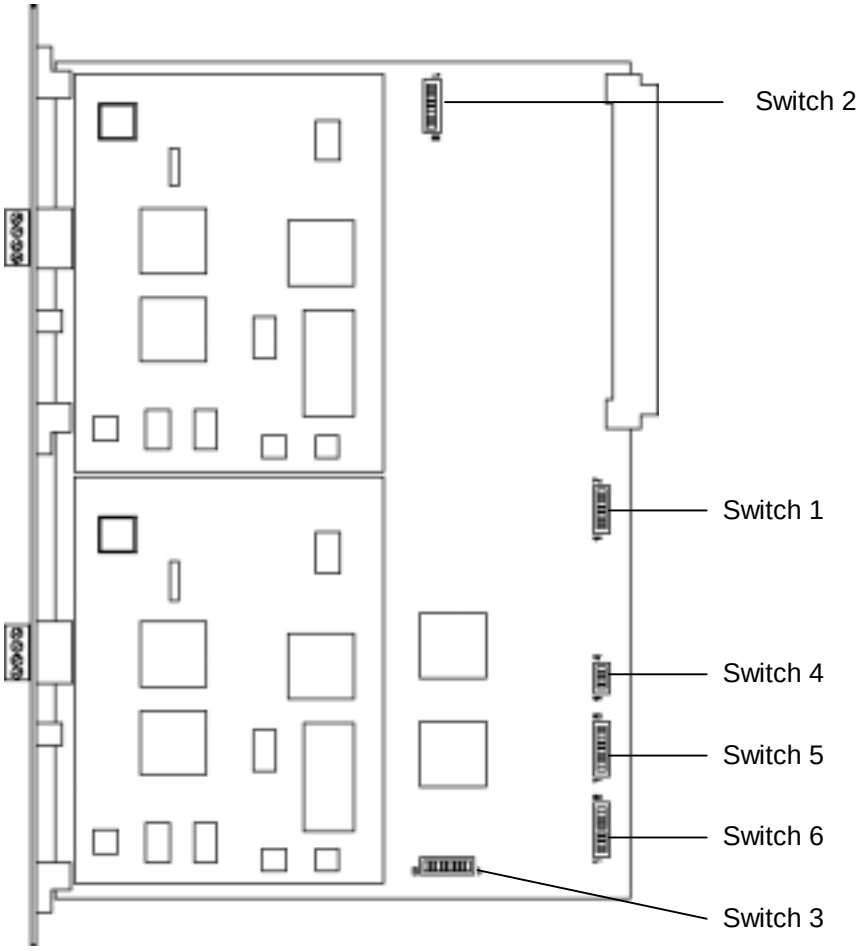


Figure 1.3 – Dip Switch Locations

The definition of these switches is shown below. Configuration based on these switches is described in Chapter 2: "Configuration".

Table 1.1 – Dip Switch Definitions	
Dip Switch	**Description**
Switch 1	Interrupt Priority
Switch 2	uGENI 1 Genius Setup
Switch 3	uGENI 2 Genius Setup
Switch 4	Interrupt Mask / user Mode
Switch 5	uGENI Memory Address
Switch 6	uGENI I/O Address / interrupt Vector

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CHAPTER 2: CONFIGURATION

This chapter discusses the configuration of an HE700GEN100/200 uGENI VME Interface Module for operation in a generic VME rack, and for Genius communications.

2.1 Genius Configuration

The configuration for each uGENI board is independent. There is one 8 position dip switch for each uGENI board. Dip Switch 2 sets up the Genius configuration for uGENI 1 and Dip Switch 3 sets up the Genius configuration for uGENI 2 (see Figure 1.3 on page 10). Below is the description of the dip switch positions

Table 2.1 - Genius Bus Address Switch Settings
(Dip Switch 2: uGENI 1, Dip Switch 3: uGENI 2)

Block Number	Switches					Block Number	Switches				
	5	4	3	2	1		5	4	3	2	1
0	1	1	1	1	1	16	0	1	1	1	1
1	1	1	1	1	0	17	0	1	1	1	0
2	1	1	1	0	1	18	0	1	1	0	1
3	1	1	1	0	0	19	0	1	1	0	0
4	1	1	0	1	1	20	0	1	0	1	1
5	1	1	0	1	0	21	0	1	0	1	0
6	1	1	0	0	1	22	0	1	0	0	1
7	1	1	0	0	0	23	0	1	0	0	0
8	1	0	1	1	1	24	0	0	1	1	1
9	1	0	1	1	0	25	0	0	1	1	0
10	1	0	1	0	1	26	0	0	1	0	1
11	1	0	1	0	0	27	0	0	1	0	0
12	1	0	0	1	1	28	0	0	0	1	1
13	1	0	0	1	0	29	0	0	0	1	0
14	1	0	0	0	1	30	0	0	0	0	1
15	1	0	0	0	0	31	0	0	0	0	0
1 = ON, 0 = OFF											

Table 2.2 - Genius Baud Rate Switch Settings
(Dip Switch 2: uGENI 1, Dip Switch 3: uGENI 2)

Baud Rate	Switches	
	7	6
153.6k Extended	1	1
38.4K	1	0
76.8K	0	1
153.6K Standard	0	0
1 = ON, 0 = OFF		

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Table 2.3 - Genius Output Enable Switch Settings (Dip Switch 2: uGENI 1, Dip Switch 3: uGENI 2)	
Outputs	**Switch 8**
Enabled on Startup	1
Disabled on Startup	0
1 = ON, 0 = OFF	

2.2 User Mode Configuration

The User Mode is a setting that affects the entire module and is determined by switch 4 on Dip Switch 4. This setting determines which AM Codes the module will respond to. Below is a description of the switch settings and addresses.

Table 2.4 – User Mode Switch Settings (AM Code Addressing, Dip Switch 4)	
Switch 4	**Mode**
1	User Mode I/O is AM = 29H uGENI is AM = 39H
0	Supervisor Mode I/O is AM = 29H or 2DH uGENI is AM = 39H or 3DH
1 = ON, 0 = OFF	

NOTE: If a Series 90-70 PLC is used, User Mode cannot be set to Supervisor Mode if an I/O Address of less than 5000H is used.

2.3 I/O Address and Interrupt Vector Configuration

The I/O Address and Interrupt Vector Address in the short address space is determined by the Dip Switch 6 setting. The eight switches represent each of the eight bits in the upper two digits of the address. The lower two digits are always zero. The most common I/O addresses are; 1000H, 1800H, 2000H, 2800H, 3000H, 3800H, 4000H, 4800H and 5000H (See CPU documentation for detailed descriptions on available addresses). On the following page is a description of the Dip Switch settings. The Interrupt Vector Address is the address immediately following the I/O Address (I/O Address Base + 1).

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Table 2.5 – I/O Address Switch Settings																
I/O Address Base (Dip Switch 6)																
I/O Address Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Switch Number	8	7	6	5	4	3	2	1	X	X	X	X	X	X	X	X
1 = ON (Address bit Active) 0 = OFF (Address bit Inactive) X = Always Zero																

Example I/O Addresses (Dip Switch 6)								
Example I/O Address	**Switches**							
	8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
1000H	0	0	0	1	0	0	0	0
1800H	0	0	0	1	1	0	0	0
2000H	0	0	1	0	0	0	0	0
2800H	0	0	1	0	1	0	0	0
3000H	0	0	1	1	0	0	0	0
3800H	0	0	1	1	1	0	0	0
4000H	0	1	0	0	0	0	0	0
4800H	0	1	0	0	1	0	0	0
5000H	0	1	0	1	0	0	0	0
1 = ON, 0 = OFF								

Table 2.6 – Interrupt Vector address (Dip Switch 6)
I/O Address Base +1

2.4 uGENI Address Configuration

The uGENI Address is determined by the Dip Switch 5 setting. The eight switches represent the eight bits in the upper two digits of the address. The lower four digits are always zero. The most common starting addresses are; 000000H, 020000H, 040000H, 060000H, 080000H, 0A0000H, 0C0000H, 0E0000H and 100000H (See CPU documentation for detailed descriptions on available addresses). Below is a description of the Dip Switch settings.

Table 2.7 – uGENI Address Switch Settings																								
uGENI Address Base (Dip Switch 5)																								
uGENI Address Bit	**24**	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Switch Number	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**
1 = ON (Address bit Active) 0 = OFF (Address bit Inactive) X = Always Zero																								

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Example uGENI Address (Dip Switch 5)								
Example uGENI Address	**Switches**							
	8	**7**	**6**	**5**	**4**	**3**	**2**	**1**
000000H	0	0	0	0	0	0	0	0
020000H	0	0	0	0	0	0	1	0
040000H	0	0	0	0	0	1	0	0
060000H	0	0	0	0	0	1	1	0
080000H	0	0	0	0	1	0	0	0
0A0000H	0	0	0	0	1	0	1	0
0C0000H	0	0	0	0	1	1	0	0
0E0000H	0	0	0	0	1	1	1	0
100000H	0	0	0	1	0	0	0	0
1 = ON, 0 = OFF								

2.5 Interrupt Configuration

The interrupt level is determined by the Dip Switch 1 settings. The interrupt acknowledge level is determined by the Dip Switch 4 settings. The interrupt acknowledge level must match the interrupt level setting.

Table 2.8 – Interrupt Level (Dip Switch 1)	
Switch	**Interrupt Level**
1 = ON	1 (Lowest Priority)
2 = ON	2
3 = ON	3
4 = ON	4
5 = ON	5
6 = ON	6
7 = ON	7 (Non Maskable)
1 = ON, 0 = OFF	
At most only one of the eight switches should be on. For no interrupts, all switches should be OFF.	

Table 2.9 – Interrupt Acknowledge Level (Dip Switch 4)			
Interrupt Level	**Switch 3**	**Switch 2**	**Switch 1**
None	1	1	1
1	1	1	0
2	1	0	1
3	1	0	0
4	0	1	1
5	0	1	0
6	0	0	1
7	0	0	0
1 = ON, 0 = OFF			
Interrupt Acknowledge Level must match Interrupt Level set by Dip Switch 1			

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CHAPTER 3: MEMORY MAP

This chapter discusses the Memory Map of an HE700GEN100/200 uGENI VME Interface Module.

3.1 Short Address I/O Space

The Short Address I/O Space configured by Dip Switch 6 is used to retrieve and send status information to and from the uGENI boards. The tables below show the definition and use of the bits for each address.

Table 3.1 – Short I/O Address Space Definition
(Set by Dip Switch 6)

Input Bit	Description	Output Bit	Description
0	uGENI 1 interface ok status 0 = On	0	Not Used
1	uGENI 1 communications ok status 0 = On	1	Not Used
2	uGENI 1 interrupt status 1 = Interrupt present	2	uGENI 1 reset interrupt 0 = Held in reset
3	uGENI 1 reset status 0 = Held in reset	3	uGENI 1 reset control 0 = Held in reset
4	uGENI 2 interface ok status 0 = On	4	Not Used
5	uGENI 2 communications ok status 0 = On	5	Not Used
6	uGENI 2 interrupt status 1 = Interrupt present	6	uGENI 2 reset interrupt 0 = Held in reset
7	uGENI 2 reset status 0 = Held in reset	7	uGENI 2 reset control 0 = Held in reset

Table 3.2 – interrupt Vector Address Space Definition (Set by Dip Switch 6 + 1)
Interrupt Vector (1 byte)
NOTE: The interrupt vector must be defined before the uGENI is taken out of reset.

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3.2 uGENI Address Space

The uGENI Address Space configured by Dip Switch 5 is used to retrieve and send data to and from the uGENI boards. The table below shows the memory address for each section of memory on the uGENI boards.

Table 3.3 – uGENI Address Map

	Decimal Starting Location	Hexadecimal Starting Location	Description	Size (in bytes)
uGENI 1	uGENI Address + 0000	uGENI Address + 0000H	Request Queue	2176
	uGENI Address + 2176	uGENI Address + 0880H	Request Queue Head pointer	1
	uGENI Address + 2177	uGENI Address + 0881H	Request Queue Tail Pointer	1
	uGENI Address + 2178	uGENI Address + 0882H	GENI Setup Table	16
	uGENI Address + 2194	uGENI Address + 0892H	GENI Status Table	16
	uGENI Address + 2210	uGENI Address + 08A2H	Interrupt Status Table	16
	uGENI Address + 2226	uGENI Address + 08B2H	Interrupt Disable Table	16
	uGENI Address + 2242	uGENI Address + 08C2H	Command Block	16
	uGENI Address + 2258	uGENI Address + 08D2H	Transmit Datagram Buffer	240
	uGENI Address + 2498	uGENI Address + 09C2H	Read Datagram Buffer	134
	uGENI Address + 2632	uGENI Address + 0A48H	I/O Table Lockout Request	1
	uGENI Address + 2633	uGENI Address + 0A49H	I/O Table Lockout State	1
	uGENI Address + 2634	uGENI Address + 0A4AH	Reserved	5045
	uGENI Address + 7680	uGENI Address + 1E00H	Device Configuration Table	256
	uGENI Address + 7936	uGENI Address + 1F00H	Directed Control Input Table	128
	uGENI Address + 8064	uGENI Address + 1F80H	Broadcast Control Output Table	128
	uGENI Address + 8192	uGENI Address + 2000H	Device I/O Table	8192
uGENI 2	**Decimal Starting Location**	**Hexadecimal Starting Location**	**Description**	**Size (in bytes)**
	uGENI Address + 16,384	uGENI Address + 4000H	Request Queue	2176
	uGENI Address + 18,560	uGENI Address + 4880H	Request Queue Head pointer	1
	uGENI Address + 18,561	uGENI Address + 4881H	Request Queue Tail Pointer	1
	uGENI Address + 18,562	uGENI Address + 4882H	GENI Setup Table	16
	uGENI Address + 18,578	uGENI Address + 4892H	GENI Status Table	16
	uGENI Address + 18,594	uGENI Address + 48A2H	Interrupt Status Table	16
	uGENI Address + 18,610	uGENI Address + 48B2H	Interrupt Disable Table	16
	uGENI Address + 18,626	uGENI Address + 48C2H	Command Block	16
	uGENI Address + 18,642	uGENI Address + 48D2H	Transmit Datagram Buffer	240
	uGENI Address + 18,882	uGENI Address + 49C2H	Read Datagram Buffer	134
	uGENI Address + 19,016	uGENI Address + 4A48H	I/O Table Lockout Request	1
	uGENI Address + 19,017	uGENI Address + 4A49H	I/O Table Lockout State	1
	uGENI Address + 19,018	uGENI Address + 4A4AH	Reserved	5045
	uGENI Address + 24,064	uGENI Address + 5E00H	Device Configuration Table	256
	uGENI Address + 24,320	uGENI Address + 5F00H	Directed Control Input Table	128
	uGENI Address + 24,448	uGENI Address + 5F80H	Broadcast Control Output Table	128
	uGENI Address + 24,576	uGENI Address + 6000H	Device I/O Table	8192

NOTE: For more detailed information on the uGENI board, obtain document number **GFK-0073 "Genius I/O GENI Board"** from your GE Fanuc distributor.

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CHAPTER 4: OPERATION

This chapter discusses the operation of the HE700GEN100 and HE700GEN200 uGENI VME Interface Modules.

4.1 Configuration

The configuration of the uGENI VME Interface module requires the joint operation of several devices. The VME CPU has a required addressing scheme that must be followed and Genius must also be configured separately. The uGENI VME Interface module must be configured to operate properly in both environments.

Before configuring the Interface module, several items need to be determined. Below is a list of these items and the associated page number for the configuration setting.

1. A. Which AM codes does the VME CPU support? (Page 12)
   B. Does the VME CPU support both USER and SUPERVISOR modes for AM code addressing? (Page 12)
2. Which addresses does the VME CPU support for Short Address space? (Page 13)
3. Which addresses does the VME CPU support for Standard Address space? (Page 13-14)
4. Does the VME CPU support VME Interrupts? (Page 14)
5. Which Interrupt levels does the VME CPU support? (Page 14)
6. Which Interrupt Vectors does the VME CPU support? (Page 13)
7. What is the Genius Bus Address for each uGENI? (Page 11)
8. What is the Genius baud rate for each uGENI? (Page 11)
9. Should each uGENI control outputs on start-up? (Page 11)

Once these items have been determined, the appropriate sections in chapter 2 can be used to determine the dip switch settings.

4.2 Initialization

On power-up the uGENI boards should be initialized. This is accomplished by first writing a 0 to the appropriate bits in the Short Address I/O space (Page 19). Writing a 1 to these values will bring the uGENI boards out of reset. If the uGENI boards recover from reset correctly, the Interface Ok Status bits will be cleared. If there are no conflicts on the Genius bus the Communications Ok Status bit will also be cleared at this time.

If the interrupt capability of this board is to be utilized, the Interrupt Vector must be written to the appropriate Short Address space before bringing the uGENI boards out of reset (Page 19).

4.3 Communications

Once the initialization is complete, the uGENI board may be directly addressed using Standard Address space (Page 20). The GE Fanuc document **GFK-0073** "Genius I/O GENI Board" describes in detail, how communications over the Genius network is accomplished. Contact your GE Fanuc distributor to obtain a copy of this document.

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