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Errata

Title & Document Type: 1630A/D/G Logic Analyzer Operating and Programming Manual

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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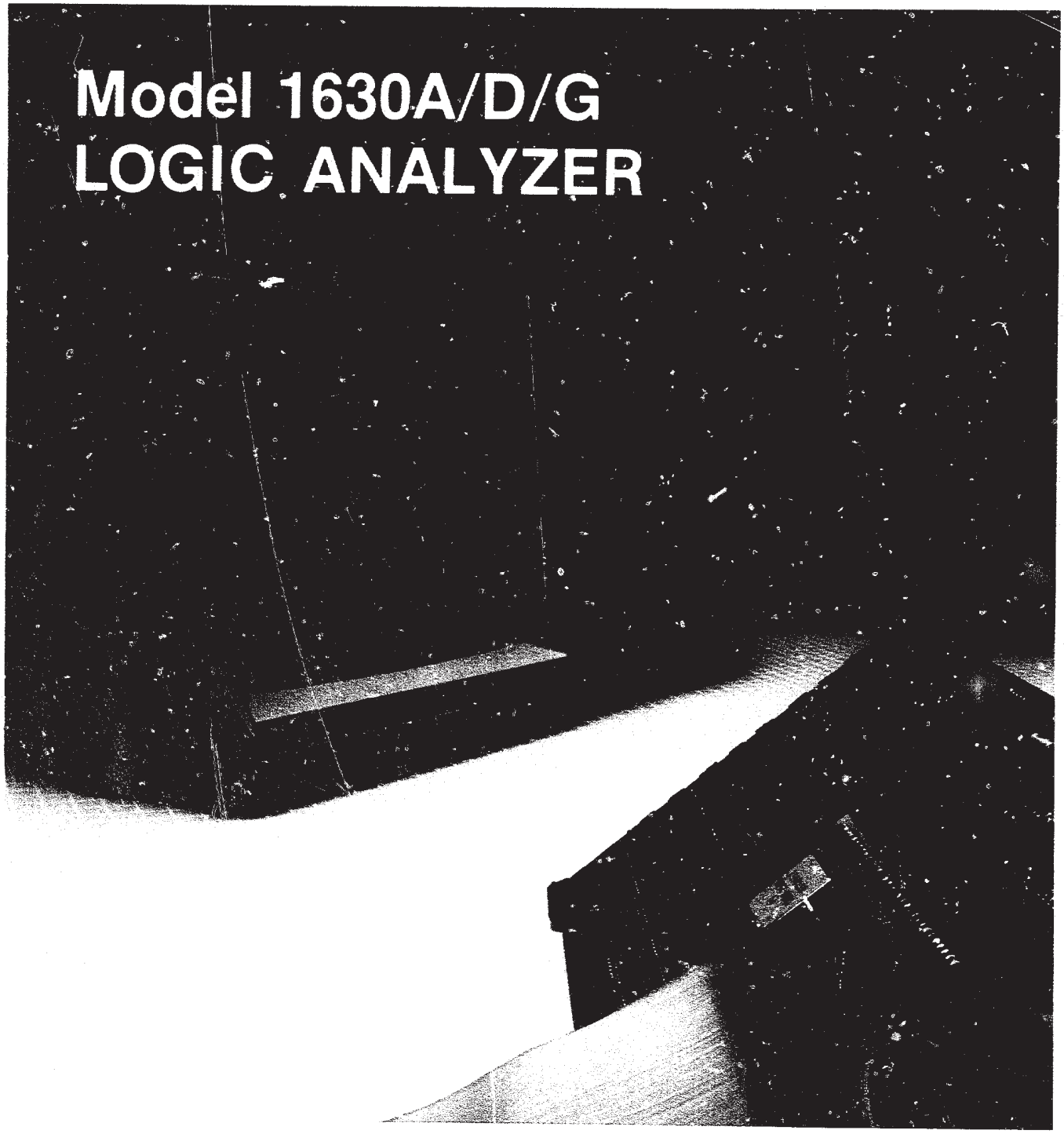
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OPERATING AND PROGRAMMING MANUAL



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OPERATING AND PROGRAMMING MANUAL

HP LOGIC ANALYZERS
MODELS 1630A/D/G

This manual applies to **Models 1630A/D (Option 007) and all 1630G** instruments. It also applies to **1630A** instruments serial prefixed **2424A and below,** and **1630D** instruments serial prefixed **2428A and below.**

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SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

USE CAUTION WHEN EXPOSING OR HANDLING THE CRT.

Breakage of the Cathode-ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the instrument. Handling of the CRT shall be done only by qualified maintenance personnel using approved safety mask and gloves.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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1630A/D/G Operating and Programming Manual

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Chapter 1
General Information

INTRODUCTION

This manual describes how to operate the Hewlett-Packard Models 1630A, 1630D, and 1630G Logic Analyzers. The three analyzers operate the same, but each have different configuration capabilities. The 1630G is the latest configuration with added performance measurement capabilities that are not possible with the 1630A or 1630D logic analyzers. The differences are described, wherever applicable, throughout this manual. This first chapter describes the physical and electrical characteristics of the analyzer. At the end of this chapter are two tables: one lists the analyzer specifications guaranteed by HP, and the other lists the analyzer operating characteristics.

MANUAL CONTENTS

This manual contains instructions and information to help you install and operate the logic analyzer. It shows how to assign labels in the format specification to identify signals from the input probes, and how to assign symbols to represent values found on those labeled inputs.

Chapter 2 describes how to set up the logic analyzer for use. Directions are given for connecting the probe cables to a system under test and initiating the analyzer self test.

Chapter 3 contains a menu map and a front panel keyboard description. The menu map helps to put the overall operation of the analyzer into perspective. Page numbers are given by each menu to reference the description of the menu in the manual.

Chapter 4 of this manual is State Measurements. The basic state measurements, from taking a trace in a free-run mode to selective tracing, is explained in a step-by-step process.

Chapter 5 contains the software performance analysis measurements. Although these measurements are state measurements, an entire chapter is devoted to them because of the complexity of overview analysis.

Chapter 6 is a description of the timing measurements. Simple timing measurements are described in a step-by-step process.

Chapter 7 describes interactive state/timing measurements.

Chapter 8 is a description of the system peripheral menus of the 1630A/D and the 1630G.

Chapter 9 contains the instructions used for programming the 1630 logic analyzers via HP-IB or HP-iL.

Appendix A contains all the possible display messages that may appear on the analyzer screen. An HP-IB overview is given in Appendix B for use as a reference for programming over the HP-IB. Appendices C, D, and E explain using a printer, tape memory, or disc memory accessories with the logic analyzer.

ANALYZER DESCRIPTION

Logic analyzers perform trace measurements. The HP 1630A/D/G models are interactive state and timing analyzers for use in the design and troubleshooting of microprocessor based systems. An analyzer traces activity from several points during a period of system operating time. The analyzer may perform both state and timing measurements together and interactively control the capture of information in each of these two functions.

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The analyzer can perform overview measurements with which the performance of code modules in software-intensive systems may then be analyzed. Overview measurements available in all three 1630 models include state and time interval histograms. The 1630G has added overview measurement features that enhance the state label histogram and allow time position and linkage measurements. The logic analyzers can be described as having two basic functions, that of state and timing, and have special features in each function which are listed below.

State Analysis

The state analysis function of each model features:

- Continuous trace until compare "equal to" or "not equal to" is provided. The compare file is the width of the analyzer, and has depth of up to 16 words with the 1630A/D and in the edit compare mode of the 1630G. The 1630G has a full compare mode in which the entire trace may be compared.
- Three ORed clocks given in single-phase or two-phase demultiplexing modes.
- Data sampling up to 25 MHz.
- 1024 states available in memory after a trace.
- A State Chart of any user-defined label may be selected for display.
- State analysis can be armed by the timing analysis section.
- A State Histogram of any user-defined label may be selected.
- A Time Interval Histogram of the time software takes to execute from one selected point in software to another.
- Time Positional measurements for the occurrences of an event per unit time may be made. (1630G only)
- Linkage measurements which show the relative frequency of occurrence of a set of events. (1630G only)

Timing Analysis

The timing analysis function of each system features:

- Sampling ranges from 10 nS to 500 mS, in increments of 1, 2, and 5.
- Timing waveforms that can be magnified from X1 to X40 in 1, 2, and 4 increments.
- Time between dual cursors (x and o) can be displayed to within 1 sample period.
- 1024 samples available in memory after a trace.
- Timing analysis can be armed by the state analysis section.
- Timing can be triggered by an asynchronous pattern, ANDed with a glitch or edge on any channel, and patterns that exceed or fall short of a specified time limit.

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INTERNAL STORAGE

The 1630G has the added feature of an internal storage space which allows the user to store menu configurations and an inverse assembler. One configuration of each menu and one inverse assembler may be stored at one time. The stored configurations and inverse assemblers may be specified for automatic loading at power-up of the 1630G.

THE SYSTEM SPECIFICATION

Use the menus in this specification to identify how the analyzer will be used: whether as a state analyzer, a timing analyzer (with or without glitch capture), or a combined state and timing analyzer. In this menu, you also identify the way the analyzer will operate when used as part of a system, or when using capabilities offered by accessories.

THE FORMAT SPECIFICATION

Use the menus in this specification to set up the way the analyzer formulates displays from its captured information. You can label individual bits or sets of bits, and assign names to identify address ranges and/or specific values found in those labeled sets. The analyzer will compose displays using your labels and names, if desired.

THE TRACE SPECIFICATION

Use the menus in this specification to enter parameters for making your measurements. You can set up the analyzer to trace state flow and/or record electrical activity at nodes in a system under test. The analyzer can also perform overview measurements to gauge the efficiency of selected software routines.

LIST DISPLAYS

The analyzer composes lists of information captured from labeled sets of bits. These lists show a series of software executions, and/or a sequence of electrical activities at nodes in a system under test. Values shown in these lists can be expressed using names of your choice, as well as using numbers in the binary, octal, decimal, and hexadecimal number bases. Values can also be expressed as ASCII codes for labels having from 6 to 16 bits.

WAVEFORM DISPLAYS

The waveform display shows up to 16 individual traces of electrical activity on selected bits. Each trace is shown as a continuous line of high and low states. The waveform shows how the states changed with time at each monitored point. You can also see points on the traces where glitches were detected during the measurement, if desired. Glitch detection is accomplished by internally combining two timing channels attached to a single probe, using one channel for data values, and using one of the channels as a glitch detector.

CHART DISPLAYS

The analyzer can format two types of chart displays: XY charts, and histograms. XY charts show a plot of the flow of values on a labeled set of bits. You can control the horizontal and vertical scales of the chart to examine the details around areas of interest on the XY chart.

Histogram charts are bar graphs used to measure the performance of software modules in a system under test. The analyzer can show two types of histograms: state label histograms, and time interval histograms. A state label histogram shows the relative number of executions within each range of states you define. Up to eight ranges of states can be defined for a label histogram. Time interval histograms show eight time ranges; you can define the period of each range. You can set up the analyzer to make time interval measurements each time the software executes from one selected point to another in the system under test. The time interval histogram shows how often execution of the selected software module was completed within each of the time ranges you defined.

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PHYSICAL CONFIGURATIONS

The following is a list of the analyzer configurations, components, and optional accessories:

1. HP Model 1630A Logic Analyzer. Offers 35 channels for state, timing, and combined state/timing measurements.

2. HP Model 1630D Logic Analyzer. Same as 1630A, except offers 8 additional channels for state and timing measurements.

3. HP Model 1630G Logic Analyzer. Same as 1630A, except offers 30 additional channels for state measurements.

4. HP Model 10271A General Purpose State Probe. Nine channels for collecting state activity plus an input clock channel. Used to supply state activity only. Three state probes are supplied with the 1630A/D/G.

5. HP Model 10272A General Purpose State/Timing Probe. Eight channels for collecting state activity or timing activity. No input clock channel. One state/timing probe is supplied with either 1630A or 1630G and two are supplied with the 1630D.

6. HP Model 10273A General Purpose State Probe. 10 channels for collecting state activity. Three state probes are supplied with the 1630G.

7. HP Model 82161A Digital Cassette Drive. Optional accessory for Models 1630A/D used to store instrument setups and captured data in tape memory.

8. HP Model 9121D/S Flexible Disc Drive. Optional accessory for Model 1630G to store instrument setups and captured data in disc memory.

9. HP Model 10269A Probe Interface (for Models 1630A/D) with HP preprocessor option. HP option used to make all connections to interface the analyzer to a specific microprocessor.

10. HP Model 10269B Probe Interface (for Models 1630A/D/G) with HP preprocessor option. Second generation 10269A with added connections to interface the 1630G to a specific microprocessor.

11. HP Model 10340A modification kit to modify Models 1630A/D to a Model 1630G configuration.

The following accessories are supplied with the 1630 Logic Analyzers:

1630A:	Three 9-bit 10271A State Probes and one 8-bit 10272A State/Timing Probe.
1630D:	Three 9-bit 10271A State Probes and two 8-bit 10272A State/Timing Probes.
1630G:	Three 9-bit 10271A State Probes, one 8-bit 10272A State/Timing Probe and three 10-bit 10273A State Probes.
1630A/D/G:	One 2.3 meter (7.5 ft) power cord. One Operating and Programming Manual.

ANALYZER MEMORY

The trace memory of the analyzer is 1024 states deep. It stores each qualified state captured by the input probes. The trace memory also stores measurements of time for the timing listing so you can analyze periods between occurrences of interest.

The compare memory of the 1630A/D, and of the 1630G, (when in [Edit Compare] mode), is sixteen states deep. It can store up to sixteen lines for comparison with the corresponding lines in the trace memory. The compare memory of the 1630G, when in [Full Compare] mode, is 1024 states deep and an entire trace may be compared with the compare memory.

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Table 1-1. Specifications

Measurement Configurations

	STATE	TIMING
1630A:	35	0
	0	8
	27	8
1630D:	43	0
	0	16
	35	8
	27	16
1630G:	65	0
	0	8
	57	8

Note: Number of timing channels halved in Glitch mode.

Measurement Functions

Memory

Data Acquisition:	1024 words.
Compare:	16 words (1630A/D, 1630G in [Edit Compare] mode). Entire trace for 1630G in [Full Compare] mode.
Search:	Memory may be searched for any pattern defined within a label set. All pattern matches in memory may be marked or separately displayed.

Input Specifications

Clock repetition rate

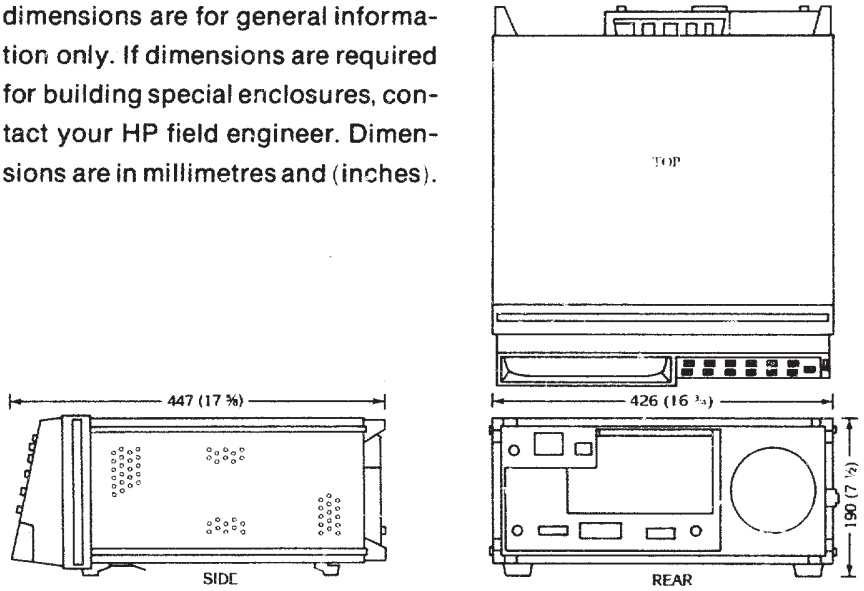
Single Phase:	25 MHz with single clock and single edge specified. 20 MHz with any ORed combination of clocks and edges.
Multiplexed:	Master Slave clock timing. Master clock must follow slave clock by at least 10 ns and precede next slave clock by 50 ns or more.
Clock Pulse Width:	≥10 ns at threshold.
RC:	100 kilohms ±2% shunted by approx 5 pF at probe body.
Setup time:	time data must be present prior to clock transition, ≥20 ns.
Hold time:	time data must be present after clock transition, 0 ns.
Minimum swing:	600 mV p-p.
Minimum input overdrive:	250 mV or 30% of input amplitude, whichever is greater.
Maximum voltage:	±40 volts, peak.
Threshold Range:	−9.9 volts to +9.9 volts in 0.1-volt increments. Accuracy 2.5% ±120 mV.
Dynamic Range:	±10 volts about threshold.
Skew:	Between channels in one pod: ≤6 ns. Between channels in different pods: ≤10 ns. (These specifications are true for input signal, VH=−1.0V, VL=−1.6V, VTH at −1.3V, slew rate greater than 0.25 V/ns.)
	Glitch: With glitch detection on, number of timing channels are halved. Minimum detectable glitch: 5 nsec width at threshold.

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Table 1-1. Specifications (Cont'd)

Operating environment

Temperature:	0° to 55° C (32° to 131° F), 20° to 30° C recommended.
Humidity:	up to 95% relative humidity at +40° C, 40% to 80% relative humidity recommended.
Altitude:	to 4600 m (15,000 ft).
Vibration:	vibrated in three planes for 15 min. each with 0.3 mm excursions, 5 to 55 Hz.
Dimensions:	dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer. Dimensions are in millimetres and (inches).



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Table 1-2. Operating Characteristics

State Mode	
Clocks:	three ORed clocks operate in single-phase or two-phase demultiplexing mode. Clock edge is selectable as positive, negative, or both edges for each clock. Different edge selections may be made on the same clock if used in each phase of the multiplexed mode.
Data Indexing	
Resources:	four terms including the Boolean NOT of each term, ALL patterns, or NO pattern. (A term is the AND combination of bit patterns in each label.) Terms may be used as often as desired.
Trigger:	up to four resource terms may be used in sequence to establish the trace parameter. The last term in the sequence may use up to four resource terms in an ORed format.
Restart:	one to four resource terms may be used in an ORed condition for a sequence-restart condition.
Store qualifiers:	one to four resource terms may be used in an ORed format. Store qualification may be separately defined for each term in the trigger sequence.
Occurrence:	occurrence of the last event in the sequence may be specified up to n = 59999.
Compare:	trace until compare "equal to" or "not equal to" is provided. The compare file is the width of the analyzer, with a depth up to 16 words in the 1630A/D and in the 1630G in the [Edit Compare] mode. When the 1630G is in the [Full Compare] mode, an entire trace may be compared. Each word in the compare buffer can have "don't cares" and can be compared anywhere in the 1024 deep memory.
Arming:	the state analyzer can be armed by the full Data Indexing capability of the Timing Analyzer.
Overview	
XY Chart:	a chart of any user-defined label can be shown. The user can change the upper and lower bounds of the chart, and all 1024 states of the memory can be simultaneously displayed.
Time measurement:	a timer can be started on completion of a sequence of up to three resource terms with restart and occurrence capability like state data indexing. The timer can be stopped and/or restarted on OR'd combinations of one to four resource terms. A histogram of the start/stop time measurement is displayed. The user can specify up to eight time ranges. Minimum time, maximum time, average time, last time, total time, and total samples are also displayed. Resolution - displayed statistics 250 ns or 0.1% of reading, whichever is greater, (4-digit display). Histogram ranges: 1 usec.
State histogram:	a histogram of any user-defined label can be shown. The user can specify up to eight labels and ranges. Maximum Count - approx 2(E63).
Time position measurement:	produces a time-varying profile of system activity. Measurements are the number of occurrences of an event per unit time. The measurement is used to understand the behavior of systems under time-varying loads.
Linkage measurement:	the relative frequency of direct transfers between module pairs are depicted in a histogram for identification of light or heavy transfer. Modifications of software may then be made to optimize program efficiency. Resolution - actual count is rounded to 0.1% (4-digit display).

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Table 1-2. Operating Characteristics (Cont'd)

Timing mode

Clock

Ranges: 10 ns to 500 ms in 1, 2, 5 sequence.

Accuracy: ±0.01%.

Data Indexing

Asynchronous pattern: 20 ns to 1 ms in 1, 2, 5 sequence with an accuracy of ±20% or 15 ns, whichever is greater.

Glitch or edge on any channels AND'd with asynchronous pattern.

Maximum time delay: approx 2(E18) times the sample period to a maximum of 9999 sec.

Arming: the timing analyzer may be armed by the full data indexing capability of the state analyzer.

Markers: time between dual markers (x and o) is displayed to accuracy of one sample period.

Expansion: X1 to X40 in 1, 2, 4 sequence. Display is a compressed representation of the 1K memory in X1 magnification. In X2 magnification, each displayed sample represents a single sample in memory.

Overview: a chart of any user-defined label can be shown. The user can change the upper and lower bounds of the chart, and all 1024 states of the memory can be simultaneously displayed.

General Characteristics

Labels

Input channel labels: up to 8 state, 16 timing, user-defined, 5-character labels may be assigned bit patterns in any configuration. Bits may be used in more than one label and need not be contiguous. Primary use is for identifying bits assigned to bus structures such as Address, Data, and Status.

User field: all labels with 4 bits or less allow mnemonics to be assigned to specific patterns. Primary use is to identify such functions as Read, Write, Op Code, etc.

Relocatable field: any single state label may be defined to have relocatable properties to facilitate viewing software modules in the format they were written. Up to 16 module starting locations may be specified, allowing trigger parameters to be based on module names, plus an offset value. An onboard calculator that operates in hex, octal, binary, or decimal facilitates general offset calculations.

Time-of-day-clock: 24-hour clock prints out time of data collection on all stored records.

Activity Markers: provided in format display for quick identification of active inputs.

Outputs

HP-IB: HP-IB connector with 8-position HP-IB switch located on rear panel. Five positions on switch are used to determine address, 2 positions used to determine TALK ONLY mode for hardcopy, or system controller.

HP-IB can be used in following environments:

1. Logic analyzer being controlled from a controller, such as HP 9826A. Maximum bus transfer rate is approximately 4K bytes per second.
2. Stand-alone hard copy on a graphics printer, such as HP 2671G.
3. Storage of user setups and measurement results on a disc memory accessory.

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Table 1-2. Operating Characteristics (Cont'd)

HP-IL:	HP-IL connector located on rear panel for HP-IL control, or for interfacing to HP 82161A, low-cost mini-cassette drive. Not required to use analyzer, but enhances analyzer operation as follows: 1. Storage of user setups and measurement results; 10 different files can be stored on one cassette. 2. When coupled with an appropriate preprocessor, allows analyzer to assume a processor-specific personality to present data in mnemonic format.
Rear-panel BNCs:	one output BNC labeled PORT, located on rear panel, with a TTL output level; high =2V into 50 ohms; low =0.4V into 50 ohms. The BNC can be programmed from the keyboard to provide the following signals: 1. Pulse on State Trace Point. 2. High until State Trace Point. 3. Low until State Trace Point. 4. High on last Sequence. 5. High on Timing Pattern. 6. Constant High. 7. Constant Low. one BNC labeled ACCESSORY POWER supplies +5V for preprocessor or logic probes.
Weight:	1630A: 12.6 kg (28 lb) net; 17 kg (38 lb) shipping. 1630D: 13.2 kg (29 lb) net; 17.7 kg (39 lb) shipping. 1630G: 13.6 kg (30 lb) net; 18.14 kg (40 lb) shipping.
Power requirement:	115/230 Vac, −22% to +10%; 275W max. 48 to 66 Hz.
Service And Calibration Support:	The 1630A/D/G contains all necessary interfaces to allow high-speed troubleshooting and calibration with automatic equipment. Guided probe techniques, utilizing signature analysis under computer control, coupled with special test instruments and fixtures allow most failures to be isolated to the component level in a minimum amount of time. After repair, full and complete calibration can be accomplished in minutes, using the same equipment. Since this integrated design can only be serviced efficiently and economically with this automated system, all major HP service facilities have installed this special equipment. This HP investment will provide you with the fastest, most complete and lowest cost repairs and calibrations. For those companies where economies of scale make in-house repair and calibration cost-effective, an option is available that provides the special hardware, software and related documentation and training to allow 1630A/D/G repair. Additional test equipment is required. Contact your local HP sales representative for further information.

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Chapter 2
Installation

INTRODUCTION

The purpose of this chapter is to describe how the analyzer is set up and the probe cables are connected for measurements in a system under test. The self test of the analyzer and messages that may be displayed during the self-test are also described.

INITIAL INSPECTION

WARNING

To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the outer enclosures of the instrument (covers and panels).

Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been inspected mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the self test, notify your nearest Hewlett-Packard Sales and Service Office. If the shipping container is damaged, or the cushioning materials show signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for inspection by the carrier.

POWER REQUIREMENTS

The 1630A/D/G Logic Analyzer requires a power source of either 115 or 230 Vac −22% to +10%; single phase, 48 to 66 Hz; 275 watts maximum power.

WARNING

This is a Safety Class I product (provided with a protective earth terminal). An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.

If this instrument is to be energized via an autotransformer for voltage reduction, make sure the common terminal is connected to the earthed pole of the power source.

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LINE VOLTAGE SELECTION

CAUTION

BEFORE CONNECTING THIS INSTRUMENT to line (Mains) voltage, be sure the line voltage switch is set correctly and that the proper fuse is installed.

If the line fuse burns out, do not replace it until the cause for failure has been determined and repaired by a qualified service person. Replacing this fuse in a damaged instrument can cause additional damage.

AC POWER CABLE

WARNING

BEFORE CONNECTING THIS INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (Mains) power cord. The Mains plug must be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two conductor outlet does not provide an instrument ground.

OPERATOR'S MAINTENANCE

The only instrument maintenance an operator needs to perform is to occasionally clean the display screen and the front panel keyboard. When cleaning the 1630A/D/G, caution must be used with which cleaning agents are used. Use a mild soap and water solution. If a harsh soap or solvent is used, the water-base paint finish will be damaged.

CAUTION

Use care when cleaning the front panel keyboard. Water can damage the keyboard circuitry if it seeps under the keys.

CAUTION

Do not use chemical cleaning agents or abrasive cleaners that may damage the plastics in this instrument. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), or a solution of 1% mild detergent and 99% water.

SITE SELECTION

Place the logic analyzer on a clean workspace which has adequate ventilation.

REAR PANEL ADDRESS SWITCH

The dip (dual-inline-package) switch on the rear panel of the logic analyzer is used to configure the analyzer for operation on the HP-IB and/or HP-IL interface buses, and to execute the self-test routine. The first five switches set the address of the analyzer for HP-IB operation. Switch six executes the analyzer self-test when set to "1". The positions of switches 7 and 8 determine the analyzer configuration on the HP-IB/HP-IL interface buses.

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1. When operating the analyzer as part of a system, set switches one through five to select the system address for your analyzer. Set switches seven and eight to select the desired system controller.

2. If operating the analyzer in a stand-alone (no external controller) configuration, with or without an external printer, set switches seven and eight to select the TALK ONLY mode (both switches to "0").

3. Set switch six to "0". Switch six is set to "1" only during the self-test.

NOTE

A switch is set to "1" when its toggle lever is up, and set to "0" when its toggle lever is down.

REAR PANEL BNC CONNECTORS

The rear-panel BNC labeled ACCESSORY POWER provides 5 volts (1 ampere maximum) for operating an external HP preprocessor interface module.

The rear-panel BNC labeled PORT provides a TTL control signal whose characteristics are selectable in the SYSTEM [Peripherals] menu for control of external measurement instruments and equipment.

CONNECTING OPERATING POWER

WARNING

Before switching the instrument on, connect all protective earth terminals, extension cords, auto-transformers, and devices to a protective earth grounded socket. Any interrruption of protective earth grounding is a potential shock hazard that could result in personal injury or death.

Use only the recommended fuse with the required current rating. Do not use repaired fuses or short-circuited fuseholders. To do so could cause severe shock or fire hazard.

CAUTION

Before switching the instrument power switch to the on positon, the line selection switch on the rear panel must be set to the voltage power source, or damage to the instrument may result.

Excessive input voltage will damage the input attenuators. Observe the maximum input rating described in table 1-1.

APPLYING OPERATING POWER

Follow these steps before applying line power to the instrument.

On rear panel:

1. Check VOLTAGE SELECTOR switch for correct setting.

2. Plug in supplied power cable.

Press front panel LINE to 1 (down position).

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SELF-TEST

The analyzer has a self test routine contained in the analyzer ROM. The self-test of the 1630A/D checks RAM, ROM, and functioning of the measurement channels within the analyzer. The self-test of the 1630G makes the same checks and also checks the HP-IB port and internal storage.

The self-test provides troubleshooting information if the analyzer is not functioning in the normal manner. If an error is displayed during the self-test, or if the self-test does not occur, contact your nearest Hewlett-Packard Sales and Service Office.

NOTE

Before initiating the self-test, disconnect any connected pods from the target system and the HP-IB cable from the rear panel of the analyzer.

To initiate the self-test, set switch 6 of the HP-IB address switch on the rear panel to "1" (switch lever up). Cycle the front panel LINE power, off and on, and the analyzer automatically executes the self-test.

1630A/D Self-Test

When the self-test of the 1630A/D has been successfully completed, the following messages are displayed on-screen:

```
PV Tests Pass
Reset Rear Panel Switch to XXXX XOXX to continue
```

If the self-test has not been successful, one or more of the following messages will appear on-screen:

```
Error in RAM
Error in ROM #n   Expected XX was YY
Acq error
  nn  nn  nn  nn  nn  nn  nn
```

1630G Self-Test

When the self-test of the 1630G has been successfully completed, the following messages appear on-screen:

```
RAM ok

ROM ok

Acquisition ok

internal storage ok

HP-IB ok


Toggle HP-IB address MSB to reset internal storage

Reset rear panel switches to XXXX XOXX to continue
```


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If an error occurs in RAM or ROM, the self-test is discontinued. When the self-test is not successful, the following messages may appear in place of any one or more of the previous messages:

Error in RAM

Error in ROM #(0-7) Expected XX was XY

Acq error:
nn nn nn nn nn nn nn nn nn nn

Internal checksum error

HP-IB failed loopback test

RESETTING INTERNAL STORAGE

When an error is detected in the checksum of internal storage during the self-test, the analyzer automatically resets internal storage. While resetting internal storage, the message "WAIT Resetting internal storage" is displayed on-screen. If the reset is successful, the message "Internal storage reset successful" is displayed on-screen. If the reset has not been successful, the message "Reset failed, internal storage has failed" is displayed.

To manually reset internal storage, toggle switch 1 of the HP-IB address switch. The message "WAIT Resetting internal storage" will appear on-screen while the reset is taking place. When the reset has been completed successfully, the message "Internal storage reset successful" is displayed. If the reset has not been successful, the message "Reset failed, internal storage has failed" is displayed on-screen. The analyzer may be used without the internal storage and the performance of the analyzer is not affected. When attempting to store information to the internal storage via the SYSTEM [Peripherals] menu, the analyzer will attempt to reset internal storage and the message "Internal storage failed power-up" will be displayed. Refer to Chapter 8 for more information about internal storage and the SYSTEM [Peripherals] menu. Inverse assemblers may not be loaded to the analyzer without internal storage.

POWER UP DISPLAY MESSAGES

When the analyzer is powered-up, it goes through a sequence of power-up routines and displays messages on the SYSTEM [Configuration] menu. The same power-up routines are performed after the self-test when the Self-Test switch on the HP-IB address switch has been returned to "0" (switch lever down).

NOTE

Reconnect HP-IB accessory instruments to rear panel HP-IB port before setting HP-IB switch 6 to "0".

During the power-up routine, the analyzer reads the HP-IB port and automatically assigns addresses to any accessories that may be connected to the HP-IB port. Addresses are assigned so duplication of addresses does not take place. Inverse assemblers and stored configurations are automatically re-loaded in the power-up sequence unless instructed otherwise in the SYSTEM [Peripherals] menu. The inverse assembler is loaded first, and then the stored configurations. The messages "Inverse assembler loaded" and "Configuration loaded" will be displayed in the lower left hand corner of the display when the internal storage checksum is correct. If on power-up, the internal storage checksum is in error, the message "Internal storage corrupt" is diplayed in the lower left hand corner of the display. The analyzer will reset the internal storage and display "Internal storage reset successful" if it was able to reset. When not able to reset, the message "Internal storage failure" will be displayed. If an inverse assembler was stored it will be lost and the message "Inverse assembler lost" will be displayed whether the internal storage failed or was successfully reset.

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CONNECTING ANALYZER TO TARGET SYSTEM

The analyzer can collect information through either HP Model 10269A/B Probe Interface or through direct connections from the general purpose probes. The procedures to be followed when making the connections will differ, depending upon which of the two types of connections are made. Refer to the procedures given in the following paragraphs for a description of how to make the connections for your particular equipment.

Connecting Analyzer Through Probe Interface

1. Install the preprocessor interface module in the probe interface.
2. Connect the ribbon cable from the probe interface (with preprocessor interface module installed) to the microprocessor in the target system.
3. Connect the probe pods from the analyzer to the appropriate pod sockets on the probe interface. Refer to the general purpose preprocessor operating note for appropriate pod connections.
4. Connect a BNC cable from the ACCESSORY POWER BNC on the analyzer rear panel to the ACCESSORY POWER (+5V) BNC connector on the probe interface.

NOTE

Some interface modules can draw up to 1 ampere from the 5-volt supply. If using coaxial cable, HP recommends using 4 feet, maximum, of type RG-58 coaxial cable to minimize voltage drop.

Connecting Probes Directly To Target System

1. Snap on the adapters for each of the general purpose probe pods.
2. Connect the line for each probe bit to monitor a node in the system under test. Leave extra lines unconnected. Do not connect signals with different threshold levels (some TTL and some ECL, for example) in the same probe pod.
3. Connect the ground probe from each pod to a ground point in the system under test.

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Chapter 3. Front Panel Controls and Menu Map

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Timing Measurements 3-1
Interactive State/Timing Measurements 3-1

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Chapter 3
Front Panel Controls and Menu Map

INTRODUCTION

This chapter consists of two figures to help familiarize the user with the operation of the 1630A/D/G Logic Analyzers. Figure 1 is the front panel keyboard of the 1630. The function of each key is described in the figure.

Figure 2 is a map of the available menus by selection with the INPUT or OUTPUT DISPLAYS keys at the top of the front panel keyboard. In general, making state, timing or interactive state and timing measurements may be accomplished by the following steps:

State Measurements

- Start with the SYSTEM Specification [Configuration] menu. (power-up or press SYSTEM)
- Configure for state analysis by selecting all channels for state measurements. (use ROLL keys)
- FORMAT the input data by assigning labels to groups of probe bits. (press FORMAT)
- Specify the TRACE to be collected by the state analyzer. (press TRACE)

Timing Measurements

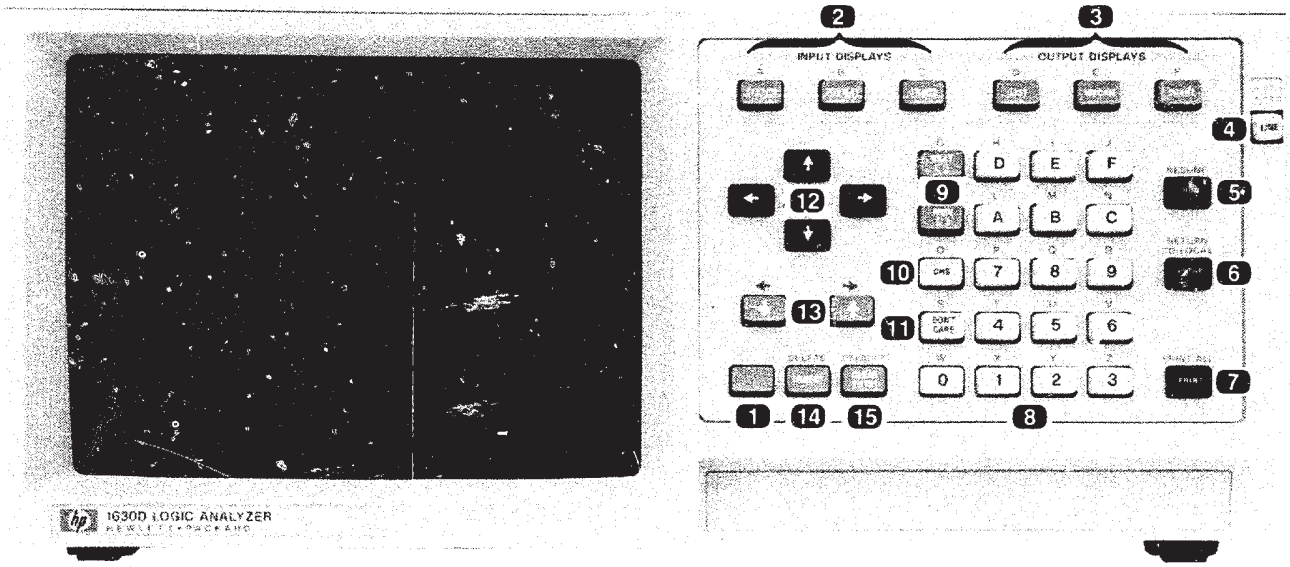
- Start with the SYSTEM Specification [Configuration] menu. (power-up or press SYSTEM)
- Configure for timing analysis by selecting timing channels and glitch mode (on or off).
- FORMAT the input data by assigning labels. (press FORMAT)
- Specify the TRACE to be collected by the timing analyzer. (press TRACE)

Interactive State/Timing Measurements

- Start with the SYSTEM Specification [Configuration] menu. (power-up or press SYSTEM)
- Configure for interactive measurements by selecting a combination of state and timing channels.
- FORMAT the input data by assigning labels to both state and timing pods. (toggle FORMAT)
- Specify the TRACE to be collected by the timing and the state analyzers. (toggle TRACE)

Chapters 4 through 8 contain step-by-step procedures for setting up the specific menus.

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Blue key. This key activates the blue SHIFT function assigned to each keyboard key. A momentary press activates the SHIFT function for the next keystroke. The SHIFT function will continue as long as you keep the blue key pressed.

2 INPUT DISPLAYS. Three keys that select sets of 1630A/D/G menus. SYSTEM calls up menus that define the instrument configuration, set up secondary configurations and outputs for peripherals, and control tape or storage operations (when a tape or disc drive is connected and active). FORMAT has three menus that determine how data is collected and interpreted on the display. TRACE has a series of menus that specify the measurement mode and parameters for collecting data.

3 OUTPUT DISPLAYS. Three keys that select a state display (LIST), timing display (WFORM), or performance overview chart (CHART).

4 LINE. Turns on operating power.

5 RUN. Initiates a new measurement; RESUME continues an incomplete measurement that was halted by pressing the STOP key.

6 STOP. Terminates a measurement or print out; RETURN TO LOCAL overrides an HP-IB or HP-IL controller to return control of the analyzer to the keyboard.

7 PRINT. Commands the current display content to be printed on an HP-IB graphics printer; PRINT ALL prints the entire content of a displayed menu or, when a list is displayed, prints the entire trace list (including all off-screen information) from the on-screen information to the the end of trace memory.

8 Hex keyboard for data entry.

9 NEXT[ ] and PREV[ ] keys cycle through all the menu selections available for fields enclosed in brackets, [ ].

10 CHS. Used to change +/– signs when specifying memory locations in either direction from the trigger event, and when specifying polarities. This key will also print a dash when used in a text field.

11 DON'T CARE. enters an "X" in lieu of a number, to indicate "any value will serve". When used in a text field in lieu of a letter, enters a space.

12 CURSOR. These keys move the cursor from field to field in the menus. The blue SHIFT function allows these keys to rearrange the order of labels in the menus, and to move the cursor from pod to pod in the label lines of the FORMAT [Assignment] menu. The CURSOR keys can also move the configuration bar in the SYSTEM [Configuration] menu, and the "x" and "o" markers on the waveform and chart displays.

13 ROLL keys move timing displays left or right, state lists up or down, and the configuration bar in the SYSTEM [Configuration] menu.

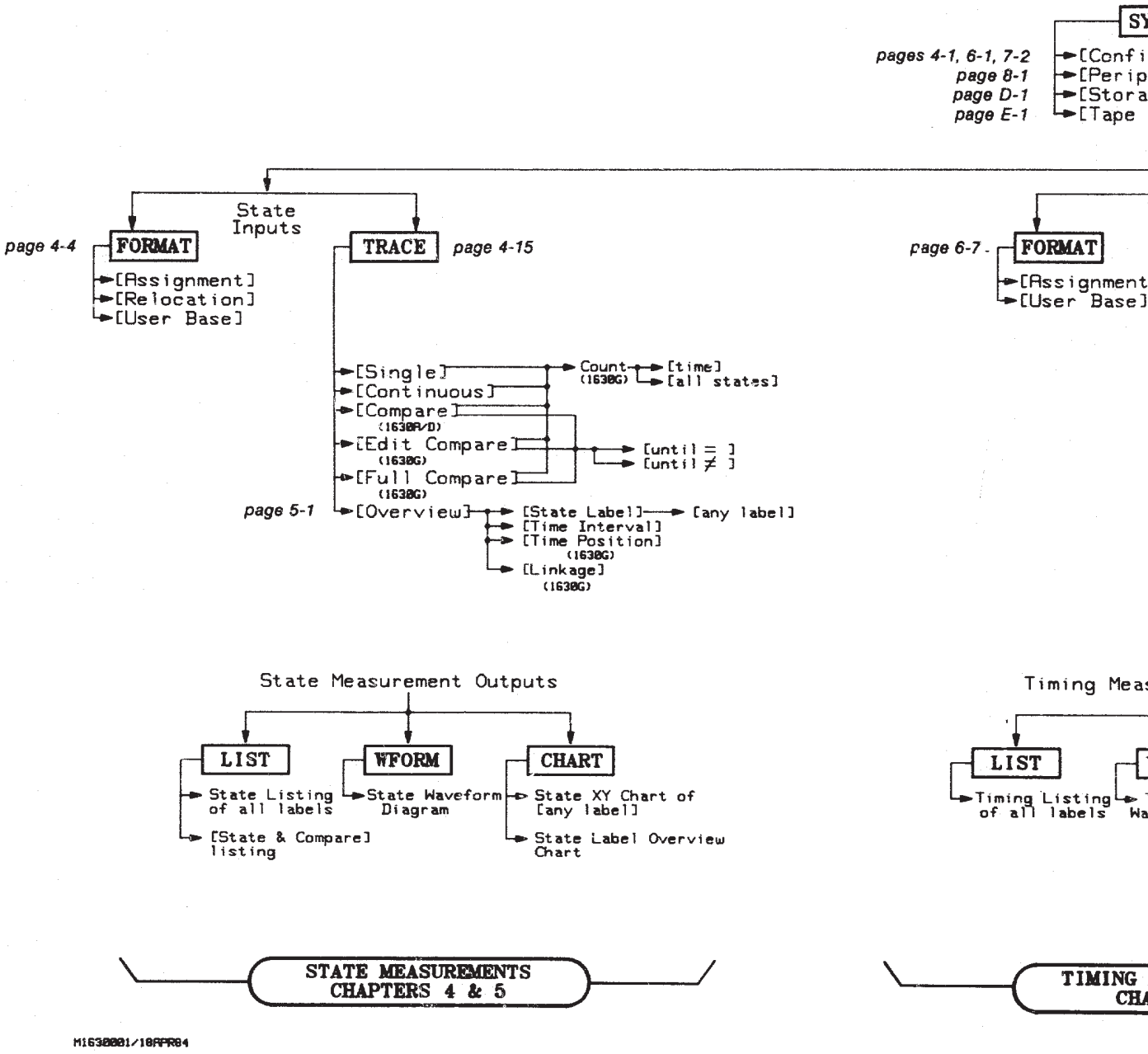
14 INSERT/DELETE are used to add or delete fields and labels.

15 CLEAR ENTRY. This is the field eraser key; DEFAULT returns all fields in the displayed menu to their power-up conditions.

Figure 3-1. 1630 Front Panel Controls

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INPUT/OUTPUT DISPLAYS MENU MAP



M1630001/10APR84

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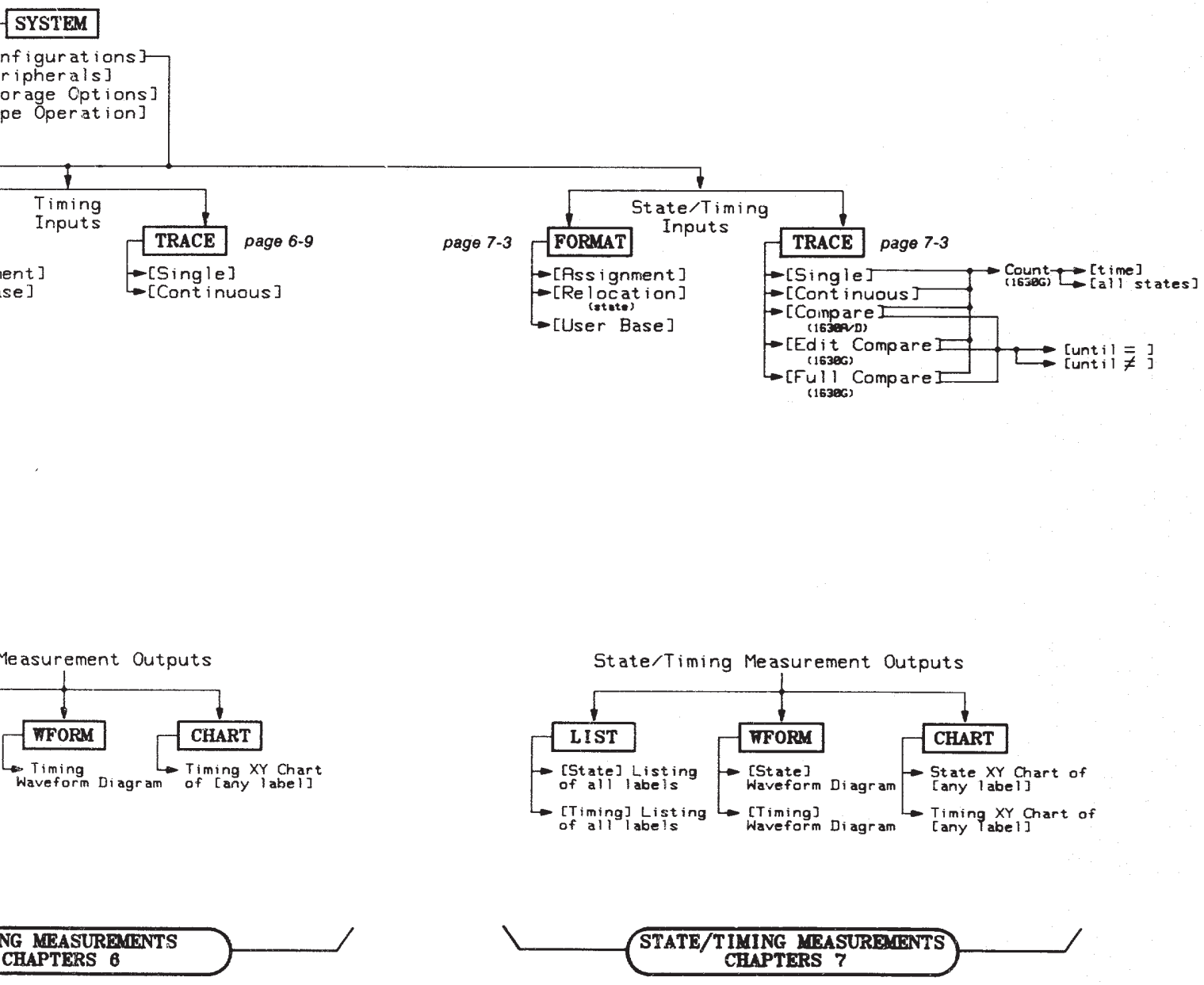


Figure 3-2.
Input/Output Displays Menu Map

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Chapter 4
State Measurements

INTRODUCTION

The 1630A/D/G Logic Analyzers are capable of capturing large quantities of data. To make this data useful, the incoming data needs to be formatted in an arrangement that is easily comprehensible. This is accomplished with the 1630A/D/G analyzers by grouping the incoming lines and labeling the groups for the typical connections for the address, data, status, and other lines of interest. Incoming data may be further identified by assigning user defined labels for conditions rather than the provided bases of hexidecimal, binary, or ASCII. Another type of user base may be assigned in which relocatable code is labeled by the user.

The next step in making the captured data useful is to edit the data before it is stored by the analyzer. Selective tracing techniques are used for recognizing and storing only qualified data. The 1630A/D/G Logic Analyzers provide a trace specification menu in which resource terms may be identified for selective tracing. Resource terms may be specified for simple triggering, sequence triggering, sequence restart, and store qualifying.

The target system used throughout this manual for examples is the HP Model 5036A Microprocessor Lab which contains an 8085 microprocessor. All traces shown in the figures are from the 5036A.

CAPTURING A STATE TRACE

1. Make all the required connections to the target system. Information for connecting the probes, directly or through an interface, is in chapter 2 of this manual.

2. Apply operating power to the logic analyzer and to the target system.

NOTE

When using a preprocessor, be sure to apply power to the analyzer first or the target system may not run.

The logic analyzer will execute power-up sequences and display the system menu in the default configuration. The 1630G will also display messages indicating what is being loaded from internal storage when it has been instructed to load internal configurations or an inverse assembler. See Power-up Display Messages in chapter 2 for more information on the power-up sequence and messages. The default system configuration assigns all channels to state measurement and none to timing measurements. Figures 4-1a and 4-1b are the default System Specification menus for the 1630D and 1630G. The 1630A default System Specification menu has eight less channels than the 1630D. Power-up display messages will appear on the display only when the analyzer is powered up.

3. Press RUN. The logic analyzer will execute a single trace and display a State Listing in hexadecimal. The measurement ensures the logic analyzer is connected to the target system and the target system is running. Figures 4-2a and 4-2b are examples of the state traces that will be displayed when collecting a free-run trace with the logic analyzer. The State Listing for the 1630G has more columns than the 1630A/D because it has more state channels and a counting function.

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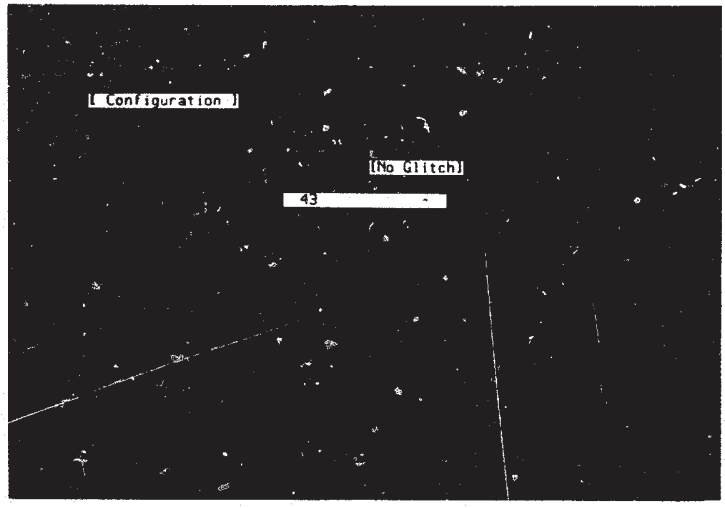


Figure 4-1a. 1630D Default System Specification Menu

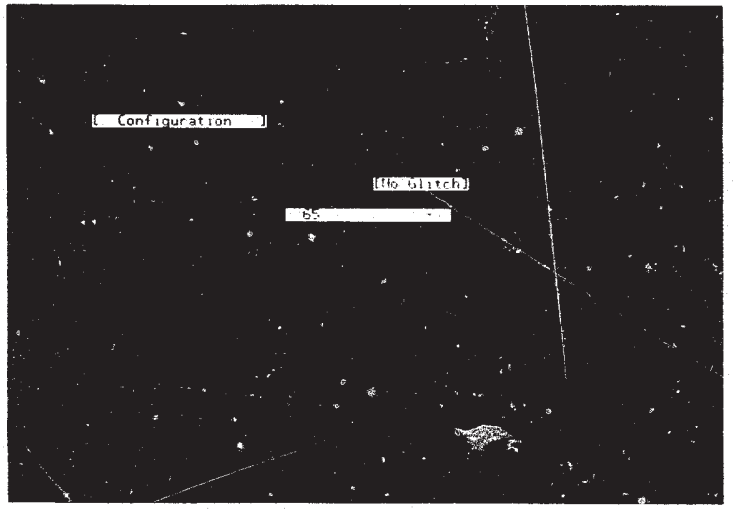


Figure 4-1b. 1630G Default System Specification Menu

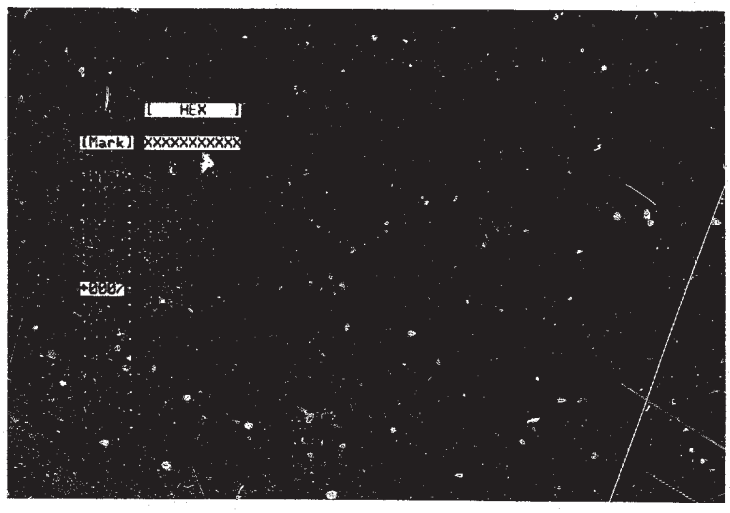


Figure 4-2a. Free-run State Trace Captured by the 1630A/D

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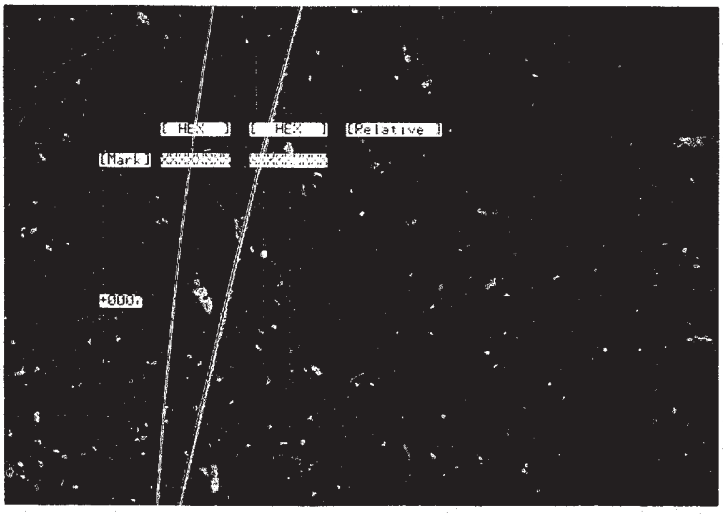


Figure 4-2b. Free-run State Trace Captured by the 1630G

NOTE

The figures in this manual apply directly to the display of the 1630G, unless titled otherwise. Therefore, when illustrating state listings the figures will appear different than the display of a 1630A/D. The 1630A/D does not have a time tagging function.

4. In the State Listing, the blinking cursor is in the first column of the field next to Base. When the cursor is in a field enclosed in brackets, [ ], the NEXT[ ] and PREV[ ] keys are used to select available parameter choices for that field. Use the NEXT[ ] and PREV[ ] keys to cycle through the parameters available for number bases. Each time one of the two keys is pressed, the data in the column changes to the new number base and all columns are shifted to accommodate number bases requiring more characters. To return the columns to the original position, press the blue shift key in the lower left corner of the of the keyboard panel and the ROLL left or right key, as required.

NOTE

The blue shift key enters the alternate function/character shown in blue above each key. When the blue key is pressed the next key pressed will enter the blue alternate function/character. The blue key may be held down for repeated entries.

Use the blue key and the ROLL keys to move the entire display area left and right.

Use the blue shift key and LABEL arrow keys to move entire labels or, when the cursor is within a label field, the blue shift key and an arrow key may be used to move the cursor to the first position in the next field of the label.

NOTE

In the upper right hand corner of the display, arrows indicate the keys that may be used to control the display. The arrows indicate the CURSOR left, right, up, or down keys and the ROLL up or down keys.

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THE STATE FORMAT SPECIFICATION

The State [Assignment] Format Specification

The logic analyzer must acquire data from the target system in exactly the same manner as the target system interprets the data. Therefore, the clock assignments and voltage thresholds utilized by the system must also be used by the logic analyzer. The logic analyzer must see the exact information that the target system sees. The type of information is specified in the analyzer with the State [Assignment] Format Specification menu. The State [Assignment] Format Specification menu is also used to group incoming channels and assign names (labels) to the groups. Assigning labels to groups (such as the address, data and status channels) makes the data displayed on the logic analyzer much easier for the user to interpret and analyze.

Figures 4-3a and 4-3b are the default State Format Specification menus that are displayed on the 1630A/D and 1630G when the FORMAT key is pressed. When the analyzer runs a trace, only probe channels assigned to a label are displayed in the listing. All channels on the 1630A/D are defaulted to label "A". The 1630G assigns channels from pods 5, 6, and 7 to label "A0" and channels from pods 1 through 3 to label "A1". All probe channels are initially assigned to a label so when a trace is listed, all channels are included in the listing. All channels not connected are indicated by a zero in the State Listing.

NOTE

The arrows at the left and right of the label fields in figure 4-3b indicate there are more bits assigned to the left of label A0 and to the right of label A1.

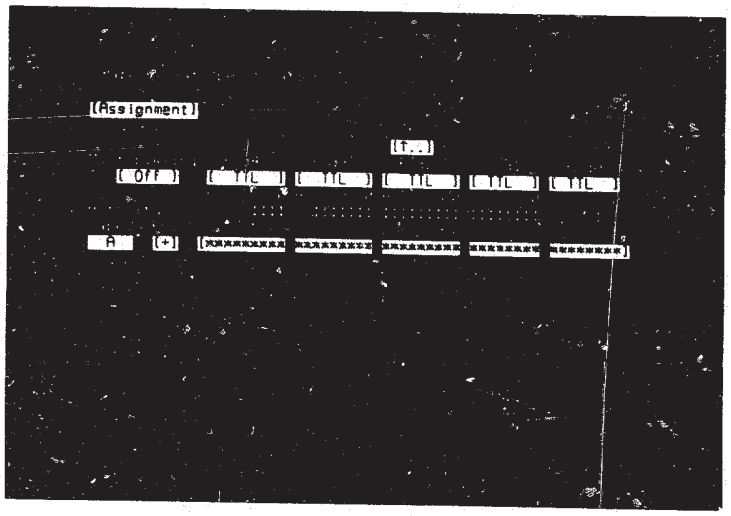


Figure 4-3a. 1630A/D Default State Format Specification Menu

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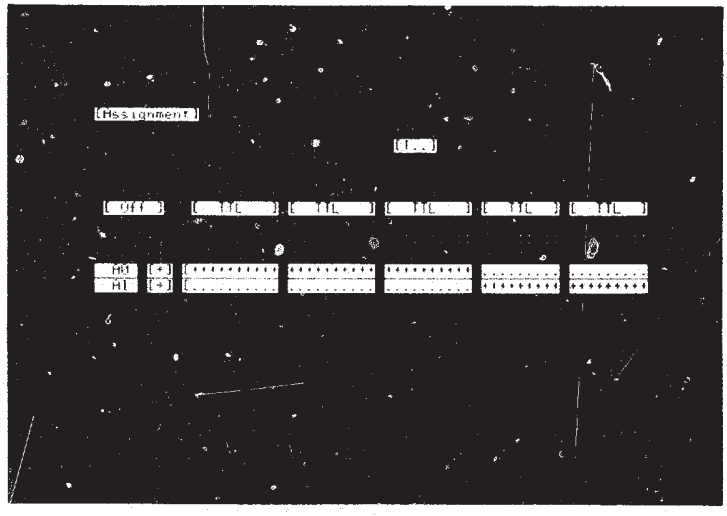


Figure 4-3b. 1630G Default State Format Specification Menu

CLOCK ASSIGNMENTS

The logic analyzer must recognize data on the same clock edge as the target system when taking state measurements. Three OR'ed clocks are available in the State [Assignment] Format Specification. The default clock assignment specifies to the analyzer to collect data on the positive edge of the J clock. Other clock specifications may be made by moving the cursor to the OR'ed clock field on the assignment menu and using the NEXT[ ] or PREV[ ] keys to select different clocks and edges.

MULTIPLEX ASSIGNMENT

Some target systems may use multiplexing in which certain signal lines are used for different information at different times. In the target system used for the examples in this manual, the data bits and eight lower address bits are multiplexed on the same pins of the microprocessor. The logic analyzer can demultiplex these lines so the data and address will be listed in separate columns in the state listing. To set the multiplexing mode on, move the cursor to the field under Multiplex (Multiplexing on 1630 A/D) in the State [Assignment] Format Specification and press the NEXT[ ] or PREV[ ] key. The multiplex choices are displayed in ratios that indicate the number of channels to be processed by the slave/master clocks. The slave clock moves information to a holding register and the master clock puts both sets of information into the logic analyzer memory. When multiplexing is on, edges for the master and slave clock are automatically assigned. To change clock assignments, move the cursor to the clock field and use the NEXT[ ] or PREV[ ] keys to select different clocks and edges.

For the target system used in examples for this manual, the multiplex field is set to [27/16] on the 1630A/D and to [27/38] on the 1630G. These are the typical settings for 8-bit microprocessors that multiplex data and address lines in the same manner as the 8085. For 16-bit microprocessors that utilize multiplexed lines, demultiplexing is usually set at 18 channels for the slave clock instead of 27.

THRESHOLD ASSIGNMENTS

Input threshold levels are selectable for each pod. The threshold is selected by moving the cursor into the field under an individual pod and selecting TTL, ECL, or absolute voltages between –9.9V and +9.9V. The threshold level determines whether the incoming voltage will be recorded as a logic 1 (if above the threshold) or a logic 0 (if below the threshold level).

NOTE

All probe connections within a pod are assigned the same threshold level.

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ACTIVITY LINE

The activity line under each pod in the State [Assignment] Format Specification indicates the channels on which voltage changes are taking place. A double-ended arrow indicates an active channel (>400 Hz) and a single bar indicates a steady state, either high or low.

LABEL ASSIGNMENTS AND POLARITY

1. Move the cursor to the label column in the State [Assignment] Format Specification menu. A message will appear on the display screen indicating a new label may be added. Press INSERT and a new label field will be added. Labels are entered with numeric keys and/or the blue shift key and the alphabetic characters. Up to eight labels may be assigned and each label may consist of up to five characters. (Labels are deleted by pressing the blue shift key and and DELETE when the cursor is anywhere on the line of the label to be deleted.)

2. Add the label ADDR to the label column in the new field. Notice the field to the right of the label field. By using the NEXT[ ] or PREV[ ] key, + or − may be selected to indicate whether a voltage above the threshold voltage is to be displayed as a 1 or 0. A + in this field indicates voltages above the threshold are 1 and voltages below are 0. Choosing − gives the opposite display.

NOTE

Polarity choice does not affect the waveform display.

3. Press and hold the CURSOR right arrow to move the cursor across the label field to bit 6 of pod 3. This is the MSB (most significant bit) of the address channels connected to the analyzer.

NOTE

Pod2 will be off-screen in the 1630G format menu, use the ROLL keys for bit-by-bit shifting of the pods, or the blue shift key and the ROLL keys to shift entire pod displays.

4. Press either NEXT[ ] or PREV[ ] key sixteen times, or hold either key down, until sixteen asterisks appear in the entries beneath Pod3 and Pod2. The asterisks assign the corresponding probe bits to the label designated ADDR.

5. Press LIST. The bits that are assigned to the label ADDR are now listed in a new label column, ADDR, in the State Listing. Figure 4-4 is the state listing with the address bits assigned to the label ADDR.

NOTE

When a trace is run, data is acquired on all connected channels (assigned to a label or not). The format may be modified and new information may be displayed without taking a new trace. Acquired data may be manipulated by changing the format menu.

6. Press FORMAT and add labels for DATA lines and STAT (status) lines the same way the ADDR label was added. Assign the appropriate bits (as connected in chapter 2) to the added labels.

NOTE

The bits assigned to labels need not be physically adjacent. Bit 2 in Pod1 may be combined with bit 5 in Pod3 for assignment of a single label consisting of the two probe channels.

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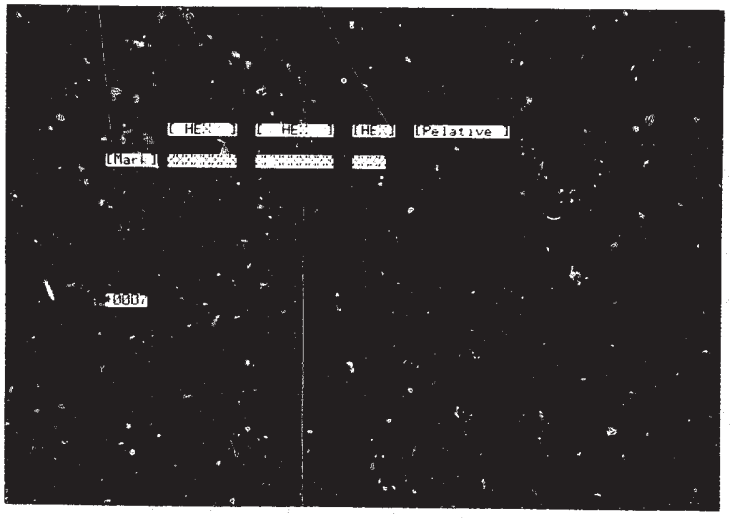


Figure 4-4. 1630G State Listing Including the ADDR Label

7 Move the cursor to the label A on the 1630A/D, or to labels A0 and A1 on the 1630G, with the CURSOR arrow keys. Press the blue shift key and DELETE to remove labels A, A0, and A1 from the State Format Specification. Figures 4-5a and 4-5b are the State [Assignment] Format Specifications for the 1630A/D and 1630G with the appropriate probe bits assigned to labels ADDR, DATA, and STAT.

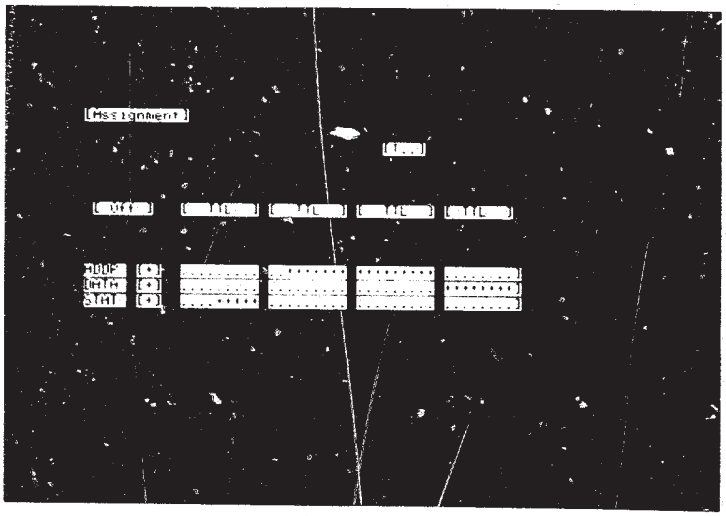


Figure 4-5a. 1630A/D State [Assignment] Format Specification Menu

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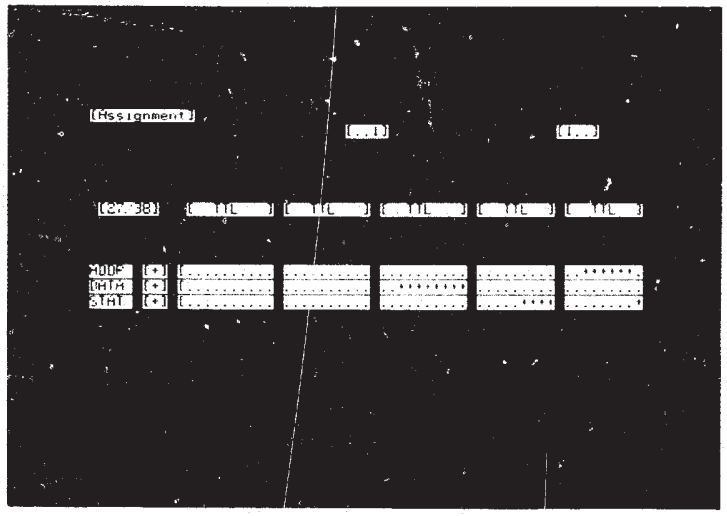


Figure 4-5b. 1630G State **[***Assignment***]** Format Specification Menu

NOTE

The format specification in figure 4-5b is for the target system, with a 8085 microprocessor, being used for the examples in this manual. All assignments pertain to the 8085 including the clock and multiplex assignments.

8. Press LIST and see that all assigned labels now appear in the state listing and the default labels (A, A0, and A1) are no longer displayed, as in figures 4-6a and 4-6b. The State Listing makes more sense now and the list is easier to analyze. The number base for any label may be changed by moving the cursor to the base field under the label and using the NEXT**[ ]** or PREV**[ ]** keys to select different bases.



Figure 4-6a. 1630A/D State Listing for ADDR, DATA, and STAT Labels

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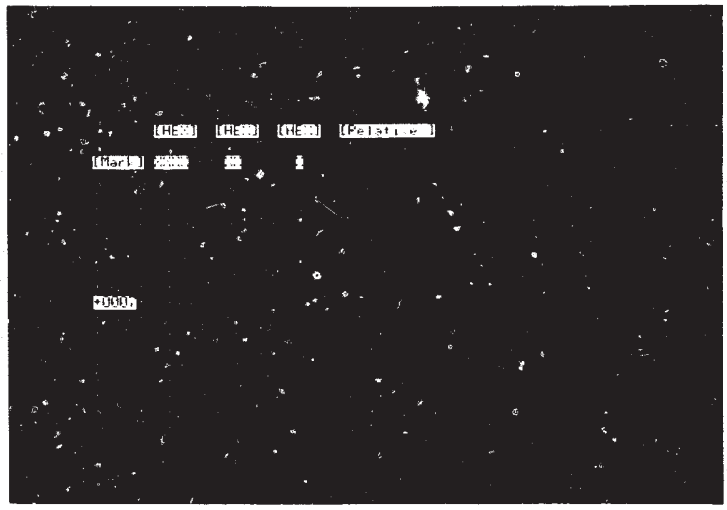


Figure 4-6b. 1630G State Listing for ADDR, DATA, and STAT Labels

NOTE

The differences in the State Listings of figures 4-6a and 4-6b are due to the format specifications in figures 4-5a and 4-5b. The data in the listing of figure 4-6b is the correct data for the 8085 because demultiplexing of the data and address lines has been specified.

9. Channels are not restricted to a single label, they may be assigned to two or more label groups. Press FORMAT and add a new label, MIX, as in figure 4-7. Assign all the STAT bits, the last four ADDR bits and the first four DATA bits to the label MIX. Steps 2 through 6 describe how to add a new label and assign bits.

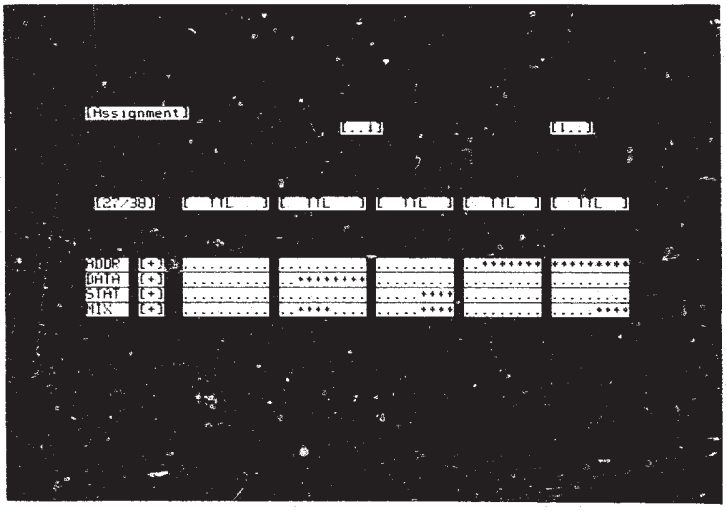


Figure 4-7. State Assignment with Bits Assigned to Multiple Labels

10. Return to the State Listing by pressing the LIST output display key. The label MIX has been added to the display as shown in figure 4-8. The characters under the MIX label are the MSB (most significant bit) of DATA, STAT, and the LSB (least significant bit) of ADDR.

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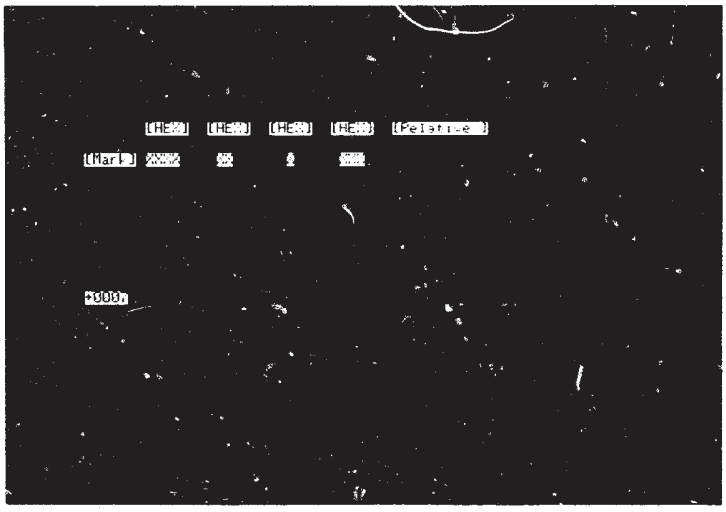


Figure 4-8. State Listing With Bits Assigned to Multiple Labels

11. The MIX label has no purpose at this time, but assigning bits to more than one label can be helpful in troubleshooting. To remove the label, return to the State [Assignment] Format Specification menu by pressing FORMAT. Move the cursor anywhere on the MIX label line. Delete the entire line by pressing the blue shift key and DELETE.

The State [Relocation] Format Specification

The State [Assignment] Format Specification provides a means to group the incoming channels to the logic analyzer into meaningful labels to make reading the display easier. These labels may be further grouped and labeled to make the display even easier to analyze. In the following steps, the address ranges in the label designated ADDR in the State [Assignment] Format Specification are grouped and given module names.

The target system has four operations that we want to label: a keyboard checking routine, a timing routine, stack operation, and OUT addresses for scan and display. Each routine has a starting address and uses a known number of addresses, however, there is unknown code in the addresses between the routines to be labeled. Table 4-1 is a listing of the routine modules with starting addresses and the known amount of addresses used for each module.

Table 4-1. Address Map for Relocation Example

Named Module	Starting Address	Addresses Used
KEYBD	01D0	0012H
TIME	0429	001EH
STACK	0BB0H	0050H
SCAN	2828H	0001H
DSPLY	3838H	0001H

1. Press FORMAT. The State [Assignment] Specification menu will be displayed. Change [Assignment] to [Relocation] by using the NEXT[ ] or PREV[ ] key. Relocation applies to any label previously defined in the State [Assignment] Specification.

2. Figure 4-9 is the default State [Relocation] Format Specification menu. Since ADDR is the first label assigned in the [Assignment] specification, it is shown in the label field. Move the cursor to the label field and cycle through the labels available for relocation by using the NEXT[ ] or PREV[ ] key.

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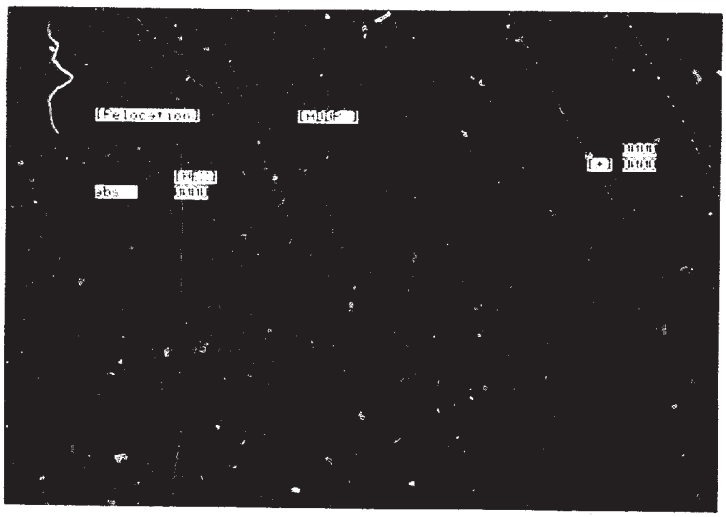


Figure 4-9. Default State [Relocation] Format Specification Menu

3. Select [ADDR] for the label field. Only one label at a time may be used in the [Relocation] mode. By naming ranges in the [ADDR] label, routines that are executing may be identified in the State Listing.

4. Move the cursor to the abs 0000 field in the Module Name column. Enter the module name KEYBD and the starting address value in the next column.

   a. Move the cursor to the first field under Calculator and enter the starting address for the module name.

   b. Move the cursor to the middle field of Calulator and enter the number of addresses used for the module.

   c. The last number in the Calculator field shows the first address of unnamed code after the module. Use this address as the starting address of the next module name.

5. There is code between the modules KEYBD and TIME which can be labeled module A to differentiate it from the KEYBD and TIME modules. Move the cursor to the Module Name column and add module A. Use the address determined by the calculator for the starting address.

6. Continue to INSERT the rest of the code modules until the State [Relocation] Format Specification looks like figure 4-10.

7. Press LIST. Change the base field for ADDR with the NEXT[ ] key to [REL+HEX]. Now the state list for the ADDR label includes the relocatable module name and the offset addresses referenced from the beginning of the module (in hexidecimal base). The new state listing is shown in figure 4-11. In figure 4-11 the trigger is now TIME+0010 which means the trigger is located 10 addresses into the TIME module.

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Figure 4-10. State [Relocation] Format Specification With Assigned Modules

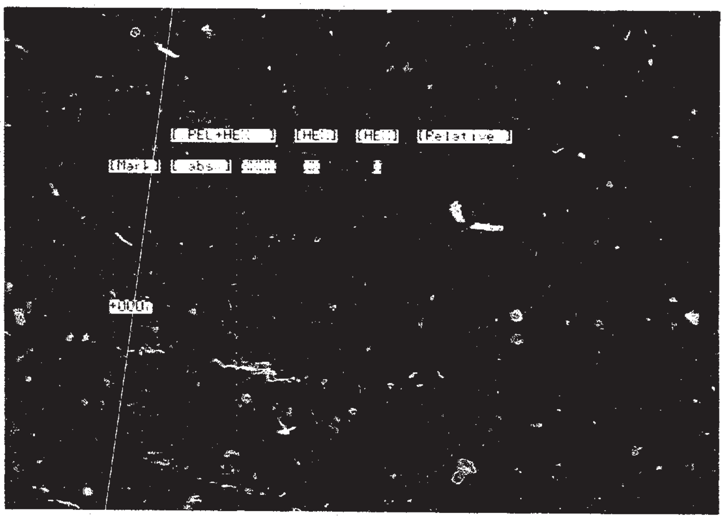


Figure 4-11. State Listing Using Relocation Values

8. A comparison of the relocatable code modules and the absolute hexidecimal values, two columns of the same states, may be made

   a. Press FORMAT twice to return to the State [Assignment] Format Specification menu.

   b. INSERT a new label, ADDR1, and assign all address probe bits to the label.

   c. Press LIST and both lists for the address bits will be displayed in the state listing as in figure 4-12.

NOTE

For easy comparison of lists, the ADDR1 list may be moved to the right of ADDR. Move the cursor to the ADDR1 label field and press the blue shift key and then the LABEL CURSOR left key.

9. Similar relocation ranges and names may be assigned to the other labels from the State [Assignment] Format Specification.

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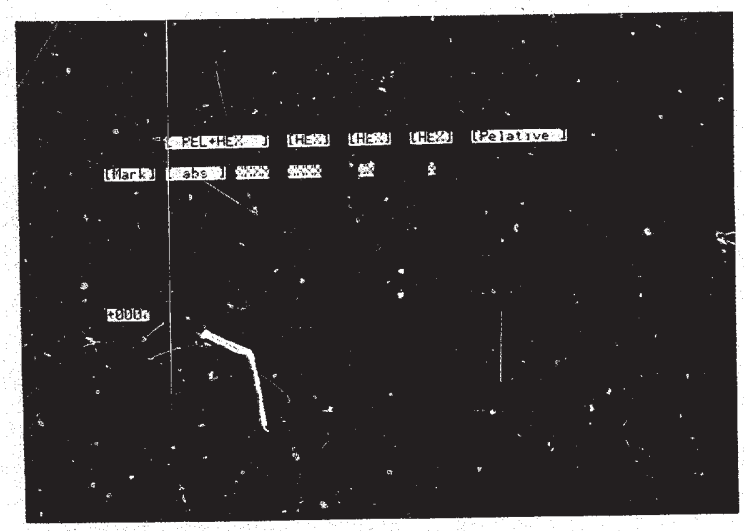


Figure 4-12. State Listing With Relocation and Absolute Value Lists

The State [User Base] Format Specification

The State [User Base] Format Specification is used to assign user defined names to conditions on control and status lines. The user base names may then be displayed on the state listing in place of the numeric values to make the data on the display easier to interpret.

Only labels with four probe bits or less may be assigned user base names. The maximum amount of user base conditions for each label is sixteen. All labels that have been assigned in the State [Assignment] Format Specification may have user base names assigned providing four or less bits are assigned to each label. The user base names may be any of 1 to 5 alphanumeric characters.

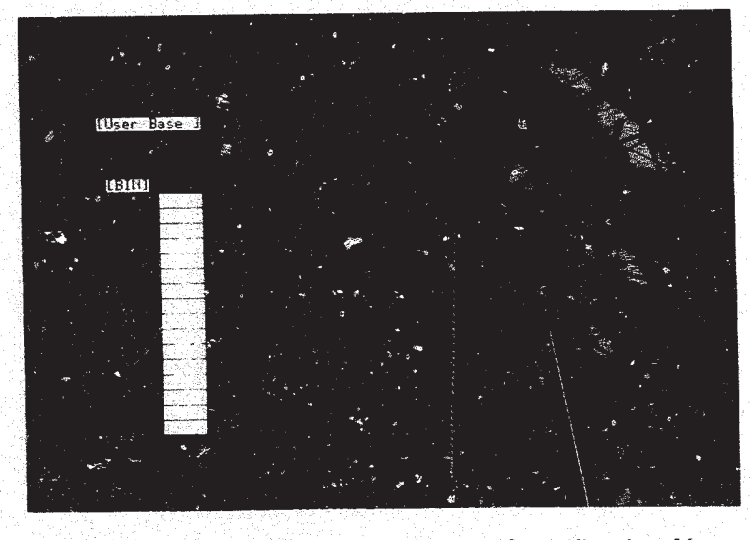


Figure 4-13. State [User Base] Format Specification Menu

1. Press FORMAT and select [User Base] with NEXT[ ] or PREV[ ] key. STAT is the label from the assignment specification with four or fewer probe bits assigned to it and is automatically displayed in the State [User Base] Format Specification menu, shown in figure 4-13. Since there are four bits assigned to the label, STAT, there are sixteen possible conditions that may exist in the STAT label. When the 8085 is executing instructions, there are six basic types of operations that are performed. The six operations, the STAT label binary conditions, and the user base names to be assigned are listed in table 4-2.

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Table 4-2. User Base Names for STAT Label

8085A Operation	User Base Name	Binary Value
Read from memory	MEMRD	0001
Write to memory	MEMWR	0010
Read from input	IO-RD	1001
Write to output	IO-WR	1010
Opcode fetch	OPFCH	0011
Interrupt acknowledge(transferring control to another location)	INTAK	1011

2. Assign the STAT label codes to the appropriate conditions in the State [User Base] Format Specification as shown in figure 4-14.

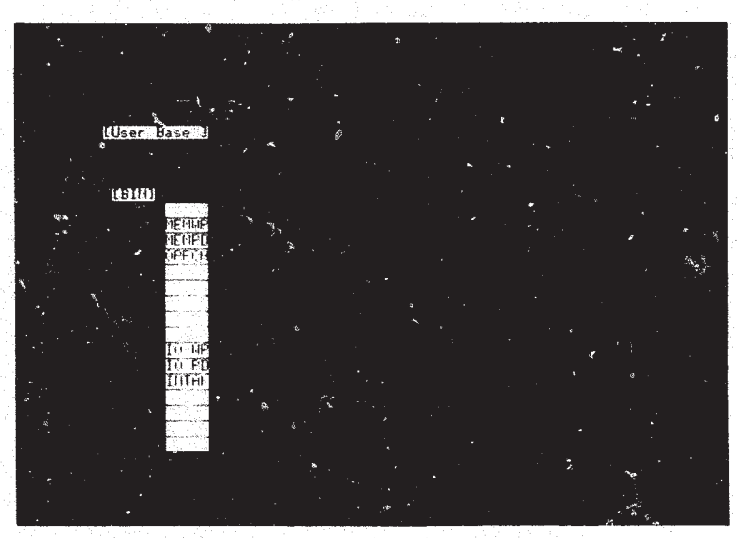


Figure 4-14. User Base Specification With Assigned Conditions to STAT Label

3. Press LIST. Move the cursor to the base field under the STAT listing and press the NEXT[ ] key twice. The STAT listing is now in the user base names, as in figure 4-15, instead of numeric values.

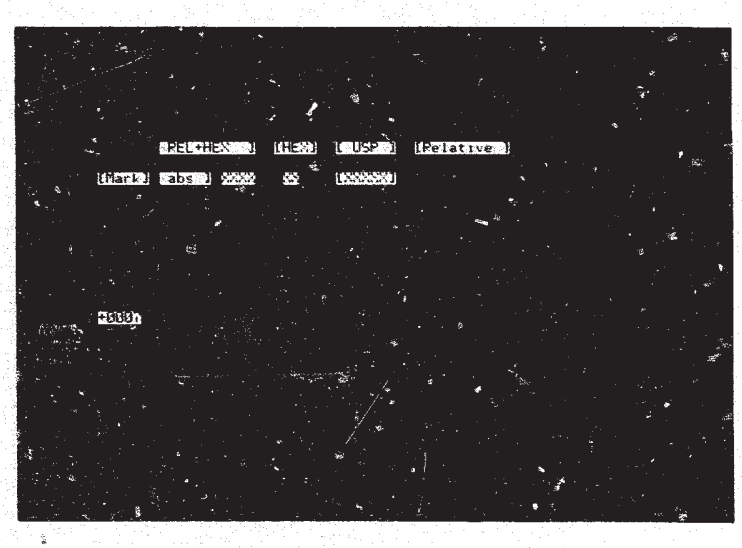


Figure 4-15. State Listing With User Base Names in STAT List

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INVERSE ASSEMBLERS FOR THE LOGIC ANALYZER

Inverse assemblers display the data from the target system on the logic analyzer screen in mnemonics similar to those of the microprocessor in the target system. Figure 4-16 is a state listing after the data from the system used for examples in this manual has been disassembled with the 8085 Inverse Assembler.

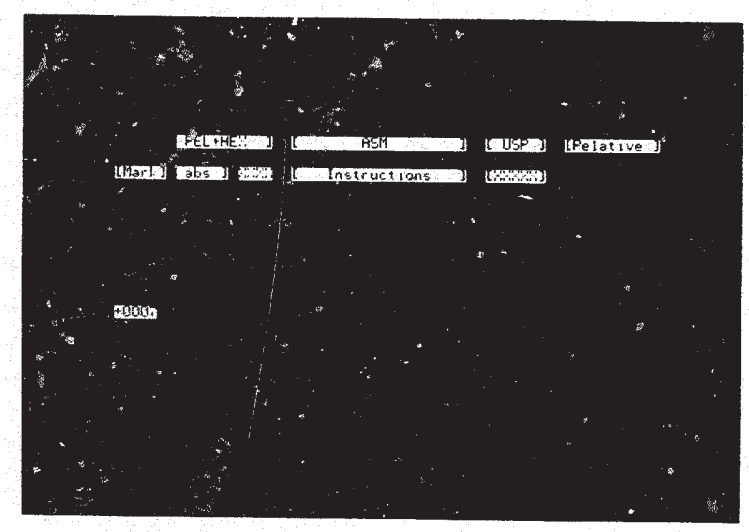


Figure 4-16. State Listing With Disassembled Data List

The inverse assembler file automatically sets up the State [Assignment] Format Specification and, in some inverse assemblers, the State [User Base] Format Specification.

When an inverse assembler has been loaded into internal storage, it is automatically reloaded upon power-up of the analyzer. The message "Inverse assembler loaded" will be displayed on the System [Configuration] Specification menu at power-up. Refer to Appendix D for information about loading and storing inverse assemblers.

Inverse assemblers are available, for many of the widely-used microprocessors, on minicassette or floppy disc. Refer to the appropriate appendix included in this manual for information on using an HP 82161A Digital Cassette Drive or an HP 9121D/S Flexible Disc Drive with the 1630A/D/G.

Most of the inverse assemblers available for use with the 1630A/D/G come in versions for HP 10269A/B Interface Module and for direct connection with individual probe connections. Refer to the operating note supplied with each inverse assembler for instructions about connections to the logic analyzer.

THE STATE TRACE SPECIFICATION

The Trace Specification determines where the logic analyzer starts a trace and what kind of information is collected in the trace. The logic analyzer can take [Single] or [Continuous] traces, [Compare] lists before storing a data, or perform [Overview] performance analysis measurements.

1. Press TRACE. The default State Trace Specification menu is shown in figure 4-17. In the default mode, the analyzer will take a single trace starting at the first occurrence of any state of the target system. All states thereafter will be stored until 1024 states are captured. The analyzer then automatically displays the stored trace.

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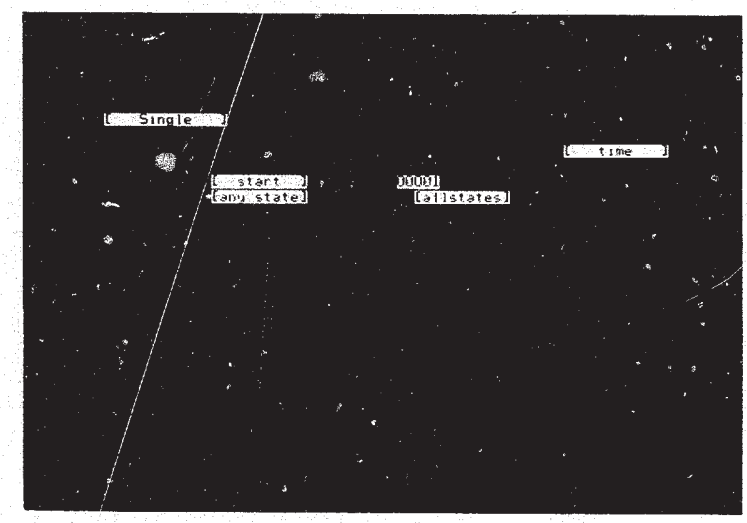


Figure 4-17. 1630G Default State Trace Specification Menu

2. Use the NEXT[ ] key and select the [Continuous] mode. Press RUN and the analyzer will perform series of trace measurements. At the completion of each measurement, the analyzer updates the display and starts a new trace measurement. The traces measurements continue until the STOP key is pressed. The time tagging list is not displayed during continuous traces, but is displayed when STOP is pressed and a single trace is taken.

NOTE

When STOP is pressed once, the analyzer completes and displays the measurement presently in progress. If STOP is pressed twice, the trace measurement is aborted and any states captured are displayed in the listing.

3. Press TRACE again and return to the [Single] trace mode by using the PREV[ ] key.

NOTE

Steps 4 and 5 apply only to the 1630G, the 1630A/D does not have the time tagging function.

4. Move the cursor to the Count field in the State Trace Specification menu. There are two choices available in the Count field for time tagging purposes. The default of the count function counts the time between each state in the state listing. This is displayed in the Time column of the state listing and may be seen in any of the previous figures of state listings of the 1630G. The 1630G can count states rather than time when the Count field specification is changed to [all states]. Figure 4-18 is a state listing when states are counted rather than execution time. States between and including each state in the state listing are counted.

   The time tagging function has many useful applications such as: measuring time between calls to a routine, looking at the time between writing to an I/O port, or capturing the time a routine takes to execute.

5. Move the cursor to the States field in the State Listing of the 1630G. Use the NEXT[ ] or PREV[ ] key to see how the analyzer can display the States (or Time) list in absolute or relative values. Figure 4-19 is the State Listing with the State list in absolute values. In the [relative] mode, counting is relative to the previous state. In the absolute mode, counting is relative to the trigger.

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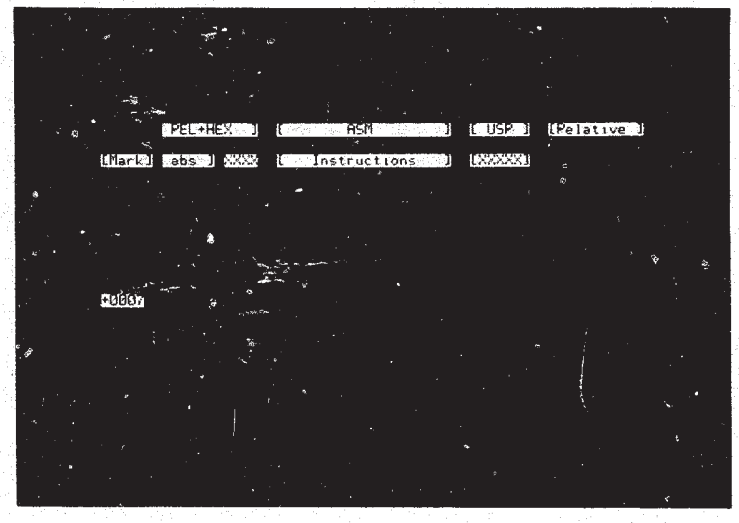


Figure 4-18. 1630G State Listing With Count States List

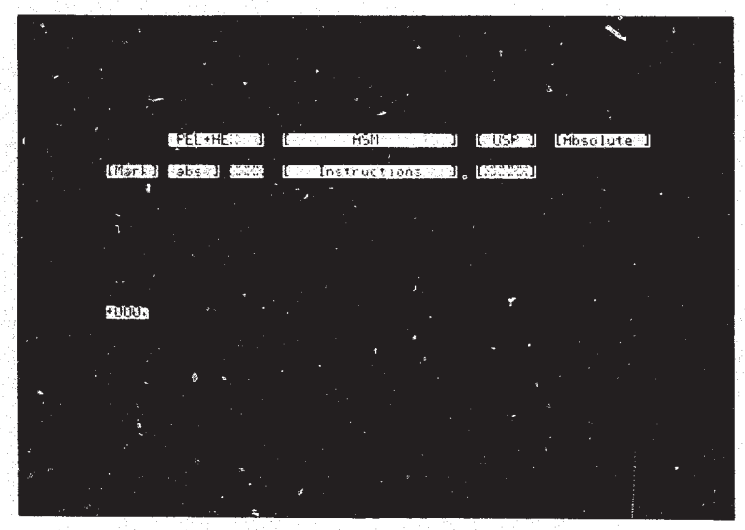


Figure 4-19. 1630G State Listing With States List in Absolute Values

6. When the analyzer captures a trace from the target system, the analyzer stores 1023 states, however sixteen states are displayed at one time. The list may be scrolled through by using the ROLL keys. Another way to quickly locate portions of the list is to move the cursor to the location in the State Listing marked by the inverse field and put a new value in the field. The list automatically changes to place the specified location in that position of the list. Typically, when a measurement is taken, only a few states or a particular event is of interest and it is not necessary to see the entire list. These states or events may be located by using the **[Mark/Show]** function of the analyzer.

7. Move the cursor to the field under ADDR at the right of the **[Mark]** field in the State Listing. Select an address in the list and place the value into this field. The asterisks that were beside each listing in the state list are now only at the locations that contain the address specified in the Mark field under the ADDR label, as in figure 4-20. If using relocatable module codes for display, use the NEXT[ ] or PREV[ ] key to select module name and enter the address to be marked with the front panel numerical keys.

8. Move the cursor back to the **[Mark]** field and change the field to **[Show]** with the NEXT[ ] or PREV[ ] key. Now only the states that contain the address specified are displayed, as in figure 4-21. The original trace is still preserved in memory, but has been temporarily edited.

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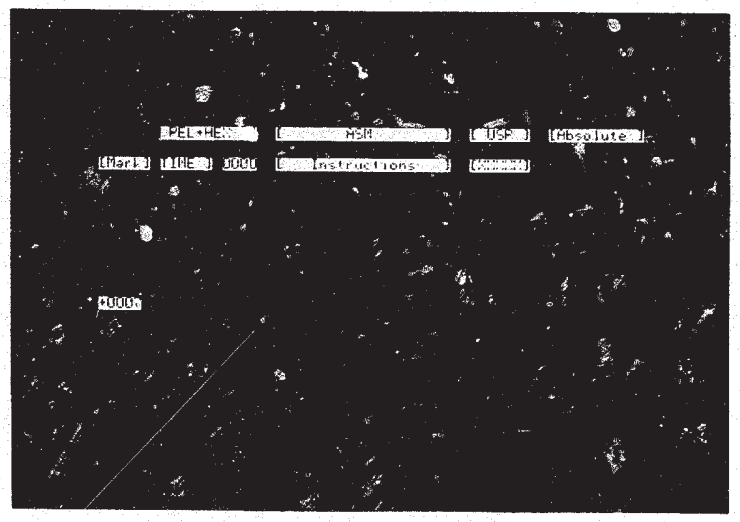


Figure 4-20. State Listing With Specific States Marked

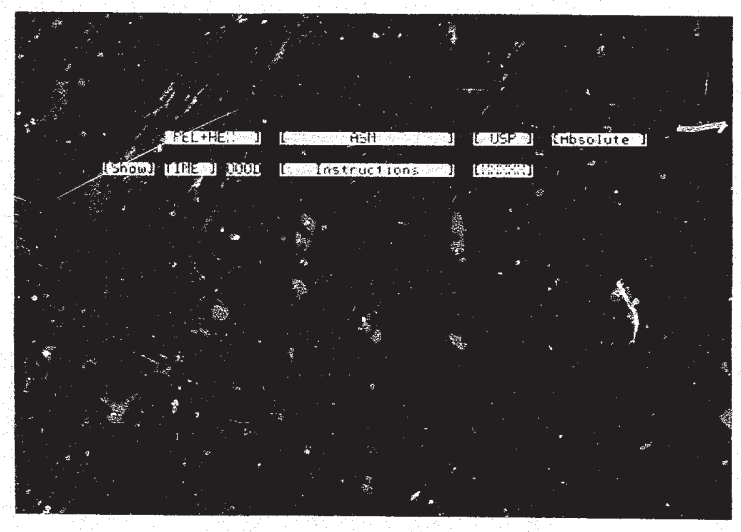


Figure 4-21. State Listing Showing Only a Specific State

9. The original list may be obtained by changing [Show] to [Mark] with the NEXT[ ] or PREV[ ] key and replacing the specified address under the ADDR label by X's with the DON'T CARE key.

NOTE

DON'T CARE triggering is useful for fault-finding in a system when part of the trigger word is unknown. For instance, if the trigger word is defined as 030X, (hexidecimal), the trace will trigger on any word from 0300 to 030F. The amount of words possible for triggering could be decreased further by specifying the trigger in binary base and defining only certain bits or one bit as DON'T CARE.

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Resource Terms

When the logic analyzer takes state traces, activity is clocked into the analyzer by a clock from the target system. After 1024 consecutive states have been stored, the trace halts and is displayed on the analyzer screen. This method of taking traces is used in many cases, but usually a sequence of data or a particular event is of interest, making need for qualification of data before it is captured. Resource terms are used to define specific states for qualifying data before it is captured by the logic analyzer.

Resource terms may be defined with the logic analyzer, with which the analyzer compares incoming bit patterns. Only activity complying with terms specified in the State Trace Specification is stored by the analyzer. Four terms are available for use as resource terms: a, b, c, and d. The resource terms are user defined and may be assigned for simple triggering, sequence triggering, sequence restart, and/or store qualifying.

TRIGGER [START/CENTER/END] TRACE

When a resource term is defined as the trigger term to [start] the state trace, the analyzer waits until the trigger is found and then starts storing states in memory. After 1024 states have been stored, the trace is halted. The captured state list is then displayed on the analyzer screen with the trigger term at line location 0000 in the State Listing. Selective storing of states may be specified in the State Trace Specification by defining terms to be stored after the trigger is found.

When the resource term is defined as the trigger term to [center] the trace, the analyzer keeps track of the trigger term in the same manner as a when a start trace term has been defined. After the trigger term is found and identified as the center of trace, states previous to the trigger term, the trigger term and the next 511 states are stored. The entire memory length of 1024 states may not always be listed in the State Listing. For instance, if the trigger term is found at the tenth state after RUN is pressed, nine states will be listed before the trigger in the listing (and labeled with a minus sign), the trigger (at line 0000), and 511 states after the trigger (labeled with a plus sign). The total listing will be 521 states long. Additional resource terms may be defined for selective storing.

The trace is stopped at the trigger term when the State Trace Specification defines the trigger term as the end of the trace. The analyzer displays the trigger term and up to 1024 states previous to the trigger depending on where the trigger is found after the RUN key is pressed. If the trigger term is found after 100 states, the State Listing will consist of 101 states.

Up to 59,999 occurrences of a state may be specified in the occurrence field of the State Trace Specification in order to pass loops in program activity that are well removed from the defined trigger term.

1. Press RUN and select one of the addresses from the ADDR column in the State Listing.

2. Press TRACE. Move the cursor to the [any state] field and select resource term [a] by pressing the NEXT[ ] key twice. When one or more resource terms have been selected, the four fields to define the terms are automatically added to the State Trace Specification menu as shown in figure 4-22.

3. Move the cursor to the first field under the ADDR label and type in the address selected in step 1. This specification tells the analyzer to start storing the trace in memory when it finds the selected address on the lines that have been labeled ADDR. The X's in the other fields indicate that any value on those lines will satisfy the trigger specification. Figure 4-23 is the trace specification to trigger on the first occurrence of a specified address.

4. Press RUN. The analyzer will monitor activity from the system under test until it finds the condition specified on the address lines. Then it captures that state in memory and all successive states until the memory is filled one time. The message "Trace Complete" will be displayed after a trace has been completed by the analyzer. The State Listing is shown in figure 4-24.

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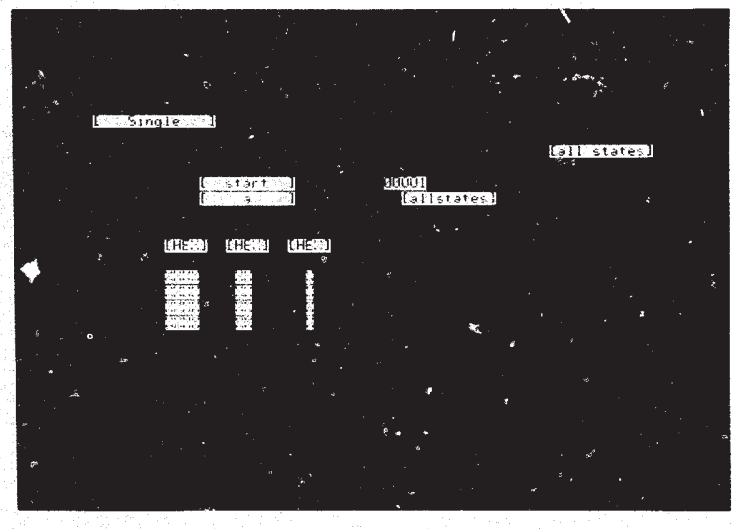


Figure 4-22. The State Trace Specification With Fields For Resource Terms

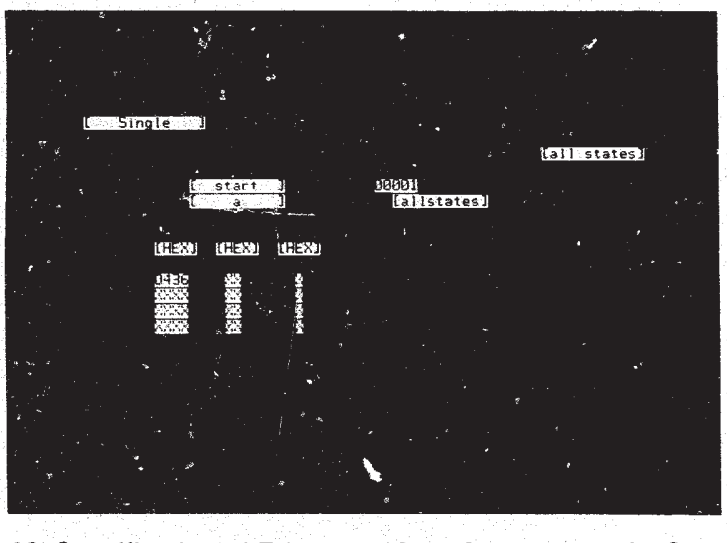


Figure 4-23. Specification of Trigger on First Occurrence of a Specific State

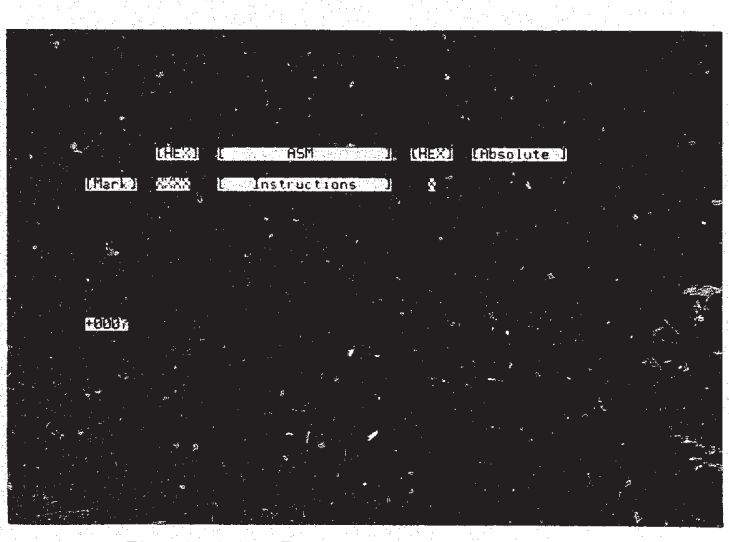


Figure 4-24. Trigger Starts Trace Listing

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5. The trigger state specified in the trace specification is at location 0000 on the State Listing. Trigger was specified to be the start of the trace.

6. Press TRACE and move the cursor to the [start] field. Select [center] with the NEXT[ ] key to place the trigger position at the center of the trace. This specification is used when it is desired to see states before and after the trigger condition. Notice a field to the right of the [a] resource term has been added to the menu for store qualifying data. Store qualifying is explained later in this chapter.

7. Press RUN. The analyzer will begin storing states into memory. When the state specified is found, the analyzer will capture that state and store an additional 512 states. The states captured before the trigger will be identified on the state list with line numbers preceded by minus signs. The trigger and the states captured after the trigger are identified by line numbers preceded with plus signs as in figure 4-25.

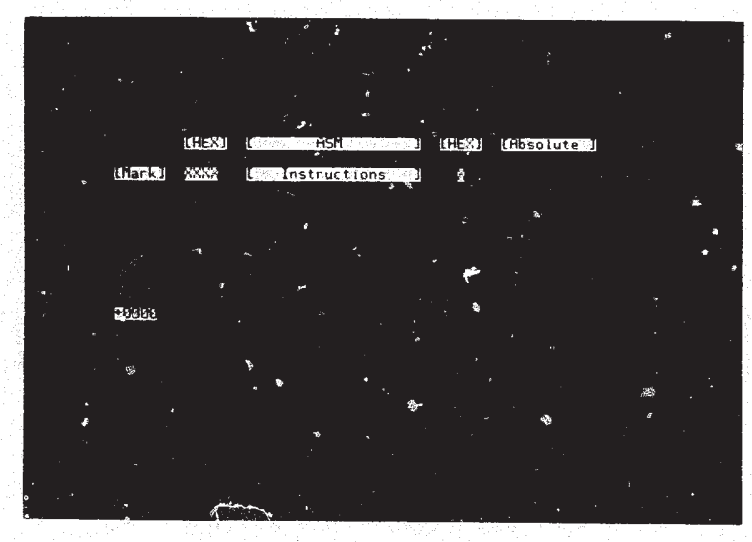


Figure 4-25. Trigger Centers Trace State Listing

8. The trigger may be placed at the end of the trace list in cases where activity after the trigger is not important but activity before the trigger is the necessary data. Press TRACE and select [end] trace on trigger. The analyzer captures activity from the target system until the trigger is found. The trigger condition and the previously captured states are then displayed in the state list, as in figure 4-26.

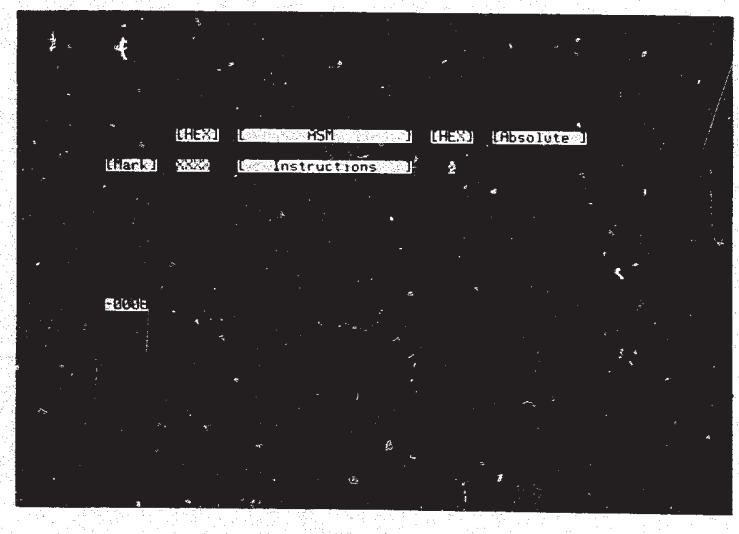


Figure 4-26. Trigger Ends Trace State Listing

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SEQUENTIAL TRIGGERING

Sequential triggering is used to trigger the analyzer only after a certain set of events has occurred in the sequence specified. It is used in defining a path of a branching network within the programming of the target system.

For example, figure 4-27 is a typical branch network. The analyzer is to execute a trace at the trigger term 6000, but only if the program has followed path 2 to reach the location 6000. Resource terms can define the trace specifications as: In sequence find [0300], then [0305], then [0500], then start trace on the first [00001] occurrence of [6000].

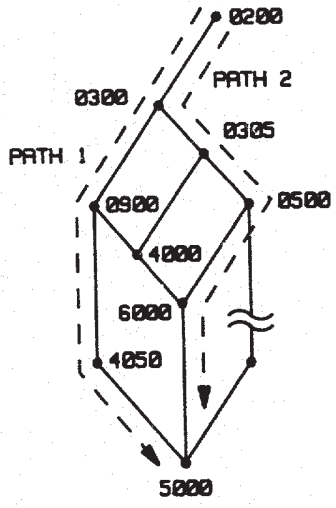


Figure 4-27. Branching Network With Specified Paths

Each resource term arms the analyzer for the next term to be recognized. The analyzer executes the trace only after all the terms have been recognized in the given sequence.

1. Press TRACE and move the cursor to the [start] field.

2. Press INSERT three times to open three fields for sequential triggering. Initially, all fields begin at [a].

3. Use the NEXT[ ] key to specify the sequence terms of find [a], then [b], then [c], then start trace at [d] as in figure 4-28. Notice the find sequence term [d] may be set for multiple occurrences before the trigger starts the trace.

   When using [then] find terms, the analyzer looks for the specified state at any time after the first state specified. The state may occur immediately after the first state or a significant time period later.

NOTE

Step 4 applies only to the 1630G.

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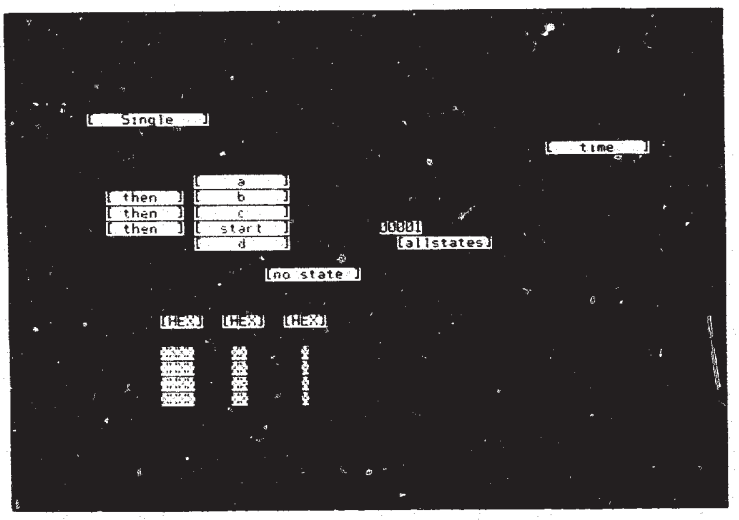


Figure 4-28. State Trace Specification With Sequence Terms

4. Move the cursor to one of the [then] fields on the State Trace Specification menu. Use the NEXT[ ] or PREV[ ] key to select [next to]. When [next to] is selected, the analyzer must see the [next to] term immediately following the previous term. If the [next to] term is not seen immediately after the first term, the analyzer will look for the first term again until it is immediately followed by the [next to] term. For example, in figure 4-29, all the [then] terms have been changed to [next to]. With this specification, the analyzer must find [a], immediately followed by [b], immediately followed by [c], immediately followed by [d]. The trace starts at term [d], and [d] will be the first state in the State Listing. If the State Trace Specification is changed to [center] or [end] the trace on [next to] term [d], all the sequence terms will be included in the State Listing, providing the storing [all states] field do not define store qualifiers. Store qualifying is discussed later in this chapter.

NOTE

Notice that the occurrence field is not on the State Trace Specification menu when the start, end, or center trace term is a [next to] term. The trace will always start, center, or end the trace on the first occurrence of the term which makes the occurrence count irrelevant.

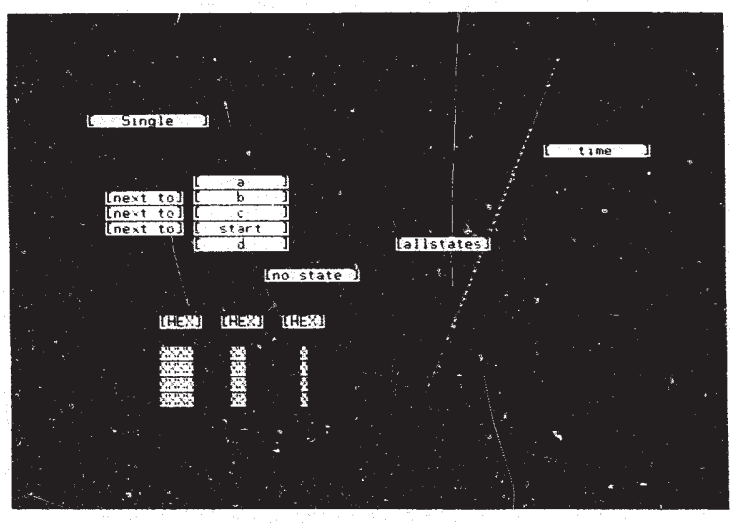


Figure 4-29. State Trace Specification With [next to] Sequence Terms

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5. Move the cursor to the [d] resource term and press INSERT three times. Three resource terms are added which may be used to define an ORed relationship to the trigger term. The NEXT[ ] and PREV[ ] keys are used to select a specific resource term for each field. The fields provide an ORed relationship for the final trigger term as shown in figure 4-29.

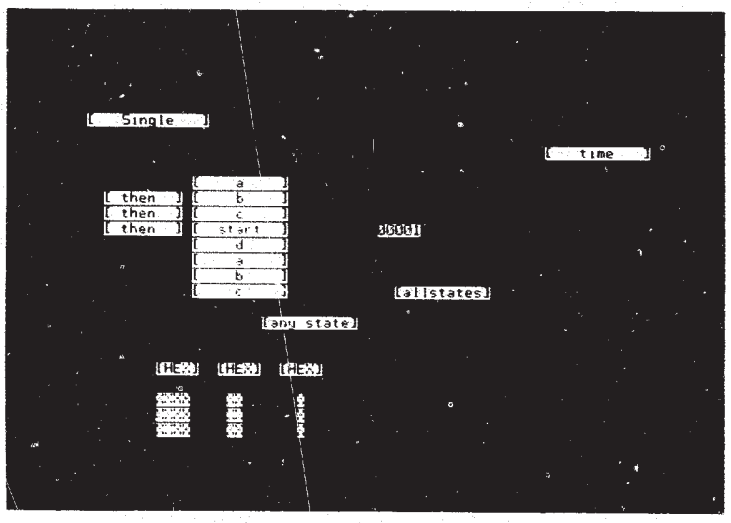


Figure 4-30. State Trace Specification With Sequence Terms and ORed Trigger Starts Terms

SEQUENCE RESTART

Sequence triggering occasionally requires a restart term to ensure the sequence is found in one pass through a branch network. If a restart term is not specified, the analyzer may eventually see all the sequence terms, though not in the path specified, and a trace will be executed. If the logic analyzer finds part of the sequence terms but not all the terms, then finding a sequence restart term will instruct the analyzer to repeat the sequence until all terms are found in the specified sequence.

1. Move the cursor to the sequence restart field.

2. Press NEXT[ ] or PREV[ ] to select a restart term.

3. As many as four resource terms may be selected to be ORed with the initial restart term by pressing the INSERT key. The State Trace Specification (figure 4-31) contains the maximum amount of resource terms to be ORed.

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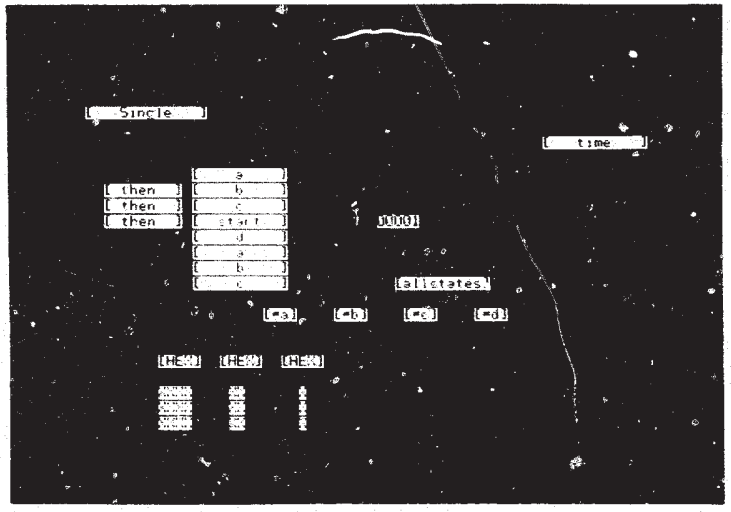


Figure 4-31. Maximum Sequence Restart ORed Resource Terms

STORE QUALIFIERS

Resource terms may be used to qualify data before it is stored by the logic analyzer. When resource terms are used as store qualifiers, only data matching the specified terms will be captured in analyzer memory. Resource terms are used to store qualify data after a sequence of terms are found, or for storing specified terms before a sequence term is found. When used for storing data before terms, the sequence terms are used as breakpoints to change the store qualifiers.

1. Move the cursor to the store [all states] field.

2. Cycle through the resource terms that may be selected by pressing the NEXT[ ] or PREV[ ] keys.

3. By pressing INSERT, up to four terms may be specified as store qualifiers to be ORed. The maximum amount of ORed store qualifiers when the trigger starts the trace are shown in figure 4-32.

NOTE

Use ROLL up key to see resource term d.

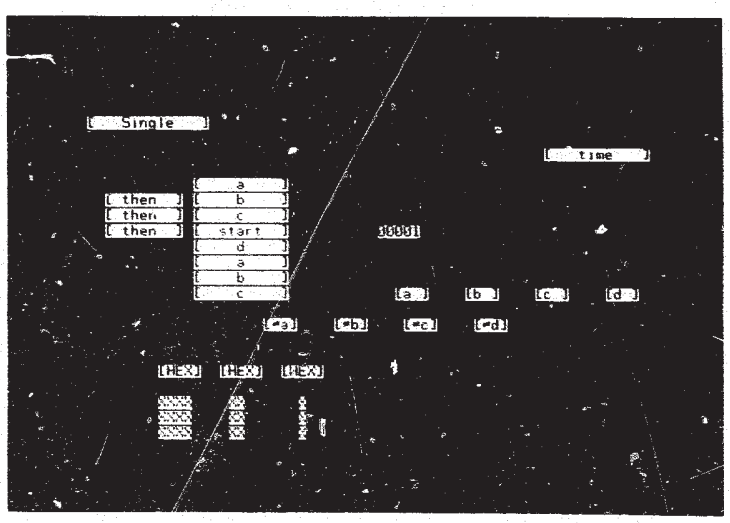


Figure 4-32. ORed Resource Terms as Store Qualifiers When Trigger Starts Trace

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