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Errata

Title & Document Type:

Manual Part Number:

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HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

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HEWLETT PACKARD

SERVICE MANUAL

HP MODEL 54100A/D
DIGITIZING OSCILLOSCOPE

SERIAL NUMBERS

This manual applies directly to instruments
prefixed with serial number:

54100A = 2740A
54100D = 2741A

For additional information about serial numbers see
INSTRUMENTS COVERED BY THIS MANUAL
in Section I.

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SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS



Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.



Indicates hazardous voltages.



Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

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SECTION 1

GENERAL INFORMATION

1-1. INTRODUCTION

This Service Manual contains information for testing, adjusting, and servicing the Hewlett-Packard 54100A/D Digitizing Oscilloscope. The manual is divided into 11 sections as follows:

1 - General Information

2 - Installation

3 - Performance Tests

4 - Adjustments

5 - Replaceable Parts

6A - Disassembly

6B - Theory

6C - Service Menu Keys

6D - Troubleshooting

6E - Internal Diagnostics

7 - Accessory Service

Information for operating, programming, and interfacing the HP 54100A/D is contained in the HP 54100A/D Operating and Programming Manual supplied with each instrument.

The General Information Section includes a description of the HP 54100A/D Digitizing Oscilloscope, its specifications, operating characteristics, instruments covered by this manual, options, accessories supplied, and recommended test equipment.

Also listed on the title page of this manual is a Microfiche part number. This number can be be used to order 4 X 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest Manual Changes supplement as well as pertinent Service Notes.

1-2. DESCRIPTION

The HP 54100A/D is a fully programmable 1 GHz digitizing oscilloscope with a 9-inch display. The HP 54100A/D is capable of automated measurements, digital storage, pre-trigger display, configurable inputs and triggering on complex digital waveforms.

To ensure proper functioning of the HP 54100A/D, extensive self-tests have been designed into the instrument. These self-tests are in addition to internal diagnostics, which aid in efficient fault locating and repair, if a failure does occur.

1-3. SPECIFICATIONS

Table 1-1 lists the specifications for the HP 54100A/D. These specifications include the performance standards against which the oscilloscope is tested.

1-4. INSTRUMENT OPERATING CHARACTERISTICS

Table 1-2 lists the operating characteristics for the HP 54100A/D. These characteristics are not specifications but typical characteristics included as additional information only.

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Table 1-1. Specifications

VERTICAL (voltage):

	Input Pod		
	HP 54002A 50 Ω Input	**HP 54001A Miniature Active Probe**	**HP 54003A 1 MΩ Probe†**
Bandwidth (-3 dB)*	dc to 1 GHz	dc to 700 MHz	dc to 300 MHz
Transition Time (10% to 90%)*	≤350 ps	≤450 ps	≤1.2 ns
Deflection Factor (full-scale = 8 divisions)	10 mV/div to 1 V/div in 1-2-5 steps	100 mV/div to 10 V/div in 1-2-5 steps	
DC Accuracy, Single Voltage Marker	±3% of full-scale ±2% of offset‡	±6% of full-scale ±2% of offset ±50 mV	
DC Delta Voltage Accuracy Using Two Voltage Markers On The Same Channel	±1% of full-scale ±3% of reading‡	±1% of full-scale ±6% of reading	

* *These specifications apply over ambient temperature range of +15°C to +35°C*
‡ *When driven from a 50 Ω source.*
† *With the 10:1 divider probe supplied with the HP 54003A*

DYNAMIC RANGE: Deflection factor and offset should be scaled such that the unmagnified signal remains within the full scale display range.

MAGNIFIER: Expands displayed signal vertically from 1 to 16X, adjustable in 0.5% steps

DC OFFSET:
Range: ±1.5 × full-scale (referenced to center screen).
Adjustment Resolution: Adjustable in steps of 0.0025X full-scale.

INPUTS: Two inputs, configurable with HP 54000 series pods.

HORIZONTAL (time):
Deflection Factor (full-scale = 10 div): 100 ps/div to 1 sec/div.
Adjustment Resolution: Adjustable in 1-2-5 steps via the knob and the step keys. Adjustable to three significant figures via the key pad or HP-IB command.

DELAY (time offset):
Pre-trigger Range: Up to −200 ms or −10 div, whichever is greater.
Post-trigger Range: Up to +1.6 secs or +600,000 div, whichever is greater.
Adjustment Resolution: Adjustable in steps of 2 ps or 1×10^{-6} × delay setting, whichever is greater.

TIME BASE ACCURACY:
Single Channel: ≤(100 ps ± 2×10^{-5} × Delta t reading).
Dual Channel: ≤(200 ps ± 2×10^{-5} × Delta t reading).

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Table 1-1. Specifications (continued)

TRIGGER:

Trigger Source	Vertical Channel 1 or 2			Trigger Input 3 (HP 54100D: Trigger Input 3 or 4)		
Input Pod	**HP 54002A**	**HP 54001A**	**HP 54003A***	**HP 54002A**	**HP 54001A**	**HP 54003A***
Trigger Level Range	±2 × full-scale			±2 V	±20 V	
Trigger Level Adjustment Resolution	0.0025 × full-scale			2 mV	20 mV	
Trigger Sensitivity DC to 100 MHz	0.12 × full-scale			40 mV	400 mV	
Above 100 MHz (frequency range)	0.24 × full-scale (100 MHz to 500 MHz)		0.24 × full-scale (100 MHz to 300 MHz)	80 mV (100 MHz to 500 MHz)	800 mV (100 MHz to 500 MHz)	800 mV (100 MHz to 300 MHz)
Pulse width > 1 ns	0.24 × full-scale			80 mV	800 mV	

*With the 10:1 divider probe supplied with the HP 54003A.

RMS Jitter: ≤ (50 ps + 5 × 10^{-7} × delay setting).
Trigger Source: Chan 1, Chan 2, Trig 3, (HP 54100D: Trig 4). Independent trigger level and polarity settings on all sources. Edge trigger on any source. Logical pattern trigger on all sources.
Trig 3 and Trig 4 Inputs: Configurable with HP 54000 series pods.

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Table 1-2. Operating Characteristics

HP 54100A/D OPERATING CHARACTERISTICS

DIGITIZER:

Resolution: 7 bits (1 part in 128). Effective resolution can be extended up to approximately 10 bits by using magnification and averaging.

Digitizing Rate: Up to 40 megasamples/second.

DISPLAY:

Data Display Resolution: 500 points horizontally by 256 points vertically.

Data Display Formats:

SPLIT SCREEN: Each channel is four divisions high

FULL SCREEN: The two channels are overlaid. Each channel is eight divisions high.

Display Modes:

VARIABLE PERSISTENCE: The time that each data point retained on the display can be varied from 200 ms to 10 sec, or it can be displayed indefinitely

AVERAGING: The number of averages can be varied from 1 to 2048 in powers of 2. On each acquisition, 1/n times the new data is added to (n-1)/n of the previous value at each time coordinate. Averaging operates continuously; the average does not converge to a final value after n acquisitions.

Graticules: Full grid, axes with tic marks, or frame with tic marks.

VERTICAL:

Input Protection: A relay opens when applied voltage exceeds rated input for the input pod in use (see Specifications).

HORIZONTAL:

Delay Between Channels: A difference in delay between channels can be nulled in 10 ps steps up to 10 ns to compensate for differences in input cables or probe length

Reference Location: The reference point can be located at the left edge, center, or right edge of the display. The reference point is that point where the time is offset from the trigger by the delay time.

Trigger:

INPUT PROTECTION: A prompt will appear on the display when the applied voltage exceeds rated input voltage for pod in use (see Specifications).

HOLDOFF:

Holdoff-By-Events: Range of events counter is from 2 to 67 million events. Maximum counting rate is 80 MHz. An event is defined as anything that satisfies the triggering conditions selected.

Holdoff-By-Time: Adjustable in 10 ns steps from 70 ns to 670 ms.

TRIGGER MODES:

Edge Trigger: On any source (see Specifications, Trigger Source).

Pattern Trigger: A pattern can be specified for all sources. Each source can be specified as high, low, or don't care. Trigger can occur on the last edge to enter the specified pattern or the first edge to exit the specified pattern

Time Qualified Pattern Trigger (HP 54100D only): Trigger occurs on the first edge to exit the specified pattern, only if the pattern was present for less than (greater than) the specified time. Filter time is adjustable from 10 ns to 5 sec. Filter recovery time is ≤8 ns. In the "When Present < (time)" mode, the pattern must be present > 1 ns for the trigger to respond.

State Trigger (HP 54100D only): A pattern can be specified for any three sources. Trigger can be set to occur on an edge of either polarity on the source specified as the clock, (not one of the pattern sources), when the pattern is present or not present. Setup time for the pattern to be present prior to the clock edge is < 4 ns; hold time is zero.

Delayed Trigger (HP 54100D only):

EVENTS-DELAYED MODE: The trigger can be armed by an edge on any source, then triggered by the nth edge on any other source. The number of events, n, can be set from 1 to $1 \times 10^9 - 1$. Maximum event counting rate is 150 MHz.

TIME-DELAYED MODE: The trigger can be armed by an edge on any source, then triggered by the first edge on any other source after a specified time has elapsed. The delay time can be set from 20 ns to 5 seconds.

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Table 1-2 Operating Characteristics (continued)

MEASUREMENT AIDS:

Markers: Dual voltage markers and dual time markers are available. Voltage markers can be assigned to either channel or to both channels

Auto Top-Base: Automatically sets voltage markers on the top and base of a pulse using a histogram technique. Markers can, also, be automatically set to 10-90%, 20-80%, or 50% points on a transition.

Automatic Edge Finders: The time markers can be assigned automatically to any displayed edge of either polarity on either channel or both channels. The voltage markers establish the threshold reference for the time markers in this mode.

Automatic Pulse Parameter Measurements: The following pulse parameter measurements can be performed automaticlly (as defined in IEEE Standard 194-1977, "IEEE Standard Pulse Terms and Definitions").

Frequency
Period
Pulse duration (± width)
Risetime
Falltime
Preshoot
Overshoot
Peak-to-peak Voltage
RMS Volts
Duty Cycle
V max (HP-IB Programmable only)
V min (HP-IB programmable only)
V top (HP-IB programmable only)
V bottom (HP-IB programmable only)

Waveform Math: Two independent functions are provided for waveform math. The operators are +, −, invert, versus and only. Either of the two vertical channels or any of the four waveform memories can be used as operands for the waveform math. If turned on, Function 1 is displayed in lieu of Channel 1 and Function 2 is displayed in lieu of Channel 2.

SETUP AIDS:

Presets: Vertical deflection factor, offset, and trigger level can be preset independently on each channel for ECL or TTL levels.

Auto-Scale: Pressing the Auto-Scale button causes the vertical and horizontal deflection factors and the trigger source to be set for a display appropriate to the signals applied to the inputs. Requires a duty cycle >0.1%, and amplitude >20 mv peak, and a frequency >50 Hz. Operative only for relatively stable input signals.

Save/Recall: Ten front panel setups may be saved in non-volatile memory. If Auto-Scale is inadvertently pressed, pressing Recall followed by Auto-Scale, restores the instrument to the state prior to the first Auto-Scale.

Waveform Memories: Four memories are provided for storage of waveforms. Only one waveform may be stored in each of these memories. These memories can be used as sources for either measurements or functions. Two additional memories are provided to store pictures. Each of these two waveform picture memories is a pixel map of the display. Any number of waveform pictures may be written into each picture memory. Once stored, individual waveforms cannot be accessed from the picture memories. The display of any of the six memories can be turned on or off without affecting their contents. Waveforms in memory are displayed in a different color from live waveforms.

POWER REQUIREMENT:

Voltage: 115/230 Vac, +15% to −25%, 48-66 Hz.

Power; 290 watts maximum, 500 VA maximum.

GENERAL CHARACTERISTICS:

Dimensions: Refer to outline drawing.

Weight:

NET: Approximately 19 kg (42 lb)

SHIPPING: Approximately 23.5 kg (52 lb).

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Table 1-2. Operating Characteristics (continued)

ENVIRONMENTAL CHARACTERISTICS:

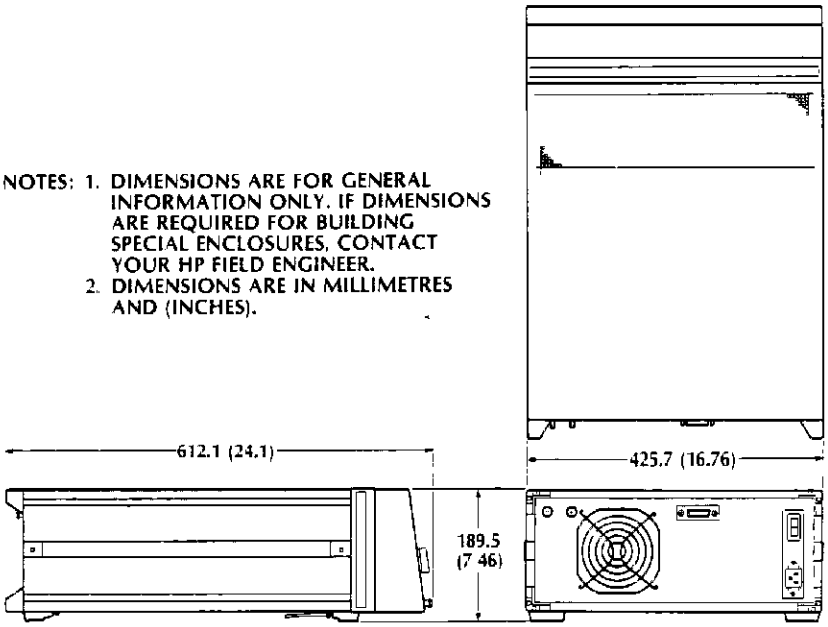
Temperature:
OPERATING 0° C to +55° C (+32° F to +131° F). Note: See specifications.
NON-OPERATING: –20° C to +75° C (–4° F to 167° F).

Humidity:
OPERATING Up to 90% relative humidity at +40° C (+104° F).
NON-OPERATING: Up to 95% relative humidity at +65° C (+149° F).

Altitude:
OPERATING Up to 4600 metres (15,000 ft)
NON-OPERATING: Up to 15,300 metres (50,000 ft).

Vibration: Vibrated in three orthogonal axes for 15 minutes per axis, 0.38 mm (0.15 in.) peak-to-peak excursion; 5 to 55 Hz 1 minute, octave sweep

NOTES: 1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).



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1-5. SAFETY CONSIDERATIONS

Safety information relevant to the service procedure being described is provided in the appropriate sections of this manual. The HP 54100A/D and this manual should be reviewed for safety markings and instruction before work is begun. Refer to the pages following the title page, which include a safety summary and safety considerations.

1-6. INSTRUMENTS COVERED BY MANUAL

The oscilloscope serial number is located on the rear panel. Hewlett-Packard uses a two-part serial number with a four-digit prefix and a five-digit suffix separated by a letter (**0000A00000**). The prefix is the same for all identical oscilloscopes and changes only when a modification is made that affects parts compatibility. The suffix is assigned and is different for each oscilloscope. This manual applies directly to oscilloscopes with the serial prefix shown on the title page.

An oscilloscope manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial prefix indicates the oscilloscope is different from those described in this manual. The manual for this newer oscilloscope is accompanied by a Manual Changes supplement. The supplement contains "change information" that explains how to adapt the manual to the newer oscilloscope.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-7. OPTIONS

The following options are available for the HP 54100A/D:

Option 908 - Rack mount kit
Option 910 - one additional Operating and Programming manual
Option 900-902, 904, 906, and 912
Power cord options (see table 2-1)

1-8. ACCESSORIES SUPPLIED

The following accessories are supplied with the HP 54100A/D:

HP 54002A 50 Ω input pod (quantity HP 54100A - 3; HP 54100D - 4)
Operating and Programming manual (quantity 1)
Service manual (quantity 1)
USA power cord (quantity 1)

1-9. RECOMMENDED TEST EQUIPMENT

Equipment recommended to maintain the HP 54100A/D is listed at the beginning of each of the manual sections where the equipment is used. The three sections requiring test equipment are Performance tests (Section 3), Adjustments (Section 4), and Service (Section 6).

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SECTION 2

INSTALLATION

2-1. INTRODUCTION

This section contains installation instructions, information about storage and shipment, operating environments, and cleaning the HP 54100A/D.

2-2. PREPARATION FOR USE

CAUTION

To prevent damage to the instrument, make sure the line voltage selector switch is in the correct setting for your AC voltage source.

2-3. Power Requirements

The HP 54100A/D requires a power source of 115 or 230 Vac +15/-25 percent; 48 to 66 Hertz single phase. Power consumption is 290 watts or 500 VA maximum.

2-4. Line Voltage Selection

Use a blade-type screwdriver to change the position of the line select switch. Figure 2-1 shows the line select switch in the 115V position. Once the correct setting of the line switch has been made, the correct circuit breaker trip current is selected.

2-5. Power Cables

WARNING

To protect operating personnel from possible injury or death, the chasis must be properly grounded. To avoid this hazard, the proper power cord must be used and the power cord ground must ***NOT*** *be defeated. Refer to table 2-3 for power cable description and application.*

This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, the cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See Table 2-1 for option numbers of power cables and plug configurations available.

2-6. CLEANING

When cleaning the HP 54100A/D, use mild soap and water. If a harsh soap or solvent is used, the water-base paint finish may be damaged.

CAUTION

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuit if it seeps under the keys.

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2-7. OPERATING ENVIRONMENT

The operating environment is noted in table 1-2. Note the non-condensing humidity limitation. Condensation in the instrument can cause poor operation or malfunction. Protect the instrument against internal condensation.

The HP 54100A/D will operate to all specifications, with the temperature and humidity range given in table 1-2. However, reliability is enhanced by operating the instrument within the following ranges.

Temperature:	0°C to +55°C (+32°F to +132°F)
Humidity:	Up to 90% relative humidity at 40°C(+104°F)
Altitude:	Up to 4600 meters(15,000 feet)

High temperature/humidity combinations should be avoided.

2-8. STORAGE AND SHIPMENT

The instrument may be stored or shipped in environments with the following limits:

Temperature:	-40°C to +75°C (-4° to +167°F)
Humidity:	Up to 95% at 40°C(+104°F)
Altitude:	Up to 15,300 Meters(50,000 Feet)

The instrument should also be protected from temperature extremes which may cause condensation within the instrument. Condensation within the instrument may cause a malfunction, if the instrument is operated under these conditions.

If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. In any correspondence, refer to the instrument by model number and full serial number.

2-9. PACKAGING

Original packaging i.e., containers and material identical to those used in factory packaging are available from Hewlett-Packard. If other packaging is to be used, the following general instructions for repackaging with commercially available materials should be followed:

a. Wrap the oscilloscope in heavy paper or plastic.

b. Use a strong shipping container. A double wall carton made of 2.4 MPa (350 psi) test material is adequate

c. Use a layer of shock absorbing material 75 to 100 mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the control Panel with cardboard.

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to ensure careful handling.

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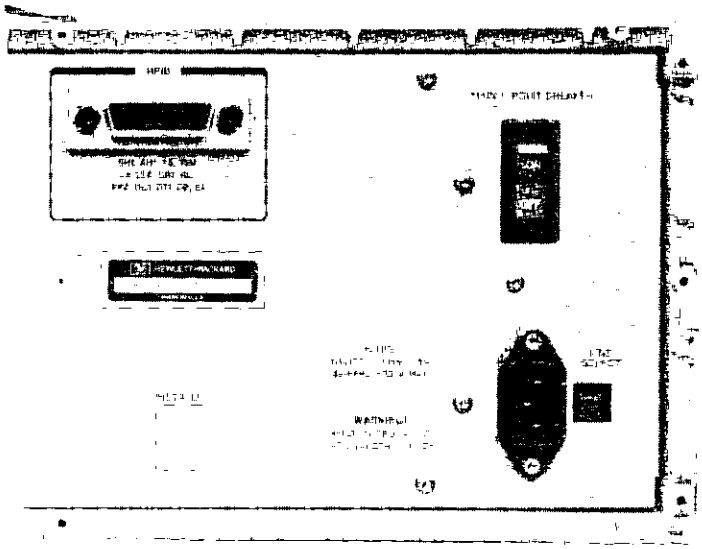
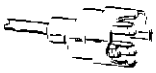


Figure 2-1. Line Voltage Selection.

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Table 2-1. AC Power Cables.

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 900 250V 	8120-1351 8120-1703	Straight *BS1363A 90°	90/228 90/228	Gray Mint Gray	United Kingdom, Cyprus, Nigeria, Zimbabwe Singapore
OPT 901 250V 	8120-1369 8120-0696	Straight *NZSS198 ASC 90°	79/200 87/221	Gray Mint Gray	Australia New Zealand
OPT 902 250V 	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79/200 79/200 79/200	Mint Gray Mint Gray Coco Brown	East and West Europe Saudi Arabia, So Africa, India (Unpolarized in many nations)
OPT 903 125V 	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical UL544	90/228 90/228 96/244	Jade Gray Jade Gray Black	United States, Canada, Japan (100V or 200V), Mexico, Philippines, Taiwan
OPT 904 250V 	8120-0698	Straight *NEMA6-15P	90/229	Black	United States, Canada
OPT 905 250V 	8120-1396 8120-1625	CEE22-V1 (Systems Cabinet use) 250V	30/76 96/244	Black Black	
OPT 906 250V 	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79/200 79/200	Mint Gray Mint Gray	Switzerland
OPT 912 220V 	8120-2956 8120-2957	Straight *DHCK107 90°	79/200 79/200	Mint Gray Mint Gray	Denmark

*Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part Number for complete cable including plug.

E = Earth Ground
L = Line
N = Neutral

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SECTION 3

PERFORMANCE TESTS

3-1. INTRODUCTION

The procedures in this section test the instrument's electrical performance using specifications in Section I as performance standards. All tests can be performed without access to the interior of the instrument.

3-2. RECOMMENDED EQUIPMENT FOR PERFORMANCE TESTS

Equipment recommended for performance tests is listed in table 3-1. Any equipment that satisfies the critical specifications stated in the table may be substituted.

Table 3-1. Recommended Equipment for Performance Tests.

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Function Generator	50 MHz Sinewave and squarewave	HP 8116A
Sweep Oscillator	1.3 GHz Leveled output	HP 8620C/86220A
Signal Generator	Stable 500 MHz output with attenuator	HP 8656B/001
Pulse Generator	Risetime <100 ps	Tektronix TYPE 284
Digital Voltmeter	>0.3% accuracy at 1 Vdc	HP 3478A
Power Divider	3dB 50 Ohm Splitter	HP 11667A

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3-3. TEST RECORD

Results of performance tests may be tabulated on the Performance Test Record (table 3-2) at the end of the procedures. The test record lists all of the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance, troubleshooting, and after repairs or adjustments.

3-4. PERFORMANCE TEST CYCLE

This instrument requires periodic verification of performance. The instrument should be checked using the following performance tests at least every six months or after 1000 hours of operation, whichever is less. Amount of use, environmental conditions, and the user's experience concerning the need for performance checks will contribute in deciding the performance test cycle.

3-5. PERFORMANCE TEST PROCEDURES

Note

Allow instrument to warm up for at least 30 minutes prior to beginning performance tests

Note

HP Model 54002A 50Ω 1:1 pods must be used for performance tests.

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3-6. VERTICAL ACCURACY TEST

Specification:

DC Delta Voltage Accuracy*:
±1% of full-scale
±3% of reading**
*Using two voltage markers on one channel.
**When driven from a 50 Ω source

Description:

Vertical accuracy of both channels is checked by applying several known voltage levels and making DELTA V measurements on each. Each DELTA V reading must be within specified limits.

Equipment Recommended: **Model**

Function Generator ..... HP 8116A
Digital Voltmeter ..... HP 3478A

Instrument Setup:

HP 54100A/D:

```
Channel 1 & 2
          - VOLTS/DIV -  1 V
          - OFFSET    - +5 V

Timebase  - SEC/DIV   - 1 us
          - Auto

Display   - Graticule - Frame
          - Split Screen - Off
          - AVERAGES  - 256

Channel 2 - DISPLAY   - OFF
```

Function Generator:

```
Offset    - +5 V
AMP       -  5.00 V

Waveform - ALL OFF
```

Digital Voltmeter:

```
DC Volts
```

Procedure:

1. Connect function generator's output to channel 1 and digital voltmeter.

Note

While observing the DVM, set the function generator output level to the voltage required for each of the following steps.

2. Make a DELTA V measurement by pressing ***AUTO-TOP-BASE*** and ***50-50%***.

3. The V(1) voltage should be within 4.77 V and 5.23 V.

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3-6. VERTICAL ACCURACY TEST (Continued)

4. Change function generator offset to -5.00 V and set HP 54100A/D OFFSET for -5.00 V.
5. Make a DELTA V measurement by pressing ***AUTO-TOP-BASE*** and ***50-50%***.
6. The V(1) voltage should be within -4.77 V and -5.23 V.
7. Adjust function generator's offset for -120 mV and set HP 54100A/D OFFSET to -120 mV.
8. Change vertical sensitivity to 10 mV/division.
9. Make a DELTA V measurement by pressing ***AUTO-TOP-BASE*** and ***50-50%***.
10. The V(1) voltage should be within -116 mV and -124 mV.
11. Change function generator's offset to +120 mV and set HP 54100A/D OFFSET to +120 mV.
12. Make a DELTA V measurement by pressing ***AUTO-TOP-BASE*** and ***50-50%***.
13. The V(1) voltage should be within 116 mV and 124 mV.
14. Repeat steps 2 through 14 for channel 2.

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3-7. BANDWIDTH TEST

Specification:

Bandwidth (-3dB)* - DC to 1 GHz

*Applies when using a 50 Ω input over ambient temperature range of +15°C to +35°C

Description:

Bandwidth is checked by ensuring the displayed signal is less than 3dB down from dc to 1 GHz.

Equipment Recommended: **Model**

Sweep Oscillator ..... HP 8620C/86220A

Instrument Setup:

HP 54100A/D Setup:

Channel 1 & Channel 2	- Mode	- Normal
	- VOLTS/DIV	- 200 mV/div
	- OFFSET	- 0 V
Timebase	- SEC/DIV	- 2 ms
	- Delay ref at	- left
	- sweep	- trg'd
Trigger	- Mode	- Edge
	- Source	- Chan 1
	- LEVEL	- +500 mV
	- Slope	- pos
	- HOLDOFF Time	- 21 ms
Display	- Mode	- Normal
	- DISPLAY TIME	- 200 ms
	- Split Screen	- Off
Delta V	- Marker 1 at +564 mV	
	- Marker 2 at -564 mV	

Sweep Oscillator:

Start marker	- .01 GHz
Stop marker	- 1.2 GHz
CW marker	- 1.0 GHz
Power Level	- +9 dBm
Trigger	- internal
Time	- 0.01
Markers	- AMPL
Marker sweep	- ON

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3-7. BANDWIDTH TEST (Continued)

Procedure:

1. Connect sweep oscillator RF output to channel 1, turn channel 1 on and channel 2 off.
2. Adjust sweep oscillator output level until displayed signal fills 8 divisions vertically. Press ***Clear Display*** key to help see this.
3. Adjust sweep oscillator's time vernier until displayed waveform is 10 divisions in length.
4. Change DISPLAY time to Infinite.
5. Press ***Clear Display*** key.
6. The DELTA V markers are the 3 dB points and each horizontal division represents approximately 120 MHz. The sweep oscillator's CW MARKER will show up as a dark line as the display area fills up. The waveform amplitude at the CW marker should be greater than the amplitude of the waveform at the delta V markers.
7. Connect sweep oscillator output to channel 2. Turn channel 1 off and channel 2 on. Change Trigger Source to channel 2 and Trigger Level to 500 mV.
8. Repeat steps 2 through 6 for channel 2.

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3-8. STEP RESPONSE (RISETIME) TEST

Specification: Transistion time (10% to 90%): ≤350 psec*
*Applies when using a 50 Ω input and over ambient tempature +15°C to +35°C.

Description:

Step Response (Risetime) is measured by applying a fast risetime pulse to both channels and making automatic risetime measurements.

Equipment Recommended: **Model**

Pulse Generator ..... Tektronix TYPE 284

Instrument Setup:

HP 54100A/D:			Pulse Generator:
Channel 1 & Channel 2	- Mode	- Normal	Mode - Pulse
	- VOLTS/DIV	- 50 mV/div	
	- OFFSET	- Center waveform	
Timebase	- SEC/DIV	- 2 ns/div	
	- DELAY	- 0 ns	
	- Delay ref at	- center	
Trigger	- Mode	- Edge	
	- Source	- channel 1	
	- LEVEL	- +120 mV	
	- Slope	- Pos	
	- HOLDOFF TIME	- 70 ns	
Display	- Mode	- Averaged	
	- AVERAGES	- 8	
	- Split Screen	- Off	

Procedure:

1. Connect pulse generator's output to channel 1, turn channel 1 on and channel 2 off.
2. Select ***MEASURE*** menu and make an automatic RISEtime measurement.
3. Risetime should be ≤360 ps.
4. Connect pulse generator's output to channel 2.
5. Set channel 1 to OFF, channel 2 to ON, Trigger Source to channel 2, Trigger Level to 120 mV.
6. Select ***MEASURE*** menu and make an automatic RISEtime measurement.
7. Risetime should be ≤360 ps.

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3-9. TIME INTERVAL ACCURACY TEST

Specification:

Single Channel: ≤100 ps±((2 X 10^{-5})(DELTA T reading))

Dual Channel: ≤200 ps±((2 X 10^{-5})(DELTA T reading))

Description:

The horizontal crossing of an input signal (at a minimum delay value) is set to center screen. The delay values are then increased and the crossing is observed to verify that it remains at center screen.

Note

Perform software calibration as directed by the CAL menu. DELAY and CHANNEL TO CHANNEL skew must be properly set. Refer to section 6C of this manual for the CAL procedure.

Note

The National Bureau of Standards requires an external clock that is traceable to ±2 ppm in timebase accuracy for this test.

Equipment Recommended: **Model**

Signal Generator ..... HP 8656B/001

Instrument Setup:

```
Signal Generator:
   Frequency - 500 MHz
   Amplitude - 200 mV
```

Procedure:

CHANNEL 1 ACCURACY

1. Connect signal generator to channel 1 and 2 and press ***AUTO-SCALE***.

2. Set HP 54100A/D as follows:

```
Channel 2 to Off                 Channel 1 & 2 VOLTS/DIV to 50 mV
Trigger Slope to Positive        Channel 1 & 2 OFFSET to 0 V
Trigger Source 1                 Trigger LEVEL for 1, 2, and 3 to 0 V
TIMEBASE to 100 ps/div           Split Screen to Off
AVERAGES to 64
```

3. Adjust Trigger LEVEL so positive edge crosses exactly at center screen.

4. Change DELAY to 2 ns and verify positive horizontal crossing occurs within 1 division of center screen.

5. Change DELAY to 10 ns and verify positive horizontal crossing occurs within 1 division of center screen.

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3-9. TIME INTERVAL ACCURACY TEST (Continued)

6. Change DELAY to 18 ns and verify positive horizontal crossing occurs within 1 division of center screen.

7. Change DELAY to 26 ns and verify positive horizontal crossing occurs within 1 division of center screen.

8. Change DELAY to 5 μs and verify positive slope crossing occurs within 2 divisions of center screen.

CHANNEL TO CHANNEL ACCURACY

9. Set channel 1 to OFF and channel 2 to ON. TRIG SOURCE remains channel 1. Set DELAY to 0 ns.

10. Change DELAY to 2 ns and verify positive horizontal crossing occurs within 2 divisions of center screen.

11. Change DELAY to 10 ns and verify positive horizontal crossing occurs within 2 divisions of center screen.

12. Change DELAY to 18 ns and verify positive horizontal crossing occurs within 2 divisions of center screen.

13. Change DELAY to 26 ns and verify positive horizontal crossing occurs within 2 divisions of center screen.

14. Change DELAY to 5 μs and verify positive slope crossing occurs within 3 divisions of center screen.

CHANNEL 2 ACCURACY

15. Set channel 2 to ON, set channel 1 to OFF, and select TRIG SOURCE channel 2. Set DELAY to 0 ns.

16. Adjust Trigger LEVEL so the positive edge crosses exactly at center screen.

17. Change DELAY to 2 ns and verify positive horizontal crossing occurs within 1 division of center screen.

18. Change DELAY to 10 ns and verify positive horizontal crossing occurs within 1 division of center screen.

19. Change DELAY to 18 ns and verify positive horizontal crossing occurs within 1 division of center screen.

20. Change DELAY to 26 ns and verify positive horizontal crossing occurs within 1 division of center screen.

21. Change DELAY to 5 μs and verify positive slope crossing occurs within 2 divisions of center screen.

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3-10. TRIGGER SENSITIVITY TEST

Specification:

(0.12) (full scale vertical) using a 50 Ω input to 100 MHz
(0.24) (full scale vertical) using a 50 Ω input from 100 MHz to 500 MHz

Description:

When a 100 MHz signal is applied to either channel, the oscilloscope must trigger. The signal must remain coherent (triggered) as the input amplitude is decreased and the frequency is increased until the specifications are met.

Equipment Recommended: **Model**

Signal Generator ..... HP 8656B/001
Power Divider ..... HP 11667A

Instrument Setup:

HP 54100A/D Setup:

Channel 1 & Channel 2	- Mode	- Normal	
	- VOLTS/DIV	- 10 mV	
	- OFFSET	- 0 V	
Timebase	- SEC/DIV	- 2 ns	
	- Delay	- 0 ns	
Trigger	- Mode	- Edge	
	- Source	- channel 1	
	- LEVEL	- 0 V	
Display	- Mode	- Averaged	
	- AVERAGES	- 8	
	- Split Screen	- Off	

Signal Generator:

Frequency	- 100 MHz
Amplitude	- 9 mV
Amp Increment	- 0.1 mV

Procedure:

1. Turn channel 1 and channel 2 on.
2. Connect signal generator to channel 1.
3. Decrease signal generator's output amplitude until a 10 mV peak-to-peak waveform is displayed. Waveform must be coherent (triggered).

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3-10. TRIGGER SENSITIVITY TEST (Continued)

4. Connect signal generator to channel 2, set Trigger Source to channel 2 and Trigger Level to 0V.

5. A 10 mV peak-to-peak waveform should be displayed and must be coherent (triggered).

6. Change 54100A\D SEC/Div to 500 ps.

7 Change signal generator frequency to 500 MHz and adjust amplitude to 20 mV peak-to-peak. Waveform should be coherent (triggered).

8 Connect signal generator output to channel 1.

9. Change trigger source to channel 1.

10. Waveform should be coherent (triggered).

11. Split signal with a power divider and apply to channel 3.

12. Adjust signal generator amplitude until an 80 mV peak-to-peak waveform is displayed.

13. Select TRIG SOURCE 3 and set Trigger Level to 0 V. Waveform must be coherent.

14. Change signal generator frequency to 100 MHz and adjust amplitude to 40 mV peak-to-peak.

15. Change HP 54100A/D SEC/Div to 2 ns.

16. Waveform should be coherent.

HP 54100D only

18. Select TRIG SOURCE 4 and set Trigger Level to 0 V. Waveform must be coherent.

19. Change signal generator frequency to 500 MHz and adjust amplitude to 80 mV peak-to-peak.

20. Change HP 54100A/D SEC/Div to 500 ps.

21. Waveform should be coherent.

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3-11. APERTURE JITTER TEST

Specification:

≤300 ps peak to peak
≤(50 ps rms + 5 X 10^{-7} X delay setting)

Description:

Aperture jitter is tested by measuring the width of the displayed waveform after it is allowed to accumulate for three minutes in infinite persistence mode.

Equipment Recommended: **Model**

Pulse Generator ..... Tektronix TYPE 284

Instrument Setup:

HP 54100A/D Setup:					Pulse Generator:
Channel 1 & Channel 2	-	Mode	-	Normal	Mode - Pulse
	-	VOLTS/DIV	-	50 mV	
	-	OFFSET	-	+120 mV	
Timebase	-	SEC/DIV	-	100 ps	
	-	sweep	-	trg'd	
Trigger	-	Source	-	1	
	-	LEVEL	-	+120 mV	
Display	-	Mode	-	Normal	
	-	Display Time	-	Infinite Persistence	

Procedure:

1. Connect pulse generator's output to channel 1 and allow display to accumulate for a minimum of three minutes. Use delay to center the leading edge of waveform.

2. Using DELTA T markers, measure the width of the display at the center crossing (X axis width). Width should be ≤300 ps peak-to-peak.

3. Turn channel 1 OFF and channel 2 ON.

4. Change TRIG SOURCE to 2, set Trigger Level to 120 mV, and connect pulse generator output to channel 2.

5. Press ***CLEAR DISPLAY***.

6. Allow display to accumulate for a minimum of three minutes.

7. Using DELTA T markers, measure the width of the display at the center crossing (X axis width). Width should be ≤300 ps peak-to-peak.

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Table 3-2. Performance Test Record

HEWLETT-PACKARD
MODEL HP 54100A/D

DIGITAL OSCILLOSCOPE

SERIAL NO. _____

Tested by _____

Work Order No. _____

Date _____

Recommended Calibration

Interval _____ Months

Paragraph Number	Test		Results
3-6	Vertical Accuracy Test	channel 1 step 3	Minimum -- 4.77 V Actual _____ V Maximum -- 5.23 V
		step 6	Minimum -- -4.77 V Actual _____ V Maximum -- -5.23 V
		step 10	Minimum -- -116 mV Actual _____ mV Maximum -- -124 mV
		step 13	Minimum -- 116 mV Actual _____ mV Maximum -- 124 mV
		channel 2 step 3	Minimum -- 4.77 V Actual _____ V Maximum -- 5.23 V
		step 6	Minimum -- -4.77 V Actual _____ V Maximum -- -5.23 V
		step 10	Minimum -- -116 mV Actual _____ mV Maximum -- -124 mV
		step 13	Minimum -- 116 mV Actual _____ mV Maximum -- 124 mV

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Paragraph Number	Test		Results
3-7	Bandwidth Test	channel 1 step 6	CW Marker greater than DELTA V markers yes ____ no ____
		channel 2 step 6	CW Marker greater than DELTA V markers yes ____ no ____
3-8	Step Response (Riselime) Test	channel 1 step 3	Riselime is ≤360 ps yes ____ no ____
		channel 2 step 7	Risetime is ≤360 ps yes ____ no ____
3-9	Time Interval Accuracy Test	channel 1 step 4	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen
		step 5	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen

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Paragraph Number	Test		Results
3-9	Time Interval Accuracy Test (cont)	step 6	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen
		step 7	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen
		step 8	Minimum-2 divisions left of center screen Actual - _____ Maximum-2 divisions right of center screen
	channel to channel	step 10	Minimum-2 divisions left of center screen Actual - _____ Maximum-2 divisions right of center screen

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Paragraph Number	Test		Results
3-9	Time Interval Accuracy Test (cont)	step 11	Minimum-2 divisions left of center screen Actual - _____ Maximum-2 divisions right of center screen
		step 12	Minimum-2 divisions left of center screen Actual - _____ Maximum-2 divisions right of center screen
		step 13	Minimum-2 divisions left of center screen Actual - _____ Maximum-2 divisions right of center screen
		step 14	Minimum-3 divisions left of center screen Actual - _____ Maximum-3 divisions right of center screen

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Paragraph Number	Test		Results
3-9	Time Interval Accuracy Test (cont)	channel 2 step 17	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen
		step 18	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen
		step 19	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen
		step 20	Minimum-1 division left of center screen Actual - _____ Maximum-1 division right of center screen

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Paragraph Number	Test	Results
3-9	Time Interval Accuracy Test (cont) step 21	Minimum-2 divisions left of center screen Actual - _____ Maximum-2 divisions right of center screen
3-10	Trigger Sensitivity Test channel 1 step 3	Waveform remains Coherent Yes____ No____
	channel 2 step 5	Waveform remains Coherent Yes____ No____
	step 7	Waveform remains Coherent Yes____ No____
	channel 1 step 10	Waveform remains Coherent Yes____ No____
	Trigger channel 3 step 13	Waveform remains Coherent Yes____ No____
	step 16	Waveform remains Coherent Yes____ No____

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Paragraph Number	Test	Results
3-10	Trigger Sensitivity Test (cont)	
	Trigger channel 4 step 18	Waveform remains Coherent Yes____ No____
	step 21	Waveform remains Coherent Yes____ No____
3-11	Aperture Jitter Test channel 1 step 2	Width ≤300 ps peak-to-peak Yes____ No____
	channel 2 step 7	Width ≤300 ps peak-to-peak Yes____ No____

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ADJUSTMENTS

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SECTION 4

ADJUSTMENTS

4-1. INTRODUCTION

This section describes the adjustments required to return the instrument to peak operating capabilities after repairs have been made. Included in this section is a table of Recommended Test Equipment (table 4-1).

4-2. CALIBRATION INTERVAL

To maintain proper calibration, these adjustments should be made at approximately one year intervals or after 2000 hours of operation, whichever is less. Some or all of these adjustments may need to be made after repairs have been completed. Amount of use, environmental conditions, and the user's experience concerning the need for adjustment checks will contribute in deciding the adjustment interval.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures. The apparatus shall be disconnected from all voltage sources before it is opened for any adjustment, replacement, maintenance, or repair.

4-3. RECOMMENDED TEST EQUIPMENT FOR ADJUSTMENT PROCEDURES

The recommended test equipment for the adjustment procedures is listed in Table 4-1 Recommended Test Equipment.

NOTE

HP Model 54002A 50Ω 1:1 pods must be used for adjustment procedures.

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Table 4-1. Recommended Adjustment Test Equipment.

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Function Generator	50 Hz to 10 MHz sine wave, square wave, triangle, dc capability	HP 8116A
Programmable Pulse Generator	Adjustable Pulse Width, Adjustable leading and trailing edge slope, Adjustable Trigger Delay	HP 8161A/002
Digital Voltmeter	>0.3% accuracy at 1 Vdc	HP 3478A
Oscilloscope	Dual channel 5 ns sweep with X10 magnification	HP 54201A
Pulse Generator	Flat Pulse < 1 percent Perturbations	Tektronix PG506
Frequency Counter	Range: 50 MHz	HP 5381A
Divider Probe	10:1 division ratio	HP 10017A
Divider Probe	50 ohm resistive divider	HP 10020A
Product Support Kit	No substitute	HP Part No. 54100-69006

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4-4. DIGITAL POWER SUPPLY ADJUSTMENT

Description:

This procedure adjusts the DC voltages required for the digital circuits.

Equipment Recommended: **Model**

Digital Voltmeter ..... HP 3478A

Instrument Setup:

HP 54100A/D:	Digital Voltmeter:
None	DC Volts 4 and 1/2 Digits Autozero - On

Digital Power Supply Board (A13) Adjustment Location



Procedure:

1. Disconnect power cord and remove power supply shield.

WARNING

*Hazardous voltages capable of causing injury or death are present in the AC Power Supply board (A11) when power is applied and for a period of time after power is removed from the instrument. To avoid this hazard, **DO NOT** remove the top power supply shield until the LED on the AC Power Supply board (A11) is extinguished. This LED is visible through an inspection hole in the cover labeled "**DANGEROUS VOLTAGE EXISTS ON PRINTED CIRCUIT BOARD WHEN LED IS LIT**".*

2. Connect positive voltmeter lead to +5 V test point (actual voltage = +5.1 V).
3. Connect negative voltmeter lead to -5 V test point (actual voltage = -5.3 V).
4. Apply power and allow instrument to stabilize for 1 to 2 minutes.
5. Adjust A13R56 for a voltmeter reading of 10.4 Vdc ± 0.01 V.
6. Disconnect power and wait until LED on AC Power Supply board (A11) is extinguished before re-installing top power supply shield.

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4-5. DC OFFSET ADJUSTMENT

Description:

DC Offset is adjusted to position baseline at mid-screen when no signal is applied.

Equipment Recommended:

None

Instrument Setup:

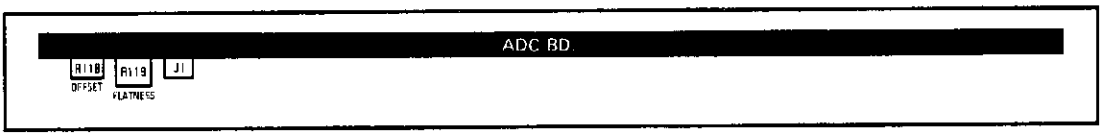
HP 54100A/D:

```
Channel 1 & 2 - Mode          - Normal
              - Display       - On
              - VOLTS/DIV     - 100 mV/div
              - OFFSET        - 0 V
       then;  - Mode          - Magnify
              - WINDOW SIZE   - 200 mV
              - POSITION      - 0.0 V

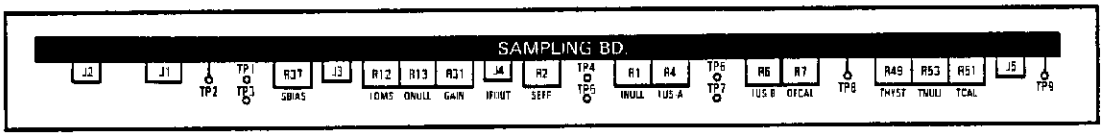
Timebase      - SEC/DIV       - 50 µs/div
              - DELAY         - 0
              - Delay Ref at  - Center
              - Auto

Display       - Mode          - Averaged
              - AVERAGES      - 8
              - Graticule     - Axes
```

Analog to Digital Board (A6/A8) Adjustment Locations



Sampling Board (A5/A7)



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4-5. DC OFFSET ADJUSTMENT (Continued)

Procedure:

1. Disconnect IFOUT (J4) cable from A5 assembly and turn channel 2 off.
2. Adjust A6R118 (OFFSET) until baseline overlays center screen.
3. Magnify baseline to 12.5 mV/division and fine adjust baseline to center screen with A6R118.
4. Reconnect IFOUT cable to A5 assembly.
5. Turn channel 1 off and channel 2 on.
6. Disconnect IFOUT (J4) cable from A7 assembly.
7. Adjust A8R118 (OFFSET) until baseline overlays center screen.
8. Magnify baseline to 12.5 mV/division and fine adjust baseline to center screen with A8R118.
9. Reconnect IFOUT cable to A7 assembly.

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4-6. INPUT AND OUTPUT OFFSET NULL ADJUSTMENT

Description:

While the actual voltage at the channel 1 and 2 input connectors is measured, the input null is adjusted for a minimum voltmeter reading. The output null is then adjusted until the trace overlays center graticule line.

Equipment Recommended: **Model**

Digital Voltmeter ..... HP 3478A

Instrument Setup:

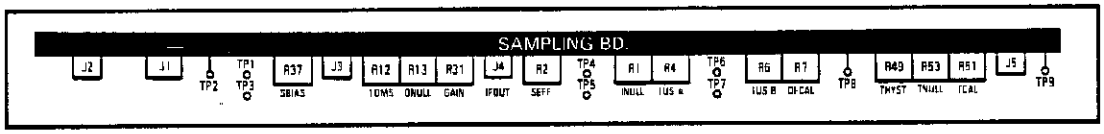
HP 54100A/D:

```
Channel 1 & 2 - Mode          - Normal
              - Display       - On
              - VOLTS/DIV     - 10 mV/div
              - OFFSET        - 0 V

Timebase      - SEC/DIV       - 100 µs/div
              - Delay Ref at  - Center
              - Auto

Display       - Mode          - Averaged
              - AVERAGES      - 8
              - Split Screen  - Off
              - Graticule     - Axes
```

Sampling Board (A5/A7) Adjustment Locations



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4-6. INPUT AND OUTPUT OFFSET NULL ADJUSTMENT (Continued)

Procedure:

NOTE

Verify the channel 1 and 2 vertical sensitivities are set to 10 mV/division.

1. Verify channel 1 offset is set to 0.00 V and turn channel 2 off.
2. With voltmeter, monitor voltage on channel 1 input BNC connector.
3. Adjust A5R1 (INULL) for a voltmeter reading of < 0.1 mV.
4. Change channel 1 vertical sensitivity to 100 mV/division.
5. Remove voltmeter from input BNC connector.
6. Adjust A5R13 (ONULL) until trace overlays center graticule line.

NOTE

*While making this adjustment it is helpful to press **CLEAR DISPLAY** key repeatedly.*

7. Turn channel 1 off and channel 2 on.
8. Verify channel 2 Offset is set to 0.00 V.
9. Using voltmeter, monitor voltage on channel 2 input BNC connector.
10. Adjust A7R1 (INULL) for a voltmeter reading of < 0.1 mV.
11. Change channel 2 vertical sensitivity to 100 mV/division.
12. Remove voltmeter from input BNC connector.
13. Adjust A7R13 (ONULL) until trace overlays center graticule line.

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4-7. SAMPLER BIAS AND SAMPLING EFFICIENCY ADJUSTMENTS

Description:

Sampler bias is adjusted for an abrupt change in overshoot on the displayed waveform. Sampler efficiency is adjusted for a minimum step that occurs 25 ns after the pulse's rising edge.

Equipment Recommended: **Model**

Pulse Generator ..... Tektronix PG506

Instrument Setup:

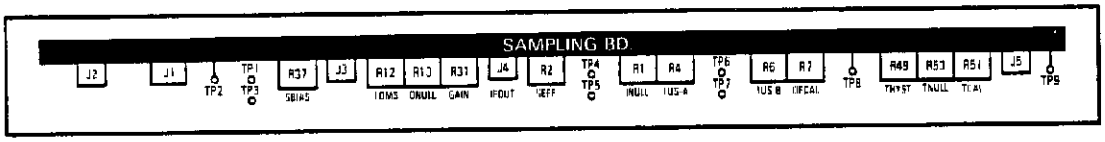
HP 54100A/D:

Will be setup during procedure

Pulse Generator:

Mode - Fast Rise
Period - 2 ms
Pulse Amplitude - 300 mV

Sampling Board (A5/A7) Adjustment Locations



Procedure:

1. Connect positive fast rise output of flat pulser to channel 1 input using a large diameter cable (ie. RG8/U).

2. Connect trigger output of flat pulser to channel 3 input.

3. Press ***AUTO SCALE*** key.

4. Setup HP 54100A/D as follows:

Channel 1 & Channel 2	- Mode	- Normal	Timebase	- SEC/DIV	- 5 ns/div
	- Display	- On		- DELAY	- 20 ns
	- VOLTS/DIV	- 50 mV/div		- Delay Ref at	- Center
	- OFFSET	- -150 mV			
Trigger	- Mode	- Edge	Display	- Mode	- Averaged
	- Source	- Trig 3		- AVERAGES	- 2
	- LEVEL	- 1 V		- Split Screen	- Off
	- Slope	- Positive		- Graticule	- Axes
	- HOLDOFF Time	- 70 ns			

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4-7. SAMPLER BIAS AND SAMPLER EFFICIENCY ADJUSTMENTS (Continued)

NOTE

Particular care should be taken to minimize the step that occurs 25 ns after rising edge of pulse. Figure 4-1 shows the sampling efficiency when it is adjusted to optimum. Figure 4-2 shows the sampling efficiency when it is over-compensated and figure 4-3 shows the sampling efficiency when it is under-compensated.

NOTE

If a relatively flat pulse is not obtained, then it may be difficult to adjust the SBIAS adjustment. Therefore, repeat this procedure.

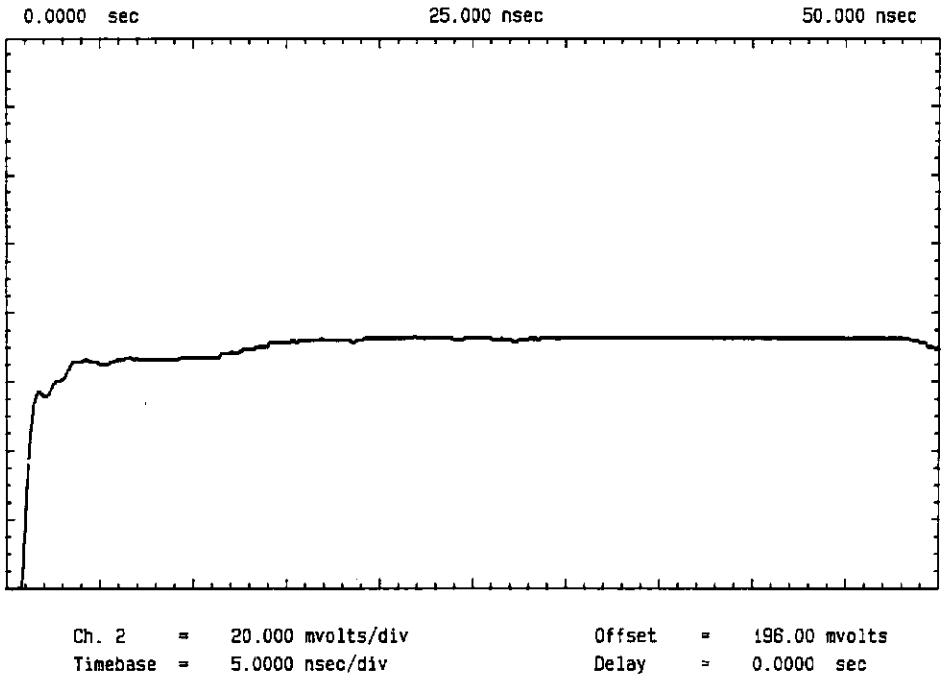


*Figure 4-1. Sampling Efficiency **Optimum** Adjustment*

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4-7. SAMPLER BIAS AND SAMPLING EFFICIENCY ADJUSTMENTS (Continued)

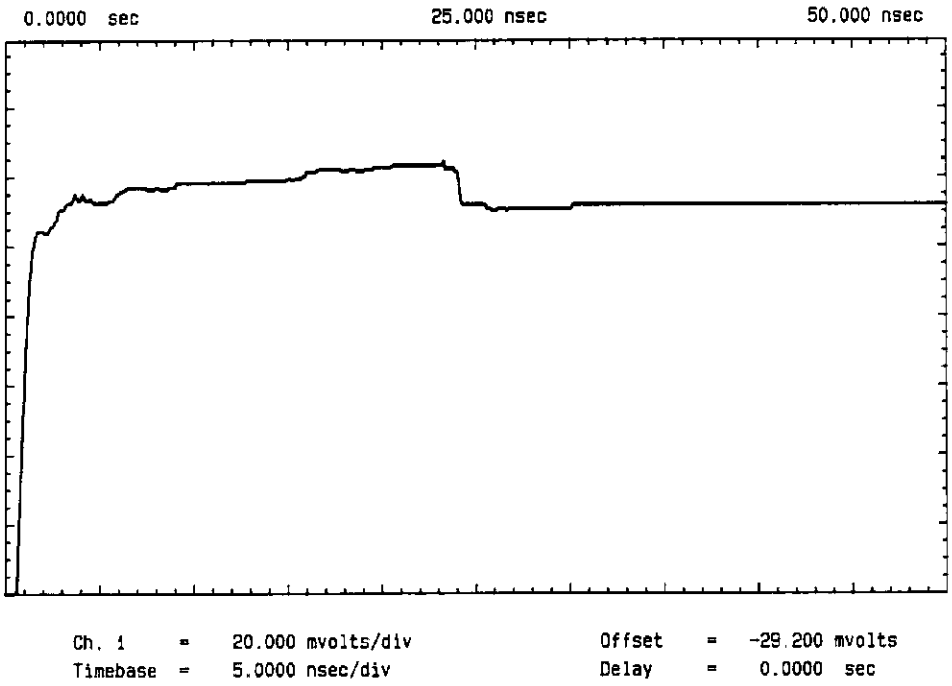


Figure 4-2. Sampling Efficiency Over-compensated

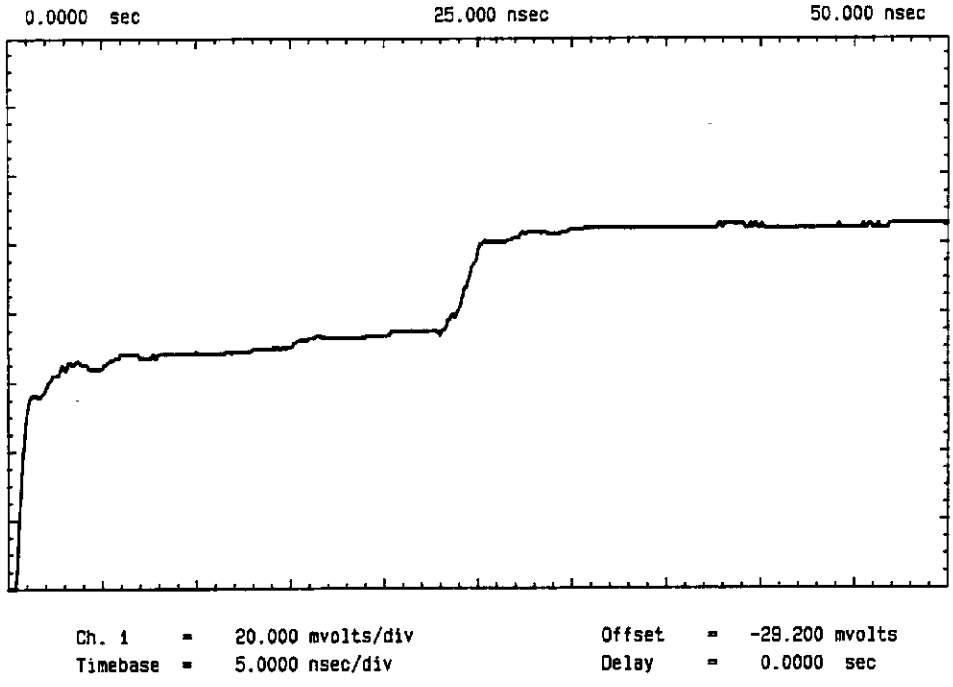


Figure 4-3. Sampling Efficiency Under-compensated

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4-7. SAMPLER BIAS AND SAMPLING EFFICIENCY ADJUSTMENTS (Continued)

5. Adjust A5R37 (SBIAS) fully counter-clockwise (CCW).

6. Short A5TP1 to ground test point (A5TP2) next to A5TP1.

7. Adjust A5R37 (SBIAS) clockwise (CW) until just before positive portion of pulse amplitude (>25 ns after the leading edge) abruptly decreases.

8. Remove short on A5TP1. This will shift the operating bias slightly to a stable operating point.

NOTE

Only the 25 ns pulse need be adjusted flat in this step. Three other flatness adjustments will be performed later.

9. Adjust A5R2 (SEFF) for flattest pulse response possible. Periodically pressing ***CLEAR DISPLAY*** helps in making this adjustment.

NOTE

The pulse response will not be completely flat but this will be corrected later. If the positive portion of the pulse amplitude does not abruptly decrease, then center the SEFF adjustment (A5R2) and repeat step 7.

10. Connect positive fast rise output of flat pulser to channel 2 input using a large diameter cable (ie. RG8/U).

11. Turn channel 1 off and channel 2 on.

12. Adjust A7R37 (SBIAS) fully counter-clockwise (CCW).

13. Short A7TP1 to ground test point (A7TP2) next to A7TP1

14. Adjust A7R37 (SBIAS) clockwise (CW) until just before positive portion of pulse amplitude (>25 ns after the leading edge) abruptly decreases.

15. Remove short on A7TP1. This will shift the operating bias slightly to a stable operating point.

NOTE

Only the 25 ns pulse need be adjusted flat in this step. Three other flatness adjustments will be performed later.

16. Adjust A7R2 (SEFF) for flattest pulse response possible. Periodically pressing ***CLEAR DISPLAY*** helps in making this adjustment.

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4-8. FLATNESS ADJUSTMENTS

Description:

Flatness is adjusted for flattest response.

Equipment Recommended: **Model**

Pulse Generator ..... Tektronix PG506

Instrument Setup:

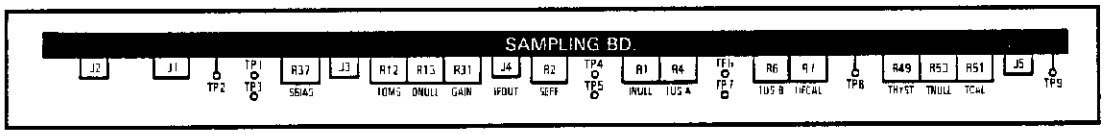
HP 54100A/D:

Will be setup during procedure

Pulse Generator:

Mode - Fast Rise
Period - 20 ms
Pulse Amplitude - 300 mV
Positive Output

Sampling Board (A5/A7) Adjustment Locations



Procedure:

1. Connect positive fast rise output of flat pulser to channel 1 input using a large diameter cable (ie. RG8/U).

2. Connect trigger output of flat pulser to channel 3 input.

3. Press ***AUTO SCALE*** key.

4. Setup HP 54100A/D as follows:

```
Channel 1 - Mode          - Normal      Display  - Mode          - Averaged
   &      - Display       - On                   - AVERAGES      - 2
Channel 2 - VOLTS/DIV     - 50 mV/div            - Split Screen  - Off
          - OFFSET        - -150 mV              - Graticule     - Axes

Trigger   - Mode          - Edge        Timebase - SEC/DIV   - 2 ms/div
          - Source        - Channel 3              Delay     - 0 sec
          - LEVEL         -  1 V                   Delay Ref-at Center
          - Slope         - Positive               Trig      - Trig'd
          - HOLDOFF Time  - 70 ns
```


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4-8. FLATNESS ADJUSTMENTS (Continued)

Procedure:

5. Turn channel 1 on and channel 2 off.

6 Adjust A5R12 (10 ms) for flattest response on positive portion of pulse.

NOTE

Using a DELTA V Marker for a flat reference line simplifies adjustment.

7. Change pulse generator's period to 2 ms and set 54100A/D SEC/DIV to 1 μs/div.

8. Adjust A5R4 (1 μs-A) for flattest response with no overshoot.

9. Adjust A5R6 (1 μs-B) for flattest response with no overshoot.

NOTE

Because of interaction between adjustments, steps 8 and 9 may need to be repeated to obtain flattest response.

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4-8. FLATNESS ADJUSTMENTS (Continued)

10. Turn channel 1 off and channel 2 on.

11. Set flat pulser PERIOD to 20 ms, and HP 54100A/D as follows:
SEC/DIV to 2 ms, Delay to 0 s, and Average to 2.

12. Connect pulse generator's output to channel 2.

13. Adjust A7R12 (10 ms) for flattest response on positive portion of pulse.

14. Change pulse generator's PERIOD to 2 ms and HP 54100A/D SEC/DIV to 1 μs/div.

15. Adjust A7R4 (1μs-A) for flattest response with no overshoot.

16. Adjust A7R6 (1μs-B) for flattest response.

NOTE

Because of interaction between adjustments, steps 15 and 16 may need to be repeated to obtain the flattest response.

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4-9. OFFSET CALIBRATION ADJUSTMENT

Description:

With the HP 54100A/D set to the same offset value as the function generator output, the OFCAL is adjusted until the trace overlays center screen.

Equipment Recommended: **Model**

Function Generator ..... HP 8116A
Digital Voltmeter ..... HP 3478A

NOTE

A dc power supply can be used to perform this adjustment in place of the HP 8116A function generator.

Instrument Setup:

HP 54100A/D:

```
Channel 1 - Mode        - Normal
   &      - Display     - On
Channel 2 - VOLTS/DIV   - 100 mV/div
          - OFFSET      - +1.2 V

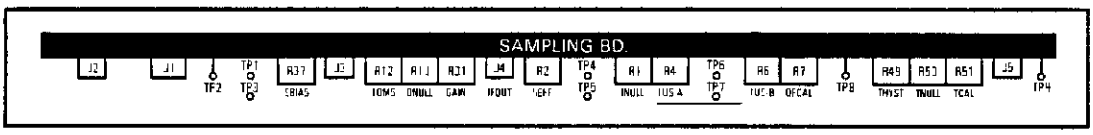
Timebase - SEC/DIV      - 20 ns/div
         - Delay Ref at - Center screen
         - Sweep        - Auto

Display  - Mode         - Averaged
         - AVERAGES     - 8
         - Split Screen - Off
         - Graticule    - Axes
```

Function Generator: or DC Power Supply:

```
Mode     -   DC
Offset   -  +1.2 V
Waveforms - All Off
```

Sampling Board (A5/A7) Adjustment Locations



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4-9. OFFSET CALIBRATION ADJUSTMENT (Continued)

Procedure:

1. Turn channel 2 off.
2. Connect function generator's output to voltmeter and channel 1 using a BNC Tee connector at scope's input.
3. While monitoring voltmeter, adjust function generator's output for a +1.2 V dc level.
4. Adjust A5R7 (OFCAL) until trace overlays center axis.
5. Change HP 54100A/D channel 1 offset to -1.2 V and function generator's offset to -1.2 V.
6. Verify trace is at center screen within ±1 minor division.
7. Turn channel 1 off and channel 2 on.
8. Connect function generator's output to voltmeter and channel 2 using a BNC TEE connector at oscilloscope's input.
9. While monitoring voltmeter, adjust function generator's output for a +1.2 V dc level.
10. Adjust A7R7 (OFCAL) until trace overlays center axis.
11. Change HP 54100A/D channel 2 offset to -1.2 V and function generator's offset to -1.2 V.
12. Verify trace is at center screen within ±1 minor division.

NOTE

If trace is not within ±1 minor division of center screen, then readjust paragraphs 4-5 through 4-9. If these adjustments have been repeated and the trace is still not within specifications, then a problem may exist. Refer to the section 6D, Troubleshooting.

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4-10. GAIN ADJUSTMENTS

Description:

A positive dc voltage is applied to the input and the gain is adjusted until trace is in the correct position. Then a negative voltage is applied to the input and trace position is checked.

Equipment recommended: **Model**

Function Generator ..... HP 8116A
Digital Voltmeter ..... HP 3478A

NOTE

A dc power supply can be used in place of the HP 8116A function generator.

Instrument Setup:

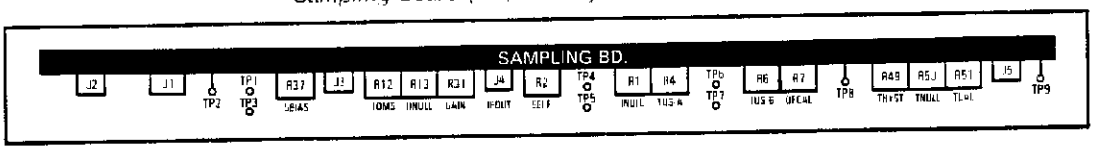
HP 54100A/D:

Channel 1 & 2	- Mode	- Normal
	- Display	- On
	- VOLTS/Div	- 100 mV/div
	- OFFSET	- 0 V
Timebase	- SEC/DIV	- 50 µs
	- DELAY	- 0
	- Delay Ref at	- Center screen
	- Sweep	- Auto
Trigger	- Mode	- Edge
	- Source	- Chan 1
	- Level	- 0 V
Display	- Mode	- Averaged
	- AVERAGES	- 8
	- Split Screen	- Off
	- Graticule	- Grid

Function Generator:

Mode	- DC
Offset	- +300 mV
Waveform	- All off

Sampling Board (A5/A7) Adjustment Locations



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4-10. GAIN ADJUSTMENTS (Continued)

Procedure:

1. Connect function generator's output to voltmeter and channel 1 using a BNC Tee connector.
2. Turn channel 2 off.
3. While monitoring voltmeter, adjust function generator's output level to +300 mV.
4. Adjust A5R31 (GAIN) until trace is 3 divisions above center screen.
5. Change function generator's output level to -300 mV.
6. Trace should now be 3 divisions below center screen.

NOTE

It may be necessary to repeat steps 3 through 6 and readjust A5R31 in order to minimize the errors of these two operating points.

7. Connect function generator's output to channel 2.
8. Turn channel 2 on and channel 1 off.
9. Adjust function generator's output level to +300 mV.
10. Adjust A7R31 (GAIN) until trace is 3 divisions above center screen.
11. Change function generator's output level to -300 mV.
12. Trace should now be 3 divisions below center screen.

NOTE

It may be necessary to repeat steps 9 through 12 and readjust A7R31 in order to minimize the errors of these two operating points.

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4-11. SAMPLING BOARD TRIGGER ADJUSTMENTS

Description:

This procedure adjusts the Trigger Hysteresis, Trigger Offset Null, and Trigger Level.

Equipment Recommended: **Model**

Function Generator ..... HP 8116A

Instrument Setup:

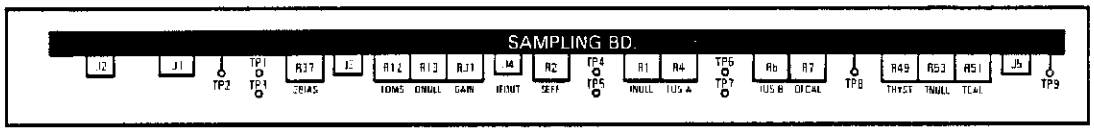
HP 54100A/D:

Channel 1 & Channel 2	- Mode	- Normal
	- Display	- On
	- VOLTS/DIV	- 100 mV/div
	- OFFSET	- 0 V
Timebase	- SEC/DIV	- 50 µs
	- DELAY	- 0
	- Delay Ref at	- Center screen
	- Sweep	- Auto
Trigger	- Mode	- Edge
	- Source	- Chan 1
	- LEVEL	- 0 V
	- Slope	- Positive
	- HOLDOFF Time	- 70 ns
Display	- Mode	- Averaged
	- AVERAGES	- 8
	- Split Screen	- Off
	- Graticule	- Axes

Function Generator:

Mode	- Normal
Frequency	- 1 kHz
Offset	- 0 V
Duty Cycle	- 50%
Waveform	- Sine wave

Sampling Board (A5/A7) Adjustment Locations



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4-11. SAMPLING BOARD TRIGGER ADJUSTMENTS (Continued)

Procedure:

1. Trigger Hysteresis Adjustment.

   a. Connect function generator's output to channel 1.

   b. Adjust function generator's output until an 8 division peak-to-peak amplitude is displayed.

   c. In Trigger Menu, switch slope repeatedly between Pos and Neg. The difference between voltage levels at time zero between Pos and Neg is hysteresis. The actual trigger level is halfway between the two observed levels.

   d. Adjust A5R49 (THYST) until the voltage difference (Y axis) at time zero is one minor division.

2. Trigger Offset Null Adjustment.

   a. Observe waveform at time zero as slope is switched.

   b. Adjust A5R53 (TNULL) until the two voltage levels at time zero are centered above and below 0 V.

3. Trigger Level Calibration Adjustment.

   a. Change channel 1 Offset to 1.2 V.

   b. Change Trigger Level to 1.2 V.

   c. Set function generator's high level output (HIL) to 1.6 V and low level output (LOL) to 0.8 V.

   d. Adjust A5R51 (TCAL) until voltage levels at time zero, as the slope is switched, are centered above and below 0 V.

   e. Change channel 1 Offset to -1.2 V.

   f. Change Trigger Level to -1.2 V.

   g. Set function generator's high level output (HIL) to -0.8 V, and low level output (LOL) to -1.6 V.

   h. Verify trigger level switching at center screen is within two minor divisions while switching slope.

4. Reset trigger level to 0 V and repeat steps 1 through 3 for channel 2 and Trigger Source 2. Adjustments for channel 2 are on the A7 assembly.

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4-12. PULSE FLATNESS ADJUSTMENT

Description:

The pulse response of the ADC is adjusted for optimum flatness.

Equipment Recommended: **Model**

Calibration Generator ..... Tektronix PG506

Instrument Setup:

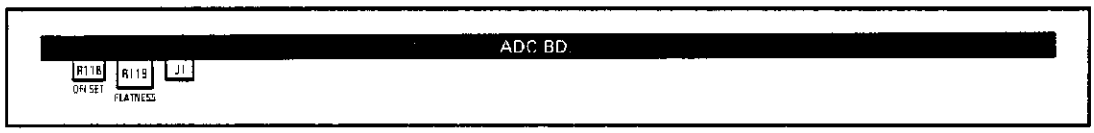
HP 54100A/D:

Channel 1 & Channel 2	- Mode	- Normal
	- Display	- On
	- VOLTS/DIV	- 100 mV/div
	- OFFSET	- 0 V
Timebase	- SEC/DIV	- 2 ms/div
	- DELAY	- 0
	- Delay Ref at	- Center
Trigger	- Mode	- Edge
	- Source	- Trig 3
	- LEVEL	- +1 V
	- Slope	- positive
	- HOLDOFF Time	- 70 ns
Display	- Mode	- Averaged
	- AVERAGES	- 2
	- Graticule	- Axes

PG506:

Period	- 20 ms
Pulse Amplitude	- 300 mV

Analog to Digital Board (A6/A8) Adjustment Locations



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4-12. PULSE FLATNESS ADJUSTMENT

Procedure:

1. Turn channel 1 on and channel 2 off.
2. Connect pulse generator's trigger output to channel 3.
3. Connect positive fast rise output of calibration generator to channel 1.
4. Adjust A6R119 for optimum flatness.
5. Turn channel 2 on and channel 1 off.
6. Connect calibration generator's positive fast rise output to channel 2.
7. Adjust A8R119 for optimum flatness.

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4-13. MAIN TRIGGER BOARD CALIBRATION ADJUSTMENTS

Description:

Hysteresis, offset and trigger level are calibrated by observing the voltage level where displayed waveform crosses the zero time reference which is set to center screen.

Note

*The adjustment procedures in paragraphs 4-5, 4-6, 4-9, 4-10, and 4-11 **(IN THAT ORDER)** must be performed before the trigger circuits are calibrated.*

Equipment Recommended: **Model**

Function Generator ..... HP 8116A

Instrument Setup:

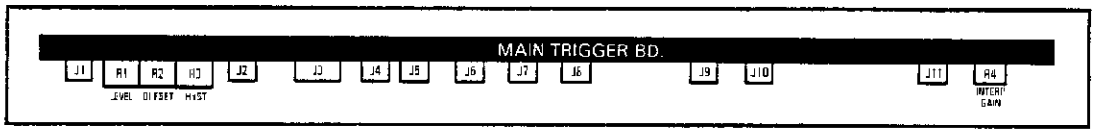
HP 54100A/D:

Channel 1	- Mode	- Normal
	- Display	- On
	- VOLTS/DIV	- 10 mV/div
	- OFFSET	- 0 V
Timebase	- SEC/DIV	- 50 µs/div
	- DELAY	- 0 Sec
	- Delay Ref at	- Center screen
	- Sweep	- Trig'd
Trigger	- Mode	- Edge
	- Source	- Trig 3
	- LEVEL	- 0 V
	- Slope	- Positive
	- HOLDOFF Time	- 70 ns
Display	- Mode	- Averaged
	- AVERAGES	- 16
	- Split Screen	- Off
	- Graticule	- Axes

Function Generator:

Mode	- Normal
Frequency	- 1 kHz
Offset	- 0 V
Waveform	- Sine wave
Duty Cycle	- 50%

Main Trigger Board (A9) Adjustment Locations



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4-13. MAIN TRIGGER BOARD CALIBRATION ADJUSTMENTS (Continued)

Procedure:

1. Connect function generator's output to channel 1 and trigger 3 inputs using a BNC Tee connector.
2. Adjust sine wave amplitude for an approximate 8 division peak-to-peak displayed signal.
3. Waveform should be triggered with 0 volt crossing at approximately center screen.
4. The hysteresis (A9R3) may require adjustment to obtain triggering.
5. Select ***Trigger*** menu, toggle slope repeatedly between Pos and Neg.

NOTE

The difference between voltage levels at time zero (center screen) as slope is switched is hysteresis. The actual trigger level is halfway between the two observed levels, that is, at the center of the hysteresis band.

6. Adjust A9R3 (Hysteresis adjustment) for a voltage difference (Y axis) of 10 mV (1 major division) at time zero as slope is switched.
7. As slope is switched, adjust A9R2 (Offset), until the two voltage levels at time zero are centered above and below 0 V.
8. Set channel 1 sensitivity to 100 mV/division and adjust 1 kHz sine wave for approximately 8 divisions peak-to-peak.
9. Set channel 3 trigger level and channel 1 offset to 1.2 volts.
10. Adjust function generator's offset until sine wave is centered on screen (approximately 1.8 V).
11. Adjust Level Cal (A9R1) until voltage level at time zero is centered around center vertical graticule (Y axis) as slope is toggled.
12. Set channel 3 trigger level and channel 1 offset to -1.2 volts.
13. Adjust function generator's offset to center signal on screen (approximately -1.8 V). As slope is toggled, verify voltage levels at time zero are centered with two minor divisions of vertical center.

NOTE

*If the voltage levels are not within ±2 minor divisions of center screen at time = 0 sec, then readjust the following procedures 4-5 through 4-12 (**IN THAT ORDER**). If these adjustments have been repeated and the voltage levels are still not within specifications, then a problem may exist. Refer to section 6D, Troubleshooting.*

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4-14. FINE INTERPOLATOR CALIBRATION

Description:

Interpolator gain is adjusted for a leading edge without any area of discontinuity.

Equipment Recommended: **Model**

Programmable Pulse Generator ..... HP 8161A

Instrument Setup:

HP 54100A/D:

```
Channel 1 - Mode          - Normal
          - Display       - On
          - VOLTS/DIV     - 200 mV/div
          - OFFSET        - -1.2 V

Channel 2 - Mode          - Normal
          - Display       - Off
          - VOLTS/DIV     - 1 V/div

Timebase  - SEC/DIV       - 1 ns/div
          - DELAY         - 0
          - Delay Ref at  - Center screen
          - Trg'd

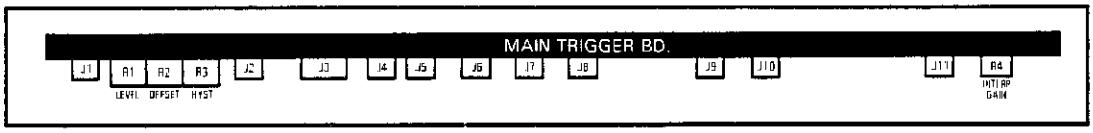
Trigger   - Mode          - Edge
          - Source        - 2
          - LEVEL         - 1.2 V
          - Slope         - pos
          - HOLDOFF Time  - 100 ns

Display   - Mode          - Normal
          - DISPLAY TIME  - 2 seconds
          - Graticule     - Axes
```

Pulse Generator:

```
Period - 1 µs
Width  - 500 ns
Leading edge
 (LEE) - 1 ns
Trailing edge
 (TRE) - 1 ns
High level
 (HIL) - -0.8 V
Low level
 (LOL) - -1.6 V
Delay  - 1 ns
Output - Enable
Complement - Off
```

Main Trigger Board (A9) Adjustment Locations



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4-14. FINE INTERPOLATOR CALIBRATION (Continued)

Procedure:

1. Preset A9R4 (INTERP GAIN) on Main Trigger asembly fully counter-clockwise (CCW).
2. Connect pulse generator's output to channel 1.
3. Connect pulse generator's trigger output to channel 2.
4. Observe display for a waveform area where no data is present. Refer to figure 4-4.

NOTE

It may be necessary to adjust both the HP 54100A/D and the pulse generator delay to place the area of discontinuity in the center of the screen.

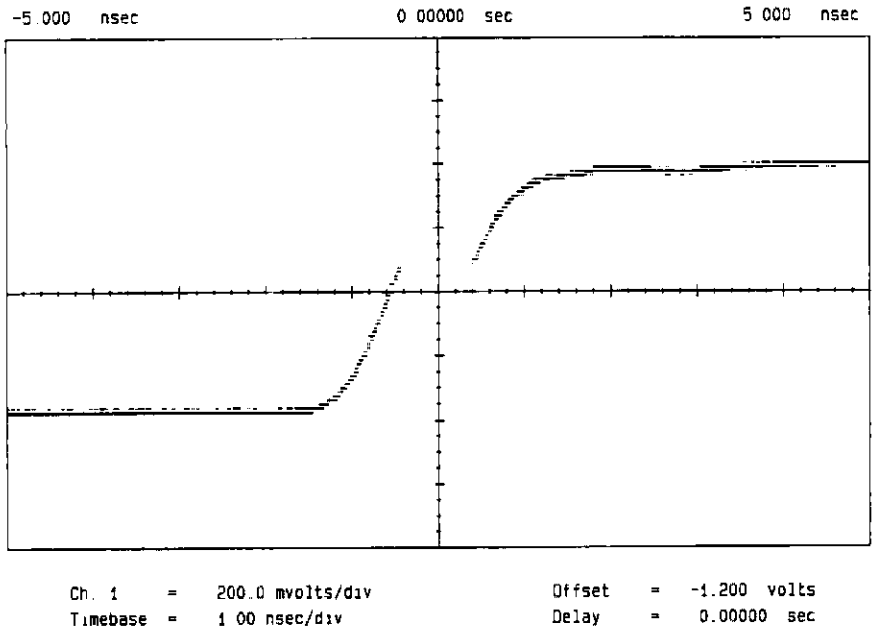


Figure 4-4. Leading edge with area of discontinuity (no data present).

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4-14. FINE INTERPOLATOR CALIBRATION (Continued)

5. Slowly change pulse generator's delay in 100 ps steps until area of discontinuity is centered vertically on display. Refer to figure 4-5.

6. With Timebase Delay function, move discontinuity until it is centered on middle vertical graticule. Timebase Delay function is obtained by selecting ***Timebase*** menu, then ***DELAY*** function. Refer to figure 4-3.

NOTE

It may be helpful to position the Delta V markers slightly above and slightly below the area of discontinuity. This will help keep track of the area of concern while further adjustments are made.

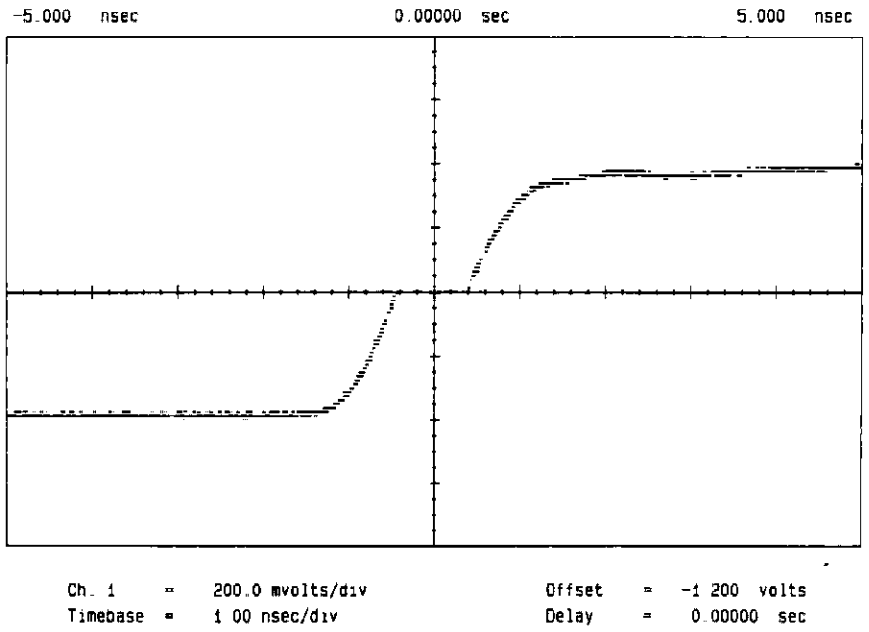


Figure 4-5. Area of discontinuity is centered vertically.

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4-14. FINE INTERPOLATOR CALIBRATION (Continued)

7. Change sweep speed to 500 ps/division.

8. Using channel 1 VERTICAL MAGNIFY MODE menu, center window and expand to 40 mV/division. (Window size = 320 mV) Refer to figure 4-6

9. Slowly adjust A9R4 (INTERP GAIN) to decrease hole size in displayed waveform

NOTE

Do not completely eliminate discontinuity at this time.

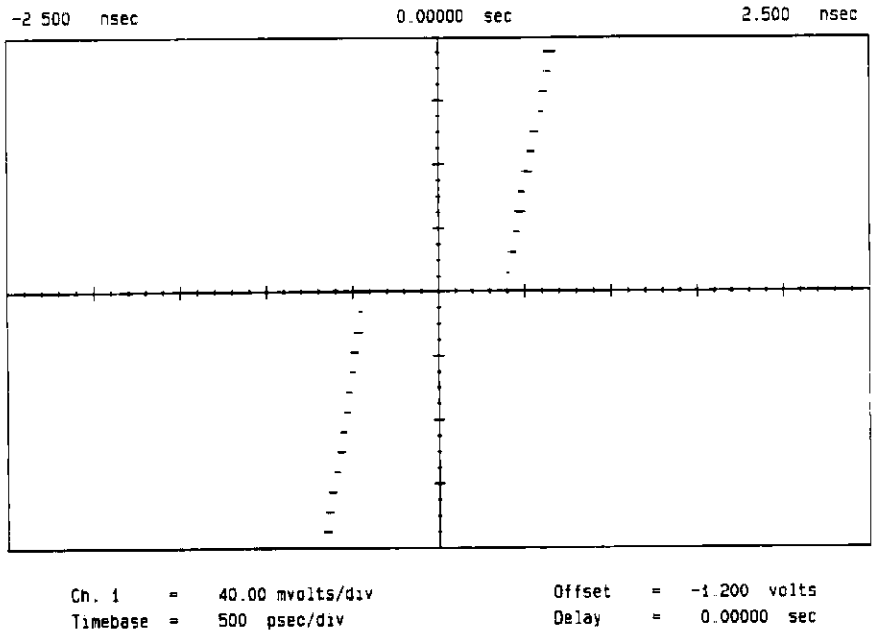


Figure 4-6. Area of discontinuity is centered and expanded.

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4-14. FINE INTERPOLATOR CALIBRATION (Continued)

10. Periodically adjust Timebase DELAY to keep area of concern at center screen.

11. As more resolution is needed, increase sweep speed to 100 ps/division.

12. Change Display to Averages = 2048 and Graticule to Frame.

13. Continue to rotate A9R4 (INTERP GAIN) clockwise until there is no longer a discontinuity in the area of concern.

14. Refer to figure 4-7 for desired waveform at correct adjustment. A9R4 is adjusted correctly when there is a continuous smooth trace where there was once discontinuity.

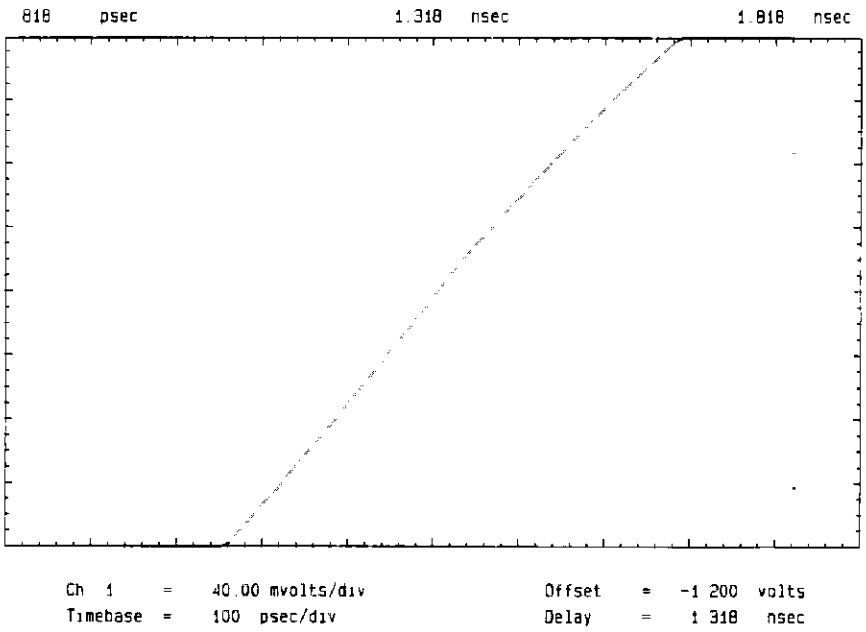


Figure 4-7. Waveform when adjustment is correct.

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4-14. FINE INTERPOLATOR CALIBRATION (Continued)

NOTE

If A9R4 is not adjusted correctly but is close, the display will have a small but very observable "S" shape as shown in figure 4-8.

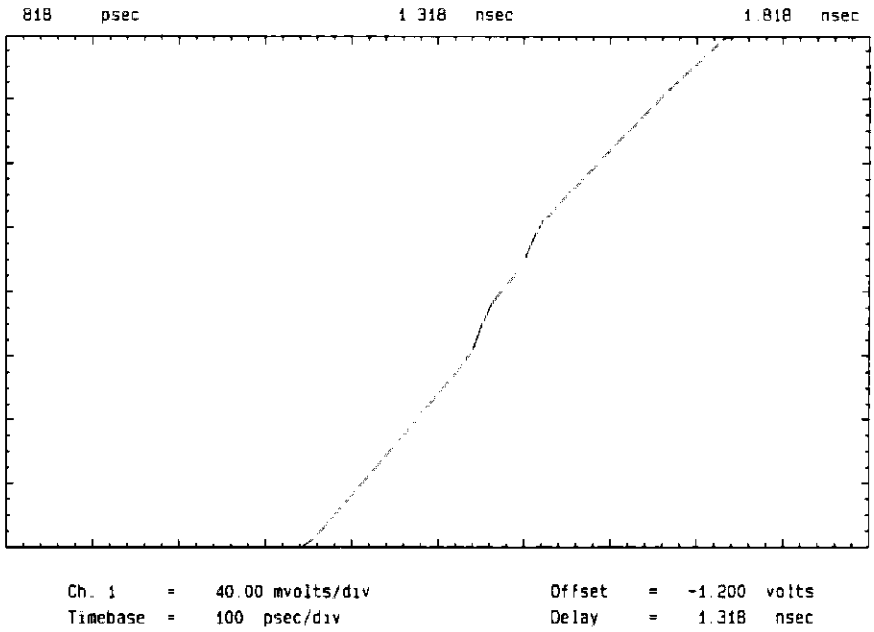


figure 4-8. Close adjustment but not correct (note small "S" shape).

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4-15. TRIGGER QUALIFIER CALIBRATION ADJUSTMENTS - HP 54100D

Description:

Hysteresis, offset and trigger level are calibrated by observing the voltage level where the displayed waveform crosses the zero time reference which is set to center screen.

Equipment Recommended: **Model**

Function Generator ..... HP 8116A

Instrument Setup:

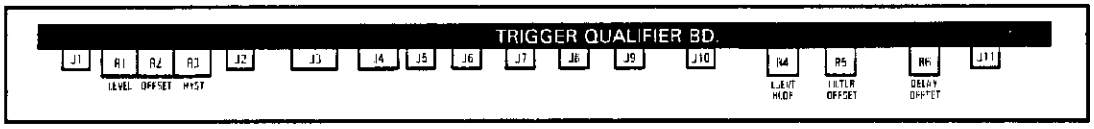
HP 54100D:

Channel 1	- Mode	- Normal
	- Display	- On
	- VOLTS/DIV	- 10 mV/div
	- OFFSET	- 0 V
Timebase	- SEC/DIV	- 50 µs/div
	- DELAY	- 0 Sec
	- Delay Ref at	- Center screen
Trigger	- Mode	- Edge
	- Source	- Trig 4
	- LEVEL	- 0 V
	- Slope	- Positive
	- HOLDOFF Time	- 100 ns
Display	- Mode	- Averaged
	- AVERAGES	- 16
	- Split Screen	- Off
	- Graticule	- Axes

Function Generator:

Mode	- Normal
Frequency	- 1 kHz
Offset	- 0 V
Waveform	- Sine wave
Duty Cycle	- 50%

Trigger Qualifier Board (A10) Adjustment Locations



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4-15. TRIGGER QUALIFIER CALIBRATION ADJUSTMENTS - HP 54100D (Continued)

NOTE

The vertical sensitivity and offset must be calibrated before trigger circuits are calibrated.

Procedure:

1. Connect function generator's output to both channel 1 and trigger 4 inputs using a BNC Tee connector.
2. Adjust sine wave amplitude for an approximate 8 division peak-to-peak displayed signal.
3. Waveform should be triggered with 0 volt crossing at approximately center screen.
4. The hysteresis (A10R3) may require adjustment to obtain triggering.
5. Select ***Trigger*** menu, toggle slope repeatedly between Pos and Neg.

NOTE

The difference between voltage levels at time zero (center screen) as slope is switched is the hysteresis. The actual trigger level is halfway between the two observed levels, that is, at the center of the hysteresis band.

6. Adjust A10R3 (Hysteresis adjustment) for a voltage difference (Y axis) of 10 mV (1 major division) at time zero as slope is switched.
7. As slope is switched, adjust A10R2 (Offset), until the two voltage levels at time zero are centered above and below 0 V.
8. Set channel 1 sensitivity to 100 mV/division and adjust the 1 kHz sine wave for approximately 8 divisions peak-to-peak.
9. Set trigger 4 and channel 1 offset to 1.2 volts.

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4-15. TRIGGER QUALIFIER CALIBRATION ADJUSTMENTS - HP 54100D (Continued)

10. Adjust function generator's offset until sine wave is centered on screen (approximately 1.8 V).

11. Adjust Level Cal (A10R1) until voltage levels at time zero are centered above and below 0 V as slope is toggled.

12. Set trigger level and channel 1 offset to -1.2 volts.

13. Adjust function generator's offset to center signal on screen (approximately -1.8 V).

14. While trigger slope is toggled, verify voltage levels at time zero are within two minor divisions of vertical center.

NOTE

If the trace is not within ±2 minor divisions of vertical center, then readjust steps 4-5 through 4-15 ***(IN THAT ORDER).*** *If these adjustments have been repeated and the voltage levels are still not within specifications, a problem may exist. Refer to section 6D, Troubleshooting.*

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4-16. DELAY/PATTERN TIME OSCILLATOR ADJUSTMENT - HP 54100D

Description:

The oscillator is adjusted to 50 MHz.

Equipment Recommended: **Model**

Frequency Counter ..... HP 5381A
Miniature Divider Probe ..... HP 10017A

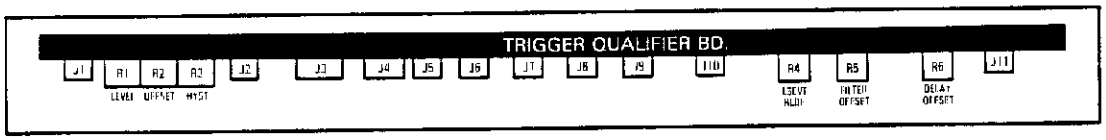
Instrument Setup:

HP 54100D:

```
Timebase  - Sweep        - Trg'd

Trigger   - Mode         - Pattern, "XXXX When Present > 30 ns"
          - HOLDOFF Time - 70 ns
```

Trigger Qualifier (A10) Board Adjustment Locations



NOTE

The right side cover must be removed to make the following adjustment.

Procedure:

1. Connect frequency counter to J11 on A9 board with a miniature divider probe.
2. Adjust A10C1 (OSC CAL) for a frequency of 50 MHz ±0.02 MHz.

Note

J11 is located approximately one-fourth of the way down the rear edge of the board and will accept a miniature probe tip.

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4-17. FILTER TIME OFFSET ADJUSTMENT - HP 54100D

Description:

Filter Offset is adjusted until oscilloscope will just trigger when a 20 ns pulse is applied.

NOTE

Startable Oscillator should be calibrated before the Filter Time Offset.

Equipment Recommended: **Model**

Programmable Pulse Generator ..... HP 8161A

Instrument Setup:

HP 54100D:

```
Channel 1 - Mode          - Normal
          - Display       - On
          - VOLTS/DIV     - 200 mV/div
          - OFFSET        - 0 V
Channel 2 - Display       - Off
Timebase  - SEC/DIV       - 5 ns/div
          - DELAY         - 0
          - Delay Ref at  - Center screen
          - Sweep         - Trg'd
Trigger   - Mode          - Edge
          - Source        - Chan 1
          - LEVEL         - 0 V
          - Slope         - Negative
          - HOLDOFF Time  - 70 ns

Display   - Mode          - Normal
          - DISPLAY TIME  - 500 ms
          - Split Screen  - Off
          - Graticule     - Axes

V-Markers - On
          - Chan          - 1
          - V(1)          - 0 V
          - V(2)          - 0 V

T-Markers - On
          - Start on Pos Edge 1
          - Stop on Neg Edge 1
```

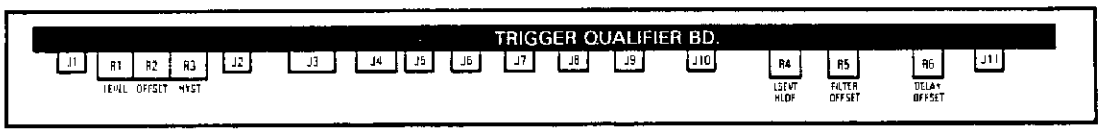
Pulse Generator:

```
Period - 300 ns
Width  - 20.0 ns
Delay  - 0 ns (DBL off)
High level
 (HIL) - +0.6 V
Low level
 (LOL) - -0.6 V
Leading edge
 (LEE) - 1 ns
Trailing edge
 (TRE) - 1 ns
Input Mode - Normal
Output Mode - Non Complemented
Output - Enabled
```


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4-17. FILTER TIME OFFSET ADJUSTMENT - HP 54100D (Continued)

Trigger Qualifier Board (A10) Adjustment Locations



Procedure:

1. Connect pulse generator's output to channel 1.

NOTE

The display should be an approximate 20 ns pulse with an amplitude of 6 divisions peak-to-peak, with the trailing edge at time zero.

2. Adjust the pulse generator's width to obtain as close as possible, but just under, a 20 ns pulse width as measured with Precise Edge Find.

NOTE

Use Precise Edge Find and not Autoparameters to measure pulse.

3. Increment pulse generator's high level (HIL) as a fine adjust to obtain a 20 ns ±100 ps pulse width.

4. Change trigger mode to Pattern: "HXXX When Present > 20 ns".

NOTE

"When Present" is obtained by pressing the "When Entered" key twice.

5. Adjust FILTER OFFSET (A10R5) until oscilloscope just triggers. Ideally, adjustment should be right on the threshold where the oscilloscope is intermittently triggering as indicated by an increase in jitter or slowed acquisition. If necessary, change SEC/DIV to a faster setting to see these effects better.

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4-18. LAST EVENT HOLDOFF ADJUSTMENT - HP 54100D

Description:

Last Event Holdoff is adjusted for a 4 ns delay after the second to the last event before main trigger is enabled.

Equipment Recommended: **Model**

Programmable Pulse Generator ..... HP 8161A

Instrument Setup:

NOTE

If Filter Time Adjustment (paragraph 4-17) has just been completed, setup channel 2 ONLY.

HP 54100D:

Channel 1	- Mode	- Normal
	- Display	- On
	- VOLTS/DIV	- 200 mV/div
	- OFFSET	- 0 V
Channel 2	- Mode	- Normal
	- Display	- On
	- VOLTS/DIV	- 100 mV/div
	- OFFSET	- -348 mV
Timebase	- SEC/DIV	- 5 ns/div
	- DELAY	- 0 V
	- Delay Ref at	- Center screen
	- Sweep	- Trg'd
Trigger	- Mode	- Edge
	- Source	- Chan 1
	- LEVEL	- 0 V
	- Slope	- Negative
	- HOLDOFF Time	- 70 ns
Display	- Mode	- Normal
	- DISPLAY TIME	- 500 ms
	- Split Screen	- Off
	- Graticule	- Axes

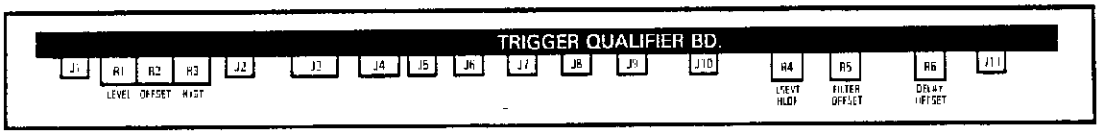
Pulse Generator:

Period - 300 ns
Width - 20.0 ns
Delay - 0 ns (DBL off)
High level (HIL) - +0.6 V
Low level (LOL) - -0.6 V
Leading edge (LEE) - 1 ns
Trailing edge (TRE) - 1 ns
Input Mode - Normal
Gate - Normal
Output - Non Complemented
Output - Enabled

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4-18. LAST EVENT HOLDOFF ADJUSTMENT - HP54100D (Continued)

Trigger Qualifier (A10) Board Adjustment Locations



Procedure:

1. Connect pulse generator's to channel 1.

2. Set HP 54100D trigger to Pattern Mode: "HXXX When Present > 20 ns".

3. Adjust pulse generator pulse's width using width (W) and high level (HIL) until oscilloscope is on the threshold of triggering.

4. Turn channel 1 OFF and channel 2 ON.

5. Remove cable from J10 (DOUT) on Trigger Qualifier assembly (A10), terminate J10 with 50 Ω. Connect J10 to a 12 inch SMB extender cable, HP part number 54111-69002. Connect the other end of the extender cable to a BNC (m) to SMB (m) adapter, HP part number 1250-0896. Connect the adapter to an HP 54002A probe pod on the scope's channel 2 input. The trigger should become stable. The extender cable and the adapter are part of the product support kit, HP part number 54100-69006.

NOTE

This 50 Ω termination may be accomplished by using an SMB to BNC Adapter and connecting to a 50 Ω load. An alternative is to use the SMB to BNC cable HP P/N 54100-61616 supplied in the product support kit HP P/N 54100- 69002.

6. Set SEC/DIV to 2 ns and increase DELAY to bring positive pulse's leading edge on channel 2 to precisely center screen

NOTE

Do not change DELAY setting for the following steps.

7. Change HP 54100D trigger to Evnt-Dly and set up as follows: After [Pos] Edge On [Chan 1], Trig On [2] Events, Of [Neg] Edge, On [Chan 1].

8. Observe positive transition on channel 2 to right of center screen and adjust LSEVT HLDF (A10R4) to position edge as close as possible to 2 divisions (4 ns) to right of center screen. Adjustment must be > 1.5 division (3 ns) and < 4 divisions (8 ns).

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4-19. DELAY OFFSET ADJUSTMENT - HP 54100D

Description:

Delay Offset is adjusted so trigger will enable on a negative pulse edge which occurs 30 ns after a positive pulse edge.

NOTE

Startable Oscillator and Last Event Holdoff calibrations should be performed prior to the Delay Offset Calibration.

Equipment Recommended: **Model**

Programmable Pulse Generator ..... HP 8161A

Instrument Setup:

HP 54100D:

```
Channel 1 - Mode          - Normal
          - Display       - On
          - VOLTS/DIV     - 200 mV/div
          - OFFSET        - 0 V
Timebase  - SEC/DIV       - 20 ns/div
          - DELAY         - 0
          - Delay Ref at  - Center screen
          - Sweep         - Trg'd
Trigger   - Mode          - Edge
          - Source        - Chan 1
          - LEVEL         - 0
          - Slope         - Negative
          - HOLDOFF Time  - 70 ns

Display   - Mode          - Normal
          - DISPLAY TIME  - 500 ms
          - Split Screen  - Off
          - Axes

V-Markers - On
          - Chan          - 1
          - V(1)          - 0 V
          - V(2)          - 0 V

T-Markers - On
          - Start on Pos Edge 1
          - Stop on Neg Edge 1
```

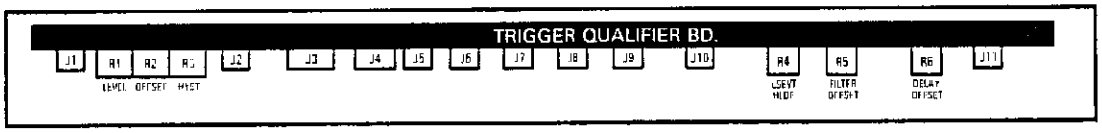
Pulse Generator:

```
Period - 300 ns
Width  - 30.0 ns
DBL    - 50 ns (Delay Off)
High level
 (HIL) - +0.6 V
Low level
 (LOL) - -0.6 V
Leading edge
 (LEE) - 1 ns
Trailing edge
 (TRE) - 1 ns
Gate   - Normal
Output - Non Complemented
Output - Enabled
Input
  Mode - Normal
```


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4-19. DELAY OFFSET ADJUSTMENT - HP 54100D (Continued)

Trigger Qualifier Board (A10) Adjustment Locations



Procedure:

1. Preset DELAY OFFSET (A10R6) fully clockwise.

2. Connect pulse generator's output to channel 1 input.

3. Adjust pulse generator's width to obtain as close as possible, but just under, a 30 ns width for first pulse as measured with Precise Edge Find.

4. Increment pulse generator's high level (HIL) as a fine adjust to obtain an observed 30 ns ±100 ps pulse width.

NOTE

Use Precise Edge Find and not Autoparameters to measure the pulse.

5. Set HP 54100D trigger to Time-Dly and setup as follows: After [Pos] Edge, On [Chan 1], Delay [30 ns] Then, Trig On [Neg] Edge, On [Chan 1]. The HP 54100D should be triggered on second pulses's negative edge.

NOTE

If a double pulse is not visible, then reenter the DBL value and repeat the procedure.

6. Adjust DELAY OFFSET (A10R6) to point where oscilloscope switches from triggering on second pulse to triggering on first pulse. Ideally this would be a point where oscilloscope is triggered equally on both negative edges as indicated by three pulses displayed on CRT.

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4-20. 81.699 MHZ MASTER OSCILLATOR OVERTONE TUNING

NOTE

Visually inspect the timebase board's bottom left corner to see if it contains A4C102 Recently manufactured instruments had several electrical components replaced by components with tighter electrical specifications If your instruement does not contain A4C102, do not perform this procedure.

Description:

The master oscillator is adjusted to ensure the circuit operates on the crystal's fifth harmonic.

NOTE

Do not perform this procedure during routine calibration. This procedure is only necessary after oscillator circuit has been replaced.

Equipment Recommended: **Model**

Oscilloscope ..... HP 54201A
50 Ω Resistive Divider probe ..... HP 10020

Instrument Setup:

HP 54100A/D:

NONE

HP 54201A:

```
CHANNEL A - on, 10 mV/div, 50 Ω coupling
CHANNEL B - off
Timebase  - 10 ns/div
Sweep     - Auto
Probe Attn- 50:1

Trigger   - CHANNEL A
          - Internal
          - Slope - Positive
          - Level 0 V

Probe     - HP Model 10020
          - 50 Ω resistive divider
          - 50:1 divider tip
          - Spanner
```

Timebase Board (A4) Adjustment Locations



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4-20. 81.699 MHZ MASTER OSCILLATOR OVERTONE TUNING (Continued)

Procedure:

1. Remove power cable.
2. Remove Trigger Qualifier PC assembly (A10) from slot 9.
3. Move Timebase PC assembly (A4) to slot 9.
4. Remove right side cover.
5. Apply power and let instrument temperature re-stabilize for approximately 10 minutes.
6. Connect 10020A probe to channel A of monitor oscilloscope and probe tip to A4TP1 on HP 54100A/D Timebase Board. Connect probe ground to square pad above A4TP1.

NOTE

A4TP1 (round pad) and the square pad for probe ground are on the front edge of the board midway between top and bottom.

7. A sine wave of approximately 80 MHz should be displayed on monitor oscilloscope.
8. Using a non-metallic adjustment tool, adjust A4C102 until the peak-to-peak amplitude of the oscillator sine wave is at its maximum value (≈600 mV).

NOTE

A4C102 is at the bottom front of PC board below J1

9. Restore instrument to original board configuration.

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4-21. YOKE ADJUSTMENT

Description:

This adjustment places the yoke on the CRT and adjusts the spot to the center of the CRT with the yoke adjustment rings.

NOTE

This adjustment should only be performed if the CRT has been replaced.

Equipment Recommended:

None

Procedure:

1. Loosen clamp that holds yoke on CRT neck.
2. Insure yoke is pushed firmly against CRT funnel.
3. Insure yoke is rotated in such a manner that raster is aligned with CRT face.

NOTE

The preceding step may have to be repeated after the raster has been set up.

4. Tighten clamp that holds yoke in place.

CAUTION

Do not over-tighten the clamp on the CRT neck or the CRT will break.

5. Set BRIGHTNESS adjustment fully counterclockwise.
6. Disconnect two connectors from CRT Driver Board that go to yoke.

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4-22. DRIVER BOARD ADJUSTMENTS

Description:

This procedure adjusts the raster size, CRT intensity, and CRT focus.

Equipment Recommended:

None

Procedure:

1. Apply power to instrument.
2. Adjust BRIGHTNESS until information on display visible.
3. Press ***More*** key, then press ***Utility*** key
4. Press ***CRT Setup*** key, then push ***CRT Pattern*** key. CRT adjustment pattern should be displayed on CRT.
5. Place CRT Calibration Template over CRT.
6. Adjust VERT PHASE and HEIGHT adjustments until CRT pattern aligns with template vertically.

NOTE

To gain access to the Height Adjustment, remove the left side cover. To remove the cover, remove the two rear feet on the left side cover, then remove the screw that holds the left side cover in place and slide the cover toward the rear of the instrument.

7. Adjust WIDTH and HOR LINEARITY until the pattern on the CRT aligns with the template horizontally. All vertical lines must be aligned when this adjustment is completed.

NOTE

If the display is "tilted" on the CRT with respect to the CRT Calibration Template Yoke Adjustment paragraph 4-21 must be repeated The horizontal position of the display may be changed with the centering rings on the yoke. If the centering rings are used care must be taken to minimize the vertical movement.

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8. Repeat steps 6 and 7 as necessary to obtain the best results.

9. Adjust HORIZONTAL HOLD (if necessary) by turning counter clockwise slowly until horizontal sync is lost, then turn clockwise slightly past point where horizontal sync is re-established.

10. Remove CRT Calibration Template from CRT face.

11. Press ***Exit CRT Menu*** key.

12. Press ***More*** key.

NOTE

At this time, the menu key labels "Timebse" and "SEC/DIV" should be displayed in Fullbright and everything else on the CRT in Halfbright.

13. Adjust BRIGHTNESS to set intensity of selected key labels (Timebse and SEC/DIV). This adjustment will increase or decrease intensity of entire display.

14. Adjust CONTRAST RATIO to set intensity of everything else on display. This adjustment affects only data written on CRT in Halfbright.

15. Press ***More*** key, then press ***Utility*** key, then press ***CRT Setup*** key, then press ***CRT Pattern*** key.

16. Adjust FOCUS control for best overall focus. Use the clusters of special characters in each corner and at CRT center for best overall focus.

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REPLACEABLE PARTS

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SECTION 5

REPLACEABLE PARTS

5-1. INTRODUCTION

This section contains information for ordering parts. Table 5-1 lists abbreviations used in the parts list, table 5-2 lists all replaceable parts in reference designator order.

5-2. ABBREVIATIONS

Table 5-1 lists abbreviations used in the parts list, the schematics, and throughout the manual. In some cases, two forms of the abbreviations are used, one all in capital letters, and one partially capitalized or without capitals. This occurs because the abbreviations in the parts list are always all capitals. However, in other parts of the manual other abbreviations are used with both lower and uppercase letters.

5-3. REPLACEABLE PARTS LIST

Table 5-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

The information given for each part consists of the following:

a. Complete reference designation.

b. Hewlett-Packard part number.

c. Total quantity (Qty) in instrument.

d. Description of part.

e. Check digit.

The total quantity for each part is only given once -- at the part number's first appearance in the list.

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5-4. EXCHANGE ASSEMBLIES

Some of the parts used in this instrument have been set up on an exchange program. This allows the customer to exchange a faulty assembly with one that has been repaired, calibrated and performance-verified by the factory The cost is significantly less than that of a new part

Exchangeable parts are listed in the replaceable parts table. They have a part number in the form XXXXX-695XX (where the new part would be a XXXXX-665XX part number).

After receiving the repaired exchange part from Hewlett-Packard, a US customer has 30 days to return the faulty assembly (contact the local HP repair organization for non-US orders). If the faulty assembly is not returned within the applicable time limit, the customer will be charged an additional amount, the difference in the price between a new and exchange assembly.

5-5. ORDERING INFORMATION

To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number, the check digit number, indicate the quantity required, and address the order to the nearest Hewlett-Packard office

To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument serial number, the description and function of the part, and number of parts required Address the order to the nearest Hewlett-Packard office.

5-6. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through local HP offices when orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices - to provide these advantages, check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local HP offices.

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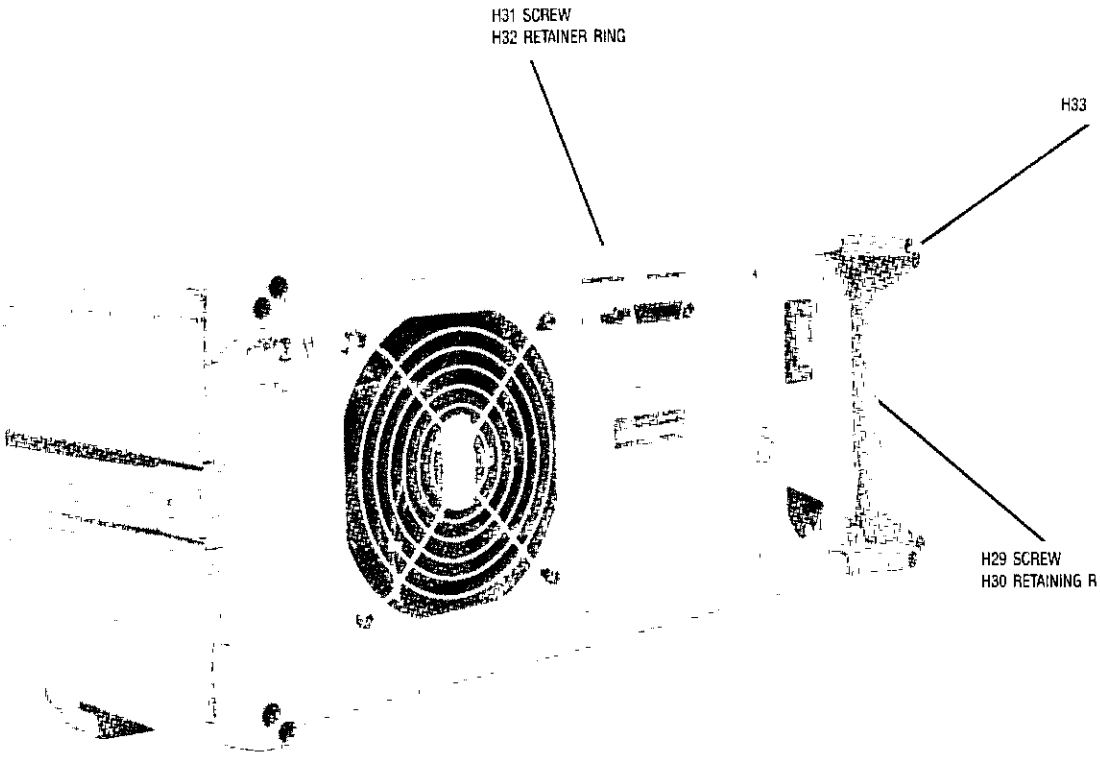


Figure 5-1. Cover Screws and Foot Screws.

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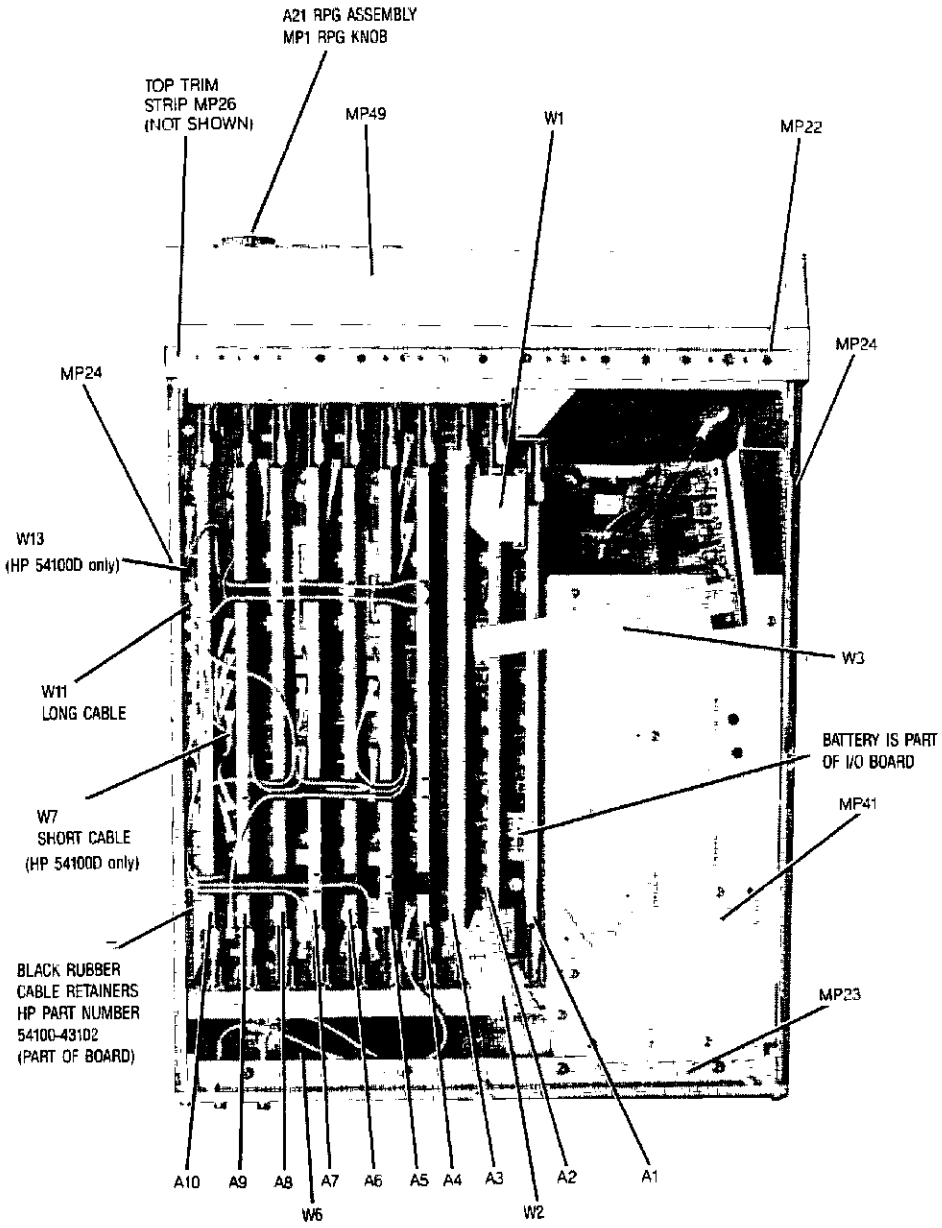


Figure 5-2. Main Printed Circuit Board Assemblies and Top Frame Parts

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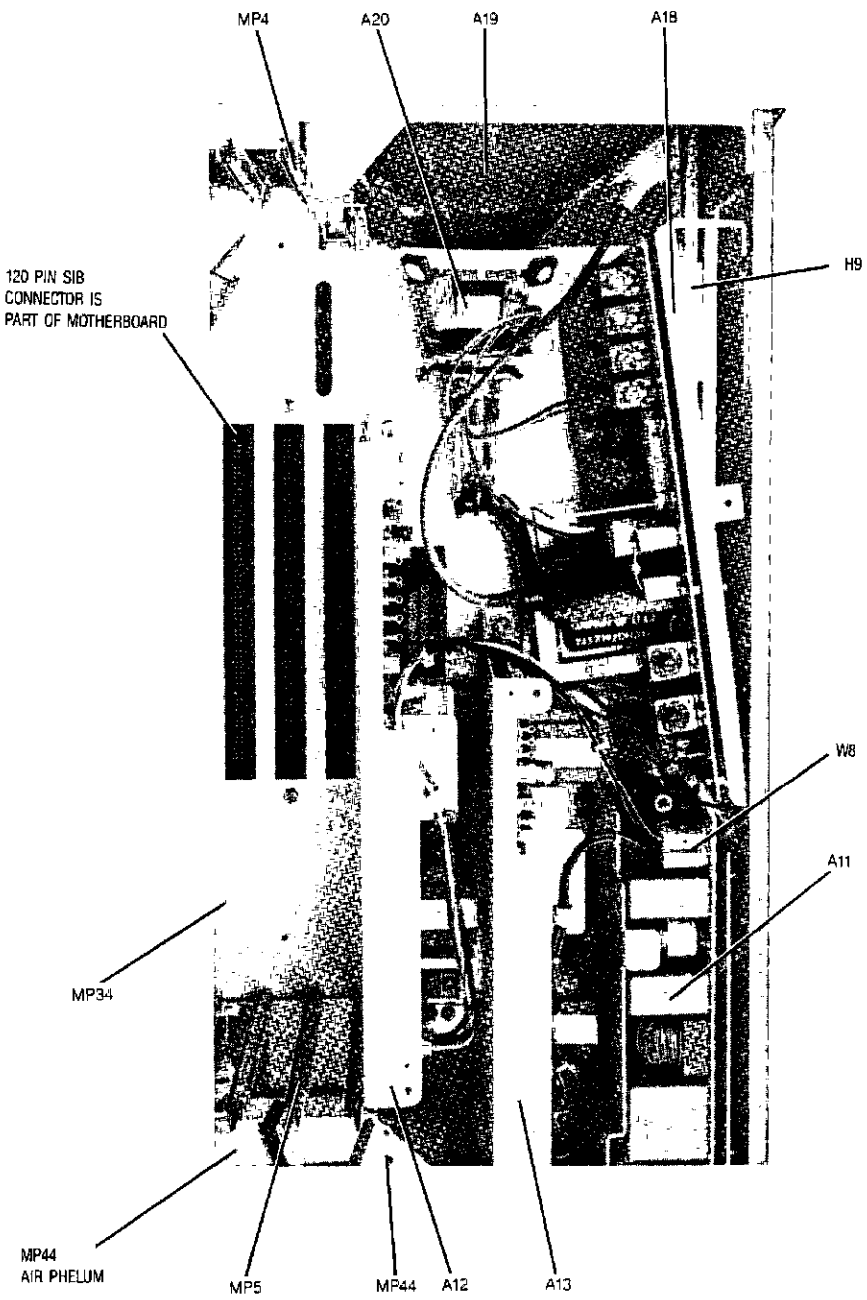


Figure 5-3. Power Supply Board Assemblies

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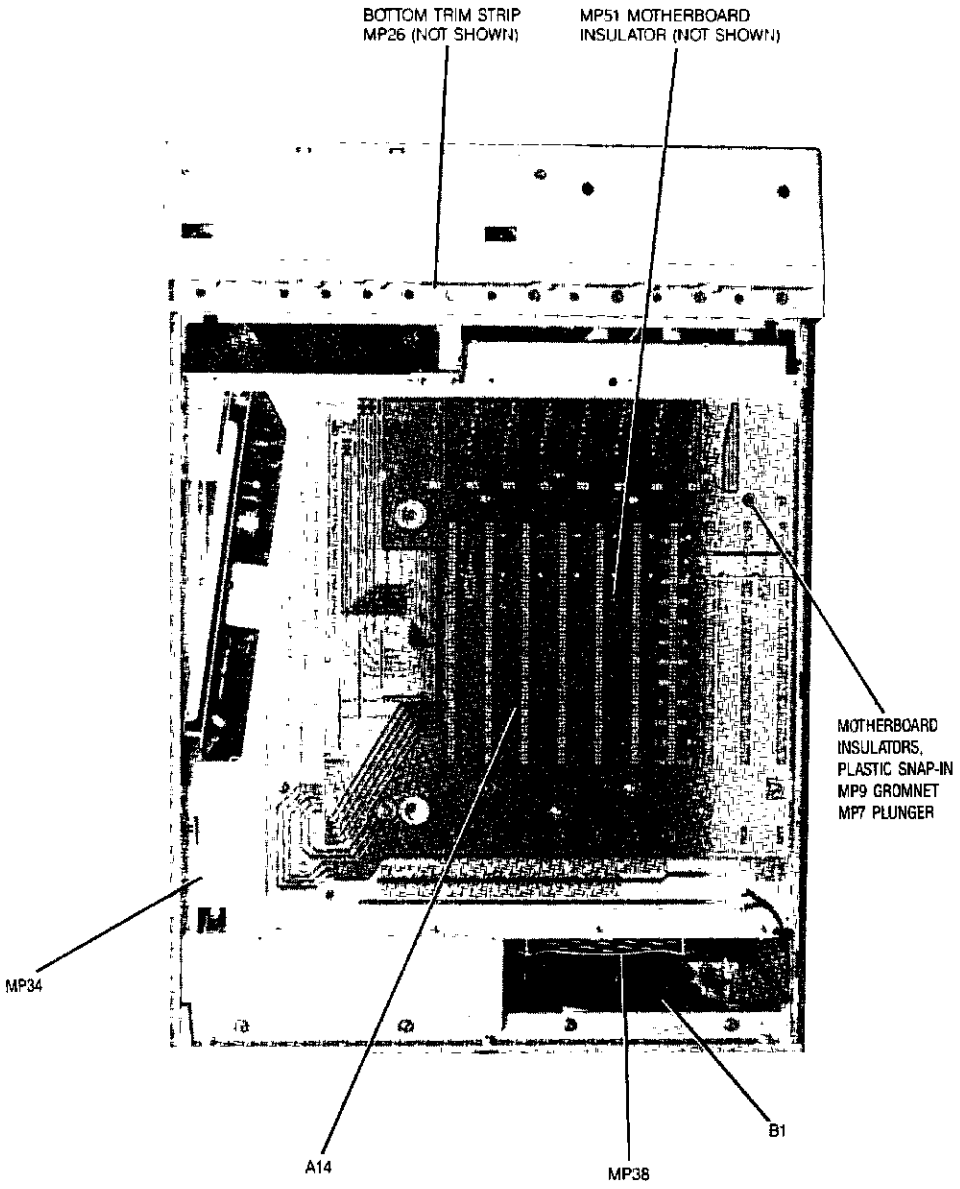


Figure 5-4. Motherboard Assembly, Air Deflection Assembly and Bottom Frame Parts

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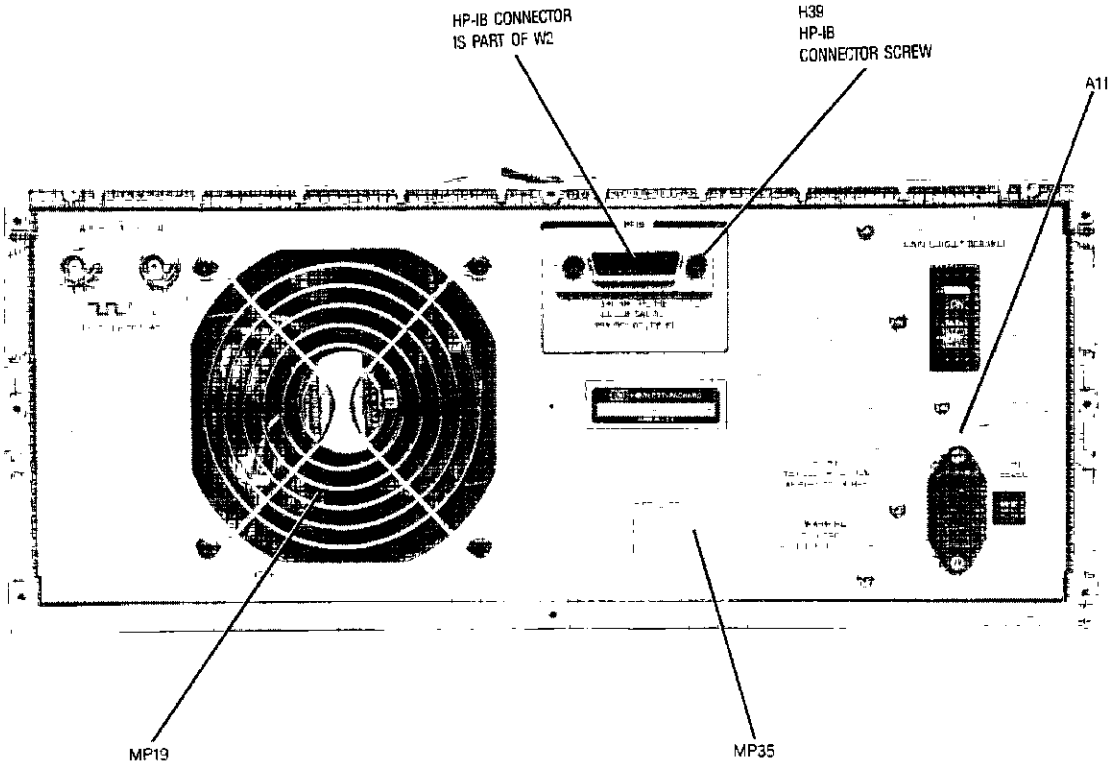


Figure 5-5. Rear Panel Assembly, Fan, and Fan Finger Guard

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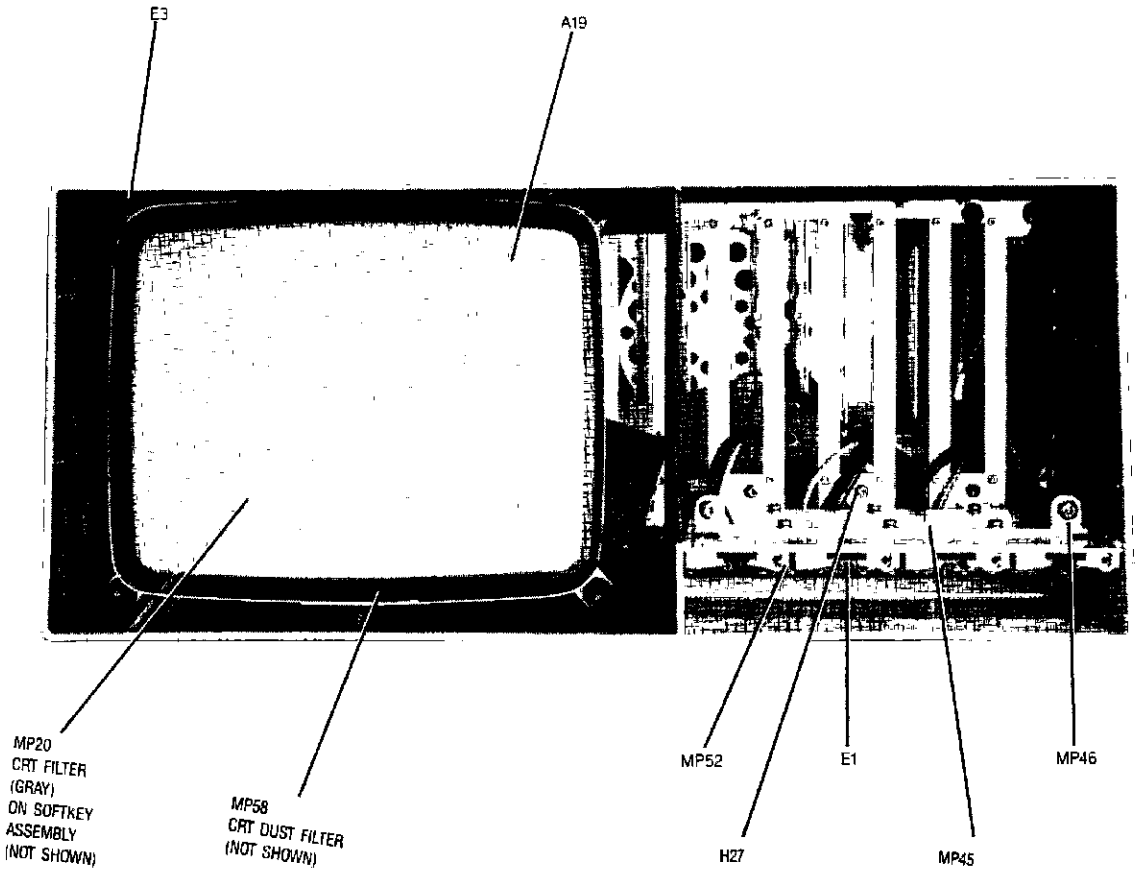


Figure 5-6. CRT, Probe Pod Connector Assembly, and Front Frame

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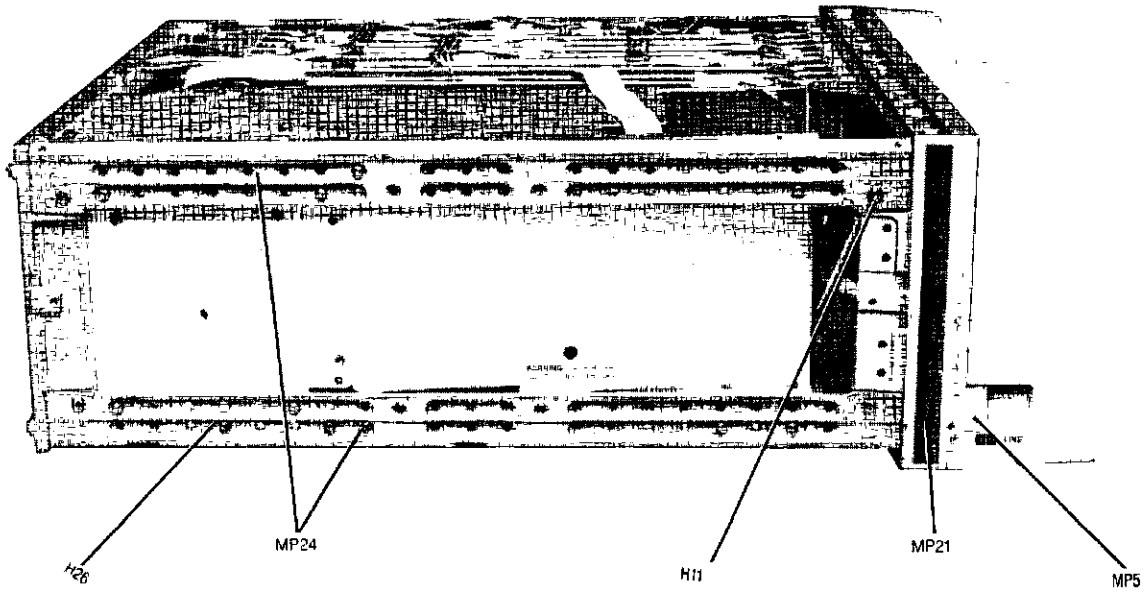


Figure 5-7. Side Frame Parts

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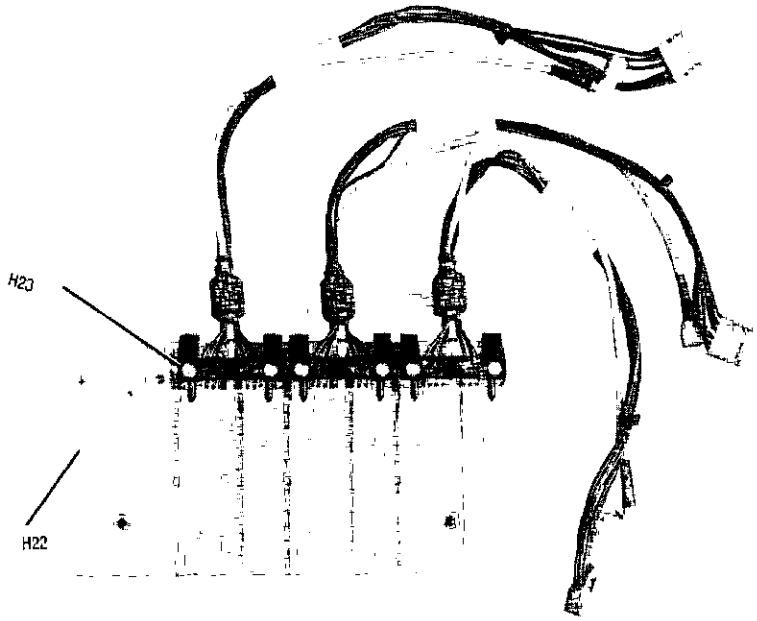


Figure 5-8. Probe Pod Guide Screws, Top View.

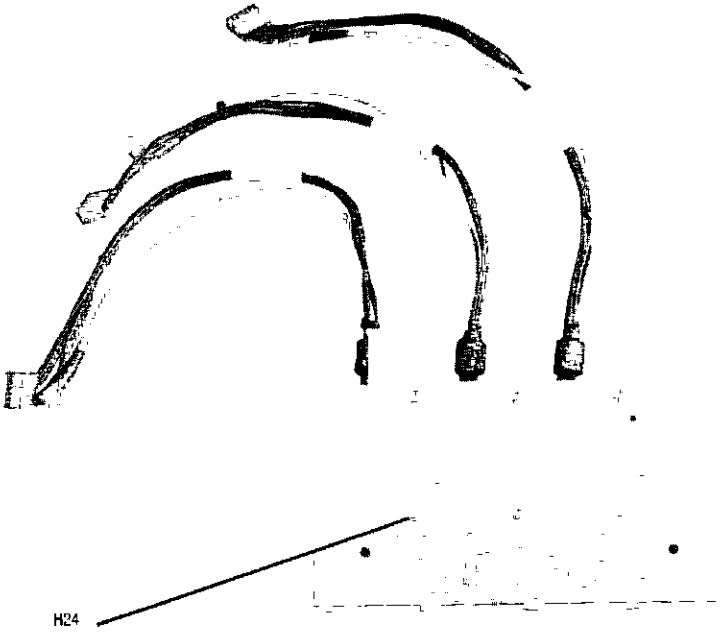


Figure 5-9. Probe Pod Guide Screws, Bottom View.

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Table 5-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	=assembly	F	=fuse	Q	=transistor,SCR; triode thyristor	U	=integrated circuit; microcircuit
B	=fan,motor	FL	=filter	R	=resistor	V	=electron tube; glow lamp
BT	=battery	H	=hardware	RT	=thermistor	VR	=voltage regulator, breakdown diode
C	=capacitor	J	=electrical connector (stationary portion),jack	S	=switch,jumper	W	=cable
CR	=diode,diode thyristor; varactor	L	=coil,inductor	T	=transformer	X	=socket
DL	=delay line	MP	=misc mechanical part	TB	=terminal board	Y	=crystal unit(piezo-electric or quartz)
DS	=annunciator,lamp,LED	P	=electrical connector (moveable portion),plug	TP	=test point		
E	=misc electrical part						

ABBREVIATIONS

A	=amperes	DWL	=dowel	MFR	=manufacturer	RND	=round
A/D	=analog-to-digital	ECL	=emitter coupled logic	MICPROC	=microprocessor	ROM	=read-only memory
AC	=alternating current	ELAS	=elastomeric	MINTR	=miniature	RPG	=rotary pulse generator
ADJ	=adjust(ment)	EXT	=external	MISC	=miscellaneous	RX	=receiver
AL	=aluminum	F	=farads;metal film (resistor)	MLD	=molded	S	=Schottky-clamped, seconds(time)
AMPL	=amplifier	FC	=carbon film/ composition	MM	=millimeter	SCR	=screw,silicon controlled rectifier
ANLG	=analog	FD	=feed	MO	=metal oxide	SEC	=second(time);secondary
ANSI	=American National Standards Institute	FEM	=female	MTG	=mounting	SEG	=segment
ASSY	=assembly	FF	=flip-flop	MTLC	=metallic	SEL	=selector
ASTIG	=astigmatism	FL	=flat	MUX	=multiplexer	SGL	=single
ASYNCHRO	=asynchronous	FM	=foam,from	MW	=milliwatt	SHF	=shift
ATTEN	=attenuator	FR	=front	N	=nano(10^{-9})	SI	=silicon
AWG	=American wire gauge	FT	=gain bandwidth product	NC	=no connection	SIP	=single in-line package
BAL	=balance	FW	=full wave	NMOS	=n-channel metal-oxide-semiconductor	SKT	=skirt
BCD	=binary-code decimal	FXD	=fixed	NPN	=negative-positive-negative	SL	=slide
BD	=board	GEN	=generator	NPRN	=neoprene	SLDR	=solder
BFR	=buffer	GND	=ground(ed)	NRFR	=not recommended for field replacement	SLT	=slotted)
BIN	=binary	GP	=general purpose	NSR	=not separately replaceable	SOLD	=solenoid
BRDG	=bridge	GRAT	=graticule	NUM	=numeric	SPCL	=special
BSHG	=bushing	GRV	=groove	OBD	=order by description	SQ	=square
BW	=bandwidth	H	=henries,high	OCTL	=octal	SREG	=shift register
C	=ceramic,cermet (resistor)	HD	=hardware	OD	=outside diameter	SRQ	=service request
CAL	=calibrate;calibration	HDND	=hardened	OP AMP	=operational amplifier	STAT	=static
CC	=carbon composition	HG	=mercury	OSC	=oscillator	STD	=standard
CCW	=counterclockwise	HGT	=height	P	=plastic	SYNCHRO	=synchronous
CER	=ceramic	HLCL	=helical	P/O	=part of	TA	=tantalum
CFM	=cubic feet/minute	HORIZ	=horizontal	PC	=printed circuit	TBAX	=tubeaxial
CH	=choke	HP	=Hewlett-Packard	PCB	=printed circuit board	TC	=temperature coefficient
CHAM	=chamfered	HP-IB	=Hewlett-Packard Interface Bus	PD	=power dissipation	TD	=time delay
CHAN	=channel	HR	=hour(s)	PF	=picofards	THD	=thread(ed)
CHAR	=character	HV	=high voltage	PI	=plug in	THK	=thick
CM	=centimeter	HZ	=Hertz	PL	=plate(d)	THRU	=through
CMOS	=complementary metal-oxide-semiconductor	I/O	=input/output	PLA	=programmable logic array	TP	=test point
CMR	=common mode rejection	IC	=integrated circuit	PLST	=plastic	TPG	=tapping
CNDCT	=conductor	ID	=inside diameter	PNP	=positive-negative-positive	TPL	=triple
CNTR	=counter	IN	=inch	POLYE	=polyester	TRANS	=transformer
CON	=connector	INCL	=include(s)	POS	=positive;position	TRIG	=trigger(ed)
CONT	=contact	INCAND	=incandescent	POT	=potentiometer	TRMR	=trimmer
CRT	=cathode-ray tube	INP	=input	POZI	=pozidrive	TRN	=turn(s)
CW	=clockwise	INTEN	=intensity	PP	=peak-to-peak	TTL	=transistor-transistor
D	=diameter	INTL	=internal	PPM	=parts per million	TX	=transmitter
D/A	=digital-to-analog	INV	=inverter	PRCN	=precision	U	=micro(10^{-6})
DAC	=digital-to-analog converter	JFET	=junction field-effect transistor	PREAMP	=preamplifier	UL	=Underwriters Laboratory
DARL	=darlington	JKT	=jacket	PRGMBL	=programmable	UNREG	=unregulated
DAT	=data	K	=kilo(10^{3})	PRL	=parallel	VA	=voltampere
DBL	=double	L	=low	PROG	=programmable	VAC	=volt,ac
DBM	=decibel referenced to 1mW	LB	=pound	PSTN	=position	VAR	=variable
DC	=direct current	LCH	=latch	PT	=point	VCO	=voltage-controlled oscillator
DCDR	=decoder	LCL	=local	PW	=potted wirewound	VDC	=volt,dc
DEG	=degree	LED	=light-emitting diode	PWR	=power	VERT	=vertical
DEMUX	=demultiplexer	LG	=long	R-S	=reset-set	VF	=voltage,filtered
DET	=detector	LI	=lithium	RAM	=random-access memory	VS	=versus
DIA	=diameter	LK	=lock	RECT	=rectifier	W	=watts
DIP	=dual in-line package	LKWR	=lockwasher	RET	=retainer	W/	=with
DIV	=division	LS	=low power Schottky	RF	=radio frequency	W/O	=without
DMA	=direct memory access	LV	=low voltage	RGLTR	=regulator	WW	=wirewound
DPDT	=double-pole, double-throw	M	=mega(10^{6});megohms; meter(distance)	RGTR	=register	XSTR	=transistor
DRC	=DAC refresh controller	MACH	=machine	RK	=rack	ZNR	=zener
DRVR	=driver	MAX	=maximum	RMS	=root-mean-square	°C	=degree Celsius (Centigrade)
						°F	=degree Fahrenheit
						°K	=degree Kelvin

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Table 5-2. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
A1	54100-66510	5	1	I/O ASSEMBLY	28480	54100-66510
A2	54100-66513	8	1	DISPLAY ASSEMBLY	28480	54100-66513
A3	54100-66523	0	1	MICROPROCESSOR ASSEMBLY	28480	54100-66523
A4	54100-66528	1	1	TIMEBASE ASSEMBLY	28480	54100-66528
A5	54100-66509	2	2	SAMPLER ASSEMBLY	28480	54100-66509
A6	54100-66507	0	2	ADC ASSEMBLY	28480	54100-66507
A7	54100-66509	2		SAMPLER ASSEMBLY	28480	54100-66509
A8	54100-66507	0		ADC ASSEMBLY	28480	54100-66507
A9	54100-66511	6	1	TRIGGER ASSEMBLY	28480	54100-66511
A10	54100-66514	9	1	TRIGGER QUALIFIER BOARD	28480	54100-66514
A11	54100-66501	4	1	PRIMARY ASSEMBLY	28480	54100-66501
A12	54100-66503	6	1	ANALOG SUPPLY	28480	54100-66503
A13	54100-66502	5	1	DIGITAL SUPPLY	28480	54100-66502
A14	54100-66504	7	1	MOTHERBOARD	28480	54100-66504
A15	54100-66505	8	1	CONTROL KEYBOARD	28480	54100-66505
A16	54100-66517	2	1	SOFT KEYBOARD	28480	54100-66517
A17	54100-66516	1	1	MENU KEYBOARD	28480	54100-66516
A18	0950-1692	3	1	DISPLAY DRIVER PCA 9 INCH DISPLAY SYSTEM	28480	0950-1692
A19	2090-0049	0	1	CATHODE RAY TUBE, 217 MM-SIZE; P-31 PHS	28480	2090-0049
A20	9140-0720	8	1	DEFLECTION YOKE FOR 20 MM NECK	28480	9140-0720
A21	01980-61062	5	1	RPG ASSEMBLY	28480	01980-61062
B1	3160-0521	3	1	FAN-TUBE AXIAL	28480	3160-0521
E1	54100-67602	8	1	PROBE POD CONNECTOR ASSEMBLY	28480	54100-67602
E2	8160-0551	4	1	RFI ROUND STRIP STL MSH/SIL RBR SN-PL	28480	8160-0551
E3	54100-61611	7	1	CRT GROUND CABLE	28480	54100-61611
E4	54110-25401	9	1	INSULATING BASKET	28480	54110-25401
H1	2190-0016	3	1	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
H2	2190-0068	5	1	WASHER-LK INTL T 1/2 IN .505-IN-ID	28480	2190-0068
H3	2950-0035	8	1	NUT-HEX-DBL-CHAM 15/32 32-THD	28480	2950-0035
H4	2950-0043	8	1	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN THK	28480	2950-0043
H5	3050-0002	2	1	WASHER-FL MTLC NO 10 .203-IN-ID	28480	3050-0002
H6	3050-0006	6	1	WASHER-SHLDR NO 10 .2-IN-ID .5-IN-OD	28480	3050-0006
H7	3050-1176	3	1	WASHER-FL NM 3/8 IN .39-IN-ID .562-IN-OD	86928	5810-323-125
H8	0624-0598	5	1	SCREW-TPG 8-16 .625-IN-LG PAN-HD-TORX	28480	0624-0598
H9	0515-0666	7	2	SCREW-MACHINE ASSEMBLY M3 X 0.5 18MM-LG	28480	0515-0666
H10	0515-0435	8	1	SCREW-MACHINE ASSEMBLY M4 X 0.7 14MM-LG	28480	0515-0435
H11	0515-1403	2	1	SCREW-SPCL M4 X 0.7 6MM-LG 90-DEG-FLH-HD	28480	0515-1403
H12	0515-0666	7		SCREW-MACHINE ASSEMBLY M3 X 0.5 18MM-LG	28480	0515-0666
H13	0515-0372	2	8	SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H14	0515-0372	2		SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H15	0515-0372	2		SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H16	0515-1269	8	4	SCREW-MACH M4 X 0.7 10MM-LG	28480	0515-1269
H17	0515-1269	8		SCREW-MACH M4 X 0.7 10MM-LG	28480	0515-1269
H18	0515-1269	8		SCREW-MACH M4 X 0.7 10MM-LG	28480	0515-1269
H19	0515-1269	8		SCREW-MACH M4 X 0.7 10MM-LG	28480	0515-1269
H20	0515-0372	2		SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H21	0515-0372	2		SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H22	0515-1103	9	1	SCREW-MACH M3 X 0.5 10MM-LG	28480	0515-1103
H23	0515-0446	1	1	SCREW-MACH M3 X 0.5 22MM-LG PAN-HD	28480	0515-0446
H24	0515-0372	2		SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H25	0515-0664	5	1	SCREW-MACHINE ASSEMBLY M3 X 0.5 12MM-LG	28480	0515-0664
H26	0515-0372	2		SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H27	0515-0372	2		SCREW-MACHINE ASSEMBLY M3 X 0.5 8MM-LG	28480	0515-0372
H28	0515-0383	5	1	SCREW-MACHINE ASSEMBLY M4 X 0.7 16MM-LG	28480	0515-0383
H29	0515-1245	0	2	SCREW FOR COVERS	28480	0515-1245
H30	0515-1253	0	2	RETAINER RING FOR COVER SCREWS	28480	0515-1253
H31	0515-1245	0		SCREW FOR COVERS	28480	0515-1245
H32	0515-1253	0		RETAINER RING FOR COVER SCREWS	28480	0515-1253
H33	0515-1402	1	1	SCREW-MACH M3.5 X 0.6 8MM-LG PAN-HD	28480	0515-1402
H34	5061-6138	2	4	FAN INSERT NUT	28480	5061-6138
H35	5061-6138	2		FAN INSERT NUT	28480	5061-6138
H36	5061-6138	2		FAN INSERT NUT	28480	5061-6138
H37	5061-6138	2		FAN INSERT NUT	28480	5061-6138
H38				NOT ASSIGNED		
H39	0380-1686	6	1	HEX STANDOFF	28480	0380-1686
H40	0515-1384	8	2	M5X0.8X10 TORX	28480	0515-1384
H41	0515-1384	8		M5X0.8X10 TORX	28480	0515-1384
MP1	01650-47401	7	1	RPG KNOB	28480	01650-47401
MP2	0400-0010	2	1	GROMMET-RND .25-IN-ID .375-IN-GRV-OD	28480	0400-0010
MP3				NOT ASSIGNED		
MP4	0403-0499	7	1	GUIDE-PC BD STEEL .032-IN-BD-THKNS	28480	0403-0499
MP5	0403-0500	1	1	GUIDE-PC BD STEEL .032-IN-BD-THKNS	28480	0403-0500
MP6	0905-0923	6	1	O-RING .176-IN-ID .07-IN-XSECT-DIA EPR	83259	2-008 E540-80
MP7	1390-0711	8	1	FASTENER-SNAP-IN PLGR PANEL THKNS 0.112	83014	HN3P-33-3-1
MP8				NOT ASSIGNED		
MP9	1390-0706	1	1	FASTENER-SNAP-IN GROM PANEL THKNS	83014	HN3G-31-2
MP10	1460-1345	5	1	TILT STAND SST	28480	1460-1345
MP11-18				NOT ASSIGNED		
MP19	3160-0092	3	1	FINGER GUARD	28480	3160-0092

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Table 5-2. Replaceable Parts (continued)

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
MP20	4330-1057	4	1	QUARTZ PLATE 5.56-IN-WD 7.71-IN LG	28480	4330-1057
MP21	5001-0440	1	1	SIDE TRIM	28480	5001-0440
MP22	5021-5805	4	1	FRONT FRAME	28480	5021-5805
MP23	5021-5806	5	1	REAR FRAME	28480	5021-5806
MP24	5021-5837	2	1	CORNER STRUT	28480	5021-5837
MP25	5040-7201	8	1	FEET	28480	5040-7201
MP26	5040-7202	9	1	TOP TRIM STRIP	28480	5040-7202
MP27	5041-6819	4	1	STRAP HANDLE CAP	28480	5041-6819
MP28	5041-6820	7	1	STRAP HANDLE CAP	28480	5041-6820
MP29	5040-7221	2	1	REAR PANEL STANDOFF	28480	5040-7221
MP30	5040-7222	3	1	NON SKID FOOT	28480	5040-7222
MP31	5060-9804	3	1	HANDLE STRAP	28480	5060-9804
MP32	5060-9884	9	1	RIGHT SIDE COVER	28480	5060-9884
MP33	5061-9517	7	1	LEFT SIDE COVER	28480	5061-9517
MP34	54100-00101	2	1	MAIN DECK	28480	54100-00101
MP35	54100-00204	6	1	REAR PANEL	28480	54100-00204
MP36	54100-00202	4	1	FRONT PANEL	28480	54100-00202
MP37	54100-00203	5	1	SUB PANEL	28480	54100-00203
MP38	54100-00605	1	1	AIR DEFLECTOR ASSEMBLY	28480	54100-00605
MP39	54100-01201	5	1	DISPLAY DRIVER BOARD BRACKET	28480	54100-01201
MP40	54100-01205	9	1	DECK SUPPORT GUSSET	28480	54100-01205
MP41	54100-04101	0	1	POWER SUPPLY COVER	28480	54100-04101
MP42	54100-04104	3	1	BOTTOM COVER	28480	54100-04104
MP43	54100-04105	4	1	TOP COVER	28480	54100-04105
MP44	54100-05201	3	1	AIR PLENUM	28480	54100-05201
MP45	54100-24101	2	1	PROBE HOUSING PLATE	28480	54100-24101
MP46				NOT ASSIGNED		
MP47	54100-25701	0	1	POD LOCK NUT	28480	54100-25701
MP48	54100-40201	7	1	DISPLAY PANEL	28480	54100-40201
MP49	54100-40501	0	1	FRAME PANEL	28480	54100-40501
MP50	54100-43701	8	1	LINE SWITCH SHAFT	28480	54100-43701
MP51	54100-44701	0	1	INSULATING SPACER	28480	54100-44701
MP52	54100-45201	7	1	PROBE GUIDE	28480	54100-45201
MP53	54100-94301	1	1	LINE LABEL	28480	54100-94301
MP54	54100-94305	5	1	LABEL ID-54100D	28480	54100-94305
MP55	54100-94308	8	1	LABEL CABLE INFO 54100D (ON TOP COVER)	28480	54100-94308
MP56	54100-94303	3	1	LABEL	28480	54100-94303
MP57				NOT ASSIGNED		
MP58	54100-42701	6	1	CRT DUST FILTER	28480	54100-42701
MP59	54100-43101	2	1	ENTENDER GUIDE	28480	54100-43101
MP60-61				NOT ASSIGNED		
MP62	54100-00613	1	1	RFI SHIELD	28480	54100-00613
MP63	54100-24702	9	1	PROBE HOUSING BRACKET	28480	54100-24702
W1	54100-61601	5	1	PANEL CABLE	28480	54100-61601
W2	54100-61602	6	1	HB-IB CABLE	28480	54100-61602
W3	54100-61603	7	1	DISPLAY CABLE	28480	54100-61603
W4-5				NOT ASSIGNED		
W6	54100-61610	6	1	CAL CABLE	28480	54100-61610
W7	54100-61614	0	1	SHORT RF CABLE	28480	54100-61614
W8-10				NOT ASSIGNED		
W11	54100-61604	8	2	RF CABLE	28480	54100-61604
W12	54100-61604	8		RF CABLE	28480	54100-61604
W13	54100-61613	9	1	OPT HOLDOFF CABLE	28480	54100-61613
				EXCHANGE ASSEMBLIES		
A2	54100-69513	4	1	DISPLAY ASSEMBLY	28480	54100-69513
A3	54100-69523	6	1	MICROPROCESSOR ASSEMBLY	28480	54100-69523
A4	54100-69528	7	1	TIMEBASE ASSEMBLY	28480	54100-69528
A5/7	54100-69509	8	1	SAMPLER ASSEMBLY	28480	54100-69509
A6/8	54100-69507	6	1	ADC ASSEMBLY	28480	54100-69507
A9	54100-69511	2	1	DISPLAY ASSEMBLY	28480	54100-69511
A10	54100-69514	5	1	TRIGGER QUALIFIER BOARD	28480	54100-69514
A12	54100-69503	2	1	ANALOG SUPPLY	28480	54100-69503
A13	54100169502	5	1	DIGITAL SUPPLY	28480	54100-69502

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DISASSEMBLY

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SECTION 6A

SERVICE

6A-1. INTRODUCTION

This section contains instrument disassembly, card cage PC assembly removal, and replacement procedures.

6A-2. SAFETY CONSIDERATIONS

The following warnings and cautions must be followed for your protection and to avoid damage to the equipment.

WARNING

Maintenance described in this section is performed with power supplied to the instrument and with protective covers removed. Maintenance should be performed only by trained service personnel who are aware of the hazards involved (for example, fire and electrical shock). Where maintenance can be performed without power applied, the power should be removed. Read the Safety Summary in the front of this manual.

CAUTION

Do not remove or replace any of the circuit board assemblies in the instrument unless instrument power is removed. The boards contain components which may be damaged if the board is removed or replaced when instrument power is applied.

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6A-3. CARD CAGE PC BOARDS

BOARD REMOVAL

1. Disconnect power cable.
2. Remove top cover.
3. Refer to illustration on underside of top panel for board locations and illustration on top of power supply shield for board extraction diagram.
4. Disconnect any cables to be removed from top of board.

NOTE

There are two types of RF cable connectors, push-on and screw-on. Do not try to pull off the screw-on type until the treaded sleeve is completely un-screwed.

5. Release PC board by pulling locks up.
6. Release board to be removed from connector by pulling up on board extractors.

BOARD REPLACEMENT

1. Make sure PC board locks are up before inserting board shield in guides.
2. Insert PC board shield edges in proper guides.
3. Make sure board extractors are down before attempting to seat connector.
4. While keeping board properly aligned in guides, push board downwards until connector is sealed. **To avoid connector pin damage, make sure connectors are properly aligned before applying insertion pressure.**
5. Lock board by pushing locks down.

CAUTION

The tabs on the bracket will be damaged by bending if they are not fully inserted into holes in top rail prior to rotating bracket down. If there is any resistance encountered while rotating the bracket down, the tabs are not fully inserted.

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6A-4. AC POWER SUPPLY PC BOARD (A11) AND DIGITAL POWER SUPPLY PC BOARD (A13)

RD REMOVAL

1. Disconnect power cable.
2. Remove top and left side covers.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Observe red LED on AC Power Supply board (A11) through top power shield. This LED indicates the presence of 300 volts and will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding to next step.
4. Remove top power supply shield by removing nine screws shown in figure 6A-1.
5. If removal of only Digital Power Supply (A13) board is required, skip steps 8 through 12 of this procedure.
6. Loosen screw that attaches Digital Power Supply (A13) to motherboard. Refer to figure 6A-2.
7. Lift Digital Power Supply (A13) out of chassis.
8. Remove four screws from power supply side cover as shown in figure 6A-3.
9. Remove two screws which attach power supply module to rear panel as shown in figure 6A-4.
10. Disconnect two cable connectors at top front corner of AC Power Supply (A11) board.
11. Lift AC Power Supply (A11) slightly. Pry off power switch extender with a small flat blade screwdriver. Refer to figure 6A-5.
13. Lift AC Power Supply (A11) out of chassis.

BOARD REPLACEMENT

1. Reverse removal procedure to install module.

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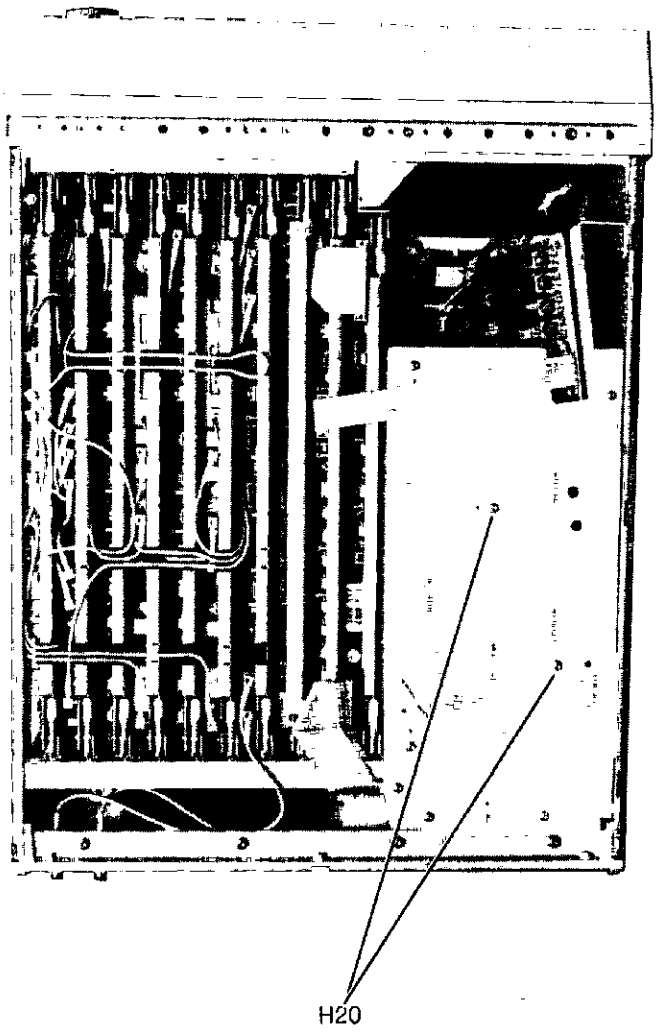


Figure 6A-1. Power Supply Shield Attaching Screws.

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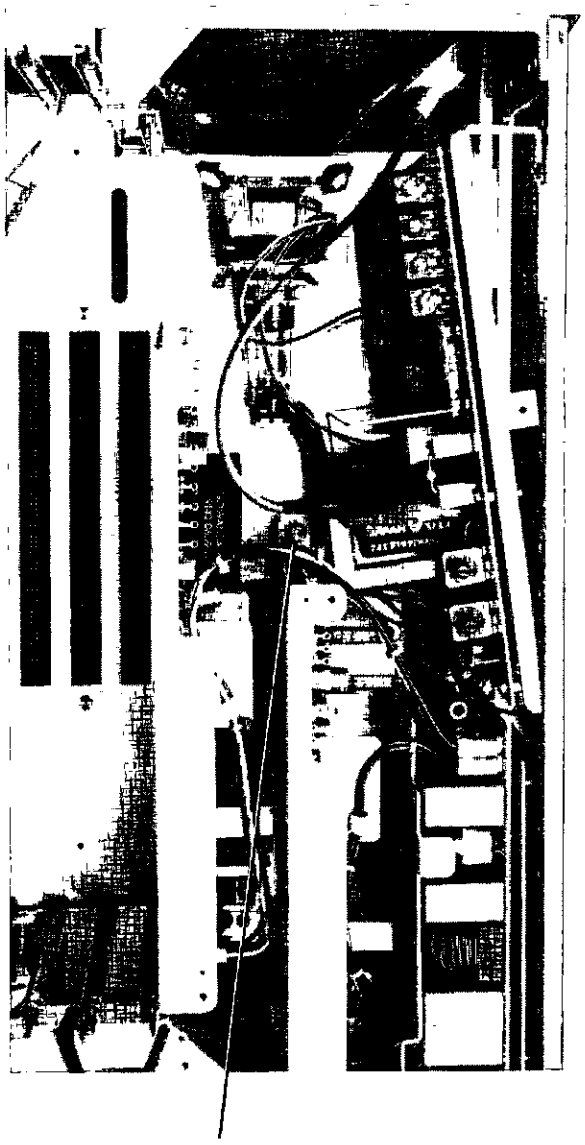


Figure 6A-2. Digital Power Supply Motherboard Retaining Screw.

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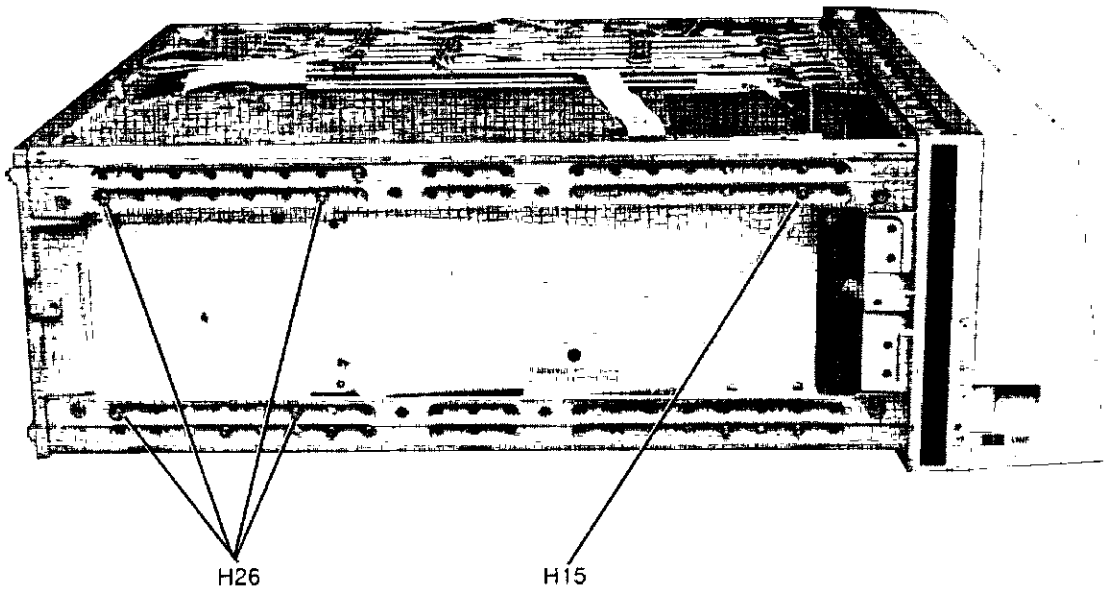


Figure 6A-3 AC Power Supply Side Attaching Screws.

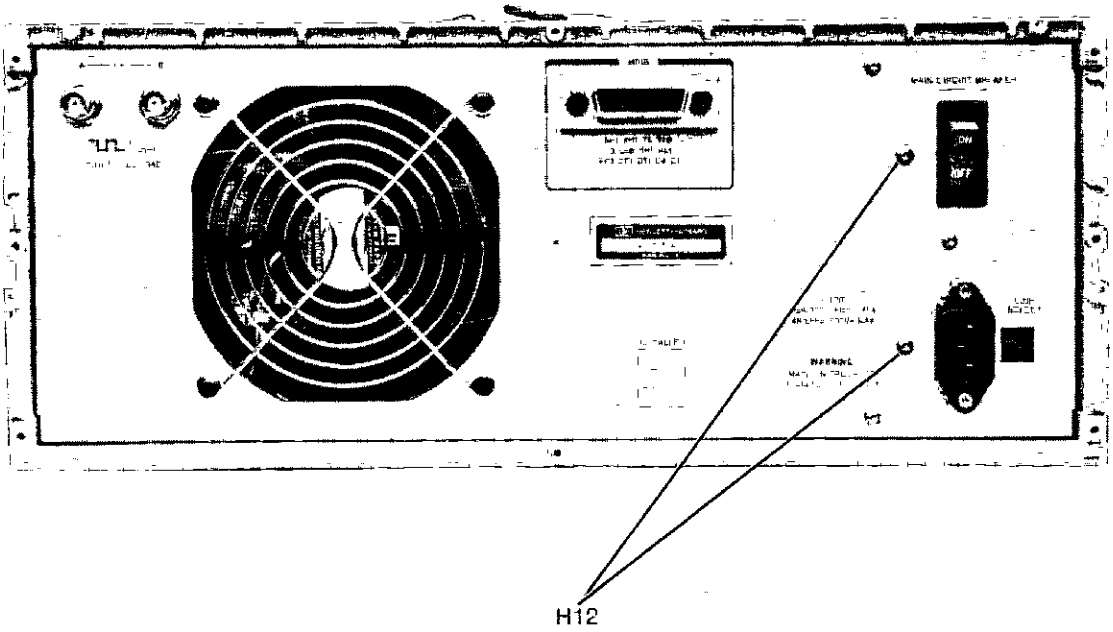


Figure 6A-4 Power Supply Rear Attaching Screws.

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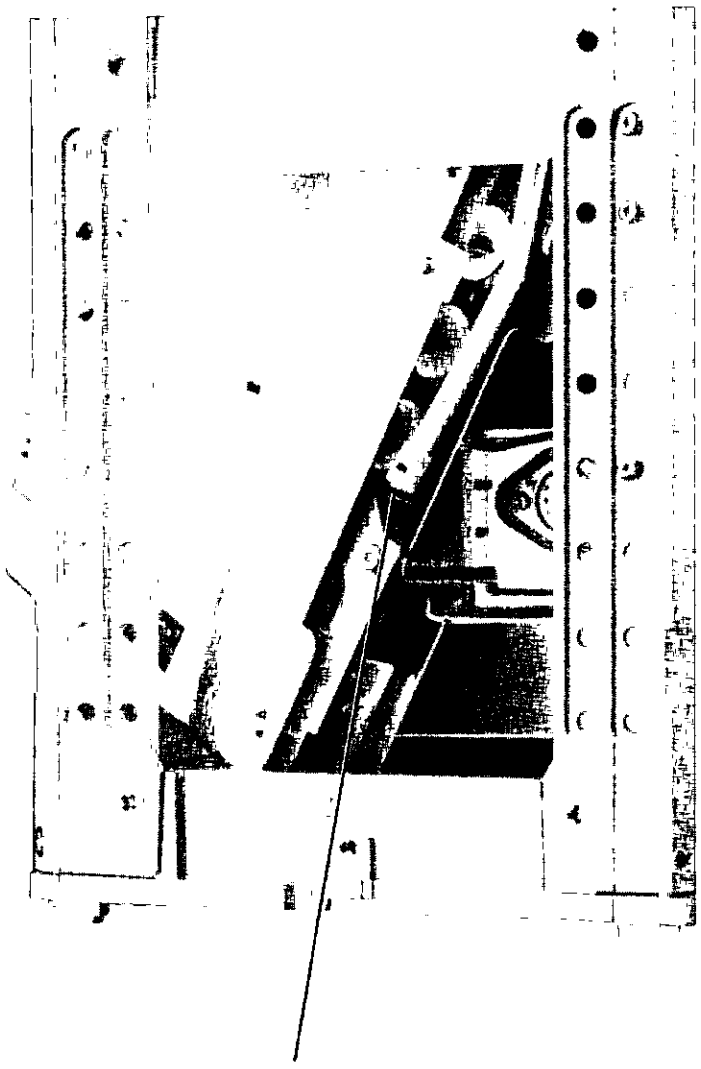


Figure 6A-5. AC Power Supply Switch Extender Removal.

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6A-5. ANALOG POWER SUPPLY PC BOARD (A12)

POWER SUPPLY BOARD REMOVAL

1. Disconnect power cable.
2. Remove top cover.

WARNING

Hazardous voltages capable of causing injury or death are present when the power supply shields are removed and AC power is applied to the instrument. To avoid this hazard make sure the AC power cable is disconnected before continuing with this procedure.

3. Observe red LED located on AC Power Supply board (A11) through top power shield. This LED indicates the presence of 300 volts and will stay illuminated until the filter capacitors discharge. Wait until this LED is no longer illuminated before proceeding to next step.
4. Disconnect Analog Power Supply (A12) board cable connector from back of Analog Power Supply (A12) board.
5. Loosen Analog Power Supply board retaining screw, near front bottom of board, as shown in figure 6A-6.
6. Disconnect cable running between Display (A2) board and Display Driver (A18) board.
7. Lift Analog Power Supply (A12) board from chassis.

BOARD REPLACEMENT

1. Reverse removal procedure to install board.

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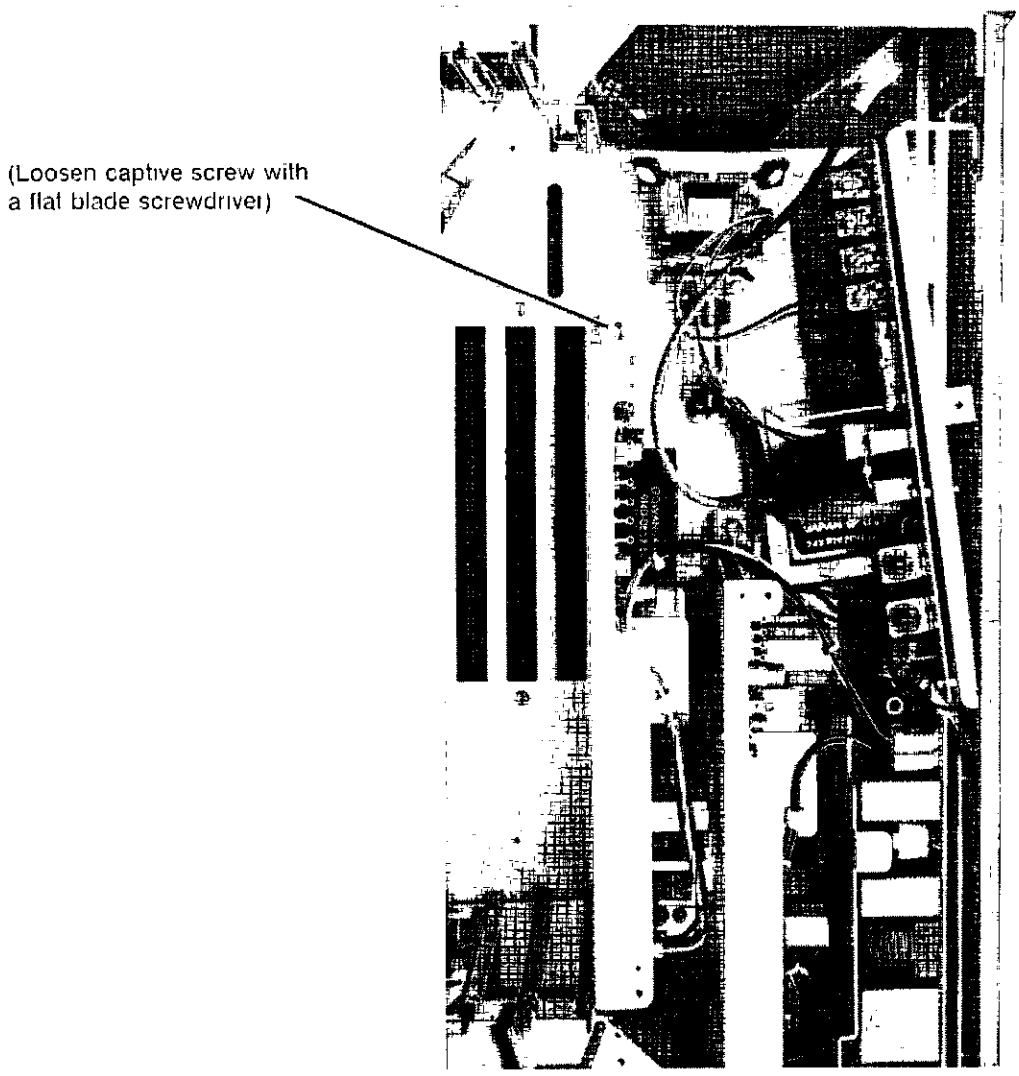


Figure 6A-6 Analog Power Supply Retaining Screw

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6A-6. CRT BEZEL AND SOFTKEY KEYBOARDS

BEZEL AND SOFTKEY KEYBOARDS REMOVAL

1. Disconnect power cable.
2. Remove 2 screws from bottom of chassis that mounts CRT Bezel. Refer to figure 6A-7.
3. Pull bottom of bezel from front panel. When bezel bottom is clear of front panel, move bezel down to allow tabs on bezel top to clear.
4. Remove two ribbon connectors from Keyboard assembly. Observe location of paint daub on connectors for proper reconnection.

NOTE

If the paint daub is not visible, the ribbon cables must be reconnected as follows: function keys cable (right side of bezel) to top connector on Front Panel Control board and menu keys cable (bottom of bezel) to bottom connector on Front Panel Control board.

5. Remove either softkey keyboards by removing two screws (H21) and lifting keyboard from CRT Bezel.

BEZEL REPLACEMENT

1. Reverse removal procedure to install bezel.

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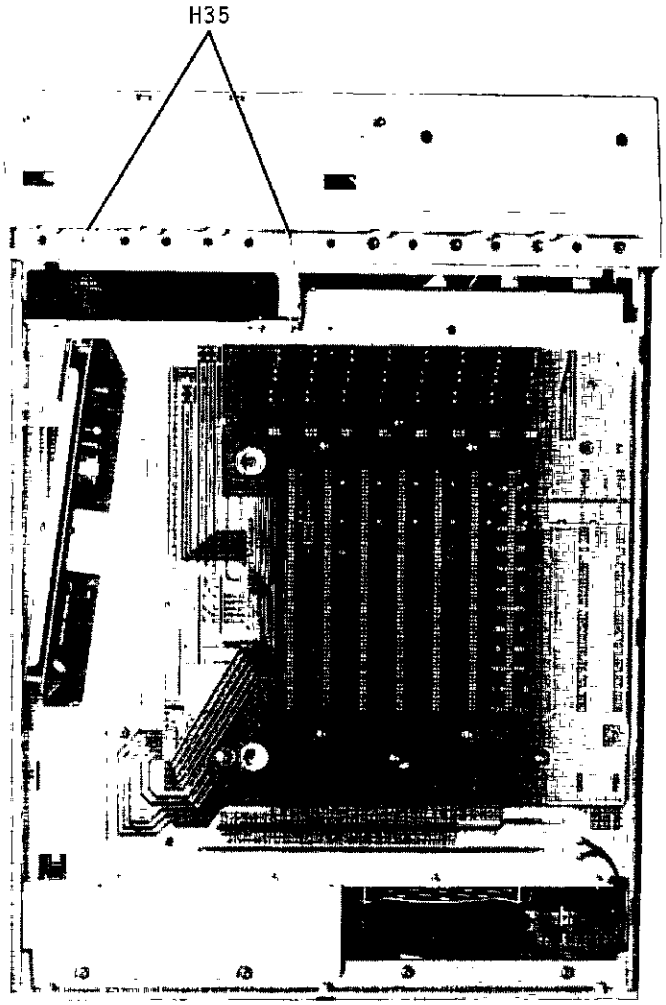


Figure 6A-7. CRT Bezel and Softkey Keyboard Removal.

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6A-7. SYSTEM CONTROL PANEL, SYSTEM CONTROL BOARD (A15), AND RPG ASSEMBLY (A21)

SYSTEM CONTROL PANEL REMOVAL

1. Disconnect power cable.
2. Remove top trim strip by carefully prying up at ends with a small flat blade screwdriver.
3. Remove all probe pods.
4. Remove two screws from bottom of (H37) instrument. These screws are removed through holes provided in bottom of instrument. Refer to figure 6A-8.
5. Remove two screws from top of instrument (H16 - under trim strip). Refer to figure 6A-9.
6. Move front panel and Control board forward just far enough to disconnect one large and two small ribbon cables from Control board. Board is held in place with 5 screws (H25).

NOTE

If the paint daub is not visible, the ribbon cables must be reconnected as follows: function keys cable (right side of bezel) to top connector on Front Panel Control board and menu keys cable (bottom of bezel) to bottom connector on Front Panel Control board.

SYSTEM CONTROL BOARD (A15) REMOVAL

7. Disconnect RPG connector from Front Panel Control board.
8. Remove five screws mounting the Front Panel Control board to Front Panel (H25).
9. Lift Front Panel Control board from Front Panel.

RPG ASSEMBLY (A21)

NOTE

The Front Panel Control board does not need to be removed to remove the PRG Assembly.

10. Disconnect RPG connector from Front Panel Control board.
11. Using an allen wrench, remove knob from RPG shaft by loosening set screws
12. Remove hex nut and washer (H1) from RPG shaft and pull RPG towards rear of Front Panel. The hex nut is 3/8 x 32, HP Part 2150-0043.

SYSTEM CONTROL PANEL, SYSTEM CONTROL BOARD (A15), AND RPG ASSEMBLY (A21) REPLACEMENT

1. Reverse procedure to replace any of these assemblies.

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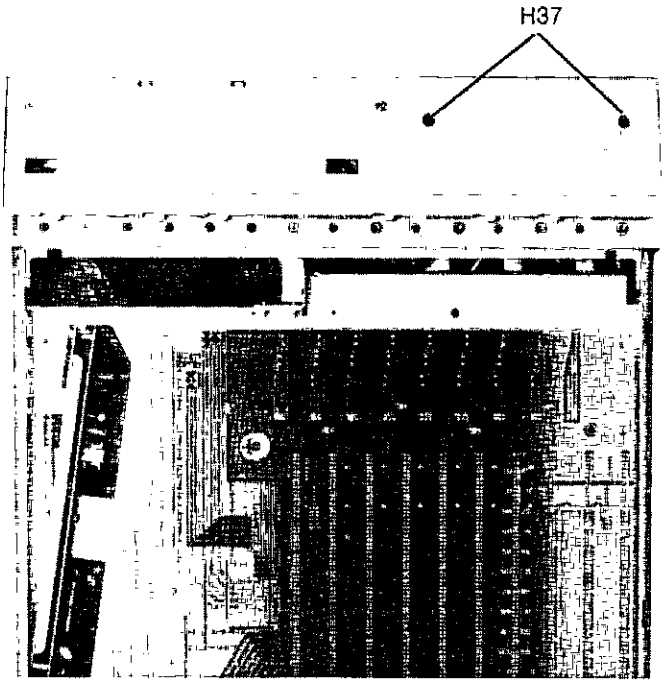


Figure 6A-8. Bottom Front Panel Attaching Screws

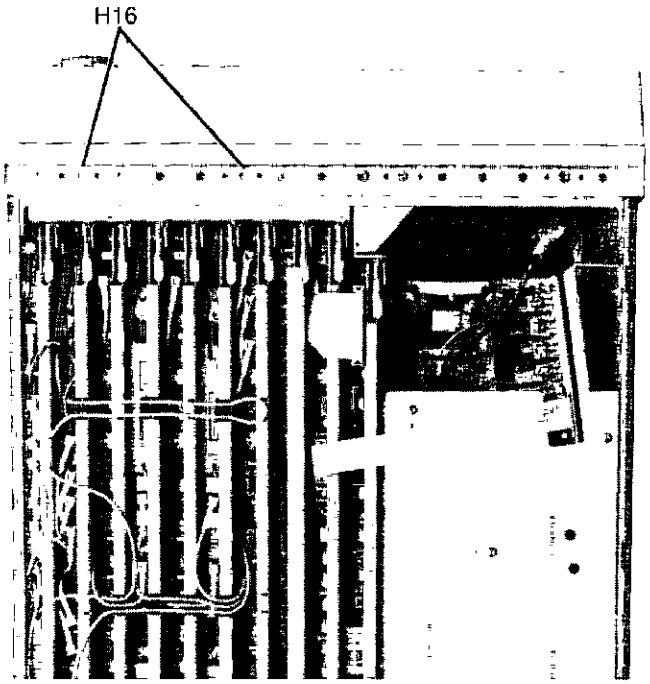


Figure 6A-9. Top System Control Panel Attaching Screws.

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6A-8. DISPLAY DRIVER BOARD

BOARD REMOVAL

1. Disconnect power cable.
2. Remove top cover, bottom cover, and perforated side panel.
3. Remove top power supply shield by removing nine screws shown in figure 6A-1.
4. Remove three torx screws shown in figure 6A-10.
5. Disconnect two connectors at Display Driver board, containing two wires each from CRT.
6. Disconnect CRT neck pin connector.

WARNING

High voltage is present at the red PA lead. Short this connector to the chassis ground before attempting to dismantle any part of the display system.

7. Disconnect red PA lead.
8. Slide Display Driver board toward back of instrument until it is free. Remove board from chassis through top.

BOARD REPLACEMENT

1. Reverse removal procedure to install board.

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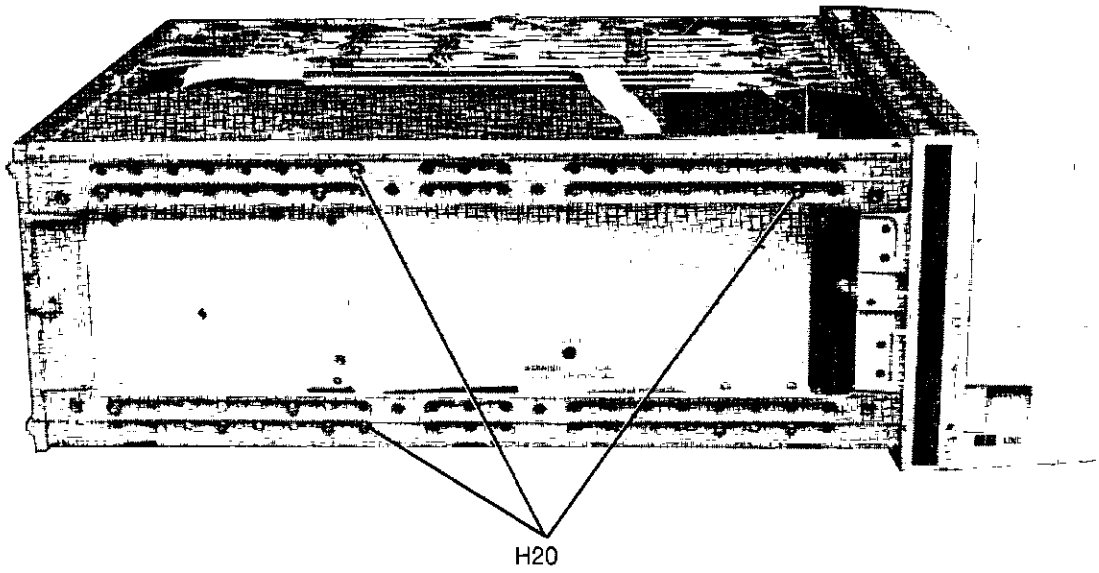


Figure 6A-10. Display Driver Board Attaching Screws.

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6A-9. CRT (A19) REMOVAL

CRT REMOVAL

1. Disconnect power cable.
2. Remove top cover.
3. Remove CRT Bezel and Softkey key boards. Refer to paragraph 6A-6.
4. Disconnect 2 connectors from Display Driver (A18) board. Each of these connectors contain two wires from CRT.
5. Disconnect CRT neck pins connector.

WARNING

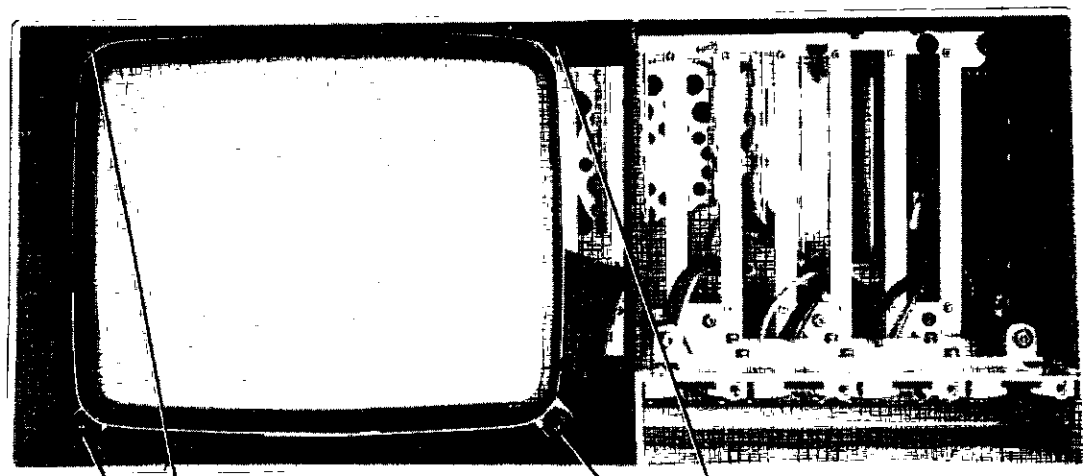
High voltage is present at the red PA lead. Short this connector to the chassis ground before attempting to dismantle any part of the display system.

6. Remove red PA lead from CRT.
7. Remove 4 torx screws and washers attaching CRT to chassis. Note should be taken of ground lead connected to upper left hand corner screw of CRT. Refer to figure 6A-11.
8. Remove CRT through front of chassis.

CRT REPLACEMENT

1. Reverse removal procedure to replace CRT.

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H8
with flat washer H5
with ground wire E3

H8
with shoulder washer H6.

Figure 6A-11. CRT Mounting.

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6A-10. POD CONNECTORS

POD CONNECTOR REMOVAL

1. Disconnect power cable.
2. Remove pods.
3. Disconnect all pod cable connectors from PC boards.

NOTE

There are two types of RF cable connectors, push-on and screw-on. Do not try to pull off the screw-on type until the treaded sleeve is completely un-screwed.

4. Remove top trim strip by carefully prying up at the ends with a small flat blade screwdriver.
5. Remove two screws from bottom of instrument. These screws are removed through the holes provided on bottom of instrument. Refer to figure 6A-8
6. Remove two screws from top of instrument (under the trim strip). Refer to figure 6A-9.
7. Move front panel and Control Board forward just far enough to disconnect one large and two small ribbon cables from Control Board.

NOTE

If the paint daub is not visible, the ribbon cables must be reconnected as follows: function keys cable (right side of Bezel) to top connector on Front Panel Control board and menu keys cable (bottom of bezel) to bottom connector on Front Panel Control board.

8. Remove 5 torx screws in figure 6A-12.
9. Remove Pod Connector Assembly by sliding out through front of chassis.

POD CONNECTOR REPLACEMENT

1. Reverse removal procedure to install pod connectors.

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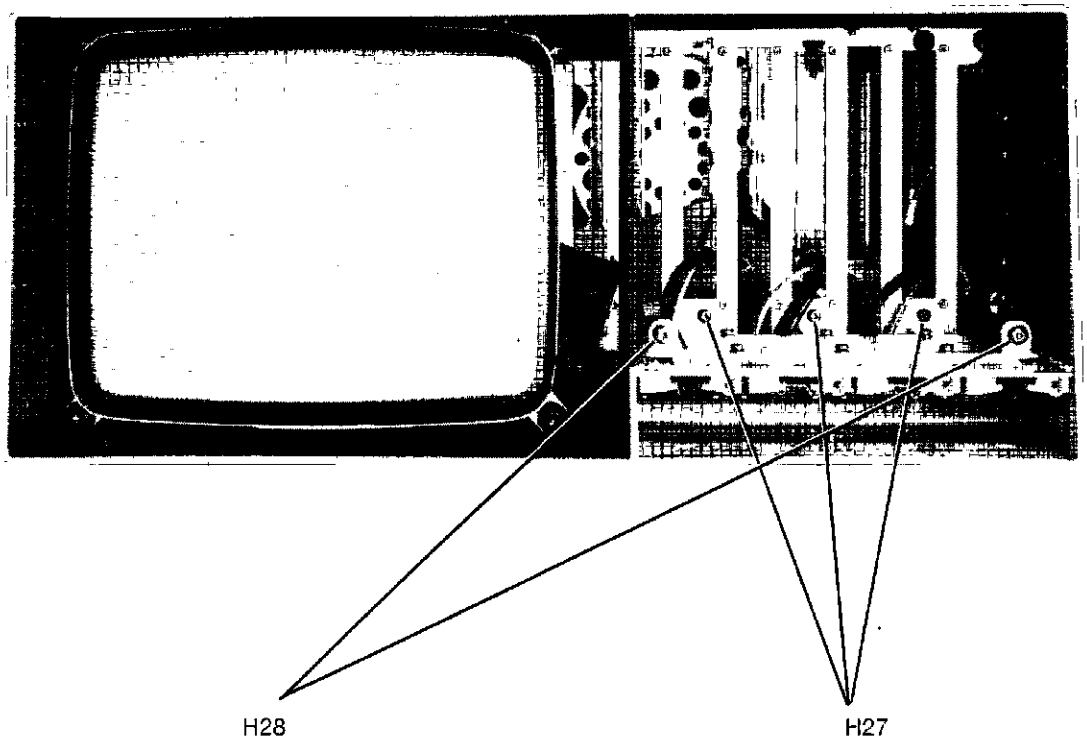


Figure 6A-12. Pod Connector Attaching Screws.

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6A-11. MOTHERBOARD (A14)

BOARD REMOVAL

1. Disconnect power cable.
2. Remove top and bottom covers.
3. Remove all card cage PC boards (refer to paragraph 6A-3).
4. Remove Digital Power Supply (A13) and Analog Power Supply (A12) (refer to paragraphs 6A-4 and 6A-5 respectively).
5. Disconnect fan power cable connector from bottom of motherboard.
7. Remove insulator on bottom of motherboard by pulling on four snap connectors.
8. Remove 12 Motherboard attaching screws and remove board from bottom of chassis (see figure 6A-13).

BOARD REPLACEMENT

1. Reverse removal procedure to install board.

NOTE

To reinstall the Snap Connectors pull the center pin toward the top of the connector before trying to place in the Motherboard.

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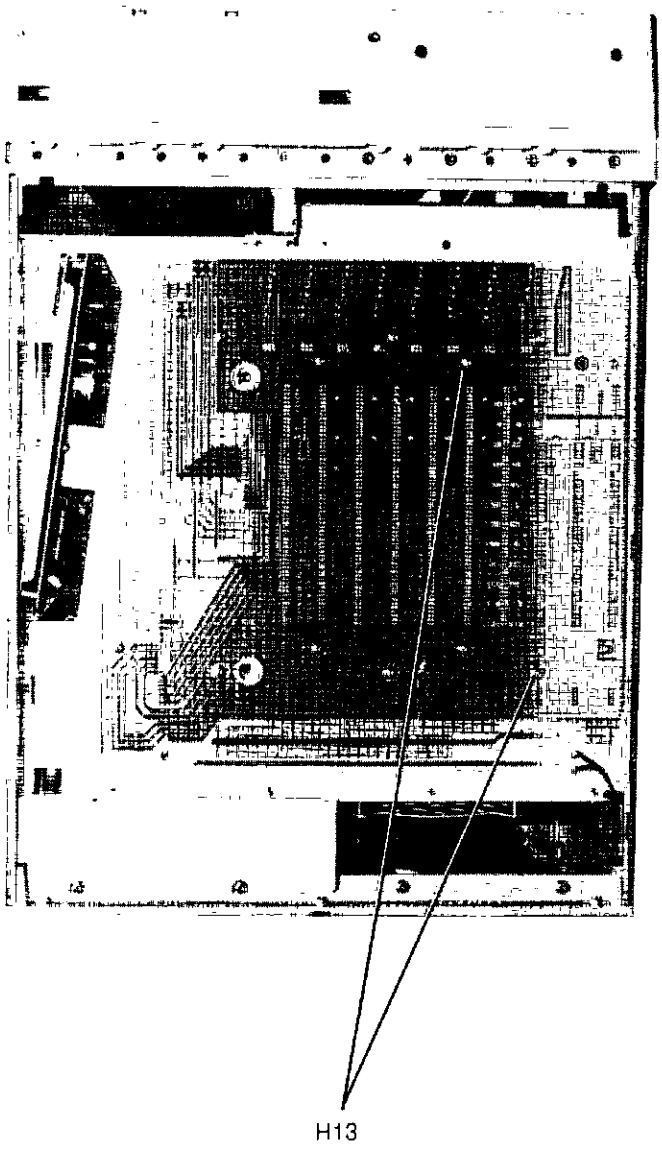


Figure 6A-13. Motherboard Attaching Screws

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6A-12. FAN (B1)

FAN REMOVAL

1. Disconnect power cable.
2. Remove bottom cover.
3. Disconnect fan power cable from bottom of Motherboard.
4. Remove four Fan Finger Guard attaching screws as shown in figure 6A-14.
5. Remove four screws holding Air Deflection Assembly to card cage. The fan will be loose and can be moved to get at these screws.
6. Remove Air Deflection Assembly through bottom of unit.
7. Remove fan through bottom of unit.

FAN REPLACEMENT

1. Reverse removal procedure to install fan.

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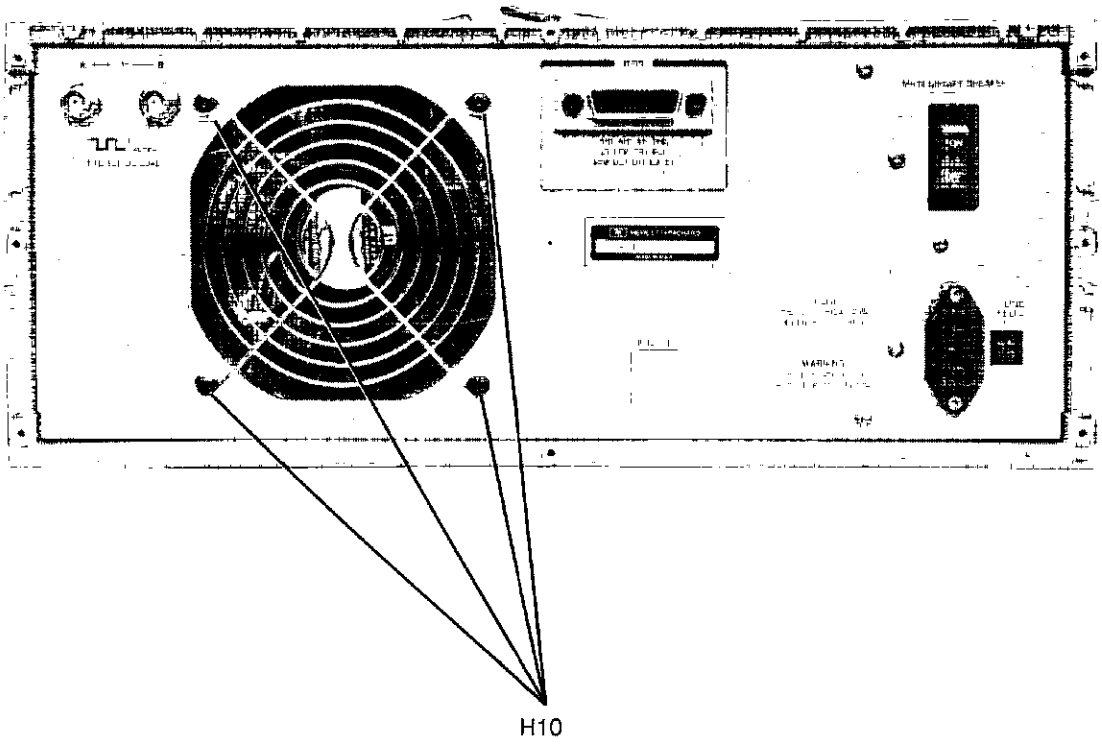


Figure 6A-14. Fan Attaching Screws.

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SECTION 6B

THEORY

6B-1. INTRODUCTION

The theory of operation is presented in a block diagram theory format. There are four parts to the theory of operation. The first part covers the entire instrument block diagram. The second part traces a signal from the channel one input probe to the display. The third part is a description of a typical data acquisition theory. The fourth part has block level theory of operation accompanying a block diagram of each assembly. This theory gives only an overview of instrument operation to aid in troubleshooting a problem to a board level.

6B-2. SYSTEM THEORY

The difference between an HP 54100A and an HP 54100D is that the HP 54100D contains a Trigger Qualifier Board in the A10 slot. The addition of this board requires some additional cabling, and some cabling is changed. This theory of operation will cover the common parts of the HP 54100A/D first and talk about the addition of the Trigger Qualifier at the end of the theory. Refer to the HP 54100A/D Overall Block Diagram, figure 6B-2 for this discussion.

As can be seen from the block diagram, the HP 54100A/D can be split into two parts; The Mainframe section and the Data Acquisition section. In theory the Data Acquisition section could contain a completely different set of boards and still work with the mainframe. Each of the ten boards (A1 through A10) plug into the Motherboard (A14). The ten Motherboard connectors each have a hard wired identification code (0 through 9). Each of the plug in boards have a built in identification code. Therefore, any board can be placed in any motherboard connector and the CPU can read the connector identification and board identification and know what type of board is in each slot. This information can be displayed on the HP 54100 CRT by selecting the ***Utility*** menu, the ***Test*** menu, then ***Display Configuration***.

Note that the microprocessor's position is displayed as an empty slot. The board configuration shown on the block diagram, figure 6B-2, has shown to be the most efficient for System Interface Bus operation, therefore the boards should generally be left in this configuration during operation.

6B-3. MAINFRAME THEORY

The HP 54100A/D Mainframe will be discussed prior to the Data Acquisition section. The mainframe contains power supplies for the entire instrument, Front Panel keys, Softkeys and HP-IB with Input/Output Board as an interface, CRT and display circuits with the Display Board as an interface; and last, but not least, is the Microprocessor Board.

Power Supplies

There are three power supply boards within the HP 54100 mainframe system. The AC Power Supply (A11) gets its input from the Line Power on the rear panel. The rear panel contains an EMI circuit and main circuit breaker. The Bulk Power Supply Board contains the power switch (from side of instrument), and some voltage regulation to output 300 volts for using the Analog Supply and Digital Supply boards. The Analog Supply board uses the 300 volt input to supply + and - 15 volts and + and - 8 volts to be used by the analog circuits. The Digital Supply board uses the 300 volts to supply + and - 5 volts for using the digital circuits within the instrument. Both of these power supplies have their own ground system and they are isolated from each other, therefore, voltage measurements must be made to the proper common point.

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Front Panel Interface

The front panel contains System Control keys, Softkeys, a keypad, and a knob. All of these devices are contained on or wired through the Front Panel board (A15). The Front Panel board also contains the Line-ON indicator Lamp. All information from the Front Panel board is input to the I/O board through a large ribbon cable connected near the front of the I/O board. The keypad and Softkeys are setup in a matrix so that the I/O board can scan the lines of keys by outputting a pulse on each line, and if a key is closed (pressed) the I/O board will detect the return of the pulse on a line. By knowing which line the pulse was output on and which line the pulse was returned on, the I/O board can determine which key was pressed. These key scan lines are also contained in the large ribbon cable.

Display System

The CRT Drive board receives its inputs from the Display board. It receives horizontal and vertical sync pulses, character and signal data, and power from the Display board. These signals and voltages are connected to the CRT Drive board through a ribbon cable from the top of the Display board. The CRT drive board creates the sweep signals, blanking, and voltages required to produce the raster scan and to display information on the CRT.

HP-IB System

The HP-IB connector on the rear panel of the instrument is connected by a ribbon cable to the rear top of the I/O board. The I/O board contains an HP-IB interface-integrated circuit to convert data to proper HP-IB format.

System Interface Bus

All digital data is moved between major boards within the HP 54100 system on the System Interface Bus (SIB). The System Interface Bus contains data lines, address lines, and control lines The SIB data, address, and control signals are under the control of the CPU. Many of the boards contain a local data bus, which is under the control of the board that contains it. The SIB and the local data buses must not be confused. In most cases data and address are accepted by a board from the SIB under CPU control, then the data is manipulated within that board on a local data bus.

Microprocessor Board (A3)

The Microprocessor (CPU) board contains a 68000 CPU, 192k bytes of ROM, 32k bytes of non-volatile RAM (battery powered), a programmable timer, and a bus arbitration circuit. This board has an internal data bus, so that it can process data without tying up the System Interface Bus. Normally data is moved on the SIB under control of the 68000 CPU. This board also contains logic circuits to allow it to operate with another CPU on the SIB, in which case the bus request/bus grant circuits would be used. In the HP 54100A/D only one CPU is used, therefore the bus request/bus grant signals are tied to the proper logic levels to insure the 68000 CPU will have control of the SIB when required.

Display Board (A2)

The Display board contains 128k bytes of dynamic RAM (DRAM) used as the bit mapped memory to store signal data to be displayed. It also contains a character generator and character refresh circuits for the characters to be displayed. This board produces vertical and horizontal sync signals to insure that signal data and characters are displayed on the CRT at the proper place and time.

I/O Board (A1)

The I/O board contains the interface circuits to read the front panel devices, including Softkeys, knob (RPG), System Control keys, and keypad keys. This board also contains the HP-IB interface logic, a clock circuit to produce the clocks required for CPU operation, a power-on reset circuit to reset the CPU and other logic to a start-up condition, and the battery power supply for the non volatile RAM.

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Table 6B-1. SIB Pin Description

The SIB is grouped into smaller buses that makes it easier to comprehend. These buses include the following:

Analog Power	12 pins
Analog 50 Ω bus	3 pins
Digital 50 Ω bus	5 pins
Digital Power	21 pins
CPU Control Bus	15 pins
CPU Address Bus	22 pins
CPU Data Bus	16 pins
Interrupts	10 pins
Misc.	4 pins
Not Used	12 pins

The following sections briefly discuss the operation of each of the SIB lines according to the bus group.

Analog Bus

Pins 1,2	+18 V Analog power supply
pins 3,4	-18 V Analog Power supply
Pins 5,6	+8 V
Pins 7,8	-8 V
Pins 9,11,13,15	AGND

The card cage PC boards, which use each of the above supplies, has their own regulation for the supply. AGND is connected very securely to the chasis by the motherboard standoffs. AGND and DGND are connected to each other in only one place, this is on the motherboard between the two supplies.

Analog 50 Ω Bus

Pin 10	MASCLK	40.849673 MHz 50% duty cycle generated by the timebase board. Open collector 0 V to -.8 V
Pin 12	STRIG1	Synchronous trigger for timebase board. Generated on Timebase board. ECL level.
Pin 14	STRIG2	Same as STRIG2.

These are special 50 Ω impedance lines that are compensated for distributed capacitance and are terminated at board ends with 47 Ω resistors to the AGND on the motherboard.

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Table 6B-1. SIB Pin Description (continued)

Digital 50 Ω Bus

Pin 18	SMCLK1	Sample rate memory clocks generated by the time-base board to clock acquisition memory on the ADC boards. Open collector ECL 0 V to -.8 V.
Pin 20	SMCLK2	Same as SMCLK 2.
Pin 22	GATE1	Output from timebase which instructs the A to D's to convert samples. Open collector ECL.
Pin 24	GATE2	Similar to Gate 1.
Pin 26	TENBL	Trigger Enable generated by timebase board to enable the trigger circuitry. Open collector ECL.

Each of these lines are used in the acquisition cycle. They are each terminated at each end by 47 Ω to DGND.

Digital Power Bus

Pins 19, 21, 23, 25	-5.2 V	digital power supply
Pins 114-117	+5.2 V	digital power supply
Pins 27,28,37,38, 46,70,93,104,109	Digital Ground	
Pin 113	+5 V ILIMIT	Incremental current limit programming resistor contact for +5 V supply.
Pin 112	-5 V ILIMIT	Incremental current limit programming resistor contact for -5 V supply.
Pin 111	ILIMRTN	Current limit return. Common contact for incremental current limits.
Pin 108	VBATT	Battery back-up power. Tracks the +5 V power supply if it is higher than the battery voltage. If +5 V is lower than the battery, it defaults to the battery voltage of 3 V. Source is on the I/O board.

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Table 6B-1. SIB Pin Description (continued)

Processor Control Bus

Pin 29	16 MHz	Processor clock outputted by the I/O board.
Pin 31	8 MHz	Processor clock outputted by the I/O board.
Pin 33	4 MHz	Processor clock outputted by the I/O board.
Pin 35	2 MHz	Processor clock outputted by the I/O board.
Pin 30	LAS	Address Strobe, TTL level, Controls SIB data transfers on D0-15 lines.
Pin 32	LUDS	Upper data strobe, TTL level, controls SIB data transfers on D8-15 lines.
Pin 34	LLDS	Lower data strobe, TTL level, controls SIB data transfers on D0-7 lines.
Pin 36	RLW	Read not write, TTL level, controls the direction of data on SIB.
Pin 39	LDTACK	Data transfer acknowledge, open collector, input to CPU, asserted by SIB device during SIB bus cycle to indicate that data has transferred.
Pin 69	LBUSERR	Bus error. Input to CPU from bus error timer on I/O board, which is asserted 50 μs after bus cycle if no LDTACK is generated. It has a 1k pullup on the I/O board.
Pin 40	LPOR	Power on reset Signal from I/O board remains low for approximately 200 ms after +5 V supply has reached 4.5 V. It also goes low if +5 V supply drops below 4.5 V during normal operation.
Pins 71-74		Not implemented in this product.

Processor Address Bus

Pins 47-68	A1-22	The SIB is a memory mapped bus. Each card looks like memory to the CPU, and is assigned a certain memory space. With 22 address lines, 4M words are possible. A19-22 are decoded for slot ID, such that these lines must match the ID slot number in order to address the board. This allows each board up to 256k words of address space. There are 1k pullups on the I/O board.

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Table 6B-1. SIB Pin Description (continued)

Processor Data Bus

Pins 77-92	D0-15	Microprocessor data bus, TTL levels, D15 is the MSB and D0 is the LSB. There are 1k pullups on I/O board.

Interrupts

Pins 94-100	LIRQ1-7	Interrupt request lines, open collector. Multiple devices can cause an interrupt. LIRQ7 has the highest priority. 1=Timebase BUSY/DONE 2=Chan 1 or 2 Input Overload 3=RPG Change 4=Keyboard 5=HP-IB 6=68000 On Board Timer 7=Not Used
Pin 102	IENBLIN	Interrupt enable in and out, TTL level.
Pin 103	IENBLOUT	This allows more then one device to cause an interrupt on a single line.
Pin 101	LIACK	Low Interrupt Acknowledge

Miscellaneous

Pin 75	SELECT	Not implemented in this product.
Pin 76	SLAVE BKT	Not implemented in this product.
Pin 105	GET	HP-IB Group Execute Trigger, TTL output from HP-IB interface chip on I/O board. It will be Set when the HP-IB controller asserts the GET command over the HP-IB.
Pin 106	RUN/LSTOP	Acquisition cycle High for RUN and Low for Output from timebase board control register. Used by trigger board to reset the fine interpolator counter and the trigger circuit.
Pins 16,17, 41-45, 107, 110-120		Not Used

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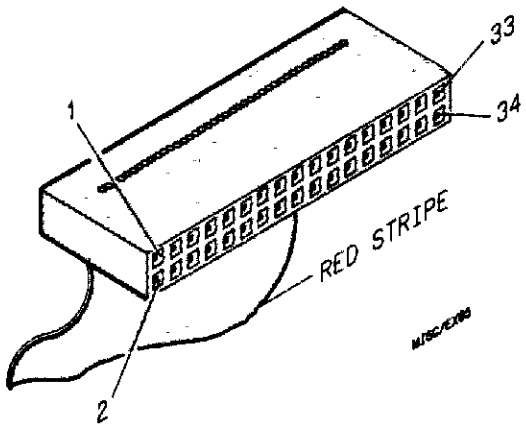


Figure 6B-1. Pin Locations for Control Panel Cable W1, 54100-61601.

Table 6B-2. Control Panel Cable Pin Description.

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	+5 V	8	SC2	15	RPG	22	NC	29	RL7
2	+5 V	9	SC5	16	NC	23	RL4	30	RL3
3	+5 V	10	SC4	17	RPG	24	RL0	31	RPG
4	+5 V	11	SC7	18	RPG	25	RL5	32	RPG
5	SC1	12	SC6	19	LED +	26	RL1	33	NC
6	SC0	13	NC	20	LED -	27	RL6	34	NC
7	SC3	14	NC	21	NC	28	RL2		

The soft keyboard 54100-66517 uses:

SC1
RL2-7
LED +
LED -

The menu keyboard 54100-66516 uses:

SC0
SC1
RL0-5

The control keyboard 54100-66505 uses:

SC2-7
RL0-7

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6B-4. DATA ACQUISITION SECTION

Introduction

The purpose of the data acquisition system is to capture an analog signal and convert it to digital data so the HP 54100 mainframe can use the data to display or output over the HP-IB. The acquisition system contains five plug in boards in the HP 54100A and six boards in the HP 54100D. Table 6B-3 contains a description of the key signals which interconnect the data acquisition boards.

Time Base Board

The purpose of the Timebase board is to control the sampling and data acquisition process. The Timebase board acts as the central control device for all the other boards in the data acquisition section of the HP 54100. Each of the other boards in the data acquisition section receives one or more controlling signals from the Timebase board. The Timebase board contains a Master Clock Oscillator circuit (MASCLK and MCLK), A Sampling Rate Generator circuit (SMCLK), Trigger Delay circuits, Trigger Synchronization circuit (TENBL), and processor board interface circuits. The Timebase board is setup by the CPU to the desired sweep speeds, ranges, etc. After the initial setup, the timebase assumes complete control of the Data Acquisition system. The timebase is responsible for all the high-speed control required to complete an acquisition cycle. An acquisition cycle is a term that has been given a specific meaning in the HP 54100. That is, an acquisition cycle is defined as the sequence of events that must occur in order to acquire a SINGLE record of sampled data. It will normally be the case that several, if not thousands of acquisition cycles, will be required to adequately measure a waveform.

Sampling Board

The purpose of the Sampling board is to acquire data points from an analog signal at a very high speed. There are two Sampling boards in the HP 54100, one for each channel.

The RF input to the Sampling Board is from the probe pod that is installed for that channel. The signal path from the probe pod to the Sampling board is through a coaxial cable connected to the attenuator (metal can) on the Sampling board. The attenuation is programmable via the System Control Bus. The Sampling board also contains an amplifier before and after the sampling circuit to isolate the sampling circuit from external loading, and the high speed sampling circuit, respectively. This board also contains a sync amplifier which provides a signal pick off, (TCLK), for use in the trigger circuit.

Analog to Digital Converter (ADC) Board

There are also two Analog to Digital Converter Boards in the data acquisition system, one for each channel. The signal input to the ADC Board is via a coaxial cable from the top of the Sampling board to the top of the ADC board. The ADC board contains a seven bit analog to digital converter which converts each acquired data value to a digital value. This board also contains a 1024 bit sample memory. The sample memory is a fast in, slow out (FISO) device.

Trigger Board

The Trigger board receives a signal input from the trigger channel 3 input probe pod via a coaxial cable to the top of the board. This signal is used to provide the trigger signal when external triggering is selected. In the HP 54100A, the trigger board receives a trigger sync signal from each of the channel 1 and channel 2 sampler boards. If one of the channels is a trigger source, the sync signal of that channel will be used as a trigger. The board receives a clock signal from the Timebase board. The Trigger board produces the system trigger signal, (STRIG), and places it on the SIB to maintain synchronization between the real signal and the displayed signal. The system trigger is produced from the selected source signal. The trigger board also contains a trigger holdoff circuit to delay the trigger signal for a programmed amount of time, and a programmable counter to delay the output trigger for a programmed number of trigger events.

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Trigger Qualifier board - HP 54100D ONLY

The Trigger Qualifier board receives a signal input from the trigger channel 4 input probe pod via a coaxial cable to the top of the board. This signal is used to provide the trigger signal when external triggering on channel 4 is selected. With the Trigger Qualifier board installed (HP 54100D ONLY) the channel 1 and channel 2 trigger pick off signals are cabled to the Trigger Qualifier board (A10) instead of the Trigger board (A9). Also a signal from the Trigger board (Trigger 3 input) is cabled to the Trigger Qualifier board. Having all four signals input to the Trigger Qualifier board allows the use of four channel state triggering, or sequence of events triggering.

Typical Data Acquisition Cycle

The following is an example of a typical data acquisition cycle. This is not a complete analysis, but covers the main events which occur.

1. The CPU loads the various counters and DAC values with information that the user has input from the front panel. These include:

   Attenuation Factor
   Vertical gain and offset
   Trigger level
   Pre trigger delay
   Post trigger delay
   Trigger holdoff
   Trigger slope
   Trigger enable
   Trigger source

2. The CPU instructs the Timebase board to start and acquisition cycle by asserting the RUN/STOP line. Once this instruction is sent, the CPU is free to perform other tasks until the acquisition is complete. The Timebase board is in complete control of how the data acquisition boards interact with each other.

3. The Timebase board asserts GATE1 which starts the A/D's conversion of the analog input data to digital values. This conversion is performed at a constant rate of 40 mega samples per second.

4. Additionally, GATE 1 starts the counting down of the pre-trigger delay counter. Even though the A to D conversion is constantly taking place at 40 mega samples per second, the digital data values are only stored in the FISO waveform memory at a rate determined by SMCLK (or sample rate generator). This is important at the slower sweep ranges. If the data were clocked in at the 40 MHz rate when set in the 1 sec/div sweep range, the 1024k acquisition memory would be filled up almost instantly.

5. When the pre-trigger delay counter reaches zero, the TENBL line is asserted. This line is used by the Trigger board as an advisory that it can accept a trigger. If the pre-trigger delay counter contains a zero, then TENBL asserts at the same time that RUN/STOP is asserted.

6. The Trigger board is now waiting for a trigger event to occur on the trigger channel that was chosen as the trigger source. Remember, all this time the A/D has been sampling the input IF signal and has been loading the digitized information into the acquisition memory.

7. Finally, the trigger event occurs and is brought in from the source by the TCLK coax. When the programmable trigger holdoff counter reaches zero, the trigger flip-flop is asserted, indicating the completion of all trigger criteria for a valid trigger.

8. The output of the trigger flip-flop starts the fine interpolator and asserts STRIG when the next master clock edge occurs.

9. STRIG is received by the Timebase board and immediately starts the coarse interpolator. The coarse interpolator counts the number of master clock transitions between the asynchronous trigger event and the next sample clock transition.

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10. The fine interpolator measures the time between the asynchronous trigger event and the next transition of the master clock signal to 10 ps resolution.

11. STRIG also starts decrementing the post-trigger delay counter.

12. Once the post-trigger delay counter reaches zero, the Timebase board negates GATE1 on the next occurrence of the sample clock. Additionally, the coarse interpolator is halted.

13. The acquisition cycle is now complete and the CPU is advised by the BUSY/DONE line.

14. The CPU clears all of the DACs and counters, deasserts RUN/STOP, and as a result TENBL goes low.

15. The CPU then reads the acquisition FISO, fine interpolator, coarse interpolator, and manipulates this data for display on the CRT.

Table 6B-3. Acquisition Signals.

Signal Name	From Timebase to	Function
MASCLK0A	Chan 1 Sampler	40.849673 MHz "Clean" clock input to sample pulse generator.
MASCLK0B	Chan 2 Sampler	40.849673 MHz "Clean" clock input to sample pulse generator.
MASCLK0C	Trigger Board	40.849673 MHz "Clean" clock enables the synchronous trigger, and stops the fine interpolator.
TENBL	Trigger Board	Used to arm and reset the trigger and fine interpolator.
STRIG	Trigger Board	Used to enable the coarse interpolator and to initiate post trigger delay.
MASCLK1	Chan 1,2, both ADC boards	40.849673 MHz clock delayed from MASCLK0. Used to clock the A to D conversion.
SMCLK1,2	Chan 1,2 both ADC boards	Used to control when digitized data is loaded into the FISO RAM.
GATE1	Chan 1,2 both ADC boards	Pulse used to enable or inhibit the conversion of data by the ADC's.

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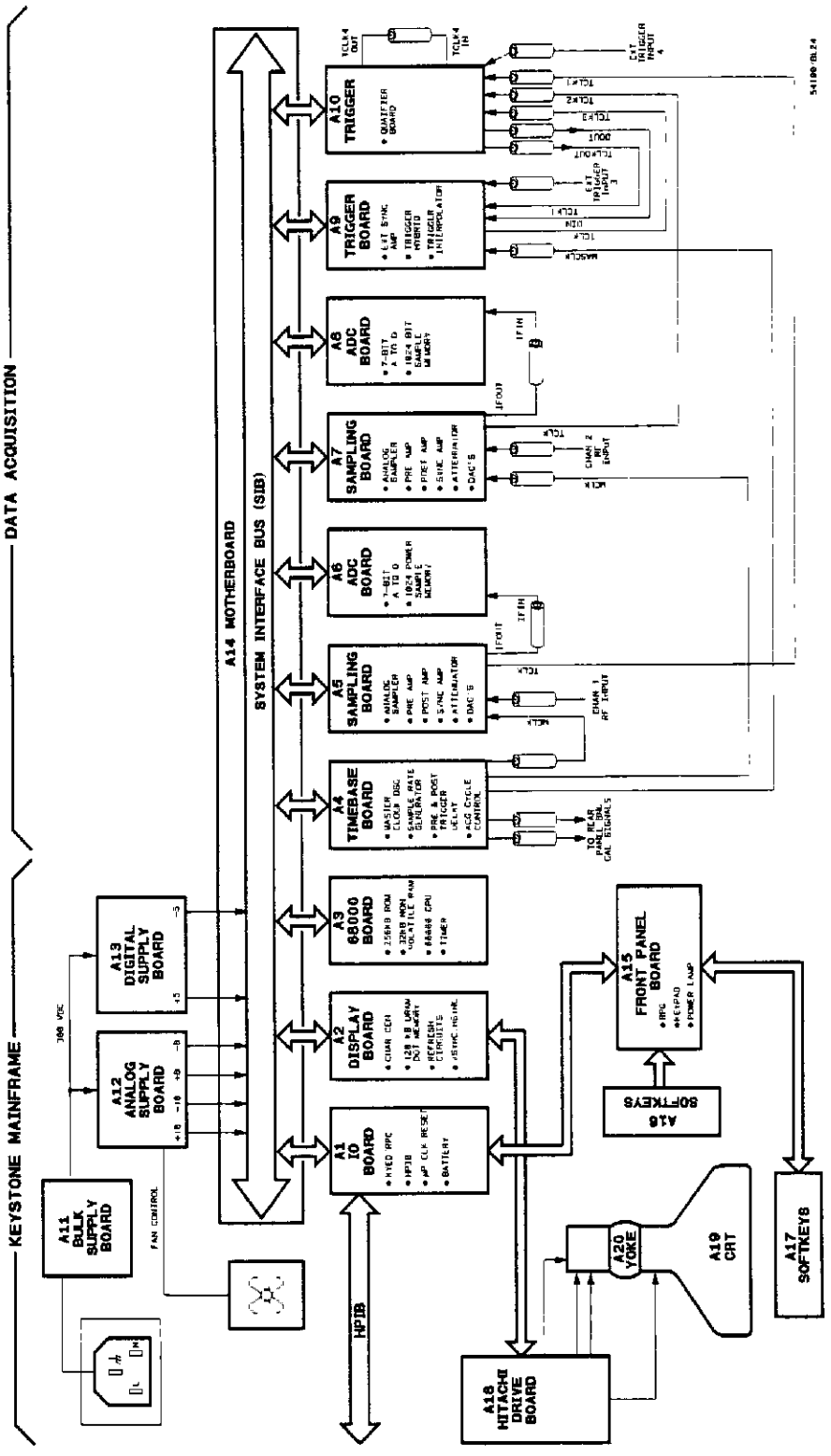


Figure 6B-2. Overall Block Diagram

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6B-5. SIMPLIFIED SIGNAL FLOW

Introduction

The following discussion will track a channel 1 signal through the entire HP 54100A. In order to keep this discussion simple, only channel 1 is discussed or shown on the reference drawing, figure 6B-3. This discussion could just as well be used for channel 2, as channel 1 and channel 2 operate in an identical manner.

Placing the probe (any of several) on a signal point will produce a signal to the channel 1 probe pod. The probe and probe pod are not part of the HP 54100A/D, but are an accessory that plugs into the HP 54100 mainframe. For information about the probe and probe pod, refer to the operating note for that accessory. The probe pod sends several signals to the HP 54100A. Three of the lines from the probe pod carry an identification signal. These signals allow the HP 54100 to read the probe attenuation factor. The other important signal from the probe pod is the actual signal to be captured and displayed. This signal is sent to the HP 54100 channel 1's Sampling board by a coaxial cable. The rest of the wires to the probe pod carry power and ground for the active components in the probe pod.

The input signal, Channel 1 RF Input, is connected through a coaxial cable to an attenuator module mounted on the Sampler board. The attenuation is set by the CPU or from the front panel of the HP 54100. Refer to the Simplified Signal Flow diagram, figure 6B-2. After the signal has been attenuated to the proper level, it is then sent to a buffer where the signal is amplified and split. The main signal path is to the sampler circuit. The other path is a pickoff of the signal that is sent to the Trigger board to allow the instrument to trigger on the channel 1 signal if desired. The trigger circuits will be discussed later in this theory.

The main portion of the signal goes to the sampler circuit. The sampler circuit consists of a sampling bridge, sampling pulse generator, and a post amplifier circuit. The output of the sampler circuit is connected to the Analog to Digital Converter Board via a coaxial cable.

Channel 1 IF is from the channel 1 sampler and is the signal input to the Analog to Digital Converter (ADC) board. At the input of the ADC, a Buffer/Amplifier with a gain of 10 will isolate the output of the ADC board and amplify the input signal. The ADC changes each sampled analog data point to a seven-bit digital value. The digital data bits are converted from ECL levels to TTL levels by the ECL/TTL Converter. The TTL data bits are then loaded into one of a set of four, high-speed data latches. The data contained in the four, high-speed data latches are then randomly loaded into a standard eight-bit RAM. Because the RAM is loaded at a relatively slow speed from the four sets of high-speed data latches, each of the sampled points will not necessarily be stored in the RAM. The high-speed data latches may be loaded several times before the data in that set of latches is read into the RAM. This makes the usable data points read into the RAM completely random. In this way we produce a Fast In Slow Out memory. That is, the data is stored into the data latch at sample speed and loaded to the RAM and used at normal display speed.

The 1024-bit FISO memory stores the data until the data can be used by the display circuits. The FISO memory data is moved, via the System Interface Bus (SIB) under the direction of the CPU, to the Display board. The processor interface circuits on the Display board maintain communication with the CPU, buffer the FISO data from the SIB, and accept and decode the address information from the CPU. Once the data is buffered it is then controlled by the timing and control circuits of the Display board.

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The Display board Timing and Control circuits control all information from the processor interface circuits to either the Character or Graphics circuits. The Character circuits contain a character ROM, character RAM and character attributes circuits. The Graphics circuits contain a graphics RAM and refresh circuits. The data from the Character and Graphics circuits then go to the Encoding circuits where a parallel to serial data conversion takes place. The serial data is then sent to the display driver board in a pixel display format.

The Timing/Control circuits will produce horizontal and vertical sync for the display, will generate a dot clock to properly time the graphics data to the horizontal and vertical sweeps, will generate a character clock to properly synchronize character display with the horizontal and vertical sweeps, and will create other necessary timing. These serial data, clocks, and sync pulses then go to the Encoding circuits. These circuits supply the video encoding and attribute encoding necessary to create a usable display.

After the Encoding circuits, the display data, sync pulses, and encoded information is sent to the Display Driver board. This board supplies the high voltage and drive signals required by the CRT.

The Sampler board had a portion of the input signal picked off for use by the Trigger board. The voltage that is picked off is sent to a voltage comparator to ensure the voltage is sufficient to create a valid trigger signal. Once the signal is on the trigger board, it is ORed with a similar signal from the channel 2 circuits, and another similar signal from the Trigger 3 Input Probe Pod.

The output of the ORed trigger signals places a digital level on the input of the Trigger Flip Flop. The Trigger Flip Flop will produce an output when the ORed signal is present, a clock is present from the timebase board, and the programmable Trigger Holdoff has met its programmed holdoff time. When the Trigger Flip Flop produces an output it goes to the Trigger Interpolator. The Trigger Interpolator circuit keeps track of the time difference between a timebase clock and the trigger signal. The trigger signal out of the trigger interpolator goes to a programmable counter which will cause a programmed number of trigger events to occur prior to placing the trigger signal (as a digital byte) on the System Interface Bus. In many cases the programmed holdoff will be the minimum value and the programmed number of events will be zero.

Once the trigger byte has been placed on the SIB the microprocessor will read and use the trigger to properly synchronize the input signal with the displayed signal. Keep in mind that all the programmable devices are programmed by the microprocessor through the System Interface Bus.

Notice that the function of the Clock Generator and Timebase Board is shown to produce the proper clock signals for the sampler and A/D converter. The timebase is programmable to produce these clocks at the proper time and in synchronization with the sampling rate and selected sweep speeds.

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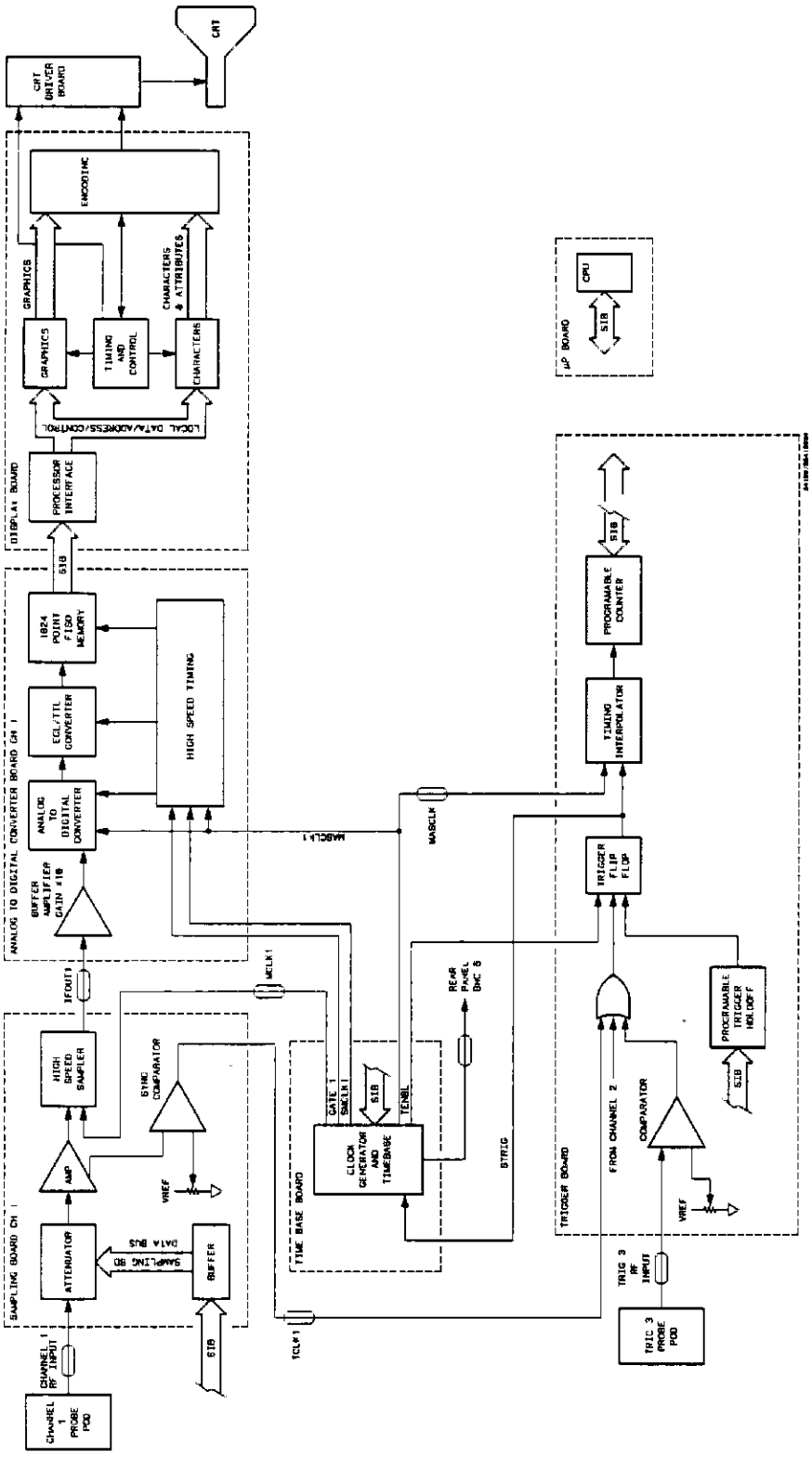


Figure 6B-3. HP 54100A/D Simplified Signal Flow Diagram

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6B-6. I/O ASSEMBLY

Introduction

Refer to figure 6B-4. The I/O Assembly serves two major purposes. First, it provides instrument interface to the keyboard and HP-IB by two ribbon cables. Second, it provides several system functions, all of which are described below. In addition the I/O contains passive pull-up resistors for data, address, and control lines for the System Interface Bus, (SIB).

HP-IB

U21 (TMS9914) interprets HP-IB commands and controls direction of data flow from an external controller to a local data bus. One side of U21, LD0-7, connects to the local data bus. The other side of U21 connects to two bidirectional data transceivers, U11 for data and U12 for control commands. All HP-IB addressing is accomplished with software, therefore no address lines are carried on the ribbon cable.

RPG

The RPG outputs two out-of-phase pulses. Direction of rotation is determined by the difference in phase angle between both pulses. The pulse frequency is a function of rotation speed and this tells the microprocessor what size of incremental steps to take. Part of U7 detects RPG activity, and interrupts the microprocessor by IRQ3 line.

Keyboard Controller

U1 (8279-5) sees a keyclosure and interrupts the microprocessor by IRQ4 line. U1 detects which key was pressed by scanning column lines with pulses and by sensing rows for a return path. When U1 is enabled, it converts key closure scan data to parallel data and places this data on the local data bus.

System Interrupt Latch

Allows one processor to interrupt any other in a multiprocessor system. Only one processor is used in the HP 54100A/D system.

Function Decoder

Decodes address lines A12-A14 to enable Keyboard controller U1, RPG Counter U15, HP-IB Controller U21, Board Type U29, and Power Supply status through U26.

Slot Decode

U25 is a 4-bit comparator which compares slot address lines A19-A22 with slot ID codes ID0-ID3. When this board is addressed, both codes will be equal. Then U29 pin 6 will enable the bidirectional buffer U28.

Board Type

One side of U29 is hard wired to represent the board ID number. When the microprocessor asks for board type, U10 pin 15 enables U29 which places a board ID number on the local data bus.

DTACK Generator

U16 generates LDTACK which is sent back to the microprocessor indicating data was received. This signal also resets the bus error timer.

Bus Error Timer

Under normal operation U18 should be reset by LDTACK before a time constant set by R19 and C40 times out. If U18 is not reset, it will generate LBUSERR which keeps the CPU from getting hung up in an instruction cycle. This could happen if any addressed board does not generate LDTACK, or if the microprocessor tries to access a nonexistent board.

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TTL Oscillator

A crystal controlled 16 MHz oscillator. A binary counter divides it into 8 MHz, 4 MHz and 2 MHz. All four signals are placed on the System Interface Bus.

Power Detect

It samples all 6 supply voltages. If one or more fails, then the front panel led will not illuminate.

Power on Reset

The power on reset circuit provides a 175 ms glitch-free pulse shortly (about 5 ms) after power up and power down. This sets many devices to a known state and prevents the microprocessor from taking damaging action during power up. This also provides a means to reset the system with a pushbutton on the I/O board without powering down the instrument.

Non-Volatile Ram Power Supply

A battery provides power for RAM memory to retain basic setup information and system configuration for several years. The circuit also provides for smooth transfer of power from battery to power supplies after power up.

SIB Resistive Pullups

The resistive pullups on the I/O board give the SIB lines known logic levels when they are not being driven by devices, as opposed to letting these lines float.

Table 6B-4. I/O Assembly Mnemonics

MNEMONICS	DEFINITION
DI1-8	HP-IB Data Lines 1-8
D0-7	SIB Data Lines 0-7
DS	Data Strobe
IDO-3	Board ID Lines 0-3
LIRQ1-7	Low Interrupt Request Lines 1-7
LA1-3	Local Address Lines 1-3
LAS	Low Address Strobe
LDTACK	Low Data Acknowledge
LD0-7	Local Data Lines 0-7
LEN	Low Enable
LLDS	Low Lower Data Strobe
LRHPIB	Low Read HP-IB
LRKEY	Low Read Keyboard
LRPWR	Low Read Power
LRRPG	Low Read RPG
LSB	Least Significant Bit
LSTROBE	Low Strobe
LUDS	Low Upper Data Strobe
LWHPIB	Low Write HP-IB
LWKEY	Low Write Keyboard
LWRPG	Low Write RPG
R/LW	Read Low Write
RPG	Rotary Pulse Generator
SIB	System Interface Bus

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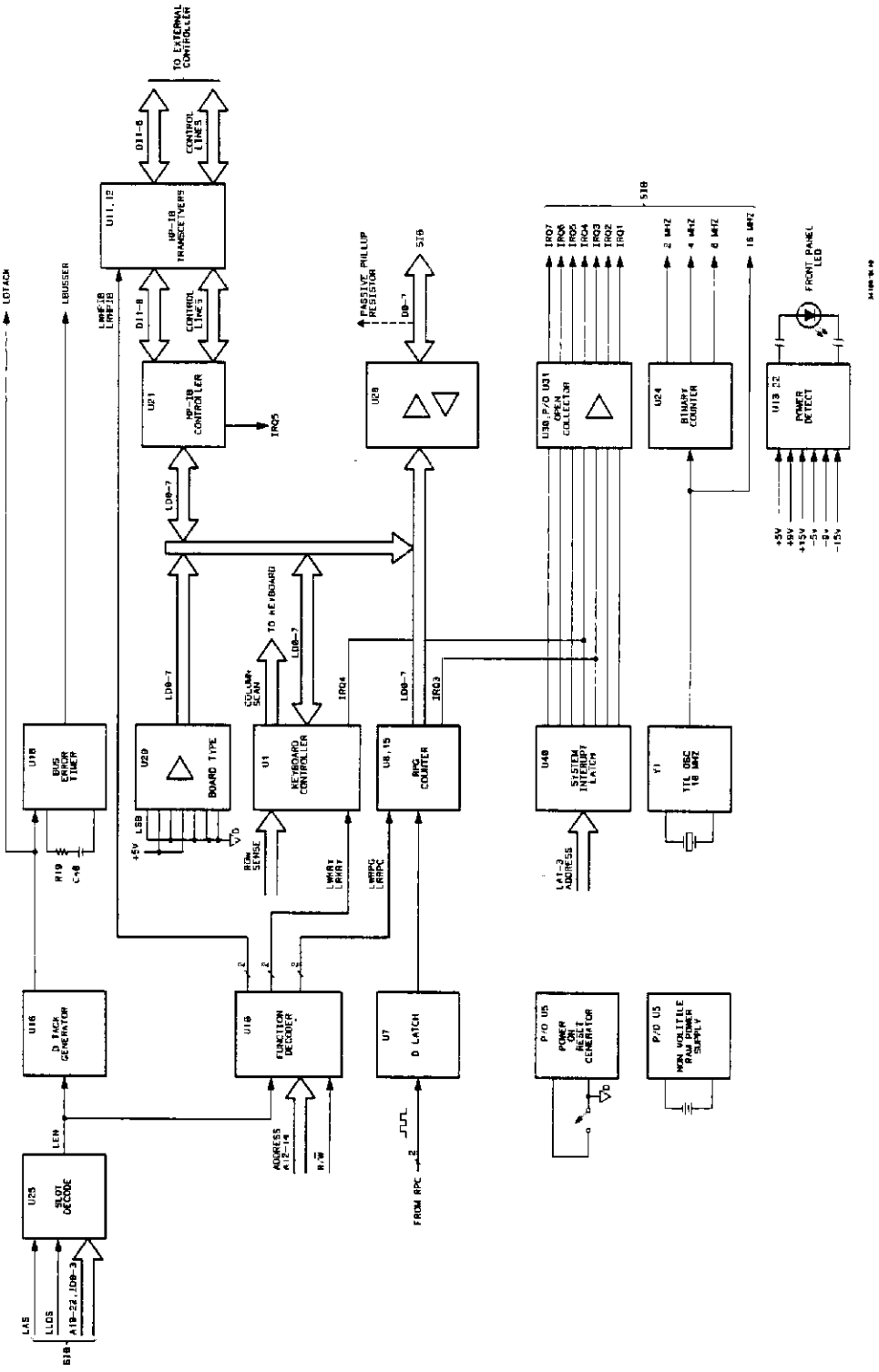


Figure 6B-4. Input/Output Assembly Block Diagram.

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6B-7. MICROPROCESSOR ASSEMBLY

Introduction

Refer to figure 6B-5. The microprocessor (CPU) has two major functions, data acquisition and I/O interfacing. It starts a data acquisition cycle by setting a RUN/LSTOP bit on the Time Base board. Some time later, the Time Base board sets a LBUSY/DONE bit which tells the microprocessor an acquisition cycle is finished. The microprocessor will then move data from ADC board memories to display board memories. I/O interfacing involves updating display information, interpreting key closure data, RPG data, and HP-IB commands. In the remote mode, the microprocessor takes commands from an external controller.

CTC

The counter timer chip (ctc) contains three counters. The microprocessor programs and reads each counter over LD0-7 lines. Each counter has an output which is used as an interrupt to the microprocessor. All three counter outputs are ORed through U35 and U42. This result is ORed through U40 with LIRQ6 from the SIB. This result is applied to the system interrupt latch.

System Interrupt Latch

A system so the microprocessor can mask off any or all interrupt lines. The microprocessor sends data to U1 on LD0-7 lines. For normal operation all outputs of U1 are normally a low, and all incoming SIB interrupt lines are normally a high. When an interrupt occurs on the SIB, that interrupt line will be a low, the corresponding output of U17 or U18 will also be a low. The microprocessor can mask off any interrupt lines by simply writing a high to U17 or U18 through U1. This will guarantee that corresponding output levels of U17 or U18 will also be a high regardless of what the SIB interrupt lines are doing.

Priority Encoder

Encodes all seven incoming interrupt lines into three lines for the microprocessor. If more then one interrupt occurs at the same time, U34 will prioritize them so the interrupt with the highest priority will be processed first. When an interrupt occurs, the system is vectored to a predetermined software location.

Bus Arbitration

This board contains circuitry so it will operate in a multiprocessor system. With only one microprocessor being used, the bus request and bus grant signals are tied to the proper logic levels to ensure this board will have control over the SIB when required.

Bus Buffers

Bus buffers enhance the drive capabilities of the microprocessor. When enabled, they connect the microprocessor with the correct bus, these are:

- U48 and U49 for SIB data bus
- U45, U46 and U47 for SIB address bus
- U4 and U21 for local data bus
- U5, U6, U22 and U23 for local address bus

Decoders

U36 decodes PA16-18 to enable ROM pairs 0-7. U19 decodes PA14-16 to enable RAM pairs 0 and 1, interrupt latch, and counter timer chip.

CPU

A Motorola 68000 microprocessor running at 8 MHz. Main characteristics are: 16 bit data bus, 23 bit address bus, and 3 interrupt lines. At initial power up condition, power on reset (POR) insures the CPU will start-up in a known condition. The CPU will then run several routines, some of which are: determine which board type is in which slot, system self diagnostics, setup display information.

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The CPU will now respond to system interrupts, HP-IB, keyboard, or RPG. To the CPU all system boards look like memory locations. When A23 is a high, then the CPU is accessing system memory over the SIB. When A23 is a low, then the CPU is accessing local processor board memory locations. After the CPU sends data over the SIB, LDTACK comes back from the addressed board which tells the CPU the information was received. This LDTACK also goes to the I/O board and resets the bus error timer. If the bus error timer is not reset, then BUSERR is sent to the CPU which will display a SOFTWARE ERROR message on the CRT.

Memory

The ROMs and RAMs have 8-bit data lines. To achieve 16-bit data words, 16-bit words are divided into a lower portion LD0-7, and an upper portion LD8-15. ROMs or RAMs are read in pairs. Software instructions for the CPU are contained in ROM memory. There is space for eight ROM pairs, but some instruments may use fewer ROMs. Please refer to the replaceable parts (Section 5) to find out how many ROMs your instrument contains. Non-volatile, battery backed-up RAM memory contains stack registers, status registers, scratch pad memory, instrument serial number, and soft cal information.

Table 6B-5. Microprocessor Assembly Mnemonics

MNEMONICS	DEFINITION
CPU	Central Processing Unit
CTC	Counter Timer Chip
LD0-15	Local Data lines 0-15
LDTACK	Low Data Acknowledge
LIRQ1-7	Low Interrupt Request lines 1-7
PA1-22	Microprocessor Address lines 1-22
PD0-15	Microprocessor Data lines 0-15
POR	Power On Reset
SIB	System Interface Bus
1LA1-15	Lower Local Address Lines 1-15
2LA1-15	Upper Local Address Lines 1-15

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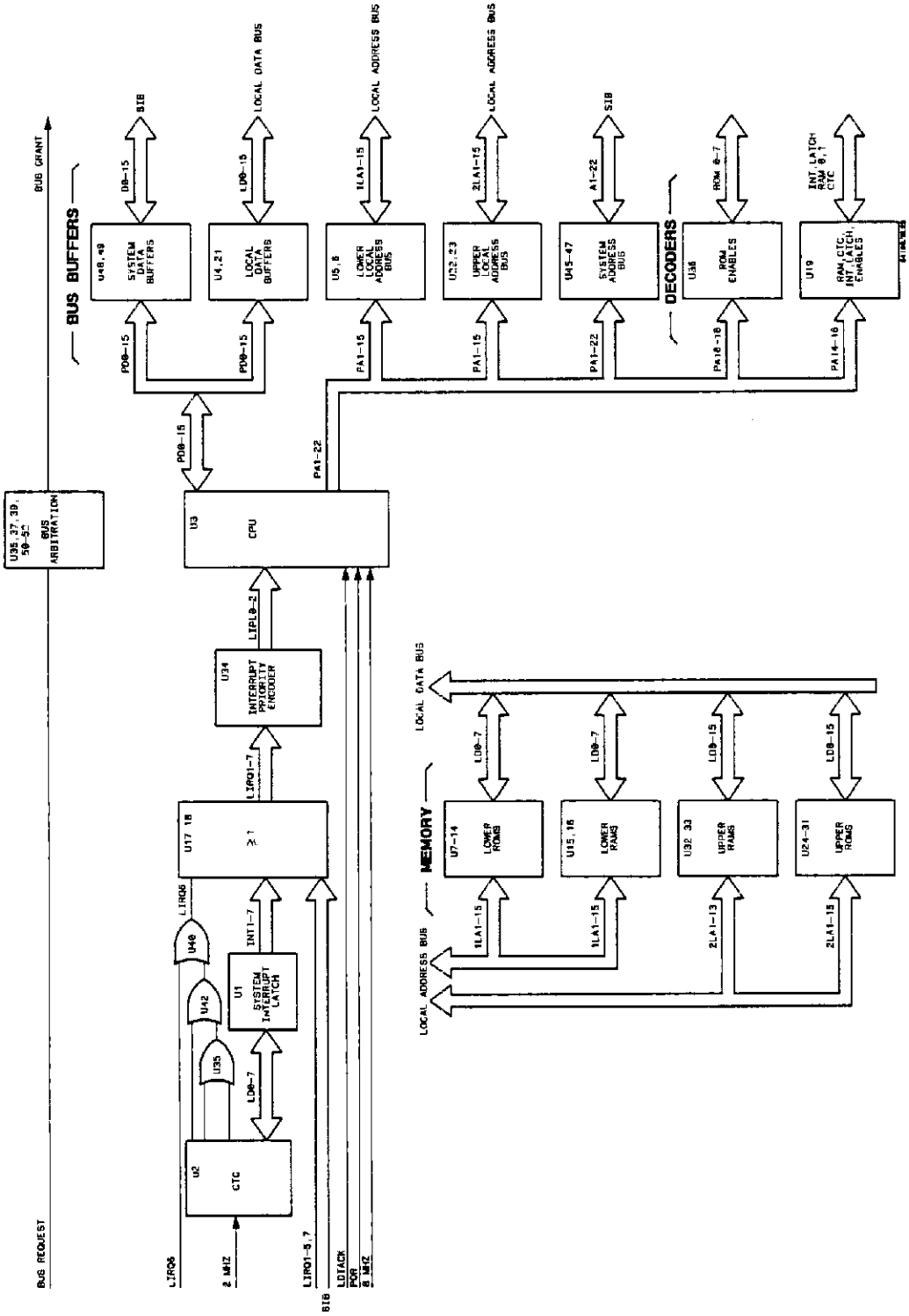


Figure 6B-5. Microprocessor Assembly Block Diagram.

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6B-8. DISPLAY ASSEMBLY

Introduction

Refer to figure 6B-6. The display board sends display information to the CRT. This display information consists of text, graphics, and their associated attributes. Attributes contain the information for displaying data in either full bright, half bright, blink, inverse video, and underline.

Slot Decode

U71 is a four bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When this board is addressed, the codes will be equal. U71 pin 6 will output a pulse to the D latch and function decoder.

D Latch

At the end of a character cycle, D latch will send LDTACK over the SIB.

Function Decoder

Decodes address lines A17 and A18 to enable various board functions, these are: LLATCHEN for board type, LCMEN for character RAM, LCRTC for CRT controller, LDRAMEN for graphics control register and graphics memory.

Board Type

When board type is requested by the microprocessor, this board will respond with 13 over LD0-3 lines. LD0, 2 and 3 will be pulled high through U74, and LD1 will be pulled low though U74. LD0 is the least significant bit so adding LD0, 2 and 3 will give 13.

Video Attribute Register

Decodes LD0 and LD1 to determine attributes for A and B video.

Dynamic Ram

16 dynamic RAMs (DRAM) where graphics data is stored. Incoming data comes through two sets of bidirectional data transceivers during a write cycle, U72/U73 and U75/U81. Two sets of video data are stored in DRAMs, A video and B video. To read video data two read cycles are required, first for A video and second for B video. Since A and B video arrive at the shift registers at different times, A video passes through a 21-bit shift register and B video passes through a 16-bit shift register. This way A and B video will arrive at the encode circuit at the same time.

DRAM Address Mux

Uses the ripple counter's output to form DRAM address lines RAS (row address strobe) and CAS (column address strobe).

Graphics Control Resister

An operator can place text on the display with an external controller. The controller addresses the DRAMs through two sets of data transceivers, U68/U69 and U32/U53.

RAM Address Mux

Addresses character RAMs. This addressing can be done by either the microprocessor through data transceivers U68 and U69, or by CRT controller U46.

Character RAM

The microprocessor stores each ASCII character and its attributes in RAMs.

Character and Attribute Register

Addresses the character ROM and sends character attribute information to character attribute register.

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Character ROM

Functions as a character generator by decoding ASCII data from character RAMs and row address lines from CRT controller. This data is then sent through the character shift register.

Character Shift Register

Parallel loaded with character data and serially outputs character video to the encoder circuit.

Character Attribute Register

Tells the encode circuit the attribute, if any, for each character to be displayed. These are: I inverse video, U underline, B blink, F full bright.

Encoder Circuitry

Sends character video or graphics video with correct attributes to the display driver board.

Blink Oscillator

Generates a 2 Hz waveform which is used as blink time period when the blink attribute is used.

Dot Clock

Generates a 20 MHz clock which is used for all display board timing waveforms.

Divide by 16

Divides 20 MHz dot clock by sixteen to form the 1.25 MHz character clock.

Ring Counter

Generates eight phases of character clock used as timing signals throughout the display board. U16 inverts phases 1 and 6.

CRT Controller

Controls the basic timing of the CRT and drive circuits. It is a bank of 18 programmable counters which are programmed by the microprocessor during the power-up sequence. This programming includes the number of characters, rows, character cell size, guard cell size, etc. Vertical and horizontal synchronization are output by this circuit to the display driver module.

Table 6B-6. Display Assembly Mnemonics

MNEMONICS	DEFINITION	MNEMONICS	DEFINITION
AA0-11	Attribute Address lines 0-11	ID0-3	Board ID lines 0-3
A1-16	SIB address lines 1-16	LA1-12	Local Address lines 1-12
B	Blink	LCMEN	Low Character Memory
CA0-11	Character Address lines 0-11	LCRTC	Low CRT Controller
CCLK	Character Clock	LDRAMEN	Low Dynamic Memory
D0-15	SIB Data lines 0-15	LD0-15	Local Data lines 0-15
DCLK	Dot Clock	LPH1,6	Low Phases 1 and 6
F	Full Bright	MA0-11	Memory Address lines 0-11
HFB	High Full Bright	PH1-8	Phases 1-8
HHB	High Half Bright	SIB	System Interface Bus
I	Inverse Video	U	Underline

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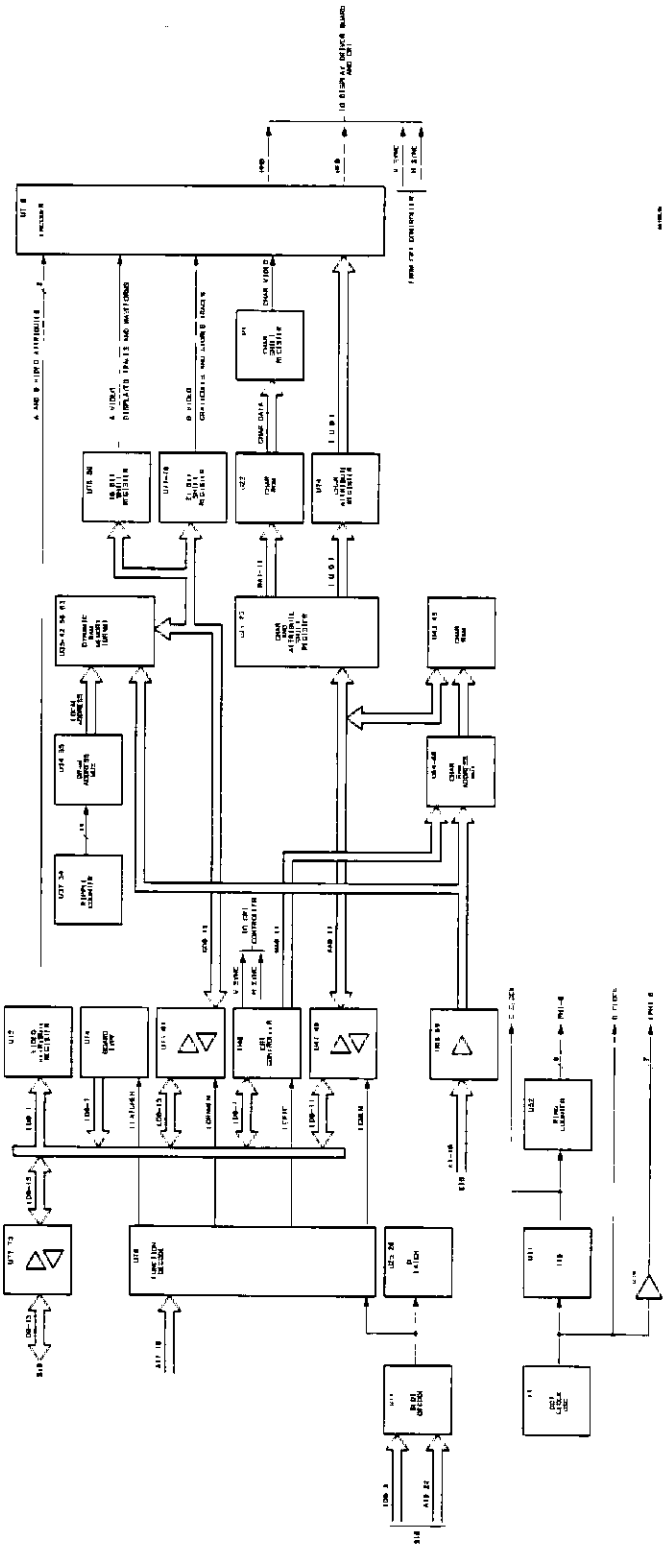


Figure 6B-6. Display Assembly Block Diagram.

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6B-9. Timebase Assembly

Introduction

Refer to figure 6B-7. The main purpose of the Timebase board is timing control for an acquisition cycle. An acquisition cycle is a sequence of events which must occur for a single record of sampled data to be stored in memories on the ADC board.

Master Clock Operation

The master oscillator generates a crystal controlled sine wave of approximately 80 MHz. This 80 MHz is applied to U43, which consists of several delay lines. The dither circuit is a ring counter which operates when the Timebase board is between acquisition cycles. When another acquisition cycle starts, this counter is stopped and outputs a random number to enmux, U41. U41 uses this random number to select which delay line to pick the 80 MHz from. This random selection of delay line lengths for each acquisition cycle causes a dithered 80 MHz. This is called dithering because the MASCLK starting point is continually changing for each acquisition cycle. Dithering is used so that during each acquisition cycle a different record of data points will be taken from the waveform. Divide by 2 divides this dithered 80 MHz into a dithered 40 MHz MASTER CLOCK, (MASCLK). MASCLK is the basic timing control for acquisition cycles

Slot Decode

U36 is a 4-bit comparator which compares slot address lines A19-A22 with slot ID codes ID0-ID3. When this board is accessed, the two codes will be equal. U36 pin 6 will output a pulse to the D Latch.

D Latch

Enables function decoder U24, and outputs LDTACK to the SIB.

Function Decoder

Decodes address lines A1, A15, and R/LW to enable the various parts on this board. The enable signals it produces are: read coarse interpolator RENCI, read status register RENSTAT, read board type RENTYPE, write to control register WENCTL, and shift clock SFTCLK.

Trigger Synchronization

When STRIG goes high, the CICLK will start running. At some point in time later, SMCLK will also go high. Trigger synchronization will then disable the coarse interpolator counter and will start PTDCLK.

Coarse Interpolator

A digital counter which is an extension of the Trigger board's fine interpolator. The fine interpolator measures the time from trigger point to the next 40 MHz MASCLK. The coarse interpolator then measures how many MASCLK edges occur before the next sample clock occurs. This is necessary bcause the sample memory clock may not be equal to MASCLK (see sample rate generator). Both the coarse and fine interpolators are read by the CPU after a data acquisition cycle. RENCI enables U25 and U38 to pass coarse interpolator data.

Board Type

When board type is asked for, LD0-LD2 and LD4-LD7 will be pulled low by the grounding of their inputs to U26. LD3 wils be pulled high because its input to U26 is connected to +5 volts. LD0 is the least significant bit, so LD3 being high represents the board type 08. Eight is put on the SIB through U37.

Divide by 16

Divides the 8 MHz input clock by sixteen to produce a 500 kHz clock. This 500 kHz square wave is used for the rear panel Cal signals.

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Pre-Trigger Delay

A programmable delay which determines how much time must elapse from the beginning of an acquisition cycle to when trigger is enabled. This pre-trigger delay establishes the negative time limits of an acquisition window. When the pre-trigger delay counter reaches zero, the TENBL line is asserted.

Control Register

The microprocessor board sets a RUN/LSTOP bit on the Timebase board through control register, U29. This initiates a series of events which enables the ADC boards to store sampled data into memories.

Status Register

At the end of an acquisition cycle, the Timebase board flags the microprocessor by setting the LBUSY/DONE bit. The microprocessor checks if the Timebase board is finished with an acquisition cycle, by checking the status register.

Gate 1

Signal which actually controls an acquisition cycle. When gate 1 is true, then data will be stored into memories on the ADC boards.

Post-Trigger Delay

A programmable counter which is preset to control the number of samples stored after the occurrence of trigger. Post-Trigger delay counts sample clocks, not 40 MHz MASCLK. This controls how much positive time is covered during an acquisition cycle. This relates to how many samples are put on screen after the trigger event. When the post-trigger delay counter reaches zero, the DONE line is asserted. This indicates to the CPU that a data acquisition cycle is over.

Sample Rate Generator

A programmable frequency divider which produces two clocks, SMCLK1 and SMCLK2. These clocks are used to control the rate at which digital data is stored in sample memories on ADC boards. Table 6B-8 contains a list of front panel sweep speeds which results in particular SMCLK frequencies.

Table 6B-7. Timebase Assembly Mnemonics

MNEMONICS	DEFINITION
A19-22	SIB Address lines 19-22
CI0-15	Coarse Interpolator data lines 0-15
CICLK	Coarse Interpolator Clock
D0-15	SIB Data lines 0-15
IDO-3	Board ID Lines 0-3
LBUST/DONE	Low Busy Done bit
LD0-15	Local data Lines 0-15
LDTACK	Low Data Acknowledge
LRUN/STOP	Low Run Stop bit
MASCLK	Master Oscillator Clock
PTDCLK	Post Trigger Delay Clock
RENCI	Read Enable Coarse Interpolator
RENTYPE	Read Enable Board Type
RENSTAT	Read Enable Status Register
SIB	System Interface Bus
SFTCLK	Shift Clock
SMCLK1	Sample Memory Clock 1
SMCLK2	Sample Memory Clock 2
STRIG	Synchronous Trigger
TENBLE	Trigger Enable

Table 6B-8. Sweep Speed vs SMCLK

Sweep Speed	SMCLK freq.
1 s	25 Hz
500 ms	50 Hz
200 ms	125 Hz
100 ms	250 Hz
50 ms	500 Hz
20 ms	1.25 KHz
10 ms	2.50 KHz
5 ms	5.00 KHz
2 ms	12.5 KHz
1 ms	25.0 KHz
500 µs	50.0 KHz
200 µs	121 KHz
100 µs	232 KHz
50 µs	425 KHz
20 µs	1.13 MHz
10 µs	2.04 MHz
5 µs	3.40 MHz
2 µs	10.2 MHz
and above	

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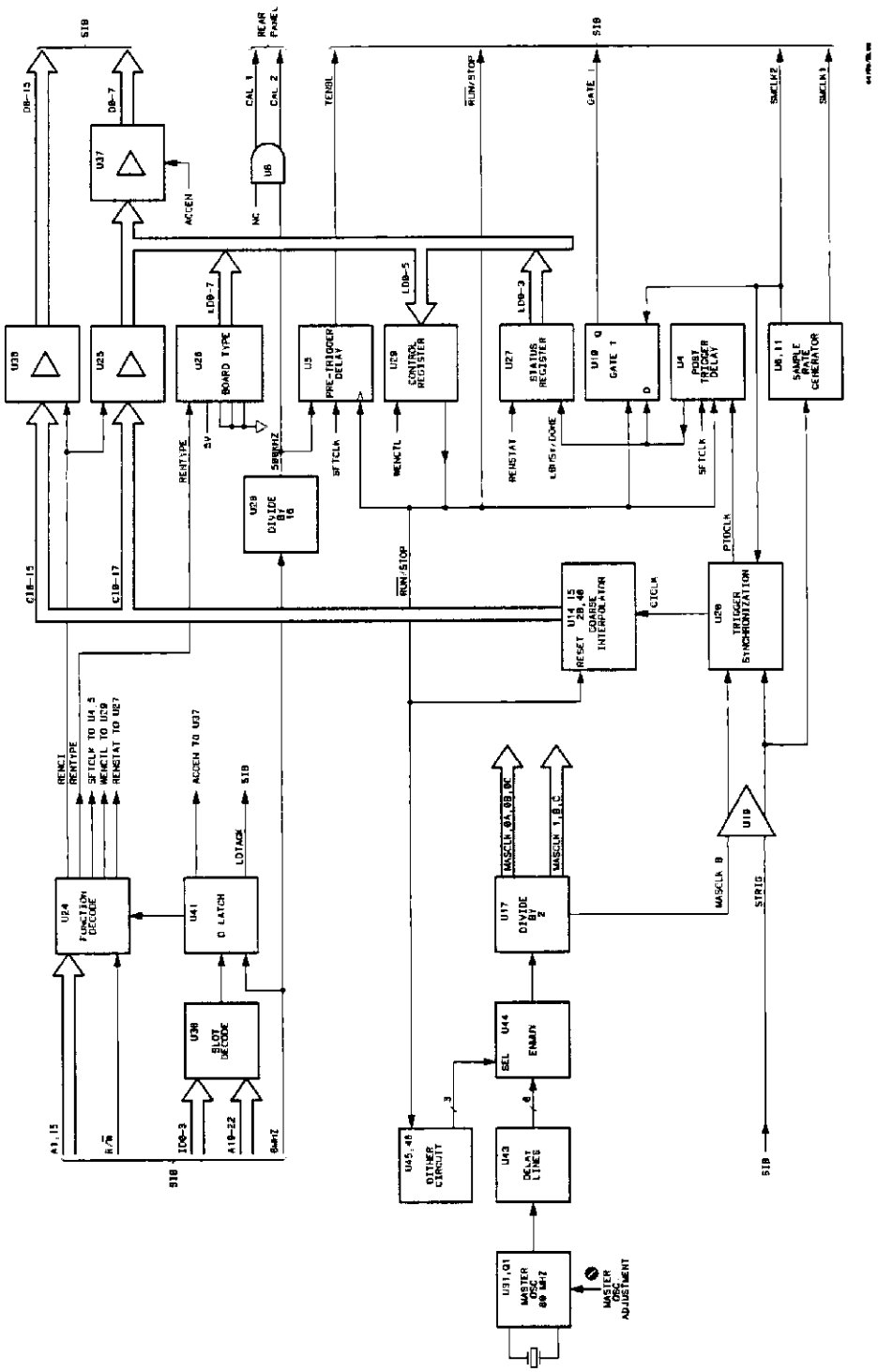


Figure 6B-7. Timebase Assembly Block Diagram.

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6B-10. SAMPLER ASSEMBLY

Introduction

Refer to figure 6B-8. The sampler board has two major purposes. First, it samples the incoming RF signal at the 40 MHz MASCLK rate. Second, it provides a sync out signal which can be used for triggering purposes.

Voltage Regulators

The inputs are the unregulated supplies from the analog power supply via the SIB connector. The outputs are regulated supplies for various uses on this board.

Attenuator

A 50 Ω programmable attenuator which scales the input signal to a level within the dynamic range of the preamplifier hybrid. The attenuator has three cascaded ranges: X2, X5, X10. These ranges can be combined to give steps of attenuation between X1 and X100. Table 6B-10 contains a logic table that correlates the front panel vertical sensitivity to the attenuator control words.

Preamplifier

The preamplifier has two major purposes. First, it terminates the RF output from the attenuator into 50 Ω. Second, it splits the RF input into two parts. These two parts are RF out and sync signal. The preamplifier isolates the sync hybrid from the sampler hybrid. This keeps sampler interference from causing false triggering in the sync hybrid.

Trigger Level DAC

The trigger level DAC converts eleven digital input lines from the shift registers to a dc level. This dc level is called the trigger level threshold.

Sync Comparator

When the sync signal crosses the trigger level threshold, logic transitions will occur. The logic transitions correspond to the sync signal and polarity switch inside the sync hybrid. When this channel is enabled, TCLK OUT edges will occur.

Sampler Hybrid

The sampler hybrid contains three functional blocks, a sample pulse generator, a sampling bridge and a post amplifier. The sample pulse generator uses MASCLK to generate a 3 ns wide pulse for the step recovery diode (SRD). The SRD produces a much faster and narrower pulse for use by the sampling bridge. The sampling bridge takes one sample of data each time it receives a pulse from the SRD. Sampling continues at the 40 MHz rate of the MASCLK. The post amplifier is used to amplify a very small signal coming from the sampling bridge. The post amplifier also has a dc feedback loop which samples the incoming RF signal and compensates for dc drift in the sampler hybrid.

DC Offset DAC

The dc offset DAC converts eleven digital input lines from the shift registers to a dc level. This dc level is applied to the sampler hybrid through a dc feedback loop. This offset is set by front panel controls.

Overvoltage Sense

Uses the overvoltage sense line from the pods to set an overvoltage flag. This flag interrupts the CPU with the IRQ2 line, and causes a message "WARNING, INPUT VOLTAGE EXCEEDED" to be displayed. The attenuator is also opened up so the preamplifier is not damaged. When the voltage returns within limits, the CPU will send out a clear overvoltage flag signal through U29 which resets the overvoltage sense circuit.

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SRD Bias

Supplies approximately ±4 volts to forward bias the step recovery diode.

Probe ID

The CPU determines what type of probe is installed in each channel by reading LD0-3 lines. When no probe has been installed, PD0-3 will indicate a HP 54002A pd is used, because these lines are pulled high by passive pullup resistors.

	PD0	PD1	PD2
54001A	L	H	H
54002A	H	H	H
54003A	H	L	H

Board Type

When board type is requested, this board will respond with nine on the LD0-3 lines. This board number nine is produced as follows. U29 will enable U31 and disable U32, overvoltage sense. LD1 and LD2 are pulled low through U31. The output of U32 goes to its high impedance state. Passive pullup resistors on the I/O board will ensure that LD0 and LD3 will be pulled high. LD0 is the least significant bit, so the board number nine is read by the CPU.

Function decoder

Decodes R/LW, A1 and A15 to enable various functions on this board: board type U31, clear over voltage flag, data strobe and data shift.

Shift Registers

Decodes data strobe, data shift and serial data to enable various attenuator ranges, trigger enable, and trigger slope. Also outputs eleven digital lines to the trigger level DAC, and eleven digital lines to the DC offset DAC.

Slot Decode

U30 is a 4 bit comparator which compares slot address lines A19-A22 with slot ID codes ID0-ID3. When the board is addressed, both codes will be equal; U30 pin 6 will output a pulse to the D latch.

D Latch

When this board is addressed, the D latch enables function decoder U29 and part of U32. This way serial data from the CPU will pass to the shift registers. The D latch also sends out LDTACK over the SIB.

Table 6B-9. Sampler Assembly Mnemonics

MNEMONICS	DEFINITION
A1,15	SIB Address lines 1 and 15
D0-10	SIB Data Lines 0-10
IDO-3	Board ID Lines 0-3
LIRQ2	Low Interrupt Request Line 2
LDS	Low Data Strobe
LDTACK	Low Data Acknowledge
LSB	Least Significant Bit
SIB	System Interface Bus

Table 6B-10. Attenuator Control Word

With HP 54002A	U13 pin 6	U2 pin 6	U11 pin 6	U10 pin 6
10 mV	H	H	H	H
20 mV	H	H	H	L
50 mV	H	H	L	H
100 mV	H	L	H	H
200 mV	H	L	H	L
500 mV	H	L	L	H
1 V	H	L	L	L

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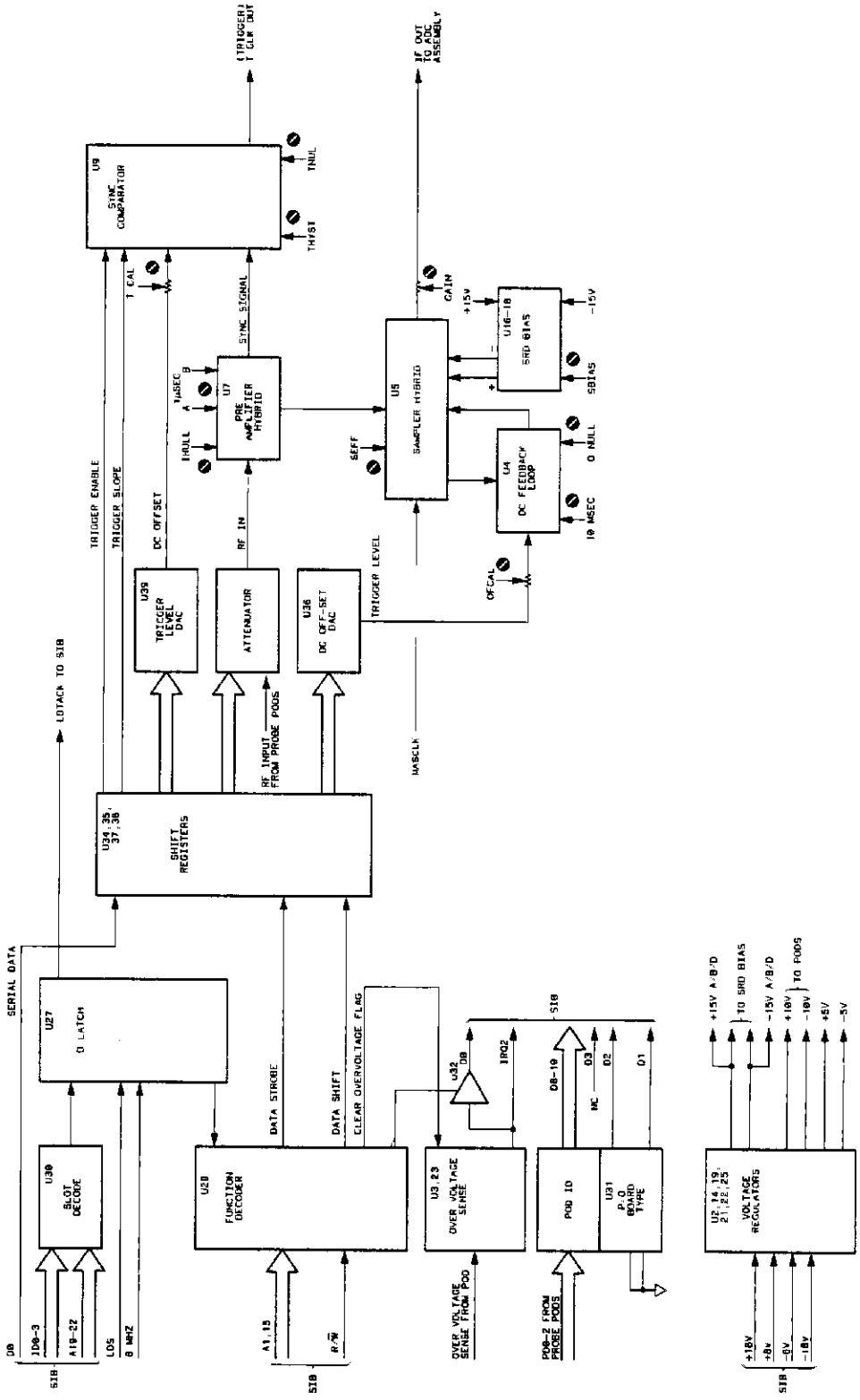


Figure 6B-8. Sampler Assembly Block Diagram.

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6B-11. ADC ASSEMBLY

Introduction

Refer to figure 6B-9. The main purpose of the ADC board is to convert incoming IF signals from a sampler board to digital words. These digital words are stored in memory IC's on the ADC board. At a later time, the CPU retrieves these digital words and places them in the display board memory. The CPU only reads information from the ADC board, it never writes to it. An acquisition cycle starts when the CPU tells the timebase board to enable the ADC board to start storing data, and to enable the trigger board to search for a trigger point. After trigger occurs, the ADC board will stop storing data. The sampler board continues to send data to the ADC board and the ADC's continue to convert analog information to digital words. These digital words will be lost data points. When the next acquisition cycle starts, new digital words will be stored in memory. Many acquisition cycles may occur before the waveform is completely reconstructed.

Buffer Amplifier

Incoming IF from the sampler board is applied to the input of the buffer amplifier. This amplifier has a closed loop gain of 10. The buffer will only allow a ±300 mV signal to the ADC's input.

A to D Converter

There are two A to D converters (ADC). The incoming analog signal is applied to both ADC's. One ADC converts the positive portion of the waveform referenced to +1.25 V, the other ADC converts the negative portion, referenced to -1.25 V. Each ADC converts its portion of the signal to a 7-bit digital word, 6 bits for data and a seventh bit for overrange. Each bit of the 7-bit word is tied to the corresponding bit from the other ADC. Both ADC's are clocked at the 40 MHz clock rate.

High Speed Data Latch

The ADCs are clocked at a 25 ns rate, but data from either ADC may be valid for less then 9 ns. Fast data latches are used to capture information during this narrow time window. The delay between the ADC clock and the latch clock is precisely set by a delay line.

Level Shifters

Converts incoming ECL data levels to TTL levels. ECL is used to assure high speed circuit operation while TTL is used for less expensive circuit configurations.

Fast Data latches

Each data latch is an 8-bit demultiplexer whose output is an 8-bit digital word. Using four latches gives you a 32-bit digital word which is written into memory as two 16-bit words by WE1 and WE2. The data latches are clocked by PCLK1-4. The PCLK1-4 clocks are 90 degrees apart in phase.

Data Storage

There are eight memory IC's with separate data in and data out lines. Each memory IC has 4 bit data lines and 8-bit address lines. Each fast data latch outputs an 8 bit digital word to a pair of memories. Because of phase differences between PCLK1-4, each 8-bit portion of the total 32-bit digital word appears on the data bus at different times. The memory IC's use WE1 and WE2 to allow for timing differences.

High Speed Timing

Combines various inputs from the Timebase board to keep the ADC board timing correct. These inputs are: MASCLK, SMCLK1, SMCLK2, GATE 1. The outputs are: WE1, WE2, PCLK1-4, ADDRESS CLOCK.

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Address Counter

An 8-bit counter that is clocked by ADRS CLK. The purpose of the address counter is to generate sequential 8-bit binary values as a write address for the acquisition RAM during data acquisition. When GATE1 goes high and ADRS CLK begins clocking, the address counter begins incrementing. Note that the actual state of the address counter is indeterminate at the beginning of the acquisition cycle. The counter is never cleared, loaded, or read by the CPU. The address counter will remain pointing to the last location in the sample memory, where the acquisition cycle stopped. The eight outputs of the address counter are placed on the D inputs of the 8-bit write address latch. The address latch is also clocked by ADRS CLK and provides the critical timing alignment of the RAM address bus to the LWE1 and LWE2 lines. The 8 outputs of the address counter are also applied to the address adder.

8 Bit Adder

An 8 bit adder which adds the write memory address to the SIB address lines A3-10. The result is called the read memory address. The CPU will start reading data from this memory address. After the data acquisition cycle is over, the data acquisition firmware will determine the number of data points to be read from the sample memory, and the locaton of these points relative to the last stored data point. The relative read address is supplied to the adder by the CPU over the SIB. The digitized sample data can then be placed on the 8-bit data buffer so that it can be read over the SIB.

Write Address Latch

Enabled by RDENBL during a local ADC board write cycle and places a write address on the local address bus.

3 State Buffer

Enabled by LRDENBL during a read cycle and places a read address on the local address bus.

Slot Decode

U28 is a 4-bit comparator which compares slot address lines A19-A22 with slot ID codes ID0-ID3. When this board is addressed, both codes will be equal and U28 pin 6 will output a pulse to the D latch.

D Latch

This part has three outputs: LRDENBL to enable function decoder U40 and read address latch during read cycles; RDENBL to enable the 3-state buffer during write cycles; and LDTACK which is sent over the SIB.

Board Type

When the microprocessor asks for board type, this board will respond with seven over the D0-D3 lines. Through U42, D0-D2 are pulled high to 5 volts and D3 is pulled low through pull down resistors. D0 is the LSB so adding D0-D2 will give seven.

Table 6B-11. ADC Assembly Mnemonics.

MNEMONICS	DEFINITION	Mnemonic	Definition
A19-22	SIB Address lines 19 to 22	PCLK 1-4	Phase Clocks 1 to 4
D0-7	SIB Data Lines 0-7	RDENBL	Read Enable
IDO-3	Board ID Lines 0-3	SIB	System Interface Bus
LATCHCLK	Latch Clock	SMCLK1	Sample Memory Clock 1
LDTACK	Low Data Acknowledge	SMCLK2	Sample Memory Clock 2
LD0-7	Local Data Lines 0-7	WE1	Write Enable 1
LRDENBL	Low Read Enable	WE2	Write Enable 2

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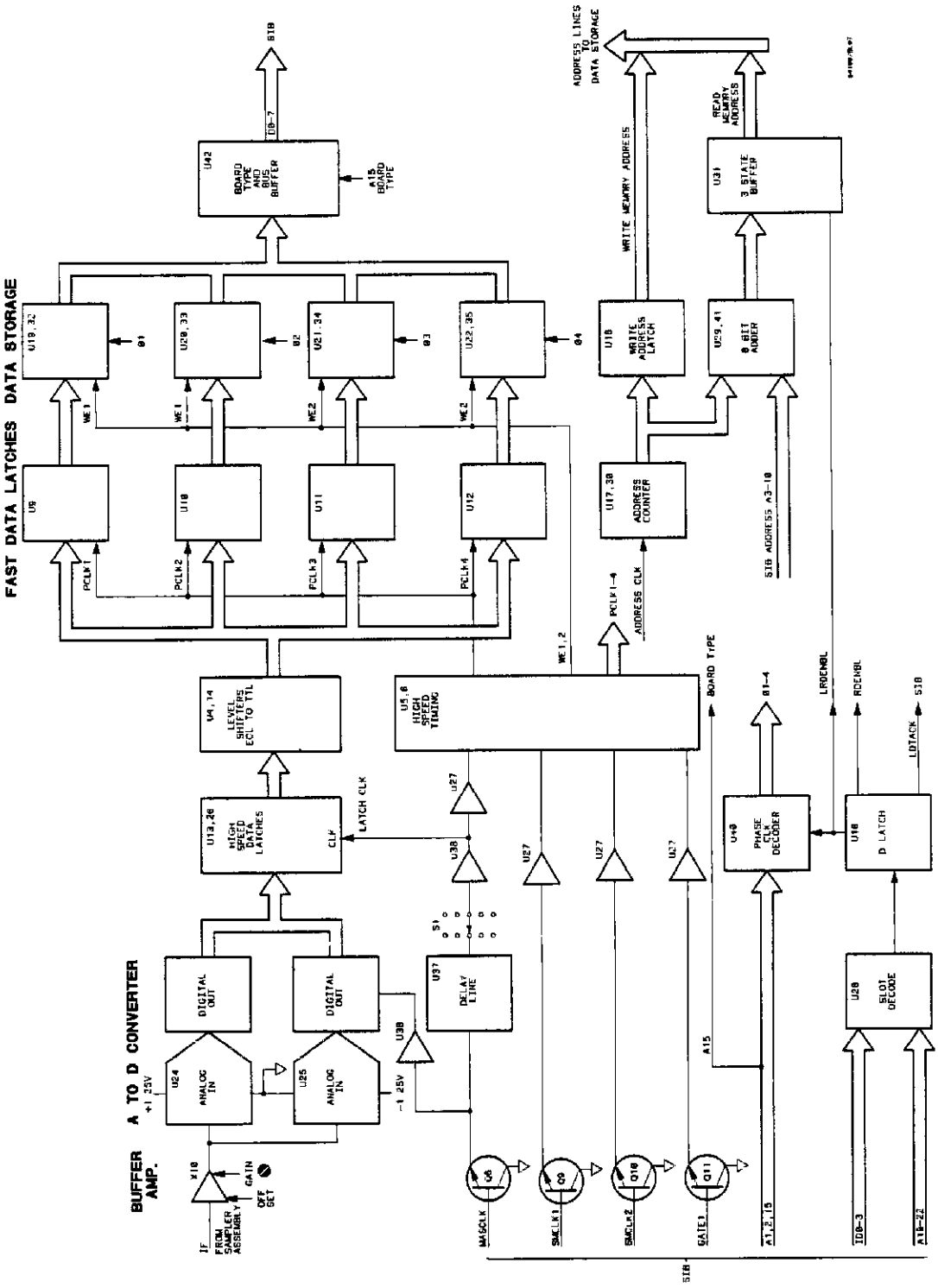


Figure 6B-9. ADC Block Diagram.

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6B-12. Trigger Assembly

Introduction

Refer to figure 6B-10. The Trigger board establishes the trigger point for an acquisition cycle, and generates fine interpolator data. Fine interpolator data establishes timing between data points from the acquisition boards and trigger input. This way the waveform can be reconstructed on the display.

Trigger Level DAC

Converts eleven digital input lines to a dc level. This dc level is called trigger level threshold.

Sync Comparator

When the sync signal crosses over the trigger level threshold, pulse transitions will occur. These pulse transitions correspond to the sync signal and polarity switch inside the sync hybrid. When this channel is enabled, TCLK out pulses will occur.

Trigger Flip-Flop

It logically ORs three input lines to produce one TCLK signal. When the front panel is set to auto trigger mode, the invert signal will force TCLK pulses to occur if the OR gate does not produce a TCLK signal. Fast trigger FF generates HTRIG pulses on the first TCLK edge after the end of holdoff.

Slow Trigger Flip-Flop

A trigger enable signal enables the slow trigger flip-flop, U11. U11 will now produce an ATRIG pulse after it receives the next HTRIG pulse.

Fine Interpolator

More precisely locates the time position of each data point relative to ATRIG by measuring the time from ATRIG to the next MASCLK.

Fine Interpolator Counter

A ripple counter which outputs fine interpolator data to the SIB for the microprocessor to read.

Holdoff oscillator

Produces a crystal controlled 100 MHz sine wave for the holdoff by time sequence.

Holdoff Counter

Counts sine wave pulses for time holdoff, or TCLK transitions for events holdoff.

Slot Decode

U53 is a four-bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When this board is addressed, the two will be equal. U53 pin 6 will output a pulse to the D Latch.

D Latch

When this board is addressed, the D latch will enable function decoder, U54. The D latch also sends out LDTACK over the SIB.

Function Decoder

Decodes address lines A1 and A15 to enable status register with RESTAT and to enable board type with RENTYPE. Function decoder also outputs control information to the data register.

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Synchronization

Synchronizes ATRIG to MASCLK to produce STRIG.

Data Registers

Decodes control information into several outputs. These are: 11 digital lines to the trigger level DAC, trigger enable and trigger polarity to U1, and invert signal to U9.

Board Type

When board type is requested by the microprocessor, this board will respond with eleven over the LDO-3 lines. LD0, 1, and 3 will be pulled high through U59. LD2 will be pulled low through U59. LD0 is the LSB so adding LD0, 1, and 3 results in eleven.

Probe ID

The CPU determines what type of probe is installed in each channel by reading the LD0-2 lines during the power up sequence. When no probe has been installed, PD0-2 will indicate a 54002A is used because these lines are pulled high by passive pullup resistors.

	PD0	PD1	PD2
54001A	L	H	H
54002A	H	H	H
54003A	H	L	H

Table 6B-12. Trigger Assembly Mnemonics.

MNEMONICS	DEFINITION
A19-22	SIB Address lines 19-22
ATRIG	Asychronous Trigger
D0-15	SIB Data Lines 0-15
IDO-3	Board ID Lines 0-3
FI0-15	Fine Interpolator Data lines 0-15
HTRIG	Hysteresis Trigger
LDTACK	Low Data Acknowledge
LD0-7	Local Data Lines 0-7
MASCLK	Master Clock
OV	Over Voltage
RENSTAT	Read Enable Status Resister
RENTYPE	Read Enable Board Type
SIB	System Interface Bus
STRIG	Sychronous Trigger
TRIGEN	Trigger Enable

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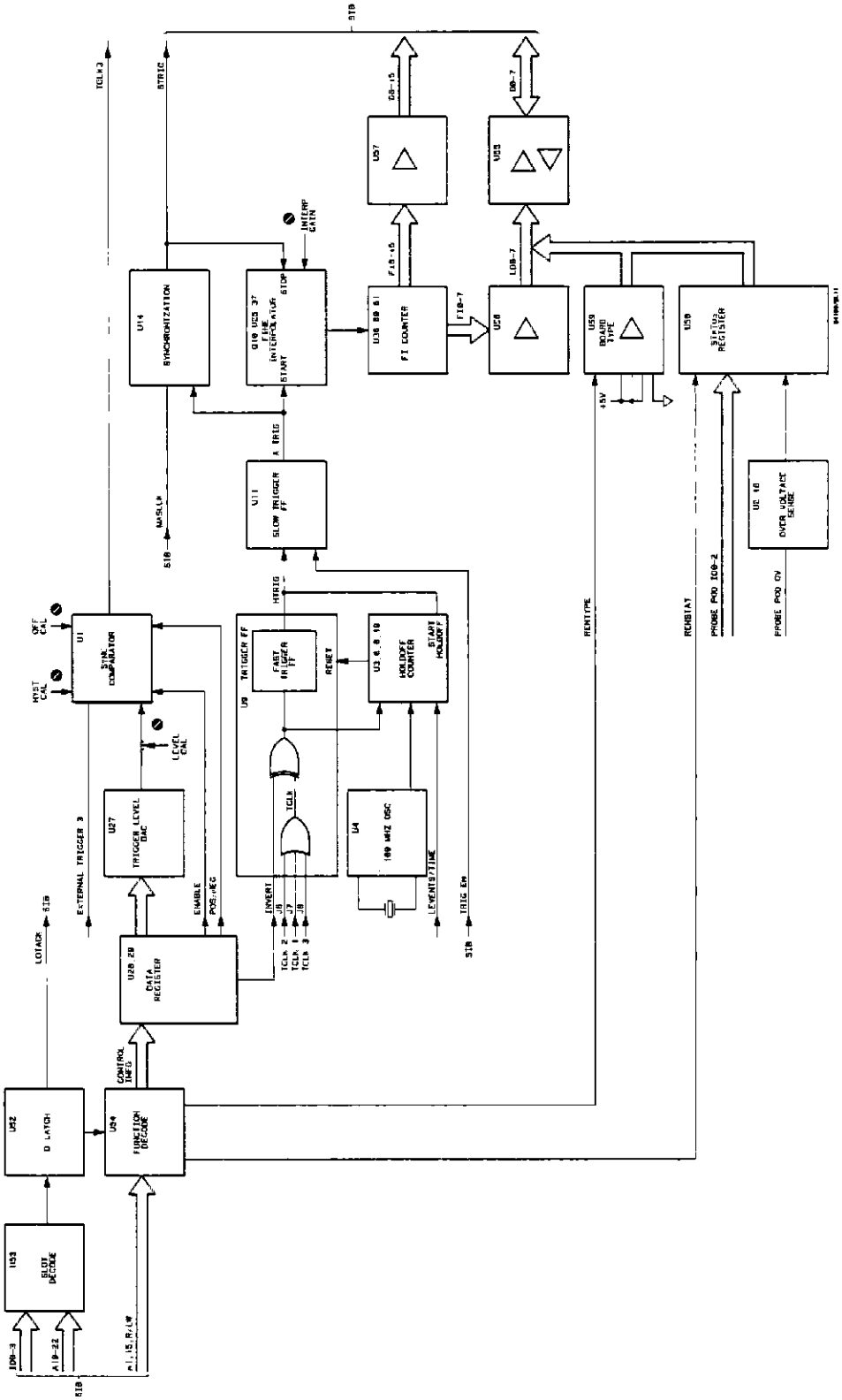


Figure 6B-10. Trigger Assembly Block Diagram.

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6B-13. Trigger Qualifier Assembly

Introduction

Refer to figure 6B-11. This board provides an additional external trigger input along with additional trigger qualifications.

Trigger Level DAC

Converts eleven digital input lines from the shift registers to a dc level. This dc level is called trigger level threshold.

Sync Comparator

When the sync signal crosses the trigger level threshold, pulse transitions will occur. The pulse transitions correspond to the sync signal and polarity switch inside the sync hybrid. When external trig 4 is enabled, TCLK 4 pulses will occur.

Sync Multiplexer Hybrid

The E1-4 lines select which TCLK1-4 signals to use as a trigger signal The selected combination TCLK becomes TCLK OUT and is sent to the trigger flip flop on the trigger board. All four TCLK signals are also sent through buffers and then outputted to U6 and U17.

TCLK Select

Decodes mode data into enable signals E1-4 for multiplexer hybrid and U17. These enable signals select one or more buffered TCLK signals to form TCLK prime.

QCLK Select

Decodes mode data into enable signals S1-4 for U6. These enable signals select one or more buffered TCLKs to form QCLK.

U6 and U17

These are OR/AND gates which each supplies two signals to the asynchronous logic block. QCLK is the signal for which some condition must become true before TCLK' is processed by asynchronous logic.

Count Mode

45-bit holding register for controlling the 29 bit counter setup and asynchronous logic set up.

Startable Oscillator

100 MHz oscillator used for time measurements.

29 Bit Counter

100 MHz counter used for counting time or events for various trigger modes. For short counts, the microprocessor may use software to disable some portions of the 29-bit counter not being used.

Slot Decode

U49 is a 4-bit comparator which compares slot address lines A19-22 with slot ID codes ID0-3. When this board is addressed, the two codes will be equal. U49 pin 6 will output a logic true pulse to the D Latch.

D Latch

When this board is addressed, the D latch enables function decoder U47. The D Latch also sends out LDTACK over the SIB.

Function Decode

Decodes R/LW, A1 and A15 to enable various functions on this board. These are: LRENTYPE for board type, LRENSTAT for board status, control information for shift registers

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Overvoltage Sense

Uses the overvoltage sense line from the probe pod to set an overvoltage flag. This flag interrupts the microprocessor over the IRQ2 line and causes a message "WARNING, INPUT VOLTAGE EXCEEDED" to be displayed. When the voltage returns within limits, the microprocessor sends a clear overvoltage signal through U47 which resets the overvoltage sense circuit.

Board Type

When board type is requested, this board will respond with fourteen over the LD0-3 lines. This board number fourteen is produced as follows; LRENTYPE will disable U51B from driving LD0-3 lines, and enable U51A to pull the LD4-7 lines low through U51A. LD1, 2, and 3 will be pulled high by pullup resistors in RP12. LRENTYPE also will enable U46 so LD0 will be pulled low through U46. LD0 is the least significant bit so adding LD1, 2, and 3 will give fourteen.

Shift Registers

Outputs eleven digital lines to trigger level DAC, also outputs trigger enable and trigger slope to sync comparator.

Mode Enable

Decodes LD0 and LD1 to form MODE DATA, MODE SHCLKA & B

Probe ID

The microprocessor determines what type of probe is installed in each channel by reading the LD0-2 lines during the power up sequence. When no probe has been installed, PD0-2 will indicate a 54002A is used because these lines are pulled high by passive pullup resistors.

	PD0	PD1	PD2
54001A	L	H	H
54002A	H	H	H
54003A	H	L	H

Table 6B-13. Trigger Qualifier Assembly Mnemonics.

MNEMONICS	DEFINITION
A19-22	SIB Address Lines 19-22
D0-7	SIB Data Lines 0-7
IDO-3	Board ID Lines 0-3
LDTACK	Low Data Acknowledge
LD0-7	Local Data Lines 0-7
LRENTYPE	Low Read Enable Board Type
QCLK	Qualified Trigger Clock
TCLK	Trigger Clock
SIB	System Interface Bus

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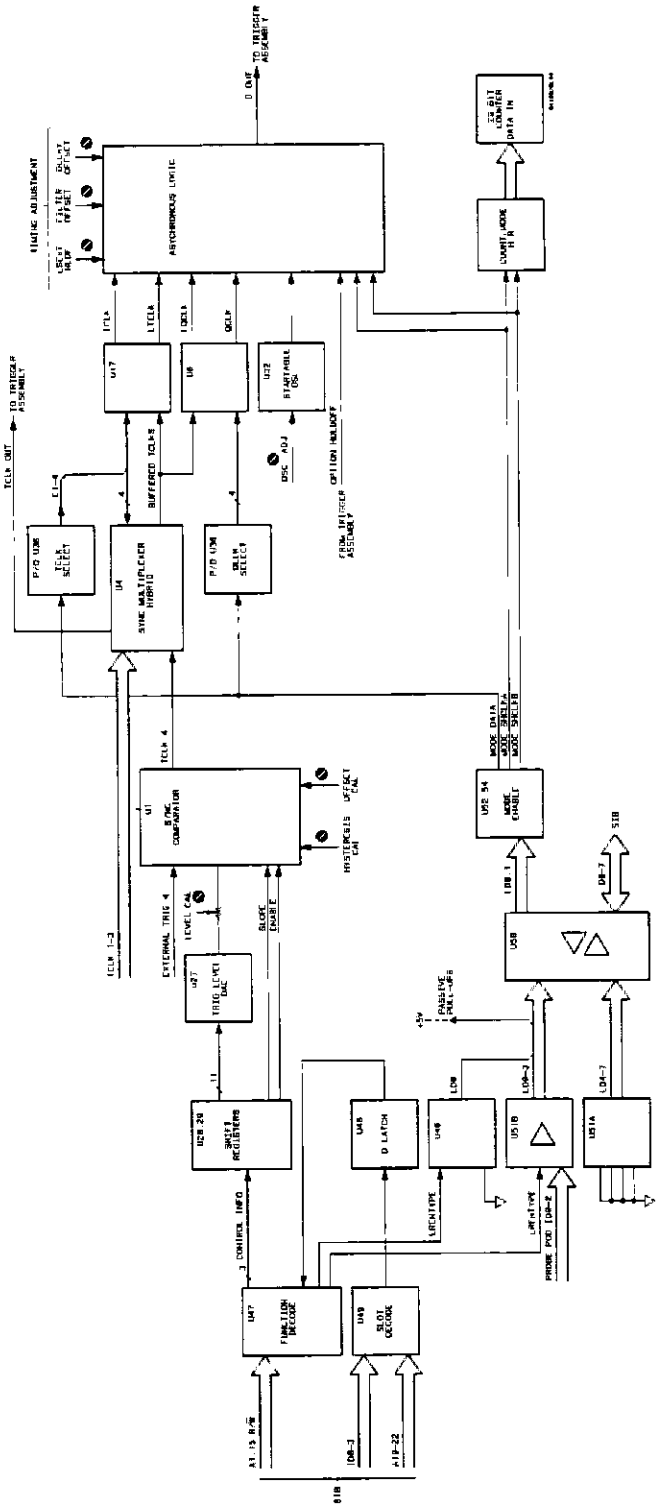


Figure 6B-11. Trigger Qualifier Assembly Block Diagram

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6B-14. POWER SUPPLIES

Primary Power Supply

The primary board rectifies and filters the input ac voltage. When the voltage select switch is in the 230 V position, the ac is bridge rectified and filtered to yield approximately 300 V dc. The input voltage is doubled in the 115 V position to yield the same dc voltage. The primary board has surge protection circuitry that protects against ac line voltage transients and current surges. Over voltage crowbar devices trip the circuit breaker for sustained input over-voltage conditions. The pulse width modulator (PWM) circuitry is powered by a bleeder resistor on one of the bulk storage capacitors. The main EMI (electromagnetic interference) filter is located in a dc current path to reduce component size and to increase effectiveness of the filter. This board also generates a fast rising 14.7 V supply which is used by the pulse width modulator circuitry in the digital and analog power supplies.

Digital Power Supply

The digital power supply is a dc-to-dc converter which converts 300 V dc to +5 V and -5.2 V dc. It also generates the digital gound (DGND) which is used throughout the system.

PULSE WIDTH MODULATOR (PWM) Is used to achieve voltage and current regulation by changing the PWM's turn-on time. It has an operating frequency of 68 kHz.

POWER STAGE Performs the actual conversion of 300 V dc to +5 V and -5.2 V dc. Digital and primary ground planes are kept isolated through transformer T2.

OPTICAL ISOLATORS Isolates the primary and digital ground planes. Voltage and current feedback control is sent through U2 to control the duty cycle of the PWM. Power supply shutdown is sent through U3.

LOOP CONTROL AND SUPERVISORY When excessive output voltage is detected, circuitry sets a latch in the PWM which can only be reset by cycling the on-off switch. This voltage shutdown can also be activated by the power supply fault line coming from the analog power supply. Circuitry also senses the current and activates foldback current limiting for excessive current loading.

Analog Power Supply

The analog power supply is a dc-to-dc converter which converts 300 V dc to +18 V, +8 V, -8 V, and -18 V dc.

PULSE WIDTH MODULATOR (PWM) Is used to achieve voltage and current regulation by changing the PWM's turn on time. It has an operating frequency of 68 kHz.

POWER STAGE Performs the actual conversion of 300 V dc to +18 V, +8 V, and -18 V dc. It also contains a fan drive output which increases the fan speed with the instrument's ambient temperature. Analog and primary ground planes are kept isolated through transformer T2.

OPTICAL ISOLATORS Isolates the primary and analog ground planes. Voltage and current feedback control is sent through U2 to control the duty cycle of the PWM. Power supply shutdown is sent through U3.

LOOP CONTROL AND SUPERVISORY When excessive over-voltage is detected, circuitry sets a latch in the PWM which can only be reset by cycling either the on-off switch or circuit breaker to the off position for 60 seconds. A fan fault will also activate this power supply shutdown. A power supply fault line also goes to the digital supply to activate its shutdown circuitry. +18 V is regulated and the other outputs are semi-regulated outputs which follow the +18 V. Each output is current limited. The -8 V output has foldback current limiting.

Fan Drive The fan is powered by circuitry on this board. A temperature sensing circuit controls the fan speed. In addition, the fan is monitored for faults. If the fan should fail, the analog power supply will shut down both secondary supplies over the power supply fault lines.

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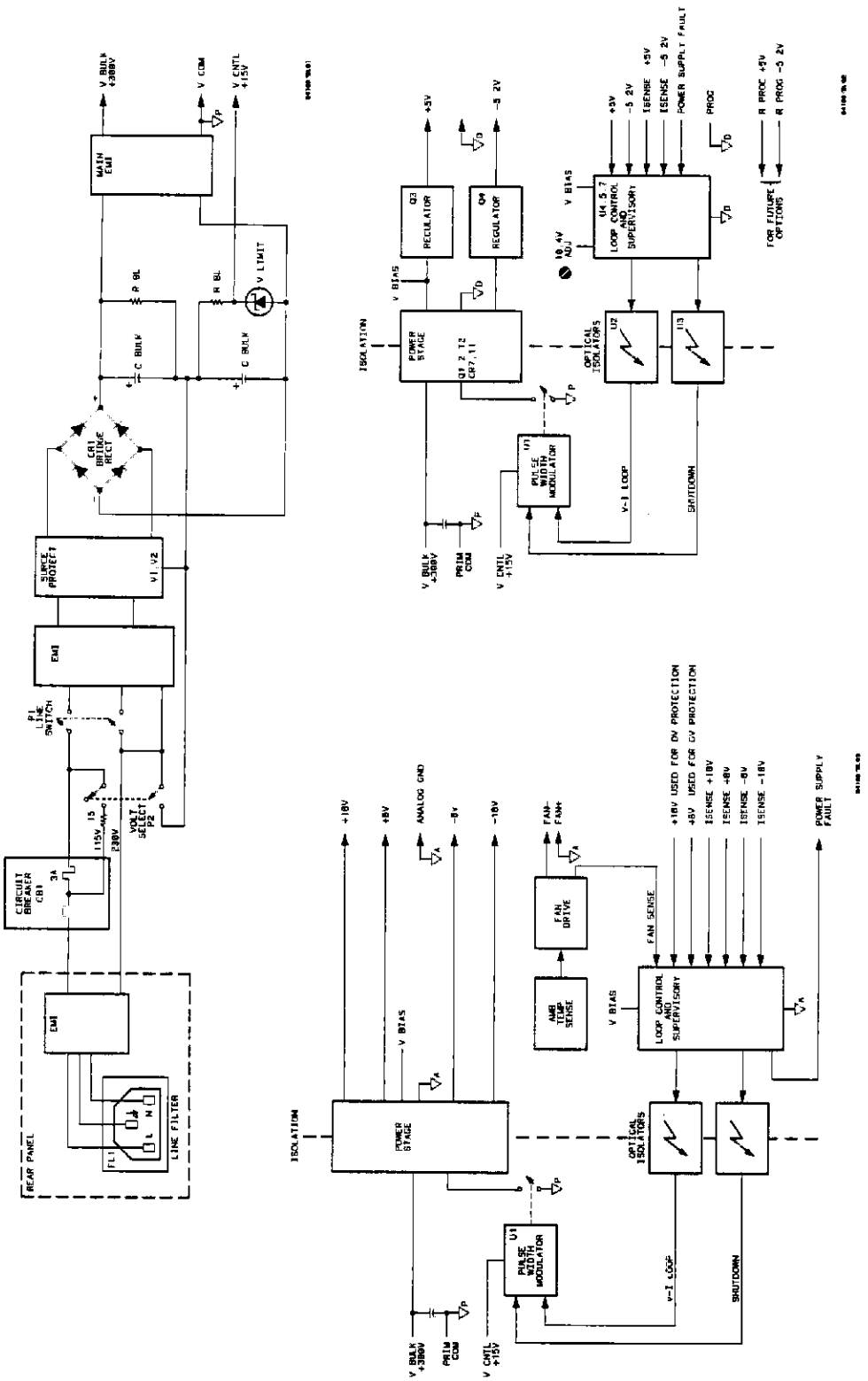


Figure 6B-12. Power Supply Assembly Block Diagram.

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SECTION 6C

SERVICE MENU KEYS

6C-1 INTRODUCTION

This section describes the Service menus and keys that are available to service personnel for calibration, troubleshooting and CRT alignment. A basic understanding of them will be helpful in troubleshooting failures; however, Self-Test (section 6E) and Troubleshooting (section 6D) are covered later in this manual.

6C-2. UTILITY MENUS

The Calibration and Test menu can be accessed by pressing the Utility key located on the second level of the Function menu. Once the Utility key is selected, four subkeys will be displayed: Cal Menu, Test Menu, CRT Setup and HP-IB Menu. These keys allow entry into routines designed to aid in calibrating, troubleshooting, CRT alignment, and setting up the instrument's HP-IB interface.

6C-3. SOFTWARE CALIBRATION

6C-4. Introduction

WfmSave	WfmMath	Measure	Plot	Print	Probes	Utility	More

Cal Menu
Test Menu
Crt Setup
HP-IB Menu

When the Utility function menu is selected four selections are available: Cal menu, Test menu, CRT Setup menu, and HP-IB Menu. The Cal menu is the only menu that will be discussed in this section. Refer to figure 6C-1.

The Cal menu function allows any differences in propagation delay between signal paths to be nulled out in the HP 54100A/D software. This is important so that time-difference measurement results accurately reflect time referenced to the probe tips, or the points where the input coaxial cables are connected to the circuit under test.

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In order to obtain the proper cal for a particular system configuration it is necessary to adjust each channel's sensitivity, offset and trigger level as well as the external trigger level(s) to the values you intend to use. This will establish each input to the configuration that will be used in the actual measurement.

Cal factors are kept as part of the SAVE/RECALL setup and different sets of factors may be kept with each front panel setup. When the instrument is powered down, these factors will be maintained in non-volatile memory.

The fastest available edge source should be used (<1 ns transition time is desirable); however, a signal of the same general characteristics as the signal to be measured is a reasonable alternative. For each cal step the inputs should be connected to the calibration source as closely to one another as possible. BNC Tees and probe adapters should be used for this purpose.

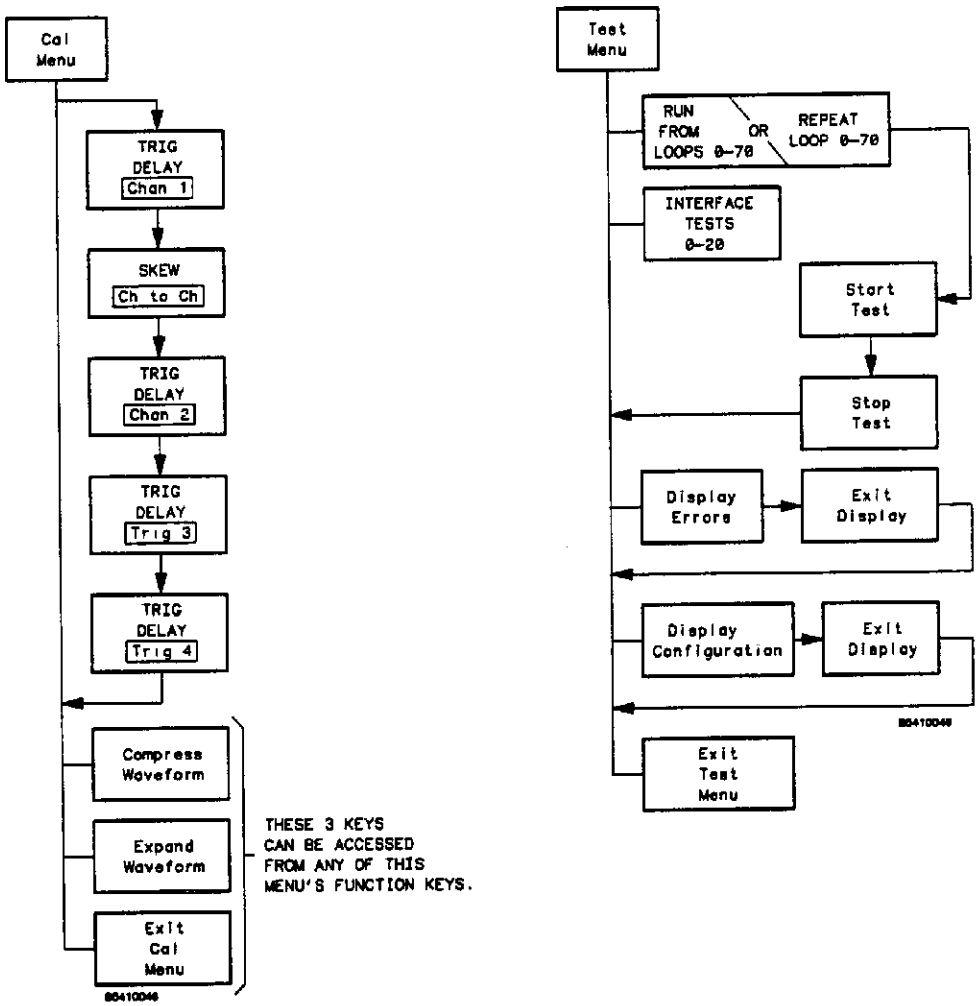


Figure 6C-1. Utility Menus

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6C-5. Calibration Procedure

There are two Cal signal outputs on the rear panel. Only one cal source should be used for the Cal Menu adjustment exercise because the two cal signals are separately buffered and the time differential between the two outputs is not characterized.

1. Connect a BNC Tee to one of the cal signal outputs on the rear of the instrument. Connect two equal length 50 Ω cables to the BNC Tee. Connect these two cables to the Chan 1 and Chan 2 inputs. Next, select the **Axes** graticule.

NOTE

Any suitable signal source can be used for this calibration. If probes are to be used to make the actual measurement, then that probe configuration should be used for the calibration.

2. For this exercise, press ***AUTO-SCALE***, then set ***OFFSET*** and ***TRIG LEVEL*** to equal values for Chan 1 and 2. Move the signal input from Chan 2 to Trig 3, then to Trig 4 (HP 54100D ONLY) and set the ***TRIG LEVEL*** Trig Src 3 and Trig Src 4 (HP 54100D ONLY) as close as possible to the TRIG LEVEL used for Chan 1 and 2. Now move the input cable back to Chan 2. Set ***Trig Src*** back to Chan 1.

3. Press the ***Cal menu*** function key and follow the instructions on the CRT (but don't AUTO-SCALE again), press the ***TRIG DELAY-Chan 1*** function key, i.e., the top key on the function menu. As the key is pressed TRIG DELAY will intensify and a single signal will be presented on the display.

4. Press the ***Expand Waveform*** function key several times until the waveform is expanded and approximates figure 6C-2. With the Entry Devices, adjust the position of the signal on the X-axis so that it intersects the crossing of the graticule at center screen. The value of Chan 1 Trigger Delay is highlighted in inverse video at the top of the display.

5. Press ***TRIG DELAY-Chan 1*** key (top function key) and the label will change to ***SKEW Ch to Ch***, also the Chan 1 and 2 signals are in the split screen format. The Chan 1 signal is in the upper half of the display and Chan 2 is in the lower half The Chan 1 signal should be positioned so that it intersects the graticule crossing, this is the result of the previous Chan 1 TRIG DELAY adjustment. Adjust the display with the Expand Waveform key until it approximates figure 6C-3. With the Entry Devices adjust the Chan 2 waveform on the X axis so that it intersects the graticule crossing at center screen. When this adjustment is made it is nulling the difference in signal acquisition times from Chan 1 to Chan 2. Chan to Chan skew time is highlighted in inverse video at the top of the display.

6. Press ***SKEW Ch to Ch*** (top function key) and the label for this key will change to ***TRIG DELAY-Chan 2***. There will also be a single signal on the display. Expand the waveform with the Expand Waveform key until it approximates figure 6C-2. Use the Entry Devices and position the displayed signal on the X axis so that it intersects the graticule crossing at the center of the display. The Ch 2 Trigger Delay will be highlighted in inverse video at the top of the display.

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7. Connect the cable that has been attached to Chan 2 to Trig 3 input. Press ***TRIG DELAY-Chan 2*** (top function key) and the label will change to ***TRIG DELAY-Trig 3***. Expand the waveform using the Expand Waveform key until it approximates figure 6C-2. Adjust the Entry Devices and move the signal on the X axis so that it intersects the graticule at the center crossing. The value of Trig 3 Delay will be highlighted in inverse video at the top of the display.

8. If an HP 54100A is being calibrated, the calibration is completed. The HP 54100D, however, has an additional external trigger input and to null the difference in signal acquisition time from Trig 4 input to the other inputs requires one further step. Move the input from Trig 3 to Trig 4 input and press ***TRIG DELAY-Trig 3*** (top function key). The label will change to ***TRIG DELAY-Trig 4***, and there will be a single signal on screen. Press the ***Expand Waveform*** key until the display approximates figure 6C-2. Adjust the Entry Devices and move the signal on the X axis so it intersects the graticule at the center crossing.

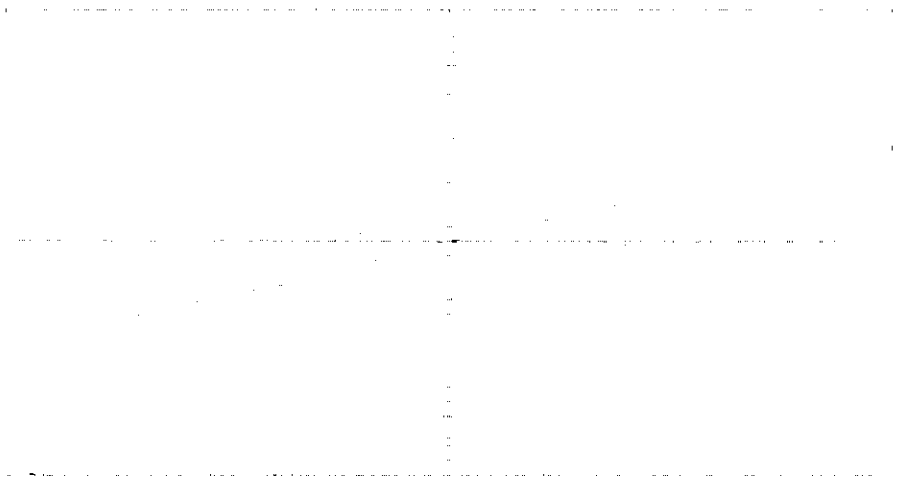


Figure 6C-2. Trigger Delay

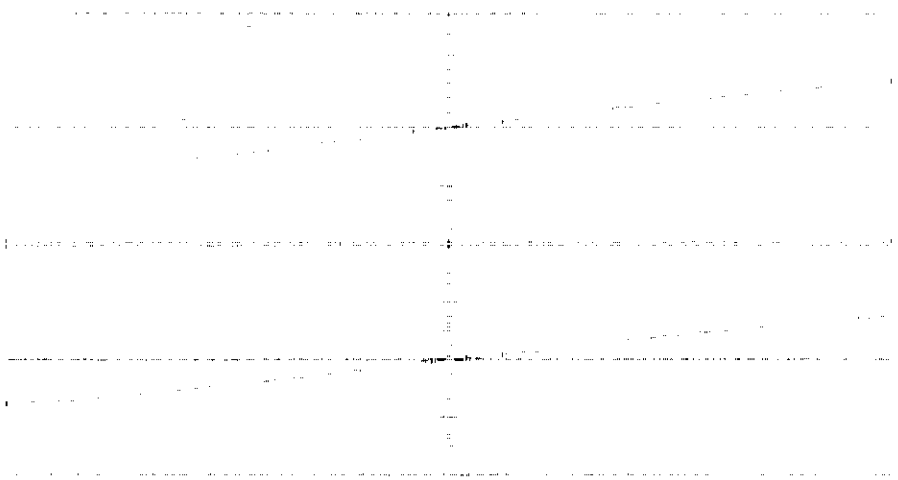


Figure 6C-3. Chan to Chan Skew

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6C-6. TEST MENU

Five keys appear when the Test Menu is selected. These keys allow the user to access and run internal diagnostic tests and view the results. In addition, the position of each of the printed circuit boards can be read and displayed.

6C-7. Display Configuration Key

The HP 54100A/D motherboard has ten slots and will accept any of the printed circuit boards at any location within the card cage. When the Display Configuration key is pressed, the resulting display shows the location of each of the PC boards.

The Processor board A3 will not be labeled on the display, but is normally loaded into Slot 2. The HP 54100A should show boards loaded in Slots 0-8, and the HP 54100D will have an additional board in Slot 9.

NOTE

Although the boards may be loaded into any of the slots and will function, an optimal arrangement does exist. Refer to the label located on the bottom of the top cover. If the I/O board is not in slot 0 and the Display board is not in slot 1, self test loops 5 and 9 will fail.

To return to the Test Menu, press ***Exit Display***

6C-8. Display Errors Key

Pressing this key will display the number of any loops which failed while running one of the following tests:

Power-up self-test
HP-IB commanded self-test
INTERFACE tests

This display shows the current loop or last loop executed, the number of times the loop was executed, and the number of times that it failed. The bottom portion of the display shows all loops that failed starting with the first loop failure.

In addition, some of the loops also use the four "status" indicators (sometimes called "errors"). These are loop dependent status codes of a pass/fail nature for each loop. They indicate counter values, status flags, addresses, etc. that were loaded during the execution of the loop. These indicators can help troubleshoot the unit, and are described in detail in section 6D, troubleshooting. If the test does not use a particular error indicator, the value will be set to -32768.

To return to the Test Menu press ***Exit Display***.

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6C-9. Repeat Loop / Run From Loop Key

The top key will toggle between REPEAT LOOP and RUN FROM LOOP. These keys in conjunction with the START TEST key will execute the internal self-diagnostic routines. All input signals must be disconnected from the instrument for these tests.

NOTE

When the instrument is left in a continuous RUN FROM LOOP mode for a period of time, a failure indication may occur when there is no failure. This is caused by random system noise and occurs less than 1% of the time. Since this is not a QA function it should be disregarded once you have verified it is not a true failure. A true failure only exists if the test is stopped and re-started and the same loop failure re-occurs at a rate greater than 1%.

REPEAT LOOP. Selecting this mode will continuously execute the routine that has been entered with the entry devices (keypad, Knob, or increment/decrement) keys. Pressing ***Start Test*** will start execution and the loop will continuously run until the ***STOP TEST*** key is pressed. Pressing ***DISPLAY ERRORS*** will show how many times the loop was executed and the number of failures that occurred.

RUN FROM LOOP. Selecting this mode will start execution from the loop entered and will proceed to execute all higher numbered loops. Upon reaching the last loop, the cycle will be repeated starting at the entered loop. If any test should fail, the instrument will change from RUN FROM LOOP to REPEAT LOOP and will repeatedly execute the loop that failed. This structure allows the use of signature analysis to detect which loop failed, if any.

NOTE

Some tests will not display the stop softkey on the display. In these cases, the stop key remains on the vertical softkey board, third key down from the top key.

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6C-10. Interface Tests Key

When this key is chosen there are 15 tests for the HP 54100A and 16 tests for the HP 54100D that are not executed at power up, but may be selected by entering the test number with the entry devices. The tests are numbered 0 through 14 for the HP 54100A and 0 through 15 for the HP 54100D. All input signals must be disconnected from the instrument for these tests.

NOTE

Tests 0 through 9, 13 and 14 should be entered only by qualified service personnel and are test loops for creating a repetitive set of signals which are used for signature analysis troubleshooting. ***No useful information is gained from the CRT display when these troubleshooting loops are entered.***

To run test loops 0 through 9, 13 and 14, the test number must be entered with the entry devices. The START TEST key must be pressed. To stop the test loop, the STOP TEST key must be pressed.

Tests 10, 11, 12, and 15 are other self tests that the user can run to give more confidence that the unit is operating properly. Tests 10 and 15 check the trigger level DAC on channels 3 and 4. Test 11 verifies proper operation of the keyboard I/O circuitry. Test 12 is a special non-power up transition reset.

Test numbers 0-9 test the digital interface between the Processor Bus and the board loaded into the slot that corresponds to the test number. If test 0 is selected, the processor will attempt to read the identification code of the board loaded in slot 0. Even though the codes are read, no information is displayed on the CRT. More details on these tests can be found in the troubleshooting section of this manual.

NOTE

Slot 0 corresponds to A1 board and Slot 9 corresponds to the A10 board.

Test 10 checks the trigger level DAC of channel 3. Disconnect any signal inputs to this channel prior to running this test. To run this test, use the same procedure listed above for tests 0 through 9. To determine whether the test passed, press the ***STOP TEST*** key, then press ***DISPLAY ERRORS***. If in the cumulative errors column loop 62 is present, then the test failed. If loop 62 was not present, then the test passed. The loop indicator is only cleared at power up. If this loop fails, refer to section 6D, troubleshooting, for diagnosis. More details on these tests can be found in the troubleshooting section of this manual.

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Test 11 will display a keyboard mockup on the CRT. This test is used to verify that all of the front panel keys and the RPG are working. After selecting Test 11 and pressing Start Test, press each of the front panel keys. The displayed box corresponding to the key being pressed should light. The RPG control will move a cursor around the circle in the lower right corner of the CRT. To exit this test the third key from the top must be pressed for the second time. The first press will light the appropriate box and then the key will be assigned as STOP TEST

Test 12 causes a system reset and actuates the power-up self-test. If the advisory message "Power-up Self-test Failed" should appear on the display, then the failing loops may be found by pressing the Display Errors key in the Test Menu.

Tests 13 and 14 are special DSA setups for testing ADC boards. Before initiating these tests, make sure the ADC to be tested is installed in Slot 9 and connect the output of Sampler 1 to the ADC. More details on these tests can be found in the troubleshooting section of this manual.

Test 15 checks channel 4's trigger level DAC. Disconnect any input to this channel before running this test. To run this test, use the same procedure listed earlier for tests 0 through 9. To determine whether the test passed, press the ***STOP TEST*** key, then press the ***DISPLAY ERRORS*** key. If in the cumulative errors column loop 61 is present, then the test failed. If loop 61 is not present, then the test passed. The loop indicator is only cleared at power up. If this test fails, refer to section 6D, troubleshooting, for diagnosis. More details on these tests can be found in the troubleshooting section of this manual.

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SECTION 6D

TROUBLESHOOTING

6D-1 INTRODUCTION

This Section describes the Self-tests and Troubleshooting routines that service personnel can use to locate failures at the PC board level. A basic understanding of the Service menus and keys will be helpful in troubleshooting failures and is covered specifically in Section 6C.

6D-2. FAILURE INDICATIONS

The HP 54100A/D will indicate failures in one of two ways; 1) no display on the CRT during and after power-up, or 2) "Powerup self-test Failed" displayed on the CRT. When a "no display" failure occurs, refer to Section 6D-X "TROUBLESHOOTING WITH NO DISPLAY" and proceed from there. If the "Power-up self-test Failed" advisory appears, refer to Section 6D-X "INTERNAL DIAGNOSTICS (SELF-TEST)". All input signals must be disconnected from the instrument when running the internal diagnostics tests.

NOTE

Occasionally the "Power-up Self Test Failed" advisory will appear when there is no failure. This is caused by random system noise and occurs less than 1% of the time. Since this is not a QA function it should be disregarded once you have verified it is not a true failure. A true failure only exists if the failure advisory again appears after running the Interface #12 test that follows.

1. Press the ***Utility*** menu selection key.
2. Press the ***Test*** menu key.
3. Press the ***INTERFACE TEST*** key and enter 12 from the keyboard.
4. Press the ***START TEST*** key.

If the "Power-up self-test Failed" advisory **does not** re-appear at the completion of this test, **do not** continue troubleshooting because the instrument **has not** failed. If this advisory does re-appear, refer to Section 6D-3 as previously indicated.

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6D-3. INTERNAL DIAGNOSTICS (SELF-TEST)

The HP 54100A/D has routines resident in firmware that ensures many of the unit's circuits are functioning correctly. The HP 54100A contains 43 routines and the HP 54100D contains 61 routines. All input signals must be disconnected from the instrument for these tests.

The processor upon command or automatically at power-up begins by checking memory and then checks its ability to communicate via the internal bus. Once bus communication is established the processor will exercise and test circuits on other boards beginning with the digital boards.

NOTE

The tests that are executed cannot guarantee that the instrument is performing to its rated specifications. However, they do provide a high degree of confidence that the unit is functioning.

When power is applied to the instrument the self-test is automatically executed. If no failures have occurred, an advisory will be displayed on the CRT approximately 4 seconds later. Some hardware failures will cause the advisory to be delayed by 30 seconds.

The complete group of tests can be executed by any of the following:

1. Apply power to the instrument and the self-test routines are executed automatically.

2. Performing test 12 in the INTERFACE TESTS portion of the Test menu.

3. Entering loop 0 in the RUN FROM LOOP portion of the Test menu. This test will cause the instrument to repeatedly exercise the complete group of tests. If a failure occurs on any of the tests, the instrument will change to REPEAT LOOP and will continue executing only the loop that has failed.

NOTE

Pressing RUN FROM LOOP 0 does not clear the loop failures shown with the DISPLAY ERRORS key All other methods of generating self-test will clear the loop failures from DISPLAY ERRORS and then will add any failures that occurred during the self-test.

4. HP-IB command TEST (TST) will trigger a power-up self-test. If a failure occurs, error number -340 will be placed in the error queue. The error buffer may be read with the ERROR? command. Refer to Section 10 of the *HP 54100A/D Operating and Programming Manual.*

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6D-4. INTERFACE TESTS #0-9

Interface tests 0-9 are special service diagnostic tests, which help determine whether the board interface or slot interface is working correctly. Test 0 corresponds to slot 0, and test 9 corresponds to slot 9.

These tests are different from the loop tests because they do not return a failure code. Instead, they set the instrument up in an infinite loop. This infinite loop continually executes the loop selected until the stop test key is pressed. The selected loop exercises the same circuity repeatedly, so a service technician can probe points in the instrument to determine the faulty board.

To run these tests:

1. Press ***More*** key
2. Press ***Utility*** key
3. Press ***Test menu*** key
4. Press ***Interface Test*** key
5. Enter test number to be exceuted

The points that should be probed are different depending on which board is inserted in the slot to be tested. Table 6D-1 cross references the board test points to waveform numbers 1-5. Refer to Figures 6D-1 through 6D-4 for the correct displayed waveforms.

Table 6D-1. Board Test Point Cross Reference.

Board	Waveform 1	Waveform 2	Waveform 3	Waveform 4	Waveform 5
Trigger Qualifier	TP5	TP4	U46 Pin 3	U45 Pin 6	U48 Pin 8
Trigger	TP28	TP29	U51 Pin 3	U48 Pin 8	U52 Pin 6
ADC	TP12	U28 Pin 6	U39 Pin 1	U39 Pin 9	U16 Pin 6
Sampler	TP3	TP2	U27 Pin 8	U28 Pin 9	U27 Pin 6
Timebase	U35 Pin 6	TP14	U35 Pin 13	U35 Pin 9	U41 Pin 6
I/O	U25 Pin 6	U2 Pin 13	TP7	U16 Pin 9	U9 Pin 8
Display	TP1	None	U26 Pin 8	None	TP14

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6D-5. LOGIC FAMILIES USED

Three different logic families are used in the HP 54100A/D. These include TTL, ECL, and ECL 2. Table 6D-2 indicates where each logic family is used.

TTL ranges from 0 V to 5 V (approximately) and is used on much of the digital circuitry and the slower speed data acquisition circuitry; such as status registers, RAM addressing, etc.

ECL ranges from -.9 V to -1.7 V and is used more often in the data acquisition circuitry where speed is of great importance.

ECL 2 ranges from 0 V to -.8 V and is used on the outputs of many custom IC's.

Because the ECL high and the ECL 2 low share about the same voltage level, a chance exists that a misinterpretation of a logic level could occur. Extra care should be taken when dealing with these levels. Typically offsets are -1.3 V for ECL and -.4 V for ECL 2.

Table 6D-2. Logic families used in the HP 54100A/D

Board	Logic Families Used
CPU	TTL
Display	TTL
I/O	TTL
Timebase	TTL, ECL
Sampler	TTL, ECL, ECL 2
ADC	TTL, ECL
Trigger	TTL, ECL, ECL 2
Trig. Qual.	TTL, ECL, ECL 2

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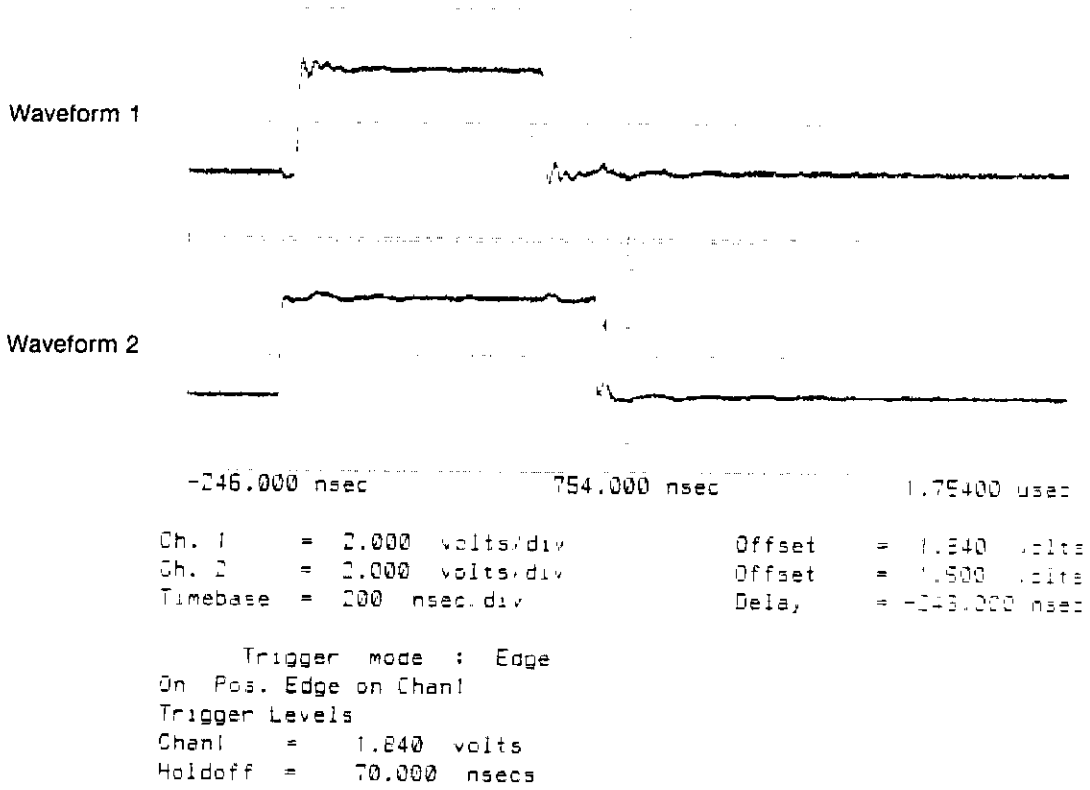


Figure 6D-1. Waveform Numbers 1 and 2.

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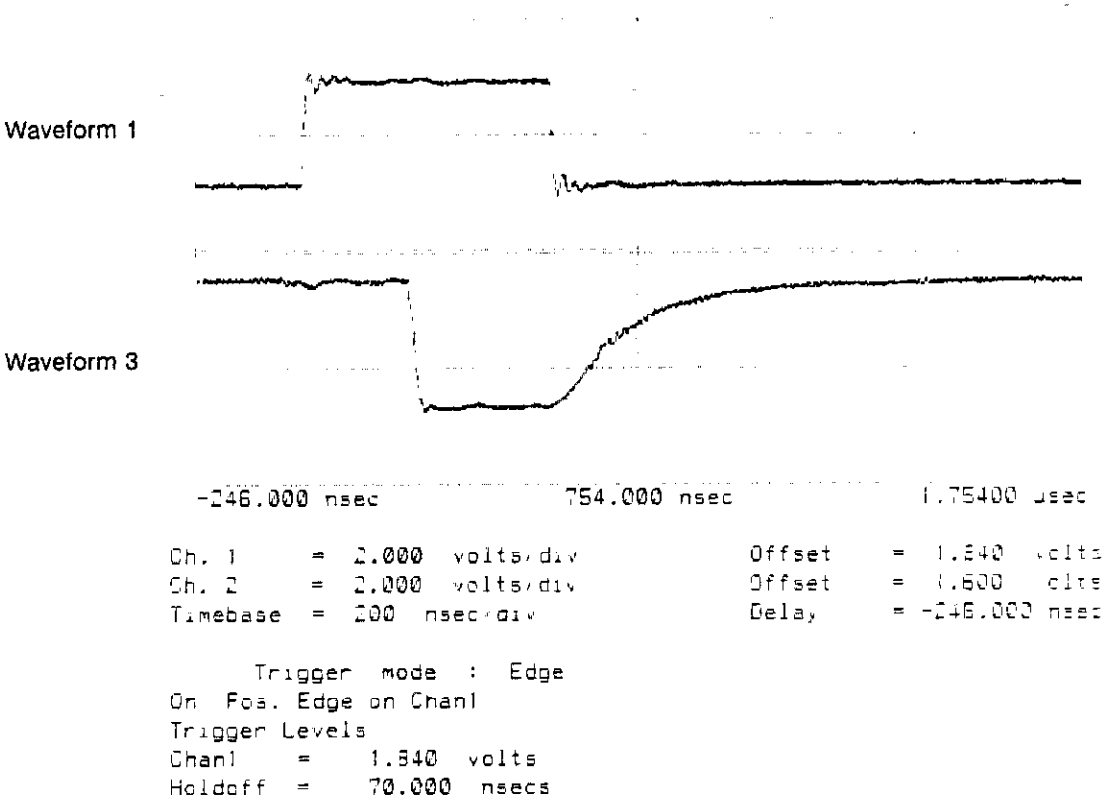


Figure 6D-2. Waveform Numbers 1 and 3.

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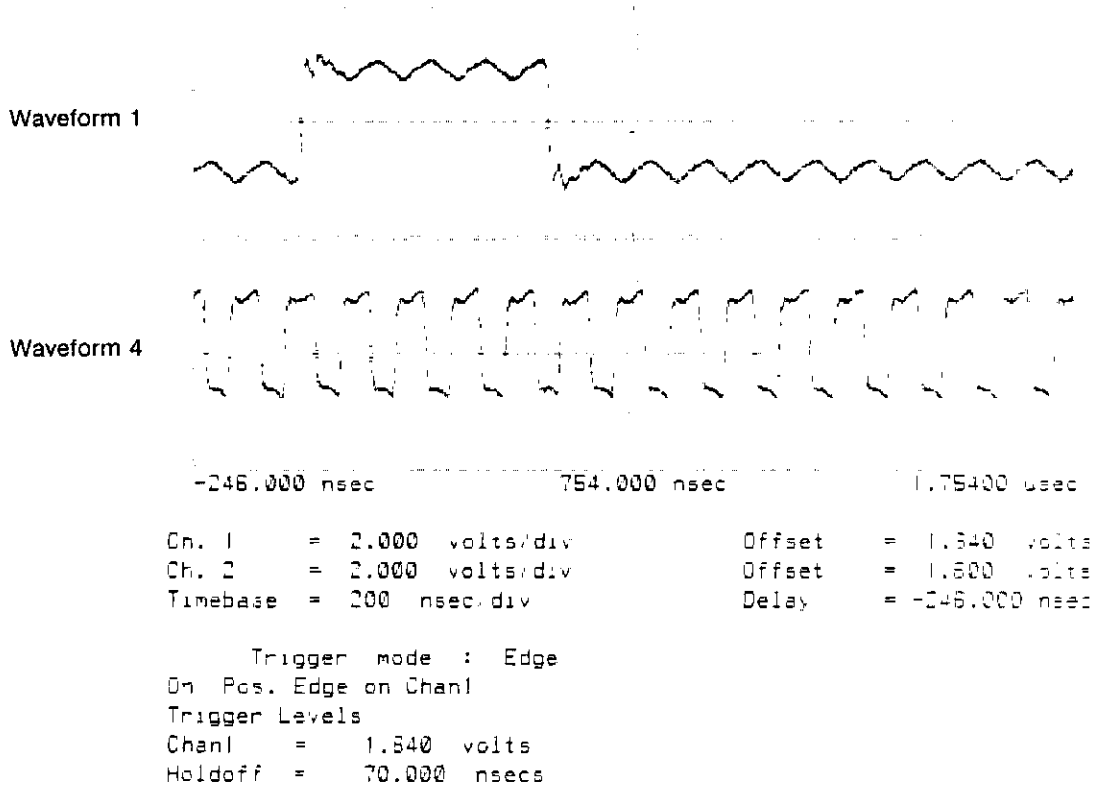


Figure 6D-3. Waveform Numbers 1 and 4.

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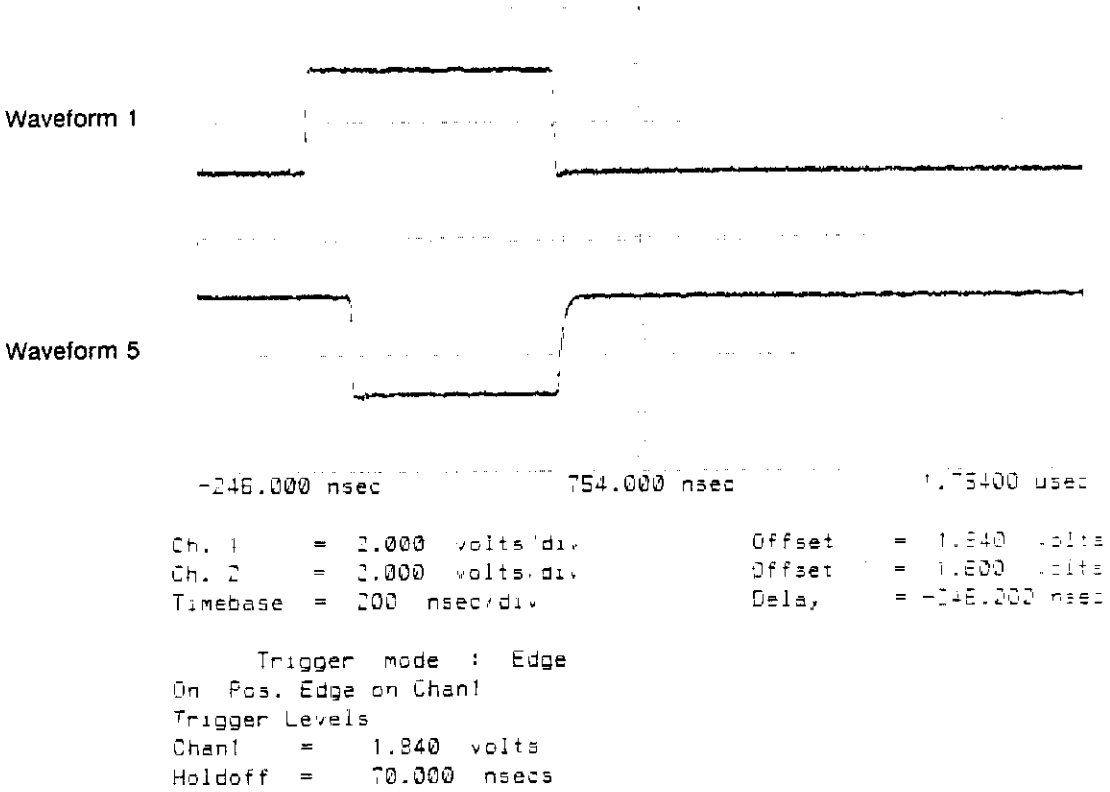


Figure 6D-4. Waveform Numbers 1 and 5.

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6D-6. BOARD EXTENDER OPERATION

The board extender, HP 54100-69501, will operate (i.e. will not cause self-test loops to fail) with all of the main card cage boards, with the following exceptions and modifications.

1. The Timebase board will not operate on the extender, i.e. the self-tests wil fail. However, it is possible to do some probing on components which function properly without the self-tests passing. To probe components which do require the self-tests to pass, place the Timebase board in the A10 slot. For an HP 54100A, this slot is vacant. For an HP 54100D, this slot contains the Trigger Qualifier board. If the instrument is an HP 54100D, it can be converted to an "A model." This is accomplished by removing the Trigger Qualifier board, and recabling the instrument as shown in figure 6D-5. The Timebase board can now be installed in the A10 slot. Remove the side panel to probe the board.

2. The I/O board is smaller in size then the other boards because it fits into a narrower mainframe opening. The extender will not fit in the I/O board slot. To service the I/O board requires placing it in slot A10. For an HP 54100A the A10 slot is vacant. For an HP 54100D, this slot contains the Trigger Qualifier board. If the instrument is an HP 54100D, it can be configured to an A model. This is accomplished by removing the Trigger Qualifier board from the instrument and recabling the instrument as shown in figure 6D-5. In this configuration loops 0 and 9 will fail, but these failures will not affect the operation of the other loops.

   Once the I/O board is installed in the A10 slot, re-route the keyboard cable so it will plug into the I/O board's new location. If HP-IB use is required, remove the HP-IB port from the rear panel. To accomplish this, remove the two black screws which hold the HP-IB port to the rear panel. Then connect the HP-IB cable to the I/O board's new location.

3. To troubleshoot the HP 54100A/D Display board requires a longer ribbon cable (HP part number 54100-69008) to connect the Display board to the Display Driver board.

4. Troubleshooting the Trigger board in an HP 54100A is straight forward. Remove the right side cover and use a monitor oscilloscope to probe the board. For an HP 54100D, configure the instrument as an "A model". First, remove the Trigger Qualifier board. Second, recable the instrument as shown in figure 6D-5. Third, remove the right side cover. A monitor oscilloscope can now be used to probe the board.

5. To troubleshoot the Trigger Qualifier board in an HP 54100D, remove the side panel and probe the board without the extender. The Trigger Qualifier will not operate on the board extender.

NOTE

When troubleshooting with the Extender board, do not leave the board on the extender longer than necessary. Using the Extender board for prolonged periods of time may over heat the board under test. This may shorten the life expectancy of other components on the board. A fan may be used to help cool the board when it is on the extender.

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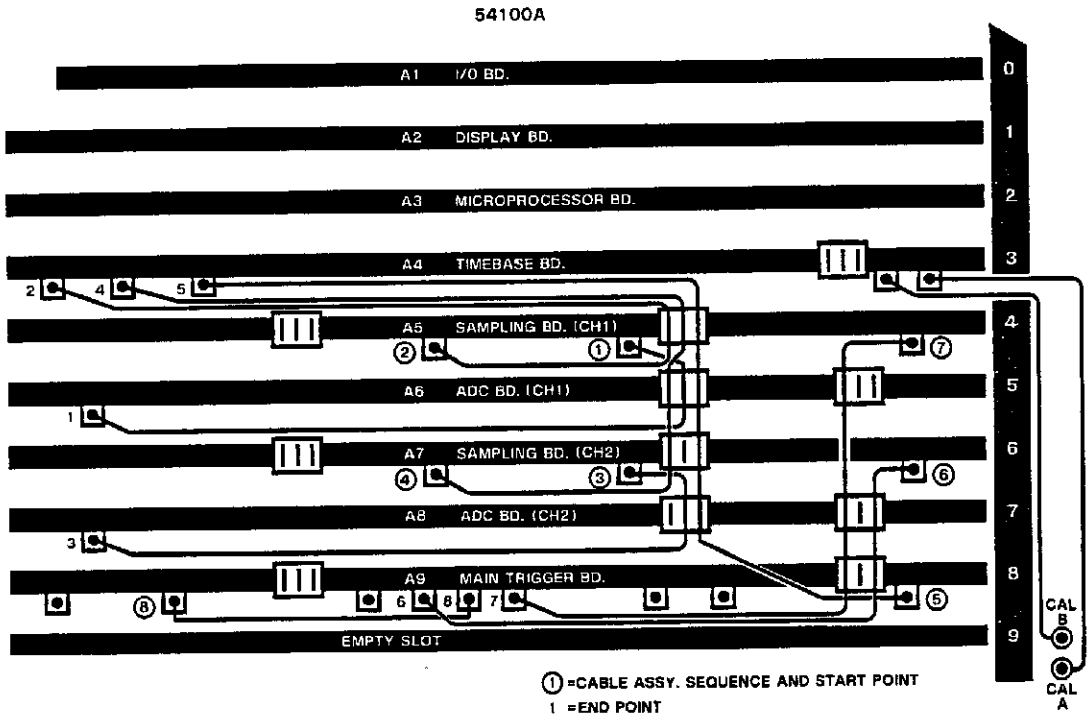


Figure 6D-5. HP 54100A Board and Cable Location Diagram.

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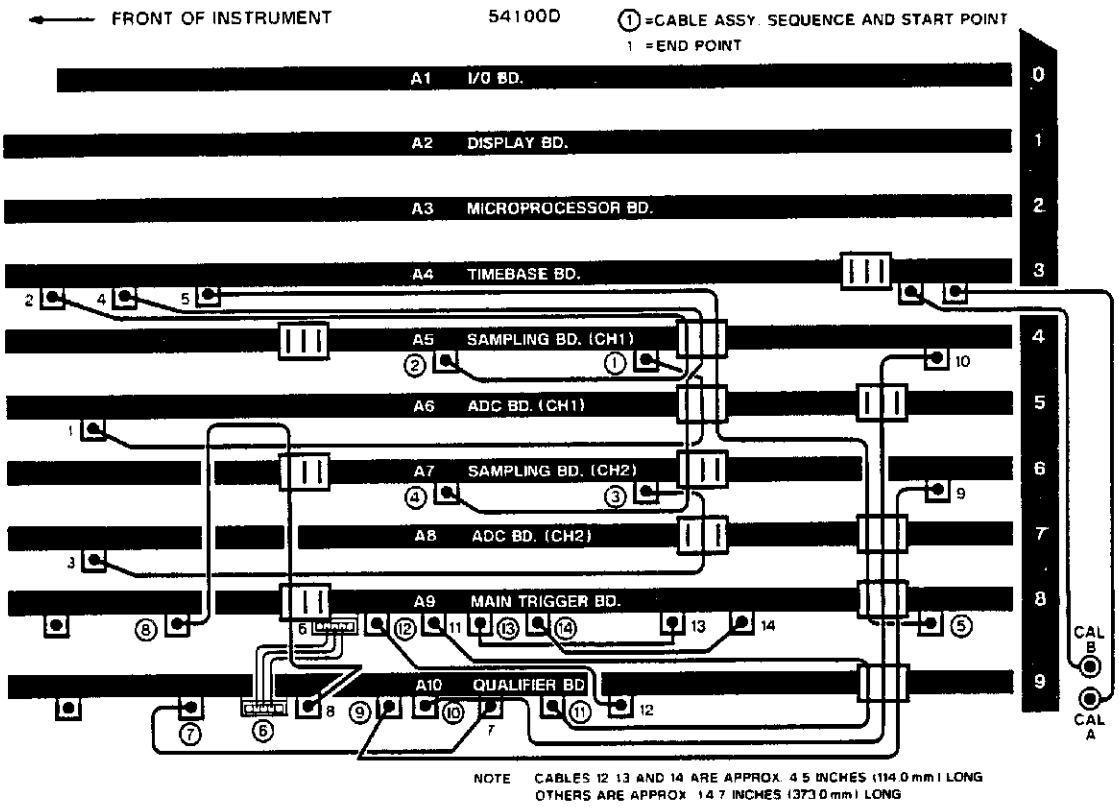


Figure 6D-6. HP 54100D Board and Cable Location Diagram.

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6D-7. 2-KEY POWER-UP (HARD RESET)

Whenever a "Power-up self-test Failed" or "Loop # = x" indication occurs more than once (true failure), a 2-key Power-Up (Hard Reset) routine may clear the problem. There may be occasions when memory will have erroneous data written to it during power-up cycles that cause a false failure. Performing the 2-key Power-up will ensure that memory is completely cleared so that the self-tests can repeated without false failure indications.

NOTE

The calibration factors are also erased from memory when a 2-key Power-Up is performed. ***Make sure the failure indication has occurred twice before using this procedure to avoid needlessly erasing the calibration factors.*** *Once a 2-key Power-Up routine is performed, the calibration factors will need to be reset in memory. To restore the calibration factors, perform the procedure in Section 6C-5.*

Procedure:

1. Turn instrument off.
2. While holding the top and bottom function keys to the right of the CRT, turn on the instrument and hold the two function keys for the duration of the power-up cycle (approximately 30 seconds maximum), or until the CRT displays either a pass or fail advisory.
3. Repeat the self-test where the failure indication occurred.
4. If the self-test still fails, continue with the troubleshooting procedure.

6D-8. I/O BOARD MASTER RESET

The I/O board contains a master reset button labeled SW1 on the I/O board schematic. This master reset allows the HP 54100A/D to be powered off, and then powered on by service personnel. The reset performs the normal power-up cycle that the instrument goes through when the line switch is cycled off and on. However, the only difference is that it does this power-up with all power supplies fully charged. If a power supply start-up problem is suspected, this master reset can be used to help determine these types of faults.

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6D-9. KEYBOARD TROUBLESHOOTING.

Interface test 11 is used to verify that all front panel keys and RPG are working. When Interface test 11 is entered, a keyboard mockup will be displayed on the CRT. The mockup consists of a box corresponding to each key on the front panel. Each box will light when the corresponding key is pressed. mockup consists of a set of radial lines representing a circle in the lower right corner of the CRT. When the RPG is rotated, an "O" cursor will rotate around the circle.

To initiate the test:

1. Select ***Utility*** menu.
2. Press ***Interface Tests*** key.
3. Enter *11* with the entry devices.
4. Press ***Start Test***.
5. Press each front panel key and verify that each corresponding box lights.

NOTE

The third softkey from the top right side of the CRT is normally assigned as the stop test key, when tests are running. When this test is first entered, the third softkey is not assigned any special functions. The first press of this key will light the corresponding box on the CRT, and at the same time the designation of stop test will now be assigned to the key.

6. Rotate the RPG and verify the "O" cursor rotates around the circle.
7. To exit this test, press the ***Stop Test*** key.

Diagnostics:

If only one key does not work, the suspect failure would be that particular keyboard.

If only one row or column of keys does not work, or if no keys work, then follow the procedure on the next page. This procedure verifies the signals coming into the keyboard from the cable connecting the I/O board to the keyboard.

If the procedure does not result in any failures, then repeat the procedure by checking the signals at the I/O board connector. This checks the continuity of the cable.

If this test and all of the self-tests pass, then the keyboard should be suspected as faulty.

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Procedure:

Probe the following points for the following signals.

Table 6D-3. keyboard Cable W1 Signals.

Pin No.	Signal
Pins 1-4	+5 V
Pins 5-12	Keyboard scan lines
Pins 13-14	NC
Pin 15	RPG 0 V
Pin 16	NC
Pin 17	RPG 1.4 V
Pin 18	RPG .8 V
Pin 19	Led 5 V
Pin 20	Led 0 V
Pins 21-22	NC
Pins 23-30	No signal except when a key is pressed.
Pins 31-32	RPG 0V
Pins 33-34	NC

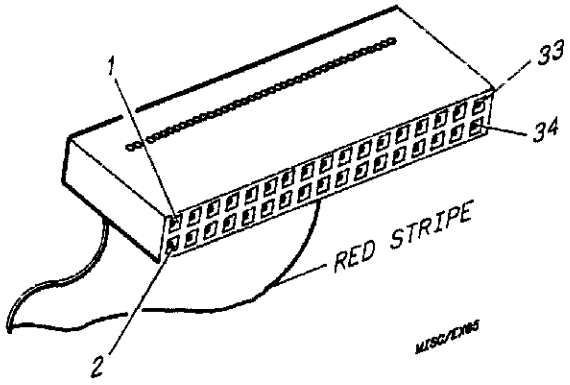


Figure 6D-7. keyboard Cable W1 Pin Locations.

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6D-10. PROBE POD TROUBLESHOOTING

The best method for troubleshooting probe pod failures is swapping the pods from one channel to another. The first step is to determine if the instrument passes self-tests. This can be done with all the pods removed. Once the instrument passes self-tests, the next step is to determine if one of the probe pods is functioning properly when an external stimulus is applied. A known good probe pod in the suspected bad channel will help isolate the problem to the pod or the analog portion of the instrument for that channel.

NOTE

When attempting to check channel 3 or channel 4 probe pods, install them in channel 1 or 2 so that the stimulus signal can be more easily observed if the pods are working.

If a probe pod proves to be faulty, it should be replaced with an exchange assembly or a new pod, depending on the probe model. Refer to Section 5, Replaceable Parts, of this manual.

Occassionally a failure caused by the probe pod connecting cable that connects the pod to one of the acquisition boards may occur. The above troubleshooting procedure would indicate that the suspected problem would be one of the acquisition boards. Before swapping out the suspect board, a check of the cable should be performed. This can be done in two ways.

1. Swap the suspected cable with a known good input channel. See the disassembly procedure, Section 6A, for details.

2. Check the continuity of each cable's ports including all six digital cables, the coax ground, and coax center conductor. See Section 7, Accessory Service, for each wire's purpose.

When a probe pod connector cable is open or intermittent, the self-tests will pass. If signal is applied to the oscilloscope, no signal will be displayed. In this case, the probe pod connecting cable can be highly suspected as the failure.

6D-11. POWER SUPPLY TESTS AND TROUBLESHOOTING PROCEDURE

The power supply consists of three PC board assemblies. When defective, one, two, or all three must be replaced with an exchange assembly. The following procedure will help isolate which board or boards has failed.

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NOTES FOR FLOWCHART 1

1) A. FRONT PANEL POWER SWITCH SHOULD BE OFF
   B. REAR PANEL LINE SWITCH SHOULD BE OFF "0"
   C. CONNECT AC POWER SOURCE
   D. TURN REAR PANEL LINE SWITCH TO ON "1"

2) A. TURN REAR PANEL LINE SWITCH TO OFF "0"
   B. ALWAYS UNPLUG AC POWER SOURCE
   C. **CAUTION!!!** ***WAIT UNTIL +300 V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

3) A. TURN FRONT PANEL SWITCH TO OFF
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300 V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

12) THIS MAY BE OCCURING BECAUSE ONE OF THE SUPPLIES IS DRAWING SLIGHTLY TOO MUCH CURRENT. IT MAY NOT BE ABLE TO LOAD DOWN THE A11 BOARD ALL BY ITSELF PERFORM SHUTDOWN SEQUENCE #2. THEN MEASURE THE FOLLOWING IMPEDANCES.

J1 TOP PIN TO MIDDLE PIN - 830 KΩ
J1 MIDDLE PIN TO BOTTOM PIN - 44 KΩ
J1 TOP PIN TO BOTTOM PIN - 790 KΩ
J2 TOP PIN TO MIDDLE PIN - 820 KΩ
J2 MIDDLE PIN TO BOTTOM PIN - 45 KΩ
J2 TOP PIN TO BOTTOM PIN - 780 KΩ

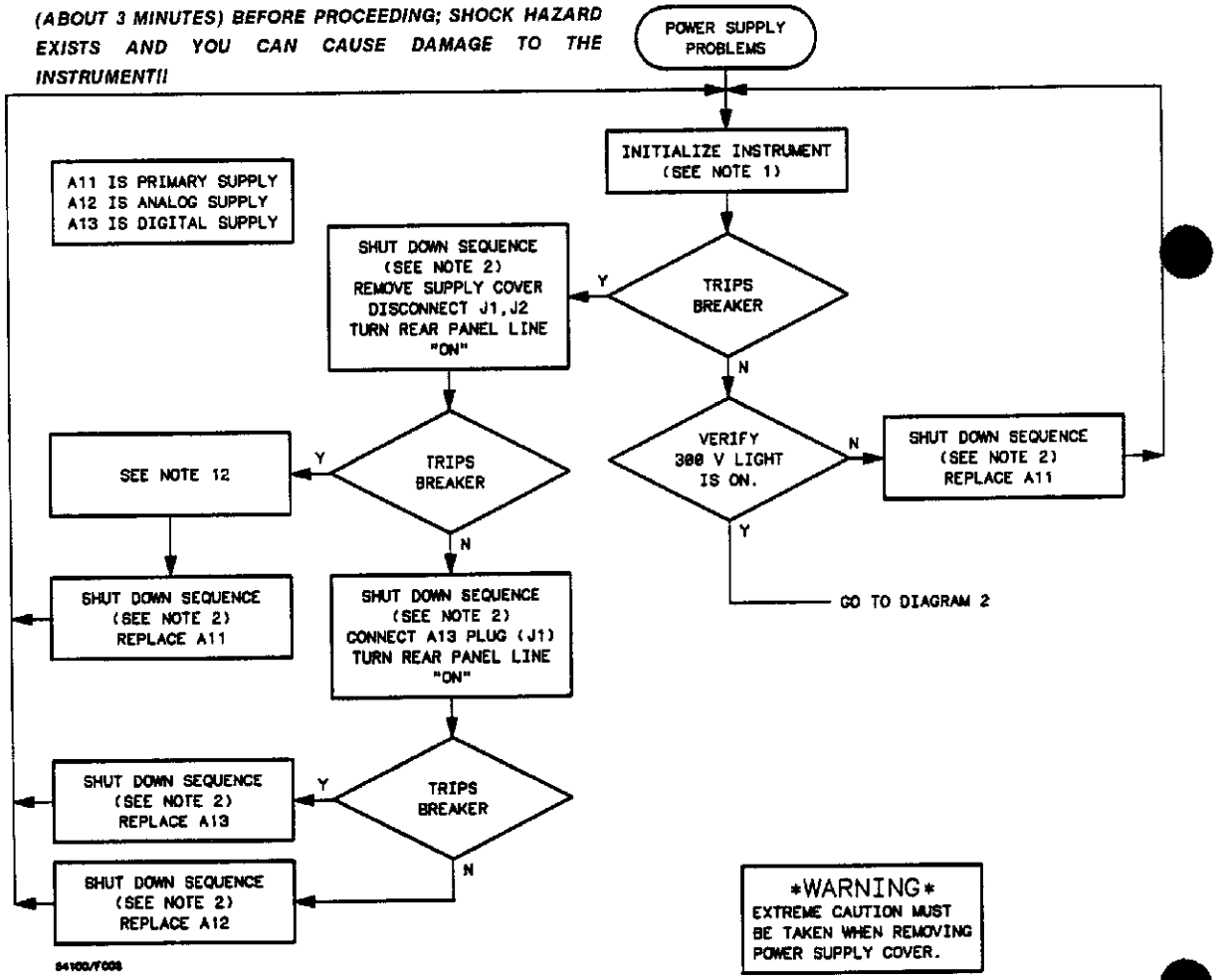


Figure 6D-8. Power Supply Troubleshooting Flowchart #1.

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NOTES FOR FLOWCHART 2

3) A. TURN FRONT PANEL SWITCH TO OFF
   B. TURN REAR PANEL LINE SWITCH TO OFF "0"
   C. ALWAYS UNPLUG AC POWER SOURCE
   D. **CAUTION!!!** ***WAIT UNTIL +300 V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

10) CONNECT THE VOLTMETER (+) LEAD TO THE "FAN" TEST POINT AND THE (-) LEAD TO SECONDARY GROUND. THE READING SHOULD BE -7.5 V. THIS VOLTAGE WILL INCREASE WITH INCREASING INSTRUMENT AMBIENT TEMPERATURE.

11) FOR POWER SUPPLY TEST POINTS AND SPECIFICATIONS SEE TABLE BELOW.

DIGITAL SUPPLY TST PTS (+) LEAD	(-) LEAD	VOLTAGE
+5 V	GND	+5.10 ±0.1 V
-5 V	GND	-5.30 ±0.1 V
+14B	GND	>+5V
ANALOG SUPPLY TST PTS (+) LEAD	**(-) LEAD**	**VOLTAGE**
+18 V	GND	+18.5 ±0.3 V
+8 V	GND	+8.9 ±1 V
-8 V	GND	-8.5 ±1 V
-18 V	GND	-18.5 ±0.3 V
FAN	GND	-7.5 ±0.3 V
+26B	GND	>+5 V

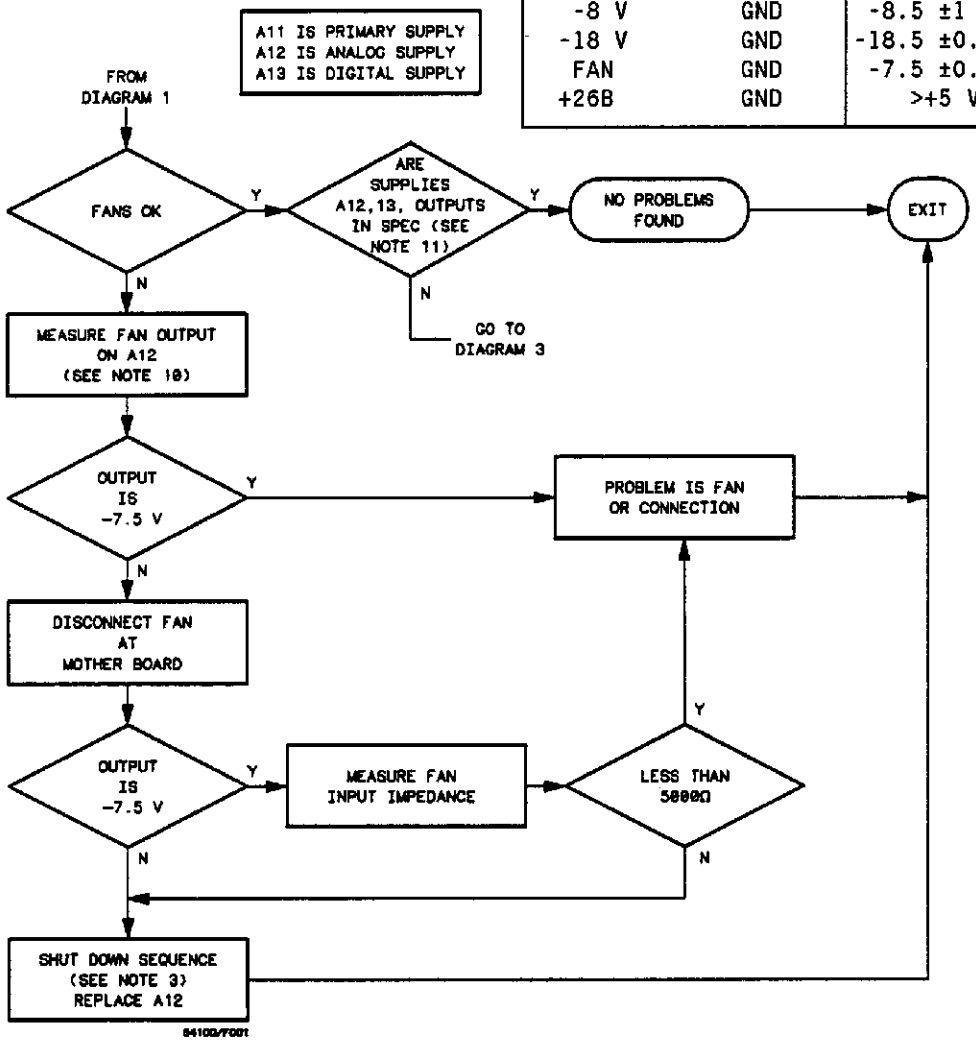


Figure 6D-9. Power Supply Troubleshooting Flowchart #2.

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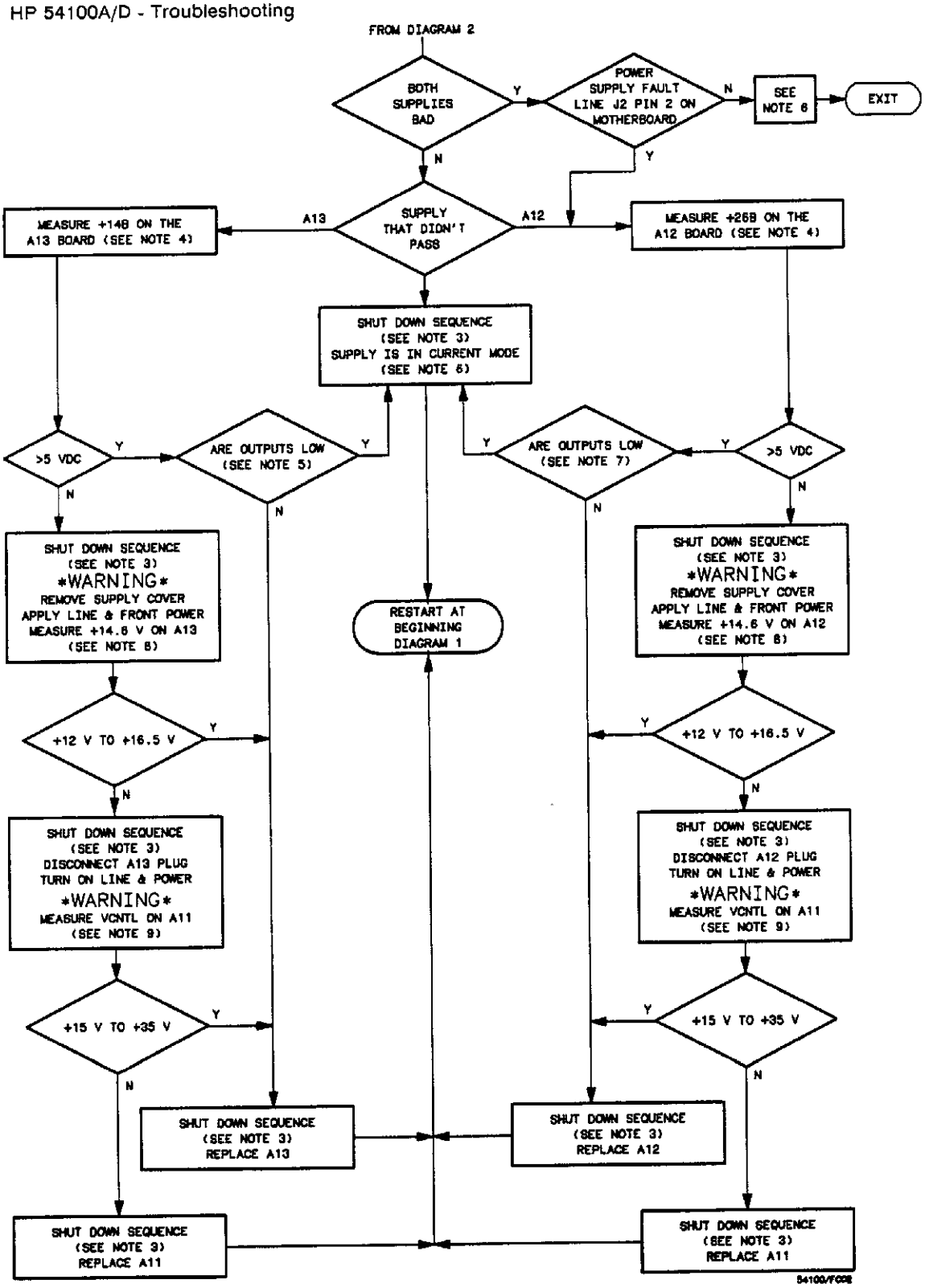


Figure 6D-10. Power Supply Troubleshooting Flowchart #3.

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NOTES FOR FLOWCHART 3

3) A. TURN FRONT PANEL SWITCH TO OFF
B. TURN REAR PANEL LINE SWITCH TO OFF "0"
C. ALWAYS UNPLUG AC POWER SOURCE
D. **CAUTION!!!** ***WAIT UNTIL +300V LIGHT IS COMPLETELY OFF (ABOUT 3 MINUTES) BEFORE PROCEEDING; SHOCK HAZARD EXISTS AND YOU CAN CAUSE DAMAGE TO THE INSTRUMENT!!***

4) THE NOMINAL OUTPUT FOR +14B IS 21V HOWEVER, WHEN THE SUPPLY IS OPERATING IN THE CURRENT LIMIT MODE, IT CAN BE AS LOW AS +5V THE NOMINAL OUTPUT FOR +26B IS 26V. IT TOO CAN BE AS LOW AS +5V WHEN IN CURRENT LIMIT.

5) MEASURE OUTPUTS +5V AND -5V ON THE DIGITAL POWER SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES IF OUTPUTS ARE GREATER THAN HALF, THE ANSWER IS NO

7) MEASURE OUTPUTS ±18V AND ±8V ON THE ANALOG SUPPLY. IF BOTH OUTPUTS ARE LOW, I.E. HALF OF NORMAL OUTPUT OR LESS, THEN DIRECTION TO TAKE IS YES. IF OUTPUTS ARE GREATER THAN HALF, THE ANSWER IS NO

8) THE TEST POINTS TO MEASURE +14.6V ARE AT THE BACK OF THE BOARD CLOSE TO THE TOP. CONNECT THE VOLTMETER COMMON LEAD TO THE COM TEST POINT ON THE BOARD. **CAUTION!!!** ***USE CAUTION WHEN MEASURING THIS VOLTAGE. IT IS NOT ISOLATED FROM THE LINE (MAINS) INPUT AND THE PRIMARY SUPPLY IS EXPOSED WHEN THE POWER SUPPLY COVER IS REMOVED.***

9) BY REMOVING THE CONNECTORS AT J2 AND J3 YOU ARE CHECKING IF EITHER THE ANALOG OR DIGITAL SUPPLY IS LOADING VCNTL.

EXTREME CAUTION MUST BE TAKEN WHEN MEASURING VCNTL ON THE PRIMARY SUPPLY THE TOP PIN ON CONNECTORS J2 AND J3 IS VBULK WHICH IS +300V THE PINS BELOW ARE VCNTL, THEN GROUND.

TO MEASURE VCNTL, TURN THE POWER OFF AND MAKE SURE THE +300V LAMP (NEAR TOP OF BOARD) IS OFF. CONNECT THE VOLTMETER (+) LEAD TO VCNTL (SECOND PIN FROM TOP) AND THE (-) LEAD TO GROUND (BOTTOM PIN). APPLY POWER AND OBSERVE THE METER READING. WITH ONE SUPPLY CONNECTED THE READING SHOULD BE ABOUT +25V AND WITH NEITHER CONNECTED ABOUT +42V TURN OFF POWER (+300V LAMP IS OFF) BEFORE REMOVING THE VOLTMETER LEADS.

---

6) WHEN THE SUPPLIE(S) ARE RUNNING IN THE CURRENT MODE THIS MEANS THAT AN EXTERNAL LOAD IS PULLING DOWN THE SUPPLY OUTPUT(S). AN EXTERNAL LOAD COULD BE A BOARD IN THE CARD CAGE OR THE DISPLAY ASSEMBLY. THE ONLY WAY TO ISOLATE THE DISPLAY ASSEMBLY IS TO COMPLETELY REMOVE IT FROM THE MAINFRAME. THE FAN CAN ALSO PUT THE ANALOG BOARD INTO THE CURRENT MODE. YOU CAN DISCONNECT THE FAN BY REMOVING THE BOTTOM COVER AND DISCONNECTING THE FAN CABLE

TO ISOLATE A CURRENT PROBLEM, REMOVE ONE LOAD AT A TIME UNTIL THE PROBLEM IS FOUND. PROBLEMS COULD INCLUDE BENT PINS ON THE MOTHER BOARD OR A BAD COMPONENT ON A PC ASSEMBLY. SEE THE ADJACENT TABLE FOR POWER DISTRIBUTION TO THE VARIOUS ASSEMBLIES

	+5V	-5V	+18V	+8V	-8V	-18V	+120V
TIMEBASE	*		*	*	*	*	
MICROPROCESSOR	*						
INPUT/OUTPUT †	*	*	*	*	*	*	
CH1 ADC CONT	*	*	*	*	*	*	
CH1 ADC	*		*			*	
CH2 ADC CONT	*	*	*	*	*	*	
CH2 ADC	*		*			*	
TRIGGER	*	*	*	*	*	*	
TRIGGER QUAL	*	*		*	*		
COLOR DISPLAY	*						
COLOR CRT MOD.							*

†ONLY THE +5V IS USED FOR POWER. THE OTHER SUPPLIES CONNECT FOR POWER TEST ONLY AND ARE HIGH IMPEDANCE POINTS. LIKELIHOOD OF LOADING THESE SUPPLIES IS LOW.

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6D-12. HOW ADJUSTMENTS CAUSE LOOP TESTS TO PASS OR FAIL

Table 6D-4 contains a simplified diagram of how the adjustments can cause the loops to pass or fail. These results are true when only one or two adjustments are slightly out of specification.

Before deciding that a self-test is failing because of a hardware problem, use this table to slightly vary the adjustments which could be causing the self-test failure.

However, using just this table is not sufficient. The reason is many of the adjustments interact with each other. The following rules should be followed when any one of the adjustments in each of the following adjustment groups is made.

1. Sampler adjustment group: when performing any of the adjustments listed below, all adjustments in the list below the adjustment that was varied should also be made.

   INULL
   ONULL
   SBIAS
   SEFF
   10 ms
   1msec A-B
   OFCAL
   GAIN
   SAMPLER TRIGGER

   Two notes: a) 1 μs A-B affects gain the most.
   b) 10 ms affects OFCAL the most.

2. ADC adjustment group: The dc offset and HF gain adjustments should be readjusted anytime one of the sampler adjustments is moved (with the exception of when just the sampler trigger adjustments are made). In addition, only the affected Sampler/ADC pair need be adjusted.

3. Trigger board adjustment group: The three Channel 3 trigger adjustments and the fine interpolator are completely independent of any other adjustments. The fine interpolator adjustment should only be made if "holes" appear in the waveform, spaced at 25 ns intervals.

4. Trigger Qualifier adjustment group: The three Channel 4 trigger adjustments are totally independent of any other adjustments. The other four Trigger Qualifier adjustments are also independent of other adjustments. Whenever one of the four Trigger Qualifier adjustments is made, the other three should be repeated.

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Table 6D-4. Which Adjustments Affect Which Loops.

Loops 1-20	Not affected by any adjustments.
Loops 21	Channel trigger hysteresis and main trigger hysteresis.
Loop 22	Not affected by any adjustments.
Loop 23	Channel trigger hysteresis and main trigger hysteresis.
Loops 24-26	Not affected by any adjustments.
Loops 27,28	Channel trigger hysteresis and main trigger hysteresis.
Loop 29	Not affected by any adjustments.
Loops 30-33	Channel trigger hysteresis and main trigger hysteresis.
Loop 34	Not affected by any adjustments.
Loop 35	Channel 1 input null, output null, sampler bias.
Loops 36,37	Channel 1 input null, output null, sampler bias, offset cal, gain.
Loop 38	Not affected by any adjustments.
Loop 39	Channel 2 input null, output null, sampler bias.
Loops 40,41	Channel 2 input null, output null, sampler bias, offset cal, gain.
Loop 42	Not affected by any adjustments.
Loop 43	Trigger qualifier hysteresis.
Loops 44-46	Trigger qualifier, main trigger, and channel hysteresis adjustments.
Loops 47-54	Trigger qualifier and main trigger hysteresis adjustments.
Loops 55-57	Trigger qualifier, main trigger, and channel hysteresis adjustments.
Loops 58-60	Not affected by any adjustments.
Loop 63	Not affected by any adjustments.

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6D-13. WHAT ADJUSTMENTS TO MAKE AFTER BOARDS ARE REPLACED

After replacement of a board, some adjustments may have to be made, because most adjustments are dependent on each other. However, make sure to follow the rules on how to make these adjustments (see Section 6D-12).

Sampler board: all sampler board adjustments should be performed.

ADC board: dc offset and all sampler board adjustments should be performed.

Trigger board: all trigger board adjustments should be performed.

Trigger Qualifier board: all trigger qualifier board adjustments should be performed.

CRT and/or Yoke: all yoke and display driver adjustments should be performed.

Digital Power Supply: The digital power supply adjustment should be performed.

6D-14. HOW ADJUSTMENTS AFFECT PERFORMANCE VERIFICATION

Whenever an adjustment is made by itself or made when a board is replaced, the performance of the unit may be affected. Listed below are the various adjustments and which specifications may have changed.

ADC board	**Specifications**
DC Offset	Vertical Accuracy
High Freq. Gain	Vertical Accuracy
Sampler board	
Input null	Vertical Accuracy, Risetime
Output null	Vertical Accuracy, Trigger Sensitivity
Sampler Bias	Vert. Accuracy, Bandwidth, Timebase Accy, Trigger Sense, Risetime.
10 ms flatness	Vert. Accuracy, Risetime, Timebase Accy, Trigger Sense.
1 μs flatness - A	Vertical Accuracy, Risetime
1 μs flatness - B	Vertical Accuracy, Risetime
Sampling efficiency	Vert. Accuracy, Bandwidth, Risetime, Timebase Accuracy
Offset Cal	Vertical Accuracy, Risetime
Gain	Bandwidth
Trigger Hysteresis	Trigger Sensitivity
Trigger Offset	Risetime, Trigger Sensitivity
Trigger Level	Timebase Accuracy, Trigger Sensitivity
Trigger board	
Trigger Hysteresis	Trigger Sensitivity
Trigger Offset	Risetime, Trigger Sensitivity
Trigger Level	Timebase Accuracy, Trigger Sensitivity
Fine Interpolator	
Trigger Qualifier	
Trigger Hysteresis	Trigger Sensitivity
Trigger Offset	Risetime, Trigger Sensitivity
Trigger Level	Timebase Accuracy, Trigger Sensitivity

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6D-15. HOW ADJUSTMENTS AFFECT THE DISPLAYED WAVEFORM

The following list is a short qualitative description of how the adjustments affect the displayed waveform. This information can be used to quickly evaluate if an adjustment is misaligned. To see the same results, connect the rear panel cal signal to channel 1. Set the display mode to eight averages.

Digital P/S Yoke Display Driver	These adjustments do not affect the displayed waveform, but the entire display's height, width, and centering.
Gain HFGAIN	These adjustments affect the gain of the displayed waveform.
ADC Offset OFCAL	These adjustments affect the offset of the displayed waveform. When the input signal is removed and the offset is set to zero, the waveform should cross very close to center screen (±1 minor division)
Trigger Hysteresis Trigger Offset (all boards)	These cause non-triggering, if they are just slightly out of adjustment. The non-triggering will only occur on the channel with the adjustment problem. The hysteresis should be set to one major division.
Trigger Level (all boards)	Has no effect on the displayed waveform when misaligned by itself. However, when coupled with the other trigger adjustments, this can cause non-triggering on that trigger channel.
Fine Interpolator	The adjustment will place "holes" in the waveform at about 25 nsec intervals. The size of the holes depends on how far off the adjustment is (typically <1 ns).
SBIAS	This adjusts the first 25 nsec step of the waveform's top. When this adjustment is slightly wrong one way, the step in the first 25 will be too high. When the adjustment is set slightly too far the other way, non-triggering can occur. This adjustment and SEFF affect each other and should always be performed together.
SEFF	When this adjustment is out, the 25 nsec step will be either too high or too low. In addition when this adjustment is out, the frequency response curve of the unit falls much faster and begins to oscillate. Also affected is the ac voltage measurement accuracy.
Input Null Output Null	These adjustments affect the input and output impedance of the pre-amp on the sampling board. They can cause offset and gain problems with the displayed waveform if not adjusted properly.
10 msec, 1msec A-B	These affect the offset level of the cal signal. This is because the cal signal is 500 KHz and a 1 KHz signal should be used to see their effect on the waveform's flatness. These adjustments affect the first X number of seconds that the waveform is flat, where X is the number of seconds indicated by the adjustment's name.
Trig Qual Adjustments	These have no affect on the cal signal when triggered in the edge mode.

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6D-16. QUICK REFERENCE TO LOOP FAILURE PATTERNS

Table 6D-5. Loop Test Failures When One of The Data Acquisition Boards Is Removed From an HP 54100A/D (no pads, or coax cables connected)

These Loops Fail	When this board is removed
20,23,30,31,32,33 (All Qual Loops)	QUAL
19,35,36,37,39,40,41	TRIG
38	ADC2
16,21,23,27,28,30,31	SAMP2
36,37,38	ADC1
16,21,23,27,28,30,31,36,37	SAMP1
17	TIME

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Table 6D-6. Loop Test Failures in an HP 54100A/D When Boards are Removed from the SIB

Loops Fail	Remove
15,16,21,23,27,28,34,38	SAMP1, ADC1, SAMP2, ADC2
16,21,23,27,28,30,31,34,38	ADC1, SAMP2, ADC2
16,21,23,27,28,30,31,38	ADC2, SAMP2
19,35,36,37,39,40,41	TRIG
17	TIME
24,27,28,35	TIMEBASE'S THREE MASTER CLOCK COAX CABLE
NONE, 35,36,37, (All are very intermittent)	TRIG MASCLK-COAX FROM TIME
16,21,23,27,28,30,31,38	ADC1, SAMP1
38	ADC2
16,21,23,27,28,30,31	SAMP2
36,37,38	ADC1
16,21,23,27,28,30,31,36,37	SAMP1
34,38	ADC1, ADC2
15,16,21,23,27,28	SAMP1, SAMP2

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Table 6D-7. Loop Test Failures When Only One Data Acquisition Board is Inserted in an HP 54100A/D on the SIB (no pods inserted).

These Loops Fail	Only Board Installed
15,16,17,19,34,38	QUAL
15,16,17,23	TRIG
15,16,17,19,20,38	ADC2
16,17,19,20,34,38	SAMP2
15,16,17,19,20,38	ADC1
16,17,19,20,34,38	SAMP1
15,16,19,20,34,38	TIME

6D-8. Loop Failures When Coax Cables are Missing, Mis-wired, or Intermittent in an HP 54100A

Loop Failure	Cable
20,21,23,27,28,30,31,32,33	When TCLK1 Disconnected:
20,21,23,27,28,30,31,32,33	When TCLK2 Disconnected:
20,21,23,27,28,30,31,32,33	When TCLK3 Disconnected:
35,36,37, none (these loops fail very intermittently)	When MCLK1 Disconnected:
none	When MCLK2 Disconnected:
20,24,27,28	When MCLK3 Disconnected:
36,37	When IF OUT1 Disconnected:
40,41	When IF OUT2 Disconnected:
20,21,23,24,27,28,30,31,32,33,36,37,40,41	When all Cables Disconnected:
46-54	OPTHLDF Cable Disconnected:

6D-17. OVERALL TROUBLESHOOTING TREES.

Basic troublshooting trees are contained in figures 6D-11 through 6D-13. The trees are not designed to isolate intermittent failures. If the tree indicates the problem is with the loops, the flowchart will not help resolve the problem.

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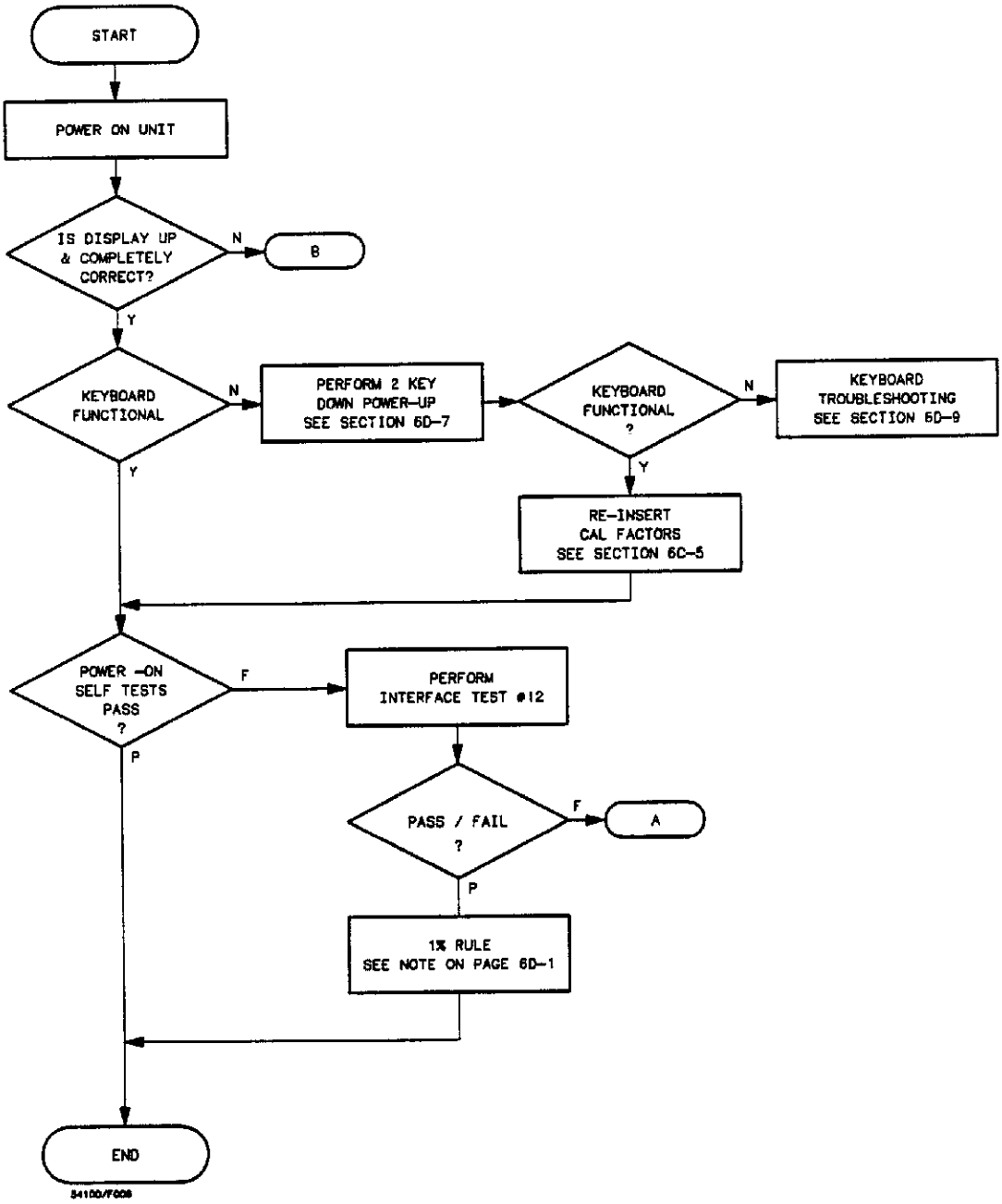


Figure 6D-11. Troubleshooting Tree Number 1.

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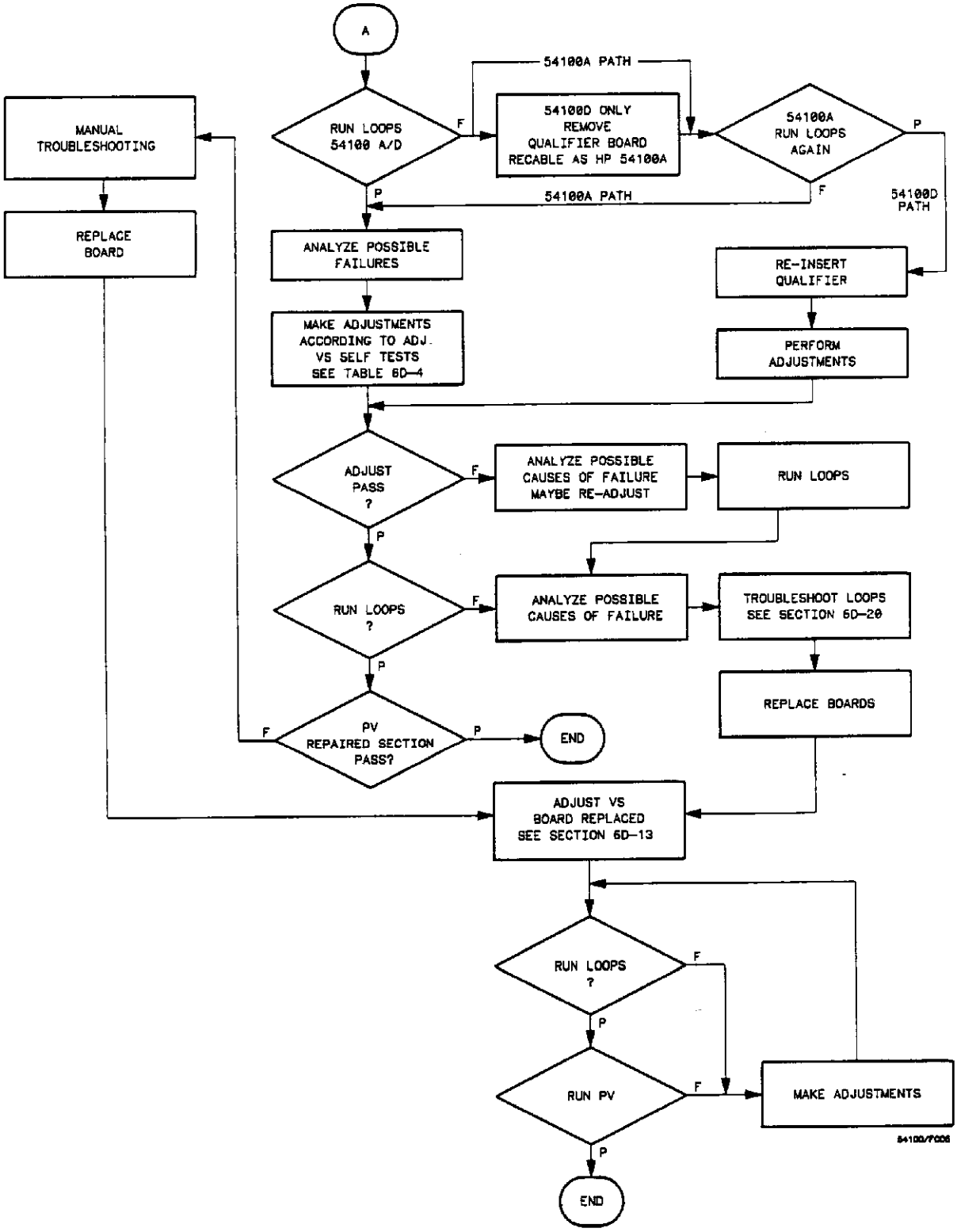


Figure 6D-12. Troubleshooting Tree Number 2.

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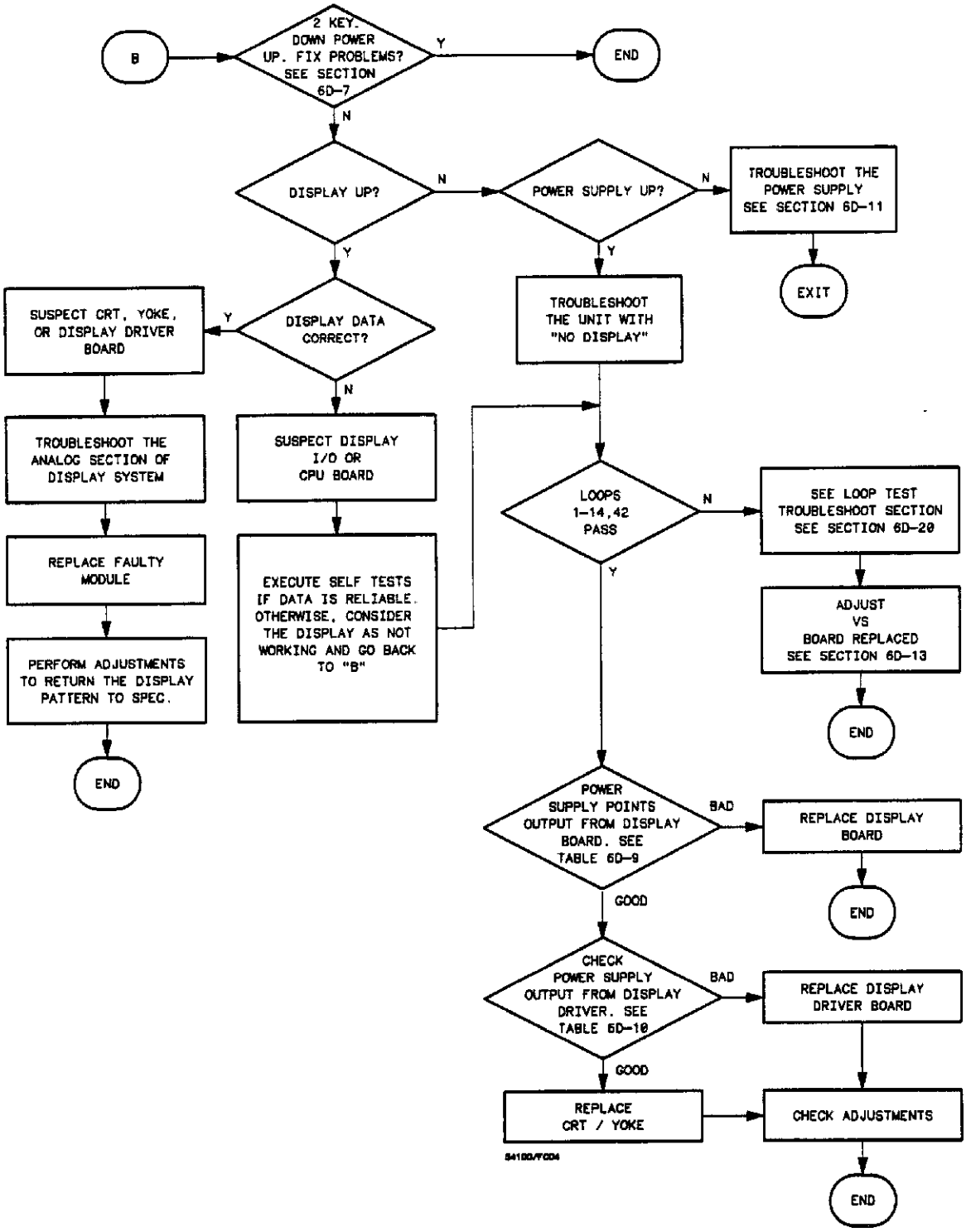


Figure 6D-13. Troubleshooting Tree Number 3.

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6D-18. TROUBLESHOOTING WITH NO DISPLAY

Troubleshooting the system when the display is not operating requires that the power supplies are functioning properly. Four other signals are also required. These are:

HVSYNC	High Vertical SYNC
HHSYNC	High Horizontal SYNC
HFB	High Full-bright
HHB	High Half-bright

Table 6D-9 shows the pin locations on the display cable for the above signals. The display cable carries the signals from the Display board to the Display Driver board. The display cable signals should be checked first to help determine if the proper signals are present so the display can operate.

Table 6D-10 defines the wires used to connect the Display Driver board to the CRT and to the Yoke. Table 6D-10 also shows the proper voltage levels which should be on these wires.

If HVSYNC or HHSYNC are missing, the microprocessor can be placed in a self-test routine. These routines allow signatures to be taken on the A3 microprocessor board.

A properly strapped processor will execute the power-up self-test routine. When an error is found, the processor will repeatedly execute the loop that is failing. By reading the signature at TP+5 and referring to the signature tables, table 6D-11 and 12, the failing loop and board can be determined.

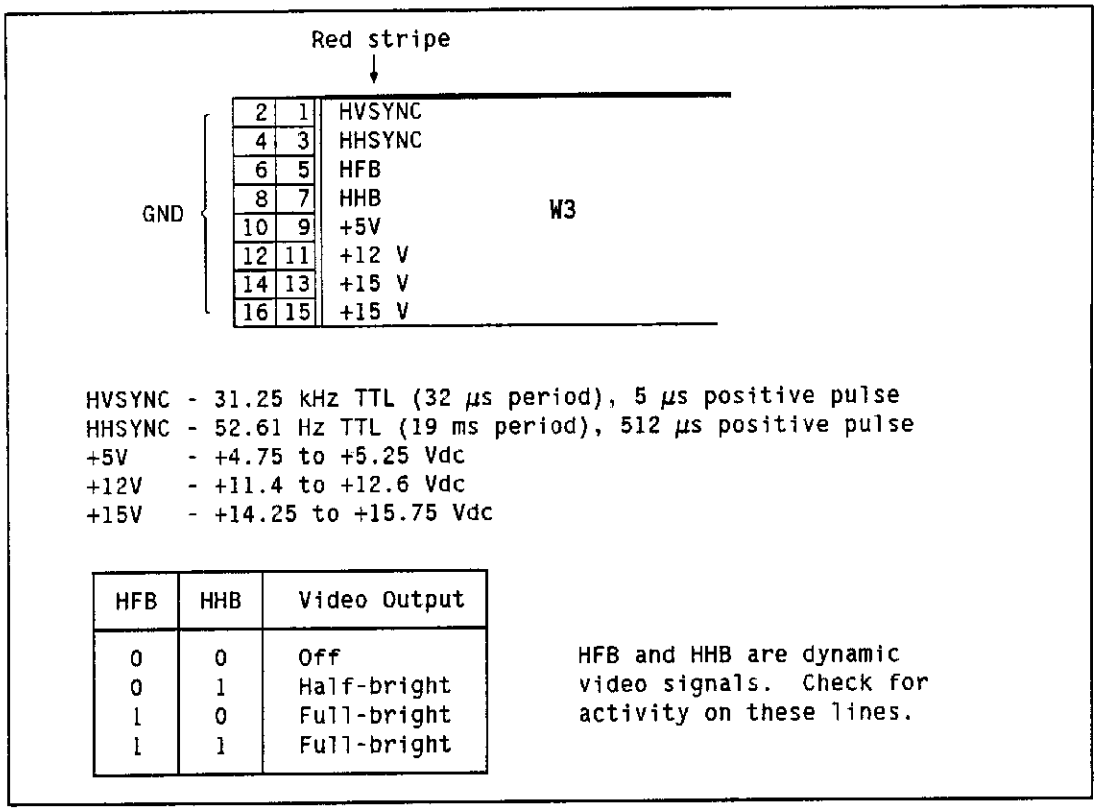
NOTE

Problems with the DISPLAY should be corrected prior to troubleshooting other system failures.

Refer to the Troubleshooting Tree Number 1 in figure 6D-11 for the sequence to follow while troubleshooting.

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Table 6D-9. Display Cable W3 Pin Locations.



HVSYNC - 31.25 kHz TTL (32 µs period), 5 µs positive pulse
HHSYNC - 52.61 Hz TTL (19 ms period), 512 µs positive pulse
+5V - +4.75 to +5.25 Vdc
+12V - +11.4 to +12.6 Vdc
+15V - +14.25 to +15.75 Vdc

HFB	HHB	Video Output
0	0	Off
0	1	Half-bright
1	0	Full-bright
1	1	Full-bright

HFB and HHB are dynamic video signals. Check for activity on these lines.

Table 6D-10. Display Driver Board to CRT Signals

	WIRE	SIGNAL
CRT Neck Pins	Blue	0 to 400 Vdc
	Red	500 to 800 Vdc (700 Vdc typical)
	Black	0 Vdc
	Brown	12 Vdc (13.2 Vdc typical)
	Yellow	48 to 82 Vdc
	Green	0 Vdc
Yoke	Blue	Dynamic video signals. Check for activity on these lines.
	Red	
	Yellow	
	Green	
Post Accelerator (large red wire to CRT body) is 8 kVdc to 12 kVdc (10 kVdc typical)		

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6D-19. SELF-TEST SIGNATURE ANALYSIS

1. Remove power from instrument and connect a jumper from A3TP2 to A3TP3.

2. Connect HP 5005B Signature Multimeter as follows:

START	A3TP1	Low to High
STOP	A3TP1	High to Low
CLOCK	A3TP6	Low to High
PROBE	A3TP+5	+5 Volts

3. Apply power to HP 54100A/D and HP 5005B Signature Analyzer.

4. After several seconds the HP 5005B readout should stabilize. Look up the signature in Table 6D-10 or 6D-11 to determine which board is causing the failure. If the readout does not stabilize, either there are no failures or a more complex problem is occurring.

NOTE

If the returned signature does not indicate a failure in loops 0 through 14 or 42, then the problem should be further isolated using the procedure in steps 5 through 8 below.

5. Remove power from HP 54100A/D.

6. Perform two key power-up. See Section 6D-7.

7. The microprocessor will write a known stable pattern to the display memory.

8. The HP 5005B multimeter should show the following frequencies at the following A2 test points:

TP4	35.7 KHz
TP5	60 Hz
TP6	3.6 MHz
TP7	3.6 MHz

If the above frequencies are incorrect, the Display Memory board A2 is faulty.

If the above frequencies are correct, the problem is either the CRT Driver (A18), the CRT, or the cabling from the Display board (A2) to the CRT Drive board (A18).

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6D-20. TROUBLESHOOTING WITH DISPLAY OPERATING.

When the display is operating, the loop failures that caused the power up self-test message to be displayed can be obtained with the following procedure.

1. Press ***UTILITIES*** menu.
2. Press ***TEST*** menu.
3. Press ***DISPLAY ERRORS*** key.
4. Read the loop failures from the display.

The loops have been organized so that loops closer to the top (loop 1) are more generalized than loops closer to the bottom (loop 63). Loops closer to the bottom tend to test specific parts of loops closer to the top. When a loop closer to loop 1 fails, it may cause some of the following loops to fail. When troublshooting loops, start with the loop closest to loop 1. Fixing that loop may result in other loops also being repaired at the same time, unless you have multiple failures. If other loops are still failing, again restart troubleshooting with the loop closest to loop 1.

When troubleshooting loops, there are several approaches which can be taken, depending on the type and number of failures that are displayed.

Loops 0 through 14, and 42 test the instrument's digital mainframe. If these loops fail, a high probability exists that only the board tested by that loop is the cause. If these digital loops fail, use Table 6D-10 to determine which board should be replaced. In addition, Section 6E, Selt-Test Loop Service, can be used to verify the probable cause.

Loops 15 through 41 test the data acquisition system of the unit. The data acquisition loops usually fail in multiples. Table 6D-10 can also be used to give a preliminary idea of the board causing the problem. Many times it will be necesary to use more sophisticated methods of troubleshooting to find the problem. The following Sections contain information on troubleshooting these loops. They are listed in order of preferred method.

1. Troubleshooting the data acquisition section.
2. Signal exchange.
3. Board swap.
4. Waveform comparison
5. Determine valid edge triggering patterns
6. Loop test troubleshooting. See Section 6E.

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Loops 43-60 test the Trigger Qualifier board. These loops are not entirely dependent on the Trigger Qualifier board. If these loops fail, use the following procedure to verify the faulty module.

1. First remove the Trigger Qualifier board from the HP 54100D. Recable the instrument as an HP 54100A model. Refer to figure 6D-5. In this mode loop 20 will fail. Loop 20 indicates that the HP 54100D software is installed and no Trigger Qualifier board was found during the power-up sequence.

2. Cycle the instrument's power off and then on. If any loops fail, they need to be repaired first. When all loops pass, continue with step three.

3. Trigger a monitor oscilloscope on the rear panel cal signal. Probe J4 pin 3 (OPHTLDF) on the Trigger board. Check for ECL transitions synchronous with the trigger. Pins 2 and 4 are ground pins.

4. With one of the 50 Ω cables (W11), connect J5 (DIN) on the Trigger board to either J8 or J9 on the Trigger board. J8 and J9 connect to pulldown resistors. The instrument should stop triggering when this connection is made. If the instrument still triggers, then replace the Trigger board.

5. If the unit operates as an HP 54100A model and all self-test loops pass, then reinstall the Trigger Qualifier board and recable unit as a D model. Refer to figure 6D-6.

6. If loop 20 fails with the Trigger Qualifier board installed, it means the CPU did not recognize the Trigger Qualifer board as being installed. This will cause loops 43-60 to fail. Check the SIB for bent pins. If there are no bent pins, replace the Trigger Qualifier board.

7. Cycle the instrument's power off and then on. If any loops still fail, the problem is either a bad cable, bad Trigger Qualifier board, or the board's trigger calibration is too far out of tolerance. If the trigger calibration is too far out of tolerance, then TRIG4 will not be able to generate an output at TCLK4. Refer to the Adjustments, Section 4, paragraph 4-15. Adjustments R1-3 may need to be centered before doing the procedure. Only do adjustments R1-3 to verify that TRIG4 is producing a TCLK4. Some of the Trigger Qualifier board problems may make it impossible to obtain a display so R1-3 can be adjusted. If the cables are good, and repeating the adjustments on R1-3 does not solve the problem, then replace the Trigger Qualifier board.

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Many of the Trigger Qualifier board loops will run even without the other data acquisition boards on the SIB. Listed below are loops 43-60 and an indication if the loop will pass or fail with the other data acquisition boards removed, but with all coax cables still connected to the boards. The boards need not be removed from the instrument, just lifted high enough so they do not make contact with the SIB pins.

Loop	Pass or Fail	Loop	Pass or Fail
43	Pass	52	Pass
44	Fail	53	Pass
45	Fail	54	Pass
46	Fail	55	Fail
47	Pass	56	Fail
48	Pass	57	Fail
49	Pass	58	Pass
50	Pass	59	Pass
51	Pass	60	Pass

If all of the cables are removed, then loops 43-57 will fail and loops 58-60 will pass.

If a loop fails which is marked above as passing, then pull the data acquisition boards off the SIB and see if the loop now passes. If the loop passes, then one of the data acquisition boards is causing the loop to fail. Reinstall the data acquisition boards one at a time until the loop starts to fail again. This is probably the faulty board. Use the signal comparison Section to verify that the Timebase board is sending the correct signals over the coax cables.

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Table 6D-11. Signatures for Loop Failures (HP 54100A/D)

LOOP NUMBER	SIGNATURE NUMBER	PROBABLE CAUSE
0	6P1C	Processor
1	6P1C	Processor
2	86H2	Processor
3	H2H8	Processor
4	6F6P	Processor
5	6PCP	Display, Processor
6	UAHH	Display, Processor
7	5U2F	Display, Processor
8	7FC2	Display, Processor
9	HHCH	IO, Processor
10	82CP	IO, Processor
11	6U57	IO, Processor
12	H5H8	IO, Processor
13	5H82	IO, Processor
14	0AU9	IO, Processor, SIB, Power Supplies
15	5U3A	Sampler 1 and Sampler 2
16	3ACC	Sampler 1 or Sampler 2
17	768C	Timebase
18	45H9	Timebase
19	C370	Trigger
20	7023	Qqualifier
21	08U6	Trigger, Sampler 1, Sampler 2, Trigger Qualifier
22	PHHH	Trigger, Sampler 1, Sampler 2, Trigger Qualifier
23	HH9A	Trigger, Sampler 1, Sampler 2, Trigger Qualifier
24	9A02	Trigger, Timebase
25	0582	Trigger, Timebase
26	4FU4	Timebase
27	9P9H	Timebase, Sampler 1, Sampler 2, Trigger, Trigger Qualifier
28	9HUH	Timebase, Sampler 1, Sampler 2, Trigger, Trigger Qualifier
29	CUC7	Timebase
30	70PA	Sampler 1, Sampler 2, Trigger, Trigger Qualifier
31	PA20	Sampler 1, Sampler 2, Trigger, Trigger Qualifier
32	2096	Sampler 1, Sampler 2, Trigger, Trigger Qualifier
33	P66P	Sampler 1, Sampler 2, Trigger, Trigger Qualifier
34	F3C4	ADC 1 , ADC 2
35	A8F4	ADC 1 , Sampler 1, Sampler 2, Timebase, Trigger, Qualifier
36	F431	ADC 1 , Sampler 1, Sampler 2, Timebase, Trigger, Qualifier
37	3102	ADC 1 , Sampler 1, Sampler 2, Timebase, Trigger, Qualifier
38	4F6C	ADC 1, ADC 2
39	5C43	ADC 2, Sampler 1, Sampler 2, Timebase, Trigger, Qualifier
40	4337	ADC 2, Sampler 1, Sampler 2, Timebase, Trigger, Qualifier
41	377A	ADC 2, Sampler 1, Sampler 2, Timebase, Trigger, Qualifier
42	HHPC	Display

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Table 6D-12. Signatures for Loop failures (HP 54100D only).

LOOP NUMBER	SIGNATURE NUMBER	PROBABLE CAUSE
43	5PU7	Trigger Qualifier, Trigger, Sampler 1 or 2
44	U7AH	Trigger Qualifier, Trigger, Sampler 1 or 2
45	HA2F	Trigger Qualifier, Trigger, Sampler 1 or 2
46	1664	Trigger Qualifier, Trigger, Sampler 1 or 2
47	8PA1	Trigger Qualifier, Trigger, Sampler 1 or 2
48	A188	Trigger Qualifier, Trigger, Sampler 1 or 2
49	8893	Trigger Qualifier, Trigger, Sampler 1 or 2
50	9390	Trigger Qualifier, Trigger, Sampler 1 or 2
51	90CF	Trigger Qualifier, Trigger, Sampler 1 or 2
52	CF42	Trigger Qualifier, Trigger, Sampler 1 or 2
53	4222	Trigger Qualifier, Trigger, Sampler 1 or 2
54	22FC	Trigger Qualifier, Trigger, Sampler 1 or 2
55	4596	Trigger Qualifier, Trigger, Sampler 1 or 2
56	FC02	Trigger Qualifier, Trigger, Sampler 1 or 2
57	0201	Trigger Qualifier, Trigger, Sampler 1 or 2
58	OPU5	Trigger Qualifier, Trigger, Sampler 1 or 2
59	U58U	Trigger Qualifier, Trigger, Sampler 1 or 2
60	F7F5	Trigger Qualifier, Trigger, Sampler 1 or 2

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6D-21. TROUBLESHOOTING THE HP 54100A/D's DATA ACQUISITION SECTION

Introduction

There are several techniques that can be used when troubleshooting the Data Acquisition Section of the instrument. CRT displayed loop failures, channel isolation, and waveform comparisons may be used singularly or in tandem to isolate faulty boards.

Signature analysis is NOT used for testing the Data Acquisition Section. The CRT will supply the same information, as that obtained with signature analysis, when in the Display Errors mode. **If the CRT is not working, then that failure should be repaired prior to continuing.**

Procedure:

1. Execute the power-up self-test by one of the following methods:

   a. Apply power to the instrument and the self-test routines are executed automatically.

   b. Performing test 12 in the INTERFACE TESTS portion of the Test menu.

   c. HP-IB command TEST (TST) will trigger a power-up self-test. If a failure occurs error number -340 will be placed in the error queue. The error buffer may be read using the ERROR? command. Refer to Section 10 of the *HP 54100A/D Operating and Programming Manual.*

2. Display the loop failures by pressing the ***Utility*** key, ***Test menu*** key and then ***Display Errors*** key.

3. Refer to table 6D-11 or 6D-12 to determine which board is most likely causing the error to occur.

NOTE

Each of the Data Acquisition Section test loops (15-41) is dependent upon circuitry on several boards. If more than one loop failure is shown on the display, the boards should be replaced in the order of the failures.

It is strongly recommended that waveform comparison or channel-to-channel signal exchange be used to further isolate problems.

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6D-22. CHANNEL 1 AND 2 BOARD SWAP

The Sampling boards (A5/A7) and the ADC boards (A6/A8) of channel 1 and channel 2 are identical. If a problem is suspected on one of these boards, swap the suspected board to the opposite channel and determine if the problem follows the board.

6D-23. CHANNEL 1 AND 2 SIGNAL EXCHANGE

The IFout signal from either Sampling board can be an input to the ADC of the opposite channel. This technique is fast and effective if either channel can trigger on and display a signal.

Procedure:

1. Apply the two CAL signals to both input channels.

2. Press ***AUTO-SCALE*** key. If neither channel displays a triggered waveform, use the Loop failure tables or the waveform comparisons to troubleshoot.

3. Set the bad channel up as follows:
   Sensitivity +100 mV/div
   Offset -215 mV
   Mode normal

4. Remove the IFin cable (J1) from both of the ADC boards. Connect the cable from the bad channel to the ADC board of the opposite channel. Change the trigger source to the bad channel and set trigger level to -215 mV. If a stable triggered signal appears on the CRT, the Sampling board of the bad channel is working and the problem is with the ADC board.

   If no signal appears, make sure that the Sampling board is receiving MCLK before replacing the board.

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6D-24. WAVEFORM COMPARISON

The clocks and signals that must go between boards are ported by 50 Ω coaxial cables. With the adapter cables supplied in the Product Support Kit (P/N 54100-69002) these signals may be applied to an oscilloscope. The observed waveforms can then be compared to figures 6D-14 through 6D-21.

Install HP 54002A probe pods in channels 1 and 2. To duplicate the waveforms shown, apply the two CAL signals to the inputs of both vertical channels and press ***AUTO-SCALE***.

Check that the HP 54100A/D has configured itself as follows. If not, change settings to the following:

```
Chan 1 & 2

  Display     - On
  Sensitivity - 100 mV/div
  Offset      - -215 mV

Timebase

  Sec/Div     - 50 ns/div
  Delay       - 0 s
  Delay Ref   - Center
  Sweep       - Auto

Trigger

  Mode        - Edge
  Slope       - Pos
  Holdoff     - 70 ns
  Level       - -215 mV
```

With a SMB to BNC adapter cable connect the signal to be tested to the input channel of the oscilloscope.

The waveforms were taken with the FULL BRIGHT test pattern found in the CRT CAL menu. To access this test pattern, make the following key selections:

Utility
CRT CAL
FULL BRIGHT

NOTE

Do NOT probe these test points with the oscilloscope in the 50 Ω input impedance position.

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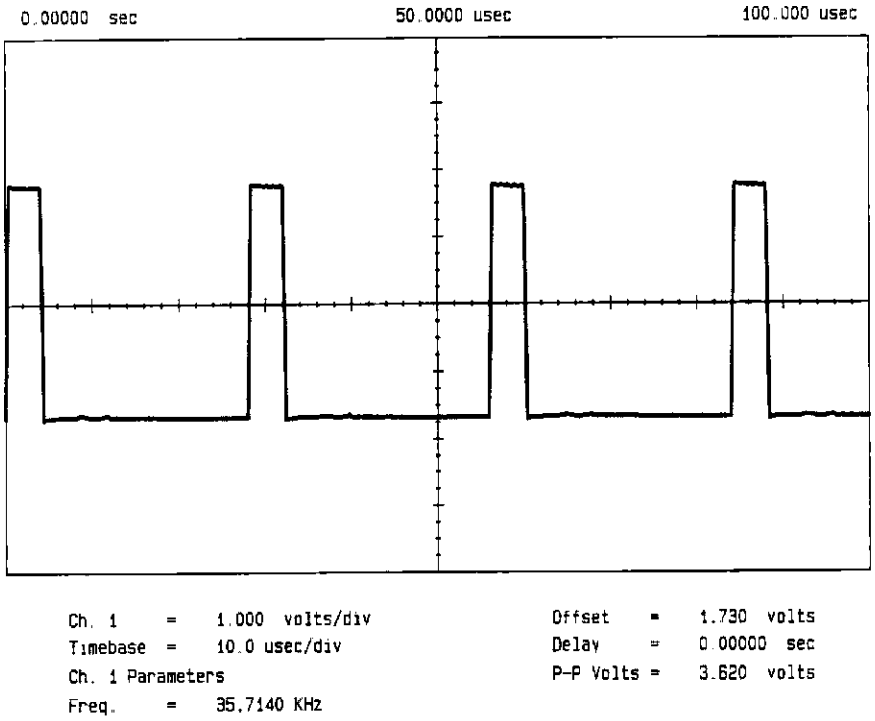


Figure 6D-14. Waveform at A2TP4 with FULL BRIGHT Test Pattern Selected.

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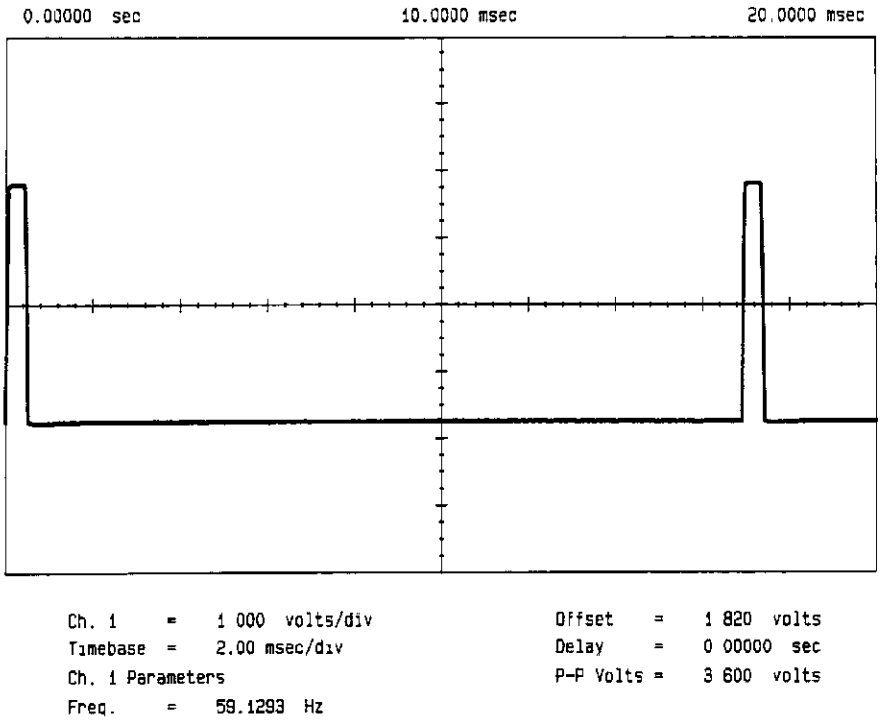


Figure 6D-15. Waveform at A2TP5 with FULL BRIGHT Test Pattern Selected.

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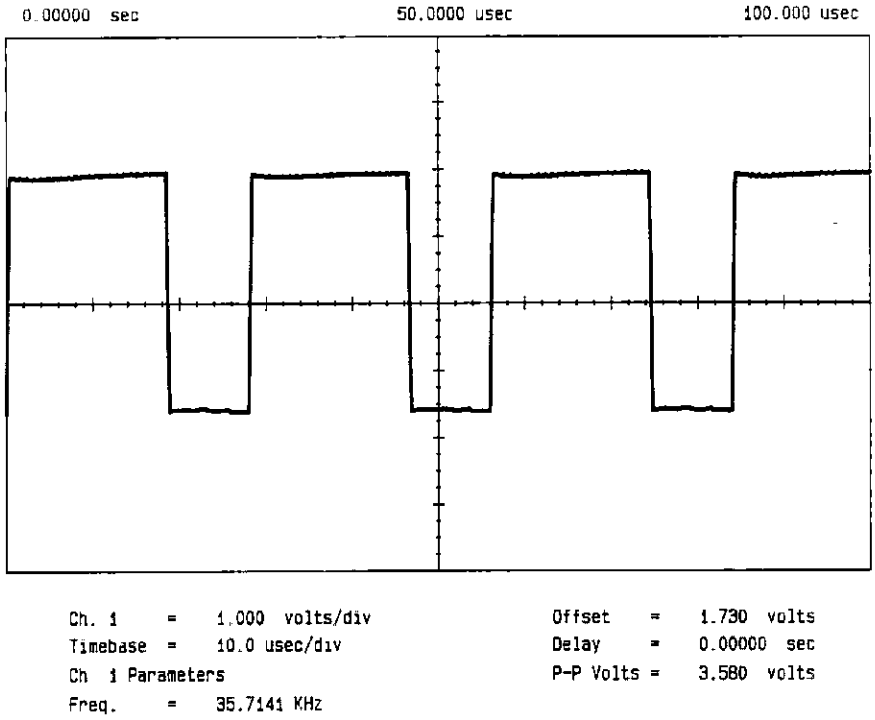


Figure 6D-16. Waveform at A2TP6 with FULL BRIGHT Test Pattern Selected.

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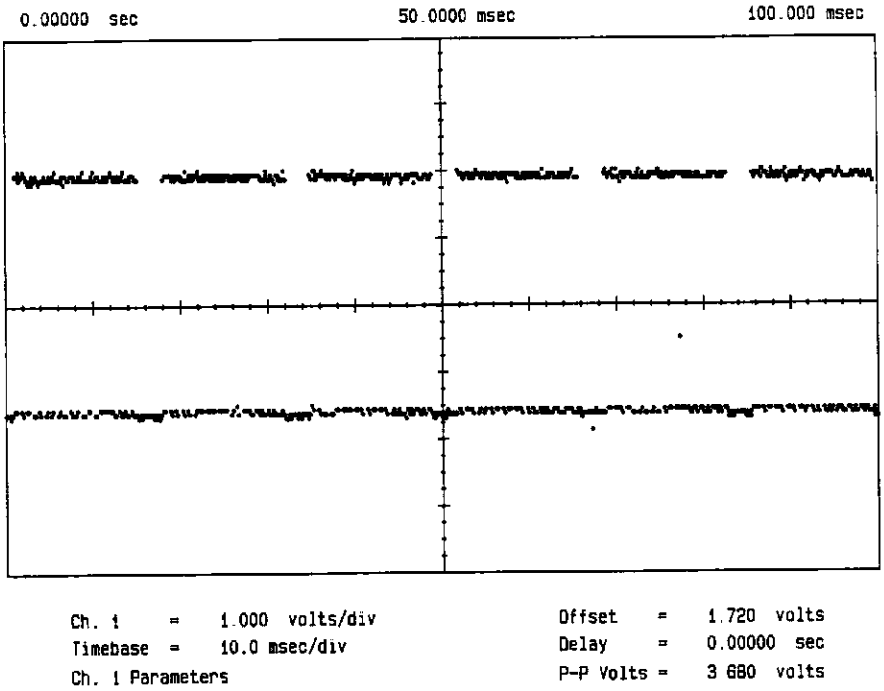


Figure 6D-17. Waveform at A2TP6 or A2TP7 with FULL BRIGHT Test Pattern Selected.

NOTE

The monitor oscilloscope must be triggered on A2TP5.

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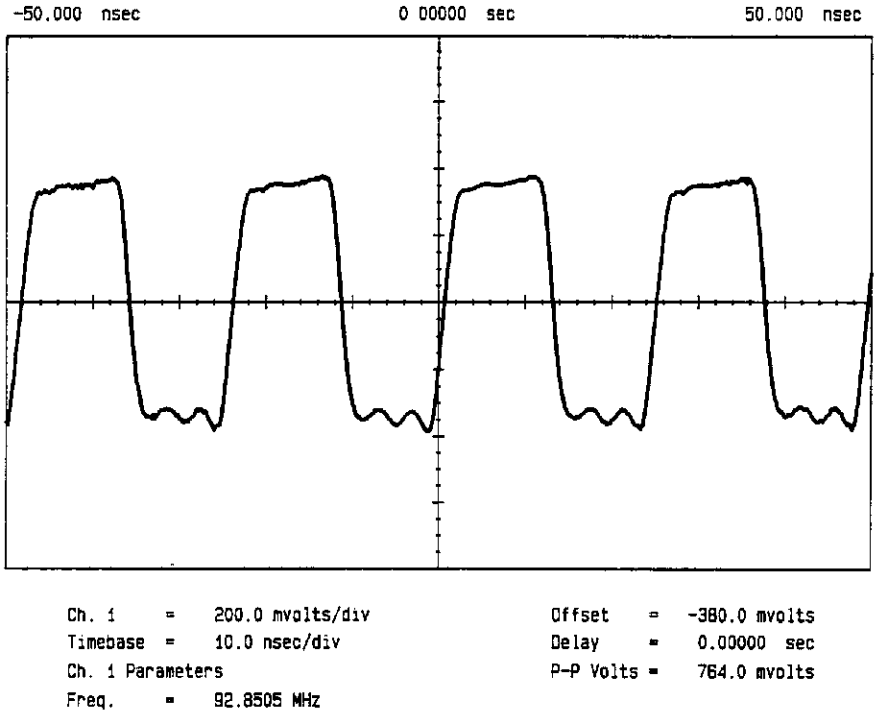


Figure 6D-18. Waveform on the A4 MCLK (Master Clock) Cables.

NOTE

This waveform must be terminated in 50 Ω, the CAL signal must be applied to both channel 1 and 2, and the oscilloscope must be configured as shown on page 6D-38.

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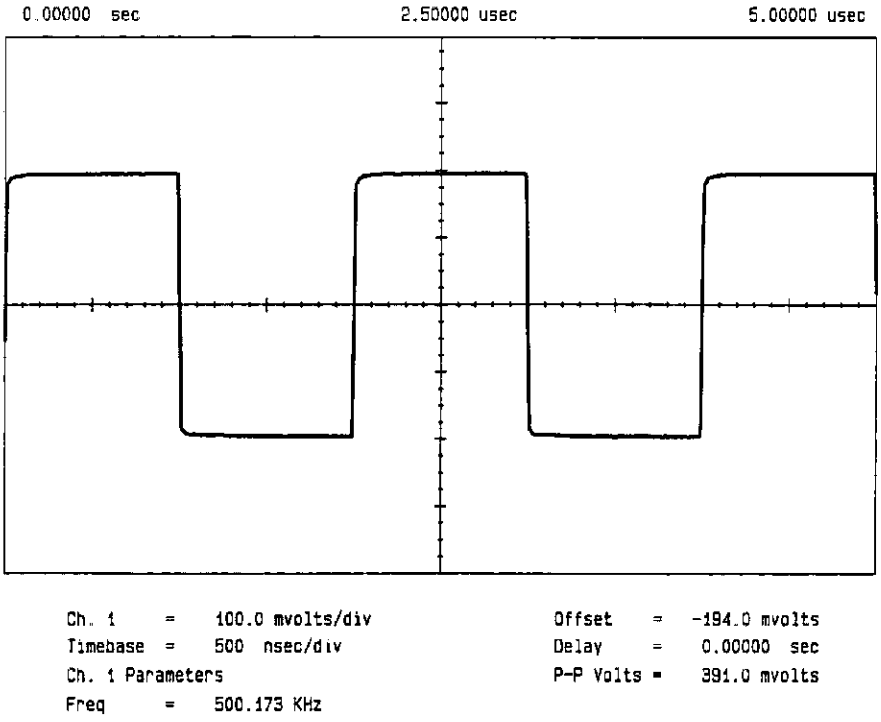


Figure 6D-19. Waveform on the A4 CAL (CAL signal) Cables.

NOTE

This waveform must be terminated in 50 Ω, the CAL signal must be applied to both channel 1 and 2, and the oscilloscope must be configured as shown on page 6D-38.

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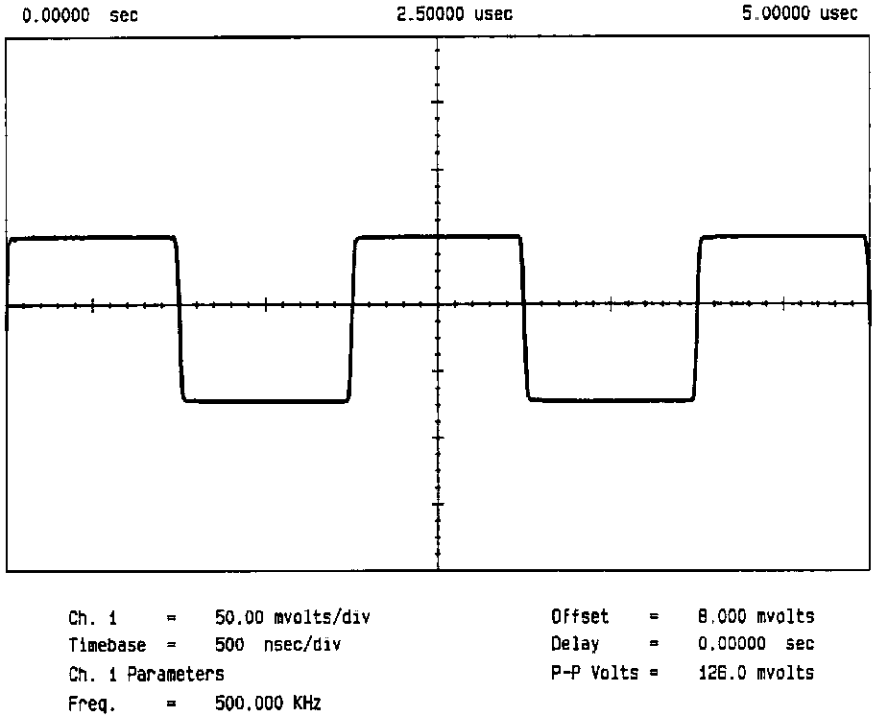


Figure 6D-20. Waveform on the A5/A7 IFout Cables.

NOTE

This waveform must be terminated in 50 Ω, the CAL signal must be applied to both channel 1 and 2, and the oscilloscope must be configured as shown on page 6D-38.

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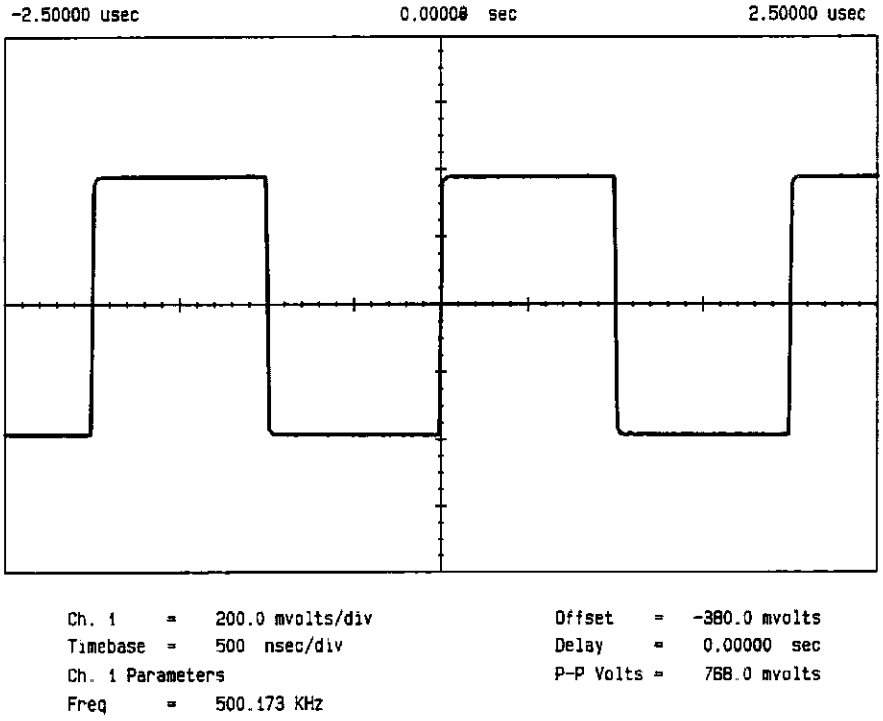


Figure 6D-21. Waveform on the A5/A7 TCLK (Trigger Clock) Cables.

NOTE

This waveform must be terminated in 50 Ω, the CAL signal must be applied to both channel 1 and 2, and the oscilloscope must be configured as shown on page 6D-38.

NOTE

The trigger level must be set to -215 mV with the CAL signal applied.

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6D-25. DETERMINING VALID EDGE TRIGGERING PATHS

During some troubleshooting routines it is advantageous to know which edge triggering paths are working properly. The procedure below verifies edge triggering paths for each trigger source.

1. Connect rear panel Cal signal to channel 1 with a BNC cable.
2. Press ***AUTO-SCALE*** key.
3. If AUTO-SCALE does not pick up the signal, then channel 1 trigger path does not work.
4. Set trigger source to channel 1.
5. Set trigger level to -200 mV.
6. The message "Running" should appear in the top left corner of the display, if this trigger path is working.
7. Move BNC cable from channel 1 to channel 2.
8. Change trigger source to channel 2 and set trigger level to -200 mV.
9. The message "Running" should appear in the top left corner of the display, if this trigger path is working.
10. Move BNC cable from channel 2 to external trigger, channel 3.
11. Change trigger source to channel 3 and set trigger level to -200 mV.
12. The message "Running" should appear in the top left corner of the display, if this trigger path is working.
13. Move BNC cable from external trigger channel 3 to external trigger qualifier, channel 4.
14. Change trigger source to channel 4 and set trigger level to -200 mV.
15. The message "Running" should appear in the top left corner of the display, if this trigger path is working.

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6D-26. LOOPS 61, 62, and 63.

Loops 61-63 are **not** executed during the following sequences:

Normal power-up routines
Run from loop 0
Interface test 12

These loops will **not** affect the power-up self-test pass or fail message.

Loop 61 Loop 61 will show up on the cummulative errors Section of the Display Errors message when interface test 10 fails.

Loop 62 Loop 62 will show up on the cummulative errors Section of the Display Errors message when interface test 15 fails.

Loop 63 Loop 63 will show up on the cummulative errors Section of the Display Errors message when the first power-up after the Cal Factors is lost. This will occur for the following reasons.

Two key-down power-up is executed.

Microprocessor board is removed from SIB pins.

A new Microprocessor board is installed.

I/O board is removed from SIB.

A new I/O board is installed.

The battery on the I/O board is bad or has been disconnected.

The motherboard has been removed from the instrument.

Any other interruption of power to the battery backed-up RAM on the Microprocessor board which contains the Cal Factors.

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6D-27. HP-IB ERROR CODES.

The following table identifies which HP-IB error code will be displayed for each loop failure.

Table 6D-13. HI-IB Error Code Listing for Loop Failures.

Loop	HP-IB Bus Error	Loop	HP-IB Bus Error	Loop	HP-IB Bus Error
0	-302	20	-370	40	-360
1	-321	21	-370	41	-360
2	-311	22	-370	42	Not Used
3	-311	23	-370	43	-360
4	-350	24	-360	44	-360
5	-370	25	-370	45	-360
6	-370	26	-370	46	-360
7	-311	27	-370	47	-360
8	-311	28	-370	48	-360
9	-370	29	-370	49	-360
10	-301	30	-370	50	-360
11	-301	31	-360	51	-360
12	-370	32	-370	52	-360
13	-370	33	-360	53	-360
14	-399	34	-370	54	-360
15	-370	35	-360	55	-360
16	-370	36	-360	56	-360
17	-370	37	-360	57	-360
18	-370	38	-370	58	-360
19	-370	39	-360	59	-360
				60	-360

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SECTION 6E

INTERNAL DIAGNOSTICS

6E-1 INTRODUCTION

This Section contains information concerning each of the 60 internal diagnostic Loop Tests. Each loop contains a description as well as a diagnostic tree for replacement to the board level (and sometimes to the component level). Each loop is divided up into five sections:

1. Description:
   This explains the basic operation of the loop. It gives the user an idea of what functional blocks are involved and how they are involved.

2. Status Register:
   Many loops use the four status registers on the DISPLAY ERRORS menu. This section describes their meaning.

3. Possible Causes of Failures:
   This section indicates the adjustments that can cause this loop to fail, the boards that could cause this loop to fail, and the functional blocks that if not working properly can cause these loops to fail. Adjustments should be checked early in the troubleshooting process as many repairs of this instrument will need only adjustment. The CPU, I/O, and SIB must work properly or all loops may fail. This is why those boards are checked first (ie. have lower number assigned to them). The functional blocks section can be used to help isolate the failure when more than one loop fails (as is the usual case).

4. Fault Diagnostics:
   This section contains troubleshooting information to the board level. Occassionally, it also gives component level failure information and many times it gives only partial component information. If the technician had more information and schematics, he could find the actual faulty component.

The loops have been set up in order of importance, the lower the loop number, the more general the loop. It is possible for higher numbered loops to fail because a lower number loop failed. Therefore, when troubleshooting the loop, it is advised to start with the lowest loop first. All troubleshooting diagnoses for loops depend on the loop being executed in the REPEAT LOOP fashion. This is described in Section 6C-9. REPEAT LOOP will indefinately (at user's command) run the loop to its end and start it over again and again. Most loops (in the short run) have stable and repeatable loop execution times. Therefore, repetitive type oscilloscopes can be used for probing. However, between executions, many loops may change in overall execution time. All loops have certain time units assigned to them, so that if the loop does not execute in that time, the loop is stopped and a failure message is put on screen. Many loops are timing loops where the CPU uses a software counter to time between a start event and an interrupt of the processor. Table 6E-1 indicates typical loop execution times.

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NOTE

These times were computed on a March 1986 version of the HP 54100 firmware, and should be very similar on all other versions. The purpose is to give an idea of when to look for reoccurring events on multiple executions of a particular loop. Knowing this will make it easier to pick accurate trigger points. The digital loops were not characterized because they are entirely different in the two models.

Table 6E-1. Loop Execution Times (to two significant digits).

Loop	Execution	Time	Loop	Execution	Time
Loop 00	180	µs	Loop 30	4600	µs
Loop 01	N/a		Loop 31	4900	µs
Loop 02	N/a		Loop 32	4700	µs
Loop 03	N/a		Loop 33	4700	µs
Loop 04	540	µs	Loop 34	93	µs
Loop 05	100	µs	Loop 35	140000	µs
Loop 06	100	µs	Loop 36	140000	µs
Loop 07	100	µs	Loop 37	140000	µs
Loop 08	100	µs	Loop 38	93	µs
Loop 09	360	µs	Loop 39	140000	µs
Loop 10	3100	µs	Loop 40	140000	µs
Loop 11	580	µs	Loop 41	140000	µs
Loop 12	120	µs	Loop 42	11800	µs
Loop 13	20000	µs	Loop 43	4400	µs
Loop 14	99	µs	Loop 44	4400	µs
Loop 15	92	µs	Loop 45	3400	µs
Loop 16	92	µs	Loop 46	2400	µs
Loop 17	93	µs	Loop 47	2300	µs
Loop 18	710	µs	Loop 48	2500	µs
Loop 19	105	µs	Loop 49	2800	µs
Loop 20	102	µs	Loop 50	3000	µs
Loop 21	60	µs	Loop 51	3200	µs
Loop 22	5600	µs	Loop 52	9800	µs
Loop 23	3200	µs	Loop 53	10000	µs
Loop 24	700	µs	Loop 54	16700	µs
Loop 25	100	µs	Loop 55	2600	µs
Loop 26	1100-1500	µs	Loop 56	2600	µs
Loop 27	3100	µs	Loop 57	2600	µs
Loop 28	6400	µs	Loop 58	2600	µs
Loop 29	100	µs	Loop 59	2000	µs
			Loop 60	1600	µs

Often in the troubleshooting section of the loop, signals may appear on the screen that look the same but have slightly different timing. This is the result of the variation of loop execution time.

Most of the loops use the LIACK signal (TP1 on CPU Board) as the trigger source. This is used because at the end of every loop, LIACK is pulled low. Therefore, whenever a trigger source is not mentioned in the section or is said to be external, the source is LIACK (at a trigger level of 1.2 V) unless specifically stated otherwise.

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6E-2. ANALOG TEST LOOP GENERAL INFORMATION

Holdoff (Loops 21,23,30,31,32,33,43, etc)

These loops start out by testing some independent blocks, and then use these in testing other, dependent blocks. The first to be tested is the holdoff section of the main Trigger board. This is needed because many of the other tests go through this circuitry. The holdoff can be selected for either time or events. In time holdoff, the counter recognizes 100 MHz clock edges. In events holdoff, it recognizes actual trigger clocks from either the external trigger or the samplers. The first edge it sees will put the circuit into holdoff and it will count down edges until it reachs terminal count, after which the circuit enables the fast trigger flip-flop (F/F). The first trigger after terminal count is the trigger event that starts the rest of trigger hardware running. This same trigger event also resets the holdoff counter and the cycle begins again. Refer to the Trigger board block diagram in Section 6B-12. There is a status bit that reflects the state of the holdoff counter. It is used in many of the loops as an indication that triggers are being received.

NOTE

The holdoff counter is not reliable for the first down counting after loading. All tests using holdoff poll and wait for holdoff to be enabled by one of two methods: by time, waiting for holdoff by time and by events, simulating triggers for down counting. Loops may fail occassionally without there being a problem in the instrument.

Triggers & Sync Amps

By disabling all three sync. comparators, the HP 54100A/D trigger system may be isolated from an external trigger source. It is a good indication of a Sync amp problem if there are loop failures dependent on whether or not there is a signal connected to a particular channel. Triggers can be simulated by three different means. First, toggling the POS/NEG bits on the sync comparators. Second, toggling the invert line. Third, by switching the trigger level DAC's output between ± fullscale with the inputs at virtual ground. When not testing the POS/NEG edge attribute of the sync comparators, they are set to NEG. The software anticipates the state of the inactive sync amps polarity bit to be set to negative. If they are not set to negative, or their terminations are inadequate, this will cause loop failures. The mechanism for this is that the trigger clocks are ORed together producing a low state for the clock of the fast trigger flip-flop. This flip-flop recognizes positive edges, and the software is set up to produce them. If one of the trigger clocks is not low, then on some tests the trigger will be 150 degrees out of phase (Loops 21, 23, etc.), other loops will not be able to simulate a trigger (Loops 30, 32, etc.).

Sampler Board

A Sampler board has one programmable attenuator on it. This device has four bits, one each for X10, X5, and X2 attenuation and one that will open the input path between the input and the attenuator stages. By turning off all stages and opening the input path, the output of the device is essentially grounded. This allows the machine to test both the trigger level DAC (as above, in Loops 31, 33, and tests 10, 15), the offset DAC and ADC system (Loops 35, 36, 37, 39, 40, 41).

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Serial Strings

All Analog boards (except ADCs) are controlled by serial data strings. On the samplers they are regular bit mapped and sign-magnitude notation. However, the Trigger and Timebase board counts are represented on Johnson Gray code. The strings are shifted in by a number of consecutive points with the data on D0. The strings are latched by a write (or read) pulse, except for timebase strings, where the toggling of a parallel control bit (RUN/STOP) latches in the string.

LIACK And The Hardware Interrupt Mask

At the address 88001H on the Microprocessor board resides an 8-bit latch that is an interrupt mask for the seven levels (D1-D7) and a bit called LIACK. LIACK stands for Local Interrupt ACKnowledge. The loops use LIACK as a Start/Stop clock for some DSA loops. It is also used as the Start/Stop for loop identification when a hardware jumper is placed on interrupt 7 (see TROUBLESHOOTING WITH NO DISPLAY section 6D-18 of this manual for more information).

Polling of STATUS BITS

Many of the loops poll various bits of the different status bytes on the analog boards. To insure that the software does not get hung-up waiting for a stuck status bit to change state, software timeout down counters are used in these situations. These counters are set at a much longer count than the expected execution time. Therefore, if there are failing loops of this type, it will probably take a much longer time to power up than normal. It takes approximately four seconds for the instrument to go through its powerup self-test initialization.

INIT Routine

A routine called init is called at the beginning of most loops. This routine performs some overhead functions to make the loops function properly. It does things like set the loop number, disable the HP-IB and the keyboard, mask the hardware interrupt timer, and calculate all needed addresses.

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Known Failed Board Troubleshooting

Occasionally, a technician may know what board is bad and will want to do more troubleshooting on it. Refer to table 6E-2. It indicates which loops exercise which boards. In addition, it also indicates which loops are the most thorough in checking out that board.

Table 6E-2. Which Loops Exercise Which Boards.

Board	Loops Which Exercise the Board
I/O	Loops 9-14
DISPLAY	Loops 5-8
CPU	Loops 0-4
TIMEBASE	17,18,24,25,26-29 (most important 18,26,27) MASCLK Generator T/S (see Section 6E-3).
SAMPLER	Loops 15,16,30-33, 35-41 (most important ch1 = 30,35; ch2 = 31,39)
ADC	Loops 34-41 (most important 35 for channel 1 and 39 for channel 2) High Speed Timing T/S (see ADC Troubleshooting Section 6E-9).
TRIGGER	Loop 21-25,27,28,30-33 (most important 23)
TRIGGER QUALIFIER	Loops 43-60 (most important 43)

6E-3. TIMEBASE TROUBLESHOOTING

In addition, the Timebase board has circuitry that is indirectly checked by the loops. It is wise to check the operation of this board more fully to get a better idea of what is failing in the instrument. The following probing points are offered for doing this. The oscilloscope is not in any loop for this exercise. It is turned on using the 2 key down power up routine (see Section 6C-5) and placed in the triggered mode. Probe the following test points and compare waveforms with those shown in figures 6E-1 through 6E-9.

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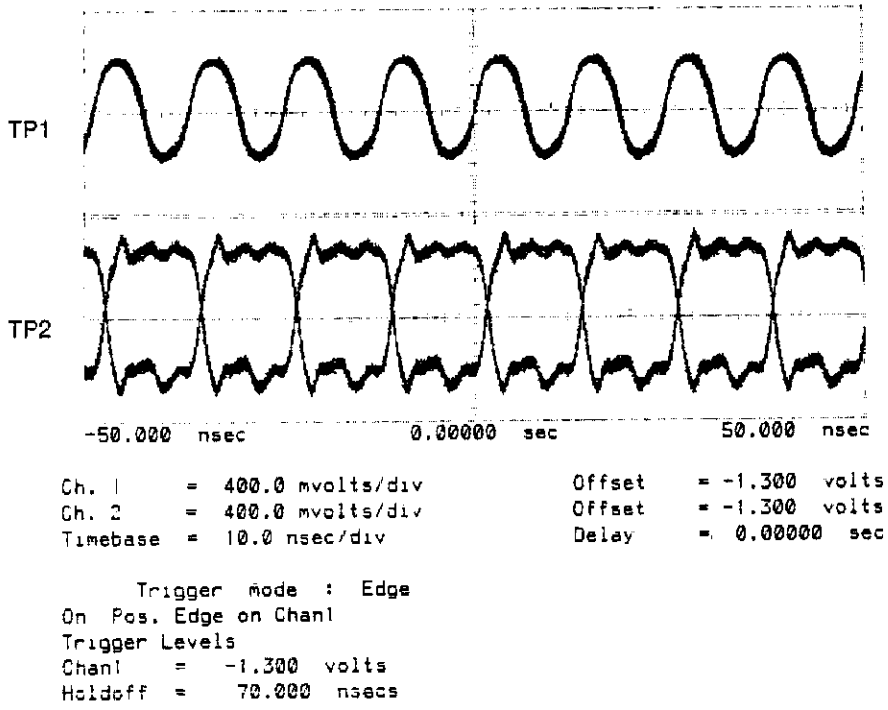


Figure 6E-1. Timebase Troubleshooting Waveforms at TP1 and TP2.

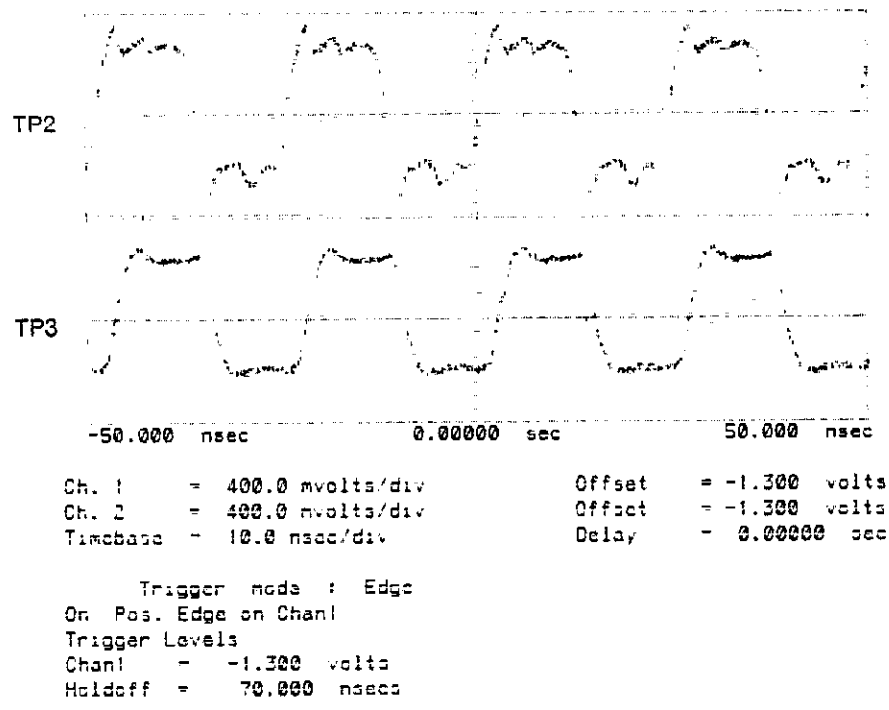
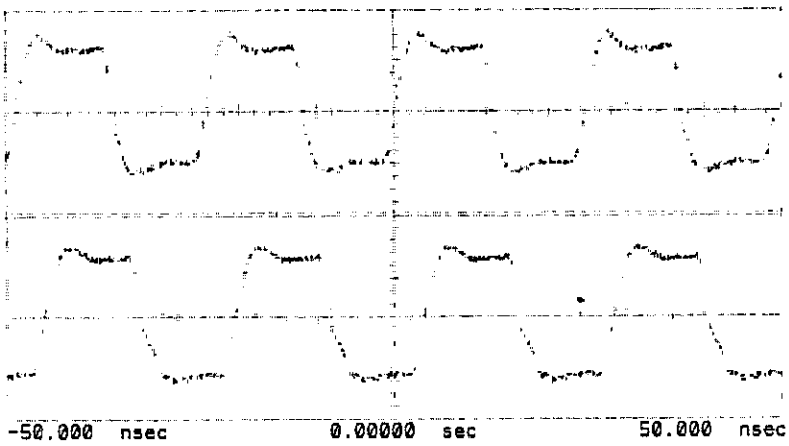


Figure 6E-2. Timebase Troubleshooting Waveforms at TP2 and TP3.

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TP3

TP5



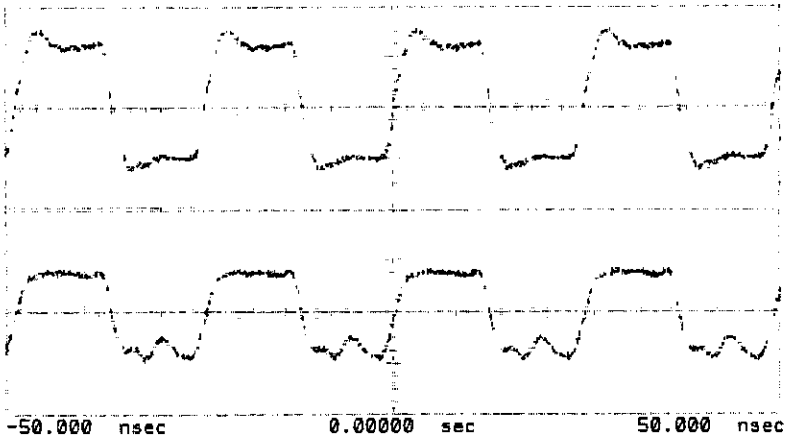

```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  10.0 nsec/div             Delay      =  0.00000  sec

      Trigger mode  :  Edge
On  Pos. Edge on Chan1
Trigger Levels
Chan1     =   -1.300  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-3. Timebase Troubleshooting Waveforms at TP3 and TP5

TP3

U8 Pins 1, 3, 15




```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0  mvolts
Timebase   =  10.0 nsec/div             Delay      =  0.00000  sec

      Trigger mode  :  Edge
On  Pos. Edge on Chan1
Trigger Levels
Chan1     =   -1.300  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-4. Timebase Troubleshooting Waveforms at TP3 and U8 Pins 1, 3, 15.

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TP3

U32 Pin 15

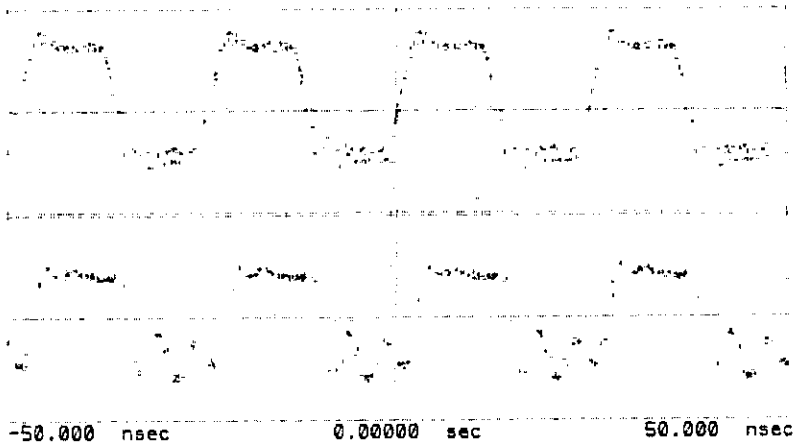


Figure 6E-5. Timebase Troubleshooting Waveforms at TP3 and U32 Pin 15.

TP3

U19 Pin 7

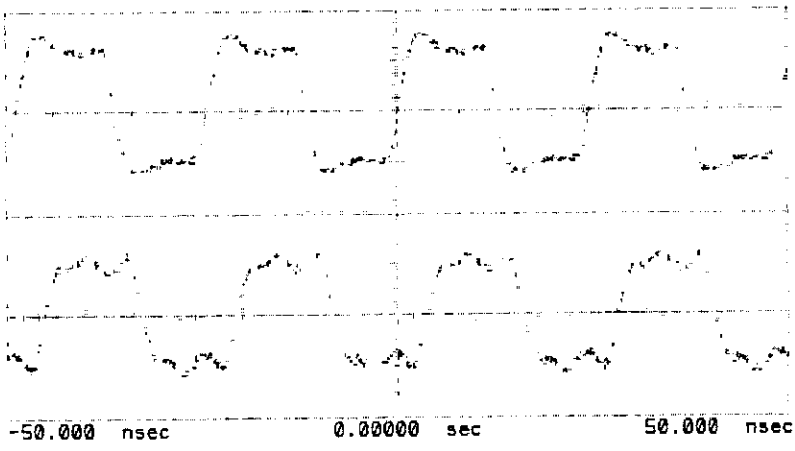


Figure 6E-6. Timebase Troubleshooting Waveforms at TP3 and U19 Pin 7.

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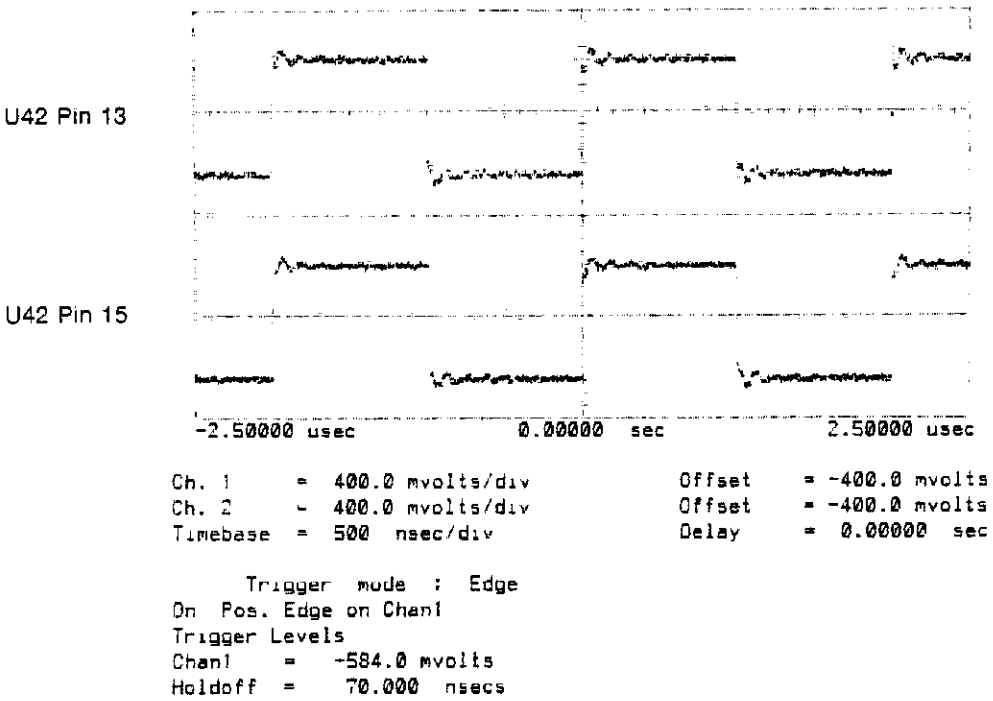


Figure 6E-7. Timebase Troubleshooting Waveforms at U42 Pins 13 and 15.

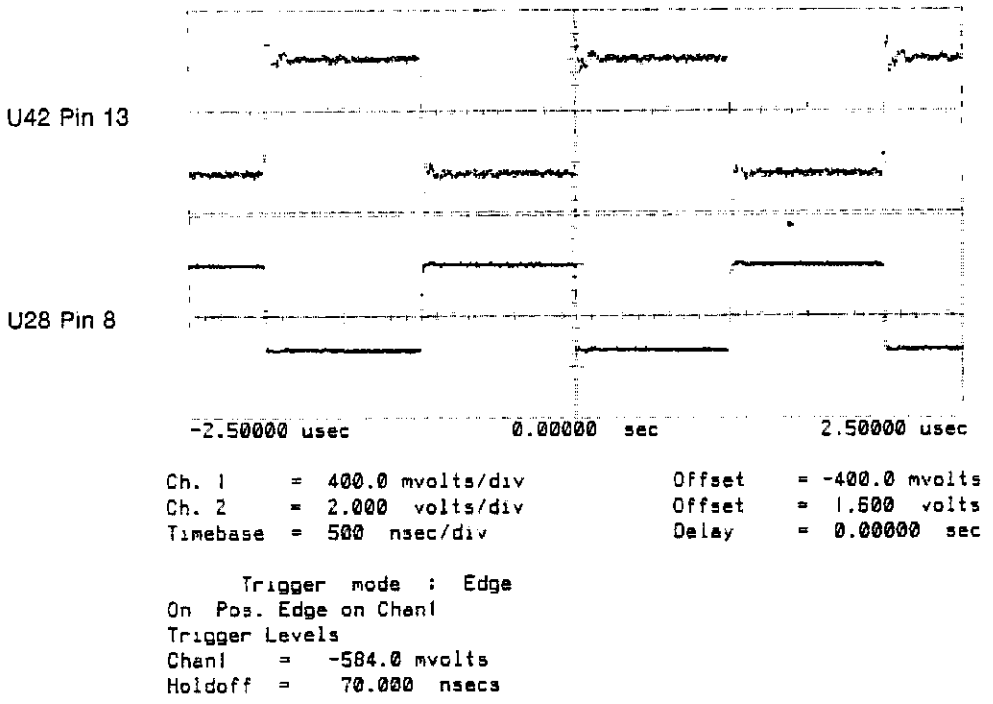


Figure 6E-8. Timebase Troubleshooting Waveforms at U42 Pin 13 and U28 Pin 8.

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6E-4. LOOP NUMBERS AND LOOP NAMES

Table 6E-3 cross references loop numbers to the main purpose of the loop. This is for the more experienced technician for quick reference purposes.

Table 6E-3. LOOP NUMBER vs LOOP NAME.

Loop	Name	Loop	Name
0		30	Sampler 1 Pos/Neg Edge Trigger
1	Rom Checksum	31	Sampler Trigger Level DAC
2	Static Ram 0	32	Sampler 2 Pos/Neg Edge Trigger
3	Static Ram 1	33	Sampler 2 Trigger Level DAC
4	Counter Timer Chip	34	ADC1 ID
5	Display ID	35	Sampler 1 -Trigger Level DAC=0
6	CRT Controller (R/W)	36	Sampler 1-Trigger Level DAC=+1/2
7	Read/Write Character RAM	37	Sampler 1-Trigger Level DAC=-1/2
8	Read/Write Graphics RAM	38	ADC2 - ID
9	I/O ID	39	Sampler 2 - Trigger Level DAC = 0
10	Overload Interupt Filter	40	Sampler 2-Trigger Level DAC=+1/2
11	System Interupt Latch	41	Sampler 2-Trigger Level DAC=-1/2
12	HP-IB Chip	42	Not Used
13	KEY Board Chip	43	Qualifier Pos/Nex Edge Trigger
14	Power Detect	44	Pattern Enter/Exit
15	Sampler 1 and Sampler 2 ID	45	State Present/Not Present
16	Sampler 1 or Sampler 2 ID	46	Delay By Events (Load=0)
17	Timebase ID	47	Delay By Events (Load=1)
18	Pre-Trigger Delay	48	Delay By Events (Load=2)
19	Trigger ID	49	Delay By Events (Load=3)
20	Qualifier ID	50	Delay By Events (Load=4)
21	Trigger Holdoff by Time	51	Delay By Events (Load=5)
22	Trigger Holdoff by Events	52	Delay By Events (Load=36)
23	Trigger SYNC Comparator-Pos/Neg	53	Delay By Events (Load=37)
24	Fine Interpolator	54	Delay By Events (Load=69)
25	Fine Interpolator Clear	55	Delay By Time = 825 μs
26	Sample Rate Generator	56	Delay By Time > 825 μs
27	Post Trigger Delay	57	Delay By Time < 825 μs
28	Coarse Interpolator	58	TCLK Disable @ Edge Mode
29	Coarse Interpolator Clear	59	QCLK Disable
		60	TCLK Disable @ Pattern Present > 10 ns

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6E-5. DATA ACQUISITION CONTROL STRINGS

The Microprocessor board in the HP 54100A/D sets up the Data Acquisition boards to acquire waveform data Once the Data Acquisition boards are told what to do, the CPU then signals the Timebase board to begin the acquisition process. The microprocessor communicates these setups to the various boards, through the use of serial control strings.

The HP 54100A contains seven serial control strings, and the HP 54100D contains eight. Below is a description of each of these control strings. Each description contains the following information: Order of entry onto board, bit number of each bit, purpose of each bit location on the boards, where to probe to assure the proper information was received, and the board that the string is sent to.

The HP 54100A/D uses one channel string for each Sampler board.
The ADC board does not contain any serial data strings.

The data acquisition strings are loaded in from right to left. For example 001000H is read in 000000000000100000000000 (The first zero is shifted in first and the last zero in the string is shifted in last).

Table 6E-4. List of Serial Control Strings.

Sampler Board Channel String (Serial Data at U34 Pin 2)

	Bit No.	Function	Location
First In	0-9	Trigger Level	U39 P 1-10
	10	Trigger Level Sign (Neg/LPos)	U39 P 18
	11	Trigger Scope (Neg/LPos)	U37 P 14
	12	Trig Enable (low enable)	U37 P 7
	13-23	13 23 Offset	U36 P 18, U36 P 1-10
	24	X2 (low true)	U34 P 14
	25	X5 (low true)	U34 P 7
	26	X10 (low true)	U34 P 6
	27	Close Attn (low true)	U34 P 5
	28	Dither Line	U34 P 4
Last In	29-31	Not Used	

Trigger Board Trigger String (Serial Data at U29 Pin 2)

	Bit No.	Function	Location
First In	0-9	Trigger Level	U27 P 1-10
	10	Trigger Level Sign (Pos/LNeg)	U27 P 18
	11	Trigger Slope (Pos/LNeg)	U29 P 14
	12	Trigger Enable (low enable)	U29 P 7
	13	Invert	U29 P 6
Last In	14-31	Not Used	

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Table 6E-4 (continued). List of Serial Control Strings.

Trigger Board Holdoff String

	Bit No.	Function	Location
First In	0-1	00 = Unused, 01=Time, 10=Events, 11 = Option Source	TP1, U3 P13
	2-28	Holdoff	U19 P3 Serial Data
Last In	29-31	Not Used	

Timebase Board Timebase String Word 2 (Serial Data String at U7 Pin 5)

	Bit No.	Function	Location
First In	0-16	Post Trigger (7-23)	U4 P3 Serial Data
Last In	17-31	Not Used	

Timebase String Word 1 (Serial Data String at U7 Pin 5)

	Bit No.	Function	Location
First In	0-23	Pre Trigger (0-23)	U5 P3 Serial Data
	24	Not Used	
Last In	25-31	Post Trigger (0-6)	U5 P3 Serial Data

Timebase String (Word 0)

	Bit No.	Function	Location
First In	0	0=Enable=25 ns	U6 P3 Serial Data
	1	Not Used	
	2	2 0=Enable>25 ns	U6 P3 Serial Data
	3-6	Sample Rate A (fast counter)	U6 P3 Serial Data
	7-30	Sample Rate B (slow counter)	U6 P3 Serial Data
Last In	31	31 Not Used	

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Table 6E-4 (continued). List of Serial Control Strings.

Trigger Qualifier Board Compartor Control String

	Bit No.	Function	Location
First In	00-9	Trigger Level	U27 P 3-10, U27 P 2,1
	10	Trig Level Sign (pos/I neg)	U27 P 18
	11	Trig Scope (pos/I neg)	U1 P 18
	12	Trig Enable (low enable)	U1 P 7
Last In	13-15	Not Used	

Trigger Qualifier Board Mode Control String (Serial Data at U36 Pin 2)

	Bit No.	Function	Location
First In	0-23	C6-C29	U37 P11,CL3 dc
	24	CL37	U37 P11,CL3 dc
	25	CL37	U37 P11,CL3 dc
	26	CL5	U37 P11,CL3 dc
	27	C2	U37 P11,CL3 dc
	28	C3	U37 P11,CL3 dc
	29	C4	U37 P11,CL3 dc
	30	C5	U37 P11,CL3 dc
	31	CL3	U37 P11
	32	LCO	U37 P10
	33	C1	U37 P6
	34	Submode	U37 P5
	35	DLYD	U37 P4
	36	Istate	U37 P3
	37-40	LE1-LE4	U36 P10-13
Last In	41-44	LS1-LS4	U36 P3-6

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6E-6. RECOMMENDED TEST EQUIPMENT

The recommended test equipment for troubleshooting the internal diagnostic loop tests is listed in table 6E-5.

Table 6E-5. Recommended Loop Test Troubleshooting Test Equipment.

Instrument	Critical Specifications	Recommended Model
Scope	300 MHz, 2 Channels External Trigger	HP 54201A
Signature Multimeter	No Substitute	HP 5005B
DVM	None	HP 3465A

6E-7. INTERFACE TEST #10

Description

This test operates exactly like Loop 3, except that the trigger events are simulated by toggling the Trigger board's trigger level DAC from rail to rail rather than the sample's trigger level DAC. The number of events loaded into the holdoff counter is 11 events instead of 10. This test is not run at power-up, but can be run by the user to verify the trigger level DAC on the Trigger board. This tests no other circuitry than is already tested in other loops. To determine if this test passes, press ***DISPLAY ERRORS*** after stop test. If loop 62 is displayed, then the test failed, otherwise it passed.

Status Register:

Same as Loop 31.

Possible Causes of Failure:

Same as Loop 31 except add the trigger level DAC of the Trigger board instead of the Sampler board.

Fault Diagnosis:

Same as Loop 31 plus probing TP7 on Trigger board with channel 1 and U1 pin 14 on trigger board with channel 2, which should give the following result: (Trig on LIACK 1 - TP1 on CPU):

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6E-8. INTERFACE TEST #15

Description:

This test operates exactly like loop 31 except that trigger events are simulated by toggling the Trigger Qualifier board's trigger level DAC from rail to rail rather than the sample's trigger level DAC. The number of events that is loaded into the holdoff counter is 11 events instead of 10. This test is not performed at power-up, but can be run by the user to verify the trigger level DAC (it tests no other circuitry than is already tested in other loops). To determine if this test failed, press ***DISPLAY ERRORS*** after stop test. If loop 61 is displayed, then the test failed. Otherwise, it passed.

Status Register:

Same as loop 31

Possible Causes of Failure:

Same as loop 31 except using the qualifier's trigger level DAC instead of the sampler's.

Fault Diagnosis:

Same as loop 31 plus probing TP8 on qualifier board with channel 1 and U1 pin 14 on the qualifier's board with channel 2 should give the following result: (Trigger source is LIACK - TP1 on CPU). Use same picture as interface test 10.

6E-9. ADC BOARD TROUBLESHOOTING

Interface Tests #13 and 14:

Interface tests #13 and 14 use digital signature analysis to thoroughly check the ADC boards. This is needed for component level repair of this board, but it can be used to help isolate the board in some cases.

High Speed Timing Verification:

Perform a 2-key down power-up, then probe the following points.

TP3	TP7
TP4	TP8
TP5	TP9
TP6	TP10

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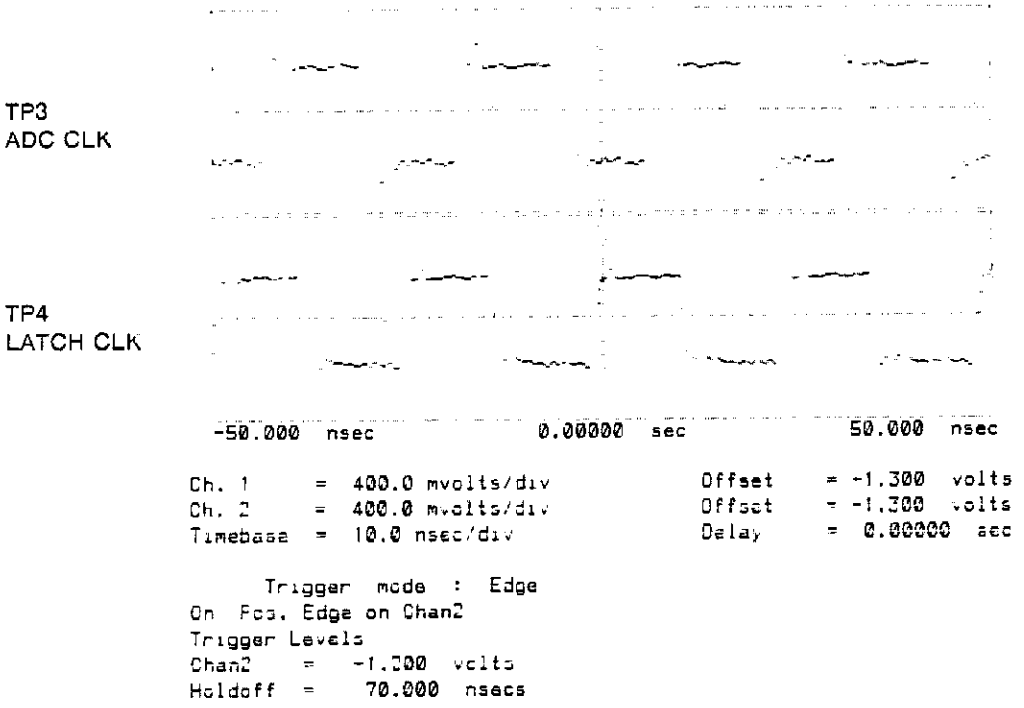


Figure 6E-9. ADC Troubleshooting Waveforms at TP3 and TP4.

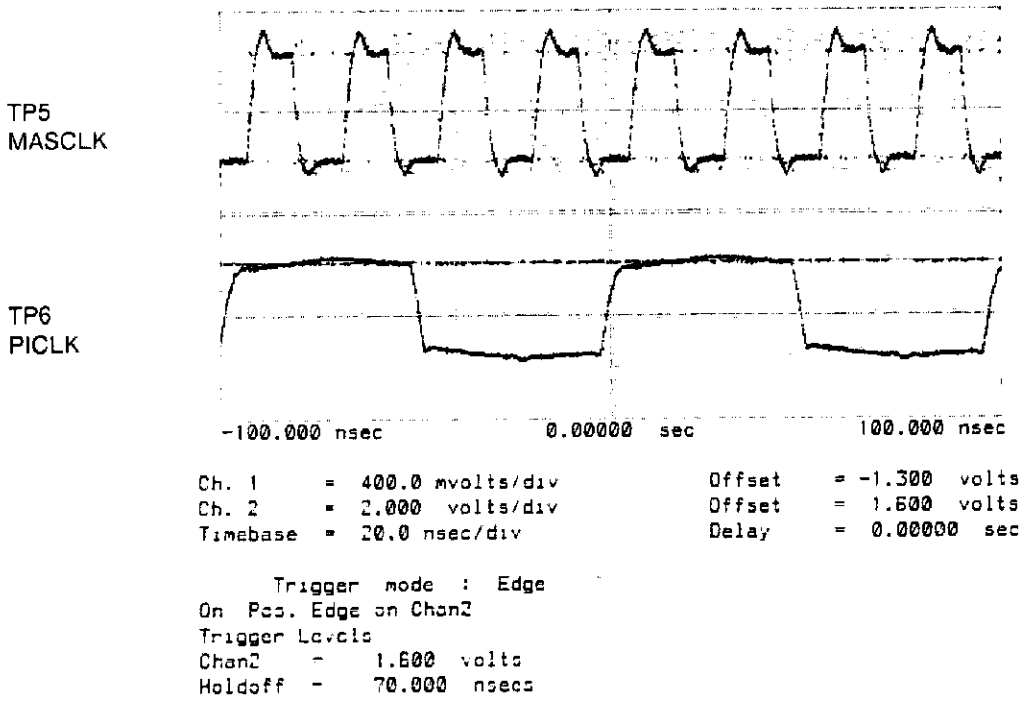


Figure 6E-10. ADC Troubleshooting Waveforms at TP5 and TP6.

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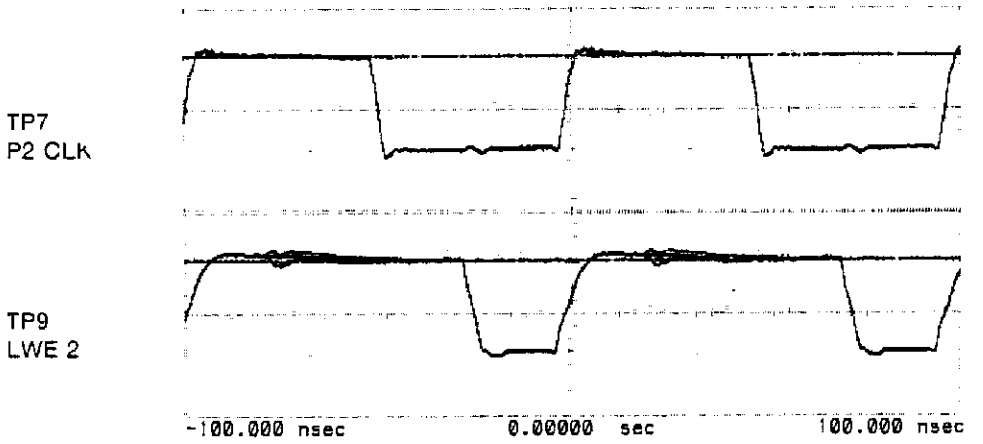


Figure 6E-11. ADC Troubleshooting Waveforms at TP7 and TP9.

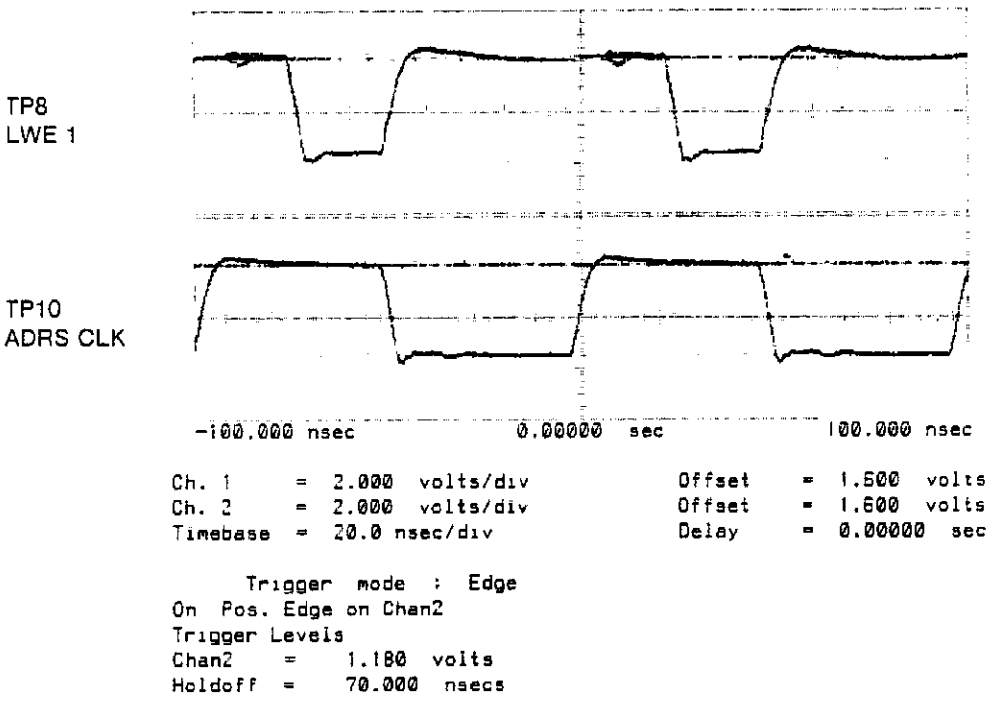


Figure 6E-12. ADC Troubleshooting Waveforms at TP8 and TP10.

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6E-10. LOOP 0

BUSERROR

Description:

This loop tests the BUSERROR circuitry by sending a request to the bus that will not be responded to; therefore, the BUSERROR circuitry should fire. The CPU times the length of time it takes to fire and compares it to a known time limit. The test fails if it never fires or if its response time is out of specification. If this test fails, all of the other tests will fail.

Status Register:

No indications.

Possible Causes of Failure:

1. Adjustments indicated - none
2. Boards indicated - I/O, CPU, SIB, any board can load the signal down.
3. Functional blocks indicated - BUSERROR circuitry, SIB, Address/Data/Control bus of CPU.

Fault Diagnosis:

Remove all boards from the SIB except the CPU and I/O. Re-power the oscilloscope and run REPEAT LOOP 0. If it fails then, the cause is either on the CPU, I/O, or SIB. Suspect the I/O board first. (The SIB troubleshooting tests can be performed to verify proper operation of the SIB.)

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6E-11. LOOP 1

ROM Checksum:

Description:

This test computes a checksum on the program ROMs and compares its result with what was stored in the ROMs at program development. If the numbers are different the test fails.

Status Register:

No indications.

Possible Causes of Failure:

1. Adjustments indicated - none.
2. Boards indicated - CPU, I/O (if pullups are not operating).
3. Functional blocks indicated -
   Program ROM, Address Bus, Data Bus, and Control Bus.

Fault Diagnosis:

Check the following circuit components.
- Bent Pins on ROMs
- If this loop fails on its own, check and replace all bad ROM's

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6E-12. LOOP 2

Static RAM 0 Checkerboard:

Description:

Same as Loop 3 except RAM 0 is tested (U15 and u32).

Status Register:

No indications

Possible Causes of Failure:

Same as Loop 3 except RAM 0 instead of RAM 1

Fault Diagnosis:

Same as Loop 3 except look at U15 and U32

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6E-13. LOOP 3

Static RAM 1 Checkerboard

Description:

This test writes an alternating set of O's and 1's into RAM1 (U16, U33). It then reads this data back and looks for discrepancies. It then inverts all the bits in the memory and looks for discrepancies again.

Status Register:

No indications.

Possible Causes of Failure:

1. Adjustments indicated - none
2. Boards indicated - CPU, I/O (If pullups are bad).
3. Functional blocks indicated - Data bus, Control Bus, Address Bus, RAM 1.

Fault Diagnosis:

If this loop fails by itself, replace U16 and U33.

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6E-14. LOOP 4

Counter Timer Chip (CTC)

Description:

This test loads each of the three CTC counters with a known value and starts them counting at three different times. Each counter should timeout at different times and interrupt the CPU before the other two counters do.

Status Register:

STATUS #1 - COUNTER O , VALID = 0
STATUS #2 - COUNTER 1 , VALID = 1
STATUS #3 - COUNTER 2 , VALID = 2
STATUS #4 - N/A

An error response of 255 indicates that there was no interrupt for that timer. A number other than the valid response indicates that one of the other timers on that chip interrupted instead of the one the loop was looking for.

Possible Causes of Failure:

1. Adjustments indicated - none
2. Boards indicated - CPU or I/O (If pullups are not operating).
3. Functional blocks indicated -
   Data shifting on Data Bus Addressing problem. CTC. 2MHz Clock. Interrupt priority encoder.

Fault Diagnosis: Check the following circuit points on the CPU board.

```
TP15
U2 Pin 21

U2 Pin 21
U40 Pin 8
```

Make sure that the following points are TTL Highs on the CPU board:
U2 Pin 20, U2 Pin 19, U40 Pin 9, U17 Pin 13

This test requires more down time after power off then the other loops. If it fails, re-cycle power (downtime at least 3 sec) to assure failure.

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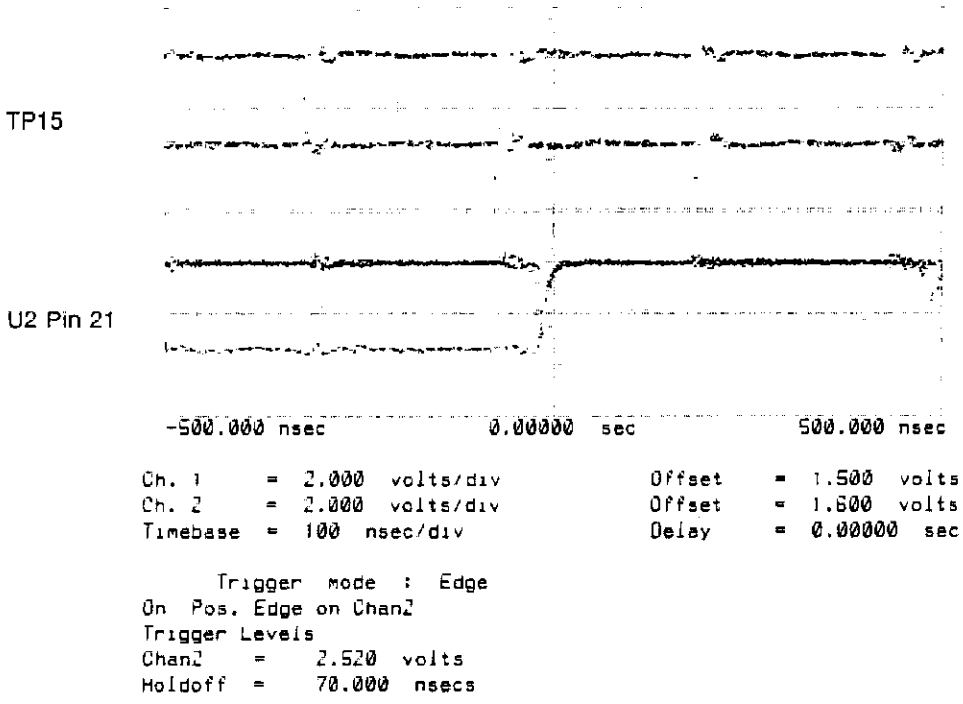


Figure 6E-13. Loop 4 Troubleshooting Waveforms at TP15 and U2 Pin 21.

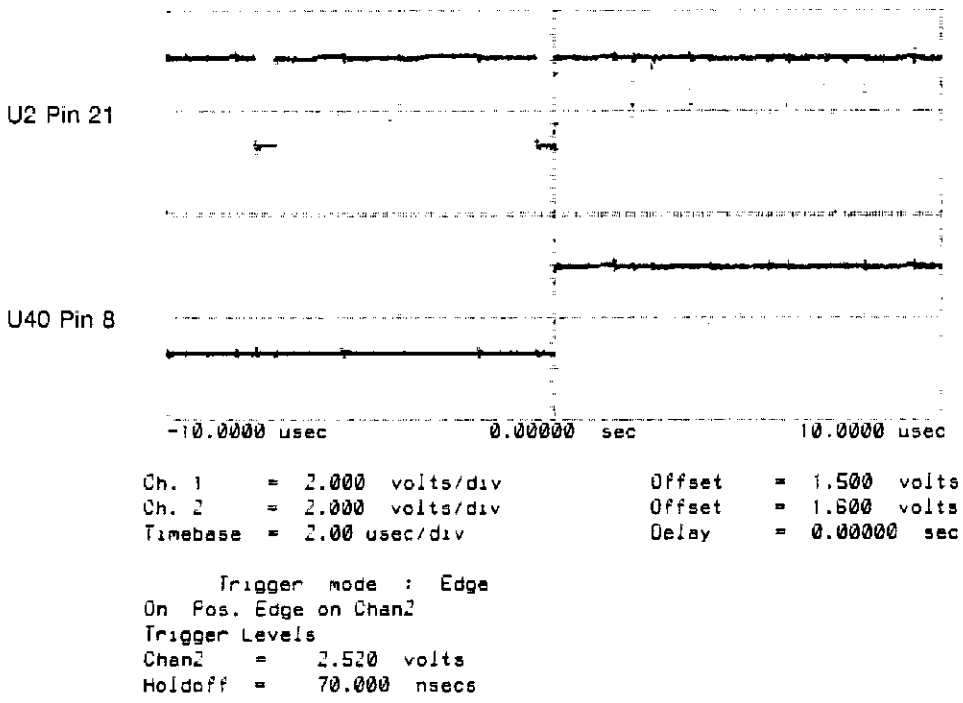


Figure 6E-14. Loop 4 Troubleshooting Waveforms at U2 Pin 21 and U40 Pin 8.

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6E-15. LOOP 5

Display ID

Description:

This test is exactly like Loop 15 in that it uses CONFIGURE to verify the response of the Display board.

Status Register:

No Indications

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - Display
3. Functional blocks indicated - SIB, all board CPU interfaces, and Display board.

Fault Diagnosis:

Same as Loop 15 except especially on Display board.

Troubleshooting Tree:

1. Place Display board on extender.
2. Follow steps 2 through 6 in the fault diagnosis section of loop 15.

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6E-16. LOOP 6

CRT CONTROLLER READ/WRITE

Description:

This loop tests the Display boards Read/Write controller. If this test fails, then the unit will probably come up with no display.

Status Register:

STATUS #1 - Read/write data to CRT controller - 26 is correct.
STATUS #2 - #4 - N/A

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - Display, CPU, I/O (If pullups are not operating).

Fault Diagnosis:

If this test fails, replace the Display board.

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6E-17. LOOP 7

READ/WRITE CHARACTER RAM:

Description:

This test sends a checkerboard of alternating 0's and 1's to the display RAM. After sending this pattern, the CPU then reads it back and checks for correctness. The pattern is then inverted and written and read again.

Status Register:

STATUS #1 - ADDRESS OF 0555H ERROR
STATUS #2 - ADDRESS OF 0AAAH ERROR
STATUS #3 - ADDRESS OF 0AAAH ERROR
STATUS #4 - ADDRESS OF 0555H ERROR

All of these numbers are offsets from the base of the character RAM. The first two represent the first checkerboard and the second two the second checkerboard. Valid range for all is 0 to 8190H (even only). They represent the last address found with an error.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - Display, CPU, I/O (If pullups are not operating).
3. Functional blocks indicated -

Fault Diagnosis:

If this test fails, replace U43, 44, and 45 on the display board. If this does not fix the problem, replace the entire Display board.

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6E-18. LOOP 8

READ/WRITE GRAPHICS RAM:

Description:

This test is exactly like Loop 7 except the Graphics RAM on the Display board is tested instead of the character RAM.

Status Register:

Same as loop 7 except the valid range is 0 to 1300H (even only).

Possible Cause of Failure:

Same as Loop 7 except in reference to Graphics RAM not character RAM.

Fault Diagnosis:

If this loop fails, replace the entire Display board due to the large number of possible RAMs that could be causing the failure.

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6E-19. LOOP 9

I/O ID:

Description:

This is exactly like Loop 15 except the I/O is checked for presense and response.

Status Register:

No indication.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - I/O or CPU
3. Functional blocks indicated - SIB, all board CPU interfaces, especially I/O board.

Fault Diagnosis:

Same as Loop 15 except as related to I/O board.

Troubleshooting Tree:

1. Put the I/O board in the extender.
2. Follow steps 2 through 6 of the Fault Diagnosis section for Loop 15.

6E-20. LOOP 10

OVERLOAD INTERRUPT FILTER:

Replace the I/O board.

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6E-21. LOOP 11

SYSTEM INTERRUPT LATCH:

Description:

This loop tests the toggling ability of each of the system interrupts. If any of the interrupts do not work, then the test fails. The status word will indicate the interrupt that is not working.

Status Register:

STATUS #1 - Last execution of the Loop
STATUS #2 - Last time it failed
STATUS #3, #4 - N/A

The ERROR word returned is weighted with Bits 0 through 6 corresponding to interrupts 1 through 7, respectively. A 63 is Valid with all Bits Set.

Possible Cause of Failure:

1. Adjustments indicated - None

2 Boards indicated - CPU, I/O

3. Functional blocks indicated - ADDR, DATA, CONTROL Bus System, Interrupt Latch, Priority Encoder.

Fault Diagnosis:

Execute REPEAT LOOP 11. Probe the following points for a 50 μs negative pulse width. Each of these points will be slightly delayed in time from each other: SIB pins 94, 96, 97, 98, 99.

SIB pins 95 and 100 should be a TTL high level.

If all of these points are correct, than the I/O board is doing its job. Therefore, replace the CPU board. Otherwise replace the I/O board.

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6E-22. LOOP 12

HP-IB Chip:

Description:

Status Register:

STATUS #1 - HPIB Status Byte, Normally = 4
STATUE #2, #3, #4 - N/A

This loop is looking for a status bit to be set. The decimal number is 4 or 16 Base 10.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - I/O or CPU
3. Functional blocks indicated - HP-IB Chip or Drivers

Fault Diagnosis:

None

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6E-23. LOOP 13

Keyboard Chip:

Description

Status Register:

STATUS #1 - Keyboard controller chip's status byte, normally=16
STATUS #2, #3, #4 - N/A

This test is looking for a status bit to reset. The decimal number is bit weighted, and is bit-4 or 16 base 10.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - I/O or CPU
3. Functional Blocks indicated - Keyboard Chip

Fault Diagnosis:

None.

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6E-24. LOOP 14

Power Detect:

Description:

This Loop is looking for a Power Failure status bit to be set by a piece of hardware on the I/O board. In order to be working properly, the ±5 V, ±8 V, and ±18 V power supplies must be operating within the tolerances set by the I/O board circuitry.

Status Register:

N/A

Possible Causes of Failure:

1. Adjustments indicated - None

2. Boards indicated -
   Digital Power Supply
   Analog Power Supply
   Primary Power Supply
   I/O
   CPU
   Motherboard
   Power Supplies located on all boards.
   Power Supply interface on all boards.

3. Functional Blocks indicated - Power Supplies, Power-on-circuitry, SIB

Fault Diagnosis

1. Measure ±5 V, ±8 V, and ±18 V on the analog and digital power supplies. They should be within the following tolerances.

Power Supply	DC Voltage Tolerance
+5 V	+5.1 V ±.1 V
-5 V	-5.3 V ±.1 V
+8 V	+8.9 V ±1 V
-8 V	-8.5 V ±1 V
+18 V	+18.5 V ±.3 V
-18 V	-18.5 V ±1 V

   If one of the supplies is missing, refer to the Power Supply Troubleshooting, Section 6D-11.

2. Put I/O board on extender (remember Loops 0 and 9 will fail but that will not affect this test).

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3. Measure the following points on the I/O board.

SIB Point	DC Voltage
U13 Pin 9	+5.1 V ±.1 V
U13 Pin 11	-5.3 V ±.1 V
U22 Pin 7	+8.9 V ± 1 V
U13 Pin 4	-8.5 V ±1 V
U22 Pin 5	+18.5 V ±.3 V
U13 Pin 6	-18.5 V ±1 V

If these points are correct, the problem is on the I/O board or CPU board - See Step 5 and 6. Otherwise, use Step 7.

5. Probe U18 Pin 2 on CPU board for a TTL HIGH. If this signal is present, then the CPU is bad.

6. Probe the following points for the signals listed below. If any of these points are dissimilar, then the I/O board is faulty. If these points are all good then the failure is on the SIB, Motherboard, or another board which uses the IRQ Line. See Step 8.

U2 Pin 10	TTL HIGH
U2 Pin 9	TTL HIGH
U4 Pin 2	TTL HIGH
U7 Pin 3	400 mV
U31 Pin 12	TTL HIGH

7. Determine why the I/O board is not obtaining its power supplies. Suspect the SIB, Motherboard, connectors, or traces on the I/O Board.

8. Disconnect all boards from the SIB one at a time until the incorrect waveforms in Step 6 appear correct. Replace the board that caused this loading. If none of the boards fix the waveforms, suspect the SIB connector or the Motherboard.

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6E-25. LOOP 15

Sampler 1 ID

Description:

This test does not actually exercise any hardware, but rather it tests whether the Sampler board is responding to "CONFIGURE", a routine which polls all slots to see what board is located in each of the slots.

Status Register:

No Indications.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - Loop 15 will fail only if the unit cannot recognize both Sampler boards. This is the case because, the unit sees the first Sampler board in the card cage as Sampler 1
3. Functional blocks indicated - SIB, all board CPU interfaces especially SAMP1 and SAMP2.

Fault Diagnosis:

Check the following common problems.

Bent pins anywhere on Motherboard, especially in the sampler 1 and 2 slots.
Reseat all boards after checking for corrosion on connectors.

Troubleshooting Tree:

1. Put the failing sampler on the Extender board.
2. Enter the "DISPLAY CONFIGURATION" mode and verify the presence of that board in the slot. The machine polls the slots from left to right looking from the front of the unit.
3. If the board is not located in the display configuration menu, try reseating the board.
4. If both 2 and 3 fail, then determine the slot number where the board is (0-9). Select interface test #X, where X is the slot number. Press the ***Start Test*** key. This test will continually read the ID code of the selected slot.
5. Refer to the section entitled "INTERFACE TESTS 0-9" located in the troubleshooting, Section 6D-4, of this manual.
6. If 5 does not locate the problem, there may be an SIB problem. Refer to the section entitled "Proposed Method for Troubleshooting SIB problem", in this section of the manual.

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6E-26. LOOP 16

Sampler 2 ID

Description:

This test does not actually test any hardware. Rather, it tests whether the Sampler board responds to "CONFIGURE", a routine which polls all of the slots to see what is contained in the slots.

Status Register:

No indications.

Possible Causes of Failure:

1. Adjustments indicated - none
2. Boards indicated - This loop will fail if either sampler 1 or 2 is not responding.
3. Functional blocks indicated - SIB, all board CPU interfaces, especially, samplers 1 and 2, and CPU interface logic.

Fault Diagnosis:

Check the following common problems.
Bent pins on any slot of the Motherboard, especially SAMP1 and SAMP2.
Reseat all boards after checking for corrosion on connectors.

Troubleshooting Tree:

1. Determine the faulty Sampler board by removing one of the samplers and running "REPEAT LOOP 15". If this loop fails, then the sampler remaining in the card cage is the problem.
2. Follow diagnosis steps 2 through 6 found in Loop 15 for futher verification of the faulty board.

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6E-27. LOOP 17

Timebase ID:

In addition this loop also performs another exercise in a loop called 17A. Loop 17A should be examined before Loop 17 because 17A is executed before 17.

Description:

This test is exactly the same test used in test Loop 15 except that it looks for the presense of the Timebase board.

Status Register:

No indications.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - Timebase
3. Functional Block(s) indicated - SIB, any of the boards' CPU interfaces, especially the Timebase board.

Fault Diagnosis:

Same as Loop 15.

Troubleshooting Tree:

1. Put the Timebase board on the extender.
2. Follow steps 2 through 6 found in Loop 15.

LOOP 17A

This is not a test, nor is it a routine which polls to see if the boards are in their slot. It is a setup routine that sets the Sampler board in the following setup for the remaining tests.

Attenuators grounded.
Sync comparator Hybrid disabled and slope set to positive.
Trigger level DAC set to maximum positive.

If this part of the test fails, there is no feedback to the user. The only way to know the results is to manually see if the operations were performed after the "STOP TEST" key is pressed.

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6E-28. LOOP 18

Timebase Pre-Trigger Delay and TENBL:

This loop has two parts: 18, 18A. Loop 18A is executed before 18 and thus it should be examined before Loop 18. See Loop 18A section.

Description:

This test sets a known count into the Pre-Trigger delay counter. When the delay times out, the TENBL line will make a high to low transition. This action also sets the TENBL Bit in the TIMEBASE status register which when polled by the CPU will advise the CPU when the timeout occurred. The CPU then compares the time it took to timeout (as counted by a software counter) to a limit value to determine pass or fail. The software counter also has a timeout should the Pre-Trig delay counter get stuck and never assert TENBL.

The Pre-Trigger delay counter is 24-Bits wide and is loaded with a Hex count of 0020H. The clock used to count down this value is the 500 KHz clock and thus the delay is 64 μs. The data is latched in with a Run/Stop Bit toggle (load while stopped, set to run, set to stop). And the counting begins the next time the run is executed.

Status Register:

STATUS 1.....Downcounter typical 3 to 6, -1 indicates a timeout of a software counter
STATUS 2.....N/A
STATUS 3.....N/A
STATUS 4.....N/A

The valid range for STATUS 1 is from 0 to 7.

Possible Causes of Failure:

1. Adjustments indicated - 81.699 MHz Master Oscillator.

2. Boards indicated - Timebase

3. Functional Blocks indicated -
   RUN/STOP
   TENBL
   3 TIMEBASE CONTROL STRINGS
   TIMEBASE STATUS REGISTER
   LIACK
   PRE-TRIG DELAY COUNTER
   TENBL
   CPU OVERHEAD (See beginning section)

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Fault Diagnosis:

Ensure Master Oscillator at TP1 on timebase is a 81.699 MHz sine wave.
Check 500 KHz clock at U5 Pin 8 and Pin 9.
Check delay between negative edge of RUN/STOP (TP7) negative edge on TENBL (U34 Pin 13). It should be around 64 μs.

RUN/STOP toggling
LIACK toggling

Probe the following points.

Fig. 6E-11	U5 Pin 1 TP9	LRUN/STOP CNTR OUT (TENBL)	
Fig. 6E-12	U5 Pin 1 U5 Pin 8	LRUN/STOP (Pre-trigger clock)	These two are not sync'd
Fig. 6E-13	U5 Pin 1 U5 Pin 3	LRUN/STOP Data In	

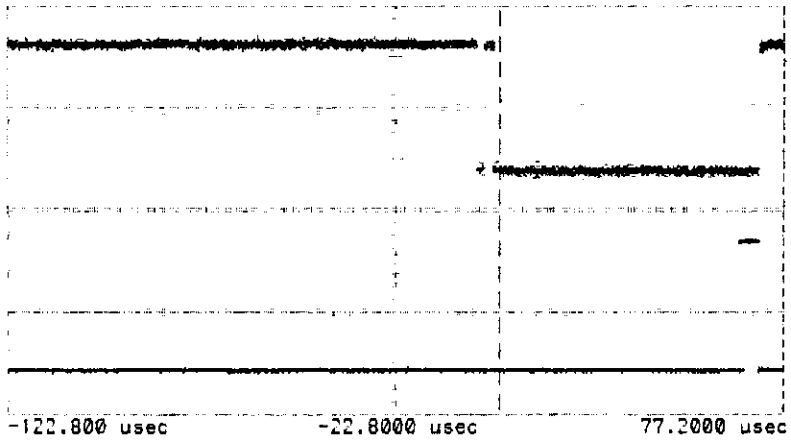
LOOP 18A

This loop determines whether or not the boards needed for Loop 18 are in the correct slots.

Test 18A looks for the Timebase board. If the Timebase board is not responding, Loop 18 is not executed. In addition, a Loop 18A failure does not appear on screen and should be assumed if Loop 18 is bypassed without executing.

You can verify that Loop 18A is failing by running a REPEAT LOOP 18 for 30 seconds. Then press ***STOP TEST*** key. If Loop 18A is failing, the status line on the screen will display some other loop number than 18.

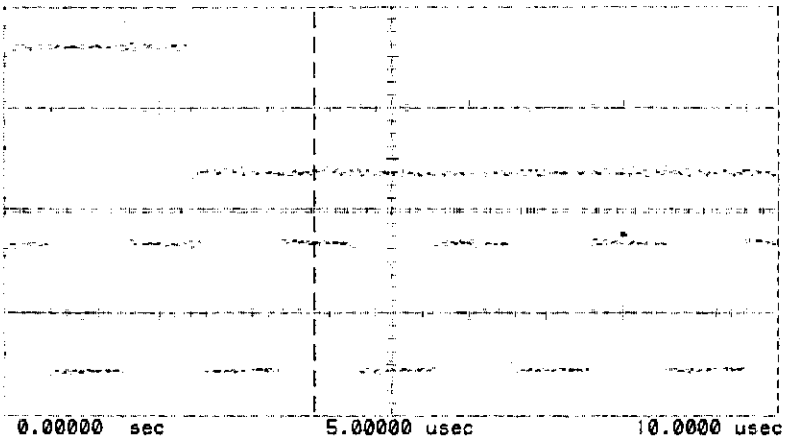
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  20.0 usec/div             Delay      = -22.8000 usec
Delta T    =  716.000 usec
Start      -  4.00000 usec              Stop       =  720.000 usec

      Trigger mode : Edge
On  Pos. Edge on Chan1
Trigger Levels
Chan1      -   -1.300  volts
Holdoff    =    540.000 usecs
```

Figure 6E-15. Loop 18 Troubleshooting Waveforms at U5 Pin 1 and TP9.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  1.00 usec/div             Delay      =  0.00000  sec
Delta T    =  716.000 usec
Start      =  4.00000 usec              Stop       =  720.000 usec

      Trigger mode : Edge
On  Pos. Edge on Chan1
Trigger Levels
Chan1      =   -1.300  volts
Holdoff    =    540.000 usecs
```

Figure 6E-16. Loop 18 Troubleshooting Waveforms at U5 Pin 1 and U5 Pin 8.

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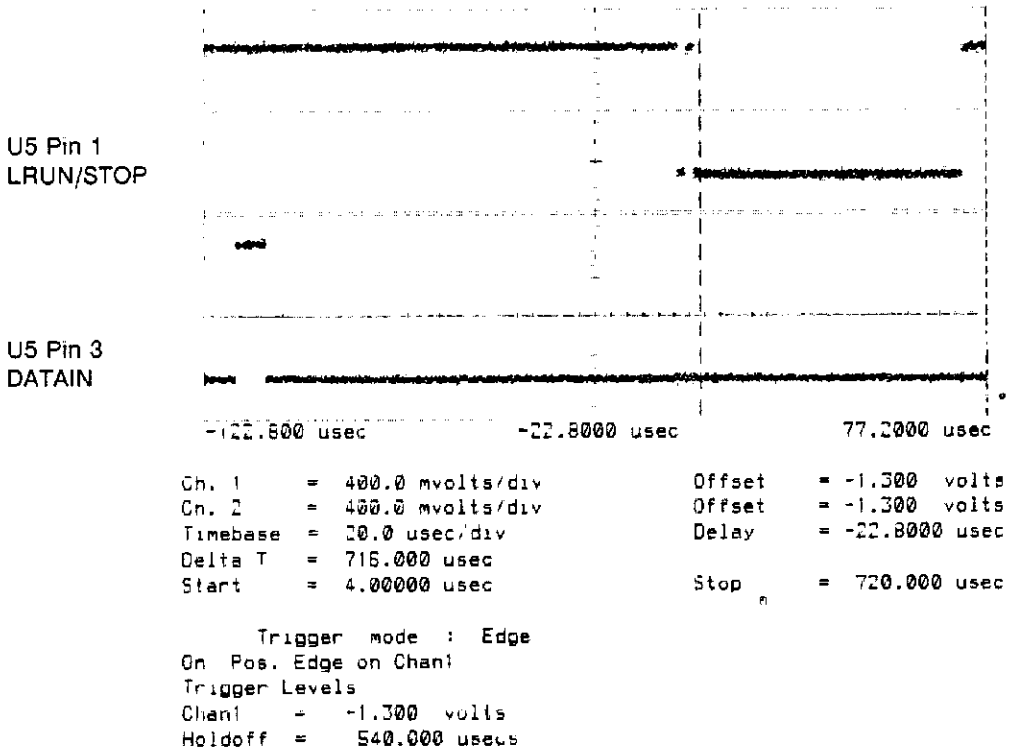


Figure 6E-17. Loop 18 Troubleshooting Waveforms at U5 Pin 1 and U5 Pin 8.

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6E-29. LOOP 19

Trigger ID

Description:

This test loop is similar to Loop 15 except that it looks to see if the Trigger board responds to "CONFIGURE".

Status Register:
No indications.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - Trigger
3. Functional blocks indicated - SIB, all board CPU interfaces especially Trigger board.

Fault Diagnosis:

Same as Loop 15

Troubleshooting Tree:

1. Put Trigger board on Board extender.
2. Follow diagnostic steps 2 through 6 in Loop 15.

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6E-30. LOOP 20

Trigger Qualifier ID

Description:

This tests the Trigger Qualifier's CPU interface circuitry by calling CONFIGURE, a routine which checks to find what board is in each slot. This loop will always fail in a HP 54100A, if any of the higher Loops (ie. 21-43) fail.

Status Register:

No indications.

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - Qualifier
3. Functional blocks indicated - SIB, all CPU board interfaces especially Qualifier board.

Fault Diagnosis:

See Loop 15 except as it applies to the Qualifier board.

Program Flowchart:

Set Loop variables for No Q_BD.
If qualifier present:
Program Q_BD for edge mode, all sources
enabled except Q_BD.
Set Loop variables for Q_BD present
ELSE
Set error indicator
END

Troubleshooting Tree:

1. Remove right side panel.
2. Follow steps 2 through 6 from the fault diagnosis section of Loop 15.

Loop Modification History:

In HP 54100A's, ROM revisions before Oct, 1985 and after or equal to Dec. 1984 may fail this loop every time due to a problem with the firmware. In these versions, Loop 20 did not check to see if the qualifier was installed before letting the test fail.

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6E-31. LOOP 21

Trigger Holdoff by Time (200 ns).

Description:

This test sets the holdoff time and the trigger to a known state. Once setup, a trigger event will start the holdoff to count. By monitoring the Trigger board's status register, for the status of the holdoff counter, the time from the simulated trigger and the end of the holdoff is measured with a software counter. The trigger event is the toggling of the invert line (U9 Pin 17) on the Trigger board. The sync comparator hybrids of the Sampler boards and the Trigger board (and the Trigger Qualifier board if installed) are disabled (ie. at - .8 V on Pin 14).

Staus Register:

STATUS #1 - Last down counter value (whether it passed or not). *
STATUS #2 - Last down counter value that failed. *
STATUS #3 - N/A
STATUS #4 - N/A

* Valid range 0-9, typical = 2-5
Invalid range -1, or >9

A -1 indicates that the holdoff counter did not timeout. Possible causes are slow or dead holdoff clock, a bad counter, or bad status register. A >9 indicates a fast clock, bad status, or bad counter operation. A value of 26 represents the initial software count. A 26 could mean a stuck status Bit, or the holdoff counter may not be loading or counting correctly.

Possible Causes of Problems:

1. Adjustments indicated - Sampler Trigger and Main Trigger Hysteresis

2. Boards indicated - Sampler 1, Sampler 2, Trigger, Qualifier

3. Functional blocks indicated - Sampler 1 and 2 sync comp hybrid's disabled, LIACK, STOP Bit on
   timebase control string, trigger control string, holdoff control string, invert line, holdoff counter, holdoff clock, holdoff shift register, trigger holdoff status, trig F/F, Fast trig F/F, shift & latch strobes.

Fault Diagnosis:

SAMP 1, 2 and Trig (and Trig Qual if installed) sync comp hybrids are disabled (ie. at -.8 V at U9 Pin 1, 3, and 19 on the Trigger board in a HP 54100A and at U4 Pin 1, 6, 12, and 17 in a HP 54100D. If U9 pin 1 is bad, replace the Trigger board. If U9 pin 3 is bad, then replace the Sampler 1 board. If U9 pin 19 is bad, then replace Sampler 2. If U4 pin 1 is bad, then replace Sampler 2. If U4 pin 6 is bad, replace Trigger board. If U4 pin 12 is bad, replace Qualifier board. If U4 pin 17 is bad, replace Sampler 1.

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6E-32. LOOP 22

Trigger Holdoff by Events

Description:

This loop is similar to Loop 21, except that this test counts simulated triggers rather than time after a trigger. The invert line on the Trigger board (U9 Pin 17) is used to simulate trigger after the trigger criteria is set up. The events counter is set to 10 counts. The first trigger event will start the holdoff, and 11 trigger events will conclude holdoff. The holdoff counter is loaded with a count of 10 events and after 10 triggers are simulated, the Trigger board status register should indicate that the holdoff has expired

Status Register:

STATUS #1 - -1 means failure, typical is 4090's.
STATUS #2 - -1 indicates that the holdoff at 9 events was not still in holdoff as expected.
STATUS #3 - -1 indicated that the holdoff was still in holdoff at 10 when when it should be out of holdoff.
STATUS #4 - N/A

Possible Causes of Failures:

1. Adjustments indicated - None

2. Boards indicated - SAMPLER1/2, TRIGGER, QUALIFIER

3. Functional blocks indicated - Sync Amp, Sync Amp control register and string, holdoff status bit in trigger status string, holdoff string, counter and shift register, Trig F/F, Fast Trig F/F, SAMPLER Sync Comp-Hybrids, Trig Qual sync Comp, Data latch strobes (both).

Fault Diagnosis:

Check the following points:

Fast trig Flip-Flop (F/F) output (U9 pin 11) - 24 cycles/Liack Invert line (U7 pin 7) - 24 cycles/Liack

SAMP1,2 and Trig (and Trig Qual if installed) sync comp hybrids are disabled (ie. at -.8 V at U9 Pin 1, 3, and 19 on the trigger board in a HP 54100A and at U4 Pin 1, 6, 12, and 17 in a HP 54100D. If U9 pin 1 is bad, replace the Trigger board. If U9 pin 3 is bad, then replace The Sampler 1 board. If U9 pin 19 is bad, then replace Sampler 2. If U4 pin 1 is bad, then replace Sampler 2. If U4 pin 6 is bad, replace Trigger board. If U4 pin 12 is bad, replace Qualifier board. If U4 pin 17 is bad, replace Sampler 1.

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6E-33. LOOP 23

Trigger Sync Comparator - Pos/Neg

Description:

This loop is similar to Loop 22 except that triggers are simulated by toggling the slope bit of the trigger board's sync comparator hybrid while it is disabled. This loop operates by setting holdoff counter to 11 events and simulating triggers. The holdoff status bit on the Trigger board is polled for determination of the status of the holdoff at different times during the test. This test requires that the SAMP 1, SAMP 2, and Trigger Qualifier trigger comparators be disabled. On the twelfth event, the holdoff should be over. The 1 comes from the fact that one trigger event is needed to start the holdoff. The description of the status register below does not include this first trigger event.

NOTE

At power-up, the trigger MUX hybrid may take several triggers to enable the holdoff for the first time. Therefore, this test may occasionally fail on power-up.

Staus Register:

STATUS #1 - This determines if holdoff can be enabled at all. A -1 indicates holdoff can't be enabled. Typical values are 4090's
STATUS #2 - This tests holdoff at 10 events. A -1 indicates that the holdoff was not sill in holdoff as expected.
STATUS #3 - This test holdoff at 11 events. A -1 indicates that the holdoff was still in holdoff when it was supposed to be out of holdoff.
STATUS 4 - N/A

Possible Causes of Failure:

1. Adjustments indicated - Sampler and Main Trigger hysteresis.

2. Boards indicated - Samplers 1 and 2, Trigger, and Trigger Qualifier

3. Functional blocks indicated - Ext 3 oscilloscope toggling, holdoff status bit in trigger status, holdoff shift, holdoff counter and register, both latch strobes, trigger control string and registers, fast and slow trigger flip-flops, Samplers 1 and 2 and Trigger Qualifier sync comparator disabled, trig 3 sync comparator, cables.

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Fault Diagnosis:

Check the following points.

Sampler 1,Samper 2, Trigger, Trigger Qualifier (if installed) sync comparator hybrids arre disabled (ie. at -.8 V at U9 pins 1, 3, and 19 on the Trigger board in an HP 54100A, but in HP 54100D on the Trigger Qualifier board U4 pins 1, 6, 12, and 17. If U9 pin 1 is bad, replace the Trigger board. If U9 pin 3 is bad, then replace the Sampler 1 board. If U9 pin 19 is bad, then replace the Sampler 2 board. If U4 pin 1 is bad, then replace the Sampler 2 board. If U4 pin 6 is bad, replace Trigger board. If U4 pin 12 is bad, replace Qualifier board. If U4 pin 17 is bad, replace Sampler 1.

Trigger SLOPE line (U1 pin 18) - 13 cycles/LIACK (TTL) If faulty, replace the Trigger board.

Trigger sync comparator output (U1 Pin 14) - 13 cycles/LIACK (EECL) If faulty, replace Trigger board (suspect U1).

Trigger Flip-flop (F/F) output (U9 pin 11) - 13 cycles/LIACK (EECL) If faulty, and the TCLK's are good, then replace the Trigger board (suspect U9).

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6E-34. LOOP 24

Trigger Fine Interpolator

NOTE

Troubleshoot this loop's 24A part first.

Description:

This loop tests the fine interpolator by setting the holdoff to 100 nsec and simulating 2 trigger events by toggling the invert line on the Trigger board. The first trigger event starts the holdoff which should end in 100 nsec (because the holdoff counter is loaded with a value equivalent to 100 nsec). The second trigger is a valid trigger event which starts the fine interpolator. When the fine interpolator is finished the Busy/Done Bit of the status register on the Trigger board will assert. After the second trigger event, the CPU goes into a polling loop which looks for the DONE assertion. The fine interpolator is stopped by the next edge of MASCLK. When DONE is received, the CPU reads the fine interpolator and compares it to set limits. The fast trigger F/F must be able to react to the toggling for this test to pass. In addition, if the pre-trigger delay is not working, it is possible that the interpolator will never get enabled. (The pre-trigger delay is set to 64 μs (very similar to LOOP 18).

Status Registers:

STATUS #1 - -1 indicated DONE not received in reasonable time
STATUS #2 - The fine interpolator value: Valid range 1800 - 4800
STATUS #3 - N/A
STATUS #4 - N/A

If a problem is indicated, either the status bit is broke, the fine interpolator is disabled or not working, or the TENBL is not correct. If Status #1 is outside its valid range and some definite number, and if all of the signals in the fault diagnosis section are good, then the fine interpolator is probably not working to spec.

Possible Causes of Failure:

1. Adjustments - Fine interpolator

2. Possible boards - Timebase, Trigger, Sampler1/2, Qualifier

3. Dependancies (Functional Block) - Shift & Data strobes, sync comp & holdoff strings, Pre-trig delay, fine interpolator, TENBL, holdoff clock & counter, Run/Stop, Slow & Fast Trig F/F, Trig Status (Busy/Done, Holdoff), sync comp hybrid SAMP1, 2 sync comp hybrid & Qual Sync Comp.

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Fault Diagnosis:

Check the following points.

SAMP1,2 and Trig (and Trig Qual if installed) sync comp hybrids are disabled (ie. at -.8 V at U9 Pin 1, 3, and 19 on the Trigger board in an HP 54100A and at U4 Pin 1, 6, 12, and 17 in an HP 54100D. If U9 pin 1 is bad, replace the Trigger board. If U9 pin 3 is bad, then replace the Sampler 1 board. If U9 pin 19 is bad, then replace Sampler 2. If U4 pin 1 is bad, then replace Sampler 2. If U4 pin 6 is bad, replace Trigger board. If U4 pin 12 is bad, replace Qualifier board. If U4 pin 17 is bad, replace Sampler 1. If the TCLK's are properly disabled then the problem is not with the Sampler boards.

Check the following points:

INVERT (U7 Pin 7 on trigger BD) - 2 cycles/Liack. Replace Trigger board if bad.
Fast trig F/F (output Trig MUX (U9 Pin 11)- 2 cycles/Liack. Replace Trigger board if bad.
100 MHz clock (TP9). Replace Trigger board if bad.
TENBL (Trig TP9) - mostly EECL low
STRIG (Trig U14 pin 15) - mostly EECL high
RUN/STOP (Time U29 pin 15) - toggling
BUSY/DONE (Time U27 pin 10) - toggling

LOOP 24A

This part of the test looks for the presense and response of the Timebase board.

If the Timebase does not respond, then CPU will not perform tests 24 through 29, inclusive.

To determine whether this part of the loop is failing, set the oscilloscope in REPEAT Loop 24 for about 30 seconds. After pressing STOP TEST, if the status line on the display lists any other loop than 24, then this part of Loop 24 is failing.

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6E-25 LOOP 25

Trigger Fine Interpolator Clear

Description:

The fine interpolator is cleared when the RUN/STOP bit is STOPPED. This test will set the STOP bit and read the interpolator, which should read zero.

Status Register:

STATUS #1 - The value of the fine interpolator. Should be Zero.
STATUS #2 - N/A
STATUS #3 - N/A
STATUS #4 - N/A

Possible Causes of Failure:

1. Adjustments - None

2. Possible boards - Timebase, Trigger

3. Functional block dependancies - Fine Interpolator
   Fine Interpolator counter
   RUN/STOP
   Timebase status register
   Timebase control string

Fault Diagnosis:

Check for the following signals.

RUN/STOP going high (U48 Pin 10) [low on U49 Pin 2]
All TTL Logic Level Lows: U35 Pins 4, 5, 12, 13 U60 Pins 3, 4, 5, 6 U61 Pins 3, 4, 5, 6, 8, 9, 10, 11

U33 Pin 4 - TTL High TP10 - ECL Low TP11 - ECL High

Loop Flowchart:

Call INIT (See section near beginning of 6C)
Set STOP bit
Clear error indicator
Set LIACK high
If fine interpolator<>0 then set error indicator

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Troubleshooting Tree:

Probe the following points. Refer to Figure 6E-14.

```
Trig U23 pin 5   (MASCLK)
Trig TP31        (LRUN/STOP)
```

If LRUN/STOP is bad, check U29 pin 15 instead of TP31. If it is bad here, replace the Timebase board.

If all of the counter's outputs are not zero (see points above), and MASCLK and RUN/STOP are good, replace the Trigger board (suspect the fine interpolator counter).

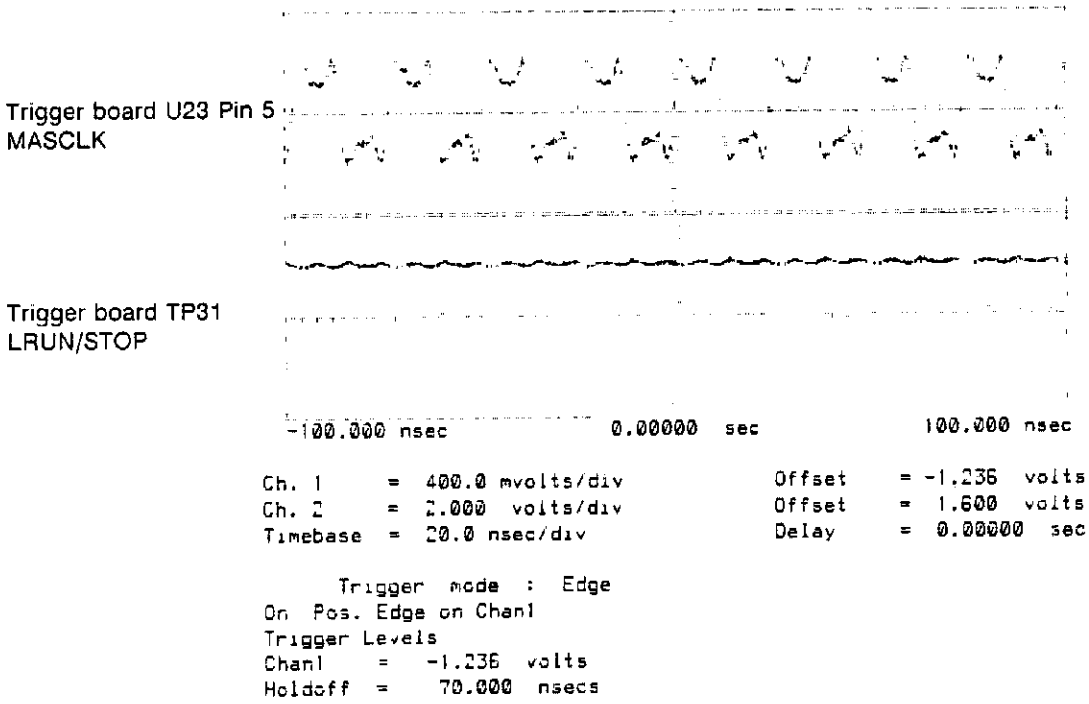


Figure 6E-18. Loop 25 Troubleshooting Waveforms at U23 Pin 5 and TP31.

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6E-36. LOOP 26

Sample Rate Generator

Description:

This test exercises the sample rate generator. The timebase status word contains a bit which reflects the state of SAMPLE CLOCK 2. This clock is set to approximately 400 μs period. This test performs the following procedure: CPU Polls the status bit until a low is detected. It then continues to poll for a high. Then it starts a software UP counter which will be used to determine the period of the clock. It then polls the status bit until a low is detected. Then the UP counter is stopped and its value recorded. The software DOWN counter is then started (this counter starts at the same value that the UP counter is stopped). The CPU then polls the status bit until a high is detected. This ends the measurement. The DOWN counter should be close to zero. This value detects duty cycle of clock. The CPU then compares the UP and DOWN counter for proper values.

Status Register:

STATUS #1 - Value of DOWN counter last time there was a failure
STATUS #2 - Value of UP counter last time there was a failure
STATUS #3 - Value of Loop DOWN counter waiting for the initial low state.
STATUS #4 - Value of loop DOWN counter waiting for the initial first rising edge.

TYPICAL VALUES FOR 3 & 4 = 4040-4095
VALID RANGE FOR 1 = 0-3
VALID RANGE FOR 2 = 47-51

Possible Causes of Failure:

1. Adjustments indicated - MASCLK

2. Boards indicated - Timebase

3. Functional blocks indicated - Sample Rate Generator
   Master Clock
   Timebase Status (SMCLK2)

Fault Diagnosis:

Check the following points.

40 MHz MASCLK (TP2)
SMCLK2 = 400 μs period (U27 pin 6)
LRUN/STOP (TP7) Toggling.

In addition, see Troubleshooting Timebase board Section 6E-3 for more information.

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TP7
LRUN/STOP

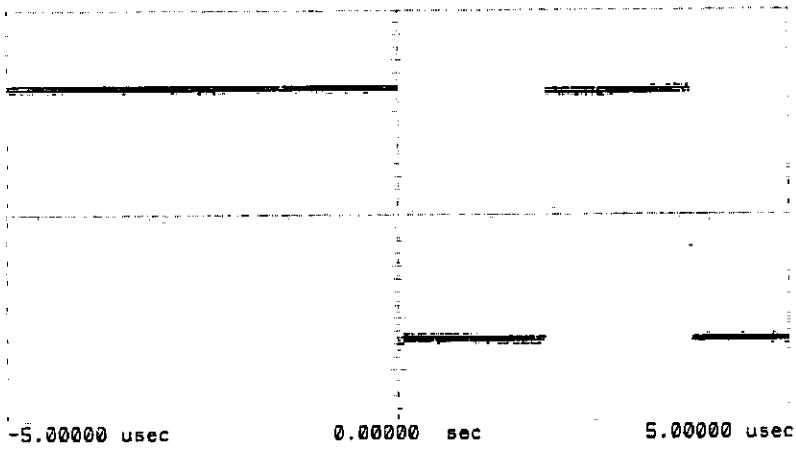


Figure 6E-19. Loop 26 Troubleshooting Waveforms at TP7.

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6E-37. LOOP 27

Timebase Post Trigger Delay

Description:

The test exercises the post trigger delay counter on the Timebase board by loading the counter with a value, starting the counter counting downward, and using a software counter to determine the time it takes for the counter to time out. Specifically, the holdoff is set to 100 nsec. The post Trig delay counter is loaded with a count of 19. And the sample rate is set to a 100 μs period. The trigger is set up so that only a data latch is required to cause a trigger event. The TENBL Bit (In timebase status) is polled until it is enabled. SMCLK2 Bit (In timebase status) is polled for a positive going edge. The trigger data latch is sent and a trigger event occurs. This starts the post trigger delay counter. The CPU polls the BUSY/DONE line for an assertion of done which will happen when the post trigger delay counter reaches zero. The time between the data latch and the DONE signal is counted with a software timer and should be within a valid range. Because the count in post trigger delay is 19 and because the post trig delay counter is clocked by SMCLK2, the time between STRIG and DONE is 1.9 msec.

Status Register:

STATUS #1 - -1 indicates that a rising edge was not found on SMCLK2 within a given amount of time.
STATUS #2 - Value of last down counter regardless whether it was valid or not
STATUS #3 - Value of last down counter that failed because the value was too large.
STATUS #4 - Value of last down counter that failed because the value was too small.

VALID RANGE #2, 3, 4 - 378 to 400

Possible Causes of Problems:

1. Adjustments indicated - Sampler and main trigger hysteresis

2. Boards indicated - Timebase, Trigger, Qualifier, Sampler 1/2

3. Functional blocks indicated - Sample rate generator, POST TRIG DELAY, TRIG COMP, TIMEBASE STATUS (BUSY/DONE, TENBL), TENBL, STRIG, PRE-TRIG DELAY, HOLDOFF STRING & COUNTER, SYNC COMP STRING, SLOW & FAST TRIG F/F, SAMPLER's TRIG COMPARATORS. TRIGGER STATUS TIMEBASE CONTROL STRINGS

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Fault Diagnosis:

Check the following points.

SAMP1,2 and Trig (and Trig Qual if installed) sync comp hybrids are disabled (ie. at -.8 V at U9 Pin 1, 3, and 19 on the Trigger board in an HP 54100A and at U4 Pin 1, 6, 12, and 17 in an HP 54100D. If U9 pin 1 is bad, replace the Trigger board. If U9 pin 3 is bad, then replace the Sampler 1 board. If U9 pin 19 is bad, then replace Sampler 2. If U4 pin 1 is bad, then replace Sampler 2. If U4 pin 6 is bad, replace Trigger board. If U4 pin 12 is bad, replace Qualifier board. If U4 pin 17 is bad, replace Sampler 1. If all of the TCLK's are correct, then the Sampler boards are not causing the problem.

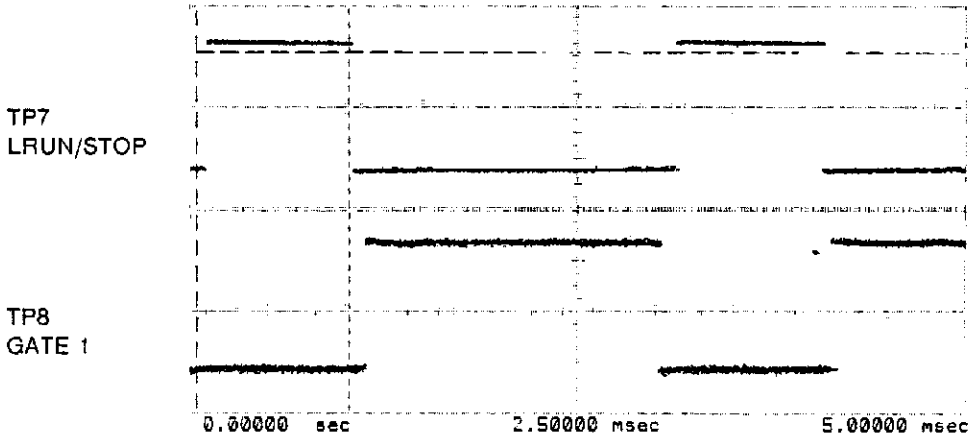
Check the following points:

SMCLK2 (U10 pin 11) = 100 μs period
Post trig delay = 1.9 msec
MASCLK (Time TP2) = 40 MHz
TRIG BD (U9 Pin 11) = 0 V to -.8 V square wave (2 cycles/LIACK)

Check the following points.

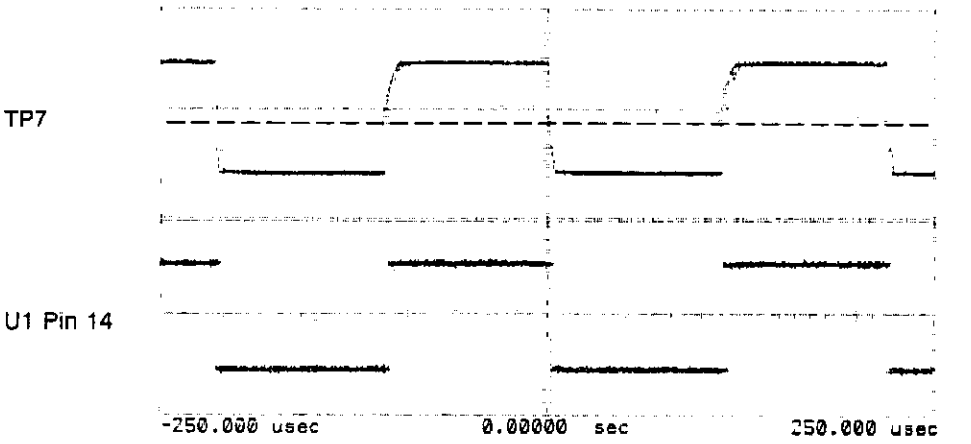
TP7 (LRUN/STOP)
TP8 (GATE1)

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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta T    =  979.901 usec
Start      =  35.3333 usec              Stop       =  1.01523 msec
Delta V    =  0.000  volts
Vmarker1   = -876.0 mvolts              Vmarker2   = -876.0 mvolts
      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    740.000 usecs
```

Figure 6E-20. Loop 27 Troubleshooting Waveforms at TP7 and TP8.




```
Ch. 1      =  10.00  volts/div          Offset     =  1.600  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  50.0 usec/div             Delay      =  0.00000  sec
Delta V    =  0.000  volts
Vmarker1   = -1.268  volts              Vmarker2   = -1.268  volts

      Trigger  mode  :  Edge
On  Neg. Edge on Chan1
Trigger Levels
Chan1      =    1.600  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-21. Loop 27 Troubleshooting Waveforms at TP7 and U1 Pin 14.

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6E-38. LOOP 28

TIMEBASE COARSE INTERPOLATOR

Description:

This loop tests the coarse interpolator by reading the number of edges of MASCLK that the coarse interpolator records between a given trigger event and a known SMCLK edge. To do this requires the following: The HOLDOFF is set to 100 nsec. The POST TRIGGER DELAY is set to a known count and the SMCLK2 is set to a 250 μs period. The trigger is set up so that only a data latch is needed to cause a trigger event. A poll of SMCLK2 is executed until a positive edge is found. The trigger string is then latched which causes a trigger event, which starts the coarse interpolator. The coarse interpolator counts MASCLK's until the next positive edge of SMCLK2. However, the CPU can only tell if the loop is done by polling BUSY/DONE for a DONE condition as defined by the POST TRIGGER DELAY counter. When DONE has asserted, the coarse interpolator must be done and within a valid count range. The valid range is determined by the number of 40 MHz MASCLK's that can occur in 1/2 of the SMCLK2 period (120 counts.) Triggers are generated by toggling the INVERT line on the Trigger board while all the TCLK's are disabled.

Status Register:

STATUS #1 - Value of down counter polling BUSY/DONE. Typical 2950 to 2970.
STATUS #2 - Value of last coarse interpolator that failed due to too large a value.
STATUS #3 - Value of last coarse interpolator that failed due to too small a value.
STATUS #4 - N/A
VALID RANGE = 7808-9472

Possible Causes of Failure:

1. Adjustments indicated - Sampler1/2 and main trigger hysteresis
2. Boards indicated - Timebase, Trigger, Sampler1/2, Qualifier
3. Functional blocks indicated - SMCLK, COARSE INTERPOLATOR, TRIG COMP, TIMEBASE STATUS (BUSY/DONE, SMCLK2),TENBL, STRIG, PRE-TRIG DELAY, HOLDOFF STRING & COUNTER, SLOW & FAST TRIG F/F, TRIG CONTROL STRING, SAMP1/2 SYNC COMP, TRIGGER STATUS, RUN/STOP, BUSY/DONE

Fault Diagnosis:

Check that Trigger U9 pin 1,3,19 and U4 pin 1,6,12,17 are disabled (-.8 V). If U9 pin 19 or U4 pin 17 is bad, replace the Sampler 1. If U9 pin 3 or U4 pin 1 is bad, replace the Sampler 2. If U9 pin 1 or U4 pin 6 is bad, replace the Trigger board. If U4 pin 12 is bad, replace the Qualifier board.

Probe the following points.

TP7	(LRUN/STOP)	U9 pin 8 or U4 pin 8	(TCLKOUT)
TP9	(TENBL)	U20 pin 5	(STRIG)
TP7	(LRUN/STOP)	U20 pin 4	(MASCLK)
U20 pin 5	(STRIG)	U20 pin 13	(LSMCLK2)

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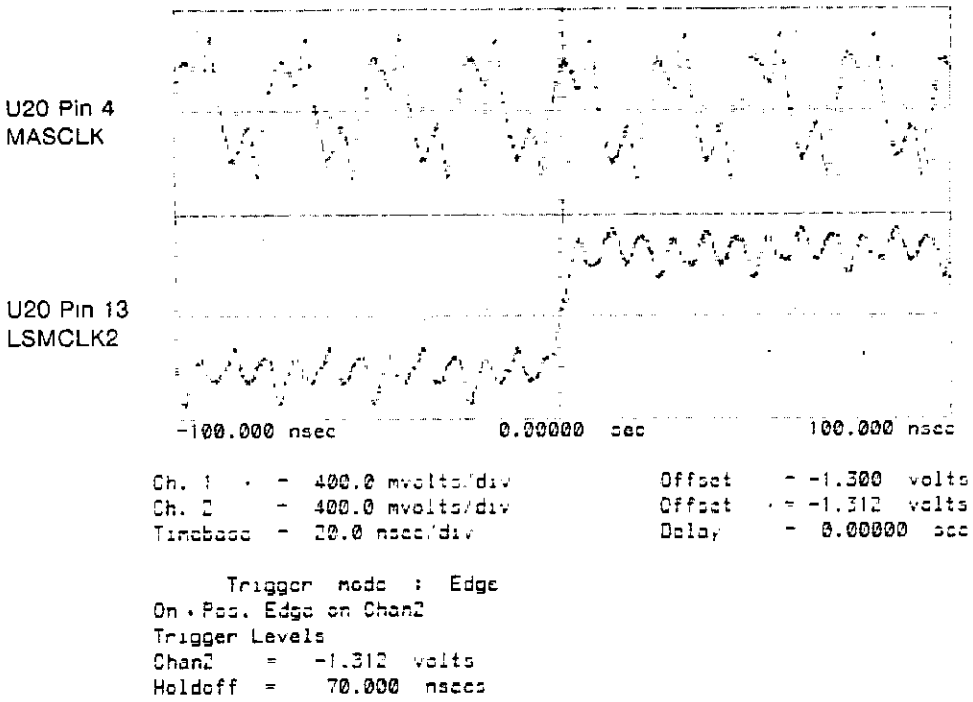


Figure 6E-22. Loop 28 Troubleshooting Waveforms at U20 Pins 4 and 13.

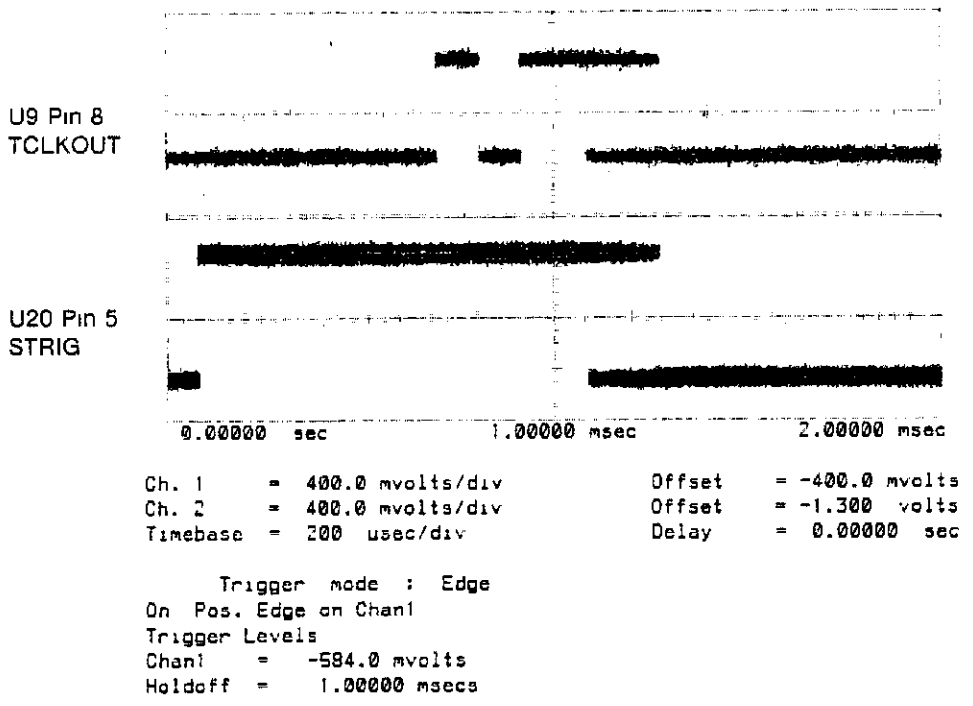
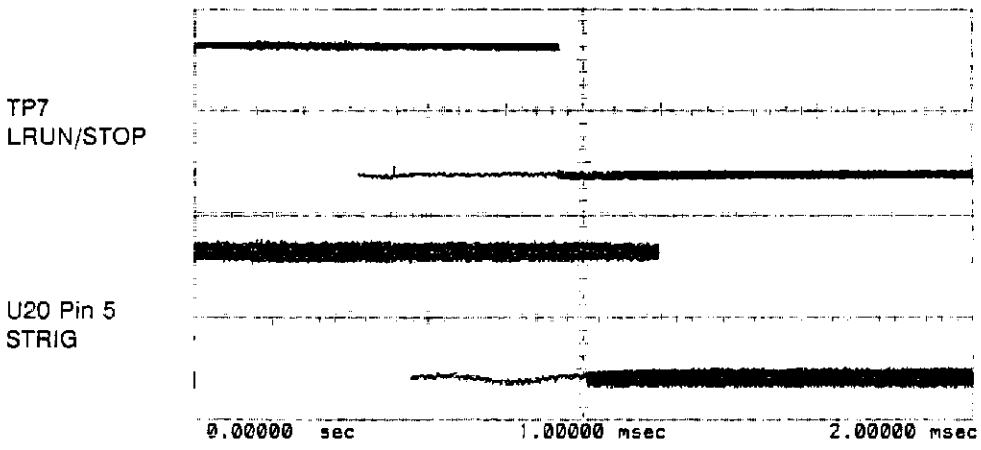


Figure 6E-23. Loop 28 Troubleshooting Waveforms at U9 Pin 8 and U20 Pin 5.

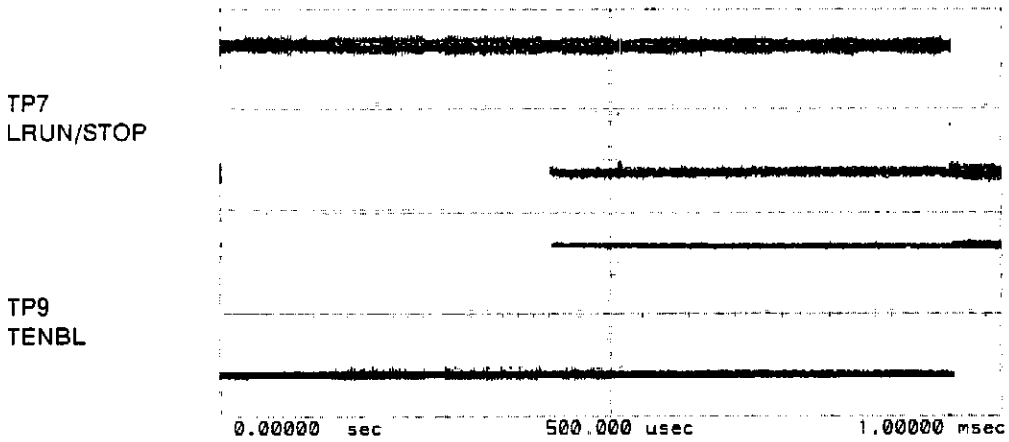
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  200  usec/div             Delay      =  0.00000  sec

     Trigger mode  :  Edge
On  Pos. Edge on Chan1
Trigger Levels
Chan1     =   -1.300  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-24 Loop 28 Troubleshooting Waveforms at TP7 and U10 Pin 5.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  100  usec/div             Delay      =  0.00000  sec

     Trigger mode  :  Edge
On  Pos. Edge on Chan1
Trigger Levels
Chan1     =   -1.300  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-25. Loop 28 Troubleshooting Waveforms at TP7 and TP9.

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6E-39. LOOP 29

Timebase Coarse Interpolator Clear

Description:

The coarse interpolator is cleared when the RUN/STOP bit is STOPPED. This test sets the STOP bit and then reads the coarse interpolator. It should read zero.

Status Register:

STATUS #1 - The value of the interpolator. Valid range is 00.
STATUS #2 - N/A
STATUS #3 - N/A
STATUS #4 - N/A

Possible Causes of Failure:

1. Adjustments indicated - None

2. Boards indicated - Timebase

3. Functional blocks indicated - RUN/STOP or Coarse Interpolator Counter

Fault diagnosis:"

Check the following points:
RUN/STOP (TP7) ECL SQUARE WAVE
U15 Pins 1, 2, 13, 14 about -5V
U28 Pins 3, 4, 5, 6 TTL low
U40 Pins 3, 4, 5, 6, 8, 9, 10, 11 TTL low

Troubleshooting Tree:

Program Flowchart -

Call INIT
Stop STOP bit
Set LIACK high
If coarse interpolator = 0 then END
Set loop error indicator
END

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6E-40. LOOP 30

SAMPLER 1 - POS/NEG EDGE SELECT

This loop has a 30A Part to it. Troubleshoot the 30A part first.

Description:

This loop is similar to Loop 23 (HOLDOFF by events) in that it counts the number of trigger events it receives and counts the HOLDOFF counter down one number for each trigger event. The difference is in how it receives its trigger. The trigger is generated by toggling the slope line on SAMPLER 1's trigger comparator hybrid. The events are set to 11 events. The first trigger event will start HOLDOFF and the 12th event will conclude HOLDOFF. The polling loop executes 10 trigger events and exits the loop. The state of the HOLDOFF counter is then tested and should still be held in HOLDOFF. Then one more trigger is generated and the unit should come out of HOLDOFF. If either time (when 10th or 11th trigger event is triggered) gives a status of HOLDOFF that is inconsistent with what is expected, then the test fails.

Status Register:

STATUS #1 - This determines if the HOLDOFF can be enabled at all.
-1 is a failure. 4090's is typical.
STATUS #2 - This tests HOLDOFF at 10 events after the first latching trigger event.
-1 indicates that it was not still in HOLDOFF as expected.
STATUS #3 - This tests HOLDOFF at 11 events after first latching trigger event. -1 indicates that it
was still in HOLDOFF when it should not have been in HOLDOFF.
STATUS #4 - N/A

Possible Causes of Failure:

1. Adjustments indicated - Sampler and main trigger hysteresis

2. Boards indicated - SAMPLER1/2, TRIGGER, QUALIFIER

3. Functional Blocks indicated - Attenuator, HOLDOFF string & counter, Slow & Fast trigger F/F, Trigger status, Sync comparators, SAMP Sync comparators, Data latch strobes, cables, POS/NEG

Fault Diagnosis:

Check that Trigger U9 pin 1,3 and U4 pin 1,6,12 are disabled (-.8 V). If U9 pin 3 or U4 pin 1 is bad, replace the Sampler 2. If U9 pin 1 or U4 pin 6 is bad, replace the Trigger board. If U4 pin 12 is bad, replace the Qualifier.

Probe the following points.

Samp U9 pin 18 (POS/NEG)
Samp U9 pin 14 (TCLK1)

Trig U9 pin 19 (TCLK1)
Trig U9 pin 11 (TCLKOUT)

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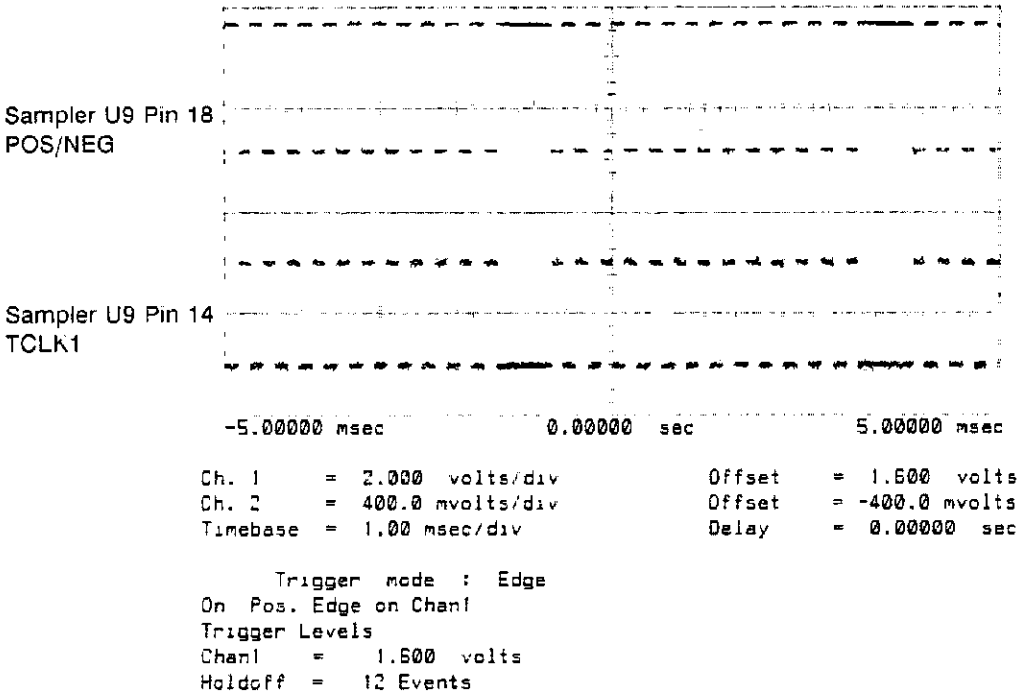


Figure 6E-26. Loop 30 Troubleshooting Waveforms at U9 Pins 14 and 18.

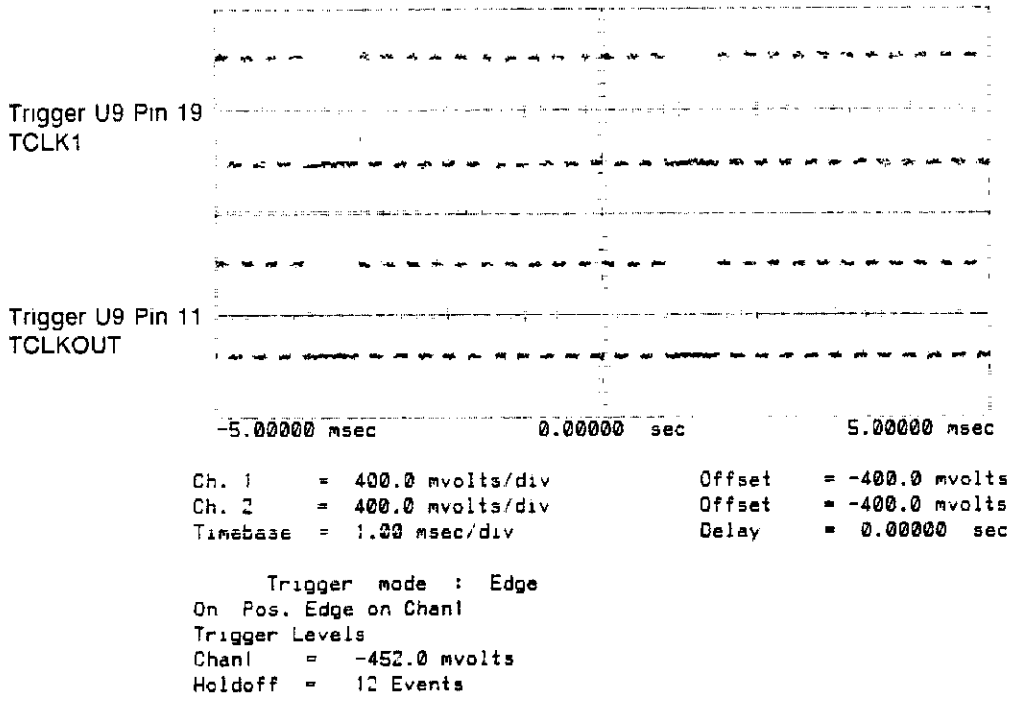


Figure 6E-27. Loop 30 Troubleshooting Waveforms at U9 Pins 11 and 19.

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LOOP 30A

Description:

This tests whether or not the following boards are in the system: SAMPLER1 (SAMPLER2 if SAMPLER1 is not installed).

If these boards are installed, all of the tests will be performed. If not installed, the following tests will not be performed:

30, 31

This loop should be troubleshot before any of the others listed above.

Make sure that this part of the loop is failing by putting the unit in the repeat loop 30 for 30 seconds and then stopping the test. If this part of the loop is failing, the unit will display a loop number other than Loop 30 on the status line of the display.

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6E-40. LOOP 31

SAMPLER 1 - TRIGGER LEVEL DAC

Description:

This tests operates exactly like loop 30 except in the way the trigger event is created. The trigger event is created by toggling the output of the trigger level DAC on SAMPLER 1 between the high and low rails. When the DAC level passes through zero and is of the correct slope, a trigger transistion is produced by the SAMPLER 1's trigger comparator hybrid. The input must be at zero volt potential going into the Pre-amp hybrid.

Status Register:

STATUS #1 - This determines if the HOLDOFF can be enabled at all. -1 is a failure. TYPICAL = 4090's.
STATUS #2 - This tests the HOLDOFF at N-1 events. -1 indicates that it was not still in HOLDOFF as expected.
STATUS #3 - This tests the HOLDOFF at N events. -1 indicates that it was still in HOLDOFF when it should have been.
STATUS #4 - N/A

Possible Causes of Failure:

1. Adjustments indicated - Same as loop 30

2. Boards indicated - Same as loop 30

3. Functional blocks indicated - Attenuator, Pre-Amp, SAMP1 Trig. Comp, TRIG F/F, HOLDOFF counter, HOLDOFF, SAMP1 TRIG Level DAC, TRIG STATUS, Fast Trig F/F, Trig load, SAMP String and load, cables

Fault Diagnosis:

Check that Trigger U9 pin 1,3 and U4 pin 1,6,12 are disabled (-.8 V). If U9 pin 3 or U4 pin 1 is bad, replace the Sampler 2. If U9 pin 1 or U4 pin 6 is bad, replace the Trigger board. If U4 pin 12 is bad, replace the Qualifier.

Probe the following points.

```
Samp TP9           (Trigger level)
Samp U9 pin 14     (TCLK1)

Trig U9 pin 19     (TCLK1)
Trig U9 pin 11     (TCLKOUT)
```

Check the following point.

Sampler TP8 = 0 V

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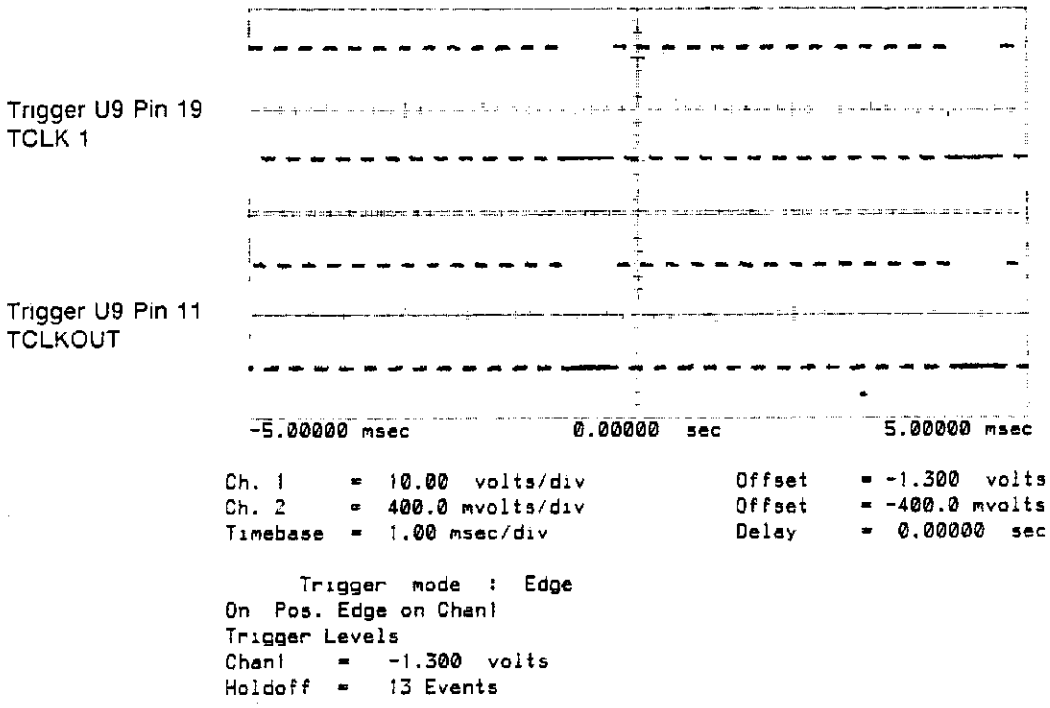


Figure 6E-28 Loop 31 Troubleshooting Waveforms at U9 Pins 11 and 19.

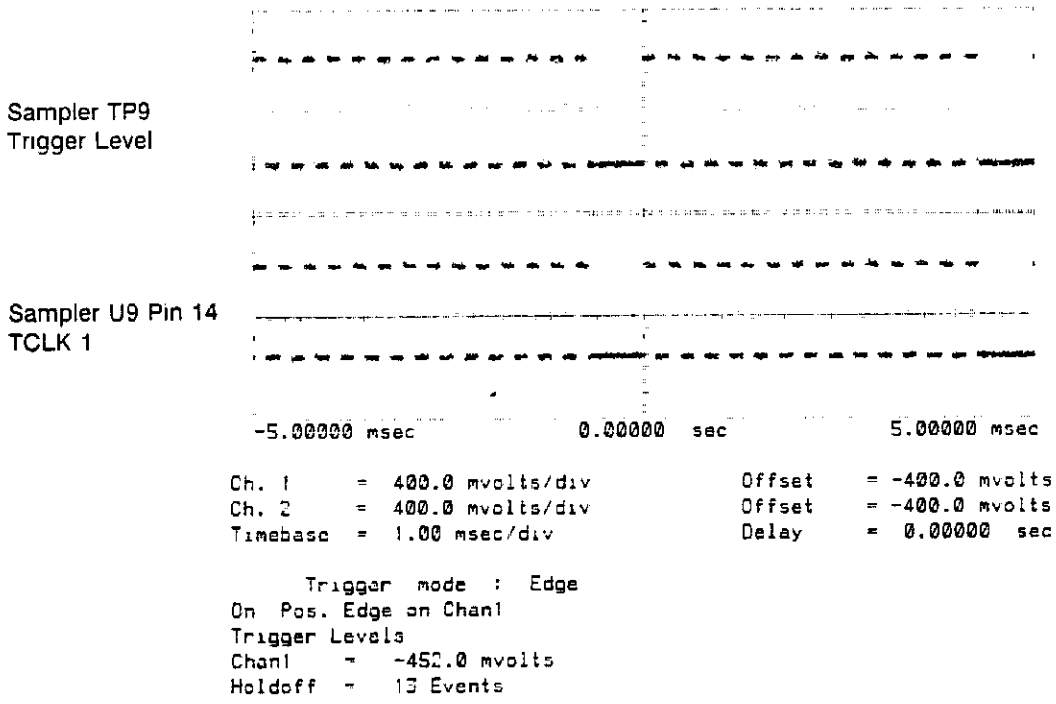


Figure 6E-29. Loop 31 Troubleshooting Waveforms at TP9 and U9 Pin 14.

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6E-42. LOOP 32

SAMPLER 2 - POS/NEG EDGE SELECT

This loop also has a part 32A. Troubleshoot Loop 32A fist.

Description:

This test is the same test as Loop 30 except the SAMPLER 2 is tested rather than SAMPLER 1.

Status Register:

Same as Loop 30 except SAMPLER 2.

Possible Causes of Failure:

Same as loop 30 except Sampler 2.

Fault Diagnosis:

Same as Loop 30 except Sampler 2 instead of Sampler 1 and replace Trigger U9 pin 19 with Trigger U9 pin 3 and replace Qualifier U4 pin 17 with Qualifier U4 pin 1.

LOOP 32A

This part of the loop checks to make sure the following boards are inserted and respond: SAMPLER 2 (or SAMPLER 1 if SAMPLER 2 gone)

These boards are needed for the following tests:

32, 33

If any one of these boards is not responding, the loops listed above will be skipped. You can determine if this part of Loop 32 is failing by executing REPEAT LOOP 32 for 30 seconds and then pressing stop test. If this part of the loop is failing, the status line on the display will indicate that it was running a repeat loop on some other loop than 32.

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6E-43. LOOP 33

SAMPLER 2 - TRIGGER LEVEL DAC

Description:

This is the same loop test as loop 31 except that Sampler 2 is tested instead of Sampler 1.

Status Register:

Same as Loop 31 except Sampler 2.

Possible Cause of Failure:

Same as loop 31 except Sampler 2 instead of Sampler 1.

Fault Diagnosis:

Same as Loop 31 except Sampler 2 instead of Sampler 1 and replace trigger U9 pin 19 with trigger U9 pin 3 and replace qualifier U4 pin 17 with qualifier U4 pin 1.

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6E-34. LOOP 34

ADC1 ID

Description:

This test does not actually test any hardware, rather it tests whether or not the ADC1 board responds to "CONFIGURE", a routine that polls all slots to determine what is present.

Status Register:

No indications

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - This loop fails if ADC1 and ADC2 is not responding
3. Functional blocks indicated - SIB, All CPU board interfaces especially ADC1 and ADC2.

Fault Diagnosis:

See Loop 15

Troubleshooting Tree:

1. Put the failing ADC in the Extender board
2. Follow fault diagnosis steps 2 through 6 of Loop 15

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6E-45. Loop 35

SAMPLER 1 - Trigger level DAC = 0.

Refer to the 35A part first.

Description:

This test sets the offset DAC of SAMPLER to a known value with the input attenuator open (which sets the sampler's output to a virtual ground). Thus the IFOUT reflects the value of the offsest DAC. The program is then paused for 100 msec (the settling time of the DAC), during which the timebase is loaded with the control strings which allow the timebase to take a complete 1024-byte record when required. (This includes loading the pre and post trigger counters, sample rate register, etc) The acquisition is started and then completed. The CPU then reads out every byte of waveform acquisition and compares its value to a value it expects to see. If any value is out of range, an error indicator is set.

When the wait-set routing allowed for the settling time, it also calculates what the pre and post trigger delays and the sample rate would need to be to fill up the entire 1024 bytes.

Status Register:

STATUS #1 - Last ADC value in error for being too high.
STATUS #2 - Last ADC value in error for being to low.
STATUS #3 - Last ADC address in error for being too high.
STATUS #4 - Last ADC address in error for being too low.

```
VALID RANGE 1,2 :    58-70
VALID RANGE 3,4 :    -30728     TO     -28680
                      87F8H     TO      8FF8H
```

NOTE

The addresses are integer representations of 2's complement 16 bit numbers. They are only even numbers and are the offset for the ADC board.

Possible Causes of Failure:

1. Adjustments indicated - INULL, ONULL, SBIAS, SEFF (on sample board being tested).

2. Boards indicated - Sampler1/2, Timebase, Trigger, Qualifier

3. Functional blocks Indicated - SMCLK2, pre-post trig delay, offset DAC, post AMP, attenuator, fast trig F/F, sampl sync, comp, STRIG, GATE1, holdoff counter & circuit, slow trig F/F, trig status string, sync comp hybrid w sampl, TENBL.

Fault Diagnosis:

Ensure that no signal is connected to the front panel BNC.

Make sure that all loops prior to this loop are passing; especially, the timebase loops (18, 26, 27, 28, and 29) and the Trigger board loops (21, 23, 30, 31, 32, 33). This will completely verify the operation of the Trigger, Qualifier, and Timebase boards for this loop. However, to make sure, probe the following points.

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```
TP3         (MASCLK)
U27 pin 5   (SMCLK1)

U27 pin 6   (SMCLK2)
U27 pin 10  (GATE1)
```

Check the following points.

```
SAMPLER 1 DAC Digital value      = 11 bits of 0 (OR 0000H)
SAMPLER SMCLK2 (Time TP11)       = 100 nsec Period
Pre-Trig Delay                   = 250 μ (from RUN/STOP (Time TP7) to
                                   TENBL(TIME TP9))
IFOUT cables are connected and non-intermittant
RUN/STOP (Time TP7)              = toggling.
SAMPLER1 Data shift (U34 pin 2) = 0001000H
```

Measure Sampler 1 U7 pin 3. It should be 0 V. If not, suspect U1 or U7 and replace the Sampler board.

Measure Sampler board U5 pin 4, it should be about -3.53 V (This number may vary slightly between units due to different pre-amp adjustment positions). If it is not, replace the Sampler 1 board (suspect the dc offset circuitry or U5 pulling the point down (this last concept occurs more frequently on tests 36, 37, 40, and 41).

NOTE

In the next procedure swapping the ADC boards may be necessary. When swapping the ADC boards, be sure that all cables are connected to the same board slots. Do not move the cables from their connectors with the ADC boards.

If all the previous steps have passed, then swap ADC boards between channels. Power the instrument with a two-key-down-power-up. If the failure has switched channels, the problem is on the ADC board that is now in channel 2. If the problem is gone, there is a high probability that there is an adjustment problem in the unit. In this case, perform a complete adjustment of the unit.

If the test still fails in channel 1, then set the vertical sensitivity to 10 mV/div and the offset to zero. Remove all input signals and tweek the offset adjustment on the ADC board until the trace overlays the center graticule. Now input a 300 mV dc level and change the oscilloscope's vertical sensivity to 100 mV /div. Make sure that the trace is 3 major divisions above the center graticule (±1 minor division). Now input a -300 mV dc level. Make sure the trace is 3 divisions below the center graticule. If these measurements are within their limits, then repower the oscilloscope. If channel 1 still fails then replace the Sampler 1 board. If these limits are not within their limits, perform a complete calibration of the instrument. If this does not help, replace the Sampler 1 board.

In addition, see Troubleshooting the ADC Board Section 6E-9 for additional information concerning ADC board failures.

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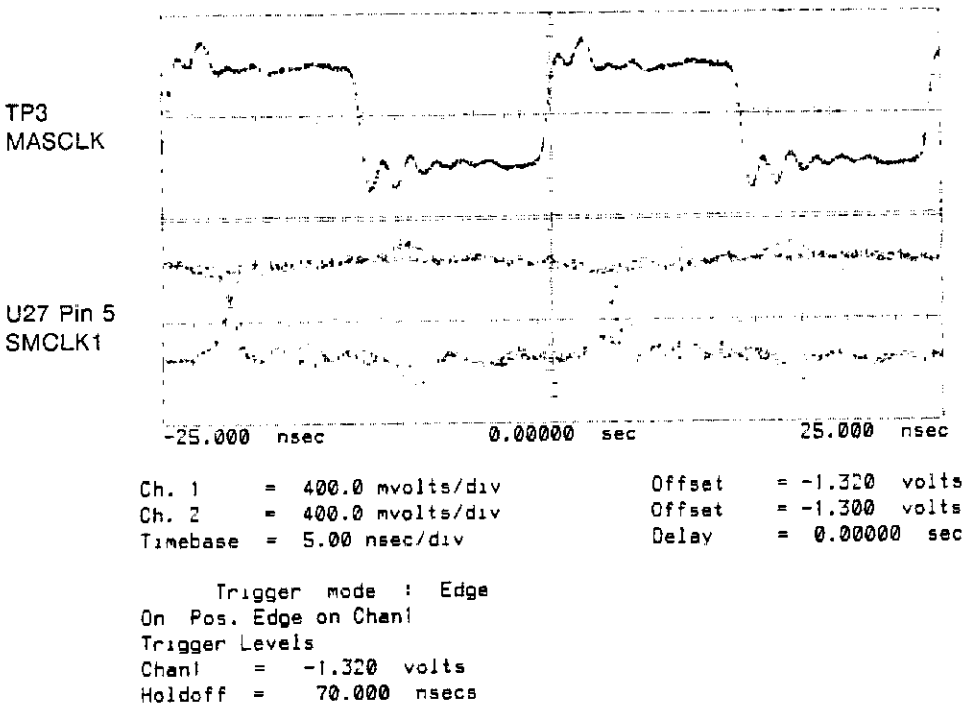


Figure 6E-30. Loop 35 Troubleshooting Waveforms at TP3 and U27 Pin 5.

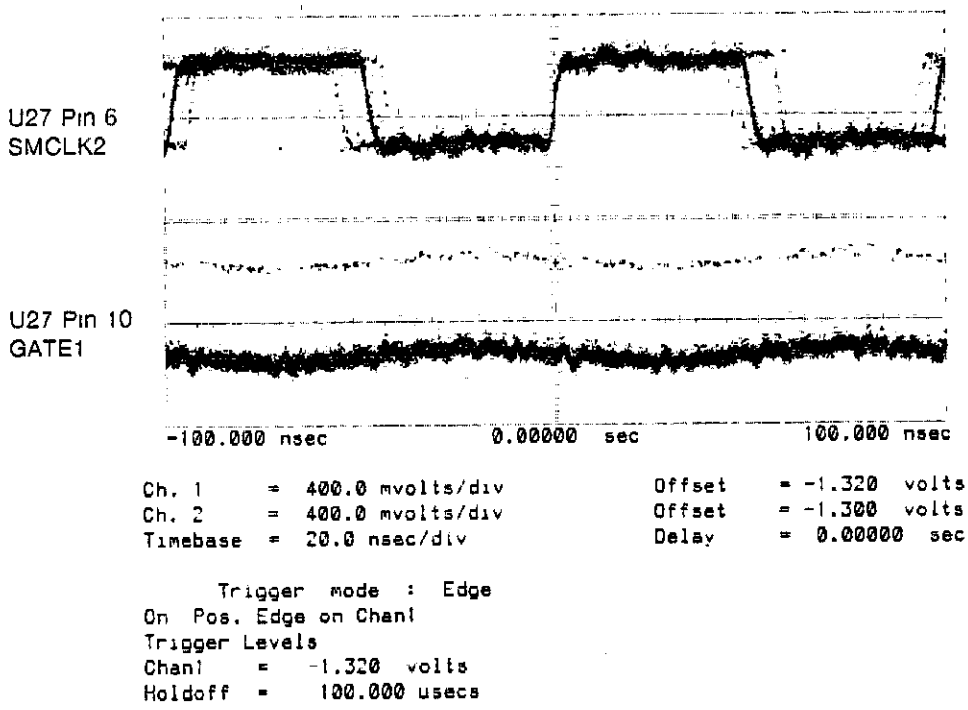


Figure 6E-31 Loop 35 Troubleshooting Waveforms at U27 Pins 6 and 10.

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LOOP 35A

This test checks for the presense of these boards:

TIMEBASE
ADC1
SAMPLER 1
TRIGGER

If these boards are not present, the following loops will not execute:

35
36
37

It can be verified that this part of the loop is failing by running REPEAT LOOP 35 for 30 seconds and then pressing STOP TEST. If this part of Loop 35 is failing, the status line on the display will indicate that it was trying to execute some other Loop than 35.

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6E-46. LOOP 36

SAMP1 - TRIGGER LEVEL DAC = +1/2 FULLSCALE

Description:

This test is exactly like Loop 35, except that the offset is set to +1/2 fullscale DAC range.

Status Register:

STATUS #1 - #4 - See Loop 35
VALID RANGE 1, 2 - 100-112
VALID RANGE 3, 4 - See Loop 35

Possible Causes of Failure:

1. Adjustments indicated - Same as Loop 35 plus offset and gain (on SAMPLE board being tested)

2. Boards indicated - Same as Loop 35

3. Functional blocks indicated - Same as Loop 35

Fault Diagnosis:

Same as Loop 35 except DAC Digital Value = 0480H (11 bits) and SAMPLER 1 control string = 0101000H. In addition, change the correct voltage at U5 pin 4 to - 3.674 V.

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6E-47. LOOP 37

SAMP1 - TRIGGER LEVEL DAC = ±1/2 FULLSCALE

Description:

This test is exactly like Loop 35, except that the offset is set to -1/2 fullscale of DAC Range. Fullscale is approximately 6V.

Status Register:

STATUS #1 - Status #4 - Same as Loop 35
VALID RANGE 1, 2 - 16-28
VALID RANGE 3, 4 - Same as Loop 35.

Possible Causes of Failure:

1. Adjustments indicated - Same as Loop 35 plus gain and offset (on SAMPLER board being tested)
2. Boards indicated - Same as Loop 35
3. Functional blocks indicated - Same as Loop 35

Fault Diagnosis:

Same as Loop 35, except offset DAC digital value = 0480H (+1/2 fullscales) and SAMPLER 1 control string is 01010004. In addition, change the correct voltage.

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6E-48. Loop 38

ADC 2 ID

Description:

The test is the same as Loop 34 except it tests ADC2.

Status Register:

Same as Loop 15

Possible Causes of Failure:

1. Adjustments indicated - None
2. Boards indicated - The loop will fail if either ADC1 or ADC2 is not responding. The way to tell which one is, is to remove ADC2 from SIB and execute REPEAT LOOP 34. If all executions fail, then ADC1 is failing. If all executions pass, then ADC2 is failing.
3. Functional blocks - Same as loop 34

Fault Diagnosis:

Same as Loop 15

Troubleshooting Tree.

1. Put the failing ADC in board extender.
2. Follow fault diagnostic steps 2 through 6 of Loop 15.

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6E-49. LOOP 39

SAMPLER2 - TRIGGER LEVEL DAC = 0

This loop has an "A" part. Troubleshoot Loop 39A first.

Description:

This test is exactly like loop 35, except that it tests SAMPLER2/ADC2 as opposed to SAMPLER1/ADC1. The offset is set to 0000H (11 bits) or 0 V.

Status Register:

Same as Loop 35.

Possible Causes of Failure:

Same as Loop 35 except use ADC2 instead of ADC1 and SAMPLER 2 instead of SAMPLER 1.

Fault Diagnosis:

Same as Loop 35 except use ADC2 instead of ADC1 and SAMP 2 instead of SAMP 1. In addition, substitute the words channel 2 for channel 1 and perform all adjustments to the channel 2 boards.

LOOP 39A

This part of Loop 39 looks for the presense of the following boards:

SAMPLER 2
ADC2
TIMEBASE
TRIGGER

If any of these boards are not present, the following loops will not execute:

39
40
41

You can verify that this part of Loop 39 is failing by running REPEAT LOOP 39 for 30 seconds and then pressing STOP TEST. If this part of the test is failing then the status line on the display will indicate that it was trying to execute some other Loop than 39.

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6E-50. LOOP 40

SAMPLER2 - TRIGGER LEVEL DAC = +1/2 FULLSCALE

Description:

This test is exactly like Loop 39 except that the offset DAC is set to +1/2 of its fullscale. Fullscale is approximately 6V. This loop is similar to Loop 36. In addition, the voltage value at U5 pin 4 is just as in Loop 36.

Status Register:

Same as Loop 35.

Possible Causes of Failure:

1. Adjustments indicated - Same as Loop 39 plus gain and offset (on SAMPLER BOARD being tested).
2. Boards indicated - Same as Loop 39.
3. Functional blocks indicated - Same as Loop 39

Fault Diagnosis:

Same as Loop 39, except offset DAC set to 0480H and SAMPLER 1 control string is 0101000H.

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6E-51. LOOP 41

SAMP2 - TRIGGER LEVEL DAC = -1/2 FULLSCALE

Description:

This test is exactly like Loop 39 except valid range for 1 and 2 is 16-28 and the offset is set to -1/2 fullscale. This loop is similar to Loop 37. The voltage value at U5 pin 4 is just as in Loop 37.

Status Register:

Same as loop 35.

Possible Causes of Problem:

Same as Loop 39 plus offset and gain (on SAMPLER board being tested) for adjustments indicated.

Fault Diagnosis:

Same as Loop 39 except offset DAC is set to 0480H and SAMP1 control string = 0101000H.

6E-52. LOOP 42

Not Applicable.

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6E-53. TRIGGER QUALIFIER LOOP S(43-6)0

Loops 43-60 test the Trigger Qualifier board. However, these loops are highly dependent on many of the other boards. Whenever a qualifier loop fails, the Qualifier should be removed and the oscilloscope wired like an "A" to verify whether the Qualifier board is causing the problem or not. If the "A" version passes all self tests, then the qualifier should be reinstalled and the qualifier loops should be troubleshot (not loops 0-41). This procedure will check all failures except ones where the Qualifier board is being pulled low or high by another board. However, this case can be verified by an ohm-meter.

For many of the qualifier loops, there are more than four failure modes. In order for the status register to display these codes, a different reporting scheme is used. In the first 43 loops, each status register is stored in RAM as a 16-bit word. If its value is not the power up value (-32768) then this is flagging an error. The qualifier loops need to allocate more than one error code:

```
example: -32768 = 8000H   - Default Value (No error)
         -32513 = 80 FFH  - GRR X L       (Lower byte reporting error)
         -255   = FF00H   - ERR X H       (Upper byte reporting error)
         -1     = FFFFH   - ERR X U└L     (Both bytes reporting error)
```

6E-54. OSCILLOSCOPE DOES NOT TRIGGER IN EDGE MODE.

1. Either the Qualifier board is pulling DOUT low when it should be high or the TCLK signals are not getting through. Pull the cable off of DOUT (J10) on the Trigger board. If the oscilloscope begins to trigger, the problem is in DOUT. If the oscilloscope still doesn't trigger, the problem is in the INB7-8030 or further back (trig SYNC comp., etc.).

2. When troubleshooting (except when running a REPEAT LOOP) always put the timebase in trg'd mode. When the oscilloscope autotriggers, it reprograms the Trigger and Qualifier board; which will generate errors throughout the system.

3. Use the edge mode to track down problems if possible. The easiest way to do this is to input the cal signal and trace it through the boards or use the procedure in the paragraph entitled VERIFYING EDGE TRIGGERING.

4. In edge mode and pattern entered/exited, the DOUT line is driven high through U7 Pin 3. Pins 13,14,15 on U7 should be low which causes pin 3 to go high, thus DOUT goes high. The three inputs are part of the control word: LSTATE = 0, SUBMODE = 0, and LS1-Ls4 = 1. (LS1-LS4 = 1 causes LQCLK = 0):. In edge/pattern entered (exited the QUAL board is actually in the state mode with a pattern of XXX (QCLK = 1) when present.

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6E-55. LOOP 43

QUALIFIER - POS/NEG EDGE SELECT

Description:

This loop sets up the trigger hardware so that trigger 4 is enabled while the rest of the other trigger sources are disabled. It is exactly like Loop 23 except the triggers are simulated by toggling the POS/NEG bit on the Qualifier board's trigger sync comparator.

Status Register:

Same as Loop 23.

Possible Causes of Failure:

1. Adjustments Indicated - Qualifier trigger hysteresis
2. Boards indicated - Sampler 1 and 2, Trigger, Qualifier
3 Functional Blocks Indicated - EXT4 slope line toggleing, holdoff status bit in trigger status register, holdoff shift, holdoff counter and register, both latch strobes, trigger qualifier control strings and registers,fast and slow trigger flip-flop, sampler 1 and 2 trigger comparators should be disabled, qualifier trigger sync comparator.

Fault Diagnosis:

Check the following points.

Sampler 1, Sampler 2, Trigger, Trigger Qualifier board, trigger sync comparators are disabled (ie at -.8V on U4 pins 1,6,12, and 17 of the Trigger Qualifier board).

Status bits should be set as follows:

STPD = 0
INTPD = 1
LS,-LS4 = 1
LE1,LE3 = 1
LE2 = 0
LE4 = 0
LSTATE = 0
DLYD = 0
SUBMODE = 0

All other status bits are set to their deasserted state.

Trig U9 pin 14 - 12 cycles/LIACK

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Probe The Following Points.

```
U4 Pin 8  (tclkout)
U1 Pin 14 (tclk4)

U4 Pin 8  (tclkout)
TP15      (DOUT)

U4 Pin 8  (tclkout)
U3 Pin 5  (opthldf)
```

If U1 pin 14 is wrong then replace the Trigger Qualifier (U1 is probably bad).

If U4 pin 8 is wrong and U1 pin 14 is good, then replace Trigger Qualifier. (U4 is probably bad).

If U3 pin 5 is wrong then replace the Trigger board.

If TP15 is wrong and not U3 pin 5, then replace Qualifier board.

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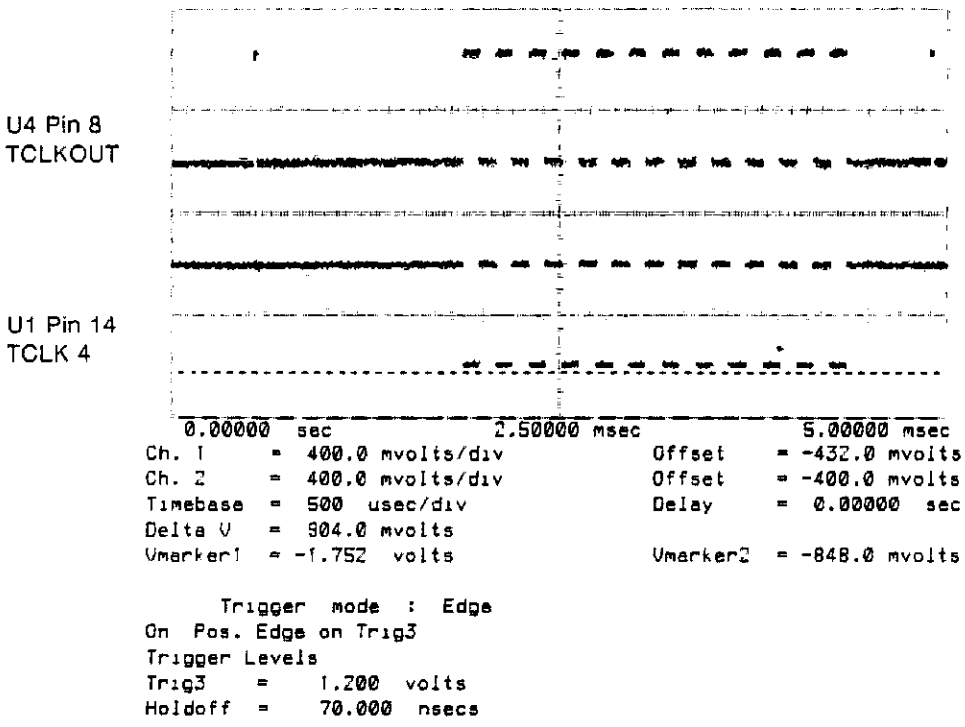


Figure 6E-32. Loops 43 and 44 Waveforms at U4 Pin 8 and U1 Pin 14.

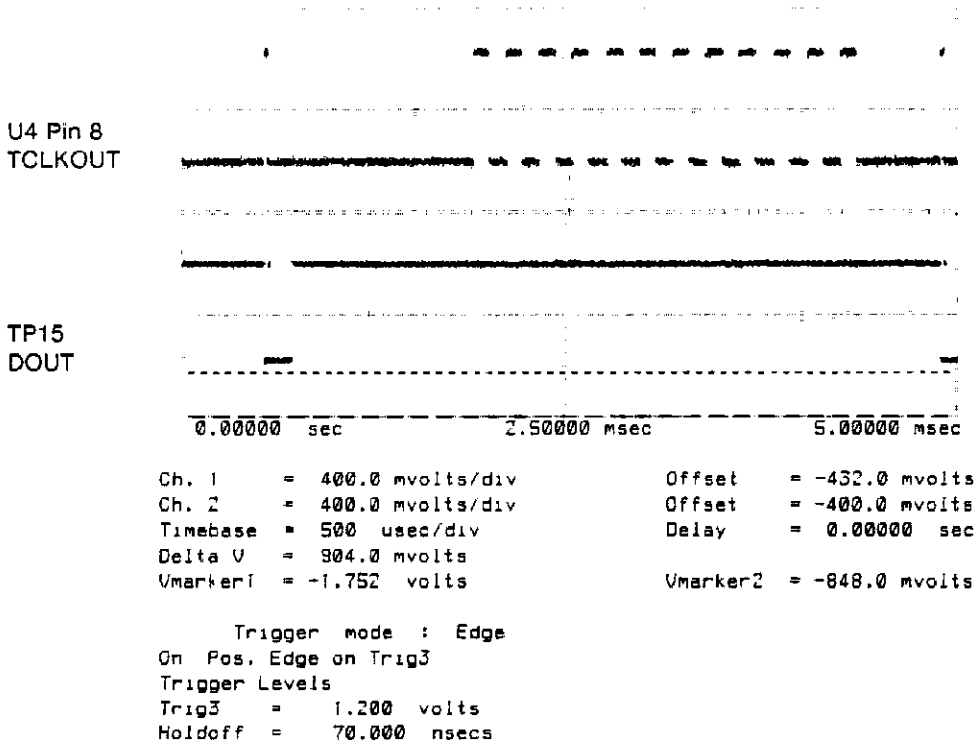


Figure 6E-33. Loops 43 and 44 Waveforms at U4 Pin 8 and TP15.

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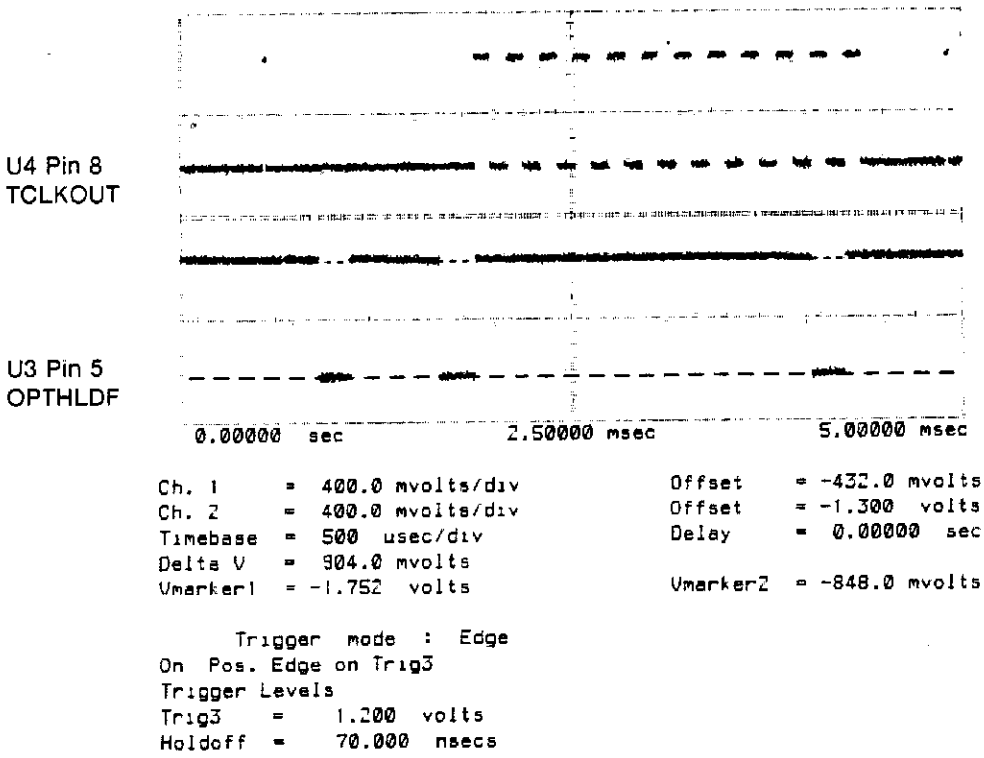


Figure 6E-34. Loops 43 and 44 Troubleshooting Waveforms at U4 Pin 8 and U3 Pin 5.

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6E-56. LOOP 44

QUALIFIER - PATTERN ENTERED/EXITED

Description:

This loop works exactly like Loop 43 except that the TCLKs coming from each channel are not inhibited by LE1 through LE4 at the trigger or hybrid. Thus if one of the TCLKs that is supposed to be disabled isn't, then this loop will fail. The Loop 43 test would fail for that reason. Therefore, Loop 43 really tests the TCLK 4 trigger comparator and Loop 44 tests all of the trigger comparators.

Status Register:

Same as Loop 43 except add trigger Sampler 1and 2 trigger hysteresis adjustments to the indicated adjustments.

Possible Causes of Failure:

Same as Loop 43.

Fault Diagnosis:

Same as loop 43 except LE1-LE4 should be asserted.

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6E-57. LOOP 45

QUALIFIER - STATE PRESENT/NOT PRESENT

Description:

In this test, the status of the trigger signal is monitored as the criteria conditions are entered (present) and exited (not present). The delay from the validity of the criteria to the enabling of the trigger flip-flop (F/F) is also tested. This is done by having the edge enter the valid criteria, and having a trigger edge of proper polarity. In the state present mode, TLCK 4 undergoes a rising edge. Previous to this TRGEN is false and the holdoff counter is awaiting a trigger event to go into holdoff by events. When this rising edge is received, the state goes from false to true and a trigger edge is seen by the trigger F/F. However, if the delay is correct, the edge happens before the F/F is enabled by TRGEN. These two conditions are reflected in the status bytes on each Trigger board. A similar but inverted situation exists for state not present. (Note: TRGEN is another name for DOUT). Trigger events are generated by toggling the trigger qualifier's slope line (U1 pin 18) while all four trigger comparators are disabled.

Status Register:

No indications.

Possible Causes of Failure:

1. Adjustments indicated - Sampler 1 and 2, main, and qualified trigger hysteresis
2. Boards indicated - Sampler 1 and 2, trigger, qualifier
3. Functional Block(s) indicated - ext 4 slope line toggling, holdoff status bit in trigger status register, holdoff shift, holdoff counter and register, both latch strobes on Trigger board, trigger qualifer control strings and control registers, fast and slow trigger flip-flops, Sampler 1 and 2 trigger comparators should be disabled, trig qual trigger comparator, state mode on qualifier TRGEN, QCLK.

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Fault Diagnosis:

Probe the following points.

```
U4 pin 8   (TCLKOUT)
U1 pin 14  (TCLK4)

U4 pin 8   (TCLKOUT)
TP15       (DOUT)

U4 pin 8   (TCLKOUT)
U3 pin 5
```

If U1 pin 14 is wrong, then replace the Trigger Qualifier (U1 is suspect).

If U4 pin 8 is wrong and U1 pin 14 is good, then replace the Trigger Qualifier (U4 is suspect.)

If U3 pin 5 is wrong, then replace the Trigger board.

If TP15 is wrong and U3 pin 5 is not, then replace Trigger Qualifier.

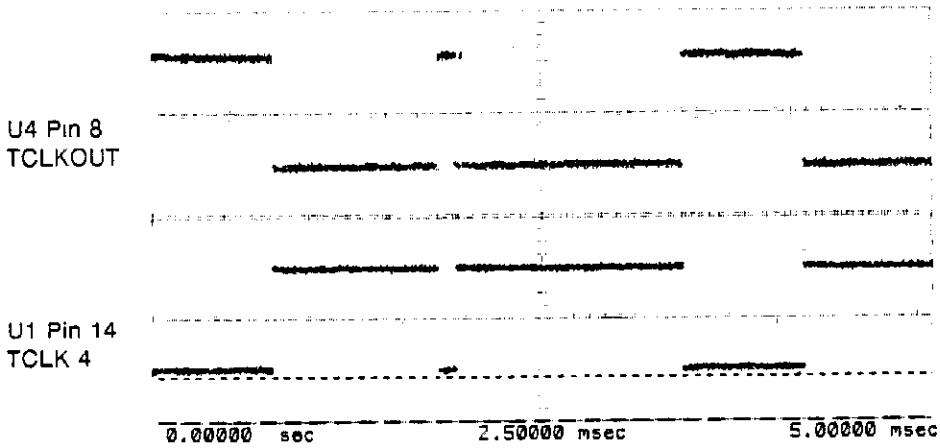
Check that the sampler1/sampler2/trigger/qualifier bd trigger sync comparators are disabled (ie at -.8v on U4 pins 1,6,12,17 of the Trigger Qualifier board).

Check U1 pin 18 on Trigger Qualifier board. It should look similar to U1 pin 14 except it is inverted.

Check that the following Trigger Qualifier control variables are set properly:

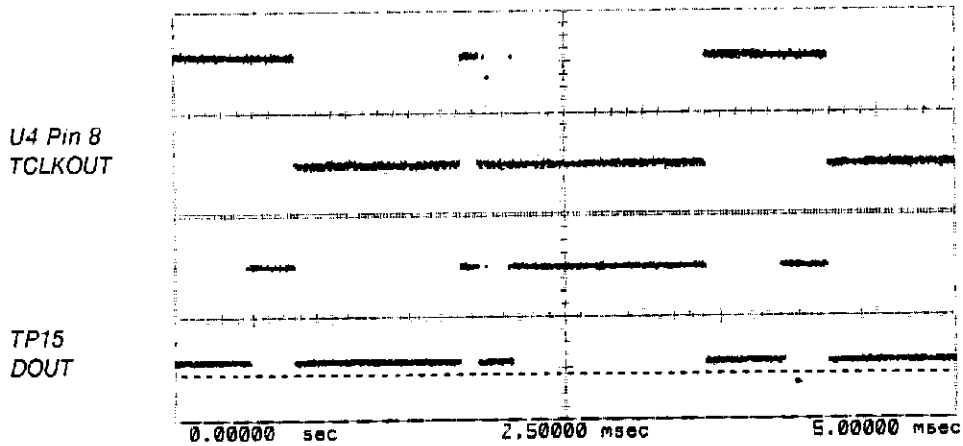
```
STPD       = DE-ASSERTED
INTPD      = SEE PRINTOUT
LS1-LS4    = ASSERTED
LE1-LE4    = DE-ASSERTED
LSTATE     = DE-ASSERTED
DLYD       = DE-ASSERTED
SUBMODE    = SEE PRINTOUT
C1         = DE-ASSERTED
LCO        = DE-ASSERTED
CL3        = De-ASSERTED
```


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```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  904.0 mvolts
Vmarker1   = -1.752  volts              Vmarker2   = -848.0 mvolts
      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-35. Loop 45 Troubleshooting Waveforms at U4 Pin 8 and U1 Pin 14.

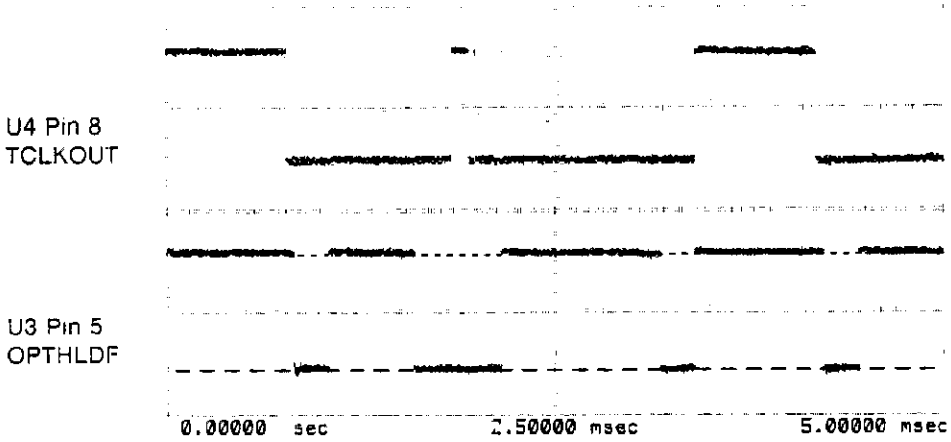



```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  904.0 mvolts
Vmarker1   = -1.752  volts              Vmarker2   = -848.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

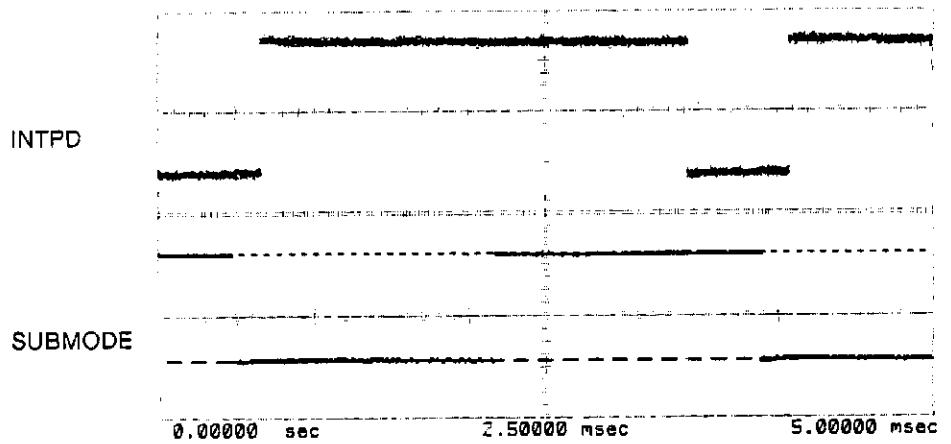
Figure 6E-36. Loop 45 Troubleshooting Waveforms at U4 Pin 8 and TP15.

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```
Ch. 1      =  400.0 mvolts/div          Offset    = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset    = -1.300  volts
Timebase   =  500  usec/div             Delay     =  0.00000  sec
Delta V    =  804.0 mvolts
Vmarker1   = -1.752  volts              Vmarker2  = -848.0 mvolts
      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-37 Loop 45 Troubleshooting Waveforms at U4 Pin 8 and U3 Pin 5.




```
Ch. 1      =  400.0 mvolts/div          Offset    = -1.300  volts
Ch. 2      =  2.000  volts/div          Offset    = -3.200  volts
Timebase   =  500  usec/div             Delay     =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2  = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-38. Loop 45 Troubleshooting Waveforms at INTPD and SUBMODE.

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6E-58. LOOP 46

DELAY BY EVENTS

Description:

This test operates as indicated on the previous page except that when QCLK goes true, it does not enable the counter, it makes TRGEN go true. This test and Loops 47-54 exercise the event delay circuitry on the qualifier. This difference between the tests lies in the fact of the number of events delayed. Each Loop (41-54) tests different parts of the 29-bit counter that allow different event delays.

For board level replacement purposes, Loop 46-54 will usually either all fail due to some other board causing the failure or only some of them will fail because of the Qualifier board. In addition, all of them can fail because the Qualifier is bad.

This loop tests the events counter when it is loaded with a value of 0, (which corresponds to a count of one trigger event). When in this mode, the count-start flip flop (U19-pin2) is routed to DOUT through U7 instead of routing the counter output to DOUT. Therefore, the counter is not thoroughly tested (except for ensuring the DOUT doesn't toggle unnecessarily). The Trigger board's trigger comparator is set to generate the QCLK by toggling the slope line on the Trigger board. The Trigger Qualifier board's trigger comparator generates the trigger events by toggling the slope line on the Trigger Qualifier board. The Trigger board is programmed for holdoff by 10 events. And the Trigger Qualifier board is set initially in a state that is awaiting a QCLK edge before arming the trigger flip-flop (on Trigger board) to trigger on TCLKOUT. TCLKOUT is pulsed which does not result in a trigger event since QCLK has not occurred yet. QCLK is then pulsed which causes DOUT to go high immediately. The next TCLKOUT edge will result in the trigger flip-flop outputting a trigger. This also asserts OPTHLDF which de-asserts DOUT and resets the qualified trigger back to its original state.

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Status Register:

No indication.

Possible Causes of Failure:

1. Adjustments indicated - Sampler 1 and 2, Trigger, and Trigger Qualifier hysteresis.

2. Boards indicated - trigger, qualifier, sampler1/2

3. Functional blocks indicated - TCLK3, TCLK4, QCLK, DOUT, Trigger and Qualifier board's trigger comparators, sampler1/2 trigger comparators are disabled, 29- bit counter, OPTHLDF

Fault Diagnosis:

Check to make sure that U4 pins 1 and 17 are at -.8. If pin 1 is bad then replace Sampler 2. If pin 17 is bad replace Sampler 1. Probe the following signals.

```
U4 Pin 8       (TCLKOUT)
U6 pin 2       (QCLK)

U19 pin 2      (count-start flip-flop)
TP 15          (DOUT)

U3 pin 3       (OPTHLDF)
U1 pin 18      (SLOPE)

U3 pin 2       (OPTHLDF)
U4 pin 6       (TCLK3)
```

If TCLKOUT is bad and if TCLK4 U1 pin 14 looks similar to U1 pin 18, then the Qualifier is bad (U1 suspected).

If DOUT is bad and TCLKOUT is good, then Qualifier is bad.

If DOUT is good and OPTHLDF is bad and if TCLKOUT is good, then replace Trigger board.

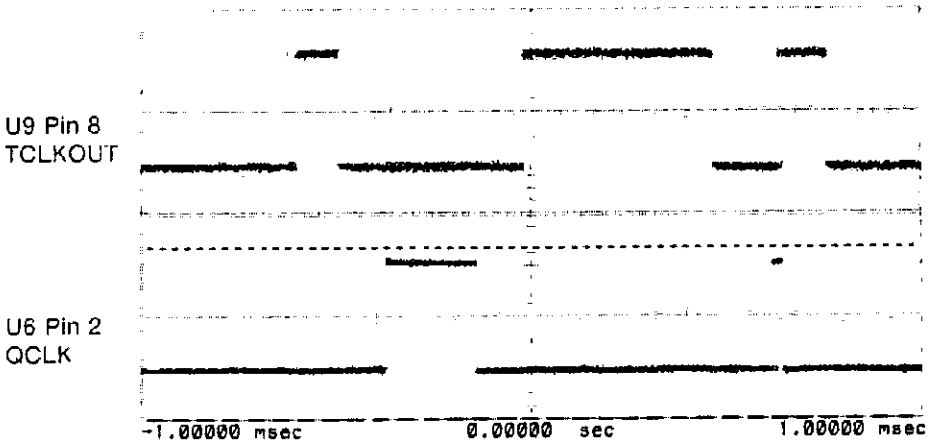
If QCLK is bad and TCLK out is good, then replace Trigger Qualifier board.

Check that the following status control values are valid:

```
INTPD    = 1          LE4      = 0
STPD     = 0          LSTATE   = 1
LS1-LS3  = 0          DLYD     = 1
LS4      = 1          SUBMODE  = 0
LE1-LE3  = 1          LCO      = 0
```

All other values are deasserted.

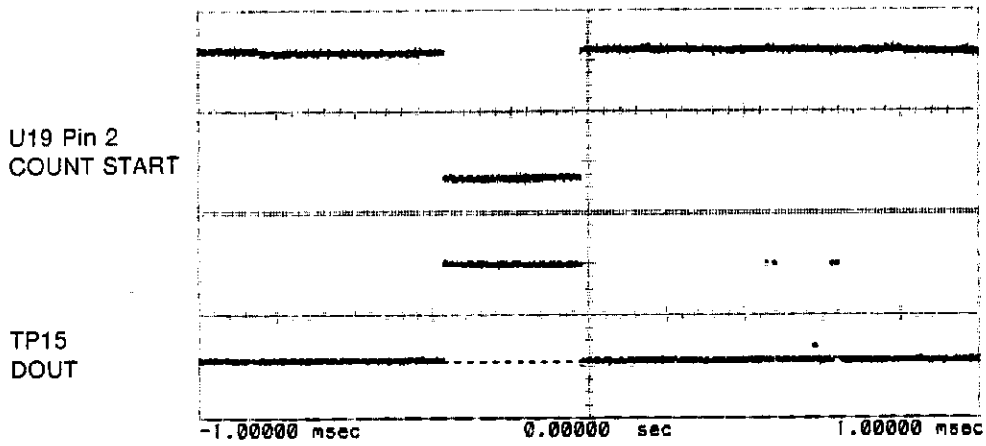
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.950  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-39. Loop 46 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.950  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-40. Loop 46 Troubleshooting Waveforms at U19 Pin 2 and TP15.

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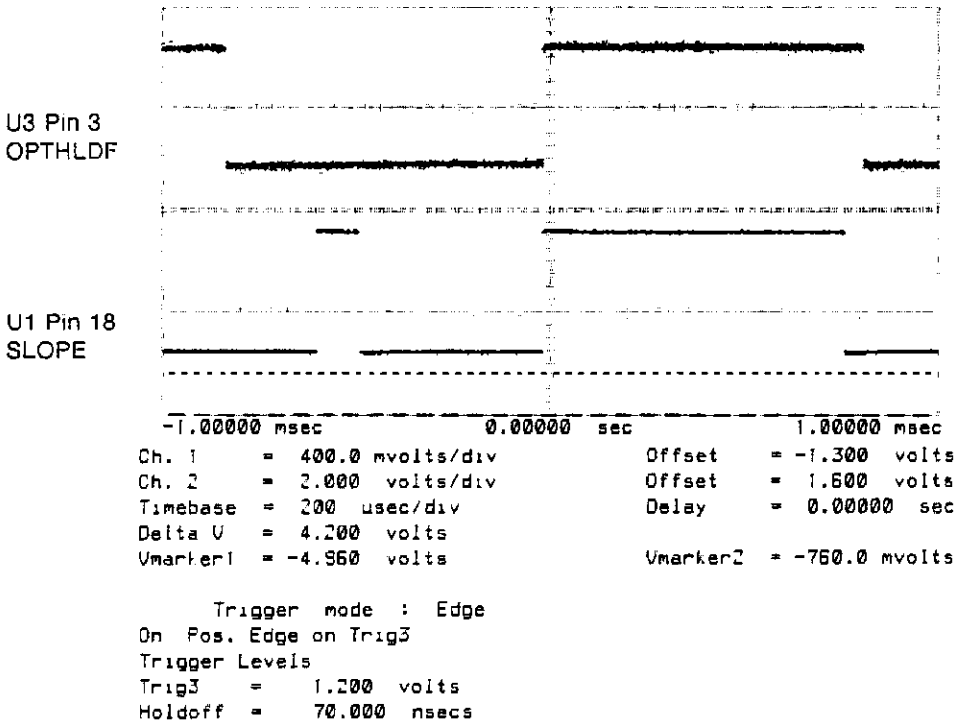


Figure 6E-41. Loop 46 Troubleshooting Waveforms at U3 Pin 3 and U1 Pin 18.

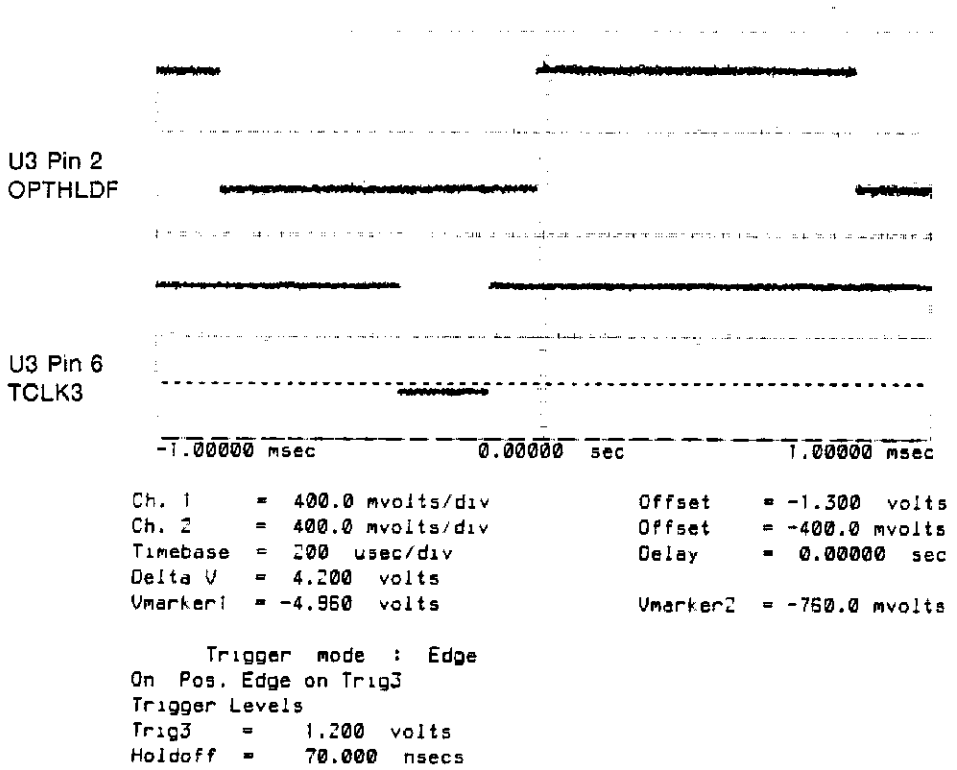


Figure 6E-42. Loop 46 Troubleshooting Waveforms at U3 Pin 2 and U4 Pin 6.

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6E-59. LOOP 47

DELAY BY EVENTS - COUNTER TIMING (LOAD = 1)

Description:

This test is exactly like Loop 46 except that the 29-bit counter is loaded with a value of 1. This loop tests different portions of the counter; but otherwise it tests the same circuitry. C1 and CL3 forces the D input of U20 pin 7 high through U21 pin 3. The first positive edge at TP1 causes U20 pin 3 to go low and after one clock the counter's output goes low. The long part of the 29-bit counter is ignored.

Status Register:

No indications.

Possible Causes of Failure:

Same as Loop 46 except the Sampler Trigger Hysteresis does not affect the test.

Fault Diagnosis:

Check to make sure that U4 pin 17,1 are at -.8V. If pin 17 is bad, replace Sampler 1. If pin 1 is bad replace Sampler 2.

Probe the following points for the following signals:

```
U4 pin 8      (TCLKOUT)
U6 pin 2      (QCLK)

U32 pin 3     (counter reload)
TP 15         (DOUT)

U3 pin 3      (OPTHLDF)
TP1           (counter clock)

U1 pin 18     (SLOPE)
U4 pin 6      (TCLK3)
```

Check for the following status register digital valves:

C1 = 0 LC2-LC3, LC5, LCL37, CL37, C6-629 = 0
LC0 = 1 CL3 =1 all other values are deasserted.

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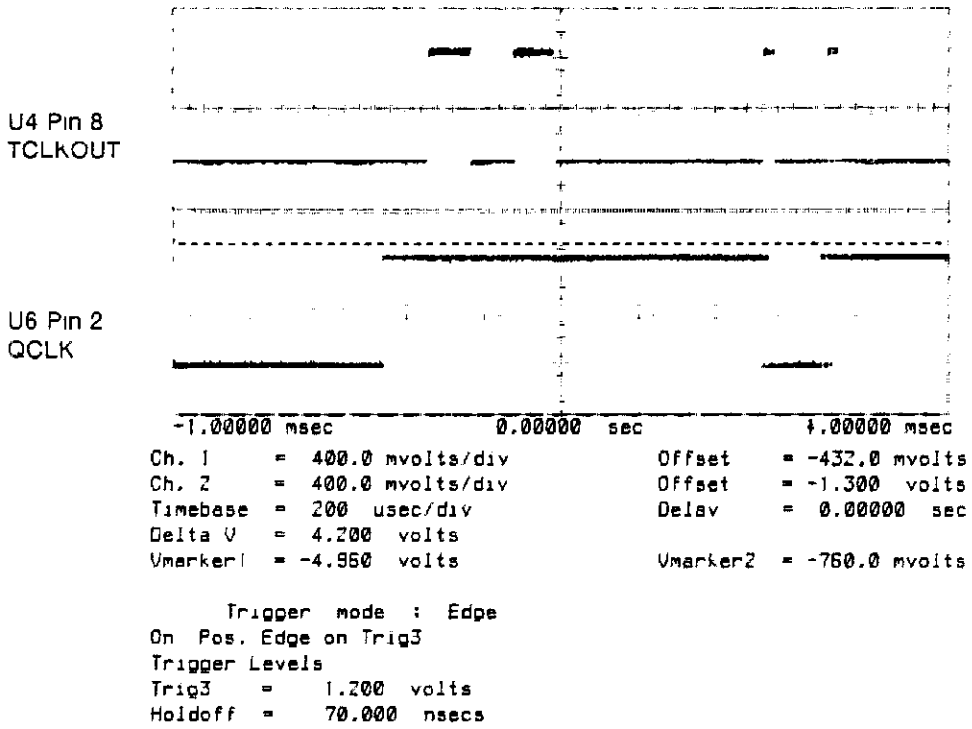


Figure 6E-43. Loop 47 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.

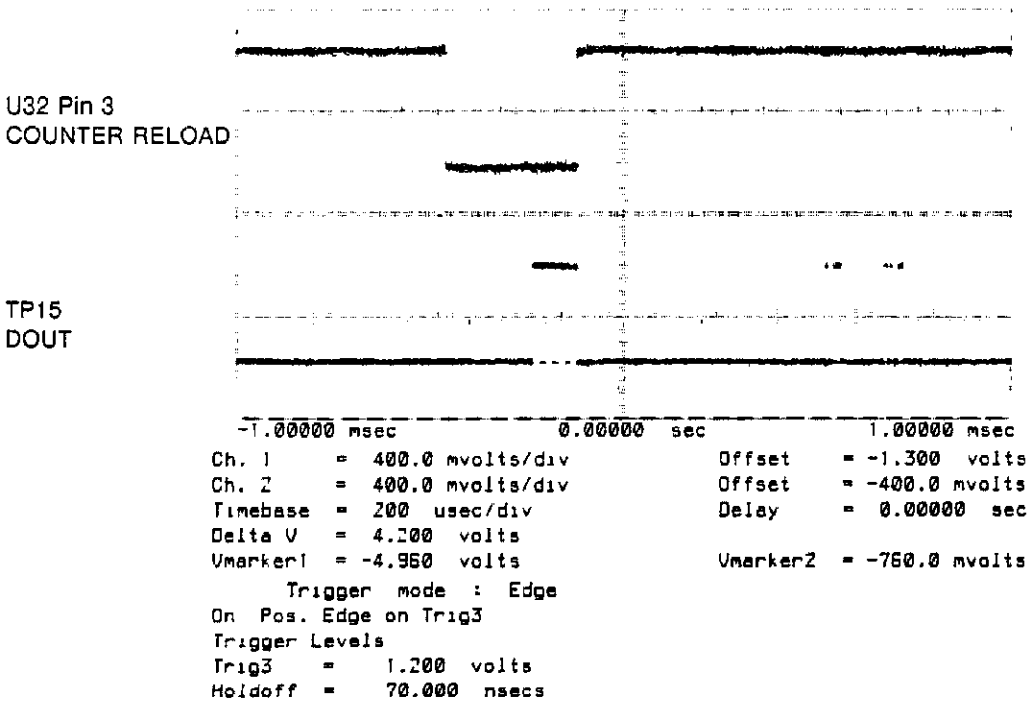
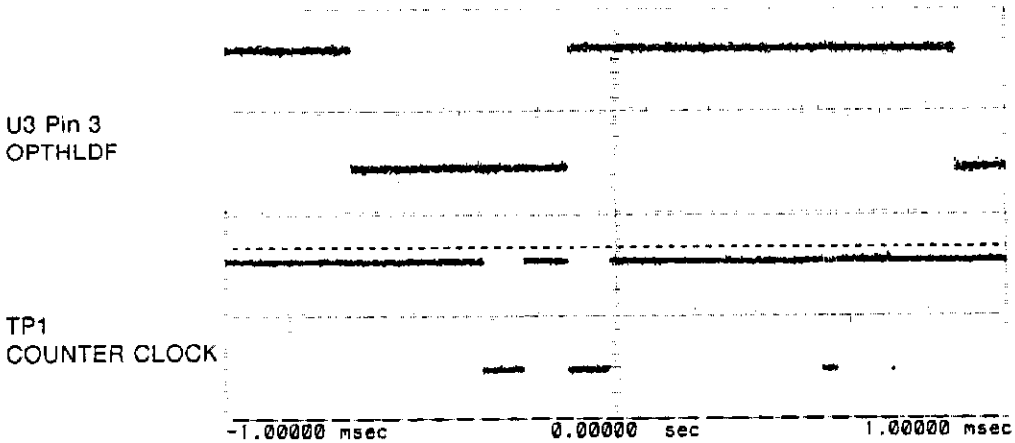


Figure 6E-44. Loop 47 Troubleshooting Waveforms at U32 Pin 15 and TP15.

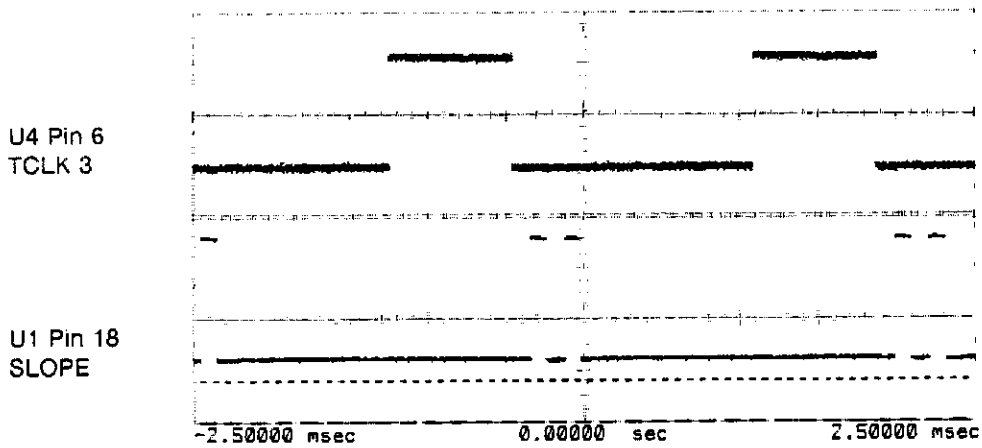
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-45. Loop 47 Troubleshooting Waveforms at U3 Pin 3 and TP1.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  2.000  volts/div          Offset     =  1.600  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-46. Loop 47 Troubleshooting Waveforms at U4 Pin 6 and U1 Pin 18.

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6E-60. LOOP 48

DELAY BY EVENTS - COUNTER TIMING (LOAD=2)

Description:

This test is exactly like Loop 46 except that the 29-bit counter is loaded with a value of 2; otherwise most of the circuits tested are exactly the same. However, a different part of the counter is checked. For this loop value, the entire long counter is ignored since CL3=1. The only signal inhibiting U20 pin 7 from going high is U20 pin 15. On the first positive edge of TP1, U20 pin 15 will go low which will allow LTLE to go low on the second edge of TP1.

Status Register:

No indications.

Possible Cause of Failure:

Same as Loop 46.

Fault Diagnosis:

Same as Loop 47 except probe these points.

```
U4 pin 8      (TCLKOUT)
U6 pin 2      (QCLK)

U32 pin 3     (counter reload)
TP15          (DOUT)

U3 pin 3      (OPTHLDF)
TP1           (counter clock)

U1 pin 18     (SLOPE)
U4 pin 6      (TCLK3)
```

Check the following trigger qualifier status register bits:

```
C1=1      LCL5=0
LC0=1     1C2-LC5, LCL5, CL37, LCL37.  C6-C29=0
```


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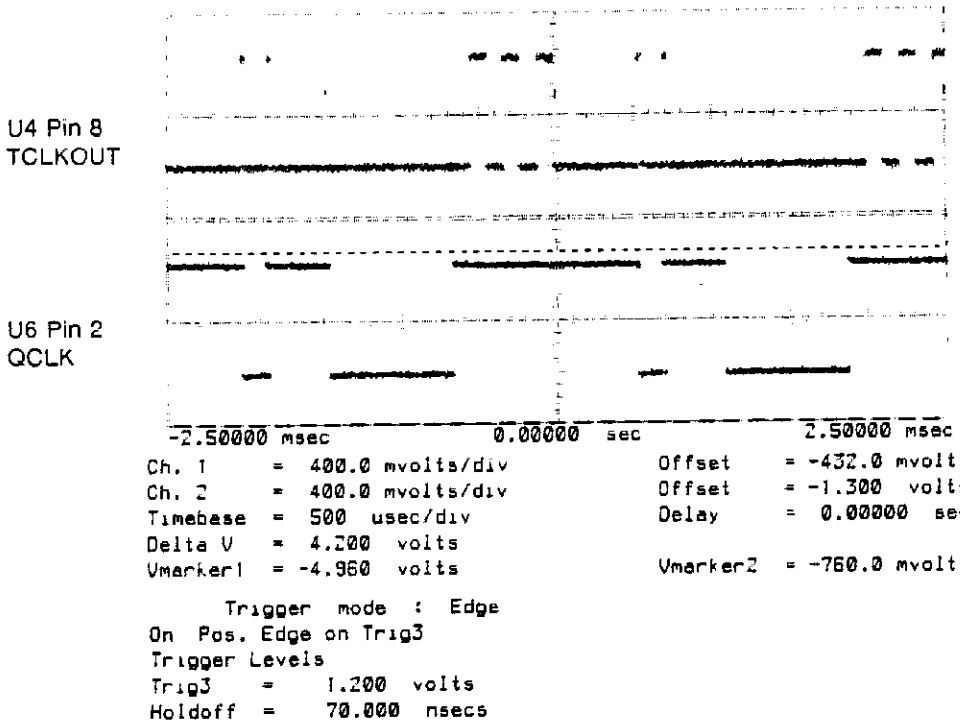


Figure 6E-47. Loop 48 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.

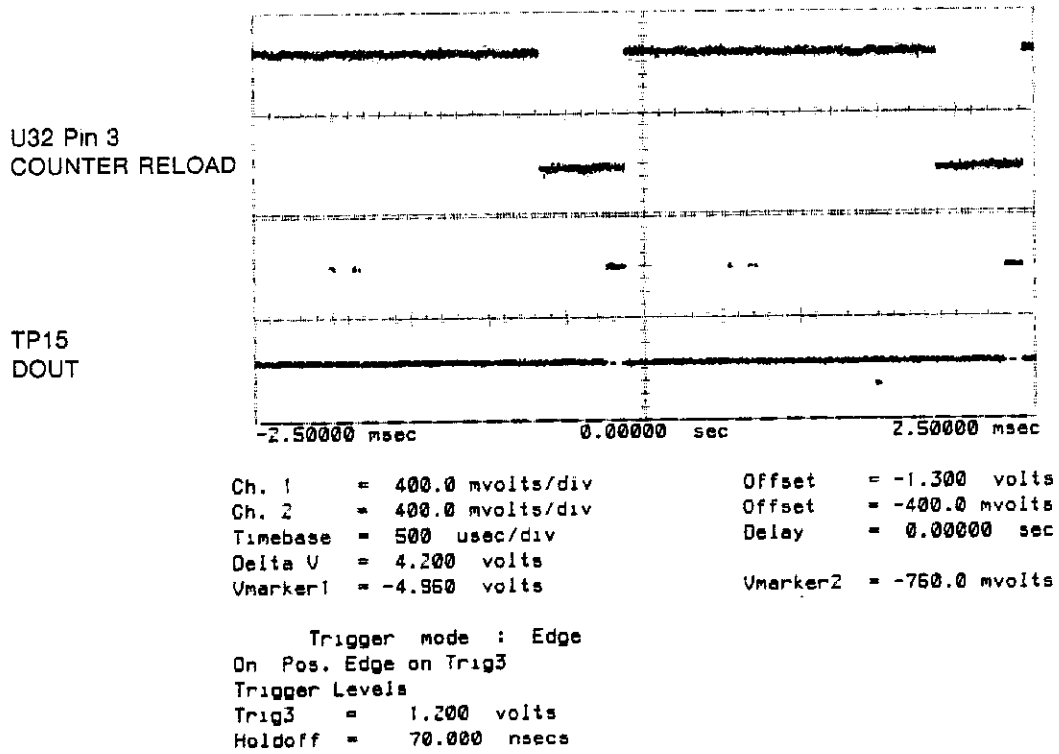


Figure 6E-48. Loop 48 Troubleshooting Waveforms at U32 Pin 3 and TP 15.

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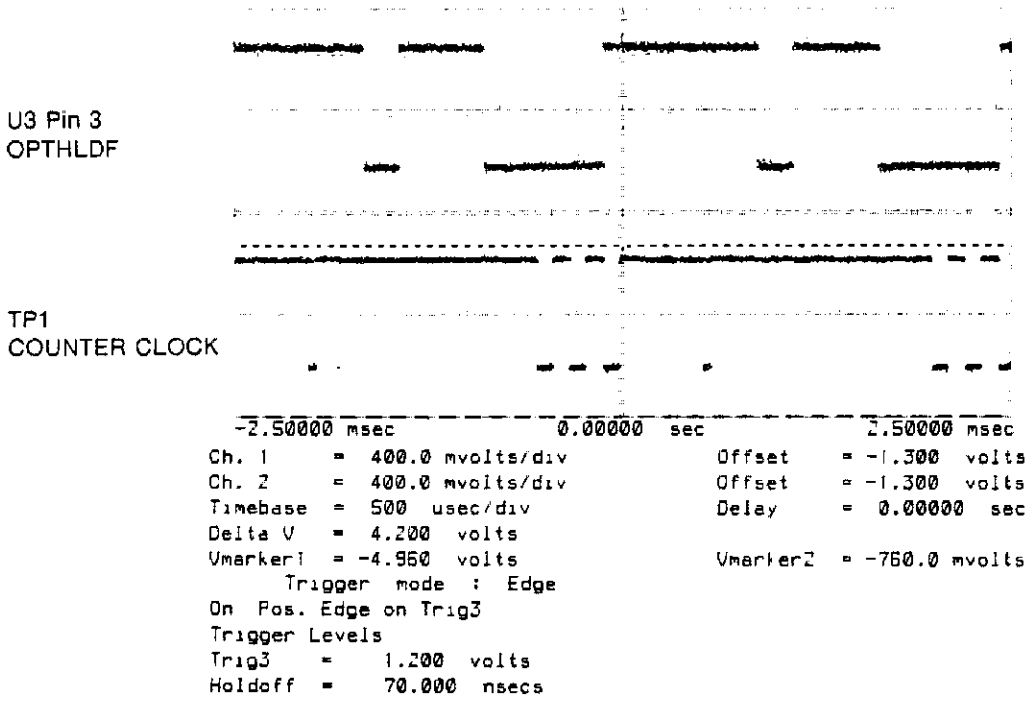


Figure 6E-49. Loop 48 Troubleshooting Waveforms at TP1 and U3 Pin 3.

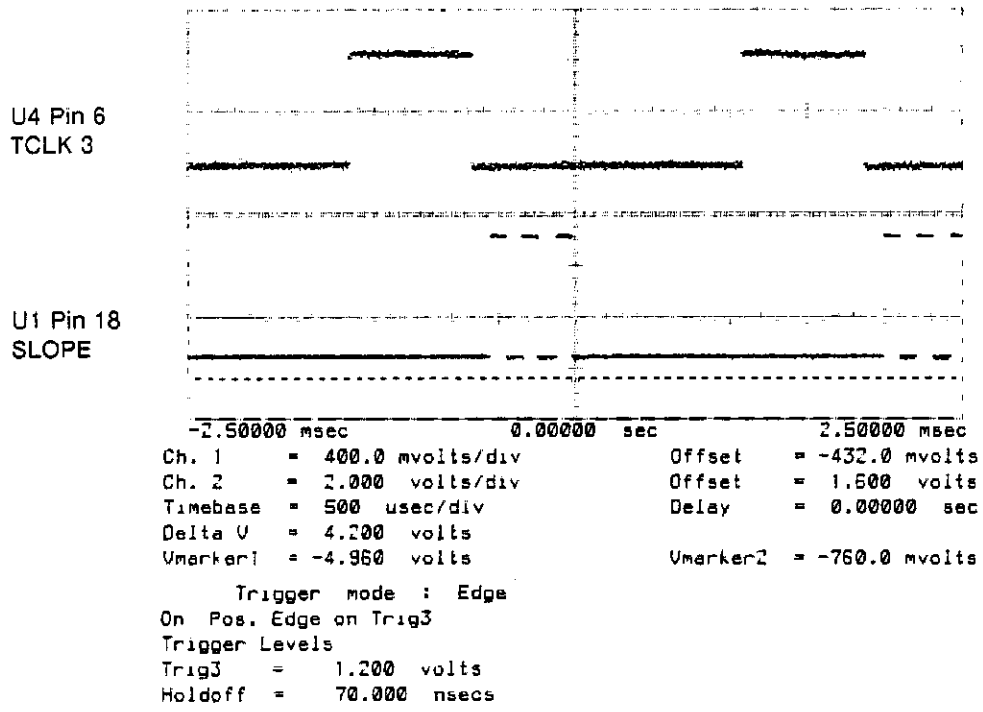


Figure 6E-50. Loop 48 Troubleshooting Waveforms at U4 Pin 6 and U1 Pin 18.

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6E-61. LOOP 49

DELAY BY EVENTS - COUNTER TIMING (LOAD=3)

Description:

This test is exactly like Loop 46 except that the 29-bit counter is loaded with a value of 3; otherwise the same hardware is tested. The long counter is still ignored because LCL5=0. The restart flip-flop (U20 pin 15) goes low on the first clock which then allows U23 pin 14 to go low on the second (U20 pin 15). U20 pin 7 goes high which allows LTLE to go low on the third clock (U10 pin 7 is forced low by LCL5=0).

Status Register:

No indications.

Possible Cause of Failure:

Same as Loop 46

Fault Diagnosis:

Same as Loop 47 except probe the following points.

```
U4 pin 8      (TCLKOUT)
U6 pin 2      (QCLK)

U32 pin 3     (counter reload)
TP15          (DOUT)

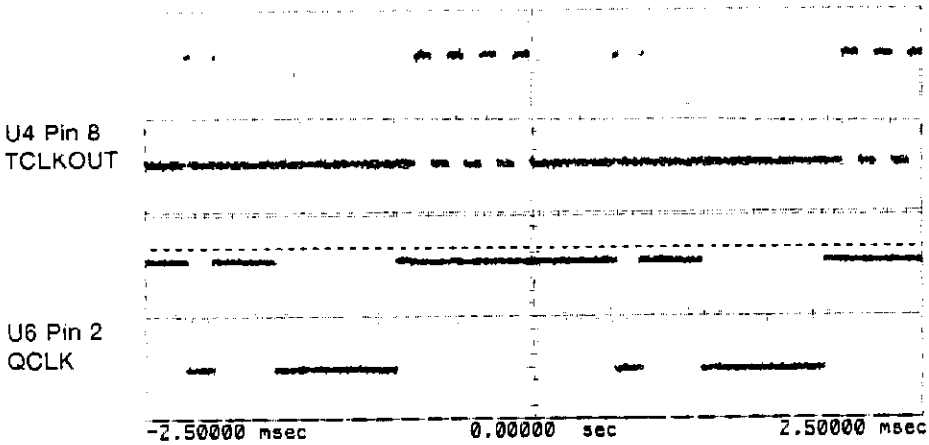
U3 pin 3      (OPTHLDF)
TP1           (counter clock)

U1 pin 18     (SLOPE)
U4 pin 6      (TCLK3)
```

Check the following digital trigger qualifier status register values:

C1=0, LC0=1, CL3=0, LCL5=0
LC2-LC5, CL37, LCL37, C6-C29=0
all others same as Loop 46.

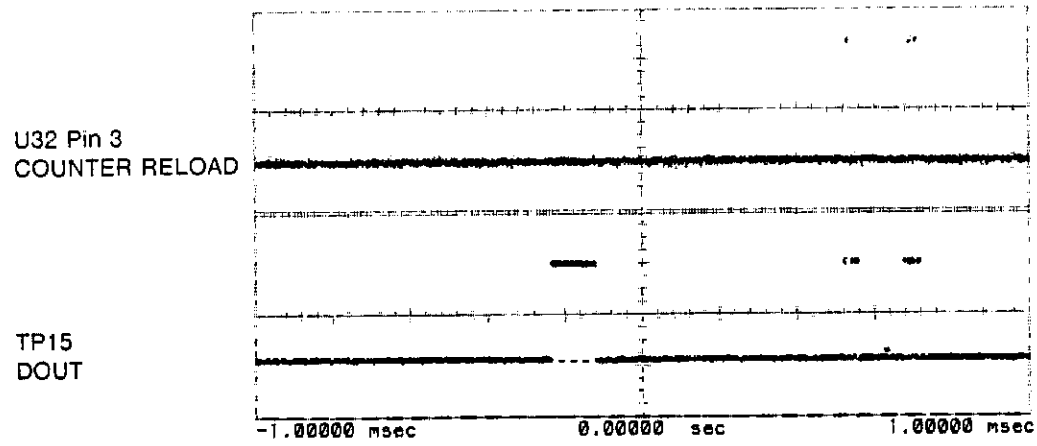
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```
Ch. 1      =  400.0 mvolts/div          Offset    = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset    = -1.300  volts
Timebase   =  500  usec/div             Delay     =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2  = -760.0 mvolts

      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =    70.000  nsecs
```

Figure 6E-51. Loop 49 Troubleshooting Waveforms at U4 Pn 8 and U6 Pin 2.

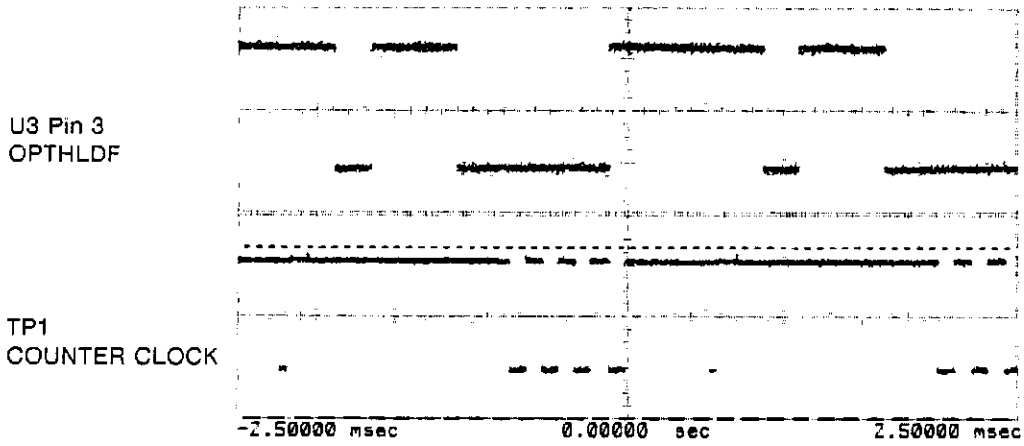



```
Ch. 1      =  400.0 mvolts/div          Offset    = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset    = -400.0 mvolts
Timebase   =  200  usec/div             Delay     =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2  = -760.0 mvolts

      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =    70.000  nsecs
```

Figure 6E-52. Loop 49 Troubleshooting Waveforms at U32 Pin 3 and TP15

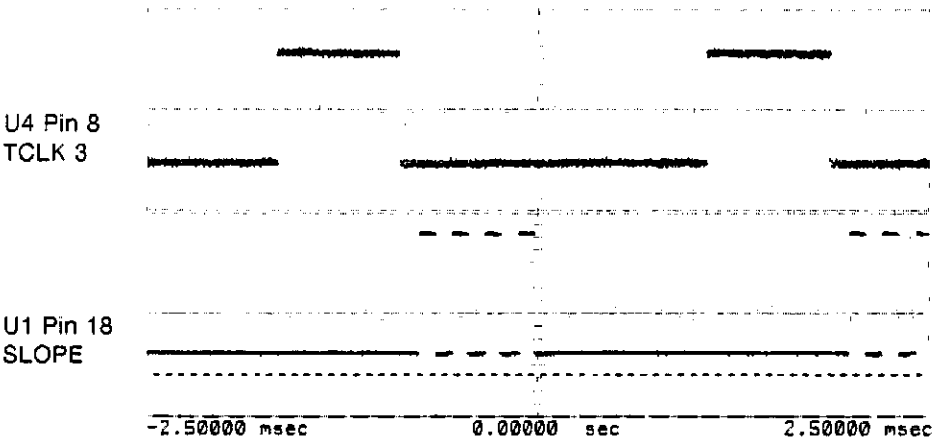
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-53. Loop 49 Troubleshooting Waveforms at U3 Pin 3 and TP1.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  2.000  volts/div          Offset     =  1.500  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-54. Loop 49 Troubleshooting Waveforms at U4 Pin 8 and U1 Pin 18.

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6E-62. LOOP 50

DELAY BY EVENTS - COUNTER TIMING (LOAD=4)

Description:

This loop is exactly like Loop 46 except that the 29-bit counter is loaded with a value fo 4; otherwise the same circuitry is tested. The long counter is ignored because LCL5=0. The restart flip-flop goes low on the first clock, which allows U23 pin 2 to go low on the second clock This allows U23 pin 14 to go low on the third clock. U20 pin 7 then goes high which sends LTCE (U20 pin 3) low on the fourth edge.

Status Register:

No indication.

Possible Cause of Failure:

Same as Loop 46.

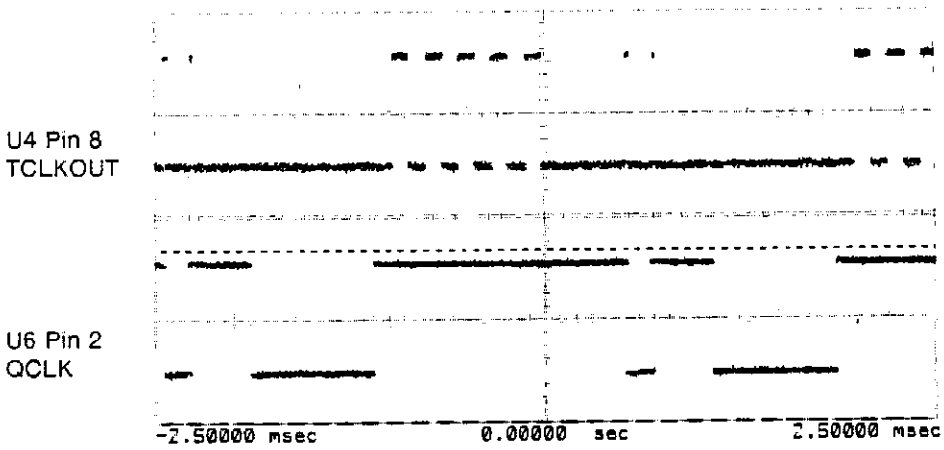
Fault Diagnosis:

Same as Loop 47 except use figures 6E-51through 6E-54.

Check the following digital trigger qualifier status register values:

C1=1
LC0=1
LCL3=0
LCL5=0
LC2-LC5, LCL37, CL37, C6-C29=0
All others are exactly like Loop 46

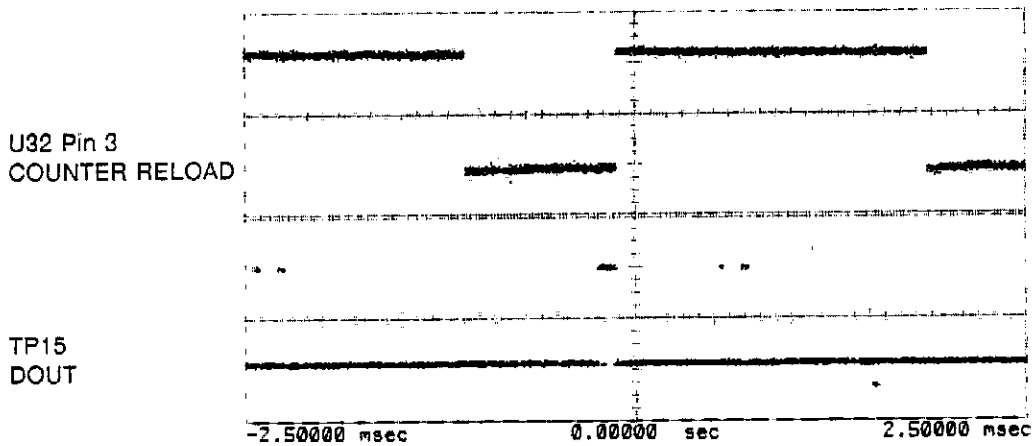
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-55. Loop 50 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-56 Loop 50 Troubleshooting Waveforms at U32 Pin 3 and TP15.

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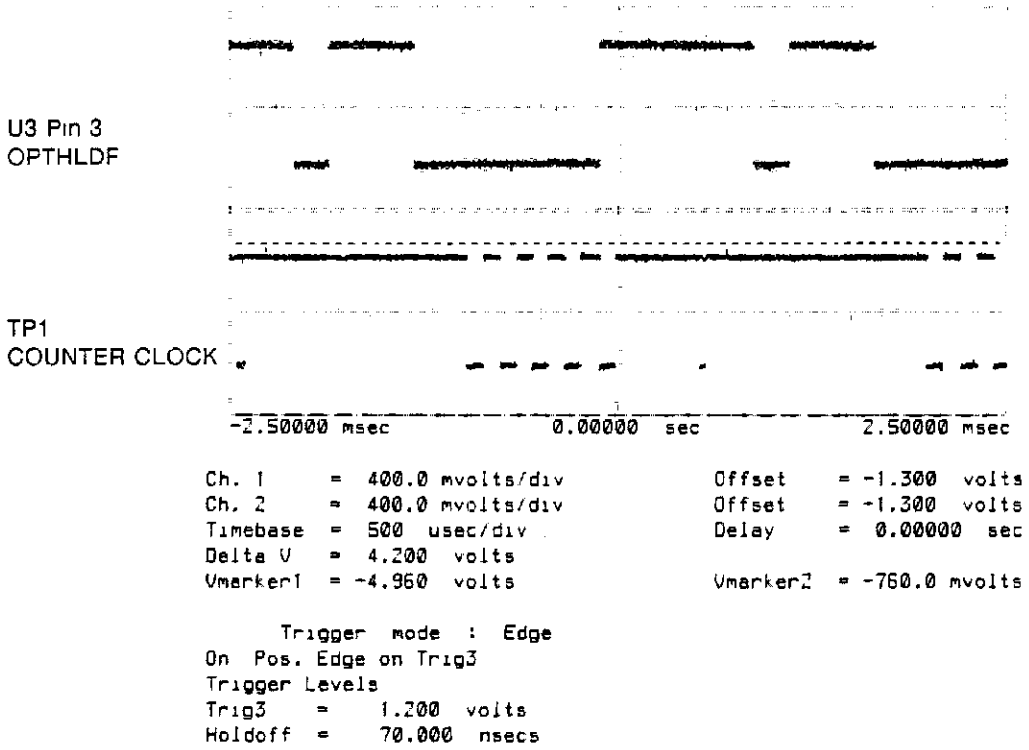


Figure 6E-57. Loop 50 Troubleshooting Waveforms at U3 Pin 3 and TP1.

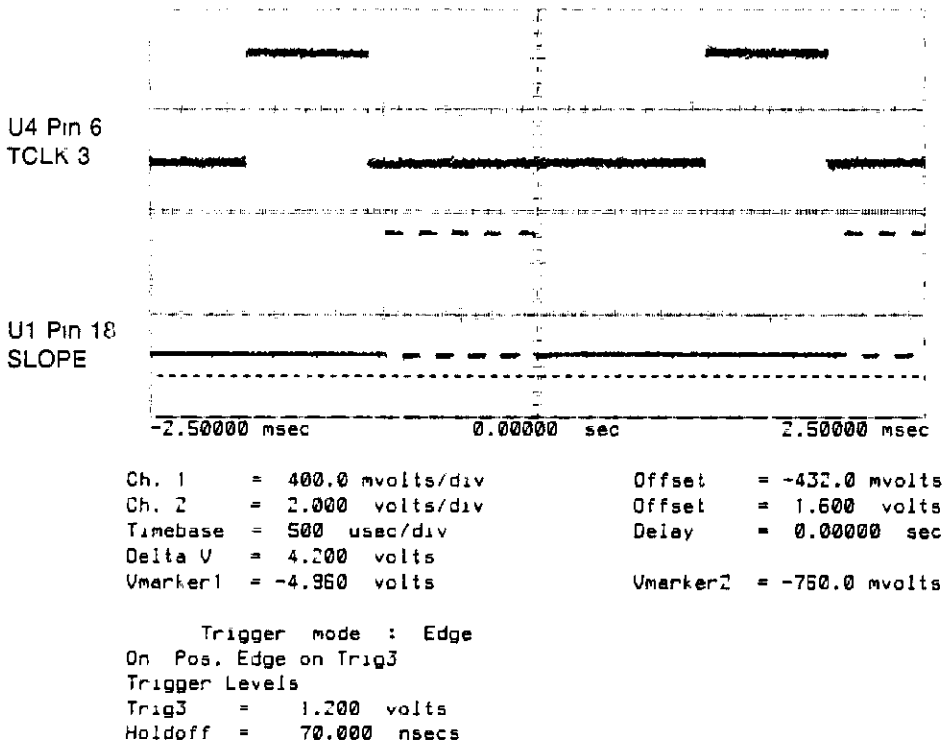


Figure 6E-58. Loop 50 Troubleshooting Waveforms at U4 Pin 6 and U1 Pin 18.

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6E-63. LOOP 51

DELAY BY EVENTS - COUNTER TIMING (LOAD=5)

Description:

This loop is exactly like Loop 46 except the 29-bit counter is loaded with a value of 5 which exercises the digital ground side of the long counter. U23 pin 2 (LRST) supplies the reset signal to long counter to initialize it. LCLK (U23 pin 14) supplies clocks to the long counter at the counter clock (TP1) divided by two. When the long counter times out, LLTC (U10 pin 7) goes low and U20 pin 7 goes low when LCLK goes low and LTCE goes low on the next transition of the counter clock (TP1) which in turn causes DOUT to go low.

On the first counter clock, LRST goes high and clears the up counter. LRST is removed from U12, and U13 on the second clock edge so these points will recognize the first LCLK which occurs on the fourth clock edge. Because CL37=1, LPE (U13 pin 5) on the up counter will be low when the first LCLK occurs so the up counter will load with LC2-LC5 (or all bits are one for load of five). This causes LTC on the output of the up counter to go low which sends LLTC (U10 pin 7) low. CL37=1 forces U12 pin 3 to stay low the entire loop and DISP (U26 pin 11) on the 1KC3 counter to stay low through U26 pin 22.

The up counter is U13. The 1KC3 is U26.

Status Register:

No indications.

Possible Causes of Failure:

Same as loop 46 except add the long counter, 1KC3 counter, and up counter to functional block lists.

Fault Diagnosis:

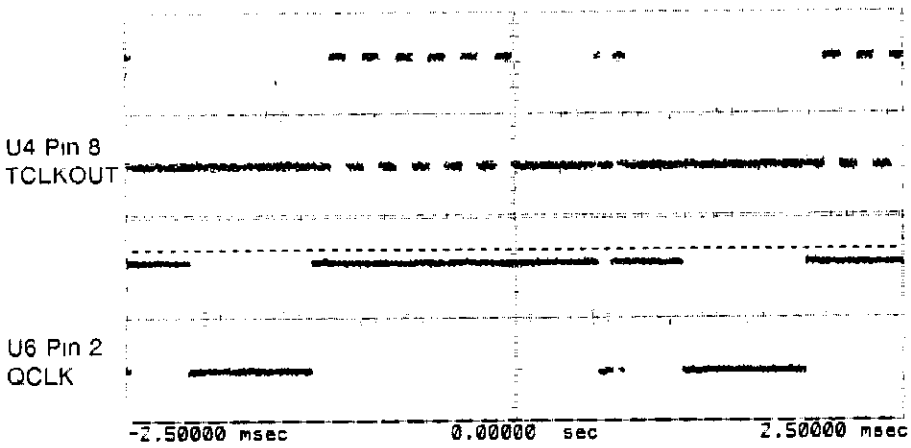
Same as Loop 47 except use figures 6E-55 through 6E-58.

Check the following trigger qualifier status register points:

C1=0	LCL5=1	C6-C29=0
LC0=1	LC2-LC5=1	LCL37=0
CL3=0	CL37=1	

All others are exactly the same as Loop 46.

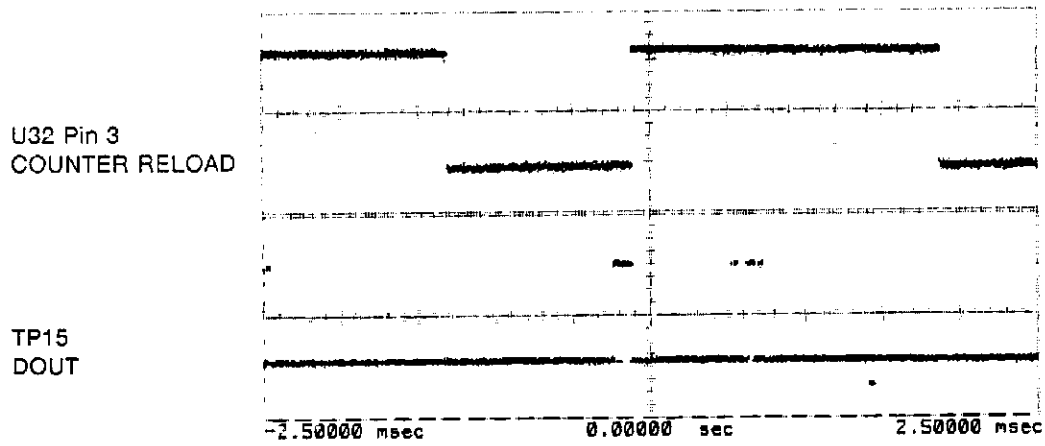
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-59. Loop 51 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.

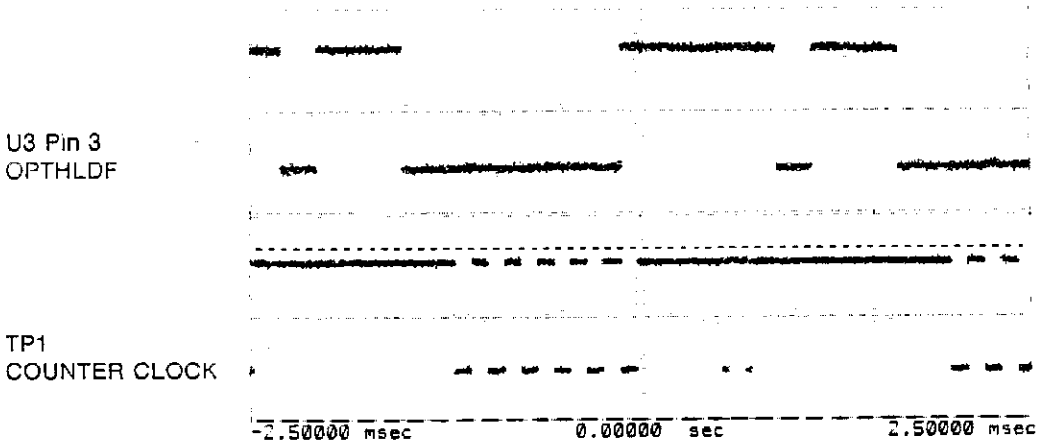



```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-60. Loop 51 Troubleshooting Waveforms at U32 Pin 3 and TP15.

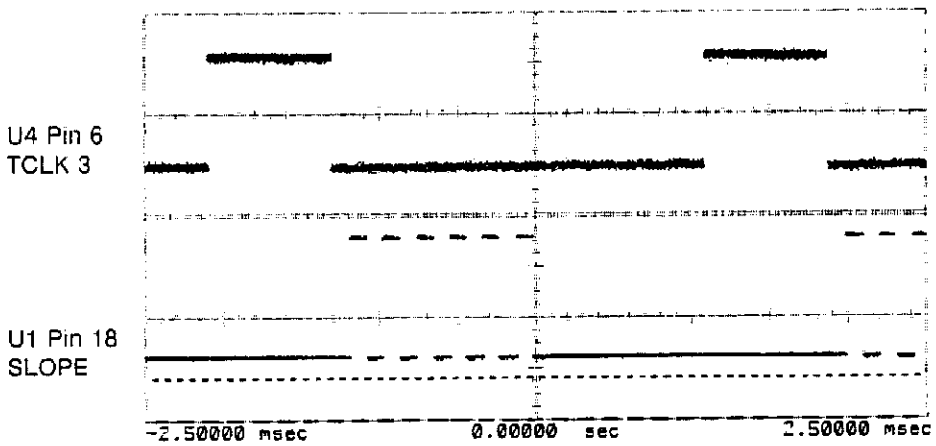
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-61. Loop 51 Troubleshooting Waveforms at U3 Pin 3 and TP1.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  2.000  volts/div          Offset     =  1.600  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-62. Loop 51 Troubleshooting Waveforms at U4 Pin 6 and U1 Pin 18.

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6E-64. LOOP 52

DELAY BY EVENTS - COUNTER TIMING (LOAD=36)

Description:

This loop works just like Loop 46 except that the 29-bit counter is loaded with a value of 36. The up counter part of the long counter is used but not the 1KC3 counter (because CL37=1). An edge at the RIL (U26 pin 22) input of the 1KC3 forces DISP (U26 pin 11) to output a low. U23 pin 14 (LCLK) supplies the reset signal (LRST) to the long counter to initialize it. U23 pin 2 (LRST) supplies clocks to the long counter at a rate that is TP1 divided by 2. LCLK continues clocking until the long counter times out and LLTC (U10 pin 7) is output. U20 pin 7 goes high when LCLK goes low. And the next counter clock (TP1) after that causes LTCE to go low which affects DOUT.

For a load of 36, the up counter is loaded with LC2-LC5=0. It then counts up to 15 (its terminal count) and sends LLTC low. U12 pin 3 and U26 pin 11 both stay low by CL37=1.

Status Register:

No indication.

Possible Cause of Failure:

Same as Loop 51.

Fault Diagnosis:

Same as Loop 47.

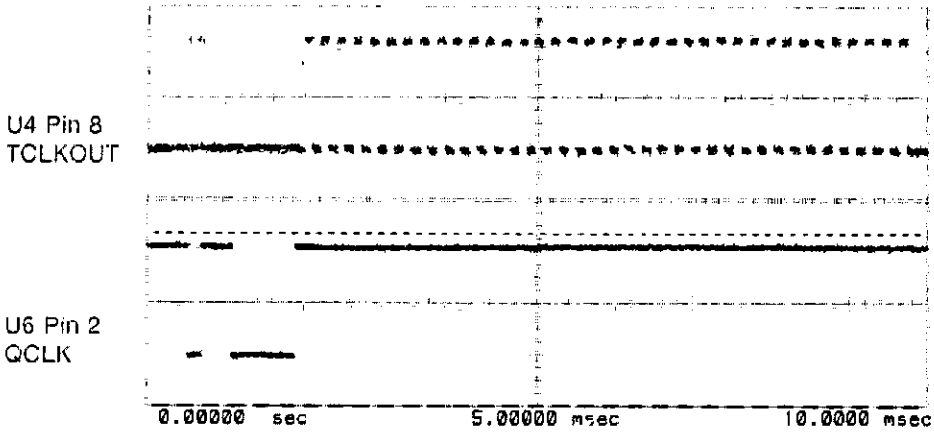
Check that the proper signals are set in the trigger qualifier control register.

C1=1	LC2-LC5=0
LC0=1	CL37=1
CL3=0	LCL37=0
LCL5=1	C6-C29=0

All others are the same as loop 46.

Probe the same points as Loop 47 except use figures 6E-63 through 6E-66.

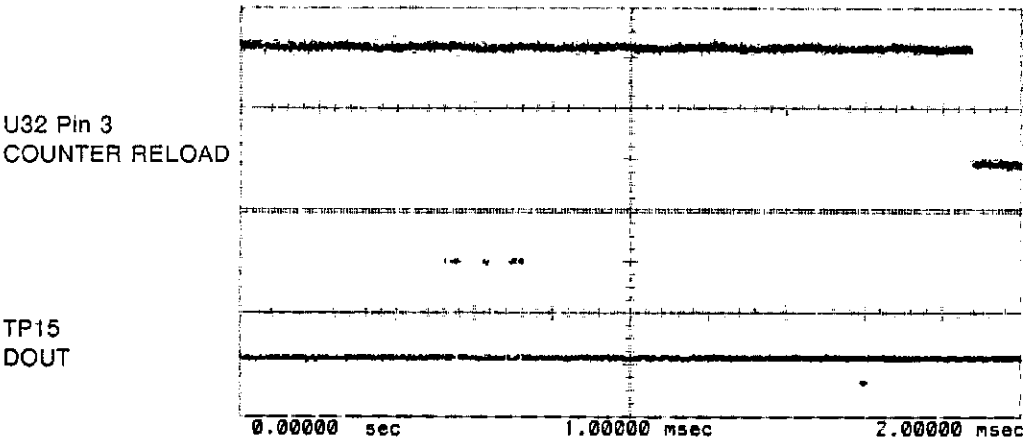
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  1.00 msec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-63. Loop 52 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.

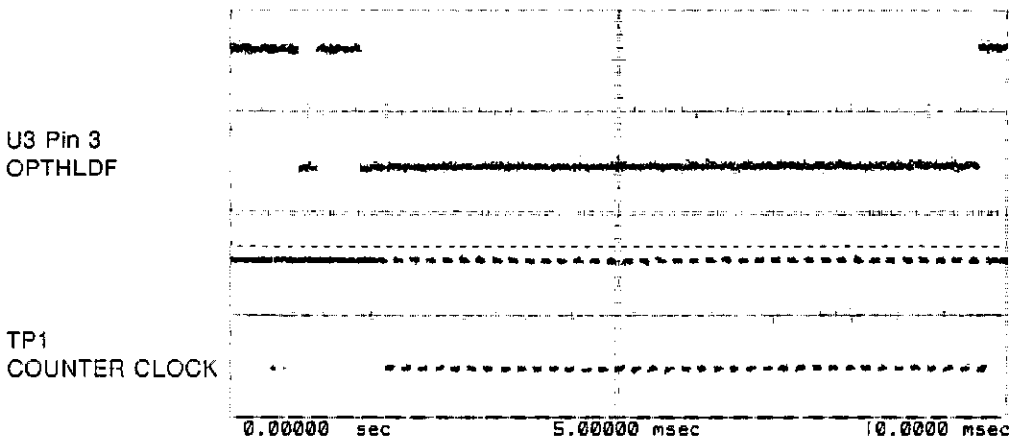



```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-64. Loop 52 Troubleshooting Waveforms at U32 Pin 3 and TP15.

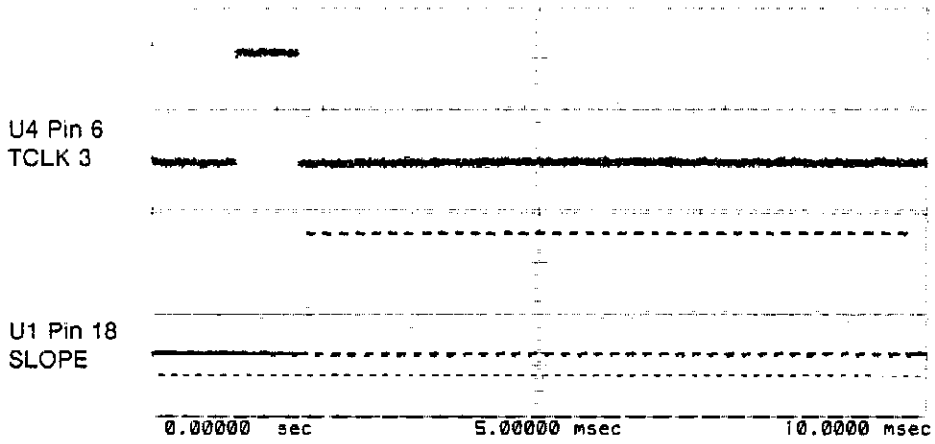
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  1.00 msec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-65. Loop 52 Troubleshooting Waveforms at U3 Pin 3 and TP1.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  2.000  volts/div          Offset     =  1.600  volts
Timebase   =  1.00 msec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-66. Loop 52 Troubleshooting Waveforms at U4 Pin 6 and U1 Pin 18.

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6E-65. LOOP 53

DELAY BY EVENTS - COUNTER TIMING (LOAD = 37)

Description:

The loop works just like Loop 46 except all parts of the long counter are in use. The 1KC3 is on because CL37=0 and is loaded with C6-C29 = 0. This causes DISP (U26 pin 11) to go low as soon as it receives LR2 (U26 pin 1). U23 pin 14 supplies LRST (U23 pin 2) to the long counter. U23 pin 2 (LCLK) clocks the long counter until the long counter sends LLTC low. U20 pin 7 will go high after LLTC low and LCLK low, then LTCE goes low on the next counter clock (TP1).

The up counter is reset by LRST going high on the first counter clock (TP1). It is then clocked up to 15 by LCLK. Instead of LLTC going low, U12 pin 3 will inhibit LLTC and cause the up counter to be loaded with LC2-LC5. Then LCLK clocks the up counter again and when it reaches 15 again LLTC goes low. (In this test it is the next LCLK since LC2-LC5=1). U12 pin 3 will also go low when LLTC goes low so that the up counter is only loaded once. Since the 1KC3 counter is counted by LR2, and LR2 goes low at LLTC, DISP goes low when LLTC goes low.

The difference between load=36 and load=37 is that U12 pin 3 is allowed to operate for load=37.

Status Register:

No indication.

Possible Cause of Failure:

Same as Loop 51 except that U12 is also checked.

Fault Diagnosis:

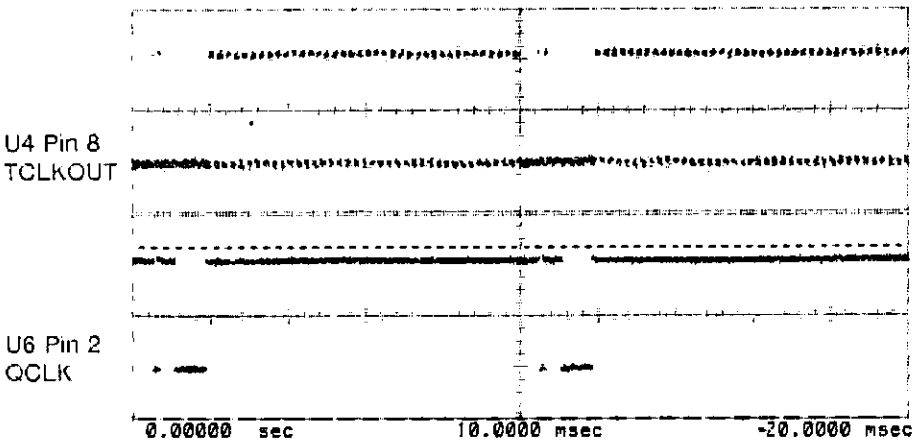
Same as Loop 47 except use figures 6E-63 through 6E-66.

Check for trigger qualifier control register values of:

C1=0	C6-C29=0
LC0=1	LC2-LC5=1
CL3=0	CL37=0
LCL5=1	LCL37=1

All others the same as Loop 46.

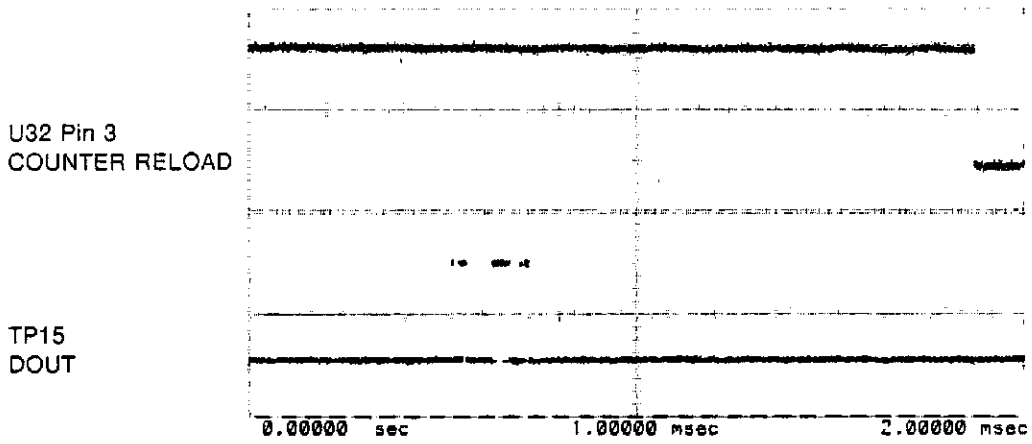
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  2.00 msec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-67. Loop 53 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.

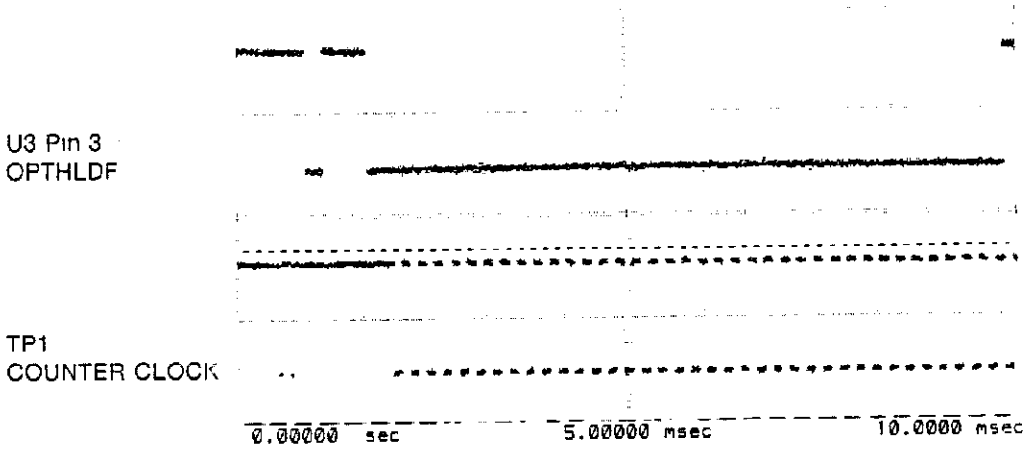



```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-68. Loop 53 Troubleshooting Waveforms at U32 Pin 3 and TP15.

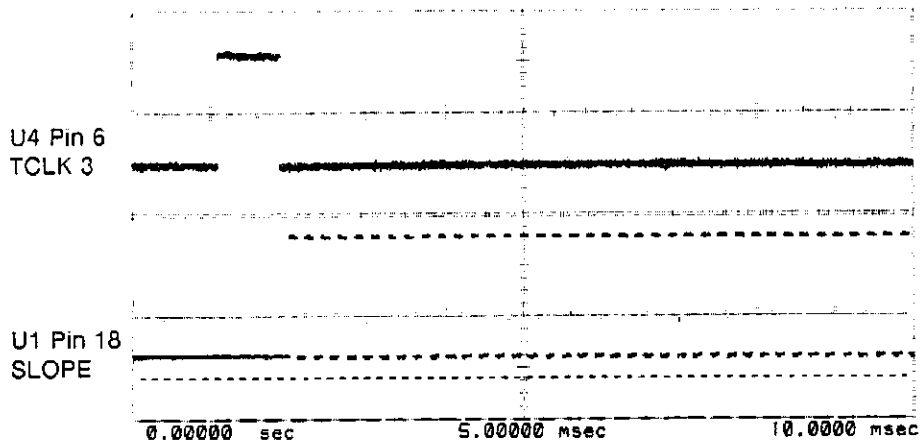
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  1.00 msec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-69. Loop 53 Troubleshooting Waveforms at U3 Pin 3 and TP1.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  2.000  volts/div          Offset     =  1.600  volts
Timebase   =  1.00 msec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-670 Loop 53 Troubleshooting Waveforms at U4 Pin 6 and U1 Pin 18.

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6E-66. LOOP 54

DELAY BY EVENTS - COUNTER TIMING (LOAD=69)

Description:

This loop works just like Loop 53 except that for all values above load=36, all parts of the long counter are tested. This test loads the 1KC3 with a value of one which means the 1KC3 will have to be clocked once before DISP goes low thereby causing LTCE and DOUT to go low.

The up counter is reset by LRST. It then counts upward and clocks the 1KC3 every time it rolls over from 15 to 0 when DISP is high. Therefore, the up counter counts to 15, then clocks 1KC3, then DISP goes low, then the up counter goes to 15 and this causes the LC2-LC5 to be loaded into the up counter (since DISP is low). The up counter will then start from this loaded value and then count up to 15 again. In this case LC2-LC5=1. Therefore, LLTC (U10 pin7) will go low when the up counter is loaded and U12 pin 3 goes low simultaneously.

Status Register:

No indications.

Possible Cause of Failure:

Same as Loop 51 except the 1KC3 counter is tested more thoroughly.

Fault Diagnosis:

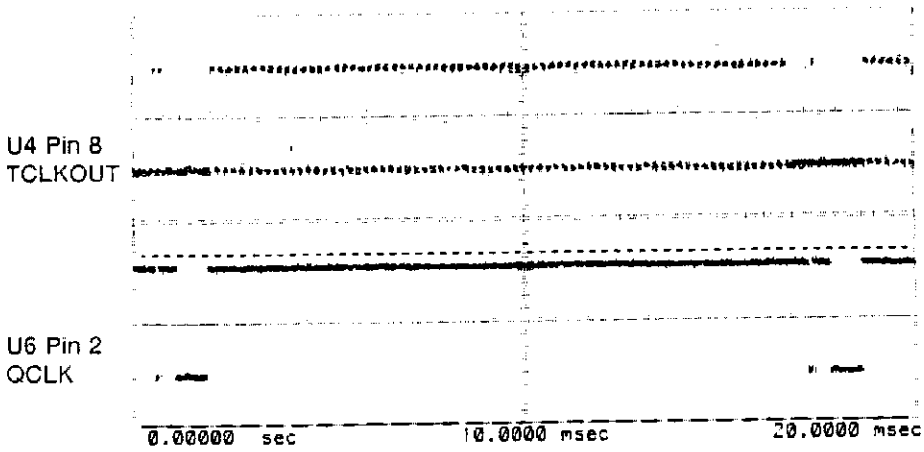
Same as Loop 47 except use figures 6E-67 through 6E-70.

Check for trigger qualifier control register values of:

C1=0	LC2-LC5=1	C7-C29=0
LC0=1	CL37=0	
CL3=0	LCL37=1	
LCL5=1	C6=1	

All points are exactly the same as Loop 46.

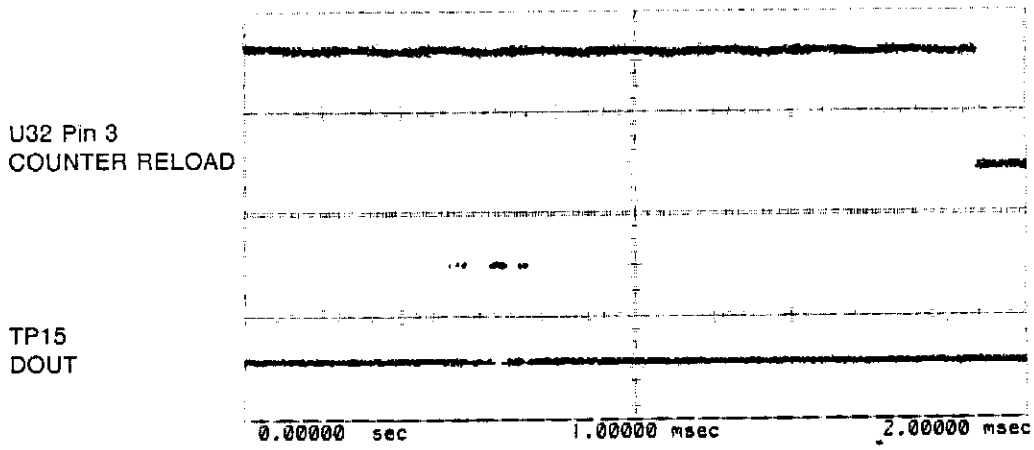
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```
Ch. 1     =  400.0 mvolts/div          Offset    = -432.0 mvolts
Ch. 2     =  400.0 mvolts/div          Offset    = -1.300  volts
Timebase  =  2.00 msec/div             Delay     =  0.00000  sec
Delta V   =  4.200  volts
Vmarker1  = -4.960  volts              Vmarker2  = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =    1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-71. Loop 54 Troubleshooting Waveforms at U4 Pin 8 and U6 Pin 2.

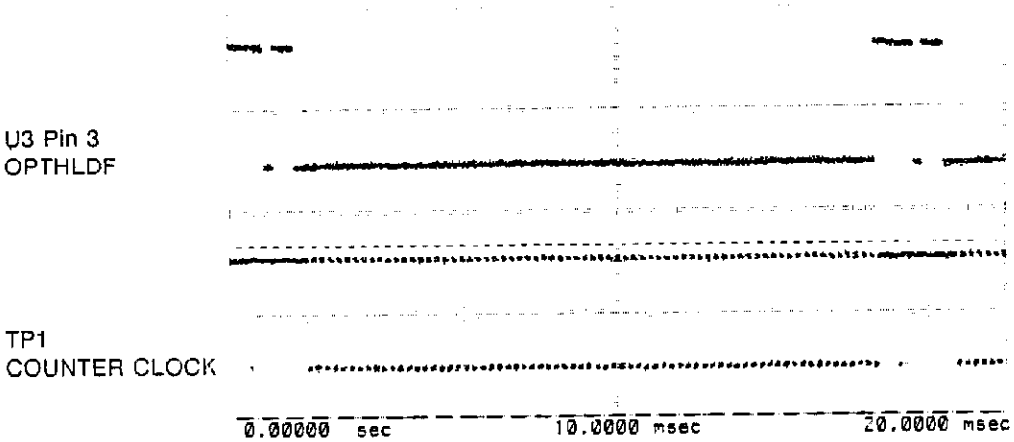



```
Ch. 1     =  400.0 mvolts/div          Offset    = -1.300  volts
Ch. 2     =  400.0 mvolts/div          Offset    = -400.0 mvolts
Timebase  =  200  usec/div             Delay     =  0.00000  sec
Delta V   =  4.200  volts
Vmarker1  = -4.960  volts              Vmarker2  = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =    1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-72. Loop 54 Troubleshooting Waveforms at U32 Pin 3 and TP15.

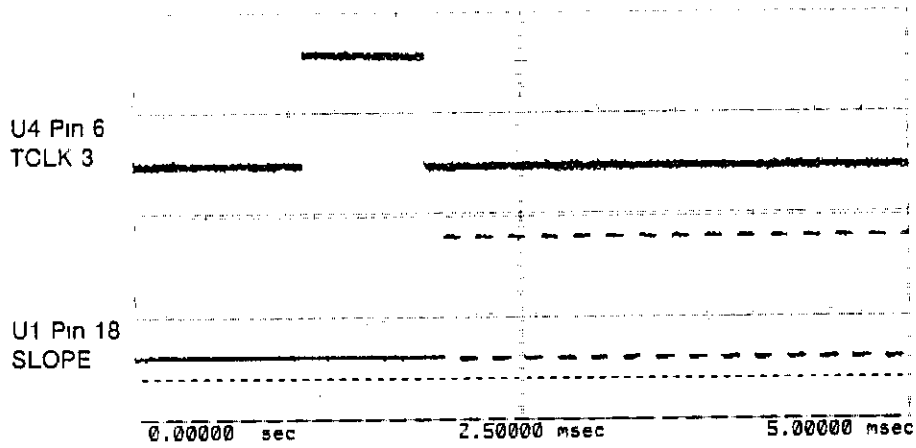
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  2.00 msec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-73. Loop 54 Troubleshooting Waveforms at U3 Pin 3 and TP1.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  2.000  volts/div          Offset     =  1.600  volts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-74. Loop 54 Troubleshooting Waveforms at U4 Pin 6 and U1 Pin 18.

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6E-67. LOOP 55

DELAYED BT TIME = 825 μs

Description:

This test is similar to the delayed-by-event loops. The conditions to start the counter are the same; but instead of counting trigger events, the counter is clocked by the 100 MHz clock. This test is set up so that approximately 825 nsec after QCLK goes true, DOUT will also go true. The DOUT part of the status byte is polled. And a software down counter keeps track of the time between QCLK and DOUT. The valid range gives +-8.5% accuracy on the timing of the 100 MHz clock.

All of the TCLK's are enabled at QCLK but inputs 1, 2, and 3 are programmed low by LE1-LE4. The QCLK edge which starts the timer comes from trigger 4 sync comparator. TCLK out is set to -.8 V and thus the Trigger board will receive no triggers. When TCLK4 creates its trigger event, QCLK's edge is generated. This causes U19 pin 3 to go high and remove the reload signal from the counter. U19 pin 4 goes low, which starts the 100 MHz oscillator. The oscillator clocks the counter which was previously loaded with a value such that it will timeout in 825 μs. DOUT goes high when the counter times out.

Status Register:

Status #1 -1 indicates that holdoff could never be enabled.

Status #2 The downcounter value of the last time loop was executed

Status #3 The downcounter value of the last time loop failed because of being too low.

Status #4 The down counter value of the last time loop failed because of being too high.

Down counter valid range = 212 ±18.

Possible Cause of Failure:

1. Adjustments indicated - Sampler 1 and 2, main, and qualified trigger hysteresis
2. Boards indicated - Sampler 1 and 2, trigger, qualifier
3. Functional boards indicated - QCLK, All TCLK's, 100 MHz clock, DOUT, 29-bit counter, TCLK4's trigger comparator, sampler 1 and 2, and the Trigger board's triggers comparator are disabled, trigger mux.

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Fault Diagnosis:

Check U4 pin 17, 1, 6 are = -.8 V. If pin 17 is bad replace Sampler 1. If pin 1 is bad replace Sampler 2. If pin 6 is bad replace Trigger board. Suspect INB7-8008 on replaced board. If those are good, then check that TCLKOUT is -.8 V. If not, the INB7-8030 is most likely faulty.

Check the following points:

```
U6 Pin 2      (QCLK)
TP15          (DOUT)

U19 pin 14    (counter clock: do this twice, the second
TP1            more magnified in the timebase)

U19 pin 4
TP1           (counter clock)

U1 pin 14     (TCLK4)
TP15          (DOUT)

U1 pin 14     (QCLK4)
U4 pin 10     (TCLKOUT4)

U19 pin 4
TP1           (counter clock)
```

If DOUT is bad and QCLK is good, replace Qualifier.

If QCLK is bad but U4 pin 10 is good, replace Qualifier (suspect U17).

If U4 pin 10 is bad and TCLK4 is good, replace Qualifier.

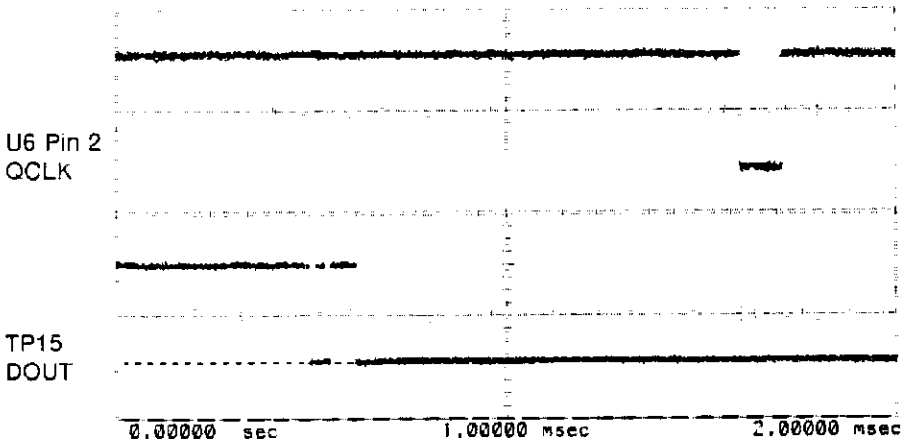
If TCLK 4 is bad and SLOPE is good (should look just like TCLK4 except it is inverted), replace Qualifier. (Suspect U1).

Check to make sure that when probing TP1 that the fast oscillation is about 100 MHZ. If not, perform adjustments, and try test again. If this cannot be made 100 MHz then replace the qualifier.

Check the following qualifier status register points.

```
INTPD=1       LE1-LE4=1         SUBMODE=1
STPD=0        LSTATE=1          LCO=1
LS1-LS4=0     DYLD=1
```

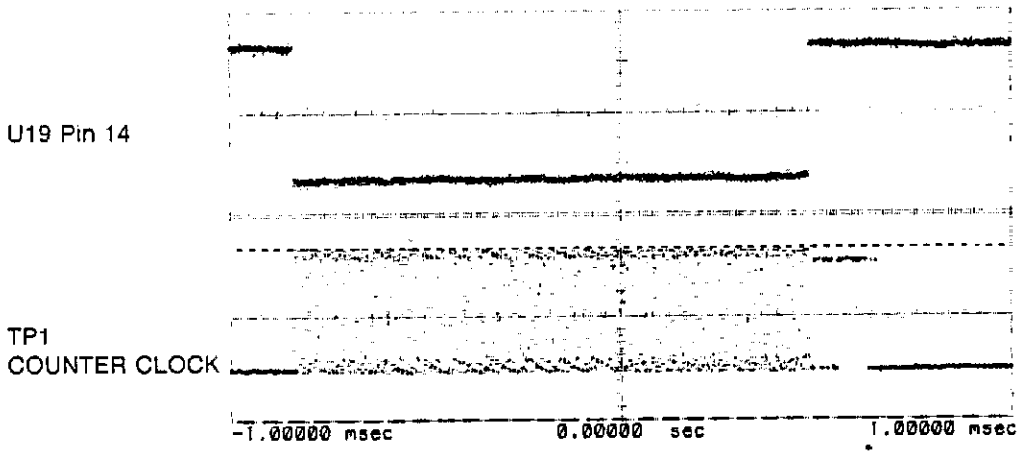

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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-75. Loop 55 Troubleshooting Waveforms at TP15 and U6 Pin 2.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-76. Loop 55 Troubleshooting Waveforms at U19 Pin 14 and TP1.

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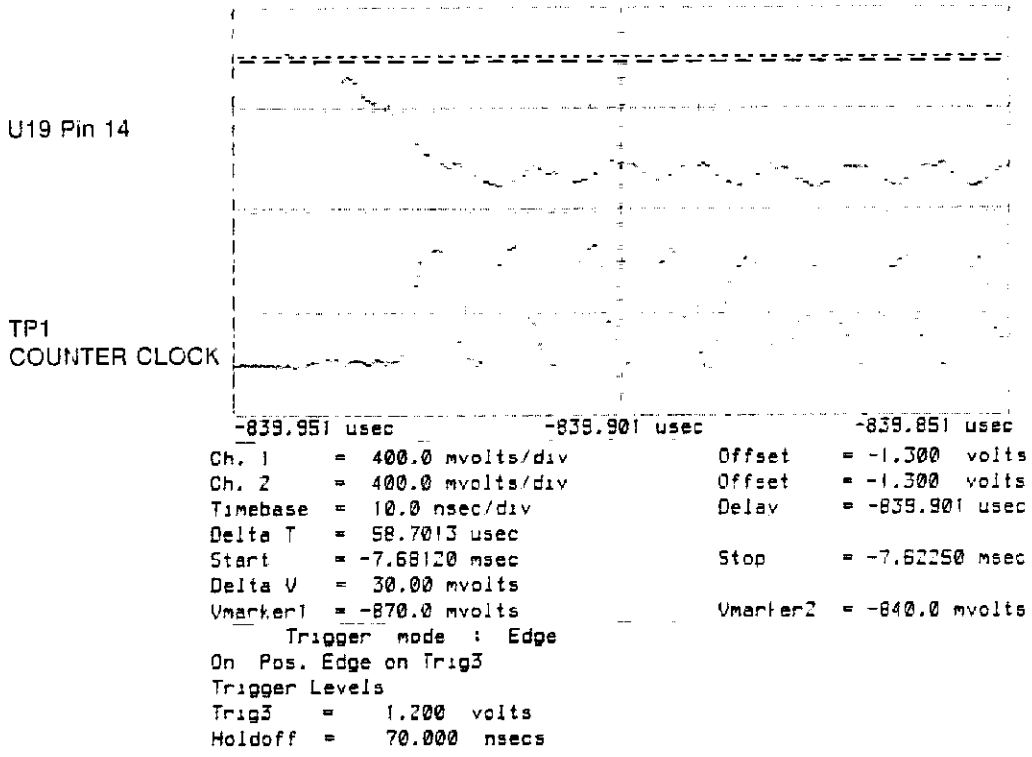


Figure 6E-77. Loop 55 Troubleshooting Waveforms at U19 Pin 14 and TP1.

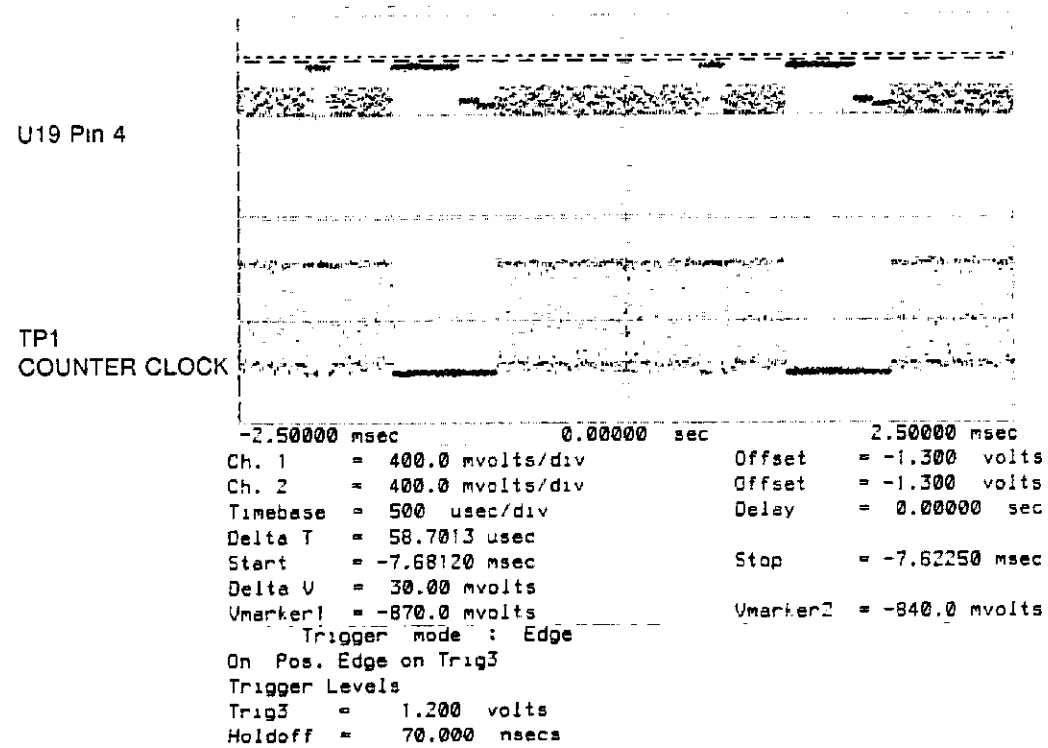
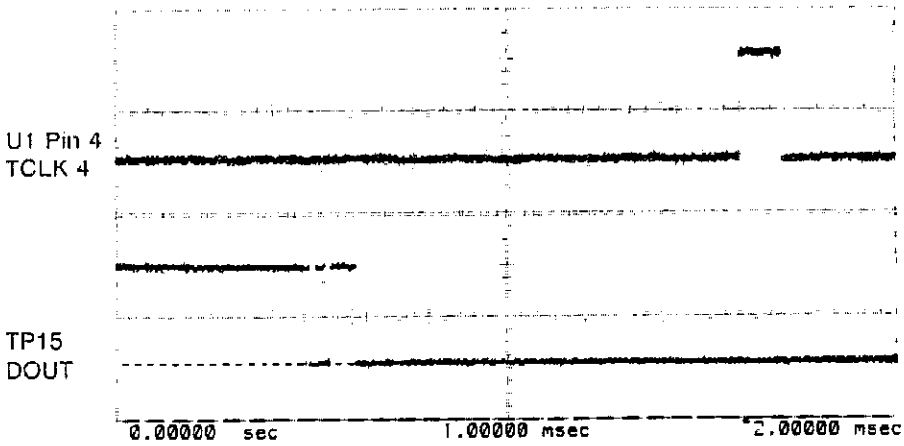


Figure 6E-78. Loop 55 Troubleshooting Waveforms at U19 Pin 4 and TP1.

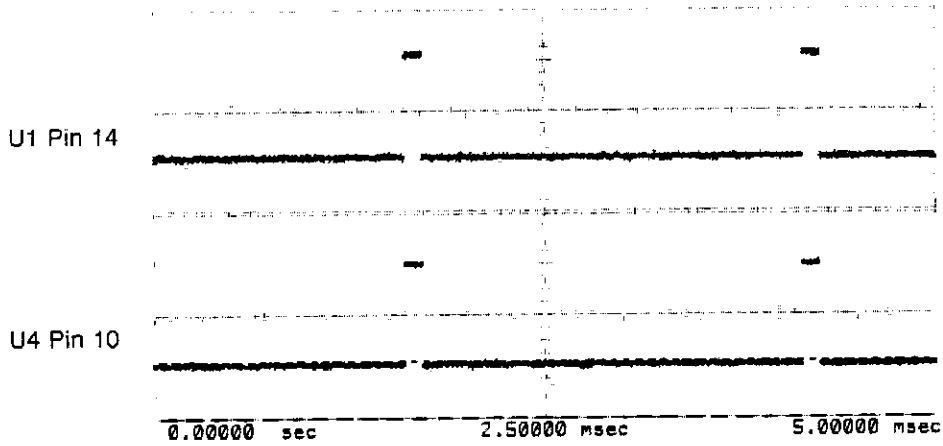
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```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-79 Loop 55 Troubleshooting Waveforms at U1 Pin 4 and TP15.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -432.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta V    =  4.200  volts
Vmarker1   = -4.960  volts              Vmarker2   = -760.0 mvolts

      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =     1.200  volts
Holdoff    =     70.000  nsecs
```

Figure 6E-80. Loop 55 Troubleshooting Waveforms at U1 Pin 14 and U4 Pin 10.

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6E-68. LOOP 56

PATTERN PRESENT > 825 μs :

Description:

This loop tests the pattern present > 825 μs mode of operation on the Qualifier board. It measures the time it takes DOUT to go high after TCLK' (U17 pin 2) goes true. After DOUT goes low the loop takes TCLKOUT low and verifies that a trigger does occur. (TCLK'=TCLK1 & TCLK2 & TCLK3 & TCLK4). A software counter measures this time by polling DOUT and the test passes if it sees 825 μs ±8.5% between these events.

QCLK is completely disabled and all TCLKS are enabled through the 1NB7-8030 hybrid, but 1-3 are programmed low. TCLKOUT transitions are generated from the trigger comparator on the qualifier board. The low to high transition at TCLKOUT starts the 100 MHz oscillator and removes the reload signal from the counter. 825 μs later, DOUT goes high as the counter clocks out. TCLKOUT then goes low (in effect an >825 μs wide TCLKOUT pulse has been generated).

Status Register:

No indication.

Possible Cause of Failure:

1. Adjustments indicated - if TCLKOUT and DOUT appear correct but no trigger occurs at U3 pin 3 at rising transitions then check operation and calibration of filter offset adjustment, sampler 1 and 2, trig, qualifier trigger hysteresis. Then check the RC network at U32 pin 4.

2. Boards indicated - Sampler 1 and 2, Trigger, Qualifier

3. Functional blocks indicated - Same as Loop 55.

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Fault Diagnosis:

Check that the following points are at -.8 V: U4 pin 4, 15, 19, 17, 1, 6 and U17 pin 13, 11, 4.

Check the following points:

```
U4 pin 8      (TCLKOUT)
TP1           (counter clock)

TP15          (DOUT)
U3 pin 3      (OPTHLDF)

TP15          (DOUT)
U4 pin 8      (TCLKOUT)

U33 pin 7
TP1           (counter clock)

U17 pin 7     (LQ4 a derivative of U4 pin 10)
U4 pin 12     (TCLK4)

U33 pin 7
TP1           (counter clock)
```

If U4 pin 17 is bad, replace Sampler 1 board.

If U4 pin 1 is bad, replace Sampler 2 board.

If U4 pin 6 is bad, replace the Trigger board.

If U4 pin 17, 1, and 6 are good but U4 pin 4,15, or 19 is bad, replace Qualifier board (suspect 1NB7-8030).

If DOUT is bad and OPTHLDF is good, replace the Qualifier board.

If OPTHLDF is bad and DOUT is good, replace the Trigger board.

If OPTHLDF is bad and DOUT is bad and TCLKOUT is good, then replace the Qualifier board if TP1, U33 pin 7, U17 pin 7, and U4 pin 12 are good; otherwise, replace the Trigger board.

In addition, if DOUT and OPTHLDF are bad, then configure the unit as an "A" model and run the self tests. If they pass, then replace the Qualifier board, otherwise replace the Trigger board.

If TCLK4 is bad replace Qualifier board (suspect INB7-8008).

Check for the following qualifier status register levels:

```
LS1-LS4=1     DLYD=0          LC0=1
LE1-LE4=0     INTPD=0
LSTATE=1      STPD=1          Counter bits are programmed for
              SUBMODE=1       825 µs at 100 MHz.
```


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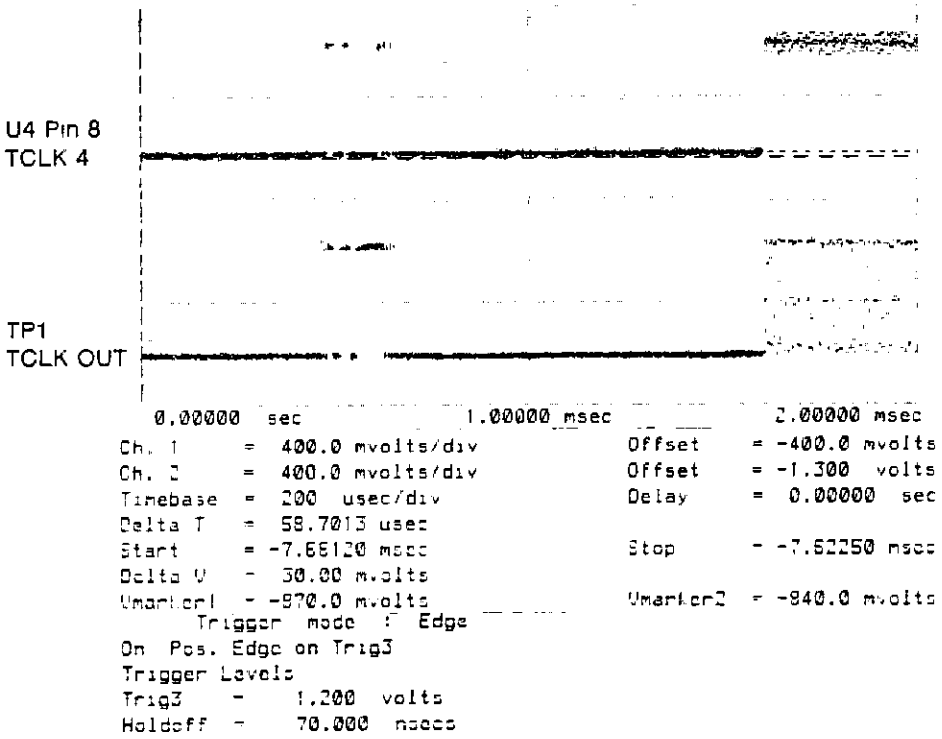


Figure 6E-81. Loop 56 Troubleshooting Waveforms at TP1 and U4 Pin 8.

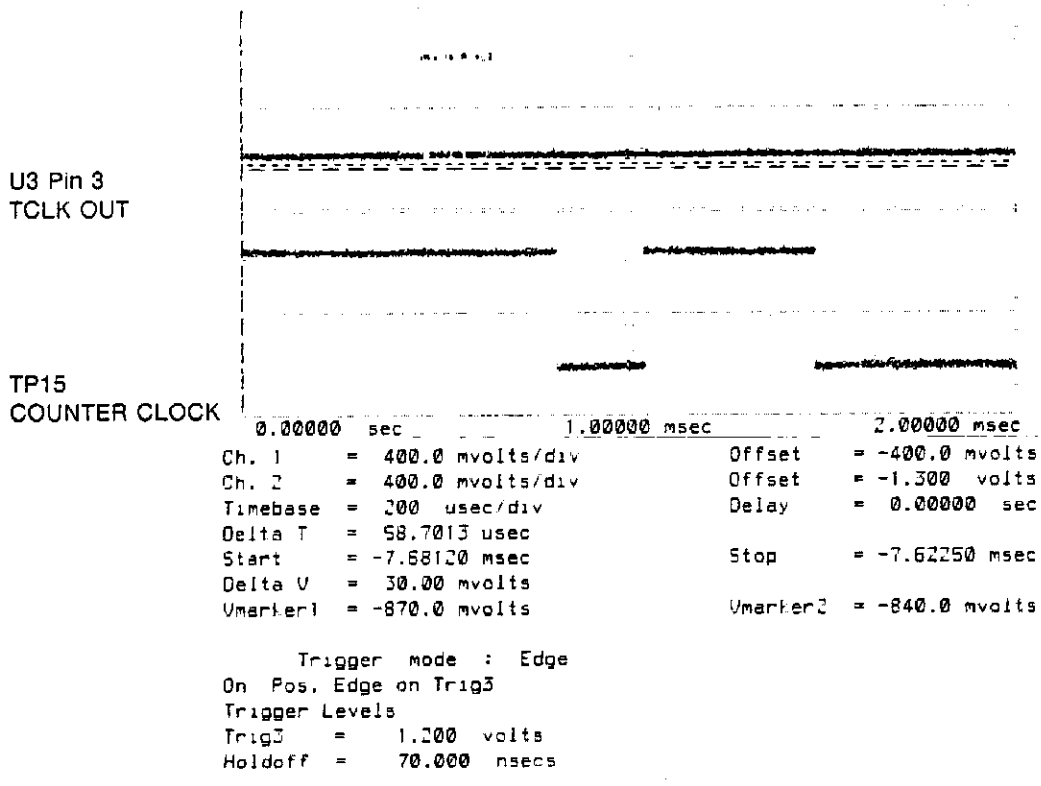
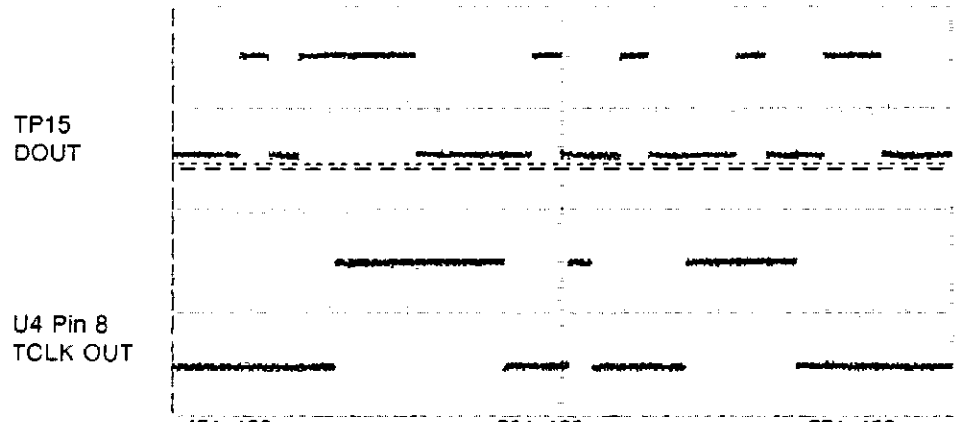


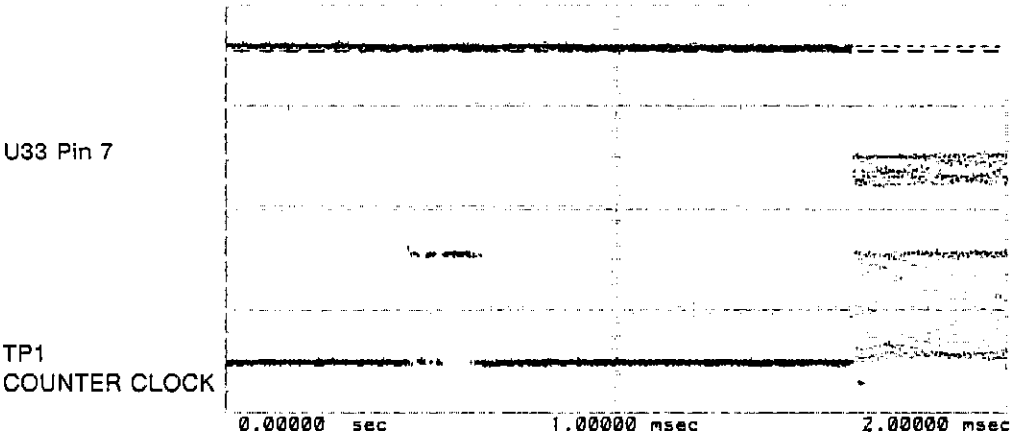
Figure 6E-82. Loop 56 Troubleshooting Waveforms at U3 Pin 3 and TP15.

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```
 454.400 usec              504.400 usec              554.400 usec
Ch. 1     =  400.0 mvolts/div          Offset    = -400.0 mvolts
Ch. 2     =  400.0 mvolts/div          Offset    = -400.0 mvolts
Timebase  =  10.0 usec/div             Delay     =  454.400 usec
Delta T   =  58.7013 usec
Start     = -7.68120 msec              Stop      = -7.62250 msec
Delta V   =  30.00 mvolts
Vmarker1  = -870.0 mvolts              Vmarker2  = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =    1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-83 Loop 56 Troubleshooting Waveforms at U4 Pin 8 and TP15.




```
 0.00000  sec            1.00000 msec            2.00000 msec
Ch. 1     =  400.0 mvolts/div          Offset    = -1.300  volts
Ch. 2     =  400.0 mvolts/div          Offset    = -1.300  volts
Timebase  =  200  usec/div             Delay     =  0.00000  sec
Delta T   =  58.7013 usec
Start     = -7.68120 msec              Stop      = -7.62250 msec
Delta V   =  30.00 mvolts
Vmarker1  = -870.0 mvolts              Vmarker2  = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =    1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-84. Loop 56 Troubleshooting Waveforms at U33 Pin 7 and TP1.

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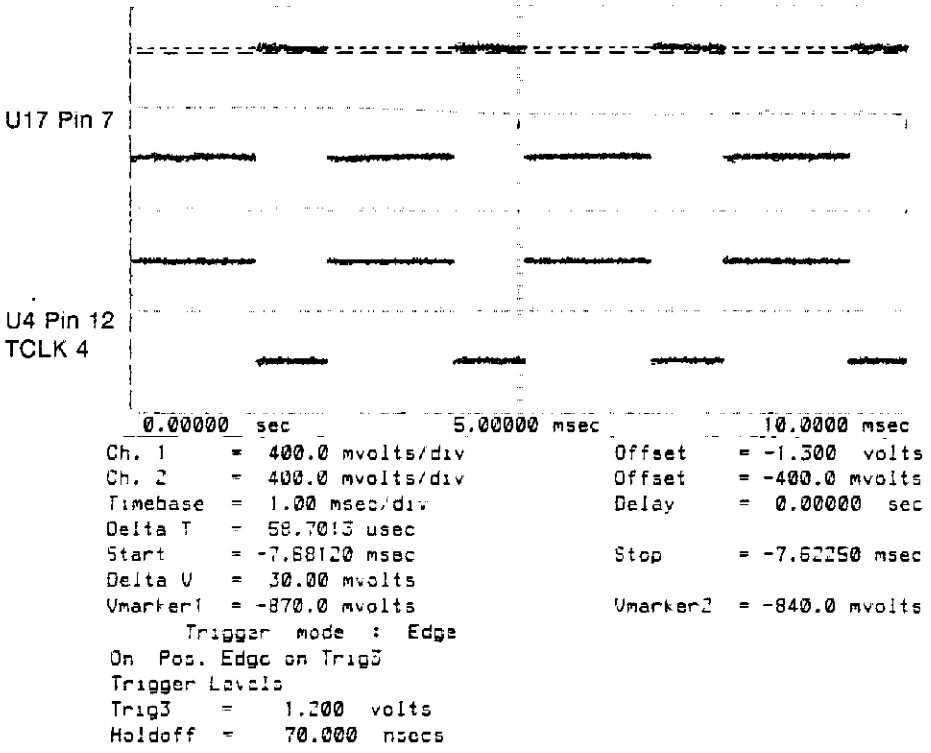


Figure 6E-85. Loop 56 Troubleshooting Waveforms at U17 Pin 7 and U4 Pin 12.

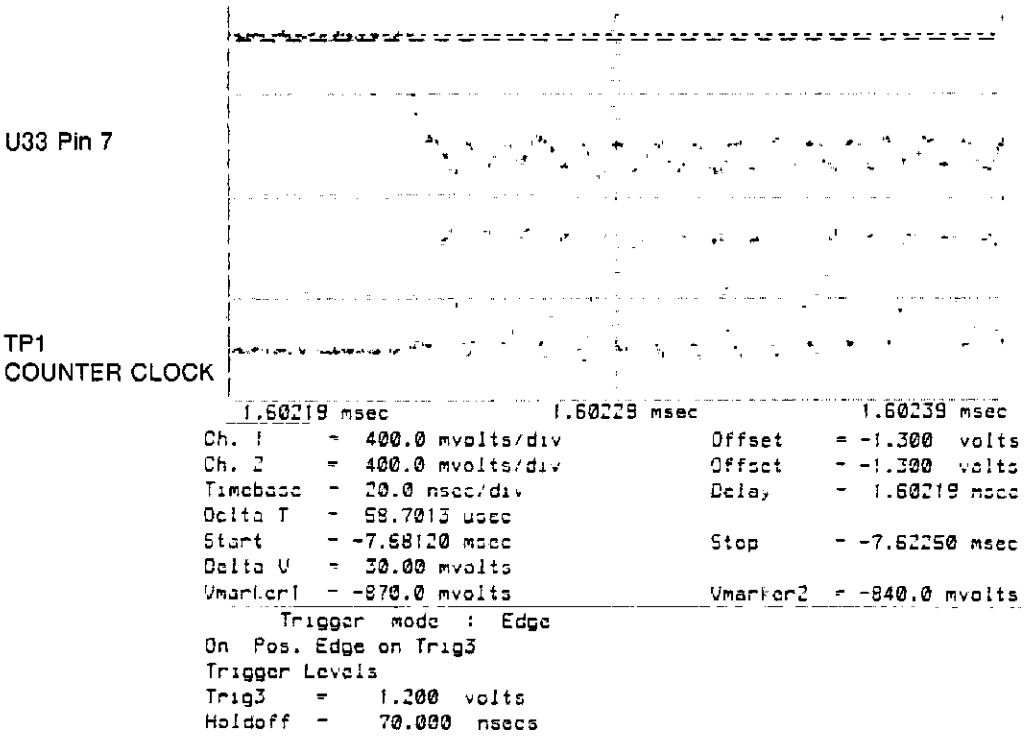


Figure 6E-86. Loop 56 Troubleshooting Waveforms at U33 Pin 7 and TP1.

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6E-69. LOOP 57

PATTERN PRESENT < 825 μs

Description:

This loop is similar to 56 except that it tests <825 μs pattern present trigger mode. TCLK' is forced true and the time required for DOUT to go low is measured. This loop will pass only if the software counter sees the pattern present as < 825 μs ±8.5%.

QCLK is completely disabled and all TCLK's are enabled through the 1NB7-8030 hybrid, but 1-3 are programmed low. TCLKOUT transitions are generated from the qualifiers trigger sync comparator. TCLKOUT is set high via TCLK4. This starts the 100 MHz oscillator and releases the counter. DOUT was initially high and goes low when the timer clocks out (825 μs after TCLKOUT going high). When DOUT goes low TCLKOUT is taken low which sends DOUT back high but no trigger will occur because TCLKOUT goes low before DOUT goes high.

Status Register:

No indications.

Possible Cause of Failure:

1. Adjustments indicated - If TCLKOUT and DOUT are correct (see below) but a trigger does occur at U3 pin 3, check the RC network at U32 pin 4. Then check the operation and calibration of filter offset adjustment. Otherwise same as Loop 56.

2. Boards indicated - Same as Loop 56

3. Functional blocks indicated - Same as Loop 56

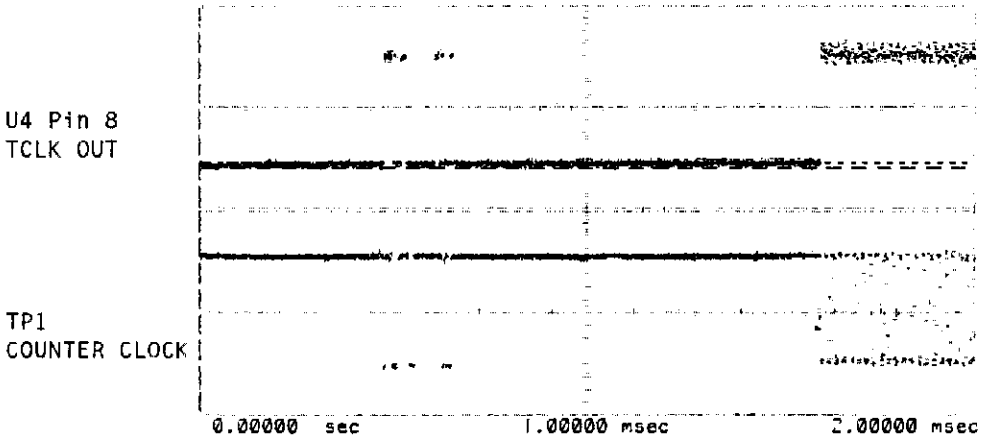
Fault Diagnosis:

Same as Loop 56.

Check the following qualifier status register levels:

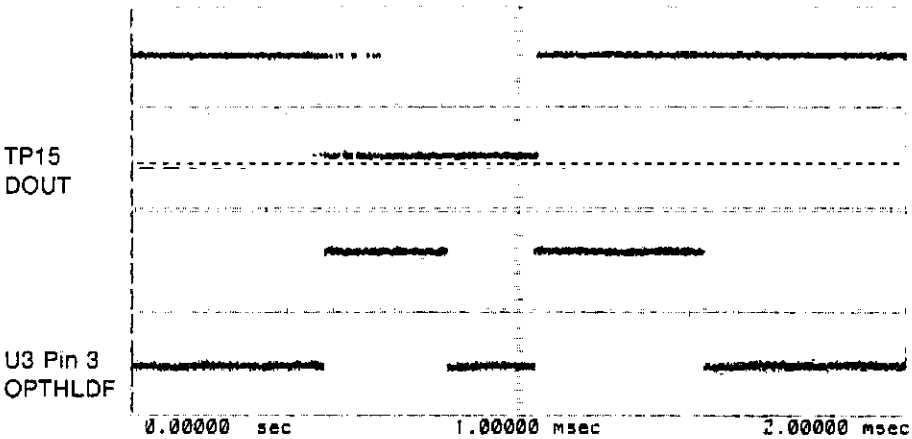
```
LS1-LS4=1     DLYD=0          INTPD=0
LE1-LE4=0     SUBMODE=0       STPD=1
LSTATE=1      I.C=1           Counter bits are programmed
                              the same as Loop 56
```


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```
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =    70.000  nsecs
```

Figure 6E-87 Loop 57 Troubleshooting Waveforms at TP1 and U4 Pin 8.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =    70.000  nsecs
```

Figure 6E-88. Loop 57 Troubleshooting Waveforms at U3 Pin 3 and TP15.

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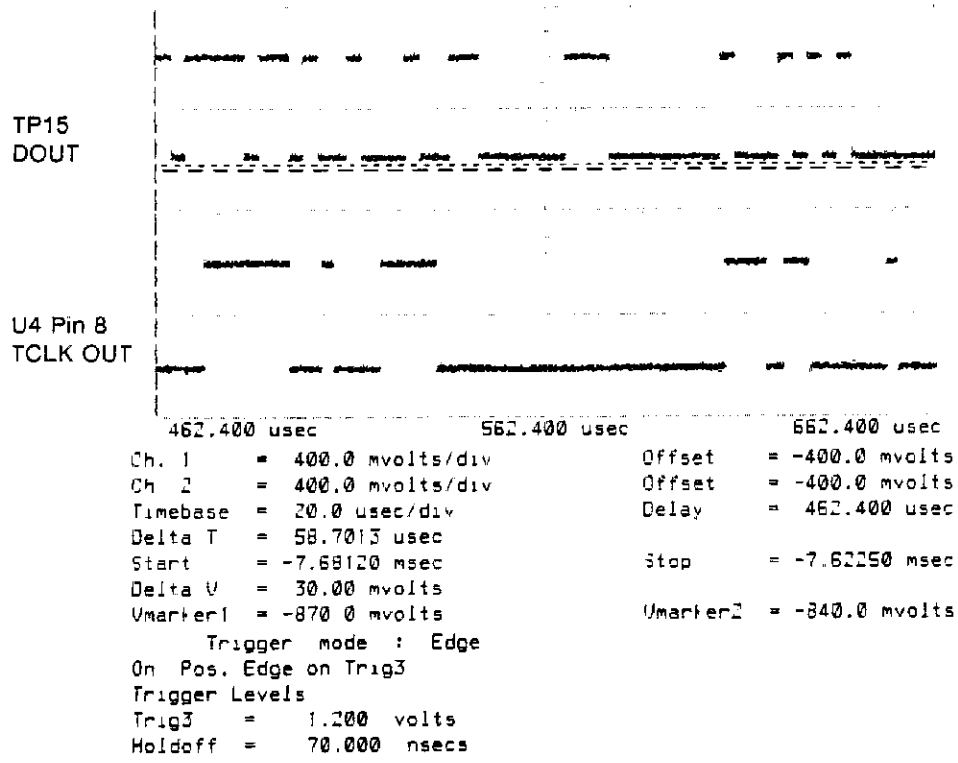


Figure 6E-89. Loop 57 Troubleshooting Waveforms at U4 Pin 8 and TP15.

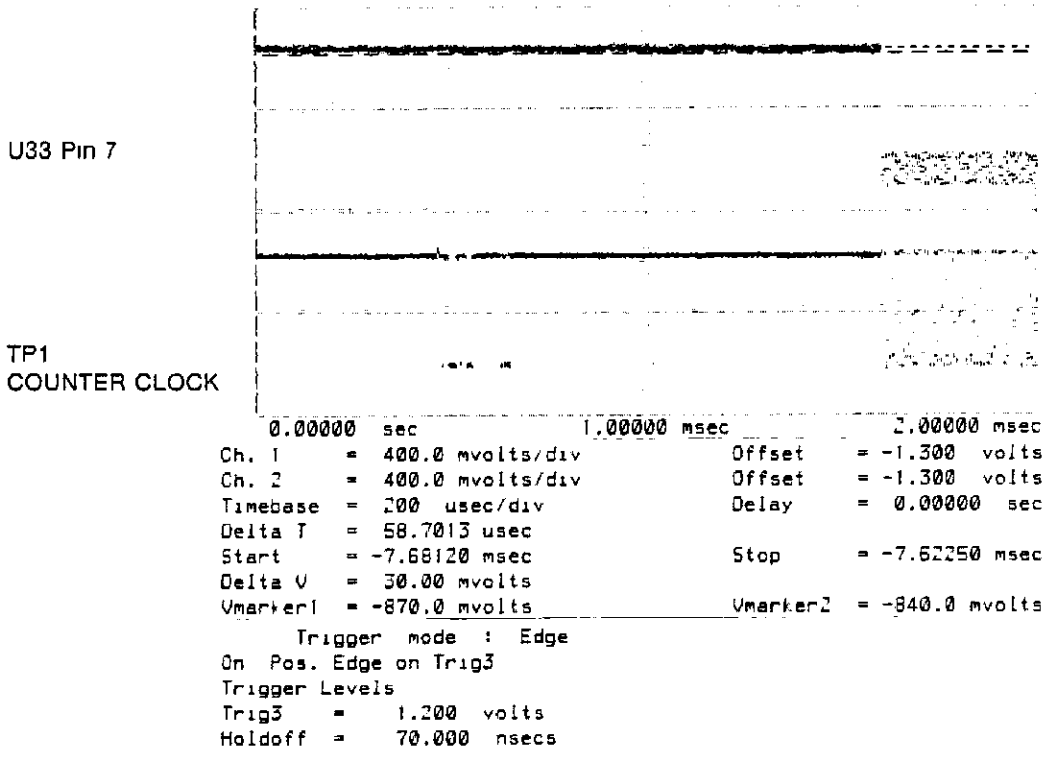
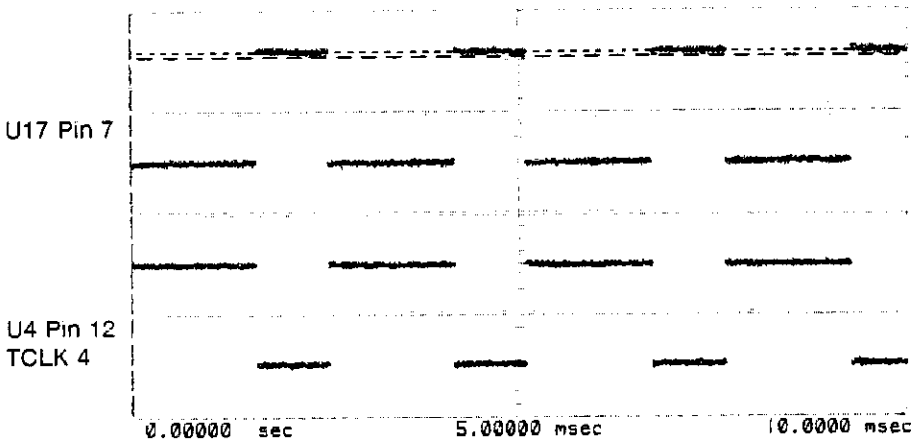


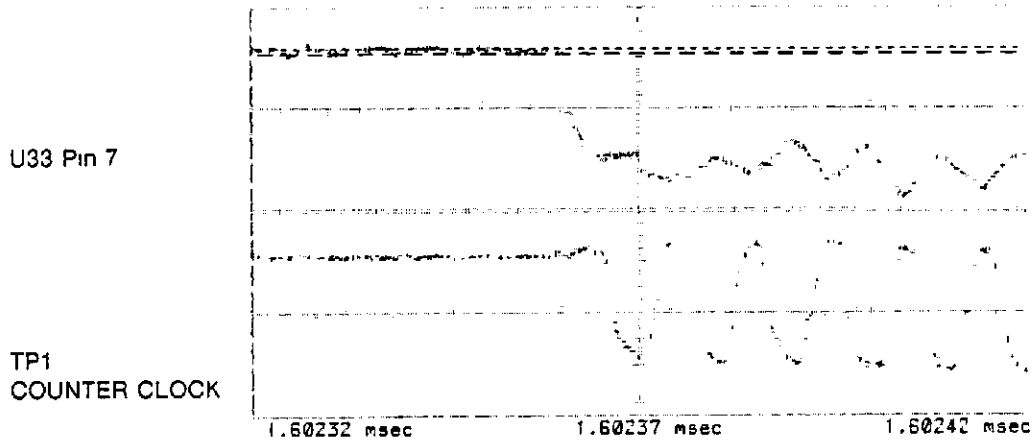
Figure 6E-90. Loop 57 Troubleshooting Waveforms at U33 Pin 7 and TP1.

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```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  1.00 msec/div             Delay      =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =   70.000  nsecs
```

Figure 6E-91. Loop 57 Troubleshooting Waveforms at U17 Pin 7 and U4 Pin 12.




```
Ch. 1      =  400.0 mvolts/div          Offset     = -1.300  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  10.0 nsec/div             Delay      =  1.60232 msec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =   70.000  nsecs
```

Figure 6E-92. Loop 57 Troubleshooting Waveforms at U33 Pin 7 and TP1.

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6E-70. LOOP 58

TCLK DISABLE @ EDGE MODE

Description:

This loop verifies that the enable control lines on the INB7-8030 hybrid (LE1-LE4) will indeed block trigger signals.

The triggering system is programmed in the edge mode (ie. DOUT always high). All TCLK's are disabled (LE1-LE4) so nothing should get through to TCLKOUT to cause a trigger. In turn TCLK 1 and TCLK 2 are taken high then TCLK3 and TCLK4 are pulsed high. DOUT should remain high and OPTHLDF should remain low which indicates that no triggers were received.

Status Register:

No indications.

Possible Cause of Failure:

1. Adjustments indicated - none indicated
2. Boards indicated - Sampler 1/2, trigger, qualifier
3. Functional blocks indicated - LE1-4, TCLK's toggling, DOUT, OPTHLDF qualifier status register, qualifier string loading, trigger comparator string loading on all trigger comparator boards, U4 on qualifier, trigger holdoff status.

Fault Diagnosis:

Probe the following points.

```
U4 pin 17     (TCLK1)
U4 pin 1      (TCLK2)

U4 pin 6      (TCLK3)
U4 pin 12     (TCLK4)

TP15          (DOUT)
U3 pin 3      (OPTHLDF)
```

Check that the following signal:
U4 pin 8 = 0 V

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If TCLK1 is bad, replace Sampler1.

If TCLK2 is bad, replace Sampler2.

If TCLK3 is bad, replace Trigger.

If TCLK4 is bad, replace Qualifier

If all TCLK's are good and TCLKOUT is bad, replace Qualifier (suspect 1NB7-8030).

If DOUT is bad and OPTHLDF is good, replace the Qualifier.

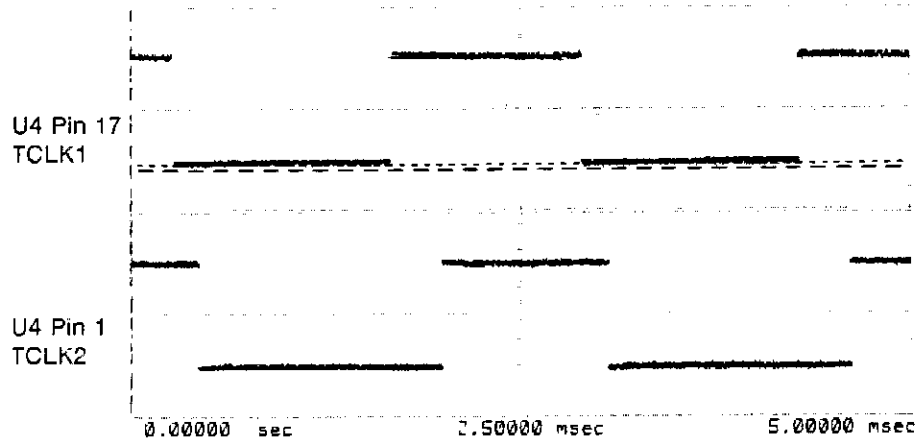
If OPTHLDF is bad and DOUT is good, replace the Trigger board.

If DOUT and OPTHLDF are bad, then configure the unit as an "A" model and run the self tests. If they pass, then replace the Qualifier; otherwise replace the Trigger board.

Check the following qualifier status register levels:

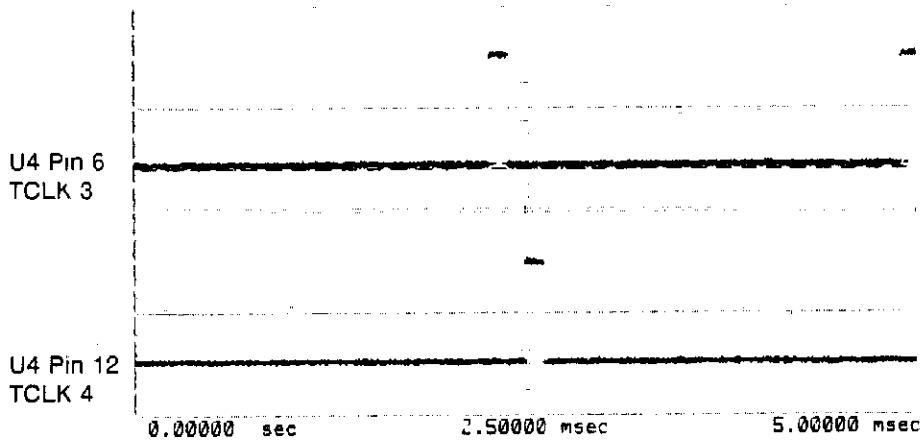
LS1-LS4=0	LSTATE=0	COUNTER BITS=0
LE1-LE4=0	DYLD=0	INTPD=1
	SUBMODE=0	STPD=0

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```
 0.00000  sec              2.50000 msec              5.00000 msec
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =    70.000  nsecs
```

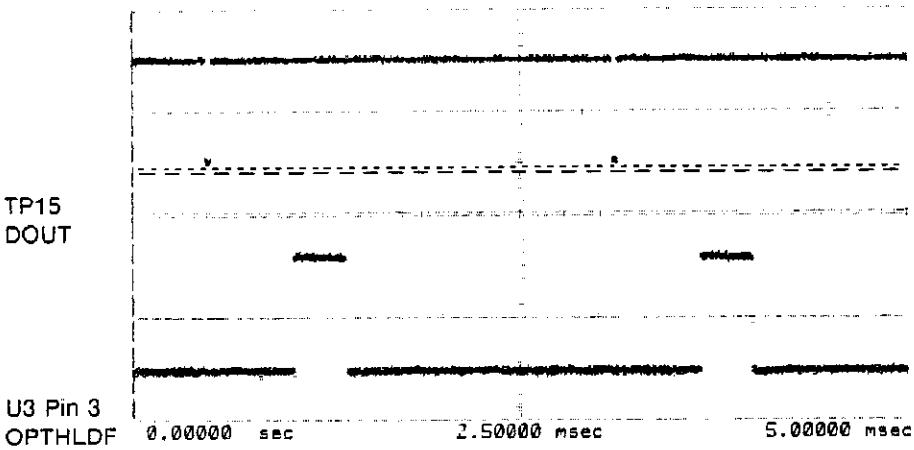
Figure 6E-93. Loop 58 Troubleshooting Waveforms at U4 Pins 1 and 17.




```
 0.00000  sec              2.50000 msec              5.00000 msec
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger  mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3    =    1.200  volts
Holdoff  =    70.000  nsecs
```

Figure 6E-94. Loop 58 Troubleshooting Waveforms at U4 Pins 6 and 12.

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```
Ch. 1      =  400.0 mvolts/div          Offset    = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset    = -1.300  volts
Timebase   =  500  usec/div             Delay     =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop      = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2  = -840.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =    1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-95. Loop 58 Troubleshooting Waveforms at U3 Pin 3 and TP15.

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6E-71. LOOP 59

QCLK DISABLE

Description:

This loop verifies that LS1-LS4 control signals actually do block the trigger outputs of the INB7-8030 at QCLK (U6).

The triggering system is programmed in edge mode with all TCLK's disabled at QCLK. TCLK1-4 are initially high, then are taken low one at a time. DOUT should remain high throughout and OPTHLDF should also remain high (In this test the trigger board is not initialized to be out of holdoff).

Status Register:

No indications.

Possible Cause of Failure:

1. Adjustments indicated - none indicated.
2. Boards indicated - Sampler 1/2, trigger, qualifier
3. Functional blocks indicated - LS1-4, TCLK's toggling, DOUT, OPTHLDF, qualifier status register, qualifier string loading, trigger comparator string loading on all trigger comparator boards, U4 on qualifier, trigger holdoff status.

Fault Diagnosis:

Probe the following points.

```
U4 pin 17     (TCLK1)
U4 PIN 1      (TCLK2)

U4 PIN 6      (TCLK3)
U4 PIN 12     (TCLK4)

TP15          (DOUT)
U3 pin 3      (OPTHLDF)
```


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If TCLK1 is bad, replace Sampler 1 board.

If TCLK2 is bad, replace Sampler 2 board.

If TCLK3 is bad, replace Trigger board

If TCLK4 is bad, replace Qualifier board

If DOUT is bad and if OPTHLDF is good, replace Qualifier board.

If OPTHLDF is bad and DOUT is good, replace the Trigger board.

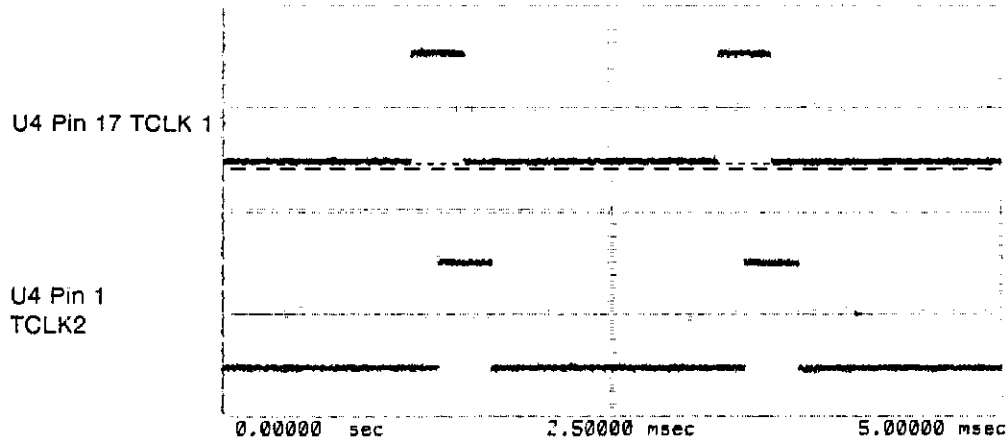
If DOUT and OPTHLDF are bad, then configure the unit as an "A" model and run the self tests. If they pass, then replace the Qualifier board; otherwise replace the Trigger board.

If TCLKOUT is bad and all the TCLK's are good, replace the Qualifier board (suspect the 1NB7-8030).

Check the following trigger qualifier status register levels.

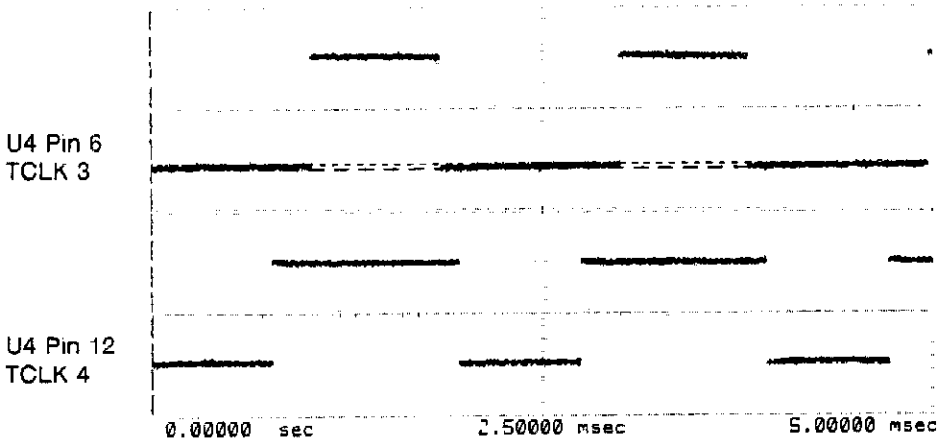
```
LS1-LS4=1     DYLD=0            COUNTER BITS =0
LE1-LE4=1     SUBMODE=0
LSTATE=0      INTPD=1
              STPD=0
```


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```
0.00000  sec              2.50000 msec              5.00000 msec
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =    1.200  volts
Holdoff   =    70.000  nsecs
```

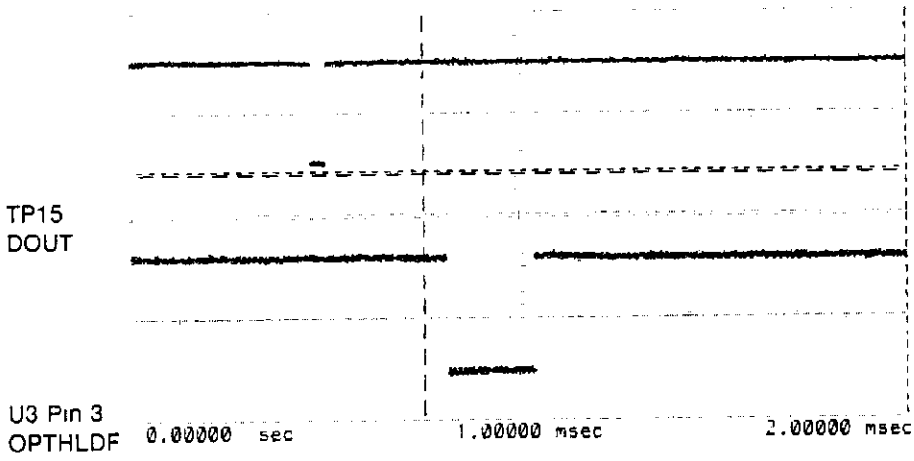
Figure 6E-96 Loop 59 Troubleshooting Waveforms at U4 Pins 1 and 17.




```
0.00000  sec              2.50000 msec              5.00000 msec
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  500  usec/div             Delay      =  0.00000  sec
Delta T    =  58.7013 usec
Start      = -7.68120 msec              Stop       = -7.62250 msec
Delta V    =  30.00 mvolts
Vmarker1   = -870.0 mvolts              Vmarker2   = -840.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =    1.200  volts
Holdoff   =    70.000  nsecs
```

Figure 6E-97. Loop 59 Troubleshooting Waveforms at U4 Pins 6 and 12.

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```
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -1.300  volts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta T    =  3.50000 msec
Start      =  750.000 usec              Stop       =  4.25000 msec
Delta V    =  28.00 mvolts
Vmarker1   = -876.0 mvolts              Vmarker2   = -848.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3     =     1.200  volts
Holdoff   =     70.000  nsecs
```

Figure 6E-98. Loop 59 Troubleshooting Waveforms at U3 Pin 3 and TP15.

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6E-72. LOOP 60

TCLK DISABLE @ PATTERN PRESENT >= 10 nS

Description:

This loop verifies that LE1-LE4 will block signals at TCLK (U17 pin 2) and checks that INTPD, and STPD operate correctly to initialize pattern present mode.

The triggering system is programmed for pattern present > 10 nsec. This means that DOUT should instantaneously follow TCLK: First TCLK 1, 2, 4 are exercised (as shown in pictures below) and DOUT should not change. Then INTPD and STPD are taken from 10 to 00 to 01. This will start the timer and send DOUT high when STPD goes from 0 to 1. The STPD and DOUT pulses appear very short in the pictures because the loop is very fast at this point.

Status Register:

No indication.

Possible Cause of Failure:

1. Adjustments indicated - none indicated.
2. Boards indicated - Sampler 1 and 2, Trigger, and Qualifier
3. Functional blocks indicated - INTPD, STPD, TCLK's toggling, DOUT, OPTHLDF, qualifier status register, qualifier string loading, trigger comparator string loading on all trigger comparator boards, U4 on qualifier.

Fault Diagnosis:

Probe the following points.

TP17	(STPD)	U4 PIN 17	(TCLK1)	U4 PIN 12	(TCLK4)
TP15	(DOUT)	U17 PIN 2	(TCLK┼)	U4 PIN 8	(TCLKOUT)
TP16	(INTPD)	U4 PIN 1	(TCLK2)		
TP15	(DOUT)	U4 PIN 6	(TCLK3)		

If DOUT is bad and the TCLK's and STPD and INTPD are good, replace the Qualifier board.

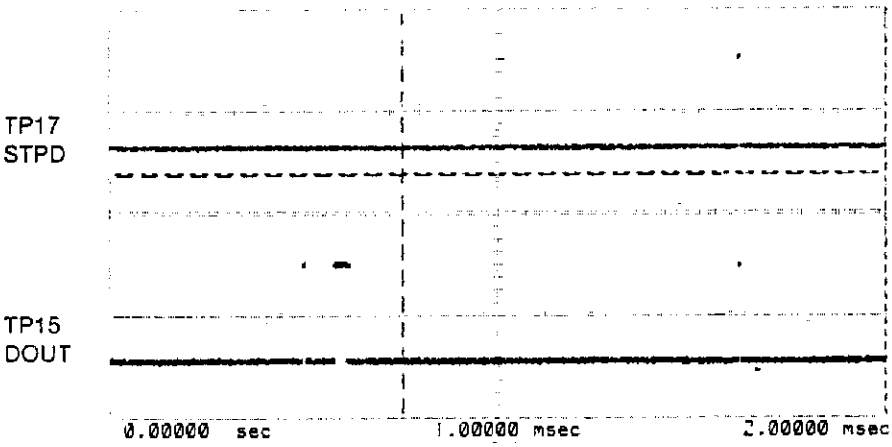
If TCLKOUT is bad and the TCLK's are good replace the Qualifier board (suspect INB7-8008).

If TCLK1 is bad, replace Sampler 1; If TCLK2 is bad, replace Sampler 2; If TCLK3 is bad, replace Trigger board; If TCLK4 is bad, replace Qualifier board.

Check the following qualifier status register levels:

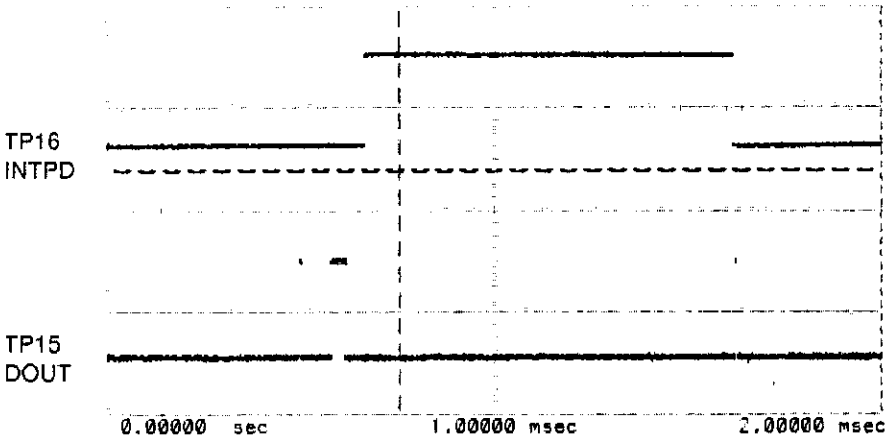
LS1-LS4=1	DYLD=0	CL3=1	CL37=1
SE1-SE4=1	SUBMODE=1	LC2-LC5=1	LCL37=0
LSTATE=1	C1=1	LCL5=0	C6-C29=0
	LC3=1		

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```
Ch. 1      =  2.000  volts/div          Offset     =  1.600  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta T    =  3.50000 msec
Start      =  750.000 usec              Stop       =  4.25000 msec
Delta V    =  28.00 mvolts
Vmarker1   = -876.0 mvolts              Vmarker2   = -848.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-99 Loop 60 Troubleshooting Waveforms at TP15 and TP17.




```
Ch. 1      =  2.000  volts/div          Offset     =  1.600  volts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta T    =  3.50000 msec
Start      =  750.000 usec              Stop       =  4.25000 msec
Delta V    =  28.00 mvolts
Vmarker1   = -876.0 mvolts              Vmarker2   = -848.0 mvolts
      Trigger mode : Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-100. Loop 60 Troubleshooting Waveforms at TP16 and TP15.

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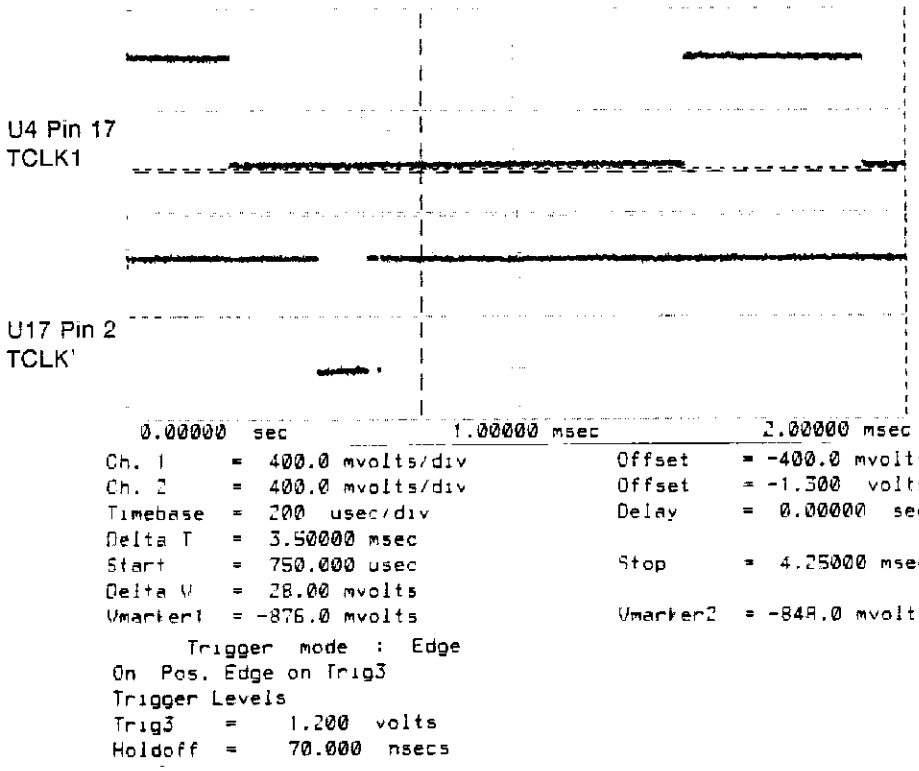


Figure 6E-101. Loop 60 Troubleshooting Waveforms at U4 Pin 17 and U17 Pin 2.

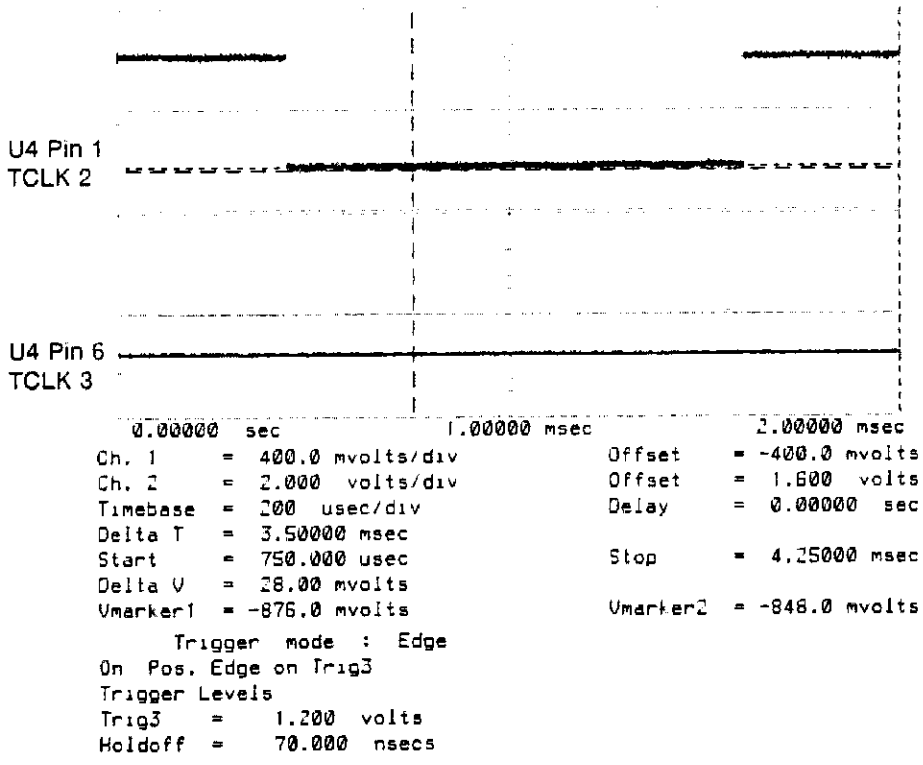
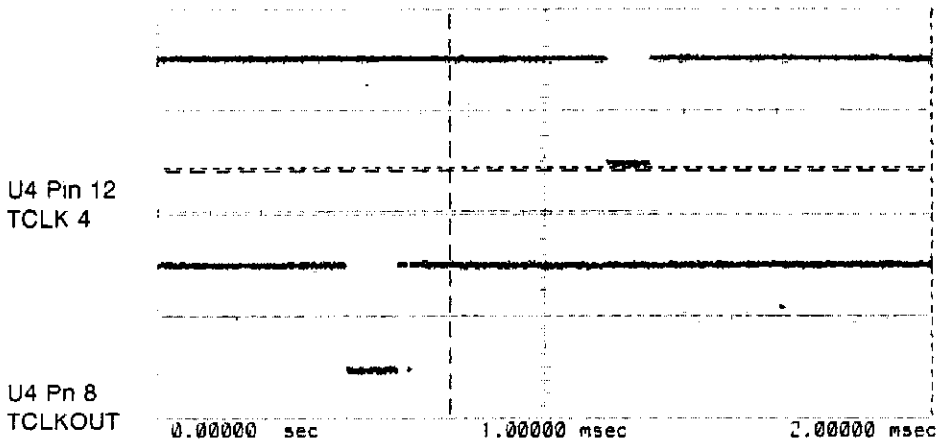


Figure 6E-102 Loop 60 Troubleshooting Waveforms at U4 Pins 1 and 6

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```
Ch. 1      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Ch. 2      =  400.0 mvolts/div          Offset     = -400.0 mvolts
Timebase   =  200  usec/div             Delay      =  0.00000  sec
Delta T    =  3.50000 msec
Start      =  750.000 usec              Stop       =  4.25000 msec

Delta V    =  28.00 mvolts
Vmarker1   = -876.0 mvolts              Vmarker2   = -848.0 mvolts

      Trigger mode  :  Edge
On  Pos. Edge on Trig3
Trigger Levels
Trig3      =    1.200  volts
Holdoff    =    70.000  nsecs
```

Figure 6E-103. Loop 60 Troubleshooting Waveforms at U4 Pins 8 and 12.

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SECTION 7

ACCESSORY SERVICE

7-1. INTRODUCTION

This section contains specifications, replaceable parts lists, schematics, adjustment and calibration information for the HP 54100A/D Accessories. This information and information pertaining to operation and applications of each of the accessories can be found in the Operating Note for that product The Operating Note for each accessory is shipped with the accessory. Each accessory is covered by a different section as described below.

HP 54001A	Section 7A
HP 54002A	Section 7B
HP 54003A	Section 7C

The Probe Support Kit listed in figure 7-1 can be used for the performance verification and the adjustment procedures of all three probes.

7-2. TEST RECORD

Results of performance tests may be tabulated on the Performance Test Record (table 7A-9 and table 7C-9) The test record lists all of the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance, troubleshooting, and after repairs or adjustments.

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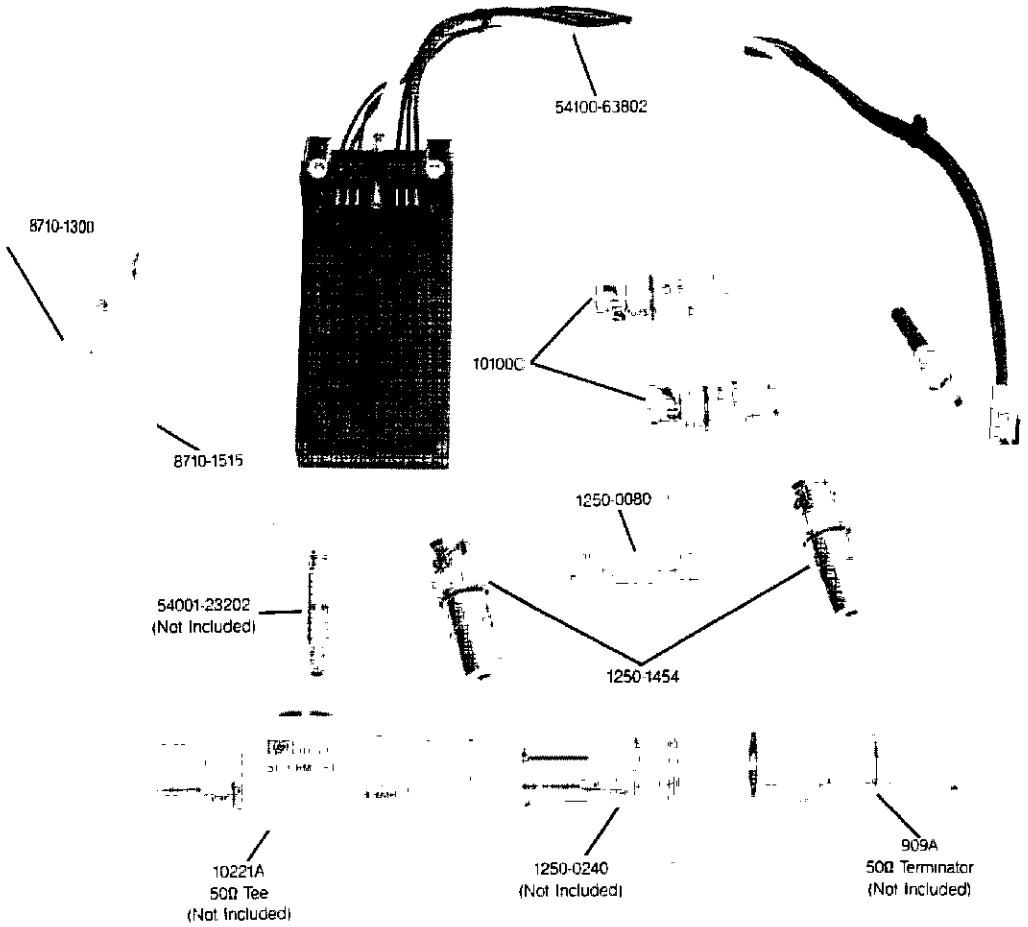


Figure 7-1. Probe Support Kit, HP Part Number 54100-69004.

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SECTION 7A

7A-1. INTRODUCTION

The HP 54001A can be used in any of the three pod receptacles in the HP 54100A, or any of the four pod receptacles in the HP 54100D Digitizing Oscilloscopes. A knurled knob is provided to secure the pod in the receptacle.

WARNING

The HP 54001A and HP 54100A/D have a common terminal at GROUND POTENTIAL (in accordance with OSHA requirements and the National Electrical Code). Exposed metallic surfaces of the HP 54001A and the HP 54100A/D ***MUST BE GROUNDED.*** *Failure to ground the common terminal during certain applications, such as operating these instruments from an external battery, will expose the operator to an electrical shock hazard that could be lethal (depending on the electrical energy available).*

CAUTION

Power must be removed from the HP 54100A/D when the HP 54001A is removed or installed, or the active probe may be damaged.

7A-2. MAINTENANCE

Maintenance consists of cleaning, adjusting, and replacing a probe cable. The probe cable can be removed from the probe pod by following the procedure in paragraph 7A-9 step 3. The HP 54001A must be recalibrated if the probe cable assembly is replaced.

Other field repairs are not recommended. If a failure should occur, contact your nearest Hewlett-Packard Sales and Service Office for details on the Blue Stripe Exchange Program.

7A-3. ACCESSORIES AVAILABLE

The following accessories are available for use with the HP 54001A:

HP 10221A 50 Ω probing Tee. Requires an HP Part No. 54001-23203 probe adapter.

HP 10211A (24 pin) and HP 10024A (16 pin) IC clips.

HP Part No. 54001-23203 probe adapter. The 54001-23203 adapts the HP 54001A mini-probe tip (of other HP mini-probes) to the accessories included with the HP 10020A resistive divider probe kit, and to the 10221A probing Tee.

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7A-4. SPECIFICATIONS

The list of specifications for the HP 54001A active probe when used with the HP 54100A/D is listed in table 7A-1 and in table 7A-2.

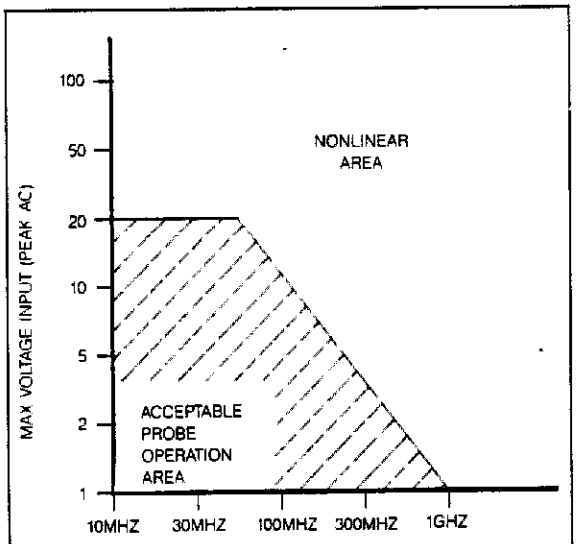
Table 7A-1. Specifications for HP 54001A Active Probe with HP 54100A/D.

Approximate Overall Length Metres (Ft)	Approximate Propagation Delay	Bandwidth	Risetime	Probe Input C Approx.	Probe Input R	Division Ratio:
1.5 metres (5 feet)	7.6 ns	700 MHz	450 ps	2 pf	10 kΩ	10:1 ±3%

Voltage Rating vs Frequency
Maximum Voltage Range for linear operation is shown in the voltage vs frequency (table 7A-2) **DO NOT** exceed the voltage levels for a given frequency or the probe may be permanently damaged.

Table 1. Specifications (Cont'd)

Table 7A-2. Voltage vs Frequency Chart.



GENERAL
OPERATING ENVIRONMENT
Temperature: 0°C to +55°C
Humidity: to 90% relative, to +40°C
Altitude: to 4.6 km (15 000 ft)
Shock: 30g's

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7A-5. REPLACEABLE PARTS

Replaceable parts are shown in Table 7A-3 through Table 7A-6. When ordering a part, address the order to the nearest Hewlett-Packard Sales and Service Office. Provide the model number, Hewlett-Packard part number, reference designator, check digit, quantity needed, and a complete description of the part.

7A-6. DIRECT MAIL ORDER

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from Hewlett-Packard parts center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through local Hewlett-Packard offices when orders require billing and invoicing).

c. No invoices - to provide these advantages, check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Hewlett-Packard offices.

Table 7A-3. Replaceable Parts for HP 54001A Active Probe.

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
A1				NOT ASSIGNED		
A2	54001-62101	2	1	10:1 PROBE	28480	54001-62101
A3	54001-69501	0	1	PROBE ACCOSSORY KIT	28480	54001-69501
MP1-7				NOT ASSIGNED		
MP8	54001-90902	0	1	OPERATING NOTE	28480	54001-90902
MP9	54001-94305	5	1	ID LABEL	28480	54001-94305

Table 7A-4. Replaceable Parts for A2 Assembly HP 54001-62101

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
A1	54001-61601	5	1	1.5 PROBE CABLE	28480	54001-61601
A2-3				NOT ASSIGNED		
A4	54001-66501	4	1	ACTIVE PROBE BOARDE ASSENBLMBLY	28480	54001-66501
MP1	0624-0637	3	1	SCREW-TPG 2-28 .375-IN-LG PAN-HD-TORX T8	28480	0624-0637
MP2	3030-0060	0	1	SCREW-SET 2-56 .062-IN-LG SMALL CUP-PT	28480	3030-0060
MP3	5081-7683	6	1	HEX SHOULDER NUT	28480	5081-7683
MP4	54001-23201	1	1	ADAPTER SLEEVE	28480	54001-23201
MP5				NOT ASSIGNED		
MP6	54001-94303	3	1	PROBE POD LABLE	28480	54001-94303
MP7	54001-94304	4	1	PROBE POD TOP LABEL	28480	54001-94304
MP8-13				NOT ASSIGNED		
MP14	0510-0958	0	1	RETAINER-PUSH ON CIRC EXT .094-IN-DIA	28480	0510-0958
MP15	54001-22401	1	1	RETAINER SCREW	28480	54001-22401

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Figure 7A-1. HP 54001A Active Probe Parts, 54001-69501.

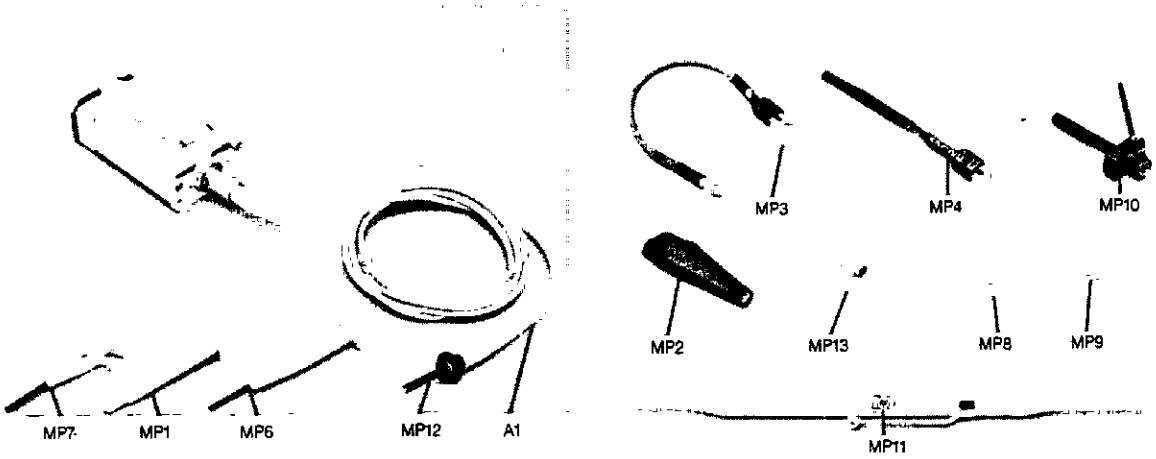


Table 7A-5. Replaceable Parts for A3, Accessory Kit, HP 54001-69501

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
MP1	10017-67602	4	1	ASSY-HOOK TIP	28480	10017-67602
MP2	5061-1258	7	1	CLIP ASSEMBLY	28480	5061-1258
MP3	54001-63201	5	1	CABLE ASSY GND	28480	54001-63201
MP4	54001-63202	6	1	LEAD ASSY-MIN PR	28480	54001-63202
MP5	5041-1484	9	1	GREEN WIRE MARKER	28480	5041-1484
MP6	10017-69501	6	1	GRABBER ASSEMBLY	28480	10017-69501
MP7	10230-62101	7	1	GRABBER ASSEMBLY	28480	10230-62101
MP8	1250-1737	4	1	SOCKET-COAXIAL .475 IN; BECU W/TEFLON	28480	1250-1737
MP9	1250-1918	3	1	VERT COAX SKT	28480	1250-1918
MP10	54001-67602	8	1	ASSY-SPANNER TIP	28480	54001-67602
MP11	8710-1300	0	1	ALIGNMENT TOOL	28480	8710-1300
MP12	10017-62302	1	1	INSULATING SLEEVE	28480	10017-63202
MP13	54001-23203	3	1	PROBE ADAPTER	28480	54001-23203
MP14	5041-1485	0	1	YELLOW WIRE MARKER	28480	5041-1485
MP15	5041-1486	1	1	ORANGE WIRE MARKER	28480	5041-1486
MP16	5041-1487	2	1	RED WIRE MARKER	28480	5041-1487
MP17	1460-1476	3	1	SPRING-TRSN .17-IN-OD .57-IN-OA-LG MUW	28480	1460-1476
MP18	54001-64501	0	1	PROBE CASE WITH FOAM	28480	54001-64501

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Table 7A-6. Replaceable Parts for A4, HP 54001-66501 PC Board.

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
C1				NOT ASSIGNED		
C2	0160-3879	7	2	CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
C3	0160-3879	7		CAPACITOR-FXD .01UF ±20% 100VDC CER	28480	0160-3879
C4				NOT ASSIGNED		
C5	0160-0573		1	CAPACITOR-FXD 4700PF	28480	0160-0573
C6	0160-3879		1	CAPACITOR-FXD .01µF	28480	0160-3879
C7	0121-0538	7	1	CAPACITOR-V TRMR-CER 5-2 5PF 250V	28480	0121-0538
C8	0180-3741	4	2	CAPACITOR-FXD 2 2UF±20% 25VDC TA	28480	0180-3741
C9	0180-3741	4		CAPACITOR-FXD 2 2UF±20% 25VDC TA	28480	0180-3741
C10	0160-4389	6	1	CAPACITOR-FXD 100PF ±5PF 200VDC CER	28480	0160-4389
C11	0160-0576	5	2	CAPACITOR-FXD 1UF ±20% 50VDC CER	28480	0160-0576
C12	0160-0576	5		CAPACITOR-FXD 1UF ±20% 50VDC CER	28480	0160-0576
C13	0160-6055	7	2	CAPACITOR-FXD 22UF ±5% 50VDC MET-POLYE	28480	0160-6055
C14	0160-6055	7		CAPACITOR-FXD 22UF ±5% 50VDC MET-POLYE	28480	0160-6055
E1	54001-26501	0	1	PROBE BD	28480	54001-26501
J1	1250-1947	8	1	CONNECTOR-RF SM-SLD FEM PC 50-OHM	28480	1250-1947
MP1	0380-1731	2	1	SPACER-PRESS-IN 1 70 MM LG 2 38 MM ID	46384	YC34564
MP2	0515-0659	8	1	SCREW-MACHINE ASSEMBLY M2 x 0 4 8MM-LG	28480	0515-0659
MP3	54001-29101	2	1	HYBRID SPRING	28480	54001 29101
MP4	54001-29102	3	1	HYBRID CLAMP	28480	54001 29102
MP5	54001-29104	5	1	GROUND SPRING	28480	54001 29104
MP6	54001-21101	6	1	HYBRID HEAT SINK	28480	54001 21101
P1	54001-67601	7	1	CONNECTOR ASSY	28480	54001-67601
R1	0698-7260	7	4	RESISTOR 10K 1% 05W F TC=0±100	24546	C3-1/8-T0-1002 F
R2	2100-2655	1	1	RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	73138	82PR100K
R3	0698-7284	5	1	RESISTOR 100K 1% 05W F TC=0±100	24546	C3-1/8-T0-1003-F
R4	0698-7188	8	1	RESISTOR 10 1% 05W F TC=0±100	24546	C3-1/8-T0-10R-F
R5	0698-7260	7		RESISTOR 10K 1% 05W F TC=0±100	24546	C3-1/8-T0-1002-F
R6	0698-7276	5	1	RESISTOR 46 4K 1% 05W F TC=0±100	24546	C3-1/8-T0-4642-F
R7	0698-7260	7		RESISTOR 10K 1% 05W F TC=0±100	24546	C3-1/8-T0-1002-F
R8	0698-7253	8	1	RESISTOR 5 11K 1% 05W F TC=0±100	24546	C3-1/8-T0-5111-F
R9	0698-7260	7		RESISTOR 10K 1% 05W F TC=0±100	24546	C3-1/8-T0-1002-F
R10	0698-7846	5	1	RESISTOR 1 01K 1% 125W F TC=0±25	19701	5033R-1/8-T9-1011-B
R11	0698-7093	4	1	RESISTOR 46 5 1% 125W F TC=0±25	28480	0698-7093
R12	0698-7267	4	1	RESISTOR 19 6K 1% 05W F TC=0±100	24546	C3-1/8-T0-1962-F
R13	2100-2061	3	1	RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	73138	82PR200
U1	1826-1151	7	1	IC OP AMP PRCN DUAL 8-DIP-C PKG	06665	OP-220GZ
U2	1NB7-8031	0	1	HYBRID	28480	1NB7-8031

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7A-7. HP 54001A CALIBRATION PROCEDURE

NOTE

The probe calibration should be performed in a properly calibrated HP 54100A/D.

7A-8. Recommended Calibration Test Equipment

The equipment recommended to adjust the HP 54001A probe is listed in table 7A-7.

Table 7A-7. Recommended HP 54001A Adjustment Test Equipment.

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Oscilloscope	No Substitute	HP 54100A/D or HP 54110D
Flat Pulse Generator	.5 Percent Flatness after 10 ns	Tek PG506
Fast Pulse Generator	70 ps risetime	Tek 284
ACCESSORIES		HP PART NUMBERS
Alignment Tool	In Probe Support Kit	8710-1300
Alignment Tool (Square tip)	In Probe Support Kit	8710-1515
Probe Extender	In Probe Support Kit	54100-63802
BNC to Probe Tip Adapter	In Probe Support Kit	1250-1454
Probing Tee	Traceable Cal only	10221A
50 ohm Termination	Traceable Cal only	909A option 12
GR874 to N-type (f)	Traceable Cal only	1250-0240
Probe Tip Adapter	Traceable Cal only	54001-23203

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7A-9. Equipment Setup

NOTE

Before performing any adjustments, the HP 54100A/D must have completed a 15-minute warm up period. Additionally, both pulse generators must also undergo a 15-minute warm up period.

1. Before an HP 54001A probe is calibrated, a probe extender, HP part number 54100-63802, must be installed in the HP 54100A/D. To do this:

   a. Turn oscilloscope off.

   b. Remove two top rear feet on oscilloscope, then remove top cover.

   c. Disconnect probe wiring harness and flexible coax from channel 1's sampling board (A5). Connect 54100-63802 probe extender in its place. Raising the PC board slightly will help facilitate these connections. Make sure board is reseated before continuing. Refer to figure 7A-2.



Figure 7A-2. Probe Extender Connections

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2. To calibrate probe circuitry, the probe board must be removed from probe shell. To accomplish this, remove two torx screws from rear of pod (see figure 7A-3).

3. Remove probe cable assembly from pod by loosening two set screws at front of pod, and unscrewing cable connector from pod (see figure 7A-3).

4. Reconnect cable connector to PC board as shown in figure 7A-2.

5. Connect PC board to probe extender. This allows adjustment points to be exposed. Refer to figure 7A-2.

6. Turn flat pulser off.

7. a. Insert probe tip into a BNC to probe tip adapter.

   b. Connect adapter to a BNC cable with a BNC barrel and then connect this cable to flat pulser's fast rise output.

8. On oscilloscope, set vertical sensitivity on channel 1 to 100 mV/div, and offset to zero. Set oscilloscope to autosweep mode. Adjust R2, probe offset adjustment, on probe PC board so trace coincides with X-axis graticule line (see figure 7A-4).

9. Setup oscilloscope as follows:

Channel 1:	On, Volts/div=100mV, offset= -300mV
Timebase:	Sec/div=10 ms, delay=0, triggered sweep
Trigger:	Mode=edge, source=chan 1, level= -300mV, slope=pos
Display:	Mode=average, averages=4, split screen off, graticule=frame
Delta V:	Markers on chan 1

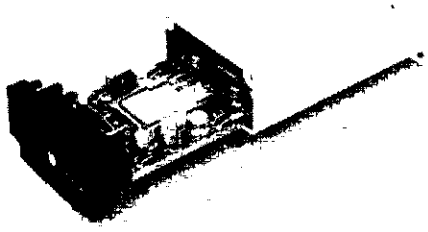


Figure 7A-3. Removal of Probe PC Board.

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10. Turn pulse generator on, and set its output for a 600 mV square wave with a 100 ms pulse period.

11. Adjust R13 (figure 7A-4) for flattest pulse top possible.

12. Change oscilloscope's sweep speed to 5 ns/div.

NOTE

In applications where a traceable calibration to the National Bureau of Standards is required, use step 13. In applications where traceability is not a concern, step 14 is an easier and less costly way of doing the calibration without diminishing the quality of the waveforms. Typically, the oscilloscope will see about 1% more overshoot and a 10 ps degradation in system risetime. However, this will not interfere with the probe's performance verification. Slight adjustments to the oscilloscope's vertical sensitivity, or the generator's output amplitude, may be required due to varying adjustment procedure setups. This adjustment will not interfere with the performance verification.

13. a. Disconnect probe tip from probe tip adapter.

    b. Connect probing Tee to fast pulser's output.

    c. Connect 50 Ω load on opposite end of Tee through a GR874 to N-type (f) adapter.

    d. Insert probe tip adapter into probing connector on Tee.

    e. Insert HP 54001A probe tip into probe tip adapter.

    f. Set pulser's mode switch to pulse output mode.

    g. Apply power to pulser.

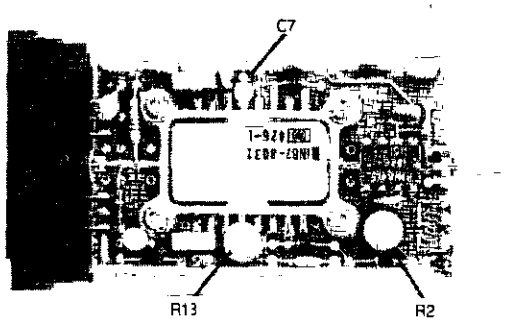


Figure 7A-4. HP 54001A Probe PC Board Adjustment Locations.

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14. a. Connect a GR874 to BNC (f) to pulse output on fast pulser

    b. Connect a probe tip to BNC (m) adapter to GR874 connector.

    c. Connect probe tip to BNC (m) adapter.

    d. Ensure pulser's mode switch is set to pulse output mode.

    e. Apply power to pulser.

NOTE

On the Tek 284, the TD bias may need to be adjusted slightly to get the pulser to fire into the non-50 Ω system. The fine adjustment for the tunnel diode is on the pulser's front panel. The coarse adjustment can be located inside the instrument on the right side when the insides are pulled forward (a captive screw on the front panel releases the pulser's insides from the frame.) See the Tek 284 instruction manual for complete details on adjusting the TD bias.

15. Adjust C7 for flattest overall pulse response with alignment tool with square tip. The square tip of this alignment tool can be broken very easily.

NOTE

At this point, it is sometimes helpful to repeat steps 7 and 8 to minimize the possibility of power up offset drift errors.

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7A-10. PERFORMANCE VERIFICATION

NOTE

Before performing this procedure, allow a 15 minute warm up period with the probe inserted into the pod slot. The best possible results are obtained when the pod has been adjusted to the input channel being tested. However, this is not a requirement.

7A-11. RECOMMENDED PERFORMANCE TEST EQUIPMENT

The test equipment recommended for use with the performance tests is listed in table 7A-8.

Table 7A-8. Recommended Performance Test Equipment.

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MODEL
DC Power Supply	±1 V	HP 6115A
Digital Voltmeter	±3 Percent dc V	HP 3478A
Fast Pulse Generator	Risetime less then 70 ps	Tek 284
Power Meter	3 Percent Accuracy	HP 436A
Power Sensor		HP 8482A
Frequency Synthesizer	1000 MHz Sine Wave	HP 8656B
Oscilloscope	No substitute	HP 54100A/D or HP 54110D
Sweep Oscillator	sweeps from 10 MHz to 900 MHz	HP 8620A with a HP 86220C

Table 7A-8 is continued on next page.

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Table 7A-8 (continued). Recommended Performance Test Equipment.

ACCESSORIES		HP PART NUMBERS
GR874 to BNC (f)		1250-0850
BNC (m) to Probe Tip Adapter		1250-1454
Probing Tee	Traceable Cal only	10221A
BNC Cable	48 inches	10503A
GR874 to N Type (f)	Traceable Cal, Two Required Non Traceable, One Required	1250-0240
50 ohm Load	Traceable Cal only	909A Option 12
Probe Tip Adapter	No Substitute	54001-23203
Power Splitter	Traceable Cal only	11667A
N Type (m) to BNC (f)		1250-0780
N Type (m) to N Type (m)		1250-1528
50 ohm Feedthrough		10100C
N type (m) to N type (m)	Traceable Cal only	1250-0778

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7A-12. RISETIME VERIFICATION

Equipment Setup:

1. Install HP 54001A into a calibrated oscilloscope.

NOTE

Use step 2a for a traceable calibration. Use step 2b for normal calibrations that do not need traceability to the National Bureau of Standards. Slight adjustments to the oscilloscope's vertical sensitivity, or the generator's output amplitude, may be required due to varying adjustment procedure setups. This adjustment will not interfere with the performance verification.

2a. 1) Connect GR874 to N type (f) adapter to probing tee.

2) Connect 50 Ω load to adapter.

3) Remove black insulating sleeve on probe tip.

4) Connect probe tip adapter to probing tee.

5) Insert probe tip of HP 54001A into adapter.

6) Connect entire assembly to pulse generator's fast rise output.

7) Switch pulse generator's mode switch to fast rise output.

2b. 1) Connect HP 54001A probe tip to pulse generator's fast rise output, through a GR874 to BNC (f) and a BNC to probe tip adapter.

2) Switch pulse generator's mode switch to fast rise output.

3. Turn on pulse generator and oscilloscope.

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Procedure:

1. a. Press ***Autoscale*** on oscilloscope.

   b. Adjust timebase to 1 ns/div.

   c. Set display mode, averages to 8.

   d. Check trigger slope, should be in positive slope.

2. Use delta V and delta T markers on oscilloscope to perform a risetime measurement as follows:

   a. Press ***Delta V*** and turn markers on.

   b. Press ***Auto-Top-Base*** and then *10%-90%*.

   c. Press ***Delta T*** and turn markers on.

   d. Select ***Start*** marker for first positive edge and ***Stop*** marker for first positive edge.

   e. Press ***Precise edge find*** key.

3. The risetime result should be ≤455 ps.

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7A-13. BANDWIDTH TEST

Instrument Setup:

Oscilloscope Setup:

Channel 1 & Channel 2	- Mode	- Normal
	- VOLTS/DIV	- 200 mV/div
	- OFFSET	- 0 V
Timebase	- SEC/DIV	- 2 ms
	- Delay ref at	- left
	- sweep	- trg'd
	- delay	- 0 s
Trigger	- Mode	- Edge
	- Source	- Chan 1
	- LEVEL	- +300 mV
	- Slope	- pos
	- HOLDOFF Time	- 21 ms
Display	- Mode	- Normal
	- DISPLAY TIME	- 200 ms
	- Split Screen	- Off
Delta V	- Marker 1 at +564 mV	
	- Marker 2 at -564 mV	

Sweep Oscillator:

Start marker	- .01 GHz
Stop marker	- .900 GHz
CW marker	- .700 GHz
Power Level	- +1 dBm
Trigger	- internal
Time	- 0.01
Markers	- AMPL
Marker sweep	- ON
Trigger Mode	- Auto

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Procedure:

1. Connect HP 54001A probe pod to channel 1 input of oscilloscope, and turn oscilloscope on.

NOTE

Use step 2a if a National Bureau of Standards traceable calibration is required. Use step 2b if a National Bureau of Standards traceable calibration is not required. Step 2b will provide similar results without the added expense of buying probing Tees. Slight adjusments to the oscilloscope's vertical sensitivity, or the generator's output amplitude, may be required due to varying adjustment procedure setups. This adjustment will not interfere with the performance verification.

2a. 1) Connect sweep oscillator's RF output to probing Tee through two adapters: N type (f) to GR874 and a N type (m) to N type (m).

2) Connect 50 Ω load to probing Tee through a GR874 to N type (f) adapter.

3) Connect probe tip adapter to probing Tee.

5) Insert probe tip of HP 54001A into adapter.

6) Turn channel 1 on and channel 2 off.

2b. 1) Connect sweep oscillator's RF output to a type N (m) to BNC (f) adapter.

2) Connect a BNC to probe tip adapter to the N type (m) to BNC (f) adapter.

3. Connect probe tip of HP 54001A to probe tip adapter.

4. Turn channel 1 on and channel 2 off.

3. Adjust sweep oscillator output level until displayed signal just fills 8 divisions vertically. (Use the Clear Display key to help see this.)

4. Adjust sweep oscillator time vernier until displayed waveform is 10 divisions in length.

5. Change oscilloscope DISPLAY time to Infinite.

6. Press ***Clear Display*** key.

7. The DELTA V markers show the 3 dB points and each horizontal division represents approximately 90 MHz. The sweep oscillator CW MARKER will show up as a dark line as the display area fills up. The waveform amplitude at the CW marker should be greater than the amplitude of the waveform at the delta V markers.

8. The approximate frequency where the waveform's amplitude crosses the Delta V markers should be ≥700 MHz.

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7A-14. DC VOLTAGE MEASUREMENT ACCURACY VERIFICATION.

Equipment Setup:

1. Connect a HP 54001A to oscilloscope's channel 1 input.
2. Turn oscilloscope on.
3. Adjust dc power supply output to exactly 300 mV (use a DVM to measure output level).

NOTE

Use step 4a for a traceable calibration. Use step 4b for normal calibrations that do not need traceability to the National Bureau of Standards.

4a. 1) Connect GR874 to N type (f) adapter to probing Tee.

2) Connect 50 Ω load to adapter.

3) Remove black insulating sleeve on probe tip.

4) Connect probe tip adapter to probing Tee.

5) Insert probe tip of HP 54001A into adapter.

6) Connect entire assembly to dc source's output.

4b. 1) Connect HP 54001A probe tip to dc source's output through three connectors: a GR874 to BNC (f), a BNC to probe tip adapter, and a 50 Ω load.

5. Adjust oscilloscope for following setup:

Split Screen	Off
Display Averages	32
Probe Attenuation	10:1
Trig Mode	Edge
Trig Source	Chan. 1
Trig Level	+300 mV
Trig Slope	Pos
Holdoff	70 ns
Sweep speed	1 ms/div
Mode	Auto Triggered
Delay	0
Delay Ref	Center
Chan Sensitivity	100 mV/div
Chan Offset	0
Channel not in use	Off

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Procedure:

1. Measure input signal's voltage level using Delta V markers as follows: (Be sure to let 32 acquisitions occur)
   a. Press ***Delta V*** and turn markers on.
   b. Press ***Auto-Top-Base*** followed by ***50%-50%***.
   c. The Delta V markers should be within 202 mV and 398 mV.
2. Change oscilloscope's offset to +300 mV.
3. Measure input signal's voltage level using procedure in step 1 above.
4. The Delta V markers should be within 244 mV and 356 mV.
5. a. Change dc supply to -300 mV (verify with DVM).
   b. Change trigger level to -300 mV.
   c. Change oscilloscope offset to 0 V.
6. Measure input signal's voltage level using Delta V markers as follows: (Be sure to let 32 acquisitions occur)
   a. Press ***Delta V*** and turn markers on.
   b. Press ***Auto-Top-Base*** followed by ***50%-50%***.
   c. The Delta V markers should be within -202 mV and -398 mV.
7. Change oscilloscope's offset to -300 mV.
8. Measure input signal's voltage level using procedure in step 1 above.
9. The Delta V markers should be within -244 mV and -356 mV.

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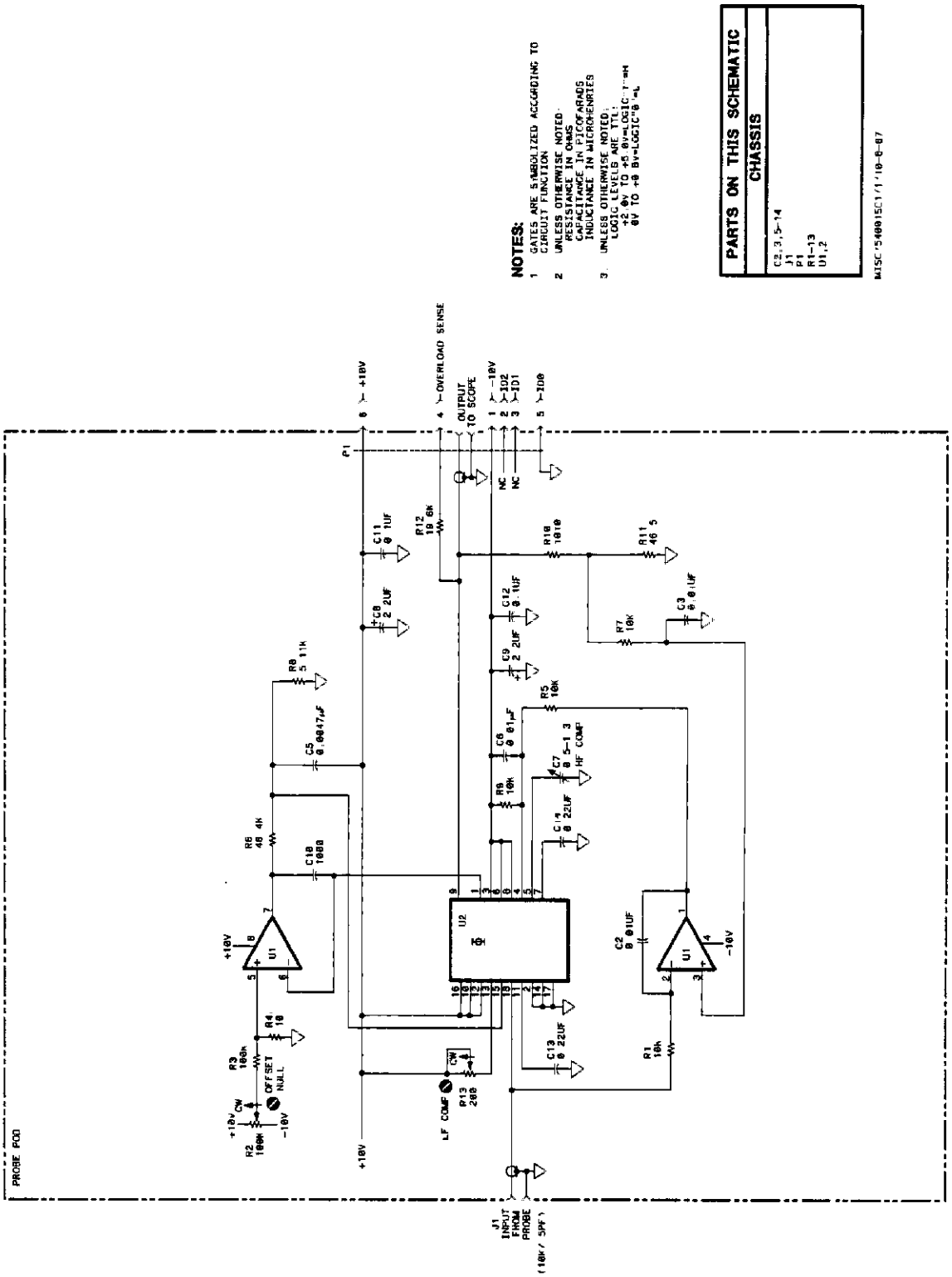


Figure 7A-5. Schematic diagram for HP 54001A Active Probe.

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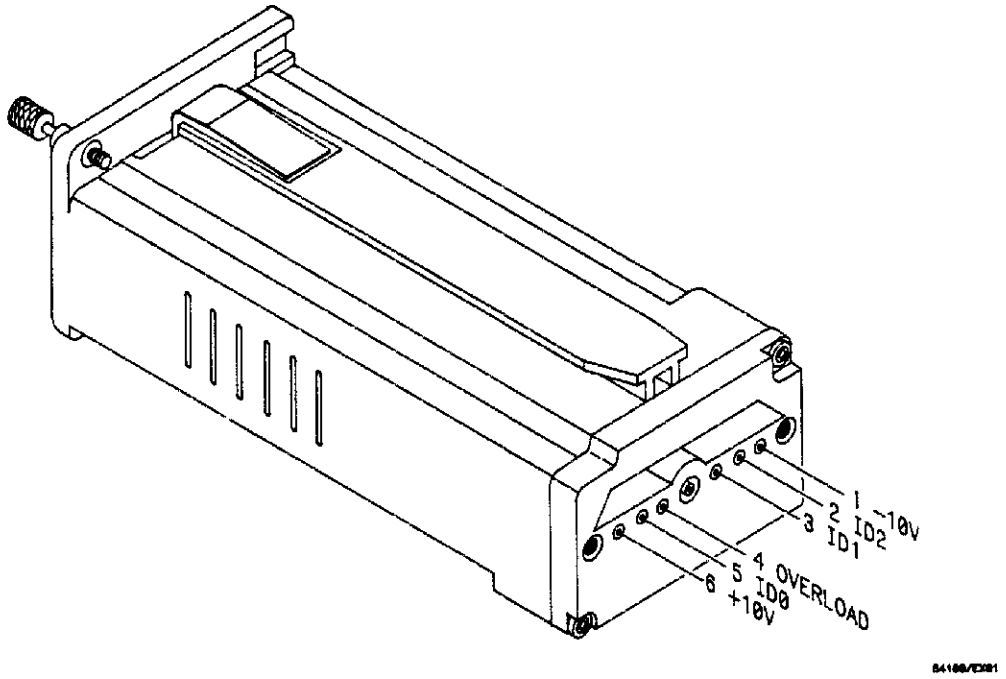


Figure 7A-6. Rear view of pod depicting pinout.

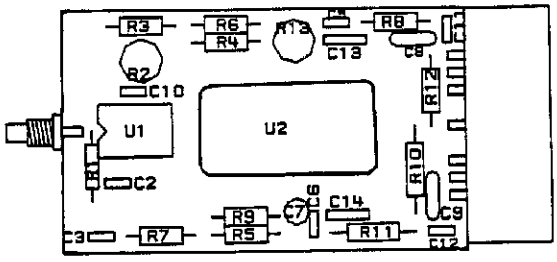


Figure 7A-7. Component locator for HP 54001A Active Probe.

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Table 7A-9. Performance Test Record

HEWLETT-PACKARD

Tested by _____

Probe Model No._____

Test Date _____

Probe Description _____

Work Order No. _____

Oscilloscope Model Used _____

Relative Humidity_____

Oscilloscope Serial Number _____

Temperature___Degrees___

Next Recommended Calibration Date

_____

Paragraph Number	Test		Results
7A-12	Risetime Specification: less then 455 ps	step 3	Minimum -- none Actual _____ps Maximum -- 455 ps
7A-13	Bandwidth Specification: dc to 700 MHz	step 8	Minimum -- 700 MHz Actual _____ MHz Maximum -- none
7A-14	DC Voltage Accuracy Specification: See note below	step 1c	Minimum -- 202 mV Actual _____ mV Maximum -- 398 mV
		step 4	Minimum 244 mV Actual _____ mV Maximum 356 mV
		step 6c	Minimum -- -202 mV Actual _____ mV Maximum -- -398 mV
		step 9	Minimum -244 mV Actual _____ mV Maximum -356 mV

NOTE: Specification for DC Voltage Accuracy: ±2% of Offset
±6% of Fullscale
±50 mV

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SECTION 7B

7B-1. INTRODUCTION

The HP 54002A can be used in any of the three pod receptacles in the HP 54100A, or any of the four pod receptacles in the HP 54100D Digitizing Oscilloscopes. A knurled knob is provided to secure the pod in the receptacle.

WARNING

The HP 54002A and HP 54100A/D have a common terminal at GROUND POTENTIAL (in accordance with OSHA requirements and the National Electrical Code). Exposed metallic surfaces of the HP 54002A and the HP 54100A/D ***MUST BE GROUNDED.*** *Failure to ground the common terminal during certain applications, such as operating these instruments from an external battery, will expose the operator to an electrical shock hazard that could be lethal (depending on the electrical energy available).*

7B-2. SPECIFICATIONS.

The list of specifications for the HP 54002A probe when used with the HP 54100A/D is listed in table 7B-1.

Table 7B-1. Specifications for HP 54002A Probe with HP 54100A/D.

Maximum Input Voltage	Bandwidth	Risetime	Probe Input Resistance	Division Ratio:
5V rms	dc to 1 GHz	350 ps (10% to 90%)	50 Ω	1:1

7B-3. PERFORMANCE VERIFICATION

The HP 54002A pod is used during the HP 54100A/D performance verification tests. If there is a problem with the pod, it will show up during these tests. Therefore this section of the service manual does not include any performance verification tests for the HP 54002A.

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SECTION 7C

7C-1. INTRODUCTION

The HP 54003A can be used in any of the three pod receptacles in the HP 54100A, or any of the four pod receptacles in the HP 54100D Digitizing Oscilloscopes. A knurled knob is provided to secure the pod in the receptacle.

WARNING

The HP 54003A and HP 54100A/D have a common terminal at GROUND POTENTIAL (in accordance with OSHA requirements and the National Electrical Code). Exposed metallic surfaces of the HP 54003A and the HP 54100A/D ***MUST BE GROUNDED****. Failure to ground the common terminal during certain applications, such as operating these instruments from an external battery, will expose the operator to an electrical shock hazard that could be lethal (depending on the electrical energy available).*

CAUTION

Power must be removed from the HP 54100A/D when the HP 54003A is removed or installed, or the active probe may be damaged.

7C-2. MAINTENANCE

Maintenance consists of cleaning, adjusting, and replacing probe cables. The probe cable can be removed from the probe pod by following the procedure in paragraph 7C-9 step 3. The HP 54003A must be recalibrated if the probe cable assembly is replaced.

Other field repairs are not recommended. If a failure should occur, contact your nearest Hewlett-Packard Sales and Service Office for details on the Blue Stripe Exchange Program.

7C-3. ACCESSORIES AVAILABLE

The following accessories are available for use with the HP 54003A:

HP 10221A 50 Ω probing Tee. Requires an HP Part No. 54001-23203 probe adapter.

HP 10211A (24 pin) and HP 10024A (16 pin) IC clips.

HP Part No. 54001-23203 probe adapter. The 54001-23203 adapts the HP 54003A with the HP 54003-61617 10:1 probe assembly to the accessories included with the HP 10020A resistive divider probe kit, and to the probing Tee.

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7C-4. SPECIFICATIONS.

The list of specifications for the HP 54003A active probe when used with the HP 54100A/D is listed in table 7C-1 and in table 7C-2.

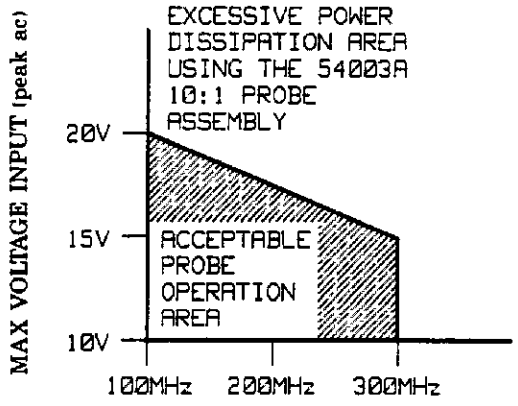
Table 7C-1. Specifications for HP 54003A Active Probe with HP 54100A/D.

Pod	Approximate Overall Length Metres (Ft)	Division Ratio	Approximate Propagation Delay	Typical Circuit Loading		Bandwidth	Rise Time
54003A		1:1	1 ns	Resistive 1 MΩ	Capacitive 10 PF	300 MHz	1.2 ns
54003A used with 54003-61617 10:1 probe Assembly	1.1 3.6	10:1	5 ns	1 MΩ	8 pF	300 MHz	1.2 ns

Pod	Maximum Input
54003A	±2V
54003A used with 54003-61617 10:1 Probe Assembly	±20V

VOLTAGE RATING VS FREQUENCY
Maximum power capability of the probe resistive center conductor is shown in the voltage vs frequency curve on page 2.

Table 7C-2. Voltage vs Frequency Chart.



Maximum Input Voltage Rating Curve at 25°C

GENERAL
OPERATING ENVIRONMENT
Temperature: 0°C to +55 40°C
Humidity: to 90% relative, to +40°C
Altitude: to 4.6 km 15 000 ft

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7C-5. REPLACEABLE PARTS

Replaceable parts are shown in Table 7C-3 through Table 7C-6. When ordering a part, address the order to the nearest Hewlett-Packard Sales and Service Office. Provide the model number, Hewlett-Packard part number, reference designator, check digit, quantity needed, and a complete description of the part.

7C-6. DIRECT MAIL ORDER

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from Hewlett-Packard parts center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through local Hewlett-Packard offices when orders require billing and invoicing).

c. No invoices - to provide these advantages, check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Hewlett-Packard offices.

Table 7C-3. Replaceable Parts for HP 54003A Active Probe.

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
A1	54003-62101	4	1	1 MOHM INPUT	28480	54003-62101
A2				NOT ASSIGNED		
A3	54001-69501	0	1	PROBE ACCESSORY KIT	28480	54001-69501
MP1	54003-90901	1	1	OPERATING NOTE	28480	54003-90901
MP2	54003-94305	7	1	ID LABEL	28480	54003-94305

Table 7C-4. Replaceable Parts for A2 Assembly HP 54003-62101

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
A1				NOT ASSIGNED		
A2	54003-61617	5	1	10 1 PROBE ASSEMBLY	28480	54003-61617
A3				NOT ASSIGNED		
A4	54003-66501	6	1	PROBE PC BOARD	28480	54003-66501
MP1	0624-0637	3	1	SCREW-TPG 2-28 .375-IN-LG PAN-HD-TORX T8	28480	0624-0637
MP2	54001-94304	4	1	PROBE POD TOP LABEL	28480	54001-94304
MP3	5081-7683	6	1	HEX SHOULDER NUT	28480	5081-7683
MP4				NOT ASSIGNED		
MP5	54001-44502	9	1	PROBE POD	28480	54001-44502
MP6	54003-94307	9	1	PROBE POD LABLE	28480	54003-94307
MP7-13				NOT ASSIGNED		
MP14	0510-0958	0	1	RETAINER-PUSH ON CIRC EXT .094-IN-DIA	28480	0510-0958
MP15	54001-22401	1	1	RETAINER SCREW	28480	54001-22401

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Figure 7C-1. HP 54003A Active Probe Parts, 54001-69501.

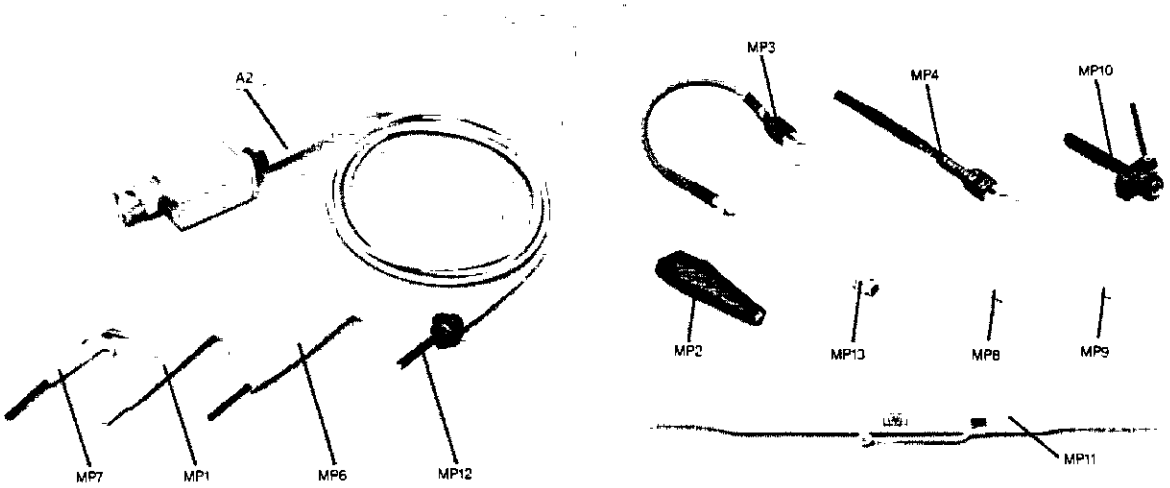


Table 7C-5. Replaceable Parts for A3, Accessory Kit, HP 54001-69501

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
MP1	10017-67602	4	1	ASSY-HOOK TIP	28480	10017-67602
MP2	5061-1258	7	1	CLIP ASSEMBLY	28480	5061-1258
MP3	54001-63201	5	1	CABLE ASSY GND	28480	54001-63201
MP4	54001-63202	6	1	LEAD ASSY-MIN PR	28480	54001-63202
MP5	5041-1484	9	1	GREEN WIRE MARKER	28480	5041-1484
MP6	10017-69501	6	1	GRABBER ASSEMBLY	28480	10017-69501
MP7	10230-62101	7	1	GRABBER ASSEMBLY	28480	10230-62101
MP8	1250-1737	4	1	SOCKET-COAXIAL .475 IN; BECU W/TEFLON	28480	1250-1737
MP9	1250-1918	3	1	VERT COAX SKT	28480	1250-1918
MP10	54001-67602	8	1	ASSY-SPANNER TIP	28480	54001-67602
MP11	8710-1300	0	1	ALIGNMENT TOOL	28480	8710-1300
MP12	10017-62302	1	1	INSULATING SLEEVE	28480	10017-63202
MP13	54001-23203	3	1	PROBE ADAPTER	28480	54001-23203
MP14	5041-1485	0	1	YELLOW WIRE MARKER	28480	5041-1485
MP15	5041-1486	1	1	ORANGE WIRE MARKER	28480	5041-1486
MP16	5041-1487	2	1	RED WIRE MARKER	28480	5041-1487
MP17	1460-1476	3	1	SPRING-TRSN .17-IN-OD .57-IN-OA-LG MUW	28480	1460-1476
MP18	54001-64501	0	1	PROBE CASE WITH FOAM	28480	54001-64501

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Table 7C-6. Replaceable Parts for A4, HP 54003-66501 PC Board.

Reference Designation	HP Part Number	CD	Qty.	Description	Mfr Code	Mfr Part Number
C1	0160-3878	6	1	CAPACITOR-FXD 1000PF ±20% 100VDC CER	28480	0160-3878
C2	0160-0576	5	2	CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-0576
C3	0160-0576	5		CAPACITOR-FXD .1UF ±20% 50VDC CER	28480	0160-0576
C4	0180-3741	4	3	CAPACITOR-FXD 2.2UF±20% 25VDC TA	28480	0180-3741
C5	0180-3741	4		CAPACITOR-FXD 2.2UF±20% 25VDC TA	28480	0180-3741
C6	0180-3741	4	1	CAPACITOR-FXD 2.2UF±20% 25VDC TA	28480	0180-3741
C7	0160-0573	2		CAPACITOR-FXD 4700PF ±20% 100VDC CER	28480	0160-0573
E1	54003-26501	2	1	PC BOARD	28480	54003-26501
H1	0515-0659	8	4	SCREW MACHINE ASSEMBLY M2 X 0.4 8MM-LG	28480	0515-0659
H2				NOT ASSIGNED		
H3	0515-1320	2	2	SCREW-MACH M2 X 0.4 13MM-LG	28480	0515-1320
H4-21				NOT ASSIGNED		
H22	0515-1275	6	2	SCREW-THD-RLG 2.26 X .91 5MM-LG PAN-HD	28480	0515-1275
J1	1250-0524	5	1	CONNECTOR-RF BNC FEM SGL-HOLE-RR 50-OHM	28480	1250-0524
MP1	54001-21101	6	1	HYBRID HEAT SINK	28480	54001-21101
MP2	54001-29101	2	1	HYBRID SPRING	28480	54001-29101
MP3	54002-24101	3	1	PLATE SUPPORT	28480	54002-24101
MP4	54001-29102	3	1	HYBRID CLAMP	28480	54001-29102
MP5	0380-1731	2	4	SPACER-PRESS-IN 1.70 MM LG, 2.38 MM ID	46384	YC3-4564
MP6	0590-1637	2	2	THREADED INSERT-NUT M2 X 0.4 1.5-MM-LG	28480	0590-1637
MP7	54001-29104	5	1	GROUND SPRING	28480	54001-29104
P1	54001-67601	7	1	CONNECTOR ASSEMBLY	28480	54001-67601
R1	0698-3944	6	1	RESISTOR 825K 1% .125W F TC=0±25	28480	0698-3944
R2	0698-7583	7	1	RESISTOR 179.43K 1% 125W F TC=0±25	19701	5033R-1/8-T9-179431-B
R3	0698-7260	7	1	RESISTOR 10K 1% .05W F TC=0±100	24546	C3-1/8-T0-1002-F
R4	0698-7250	5	1	RESISTOR 3.83K 1% .05W F TC=0±100	24546	C3-1/8-T0-3831-F
R5	2100-1986	9	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	73138	82PR1K
R6	0699-0214	9	1	RESISTOR 17.8K 1% .125W F TC=0±25	28480	0699-0214
R7	0698-7200	5	1	RESISTOR 31.6 1% .05W F TC=0±100	24546	C3-1/8-TO-31R6-F
R8	0699-0283	2	1	RESISTOR 81.92K 1% .125W F TC=0±25	28480	0699-0283
R9	0698-7284	5	1	RESISTOR 100K 1% .05W F TC=0±100	24546	C3-1/8-T0-1003-F
R10	2100-2031	7	1	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	73138	82PR50K
R11	0698-7257	4	1	RESISTOR 19.6K 1% .05W F TC=0±100	24546	C3-1/8-T0-1962-F
R12	0698-7196	8	1	RESISTOR 21.5 1% .05W F TC=0±100	24546	C3-1/8-TO-21R5-F
U1	1826-0493	8	1	IC OP AMP LOW-BIAS-H-IMPD 8-DIP-P PKG	04713	MLM308AP1
U2	1NB7-8038	7	1	HI Z PROBE HYBRID	28480	1NB7-8038

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7C-7. HP 54003A CALIBRATION PROCEDURE

NOTE

The probe calibration should be performed in a properly calibrated HP 54100A/D.

7C-8. Recommended Calibration Test Equipment

The equipment recommended to adjust the HP 54003A probe is listed in table 7C-7.

Table 7C-7. Recommended HP 54003A Adjustment Test Equipment.

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Digital Multimeter	3 Percent dc Accuracy	HP 3465A
Function Generator	11 Hz, 0 V offset, 120 mV Square Wave	HP 8116A
Pulse Generator		HP 8161A
Oscilloscope	No Substitute	HP 54100A/D or HP 54110D
Flat Pulse Generator	Less then 10 percent	Tek PG 506
Fast Pulse Generator	Risetime Less then 70 ps	Tek 284

Table 7C-7 is continued on next page.

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Table 7C-7(continued). Recommended HP 54003A Adjustment Test Equipment.

ACCESSORIES		HP PART NUMBERS
Probe Support Kit	No Substitute	54100-69004
50 ohm BNC Feedthrough		10100C
10:1 Probe Divider		54003-61617
GR874 to BNC(f)	Quantity of Two	1250-0850
Probing Tee	Traceable Cal only	10221A
GR874 to N-type (f)	Traceable Cal only	1250-0240
Probe Tip Adapter	Traceable Cal only	54001-23203
BNC Cable	48 inches	10503A
50 ohm Load	Traceable Cal Only	909A opt 12
BNC(f) to Probe Tip Adapter		1250-1454

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7C-9. Equipment Setup

NOTE

Before performing any adjustments, the HP 54100A/D must have completed a 15-minute warm up period. Additionally, both pulse generators must also undergo a 15-minute warm up period.

1. Before a 54003A probe is calibrated, a probe extender, HP part number 54100-63802, must be installed in the HP 54100A/D. To do this:

   a. Turn oscilloscope off and wait three minutes for power supply to discharge.

   b. Remove two top rear feet on oscilloscope, then remove top cover.

   c. Disconnect probe wiring harness and flexible coax from channel 1's sampling board (A5). Connect probe extender in its place. Raising the PC board slightly will help facilitate these connections. Make sure board is reseated before continuing. Refer to figure 7C-2.

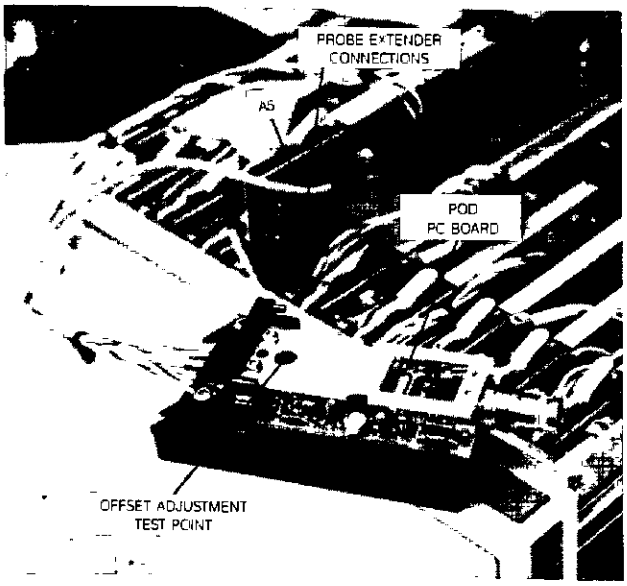


Figure 7C-2. Probe Extender Connections

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2. To calibrate probe circuitry, the probe board must be removed from probe shell. To accomplish this, remove two torx screws from rear of pod (see figure 7C-3).

3. Remove probe cable assembly from pod by loosening two set screws at front of pod, and unscrewing cable connector from pod (see figure 7C-3).

4. Reconnect cable connector to PC board as shown in figure 7C-2.

5. Connect PC board to probe extender. This allows adjustment points to be exposed (see figure 7C-2).

Offset Adjustment Procedure:

1. Turn oscilloscope on.

2. a. Set the digital multimeter to 20 mV range.

   b. Touch test leads together.

   c. Reading should be less than 0.01 mV.

3. Connect ground lead of digital multimeter to BNC connector ground shell on HP 54003A PC board.

4. Monitor output offset voltage on output connector's center conductor.

   This test point is accessed through hole in metal shield on top of pod PC board. Refer to figure 7C-3.

5. Adjust R10 for a minimum reading on digital multimeter. Reading should be less than 0.1 mV.

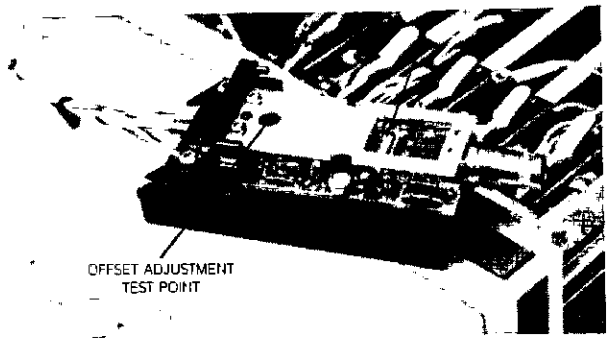


Figure 7C-3. Offset Adjustment Test Point

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7C-10. GAIN ADJUST AND DYNAMIC RANGE CHECK.

Equipment Setup:

1. Install an HP 54002A input pod in channel 2.

2. Connect probe extender to channel 1's sampling board and install HP 54003A PC board in extender. Refer to section 7C-9, steps 1-5.

3. Turn oscilloscope on.

4. Set up oscilloscope as follows:

Chan. 2	on
Sensitivity	20 mV/div
offset	0 V
Sweep speed	10 ms/div
Timebase	
delay	0
delay reference	left
Mode	Trg'd sweep
Trigger mode	edge
source	chan. 2
level	0 V
display mode	average
No. of averages	8
graticule	grid

5. a. Set function generator for 11 Hz square wave.

   b. Set function generator for 120 mV peak to peak.

   c. Set function generator for 0 V offset

   d. Connect function generator's output to oscilloscope's channel 2 input.

6. Connect 50 Ω feedthrough termination to HP 54003A.

7. Connect function generator to HP 54003A.

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8. a. Turn channel 2 off and turn channel 1 on.

   c. Select channel 1 as trigger source.

9. Use channel 1's offset to set pulse top to closest graticule line. For a reference, use a point about 40 ms after start of pulse.

10. a. Set oscilloscope sweep speed to 10 µs/div.

    b. Adjust R5 for flattest response using graticule line as a reference. The overall flatness of the entire waveform is more important during this adjustment than the overshoot and undershoot flatness. Refer to figure 7C-4.

11. a. On oscilloscope, set channel 1's vertical sensitivity to 1 V/div.

    b. Set sweep speed to 10 ms/div.

12. a. Move BNC cable on function generator from function generator's low output to high output.

    b. An approximately 4 V peak-to-peak pulse should be on oscilloscope's screen.

    c. The displayed square wave should have a flat top, this verifies the 4 V peak-to-peak dynamic range.

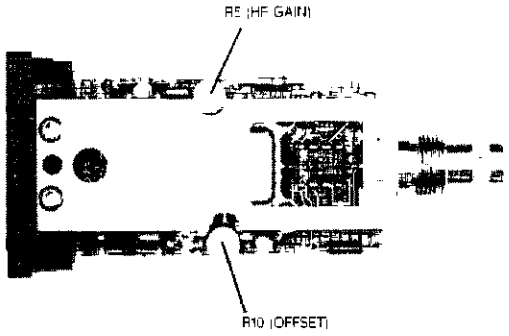


Figure 7C-4. HP 54003A Probe PC Board Adjustment Locations.

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7C-11. LOW FREQUENCY COMPENSATION.

Equipment Setup:

1. a. Install HP 54003A probe with HP 54003-61617 mini probe into oscilloscope's channel 1 input.

   b. Remove probe tip's black plastic protective cover.

   c. Insert probe tip into 50 Ω probing Tee with probe tip adapter. Refer to figure 7C-5.

   d. Connect an N type (f) to GR874 to one side of probing Tee.

   e. Connect a 50 Ω termination to this connector.

   f. On other side of probing Tee, connect a GR874 to BNC (f) adapter.

   g. Connect a 48-inch BNC cable from this side of probing Tee to flat pulser.

NOTE

Connecting the HP 54003-61617 probe tip with insulating sleeve intact to the PG 506 pulser through a BNC (f) to probe tip adapter, provides less expensive but reliable adjustment results. When using this procedure, the oscilloscope's vertical sensitivity may need to be adjusted. This adjustment will not interfere with the performance verification.

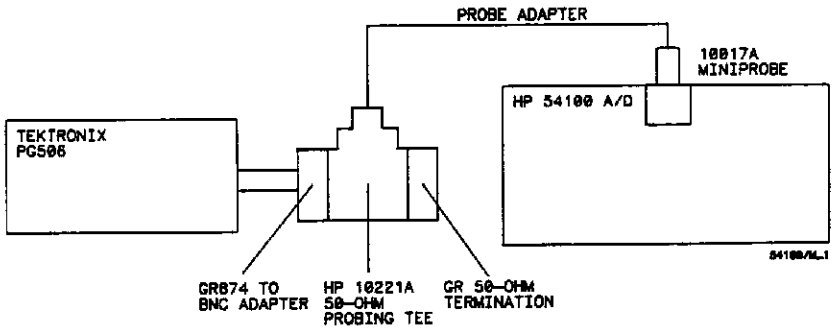


Figure 7C-5. Equipment Setup for Flatness Adjustment.

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2. Setup flat pulser for:

output	fast rise
period	10 ms
amplitude	maximum

3. Setup oscilloscope for:

Chan. 1	on
mode	normal
sensitivity	10 mV/div
offset	0 V
Chan. 2	off
sweepspeed	10 µs/div
delay	0 s
reference	center
sweep	triggered
Trigger	
mode	edge
source	chan. 1
slope	positive
level	-20 mV
Display	average
No. of	8
Delta V	off

Procedure:

1. Adjust low frequency capacitor C1 (visible through hole in compensation box) for best square wave response. Use X-axis graticule as a reference.

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7C-12. HIGH FREQUENCY ADJUSTMENT.

Equipment Setup:

1. Setup fast rise pulser for:

mode	square wave
period	100 ns
amplitude	1.0 V

2. Setup the oscilloscope for:

Chan. 1	on
mode	normal
sensitivity	sensitivity 10 mV/div
offset	0 V
Chan. 2	off
sweep speed	5 ns/div
delay	-10 ms
reference	left
sweep	triggered
Trigger mode	edge
source	Chan. 1
slope	positive
level	10 mV
display	average
No. of	8
Delta V	on
marker 1	23.2 mV
marker 2	26.6 mV

3. Use same setup as step #1. Then disconnect 48 BNC cable from flat pulser and connect it to fast rise pulser through a GR874 to BNC (f) adapter. See figure 7C-6.

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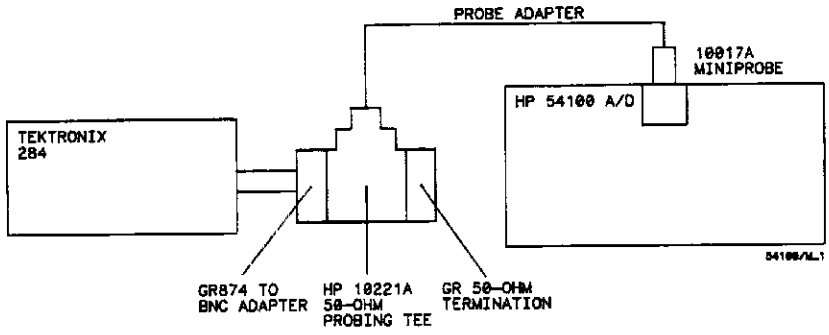


Figure 7C-6. Equipment Setup for High Frequency Adjustment.

Procedure:

1. There should be a square wave displayed on oscilloscope.

2. Remove compensation box cover from HP 54003-61617.

3. Position compensation box cover on back side of compensation box to expose adjustments. This establishes enough stray capacitance for adjustments.

4. Resistor R1 adjusts long time constant responses up to about 10 ns.

   Resistor R3 adjusts shorter time constant responses.

   Alternately adjust R1 and R3 for best response using Delta V marker 1 as a reference.

5. Install compensation box cover.

6. Note change in pulse response. Typically the cover's absence causes pulse response overshoot to increase by 2%, compared with when cover is installed.

7. Remove cover again and readjust R1 and R3 to compensate for cover.

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7C-13. PERFORMANCE VERIFICATION

NOTE

Contained in this section are complete procedures to verify both the HP 54003A with the HP 54003-61617, and the HP 54003A by itself. Except for the specific case where the HP 54003A is used by itself, performance verification done on the HP 54003-61617 combination is sufficient for providing a complete performance check. Therefore, the performance verification procedure can be shortened if verification of the HP 54003A by itself is eliminated.

NOTE

Before performing this procedure, allow a 15 minute warm up period with the probe inserted into the pod slot. The best possible results are obtained when the pod has been adjusted to the input channel being tested. However, this is not a requirement.

7C-14. RECOMMENDED PERFORMANCE TEST EQUIPMENT

The test equipment recommended for use with the performance tests is listed in table 7C-8.

Table 7C-8. Recommended Performance Test Equipment.

INSTRUMENT	CRITICAL SPECIFICATION	RECOMMENDED MODEL
DC Power Supply	±1 V	HP 6115A
Pulse Generator	Risetime less then 70 ps	Tek 284
Power Meter	3 Percent Accuracy	HP 436A
Power Sensor		HP 8482A
Frequency Synthesizer	1000 MHz Sine Wave	HP 8656B
Oscilloscope	No substitute	HP 54100A/D or HP 54110D

Table 7C-8 is continued on next page.

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Table 7C-8 (continued). Recommended Performance Test Equipment.

ACCESSORIES		HP PART NUMBERS
GR874 to BNC (f)	No Substitute	1250-0850
BNC (m) to Probe Tip Adapter		1250-1454
Probing Tee	Traceable Cal only	10221A
BNC Cable	48 inches	10503A
GR874 to N Type (f)	Traceable Cal, Two Required Non Traceable, One Required	1250-0240
50 ohm Load	Traceable Cal only	909A Option 12
Probe Tip Adapter	No Substitute	54001-23203
Probing Tee	Traceable Cal only	11667A
N type (m) to M type (m)	Traceable Cal only	1250-0778
N Type (m) to BNC (f)		1250-0780
N Type (m) to N Type (m)		1250-1528
50 ohm Feedthrough		10100C

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7C-15. RISETIME VERIFICATION

Equipment Setup:

1. Install HP 54003A with a HP 54003-61617, which was adjusted as a pair, into a calibrated oscilloscope.

NOTE

Use step 2a for a traceable calibration to National Bureau of Standards. Use step 2b for normal calibrations that do not need traceability to the National Bureau of Standards. Slight adjustments to the oscilloscope's vertical sensitivity, or the generator's output amplitude, may be required due to varying adjustment procedure setups. This adjustment will not interfere with the performance verification.

2a. 1) Connect GR874 to N type (f) adapter to probing Tee.

2) Connect 50 Ω load to adapter.

3) Remove black insulating sleeve on probe tip.

4) Connect probe tip adapter to probing tee.

5) Insert probe tip of HP 54003-61617 into adapter.

6) Connect entire assembly to pulse generator's fast rise output.

7) Switch pulse generator's mode switch to fast rise output.

2b. 1) Connect HP 54003-61617 probe tip to pulse generator's fast rise output, a GR874 to BNC (f) and a BNC to probe tip adapter.

2) Switch pulse generator's mode switch to fast rise output.

3. Turn on pulse generator and oscilloscope.

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Procedure:

1. a. Press ***Autoscale*** on oscilloscope.

   b. Adjust timebase to 2 ns/div.

   c. Set display mode, averages to 8.

   d. Check trigger slope, should be in positive slope.

2. Use Delta V and Delta T markers on oscilloscope to perform a risetime measurement as follows.

   a. Press ***Delta V*** and turn markers on.

   b. Press ***Auto-Top-Base*** and then ***10%-90%.***

   c. Press ***Delta T*** and turn markers on.

   d. Select ***Start*** marker for first positive edge and ***Stop*** marker for first positive edge.

   e. Press ***Precise edge find*** key.

3. The risetime result should be ≤1.2 ns.

4. Use step 4a for a traceable calibration to the National Bureau of Standards. Use step 4b for a non-traceable calibration.

4a. 1) Remove 10:1 divider probe (HP 54003-61617), Probing Tee, GR874 to N type (f), probe tip adapter, and 50 Ω load.

   2) Connect Fast rise source to Tee through a N type (m) to N type (m) adapter.

   3) Connect HP 54003A BNC input Tee through a 48- inch BNC cable and a N type (m) to BNC (f) adapter.

   4) Connect 50 Ω load to Tee.

   5) Set oscilloscope's probe attenuation to 1:1.

4b. 1) Remove 10:1 divider probe and BNC (f) to probe tip adapter.

   2) Connect HP 54003A to generator with a 48- inch BNC Cable.

   3) Set oscilloscope's probe attenuation to 1:1.

5. Repeat steps 1-4 to find risetime value of HP 54003A probe without the HP 54003-61617 divider attached.

6. Risetime should be ≤1.2 ns.

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7C-16. BANDWIDTH TEST

NOTE

Make sure the probe attenuation factor is set for 10:1 when testing the HP 54003A with the HP 54003-61617, and that it is set to 1:1 when testing the HP 54003A by itself.

Instrument Setup:

Oscilloscope Setup:

Channel 1 & Channel 2	- Mode	- Normal
	- VOLTS/DIV	- 200 mV/div
	- OFFSET	- 0V
Timebase	- SEC/DIV	- 2 ms
	- Delay ref at	- left
	- sweep	- trg'd
	- delay	- 0 S
Trigger	- Mode	- Edge
	- Source	- Chan 1
	- LEVEL	- +300 mV
	- Slope	- pos
	- HOLDOFF Time	- 21 ms
Display	- Mode	- Normal
	- DISPLAY TIME	- 200 ms
	- Split Screen	- Off
Delta V	- Marker 1 at +564 mV	
	- Marker 2 at -564 mV	

Sweep Oscillator:

Start marker	- .01 GHz
Stop marker	- .300 GHz
CW marker	- .500 GHz
Power Level	- +1 dBm
Trigger	- internal
Time	- 0.01
Markers	- AMPL
Marker sweep	- ON
Trigger Mode	- Auto

NOTE

*Procedure 1 is for calibrating the HP 54003A probe pod **WITH*** a HP 54003-6617 10:1 divider. Procedure 2 is for calibrating the HP 54003A ***WITHOUT*** the HP 54003-61617.

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Procedure 1: For the HP 54003A probe pod **WITH** the HP 54003-61617.

1. Connect HP 54003A probe pod with a HP 54003-61617 to channel 1 input of oscilloscope, and turn oscilloscope on.

NOTE

Use step 2a for a traceable calibration to National Bureau of Standards. Use step 2b for calibrations that do not need traceability to the National Bureau of Standards. Step 2b will provide similar results as step 2a, but without the added expense of probing tees.

2a. 1) Connect sweep oscillator's RF output probing Tee through two adapters: N type (f) to GR874, and a N type (m) to N type (m).

2) Connect 50 Ω load, to probing tee through a GR874 to N type (f) adapter.

3) Insert probe tip of HP 54003-61617 into probe tip adapter and attach adapter to Tee.

4) Turn channel 1 on and channel 2 off.

2b. 1) Connect sweep oscillator's RF output to HP 54003-61617 probe tip through two adapters: N type (m) to BNC (f) and a BNC to probe tip adapter.

2) Turn channel 1 on and channel 2 off.

3. Adjust sweep oscillator output level until displayed signal just fills 8 divisions vertically. (Use the Clear Display key to help see this.)

4. Adjust sweep oscillator time vernier until displayed waveform is 10 divisions in length.

5. Change oscilloscope DISPLAY time to Infinite.

6. Press ***Clear Display*** key.

7. The Delta V markers show the 3 dB points and each horizontal division represents approximately 50 MHz. The sweep oscillator CW MARKER will show up as a dark line as the display area fills up. The waveform amplitude at the CW marker should be greater than the amplitude of the waveform at the Delta V markers.

8. The approximate frequency where the waveform's amplitude crosses the Delta V markers should be ≥300 MHz.

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Procedure 2: For the HP 54003A probe pod only **WITHOUT** the HP 54003-6167.

1. Connect HP 54003A probe pod to channel 1 input of oscilloscope, and turn oscilloscope on.

NOTE

Use step 2a for a traceable calibration. Use step 2b for calibrations that do not need traceability to the National Bureau of Standards. Step 2b will provide similar results as step 2a, but without the added expense of probing tees.

2a. 1) Connect sweep oscillator's RF output to a Tee through a N type (m) to M type (m) adapter.

2) Connect HP 54003A's BNC input to Tee with a 48-inch BNC cable and a N type (m) to BNC (f) adapter.

3) Connect 50 Ω load, to Tee.

2b. Connect sweep oscillator's RF output to HP 54003A's BNC input with a 48-inch BNC cable through an N type (m) to BNC (f) adapter.

3. Adjust sweep oscillator output level until displayed signal just fills 8 divisions vertically. (Use the Clear Display key to help see this.)

4. Adjust sweep oscillator time vernier until displayed waveform is 10 divisions in length.

5. Change oscilloscope DISPLAY time to Infinite.

6. Press ***Clear Display*** key.

7. The Delta V markers show the 3 dB points and each horizontal division represents approximately 50 MHz. The sweep oscillator CW MARKER will show up as a dark line as the display area fills up. The waveform amplitude at the CW marker should be greater than the amplitude of the waveform at the Delta V markers.

8. The approximate frequency where the waveform's amplitude crosses the Delta V markers should be ≥300 MHz.

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7C-17. DC VOLTAGE MEASUREMENT ACCURACY VERIFICATION.

Equipment Setup:

1. Connect HP 54003A with HP 54003-61617 to oscilloscope's channel 1 input.

2. Turn oscilloscope on.

3. Adjust dc power supply output to exactly 300 mV (use a DVM to measure output level).

NOTE

Use step 4a for a traceable calibration. Use step 4b for normal calibrations that do not need traceability to the National Bureau of Standards.

4a. 1) Connect GR874 to N type (f) adapter to probing Tee.

2) Connect 50 Ω load to adapter.

3) Remove black insulating sleeve on probe tip.

4) Connect probe tip adapter to probing Tee.

5) Insert probe tip of HP 54003-61617 into adapter.

6) Connect entire assembly to dc source's output.

4b. 1) Connect HP 54001-61617 probe tip to dc source's output, through a GR874 to BNC (f), a BNC to probe tip adapter, and a 50 Ω load.

5. Adjust oscilloscope for the following setup:

Split Screen	Off
Display Averages	32
Probe Attenuation	10:1
Trig Mode	Edge
Trig Source	Chan. 1
Trig Level	+300 mV
Trig Slope	Pos
Holdoff	70 ns
Sweep speed	1 ms/div
Auto Triggered	
Delay	0
Delay Ref.	Center
Chan Sensitivity	100 mV/div
Chan Offset	0
Channel not in use	Off

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Procedure:

1. Measure input signal's voltage level using Delta V markers as follows:
   (Be sure to let 32 acquisitions occur)
   a. Press ***Delta V*** and turn markers on.
   b. Press ***Auto-Top-Base*** followed by ***50%-50%***.
   c. The Delta V markers should be within 202 mV and 398 mV.
2. Change oscilloscope's offset to +300 mV.
3. Measure input signal's voltage level using procedure in step 1 above.
4. The Delta V markers should be within 244 mV and 356 mV.
5. a. Change dc supply to -300 mV (verify with DVM).
   b. Change trigger level to -300 mV.
   c. Change oscilloscope offset to 0V.
6. Measure input signal's voltage level using Delta V markers as follows:
   (Be sure to let 32 acquisitions occur)
   a. Press ***Delta V*** and turn markers on.
   b. Press ***Auto-Top-Base*** followed by ***50%-50%***.
   c. The Delta V markers should be within -202 mV and -398 mV.
7. Change oscilloscope's offset to -300 mV.
8. Measure input signal's voltage level using procedure in step 1 above.
9. The Delta V markers should be within -244 mV and -356 mV.
10. To test the HP 54003A by itself, repeat the procedure starting with the equipment setup.
    Except, for non-traceable calibrations, do not use the 1250-1454 to connect pod to generator with a 48-inch BNC cable.
    For traceable calibrations, use setup on page 7C-19, step 4A, to connect pod to generator.

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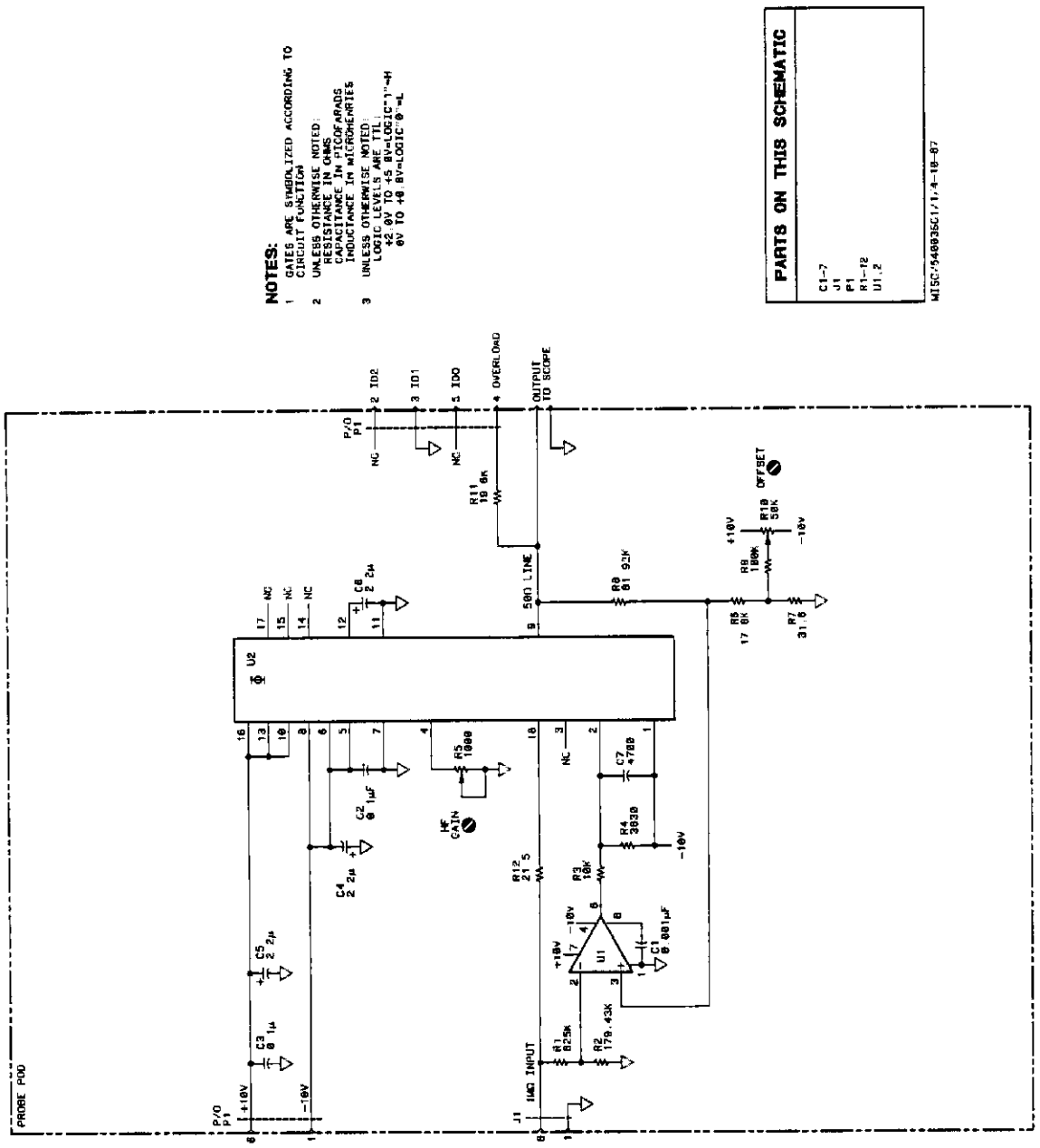


Figure 7C-7. Schematic diagram for HP 54003A Active Probe.

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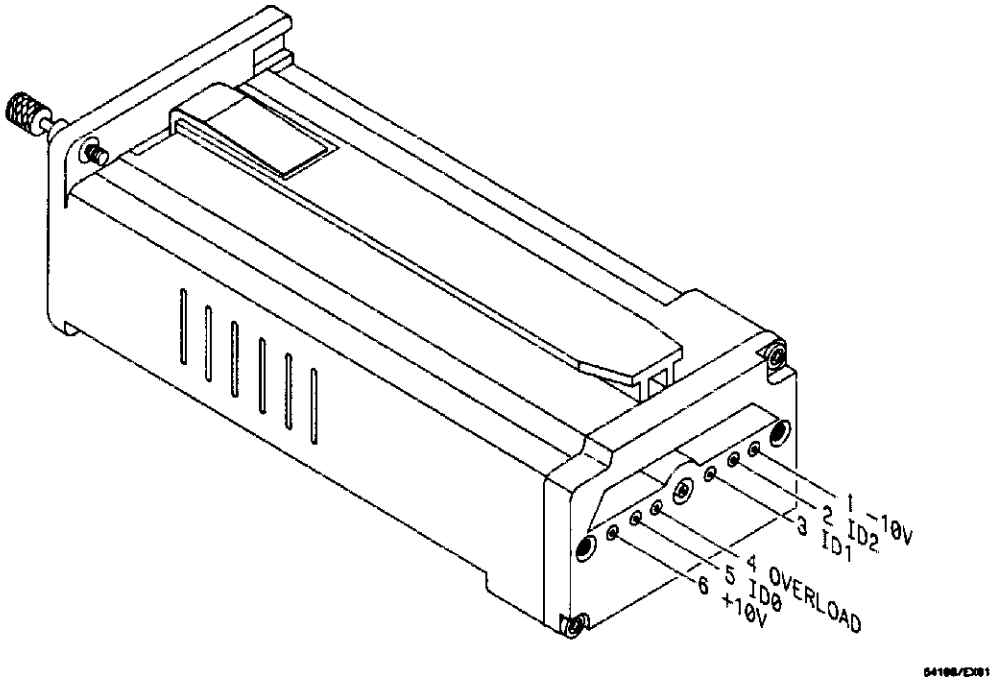


Figure 7A-8. Rear view of pod depicting pinout.

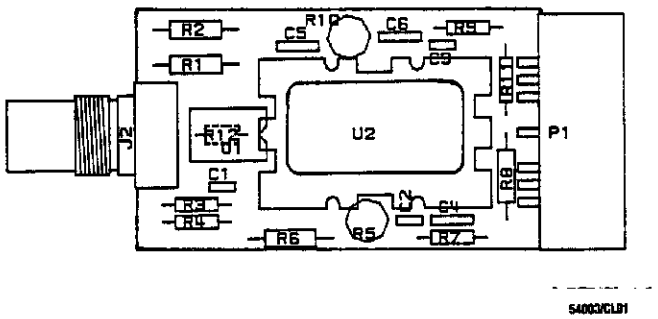


Figure 7C-9. Component locator for HP 54003A Active Probe.

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NOTE

The HP 54003A with the 54003-61617 performance verification is sufficient for most applications. The HP 54003A should only have a separate performance verification if there is a special requirement.

Table 7C-9. Performance Test Record

HEWLETT-PACKARD

Probe Model No._____

Probe Description _____

Oscilloscope Model Used _____

Oscilloscope Serial Number _____

Tested by _____

Test Date _____

Work Order No. _____

Relative Humidity_____

Temperature____Degrees___

Next Recommended Calibration Date _____

Paragraph Number	Test	With 54003-61617 Results	Without 54003-61617 Results
7C-12	Risetime step 3 Specification: Less than 1.2 ns	Minimum -- none Actual _____ns Maximum -- 1.2 ns	Minimum -- none Actual _____ns Maximum -- 1.2 ns
7C-16	Bandwidth step 8 Specification: dc to 300 MHz	Minimum -- 300 MHz Actual _____ MHz Maximum -- none	Minimum -- 300 MHz Actual _____ MHz Maximum -- none
7C-17	step 1c DC Voltage Accuracy Specification: See note below	Minimum -- 202 mV Actual_____ mV Maximum -- 398 mV	Minimum -- 202 mV Actual_____ mV Maximum -- 398 mV
	step 4	Minimum -- 244 mV Actual_____ mV Maximum -- 356 mV	Minimum 244 mV Actual_____ mV Maximum 356 mV
	step 6c	Minimum -- -202 mV Actual_____ mV Maximum -- -398 mV	Minimum -- -202 mV Actual_____ mV Maximum -- -398 mV
	step 9	Minimum -- -244 mV Actual_____ mV Maximum -- -356 mV	Minimum -244 mV Actual_____ mV Maximum -356 mV

NOTE: Specification for DC Voltage Accuracy. ±2% of Offset
±6% of Fullscale
±50 mV

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HEWLETT PACKARD

OPERATING AND PROGRAMMING MANUAL

MODEL 54110D
COLOR
DIGITIZING OSCILLOSCOPE

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Microfiche Part No. 54110-90801

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SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual, must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

This apparatus has been designed and tested in accordance with IEC publication 348, safety requirements for electronic measuring apparatus, and has been supplied in a safe condition. This manual contains some information and warnings which have to be followed by the user to ensure safe operation and to retain the apparatus in safe condition.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

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SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition note the instrument's external markings which are described under "Safety Symbols".

WARNING

- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS

Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.

Indicates hazardous voltages.

Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

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SECTION 1
WHEN YOU RECEIVE YOUR INSTRUMENT

1-1. INTRODUCTION

This Operating and Programming Manual contains information required to install, operate and program the Hewlett-Packard Model 54110D Color Digitizing Oscilloscope Paragraph 1-3 lists the accessories supplied with the instrument. Section 1 covers instrument safety, identification, options, accessories, receiving information and other basic data. Section 2 provides guidelines for using this manual.

1-2. SAFETY CONSIDERATION

The Hewlett-Packard Model 54110D is a Safety Class 1 instrument (instrument with an exposed metal chassis that is directly connected to earth via the power supply cable.)

WARNING

Before you apply power to the unit make sure you review this manual and become familiar with the definitions of the safety markings and pertinent instructions. These must be followed to insure safe operation and that the instrument is maintained in a safe condition.

1-3. ACCESSORIES SUPPLIED WITH THE 54110D

The 54110D Color Digitizing Oscilloscope is supplied complete with the following accessories;

Four 54002A input pods

One power cable

One Operating and Programming Manual and one Service Manual.

1-4. ACCESSORIES AVAILABLE

The following accessories are available for the 54110D.

54001A 10 MΩ, 1 GHz Miniature Active Probe with an attached 1.5M cable. (see figure 1-1)

54003A 1 MΩ 300 MHz, 10:1 probe.

11536A 50 Ohm Probing Tee Used to minimize disturbance of transmission characteristics. Compatible with the 54001A high bandwidth probe (see above). Requires one 54051A probe adapter (see below).

10211A (24 pin) and 10024A (16 pin) Test Clips.

54001-23203 probe adapter. Adapts the 54001A (see above) mini-probe tip (or other HP mini-probes) to the probing accessories included in the 10020A resistive divider probe kit, and to the 11536A probing tee.

10240B BNC Blocking Capacitor. Used to ac couple signals to 54110D's inputs.

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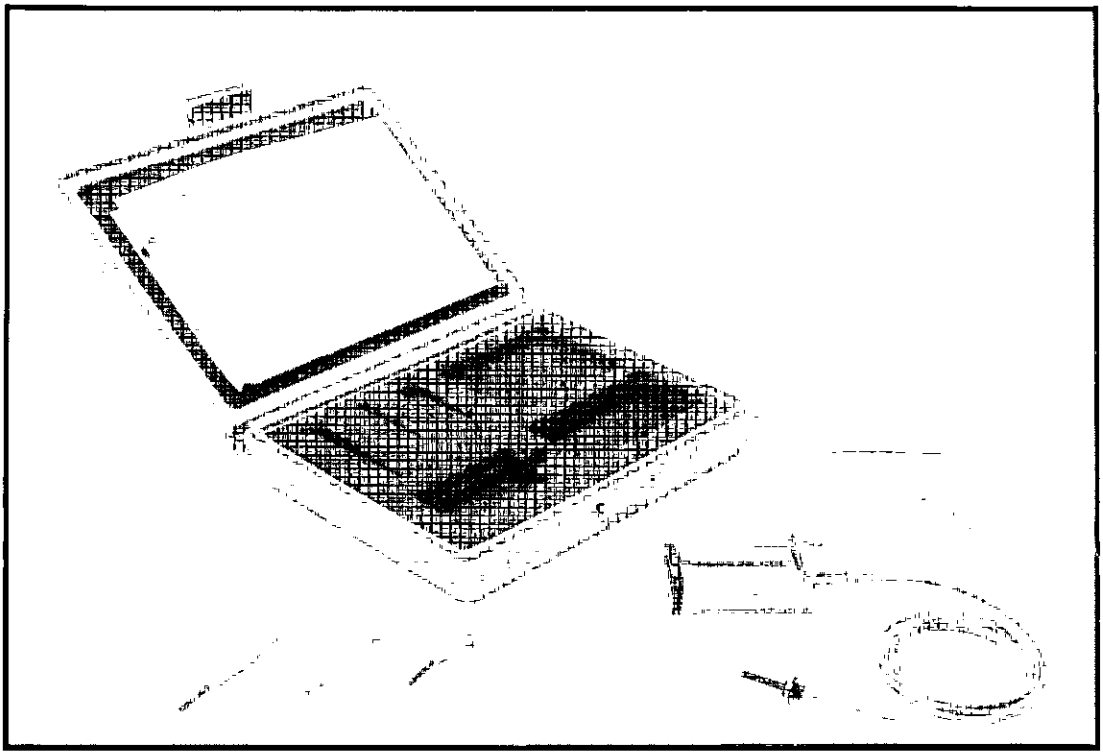


Figure 1-1. 54001A 1 GHz Miniature Active Probe

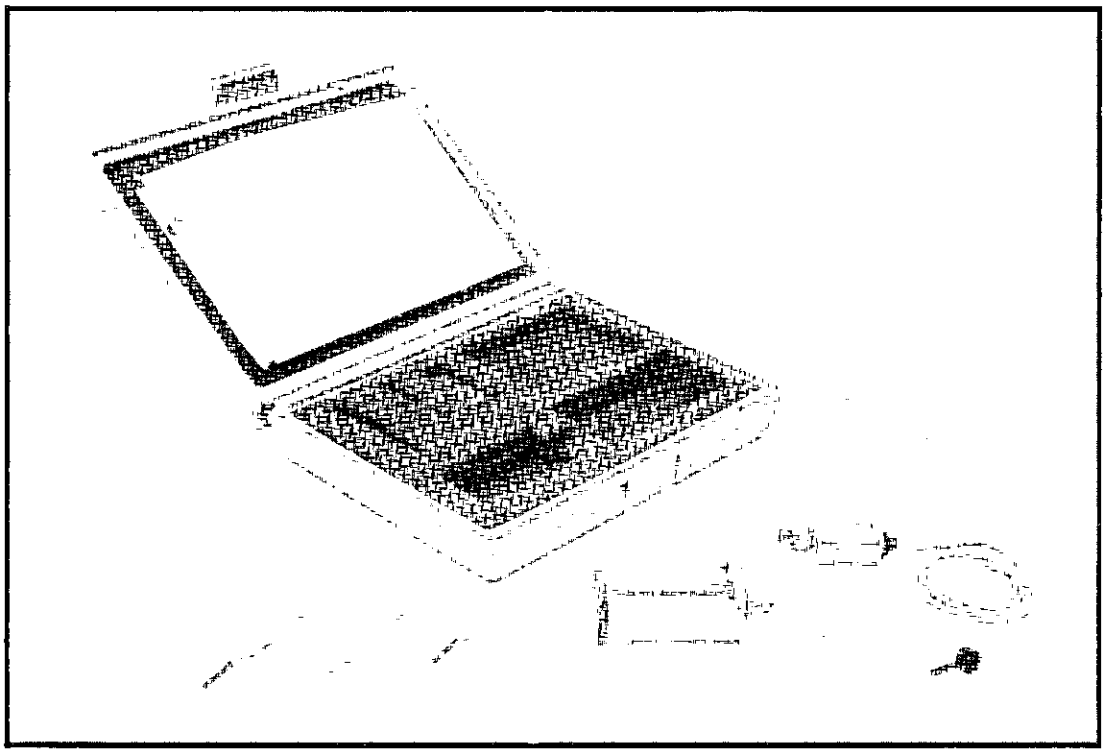


Figure 1-2. 54003A 1 MΩ 300 MHz with 10:1 Probe

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1-5. OPTIONS

The 54110D Color Digitizing Oscilloscope has two options available:

Option 908 provides rack ears and associated mounting hardware for rack mounting the 54110D. The HP part number is 5061-9679.

Option 910 provides an additional Operating and Programming Manual for the 54110D. The HP part number is 54110-90901.

1-6. POWER CABLE

WARNING

Before energizing this unit you must insure that the chassis of the instrument is properly grounded. This precaution is to avoid the possibility of injury or death which may result if the protective ground is defeated.

The 54110D is provided with a 3 wire power cable. When this cable is connected to an appropriate AC power receptacle it provides a ground for the instrument cabinet. The type of power cable shipped with each instrument depends on the country of destination. See table 1-1 for power cable description and applications

1-7. INITIAL INSPECTION

WARNING

To avoid hazardous electrical shock, do not perform electrical tests when there are signs of shipping damage to any portion of the instrument.

Inspect the shipping container for damage. If the shipping container or packaging materials are damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as listed in Paragraph 1-3. If the contents are incomplete, or if there is mechanical damage or defect, notify the nearest Hewlett-Packard office. If either the shipping container is damaged or the packaging material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection. The HP office will arrange for repair or replacement without waiting for claim settlement.

1-8. CLAIMS FOR DAMAGE

If physical damage is evident or if the instrument does not meet specifications when received, notify the carrier and the nearest Hewlett-Packard Sales/Service Office. The sales/service office will arrange for repair or replacement of the unit without waiting for settlement of the claim against the carrier.

1-9. STORAGE AND SHIPMENT

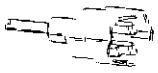
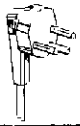
The 54110D Color Digitizing Oscilloscope may be stored and shipped in environments that do not exceed the following limits:

Temperature ..... -40°C to+75°C
Humidity ..... <95% relative
Altitude ..... <15,300 metres (50,000 feet)

This instrument should also be protected from temperature extremes that would cause condensation in the instrument

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Table 1-1. AC Power Cables

PLUG TYPE	CABLE PART NO.	PLUG DESCRIPTION	LENGTH IN/CM	COLOR	COUNTRY
OPT 900 250V 	8120-1351 8120-1703	Straight *BS1363A 90°	90 228 90 228	Gray Mint Gray	United Kingdom, Cyprus Nigeria, Zimbabwe Singapore
OPT 901 250V 	8120-1369 8120-0696	Straight *NZSS198 ASC 90°	79 200 87 221	Gray Mint Gray	Australia, New Zealand
OPT 902 250V 	8120-1689 8120-1692 8120-2857	Straight *CEE7-Y11 90° Straight (Shielded)	79 200 79 200 79 200	Mint Gray Mint Gray Coco Brown	East and West Europe, Saudi Arabia, So Africa, India (Unpolarized in many nations)
OPT 903 125V 	8120-1378 8120-1521 8120-1992	Straight *NEMA5-15P 90° Straight (Medical UL544	90 228 90 228 96 244	Jade Gray Jade Gray Black	United States Canada Japan (100V or 200V), Mexico, Philippines Taiwan
OPT 904 250V 	8120-0698	Straight *NEMA6-15P	90 229	Black	United States Canada
OPT 905 250V 	8120-1396 8120-1625	CEE22-V1 (Systems Cabinet use) 250V	30 76 96 244	Black Black	
OPT 906 250V 	8120-2104 8120-2296	Straight *SEV1011 1959-24507 Type 12 90°	79 200 79 200	Mint Gray Mint Gray	Switzerland
OPT 912 220V 	8120-2956 8120-2957	Straight *DHCK107 90°	79 200 79 200	Mint Gray Mint Gray	Denmark

**Part number shown for plug is industry identifier for plug only. Number shown for cable is HP Part no. for complete cable including plug.* E=Earth Ground, L=line , N=Neutral

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1-10. PACKAGING

Original packaging i.e , the containers and materials identical to those used in factory packaging are available from Hewlett-Packard. If the unit is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of servicing required, return address, model number, and full serial number. Mark the container FRAGILE In any correspondence refer to the instrument by model number and full serial number.

If other packaging is to be used the following general instructions for repackaging with commercially available materials should be followed;

a Wrap the instrument in heavy paper or plastic. If you are shipping the unit to a Hewlett-Packard office or service center be sure to attach a tag to the instrument indicating the type of service required, return address, model number and full serial number

b. Use a strong shipping container. A double wall carton made of 2.4MPa (350psi) test material is adequate.

c Use a layer of shock absorbing material 75 to 100mm (3 to 4 inches) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect the control panel with cardboard

d. Seal the shipping container securely.

e. Mark the shipping container FRAGILE to insure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

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SECTION 2
HOW TO USE THIS MANUAL

2-1. INTRODUCTION

This Operating and Programming Manual has been designed as both a tutorial operating manual and a reference manual for writing programs to operate the oscilloscope remotely

The first four sections of the manual are concerned with instrument specifications, receiving information and operating environment information for the 54110D.

The next four sections (5 through 8) of the manual are concerned with front panel exercises. Sections 9-11 are dedicated to the remote programming of the HP-IB interface.

Here is an overview of what this manual contains:

WHEN YOU RECEIVE YOUR INSTRUMENT, SECTION 1

This section includes installation information, receiving information, warranty data and much more. You should read Section 1 before initial installation and operation.

MEET THE 54110D COLOR DIGITIZING OSCILLOSCOPE, SECTION 3

This section provides a description of this oscilloscope and complete specifications and operating characteristics. This section also includes a probe selection table.

GETTING READY TO USE THE 54110D, SECTION 4

This section contains important data about the required operating environment and power requirements for the 54110D. You should review this section prior to initial operation.

GETTING STARTED WITH THE FRONT PANEL, SECTION 5

This section introduces you to the front panel layout and it's four functional areas. Section 5 provides vital information for the first time user.

FAMILIARIZE YOURSELF WITH THE MENUS, SECTION 6

Many of the front panel controls on the 54110D are multi-functioned. To better understand these controls this section defines all front panel functions and maps the different function groups. This section also introduces you to the color features of this instrument. This section is formatted so that it can be used as a reference by operators, regardless of skill level.

FRONT PANEL EXCERCISES, SECTION 7

This section provides step-by-step exercises that will help you become more familiar with making measurements from the front panel of the 54110D. Section 7 builds on the information presented in Section 6.

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MAKING A HARDCOPY, SECTION 8

This section provides information concerning the use of graphics printers and plotters with the 54110D via HP-IB. This section also provides a list of Hewlett-Packard printers and plotters that are compatible with this instrument.

REMOTE OPERATION, SECTION 9

This section discusses the remote operation of the instrument over the HP-IB. Such topics as HP-IB compatibility, remote/local modes, local lockout, learn and cal strings are dealt with. Review this section before writing programs for the instrument

COMMAND SET OVERVIEW, SECTION 10

This section contains the instruction set, notation conventions and definitions, syntax diagrams and other detailed programming reference information for the 54110D.

APPENDIX A

Appendix A contains example programs for the 54110D using the HP 200 series scientific computer using the HP Basic 4 0 operating system.

APPENDIX B

Appendix B provides the advanced user with a discussion of the channel-to-channel timing skew and trigger delay calibration concerns when using the 54110D.

APPENDIX C

Appendix C provides the advanced user detailed information concerning the automated measurements that the 54110D can perform. This appendix discusses such topics as measurement throughput, accuracy, and resolution.

The following table indicates those chapters which are recommended reading for various types of 54110D users You may fall into more than one category. For example, you may be an inexperienced programmer who installs the 54110D.

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Table 2-1. User Table

	Chapters										Appendix		
Reader/User	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**A**	**B**	**C**
Installation Personnel	•	•		•									
First Time User (Front Panel)			•	•	•	•		•					
Advanced User (Front Panel)						•	•	•				•	•
Beginning Programmer			•	•	•	•	•		•				
Advanced Programmer										•	•		

NOTES:

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SECTION 3
SPECIFICATIONS AND SUPPLEMENTAL CHARACTERISTICS

3-1. INTRODUCTION

This section of the manual contains a list of specifications for reference and performance verification. These specifications are listed in Table 3-1. Also included in section three are the supplemental characteristics. Supplemental characteristics are not specifications but are typical parameters and are included in this manual as additional information for the user. Supplemental characteristics are listed in Table 3-2.

NOTES:

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Table 3-1. Specifications

VERTICAL (Voltage)

Bandwidth (-3dB):[1]

with HP 54002A: dc to 1 GHz
with HP 54001A: dc to 700 Mhz[3]
with HP 54003A: dc to 300 Mhz[3]

Transition Time (10% to 90%):[1]

with HP 54002A: ≤350 ps
with HP 54001A: ≤450 ps[3]
with HP 54003A: ≤1.2 ns[3]

Deflection Factor (full-scale = 8 divisions):

with HP 54002A: 10 mV/div to 1 V/div in 1-2-5 steps
with HP 54001A: 100 mV/div to 10 V/div in 1-2-5 steps[3]
with HP 54003A: 100 mV/div to 10 V/div in 1-2-5 steps[3]

DC Accuracy, Single Voltage Marker:

with HP 54002A: ±3% of full-scale ±2% of offset[2]
with HP 54001A: ±6% of full-scale ±2% of offset ±50 mV[3]
with HP 54003A: ±6% of full-scale ±2% of offset ±50 mV[3]

DC Delta Voltage Accuracy (Two Markers On Same Channel):

with HP 54002A: ±1% of full-scale ±3% of reading[2]
with HP 54001A: ±1% of full-scale ±6% of reading[3]
with HP 54003A: ±1% of full-scale ±6% of reading[3]

DC Offset:

RANGE: ±1.5 x full-scale (referenced to center screen)

ADJUSTMENT RESOLUTION: adjustable in steps of 0.0025 x full-scale

Dynamic Range: deflection factor and offset should be scaled so that the unmagnified signal remains within the the full-scale display range.

Magnifier: expands displayed signal vertically from 1 to 16 times; adjustable in 0.5% steps.

Inputs: two inputs, configurable with HP 54000-series pods.

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Table 3-1. Specifications (Continued)

HORIZONTAL (Time)

Deflection Factor (full-scale = 10 divisions): 100 ps/div to 1 s/div

ADJUSTMENT RESOLUTION: adjustable in 1-2-5 steps via knob and step keys. Adjustable to three significant figures via keypad or HP-IB command.

Delay (Time Offset):

PRE-TRIGGER RANGE: up to -200 ms or -10 divisions, whichever is greater.
POST-TRIGGER RANGE: up to +1 second or +600,000 divisions, whichever is greater.
ADJUSTMENT RESOLUTION: adjustable in steps of 10 ps or 10^{-6} x delay setting, whichever is greater.

Time Base Accuracy: error is:

SINGLE-CHANNEL: ≤(100 ps ±2 x 10^{-5} x delta T reading)

DUAL-CHANNEL: ≤(200 ps ±2 x 10^{-5} x delta T reading)

TRIGGER

Trigger Source	Vertical Channel 1 or 2		
Input Pod	HP 54002A	HP 54001A	HP 54003A[3]
Trigger Level Range	±2 x full-scale		
Trigger Level Adjustment Resolution	0.0025 x full-scale		
Trigger Sensitivity DC to 100 MHz	0.12 x full-scale		
Above 100 Mhz (frequency range)	0.24 x full-scale (100 MHz to 500 MHz)		0.24 x full-scale (100 Mhz to 300 Mhz)
Pulse width > 1 ns	0.24 x full-scale		

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Table 3-1. Specifications (Continued)

TRIGGER (Continued)

Trigger Source	Trigger Input 3 or 4		
Input Pod	HP 54002A	HP 54001A	HP 54003A[3]
Trigger Level Range	±2 V	±20 V	
Trigger Level Adjustment Resolution	2 mV	20 mV	
Trigger Sensitivity DC to 100 MHz	40 mV	400 mV	
Above 100 Mhz (frequency range)	80 mV (100 MHz to 500 MHz)	800 mV (100 MHz to 500 MHz)	800 Mv (100 MHz to (300 Mhz)
Pulse width > 1 ns	80 mV	800 mV	

RMS Jitter: ≤(50 ps + 5 x 10^{-7} x delay setting)

Trigger Source: channel 1, channel 2, trigger 3, trigger 4. Independent trigger level and polarity settings on all sources. Edge trigger on any source. Logical pattern trigger on all sources.

Trigger 3 and 4 Input: configurable with HP 54000-series pods.

INPUTS

	HP 54002A 50Ω Input	HP 54001A 1 GHz Miniature Active Probe	HP 54003A 1 MΩ Input, With 10:1 Probe Attached	HP 54003A 1 MΩ Input, With 10:1 Probe Removed
Maximum Input Voltage	5 V rms	20 V peak	20 V peak	2 V peak

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Table 3-1. Specifications (Continued)

INPUTS (Continued)

	HP 54002A 50Ω Input	HP 54001A 1 GHz Miniature Active Probe	HP 54003A 1 MΩ Input, With 10:1 Probe Attached	HP 54003A 1 MΩ Input, With 10:1 Probe Removed
Coupling	dc	dc	dc	dc
Input Capacitance (Nominal)	N/A	2 pF	8 pF	10 pF
Input Resistance (Nominal)	50Ω	10 kΩ	1 MΩ	1 MΩ
Bandwidth * (-3dB)	dc to 1 GHz	dc to 1 GHz	dc to 300 MHz	dc to 300 MHz
Transition Time * (10% to 90%)	≤350 ps	≤350 ps	≤1.2 ns	≤1.2 ns
Division Ratio *	1:1	10:1±3%	10:1±3%	1:1±1%

CATHODE-RAY TUBE

X-RAY EMISSION: CRT emission <0.1 mR/hr; not measurable in background noise using Victoreen Model 440RF/C.

NOTES:

1. These specifications apply over ambient temperature range of +15°C to +35°C.
2. When driven from a 50Ω source.
3. With the 10:1 divider probe supplied with the 54003A.

* Refer to VERTICAL and TRIGGER specifications for system performance specifications.

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Table 3-2. Supplemental Characteristics

DIGITIZER

Resolution: 7 bits (1 part in 128). Effective resolution can be extended up to approximately 10 bits by using magnification and averaging.

Digitizing Rate: up to 40 megasamples/second.

VERTICAL

Input Protection: a relay opens when applied voltage exceeds rated input voltage for input pod in use (see Specifications).

HORIZONTAL

Delay Between Channels: difference in delay between channels can be nulled out in 10 ps steps up to 10 ns to compensate for differences in input cables or probe length.

Reference Location: the reference point can be located at the left edge, center, or right edge of the display. The reference point is that point where the time is offset from the trigger by the delay time.

TRIGGER

Input Protection: a message appears on the display when the applied voltage exceeds rated input voltage for input pod in use (see Specifications).

Holdoff

HOLDOFF-BY-EVENTS: range of events counter is from 2 to 67 million events. Maximum counting rate is 80 MHz. An event is defined as anything that satisfies the triggering conditions selected.

HOLDOFF-BY-TIME: adjustable in 10 ns steps from 70 ns to 670 ms.

Trigger Modes

EDGE TRIGGER: on any source (see Specifications, Trigger Source).

PATTERN TRIGGER: a pattern can be specified for all sources. Each source can be specified as high, low, or don't care.
Trigger can occur on the last edge to enter the specified pattern or the first edge to exit the specified pattern.

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Table 3-2. Supplemental Characteristics (Continued)

Trigger Modes (Continued)

TIME QUALIFIED PATTERN TRIGGER: trigger occurs on the first edge to exit the specified pattern, only if the pattern was present for less than [greater than] the specified time. Filter time is adjustable from 10 ns to 5 seconds. Filter recovery time is ≤8 ns. In the "Pattern present <[time]" mode, the pattern must be present ≥1 ns for the trigger to respond.

STATE TRIGGER: a pattern can be specified for any three sources. Trigger can be set to occur on an edge of either polarity on the source specified as the clock (not one of the pattern sources) when the pattern is present or not present. Setup time for the pattern to be present prior to the clock edge is <4 ns; hold time is zero.

Delayed Trigger

EVENTS-DELAYED MODE: the trigger can be armed by an edge on any source, then triggered by the *n*th edge on any other source.

The number of events, *n*, can be set from 1 to 10^8-1. Maximum event counting rate is 150 MHz.

TIME-DELAYED MODE: the trigger can be armed by an edge on any source, then triggered by the first edge on any other source after a specified time has elapsed. The delay time can be set from 20 ns to 5 seconds.

DISPLAY

Data Display Resolution: 501 points horizontally (full-scale) by 256 points vertically.

Data Display Formats

SPLIT SCREEN: each channel display is four divisions high.

FULL SCREEN: the two channels are overlaid. Each channel display is eight divisions high.

Display Modes

VARIABLE PERSISTENCE: the time that each data point is retained on the display can be varied from 200 ms to 10 seconds, or it can be displayed indefinitely.

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Table 3-2. Supplemental Characteristics (Continued)

Display Modes (Continued)

AVERAGING: the number of averages can be varied from 1 to 2048 in powers of 2. On each acquisition, *1/n* times the new data is is added to *(n-1)/n* of the previous value at each time coordinate. Averaging operates continuously; the average does not stop after *n* acquisitions.

GRATICULES: Full grid, axes with tic marks, or frame with tic marks.

DISPLAY COLORS: a default color selection is setup in the instrument. Different colors are used for Display background, Channel 1/ Function 1, Channel 2/Function 2, background text, highlighted text, Advisories, Markers, overlapping waveforms and Memories. If desired, the colors used may be changed from the front panel or from HP-IB.

MEASUREMENT AIDS

Markers: dual voltage markers and dual time markers are available. Voltage markers can be assigned to either channel or to both channels, memories and functions.

Automatic Edge Finders: the time markers can be assigned automatically to any displayed edge of either polarity on a channel memory, or function or to any combination of the preceding. The voltage markers establish the threshold reference for the time markers in this mode.

Automatic Pulse Parameter Measurements: the following pulse parameter measurements can be performed automatically (as defined by IEEE standard 194-1977, "IEEE Standard Pulse Terms and Definitions").

Frequency	Top magnitude
Period	Base magnitude
Pulse duration	Preshoot
Rise time	Overshoot
Fall time	RMS volts
Pulse amplitude	Duty cycle

Waveform Math: two independent functions are provided for waveform math. The operators are **+, -, invert, versus** and **only.** Either of the two vertical channels or any of the four waveform memories can be used as operands for the waveform math. If turned on, Function 1 is displayed in lieu of Channel 1 and Function 2 is displayed in lieu of Channel 2.

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Table 3-2. Supplemental Characteristics (Continued)

SETUP AIDS

Presets: vertical deflection factor, offset, and trigger level can be preset independently on each channel for ECL or TTL levels.

Auto-Scale: pressing Auto-Scale causes vertical and horizontal deflection factors and the trigger source to be set for a display appropriate to the signals applied to the inputs. Requires a duty cycle >0.1%, frequency >50Hz, and amplitude >20 mV peak. Operative only for relatively stable input signals.

Save-Recall: ten front panel setups may be saved in non-volatile memory. If Auto-Scale is inadvertently pressed, pressing Recall followed by Auto-Scale, restores the instrument to the state prior to the last Auto-Scale executed.

Waveform Memories: four memories are provided for storage of waveforms. Only one waveform may be stored in each of these memories. These memories can be used as sources for either measurements or functions. Two additional memories are provided to store pictures. Each of these two waveform picture memories is a pixel map of the display. Any number of waveform pictures may be written into to each picture memory. Once stored, individual waveforms cannot be accessed from the picture memories. The display of any of the six memories can be turned on or off without affecting their contents. Waveforms in memory are displayed in a different color from live waveforms.

POWER REQUIREMENTS

Voltage: 115/230 V ac, -25% to +15%, 48-66 Hz.

Power: 350 watts maximum, 650 VA maximum.

DIMENSIONS

Refer to outline drawing.

WEIGHT

Net: approximately 25.5 kg (56 lb).

Shipping: approximately 30.5 kg (67 lb).

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Table 3-2. Supplemental Characteristics (Continued)

ENVIRONMENTAL CONDITIONS

Temperature

OPERATING: 0°C to +55°C (+32°F to +131°F).
Note: see Specification Note 1.

NON-OPERATING: -20°C to +75°C (-4°F to +167°F).

Humidity

OPERATING: up to 90% relative humidity at +40°C (+104°F).

NON-OPERATING: up to 95% relative humidity at +65°C (+149°F).

Altitude

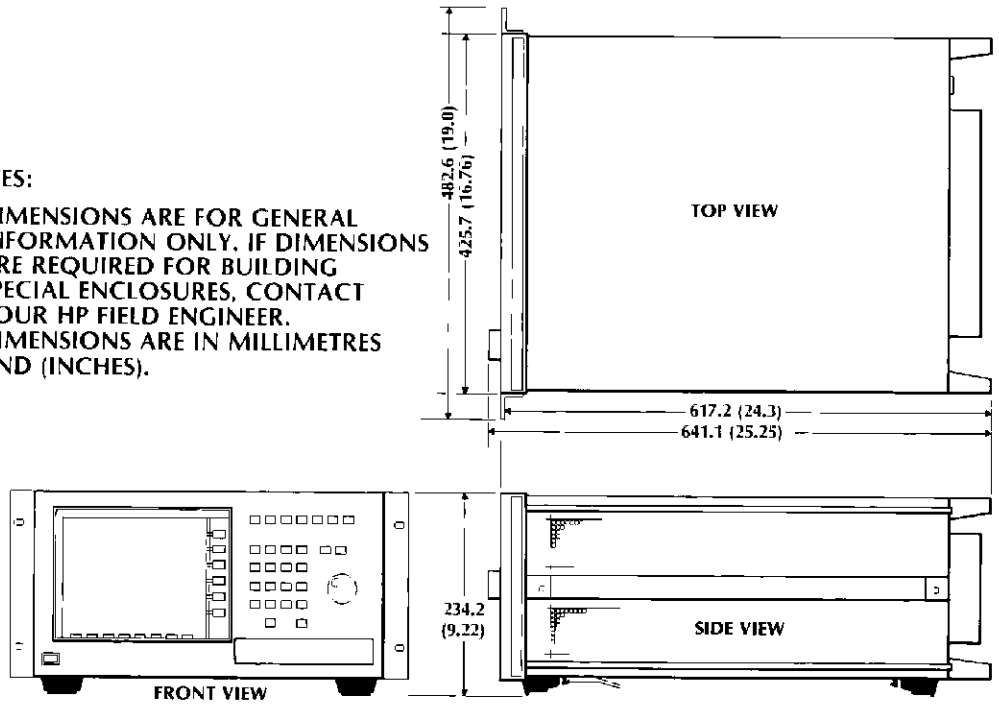
OPERATING: up to 4600 metres (15,000 ft).

NON-OPERATING: up to 15,300 metres (50,000 ft).

Vibration: Vibrated in three orthogonal axes for 15 minutes each axes; 0.38 mm (0.015 in.) peak-to-peak excursion; 5 to 55 Hz; 1 minute/octave sweep.

NOTES:

1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR HP FIELD ENGINEER.
2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).



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SECTION 4
GETTING READY TO USE THE HP 54110D

4-1. HP 54110D SPECIFICATIONS

This section provides information concerning the operating environment and the power requirements for the HP 54110D Color Digitizing Oscilloscope. It is important that the user provide the correct power source and operating environment for this instrument. Failure to do so can cause serious damage to the instrument and/or provide a health hazard to the user.

4-2. OPERATING ENVIRONMENT

CAUTION

Insure the instrument has adequate clearance on all surfaces to provide for sufficient air flow for cooling. Do not block any of the vent holes or the fan's air inlet.

The operating environment must be maintained within the following parameters:

Temperature ..... 0° C to 55° C
Humidity ..... <90% up to 40° C
Altitude ..... <4572 metres (15,000 feet)

This instrument should also be protected from temperature extremes that would cause condensation in the instrument.

4-3. POWER REQUIREMENTS

The 54110D requires a power source of 115 or 230 Vac +15/-25%; 48-66 Hertz single phase. Power consumption is 350 watts maximum or 650 VA maximum.

CAUTION

Before connecting this instrument to the AC power source, insure that the line select switch on the rear panel of the instrument is set to the appropriate position (see figure 4-1).

A blade-type screwdriver may be used to change the position of this switch. Figure 4-2 shows the line select switch set for 115 Vac operation. If this switch is not set correctly, serious damage to the instrument is likely.

Once the correct setting on the line select switch has been made and the appropriate power cord has been installed and connected to the mains, the unit can be turned on (see paragraph 4-4). By selecting the appropriate line voltage with the line select switch, you are also determining the correct circuit breaker trip current. If 115 Vac line voltage is selected, the circuit breaker trip current will be 5 amps. If 230 Vac line voltage is selected, the circuit breaker trip current will be 3 amps.

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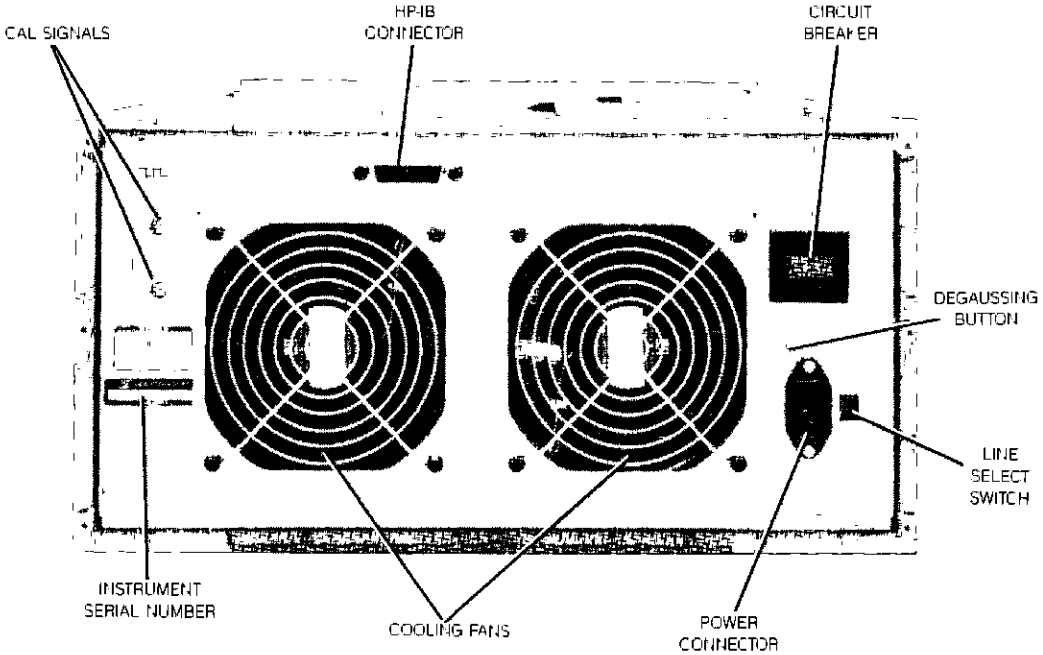


Figure 4-1 HP 54110D Rear Panel

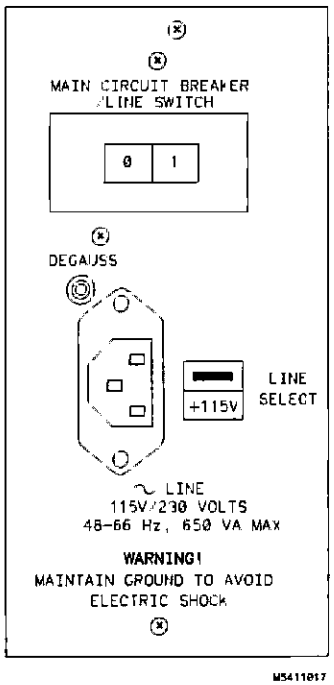


Figure 4-2. Power Module

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The 54110D has two switches that can interrupt the power for the instrument. The first is the line switch and the second is the mains breaker:

1. The line switch is located at the lower left of the front panel.

2. The mains breaker is located on the upper right hand corner of the rear panel (see figure 4-1).

If the front panel line switch is in the "STBY" position or if the mains breaker is in the OFF or "0" position, the unit will not function.

4-4. POWER CABLE

WARNING

Before energizing this unit you must insure that the chassis of the instrument is properly grounded. This precaution is to avoid the possibility of injury or death which may result if the protective ground is defeated.

The 54110D is provided with a 3-wired power cable When this cable is connected to an appropriate AC power receptacle, it provides a ground for the instrument cabinet. The type of power cable shipped with each instrument depends on the country of destination. See table 1-1 for power cable description and applications.

4-5. HP-IB ADDRESS SELECTION

HP-IB address can be read and selected from the front panel of the 54110D with the use of soft keys that are located at the right of the CRT (after pressing the Utility menu select key). In order to set or change the HP-IB address, put the 54110D into the TALK/LISTEN mode (soft key selectable), then input the desired address from the front panel. The 54110D supports the following HP-IB interface functions: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP0, DC1, DT1, C0, E1. For further information concerning the 54110D HP-IB, operation, see Section 9.

4-6. HP-IB INTERCONNECTIONS

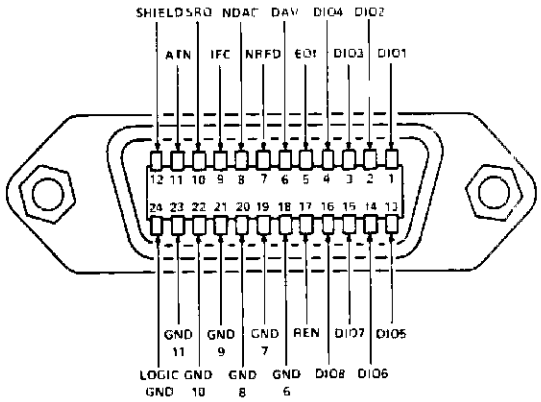
Interconnection data concerning the rear panel HP-IB connector is provided in figure 4-3. The HP-IB system allows the interconnection of up to 15 (including controller) HP-IB compatible instruments. The HP-IB cables have identical connectors on both ends so that several cables can be connected to a single source without special connectors or switch boxes. System components and devices may be connected in virtually any configuration (see figure 4-4).

4-7. INITIAL COLOR DISPLAY SETUP

The 54110D Color Digitizing Oscilloscope uses an electromagnetic color display and may require degaussing at installation or later if it becomes necessary. To facilitate this, the display section has a built in degaussing coil. The energizing switch for this coil is located on the rear panel on the power panel. (See figure 4-2) To degauss the CRT press this switch several times.

If, in certain severe situations, internal degaussing is not adequate it may be necessary to use an external television type degaussing coil. On the front panel left of the CRT are two screw driver adjust controls, Brightness and Background. The background control sets the luminosity of the background of the CRT. The brightness control sets the gain of the Z axis, that is, controls the intensity of the displayed information on the CRT. These two controls are usually adjusted to accommodate users taste and ambient light.

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Where: ATN = Attention
DAV = Data Valid
DIO 1-8 = Data Input-Output
EOI = End or Identify
IFC = Interface Clear
NDAC = Not Data Accepted
NRFD = Not Ready For Data
REN = Remote Enable
SRQ = Service Request

Logic Levels
The Hewlett-Packard Interface Bus Logic Levels are TTL compatible, i e., the true (1) state is 0 0 Vdc to +0 4 Vdc and the false (0) state is +2 5 Vdc to +5 0 Vdc.

Programming and Output Data Format
Refer to Section 9.

Mating Connector
HP 1251-0293, Amphenol 57-30240

Mating Cables Available
HP 10833A, 1 metre (3.3 ft)
HP 10833B, 2 metres (6 6 ft)
HP 10833C 4 metres (13 2 ft)
HP 10833D, 0.5 metres (1 6 ft)

Cabling Restrictions

1. A Hewlett-Packard Interface Bus system may contain no more than 2 metres (6 ft) of connecting cable per instrument
2. The maximum accumulative length of connecting cable for any Hewlett-Packard Interface Bus system is 20.0 metres (65 6 ft)

Figure 4-3. HP-IB Interface Connector

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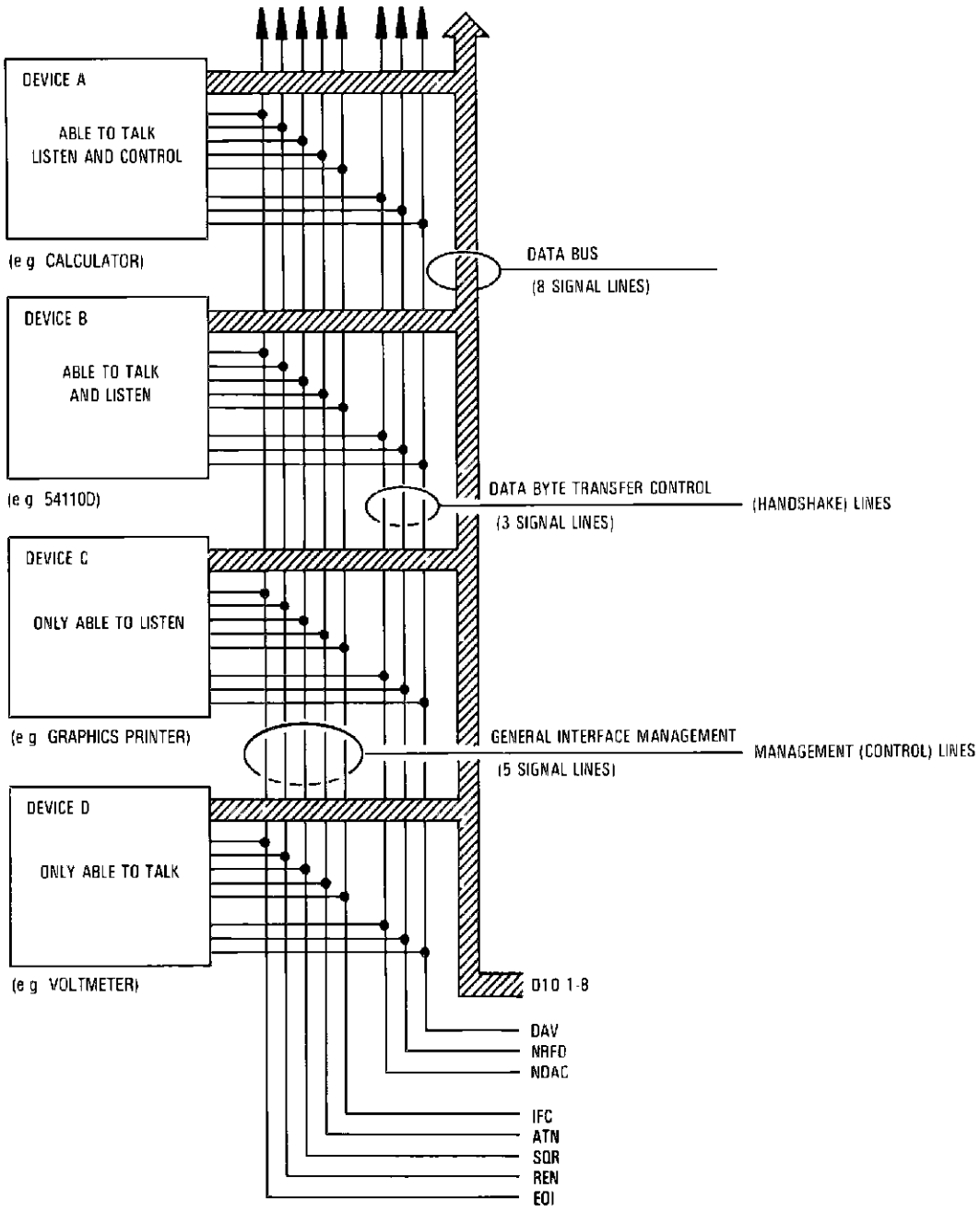


Figure 4-4. HP-IB Interface

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SECTION 5
FRONT PANEL

5-1. GETTING STARTED WITH THE FRONT PANEL

This section describes the front panel of the 54110D and discusses its four functional areas. The four functional areas of the front panel of the 54110D Color Digitizing Oscilloscope include:

A. System Control
B. Entry
C. Menu Selection
D. Function

These four groups of keys give the operator complete local control of the instrument. (See Figure 5-1.)

5-2. SYSTEM CONTROL

The SYSTEM CONTROL keys are located on the top right-hand side of the front panel directly under the label, "SYSTEM CONTROL"

The SYSTEM CONTROL keys provide control of acquisition, the dynamic display, SAVE/RECALL registers and automatic display scaling.

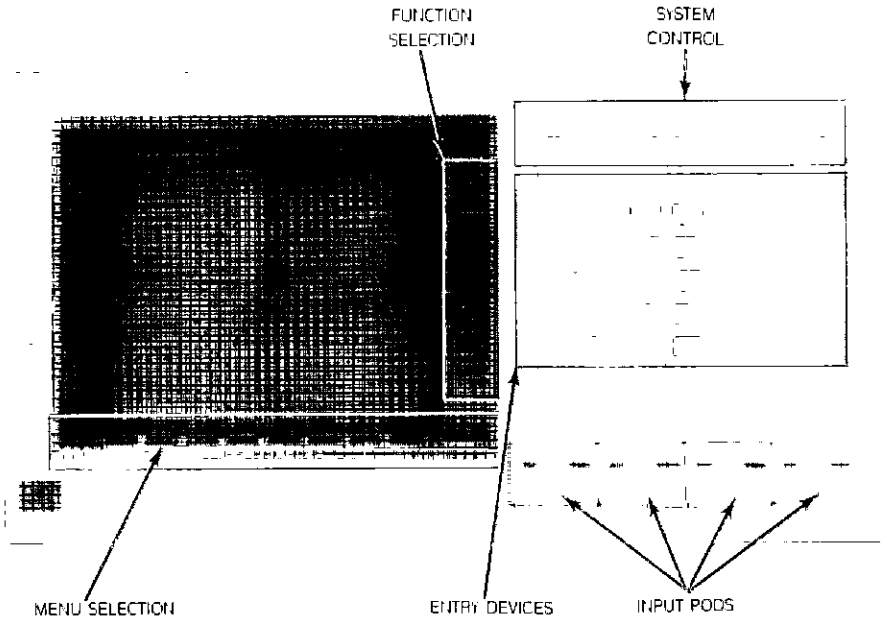


Figure 5-1. 54110D Front Panel

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The CLEAR DISPLAY key erases the dynamic (active) display. This key will not erase a waveform in memory that is being displayed. When the CLEAR DISPLAY key is pressed the instrument will momentarily stop acquiring data, erase the screen and then resume acquiring data. If the STOP/SINGLE key has previously been pressed, the CLEAR DISPLAY key will erase the displayed waveform and acquisition will not resume unless the RUN key is pressed, or if a single acquisition is desired the STOP/SINGLE key can be pressed for the second time. If you are acquiring a large number of averages and you change the input signal you can quickly reset the average registers by pressing the CLEAR DISPLAY key. This will save the time that the display would normally take to integrate to the new signal levels.

The RUN key causes the 54110D to resume acquiring data after acquisition has been stopped by the STOP/SINGLE key. When the STOP/SINGLE key is pressed the instrument will stop acquiring data and display, indefinitely, the last data that was acquired. Each subsequent STOP/SINGLE key press arms the instrument to make a single acquisition that would be started by the next trigger event. To return to the previous operating mode press the RUN key. When the STOP/SINGLE key has been pressed the SEC/DIV, VOLTS/DIV and other front panel controls that would normally cause the displayed waveform to change will erase the active display as if the CLEAR DISPLAY key had been pressed.

5-3. SAVE/RECALL

This instrument allows the user to SAVE and RECALL up to ten different front panel setups in nonvolatile memory.

To SAVE the current front panel setup in one of the ten SAVE/RECALL registers, press SAVE, then press the number (0-9) of the register desired. All front panel functions, modes and Cal factors, menu selection and input device assignments are not saved. SAVE/RECALL will not cause execution of measurements, edge finders, "Start Print", or other action keys.

To RECALL a previously saved front panel setup press RECALL, then press the number (0-9) of the desired register.

To return to the condition that existed prior to the last AUTO-SCALE, press RECALL then press AUTO-SCALE. This feature allows you to recover if the AUTO-SCALE is accidentally pressed.

5-4. LOCAL

When the LOCAL key is pressed an RTL (return to local) message is sent to the HP-IB interface and the unit will return to local (front panel) control if it had previously been in remote operation and if the HP-IB controller had not invoked a local lockout.

The LOCAL key is the only active front panel key when the unit is in REMS (remote state).

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5-5. AUTOSCALE

When the AUTO-SCALE key is pressed the instrument will select the vertical sensitivity, vertical offset, trigger level and sweep speed for a display of the input signal. If input signals are present at both vertical inputs the sweep will be triggered on Chan 1 and the display will go to the split screen mode and the vertical sensitivity for each channel will be scaled appropriately If only one of the vertical has a signal on it, the split screen function will be turned off. See Operating Characteristics for input signal requirements for proper AUTO-SCALE operation.

When the AUTO-SCALE cycle is complete, the Timebase menu will be selected and the input devices will be assigned to the SEC/DIV function.

5-6. ENTRY DEVICES

Under the SYSTEM CONTROL keys is an area labeled ENTRY. Located in this portion of the front panel is a number pad, a vertical column of 5 ENTER keys, the "knob" and two step keys, (refer to figure 5-1) These four items are referred to, throughout this manual, as the "entry devices".

The entry devices are used to change the value of any of the items in the function menus that are displayed in UPPER CASE letters e.g., VOLTS/DIV and SEC/DIV. The function menus are on the right side of the CRT.

The value of the selected variable function is listed at the top of the waveform display area on the CRT.

5-7. MENU SELECTION

Softkeys provide front panel control of the 54110D color digitizing oscilloscope

This instrument has two sets of softkeys, the first set is located at the bottom of the CRT, and the second set is right of the CRT. The keys at the bottom of the CRT are referred to as the "menu selection keys" as they are used to choose a desired function menu. As you press the different function menu selection keys the function menus along the right side of the CRT will change. Pressing the More key at the bottom right-hand corner of the CRT provides an additional seven function menus. If the More key is pressed again the original menu will return.

After you have selected a function menu, notice some of the function menu softkey labels have text shown in inverse video. If the adjacent softkey is pressed the text that is in inverse video will change, e.g., to turn a function On or Off, or to activate an associated function, e.g., pattern trigger, edge trigger, state trigger. If the function select key allows you to select a waveform source the text of the selected source will be the same color as the displayed waveform from that source, for example, if the default colors are used all text relating to channel 1 will be yellow and all text relating to channel 2 will be green.

When a softkey with an upper case label is pressed the label will typically change to a color associated with the function that has been selected to be slaved to the input devices.

The third type label for function softkey will have the first letter of each word in upper case and there will be no inverse video text associated with the label. When a function key with this type of label is pressed the function will execute. This type of label is used primarily in the Measure and Utility menus.

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SECTION 6
FAMILIARIZE YOURSELF WITH THE MENUS

6-1. FAMILIARIZE YOURSELF WITH THE MENUS

This section contains a description of the front panel operation of the 54110D. Operating details and front panel layout are discussed in detail. You should read this section completely before continuing to Sections 7 and 8.

6-2. VERTICAL

After you have energized the unit, connect one of the cal signals from the rear panel to the channel 1 input. The most convenient method of scaling the vertical and horizontal is to press the AUTO-SCALE key. This key causes the 54110D to evaluate the vertical inputs and scale the vertical and timebase for a triggered and appropriately scaled display. See Operating Characteristics in Section 1 for limitations of AUTO-SCALE.

6-3. AUTO-SCALE

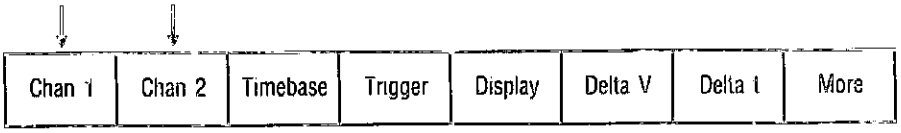
When the AUTO-SCALE key is pressed, the DELAY will be set to 0 seconds and referenced to center screen. The instrument will be left in the Timebase menu with SEC/DIV the assigned function for the Entry Devices.

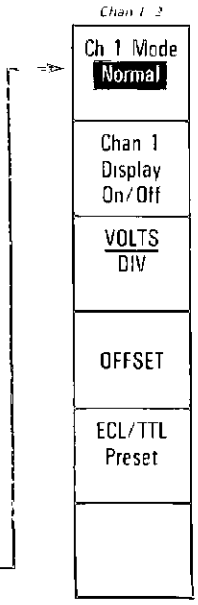
Rotate the "knob" and notice the sweep speed change, enter "1" from the key pad and press the μsec entry key, the sweep speed will go to 1 μsec/div. Next alternately press the step keys, the sweep speed will either sweep faster or slower depending on which step key is pressed. These three devices are referred to as the Entry Devices and are used to change variable functions on this instrument.

If no signal is detected on the inputs, a red error message will state "No signal found".

If there is a signal present at the inputs of both channels, the 54110D will go to the split screen function, that is, channel 1 will be displayed in the top half of the display and channel 2 will be displayed in the bottom half of the display. The unit will be set to trigger on channel 1.

6-4. CHANNEL 1 and CHANNEL 2 MENUS





When Chan 1 or 2 is selected, one of three channel modes will appear on the right side of the display, (see Figure 6-1) The first is the Normal mode, the second is the Magnify mode, and the third is the Func 1/2 on. The normal and magnify modes have associated menus, and the func1/2 modes do not. Func1/2 can be turned off or on in the Wfm Math menu. When they are on, they replace chan 1 and 2 respectively Chan 1/2 and Func 1/2 are displayed in the same color respectively.

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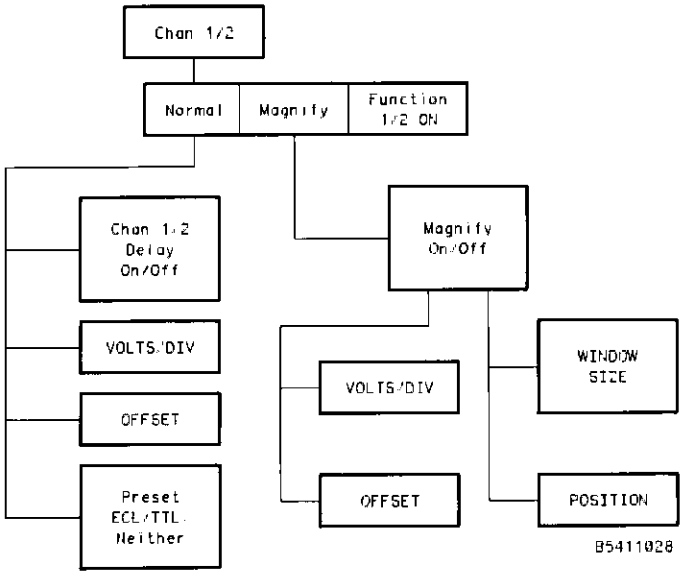
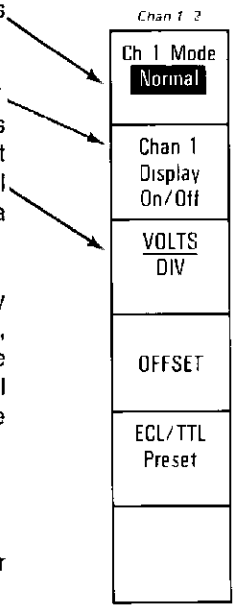


Figure 6-1 Chan 1/2 Menu

6-5. NORMAL MODE

The Normal mode should be selected when the entire vertical magnitude of the input signal needs to be observed. When operating in this mode, you should not adjust VOLTS/DIV or OFFSET in such a fashion that the signal will be off scale vertically as erroneous results may be acquired.



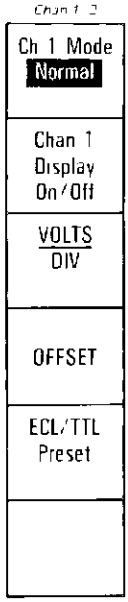
The display On/Off key is the second from the top. Push it and notice that the Chan 1 signal disappears and reappears depending on whether On or Off is selected. This function key turns off the display for a particular channel. It does not stop that channel from acquiring data. Next is the VOLTS/DIV key which when selected will allow the vertical sensitivity to be changed in a 1-2-5 sequence in three ways: (Note; a 1-2-4 sequence is used when are in the split screen mode).

1. Vertical sensitivity can be changed by using the number pad on the Entry portion of the front panel. After a number on the key pad has been pressed, the appropriate "units" key must be pressed to complete the operation. The units keys are located just to the right of the key pad. Note: In the Normal mode all entries other than 1-2-5 will default to the nearest 1-2-5 range. In the Magnify mode, sensitivity can be entered to 3 digit resolution.

2. The knob may be used to change the vertical sensitivity.

3. The step keys, located just above the knob, may be used to increment or decrement the vertical sensitivity.

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These three entry devices may be used on any function menu item that is written in UPPER CASE letters Notice that as these upper case functions are selected they assume the color of the source that they are associated.

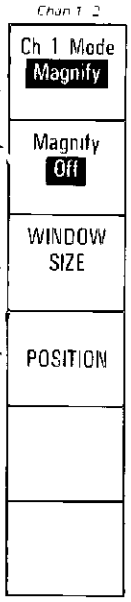
The next function key is OFFSET which when selected allows the trace to be moved up or down by using the number pad, the knob, or the step keys. This function works much the same way as a conventional oscilloscope position control. The OFFSET voltage as referenced to center screen is shown at the top of the waveform display area

The next function key is the Preset key. This key provides three choices:

1. ECL
2. TTL
3. Neither

When ECL or TTL is selected for a channel the instrument automatically selects the correct OFFSET, VOLTS/DIV, and TRIG LEVEL for the logic family that was selected. If the ECL or TTL function is selected the selection will be highlighted. When neither preset is desired, press the preset key until neither ECL or TTL is highlighted The OFFSET, VOLTS/DIV, and TRIG LEVEL will then return to their previous settings.

6-6. MAGNIFY MODE



When the magnify mode is selected, Magnify can be turned On/Off by pressing the Magnify On/Off key. When Off is selected there will be two variable functions on the vertical function menu; WINDOW SIZE and POSITION. They can be changed by using any of the entry devices i.e., step keys, the knob, or number pad. The horizontal lines that define the window can be moved closer together or farther apart by manipulating the entry devices. The window defines the range that will be displayed full scale when Magnify is keyed on When the POSITION function is selected, the user can move the window on the vertical axis by using the input devices. Note: This is different from vertical position; the window moves not the signal. The Magnify function is easy to demonstrate:

Connect the cal signal to Chan 1 and push AUTO-SCALE.

Select:

Mode = Magnify
Magnify = Off
Display = Averaged
# of Averages = 64

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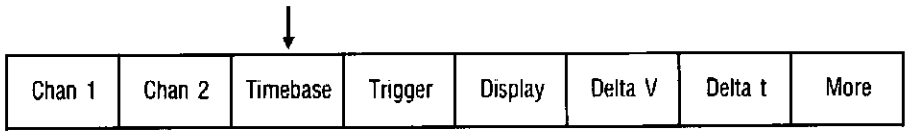
Alternately select and adjust the WINDOW SIZE and POSITION so the window is about the pulse top. When Magnify is turned On the portion of the signal that was defined by the window will fill the display. The vertical sensitivity or offset for the magnified display is shown at the top of the waveform display area.

The vertical sensitivity and offset can be adjusted in the Magnify mode by selecting the appropriate function key and using one of the entry devices.

You would use the magnify function if you wanted to evaluate a small signal such as a reflection or overshoot that was present on large signal. Magnify can also be used to provide increased vertical sensitivity.

The Magnify mode allows higher vertical resolution, up to 16X magnification in the average mode. Note, the magnify mode is most useful when the instrument is in the average mode.

6-7. TIMEBASE MENU



After the AUTO-SCALE system control key is pressed you will notice that the instrument has established itself in the timebase menu and the SEC/DIV function.

The Timebase menu contains two variable functions. Note: Variable functions are identified by UPPER CASE LABELS. (See Figure 6-2.)

The SEC/DIV function allows the time scale on the X-axis to be varied from 1 sec/div to 100 ps/div in a 1-2-5 sequence by using the entry devices. Sweep speeds can be entered from the number pad with up to 3 digits of resolution.

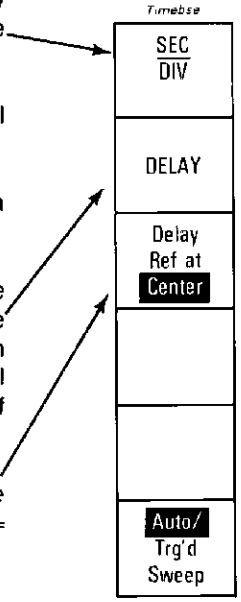
The effect is very similar to turning the time/division switch on a conventional oscilloscope.

For sweep speeds slower than 2.5 µs/div the sampling rate is changed to provide an appropriate display on the CRT.

The DELAY function controls the pre and post trigger delay and can be varied by the entry devices. The adjustment resolution for DELAY time is equivalent to 0.2% of the time interval represented by 10 horizontal divisions (but not less than 2 ps or 1 ppm whichever is greater). The DELAY function has an effect similar to that of a horizontal position control on a conventional oscilloscope, but with the added advantage of having a range of millions of screen widths.

The Delay Ref key allows you to reference the delay to the right or left graticule edge or center screen. The time at the Delay ref. is equivalent to the delay time. DELAY = 0 is the trigger point

When the DELAY function is selected, delay time is displayed at the top of the waveform display area. Maximum pre and post trigger time intervals vary with sweep speed and Delay Ref. location.



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Negative DELAY values infer time before the trigger and positive DELAY values infer time after trigger. The trigger point is at DELAY = 0.

The last key on the Timebase menu is the Auto/Triggered (Trg'd) key. When the Auto sweep function is chosen the unit will provide a baseline on the display in the absence of a trigger signal. If a signal is present, but is not triggered, the display will be unsynchronized but will not be a baseline.

If the unit is in Trg'd sweep and no trigger is present the unit will not sweep, and the data acquired on the previous trigger will remain on-screen.

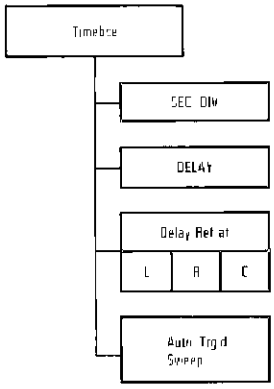


Figure 6-2. Timebase Menu

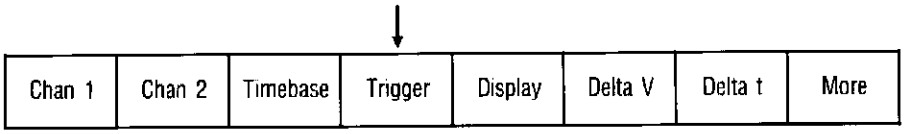
Always use the Trg'd Sweep function when the trigger rep rate goes below 20 Hz, to prevent Auto Sweep from generating a sweep prior to the trigger event. The signal on the display that was initiated by Auto Sweep would be asynchronous with the signal on the sweep that was initiated by the trigger event. The oscilloscope will trigger normally if the trigger repetition rate is greater than 20 Hz.

NOTE

The STATUS line in the upper left corner of the screen indicates the current trigger status. It is updated every half second. In the Trg'd sweep mode the STATUS line indicates whether the instrument is "Running" or "Awaiting Trigger". In the Auto Sweep mode the STATUS line indicates whether the instrument is "Running" or "Auto Triggering". Other status indications are "Stopped", "Measuring", "Printing", "Plotting", and "Testing". The 20 Hz auto trigger repetition rate applies even for long DELAY or large SEC/DIV settings.

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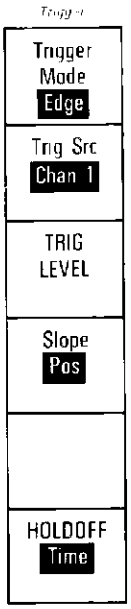
6-8. TRIGGER MENU



The Trigger menu allows you to select trigger mode, source, slope and holdoff. This menu also is used to invoke the unit's combinatorial triggering capability (logic pattern triggering). (See Figure 6-3).

When previewing the trigger menu notice the five trigger modes: Edge, Pattern, State, Time-Delay, and Event-Delay modes. Let's first discuss the Edge Mode Edge Mode allows you to select one of four trigger sources (Trig Src), adjust the trigger level (TRIG LEVEL), select the slope of the input signal that is to be used to define the trigger (Pos/Neg), and define the HOLDOFF in Time or Events.

The Trig SRC key permits the selection of one of four possible trigger sources; Chan 1, Chan 2, Trig 3, or Trig 4.



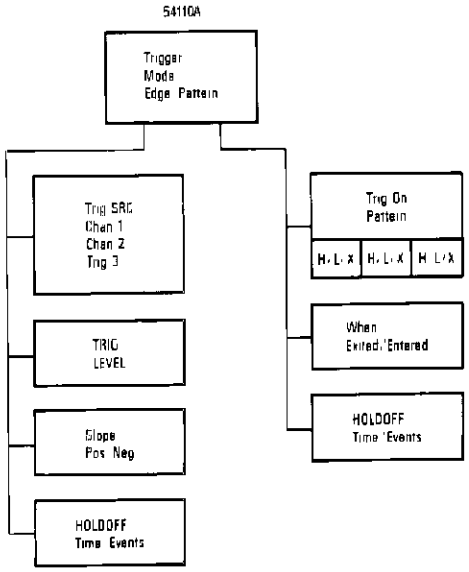


Figure 6-3. Trigger Menu

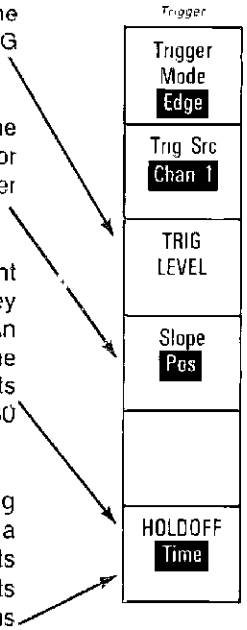
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If Chan 1 or 2 is selected as the Trig Src a horizontal line (orange) will appear on the display showing the TRIG LEVEL with respect to the displayed signal when TRIG LEVEL is assigned to the entry devices.

Slope selects the Neg or Pos slope of the input signal to be used as the trigger. The trigger slope and level can be set independently for each channel and the settings for the channel will be retained even though another channel is selected as the trigger source, or another trigger mode is selected.

The HOLDOFF circuitry allows you to define the period following a trigger event during which the trigger circuit is disabled. By pressing the HOLDOFF function key you can determine whether the HOLDOFF is to be defined by time or events. An event is defined as a change in the input that satisfies the trigger conditions. If Time is used to define holdoff the range is from 70 ns to 670 ms. HOLDOFF by Events range is from 2 events to 6.7 X 10E7 events. Maximum counting rate for events is 80 MHz.

Holdoff by events can be used to trigger stably on a complex waveform by counting the number of trigger events that are to be skipped before accepting another for a trigger. By setting the holdoff by events to one less than the number of events occurring over the fundamental period, a stable display will result. Holdoff by events is equivalent to placing a divide-by-N counter in the trigger path where N is one plus the holdoff value.



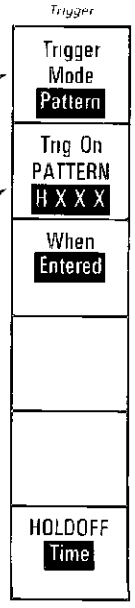
Unlike conventional oscilloscopes the trigger system in the 54110D is completely independent of the timebase. This means that adjusting the DELAY or SEC/DIV functions will not disturb the display synchronization established with holdoff. Also, it should be noted that auto sweep acts on the repetition rate of accepted triggers so holdoff by time values greater than 50 ms or large holdoff by events values can result in a low effective trigger repetition rate. In this case the Trg'd sweep function should be used. Holdoff can be varied by using any of the entry devices and is displayed at the top of the waveform display area.

6-9. PATTERN MODE

Press trigger mode function key to access the Pattern Mode. In this mode you have 4 bit pattern recognition capability and the instrument can be triggered either when entering or exiting this pattern. Holdoff can be defined either by events or time.

The label for the Trig On PATTERN function key includes four characters in an inverse video text field. When the Trig On PATTERN key is pressed one of these characters will be highlighted. By using the entry devices you can change this character to one of three letters; X, L, or H. Pressing trig on pattern again will sequence through the character field so each can be edited. X indicates a "don't care condition", L indicates a requirement for an input < the trigger level for that input. H indicates a requirement for an input > the trigger level for that input.

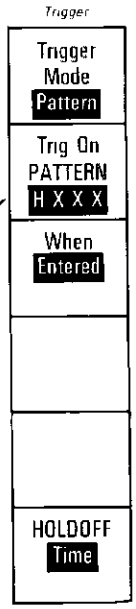
The three characters in this text field determine whether the voltage levels at each of the four inputs (Chan 1, Chan 2, Trig 3, and Trig 4) are required to be above or below TRIG LEVEL or are not used as a trigger qualifier. If these characters read "LHXX", Chan 1 would have to be below the trigger level, Chan 2 would have to be above the trigger level to satisfy the pattern condition.



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NOTE

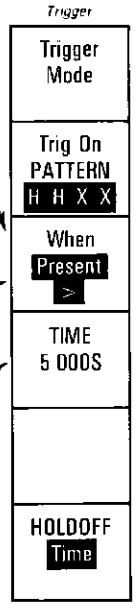
Set the TRIG LEVEL for each trigger source while you are in the Edge mode. These trigger levels must be set before going to the Pattern mode or proper Pattern triggering may not occur.



The next key on the function menu is the When Entered/Exited key. When this key is pressed the inverse video text field next to the key will change from Entered to Exited or vice versa. If When Entered is selected, the unit will generate a trigger on the last transition that makes the PATTERN true. If When Exited is selected the unit will generate a trigger on the first transition on any of the inputs that cause the pattern to be false, after it was initially true.

When you are in the pattern mode and you have pressed the Trig On PATTERN key the condition that a particular input must be in to satisfy the requirements the pattern requirements will be shown at the top of the waveform display area.

If When Present > is selected, a trigger event will occur if the trigger pattern is true for a minimum time period. This period is listed in the label for the time key and can be varied from 10 ns to 5 sec. by the entry devices.



When the trigger pattern remains true for the required period of time, a trigger will occur when any of the inputs transition to a false state.

If the pattern becomes true and then goes false before the specified time, no trigger will occur.

If When Present< is selected, a trigger will occur only if the trigger pattern is satisfied and one of the inputs transitions to a false state before a given time period. In this mode, the pattern must be true for at least 1 ns to be recognized.

This period is listed in the time key label and can be varied from 10 ns to 5 sec. by the entry devices. Only holdoff by time is available within the when present modes.

Press the Trigger Mode key, the label will change to State. In the State mode one of the inputs is selected as a simple edge source, the other three are used to define a pattern.

A trigger will occur on the edge (pos/neg) when the pattern is true and Is Present is selected. A trigger will also occur on the edge (pos/neg) when the pattern is false and Is Not Present is selected. The threshold is set by TRIG LEVEL when you were in the edge mode. Only holdoff by time is available with the state mode.

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Press the Trigger Mode key and the label will read "Time Dly", (Time Delay). This menu allows you to arm on a signal edge on any source, wait for a period of time and then trigger on an edge from a different source. The edge polarities, the sources that are used to define the edges, and the delay time are all user definable.

The second and third function keys allow you to select the polarity and source of the arming edge. The delay time range is from 20 ns to 5 sec

The fourth key allows you to define a waiting period between the arming edge that is used as a trigger qualifier and the edge on which the instrument triggers.

The fifth and sixth function keys allow you to select the polarity and source of the edge that is used as the trigger event.

The last trigger mode is Evnt-Dly, (event delayed), This menu allows you to define an edge as a trigger qualifier. Once this edge is detected the unit will trigger after a definable number of edges on any other source.

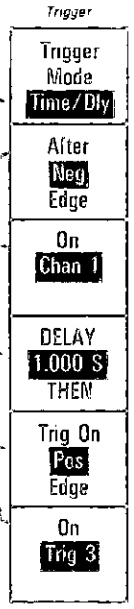
The second and third keys on the menu allow you to select the polarity and source of the arming edge.

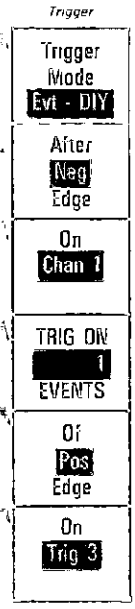
The fourth key allows you to determine the number of edges on the trigger source that are to take place before the trigger event.

The fifth and sixth keys allow you to determine the polarity and source of the triggering and counting edge.

In the edge mode TRIG LEVEL is used to specify a threshold for each source independently. It is these thresholds that are in effect in all other modes wherever a source is active in a triggering function. Other than thresholds there is no interaction between the trigger menus. Changing slopes or patterns in one menu will not affect corresponding entries in other mode menus.

In most of the triggering modes it is possible to specify parameters which will reduce the effective trigger repetition rate (display triggers) to below 20 Hz. Since the auto sweep function measures the rate of display triggers the timebase should be put in Trig'd mode to avoid premature automatic triggers with large event delay counts, filter times etc.





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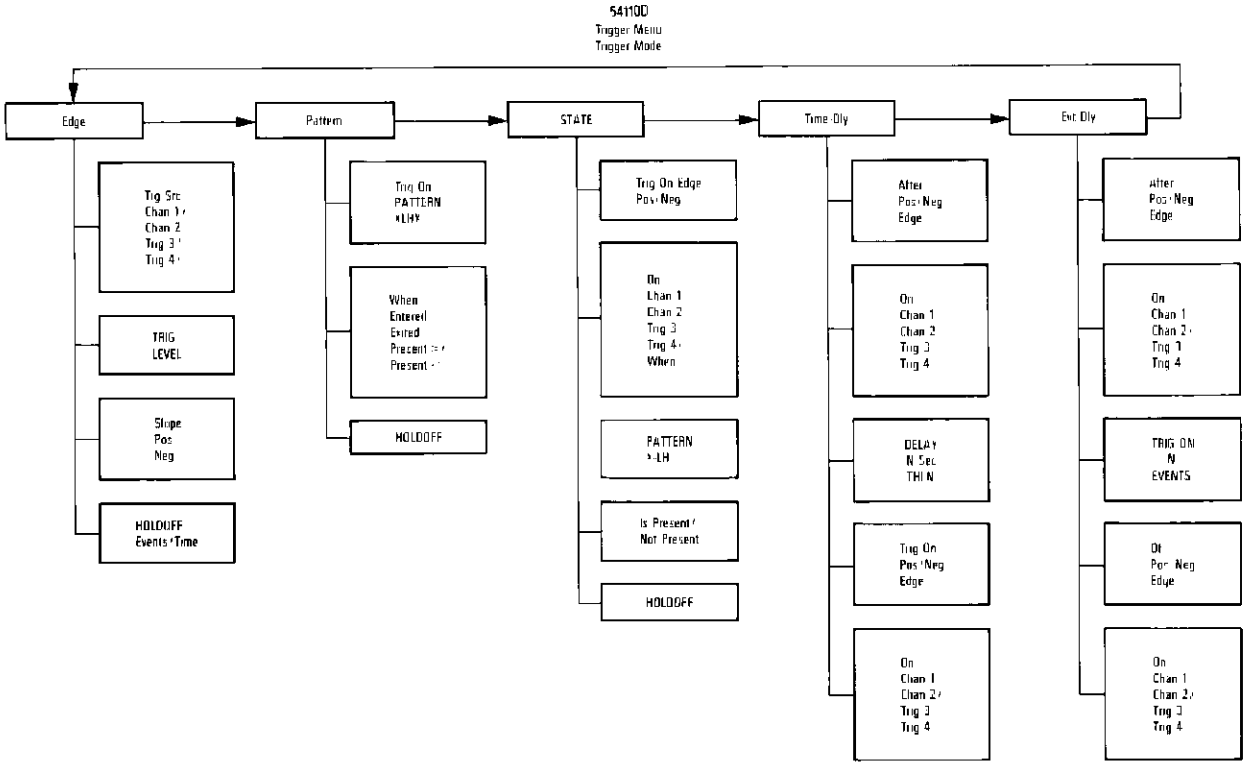
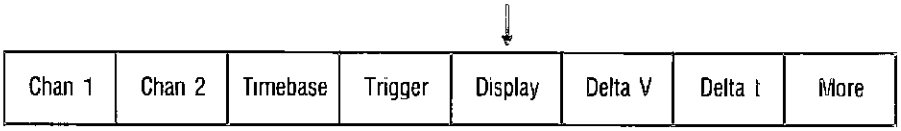
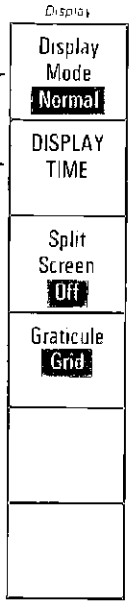


Figure 6-4. Trigger Menu

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6-10. DISPLAY MENU





When the Display function menu is chosen two modes are available, Normal and Averaged. (See figure 6-5.)

In the Normal mode each displayed data point is displayed for a period of time defined by the user. You can vary the DISPLAY TIME (persistence) from 200 ms to infinity.

In infinite persistence the data points will remain on the display until the CLEAR DISPLAY key is pressed or until the sweep speed, vertical sensitivity or trigger level are changed. The persistence is shown at the top of the waveform display area.

If variable persistence (persistence other than infinite) is selected, you have a flexible display that changes with variations in the input signal but stores the signal indefinitely on the display if the trigger is lost and the unit is in Trg'd Sweep.

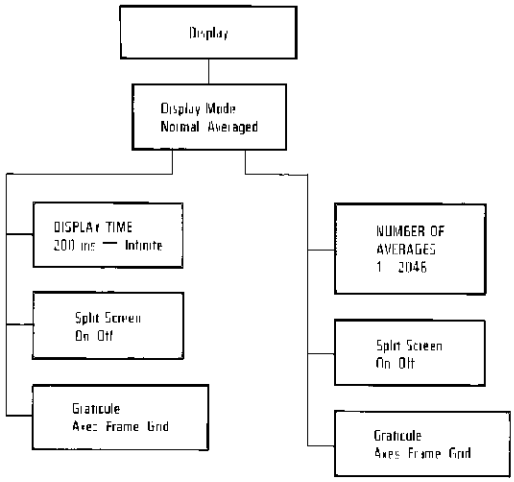
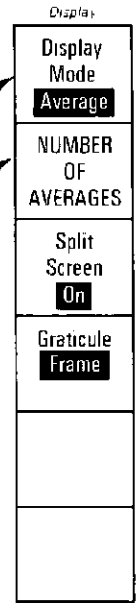


Figure 6-5. Display Menu

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A minimum persistence setting is useful when the input signal is changing and the user needs immediate feedback, such as in rapid probing from point-to-point, or setting the amplitude or frequency of a signal source. More persistence is useful when observing long-term changes in the signal or low signal repetition rates. At fast sweep speeds and low trigger rep. rate conditions more persistence is needed to gain an adequate number of data points on the display. Infinite persistence is useful for worst-case characterization of signal noise, jitter, drift, timing, etc.

There is a limit to the number of data points that can be displayed on the screen at any one time in the variable persistence mode. The display time is temporarily reduced whenever the number of points exceeds 5,600. This has the effect of reducing the number of data points on the display. When this happens you might see the display appearing to pulsate, that is, a number of points will accumulate and then the display will fade and build up again, etc.



If Averaged Mode is selected the last acquired data points are averaged with previously acquired data before they are displayed. The number of data points that is averaged is variable from 1 to 2048. The step keys and the knob change the number of averages in powers of 2; however, any number of averages between 1 and 2048 can be entered from the key pad.

Vertical resolution can be extended and displayed noise can be significantly reduced by using the averaged mode. As the number of averages is increased, the display becomes less responsive to changes to the input signal(s), however, noise is reduced, and resolution is improved as more averages are used. By selecting the appropriate number averages the throughput for the automatic pulse parameters or the precise edge locators can be controlled. Since these automatic measurements use averaging the user can trade off the speed of the measurements against the repeatability of the measured results.

The input signal is digitized and each data point is assigned a time slot relative to the trigger. In the averaging mode the unit calculates the average of the most recent data point with the previous values in the same time slot. You can define the number of data points that are to be averaged from 1 to 2048. Each average is calculated from data acquired for each time slot, data for adjacent time slots is not averaged together.

The current number of averages which have been accumulated is listed on the second line of text in the upper left of the screen. When a precise measurement is made in the average mode, this readout displays the running number of averages for the measurement. Because only data points in the same time slot with respect to the trigger are averaged together, averaging does not reduce the bandwidth or risetime of the acquired waveform.

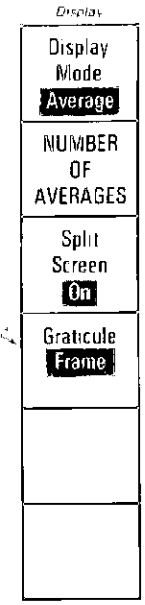
The next function key on the display menu is the Split Screen key. When split screen is keyed On, Chan 1 or Func 1 will be presented in the upper half of the display and Chan 2 or Func 2 in the lower half. Scaling accuracy is maintained as this function is turned off/on. When the split screen function is keyed off Chan 1 or Func 1 and Chan 2 or Func 2 will be overlaid on the display area.

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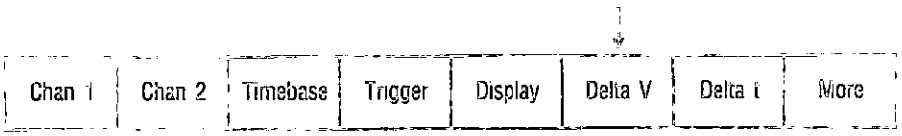
NOTE

In the split screen mode each channel occupies 4 vertical divisions rather than 8 as is the case when split screen is off. This requires the vertical sensitivity in volts/div be doubled.

Three different graticules are available in the display function menu. Press the graticule key and cycle through them to see how they appear. You will find that using the frame graticule makes it easier to see the Delta V and Delta t markers.



6-11. DELTA V (VOLTS) MENU



When the Delta V (delta volts) menu is enabled, two markers are displayed. These markers can be used to make absolute voltage measurements on the signal under evaluation or as reference markers when adjusting a signal to a given amplitude. (See figure 6-6)

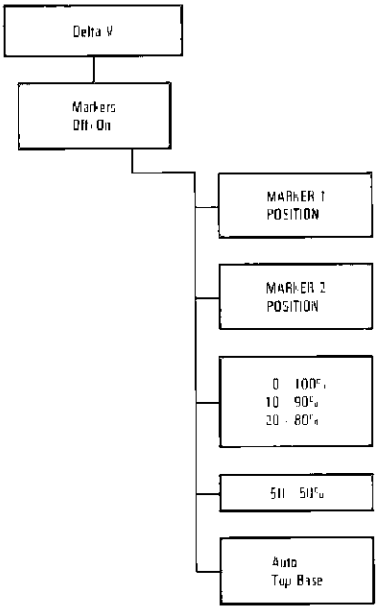


Figure 6-6. Delta V Menu

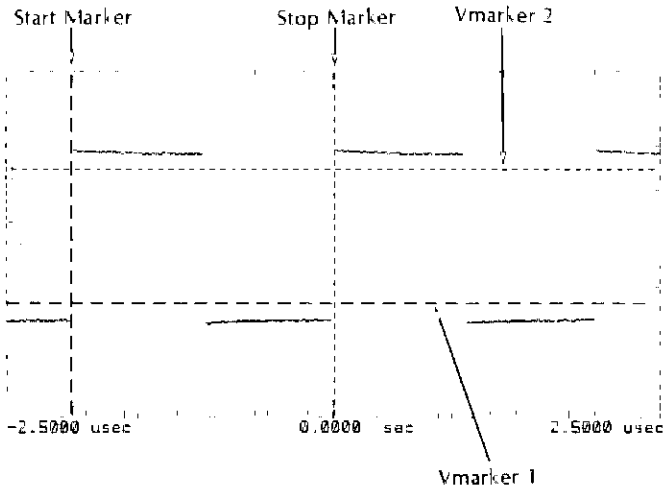
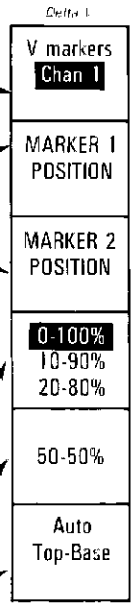


Figure 6-7. Vmarkers

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Once the delta V menu is selected, the markers cannot be activated unless the display for chan 1 or 2 or func 1 or 2 or memory 1-4 is turned on. Choose the source you would like to evaluate and enable the V markers. Observe the next two functions on the delta V menu, MARKER 1 POSITION and MARKER 2 POSITION. (See figure 6-7.)



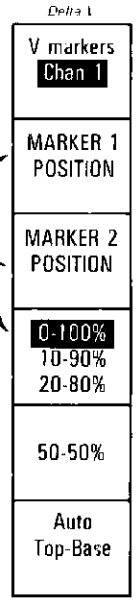
After assigning the markers to the desired channel(s), func(s), memory or memories selecting marker 1 position and marker 2 position function keys will allow you to position the markers vertically with the entry devices. The voltage shown at the top of the waveform display area indicates the voltage level of the selected V marker. Note, if you are using the default color, set the V marker you have selected and it's label will be orange. Delta V (also orange), the difference between the two markers, is shown in the factors area at the bottom of the display.

In the lower portion of the display are the "display factors", these factors include the delta V value and the absolute value for each marker. The delta V function simplifies waveform measurements.

The next three keys on the delta V menu automatically position the V markers on the display. The 0-100/10-90/20-80% key causes the instrument to perform some calculations and position the V markers for the user. When the V markers are positioned manually the inverse video field will change to 0-100%. If the key that is showing 0-100% is pressed the label will change to 10-90% and the markers will move to the 10% and 90% points of their previous levels. If the key is pressed again the label will change to 20-80% and the markers will move to the 20% and 80% points of their original levels. The 50-50% key moves both markers to the 50% point of the 0-100% levels.

The Auto Top-Base automatically locates the top and base of the displayed waveform. This is done by evaluating a histogram of the displayed signal.

If either of the V markers are manually repositioned while the function switch is in 10-90%, 20-80%, or 50-50% the original reference will be lost and the label for the key will change to 0-100%.

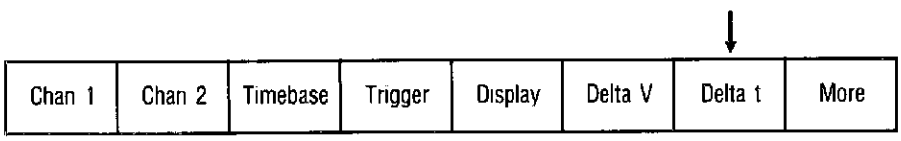


If two channels/functions/memories are on the Vmarkers can be assigned to either display trace or assigned to Dual where Vmarker 1 can be assigned to one trace and Vmarker 2 is assigned to the other If Auto 50-50% key is pressed with Vmarkers set to dual, one Vmarker will go to the 50% point of one trace and the second Vmarker will go to the 50% point of the other trace.

Input the cal signal from the rear panel to Chan 1 and press auto-scale. Next select the Delta V function menu and key on the V markers. Now, establish the top-base by pressing auto top-base. To demonstrate the action of the 0-100/10-90/20-80% key, press it several times, notice how it cycles through the three selections and how the V markers move. Press the 50-50% key, this establishes the V markers at the 50% point of the signal.

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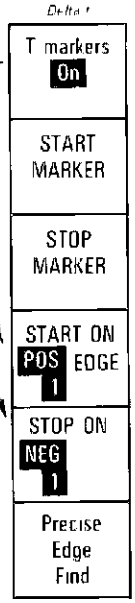
6-12. DELTA T (TIME) MENU





The Delta T function menu provides control for two T (time) markers that can be used to make measurements in the time domain. The display factors include Δt which is the time interval between the two t markers. In figure 6-8 the Start marker = 2 us and the Stop marker = 0 sec. These times tell you the time between the T markers and the delay ref. (See figure 6-8.)

After the t markers have been enabled, each t marker can be moved manually by selecting START MARKER or STOP MARKER and using the entry devices. The time between the selected t marker and the trigger event is listed just above the waveform display area on the CRT.



The Delta t menu is extended when the Delta V markers are turned on. START ON EDGE, STOP ON EDGE, and Precise Edge find Functions are available on the Delta t menu when the Delta V markers are on. Try this exercise to demonstrate these capabilities.

Connect the cal signal to Chan 1 and press the AUTO-SCALE control key. Select the delta t menu and turn the t markers on. Manually move the start marker so that it coincides with the first positive leading edge of the cal signal (figure 6-7). This is one way of making a time interval measurement.

In the display factors, the start marker is approximately 2 us ahead (-2 us) of the trigger event (delay = 0) which was established at center screen when you used AUTO-SCALE. The stop marker is located approximately center screen and the time interval between the t markers (delta t) is approximately 2 us

Select the delta V menu and turn the V markers on. Press auto top-base then press 50-50%. For this measurement the significant thing is to make sure that the V markers intersect the rising and falling edges of the signal.

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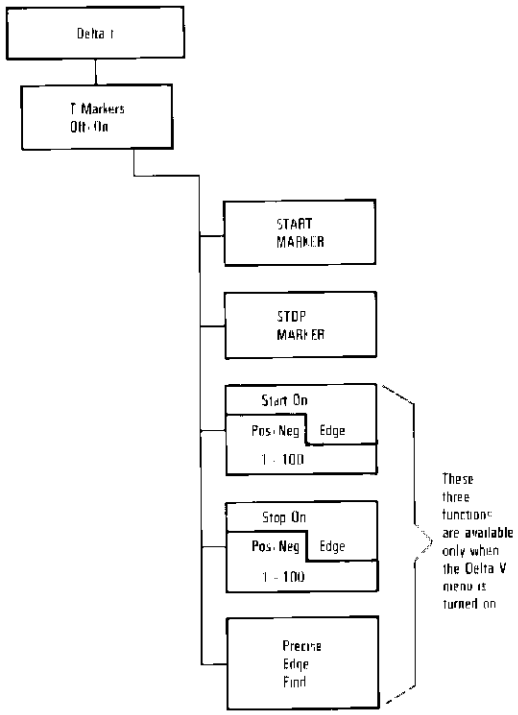


Figure 6-8 Delta t Menu

Return to the delta t menu Press START ON EDGE function key several times, notice that the pos/neg indicator alternates and the start marker moves from the positive edge of the first pulse to the negative edge of the same pulse. Try using each of the entry devices to move the START EDGE to another pulse STOP EDGE can be changed in this fashion also. Start on edge and stop on edge are "coarse" edge locators in as much as data already collected on screen is used to locate the edges.

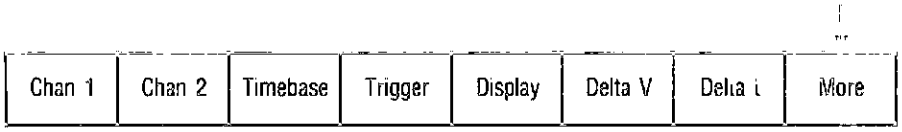
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To demonstrate the last delta t menu function, precise edge find, return to the delta V menu and press auto top-base to locate the top and base of the cal signal, then select 10-90%. Now again return to the delta t menu. Set start edge to pos 1 and stop edge to pos 1 and press precise edge find. Δt (in the factors field) will represent the rise time of the pulse, in this case approximately 2 ns. Note that the instrument automatically selects a faster sweep range, to increase the resolution of the edge finder

The precise edge find function initiates an automatic time interval measurement. The instrument will acquire the data, make the measurement and have the delta t and delta V markers visible on the display so that you can see where the automated measurements were made

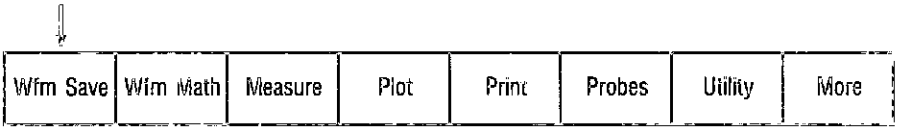
When you use the precise edge find function the unit will expand the selected edges defined by the start on edge and stop on edge functions. This expansion is accomplished with newly acquired data. By expanding the edge in this fashion the horizontal resolution is increased. The speed and repeatability of this measurement is influenced by the number of averages The more averages the more repeatable and slower the measurement will be Other items that will influence measurement speed and repeatability are: input signal edge speed, repetition rate, signal jitter, starting sweep speed and delay. If the Vmarkers are set to dual and you press auto 50/50, you may do a semi-automated 2 channel time interval measurement by going to the Delta t menu and pressing precise edge fine key.

6-13. MORE



To view the remaining menus press the "More" key it is located in the lower right hand corner of the display. This key allows you access to seven additional function menus. Pressing the More key again allows you to return to the original set of menu keys.

6-14. WFMSAVE (WAVEFORM SAVE)

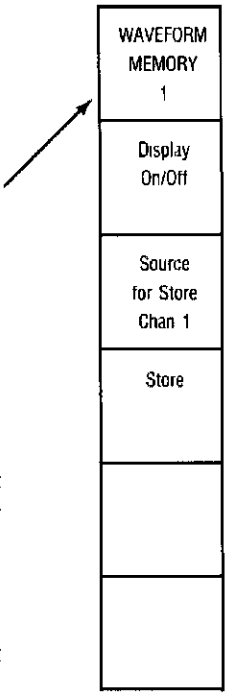


The 54110D has 6 waveform memories available from the front panel; Waveform memories 1 through 4 and pixel memories 5 and 6. (See Figure 6-9.)

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When waveforms are stored to one of the four waveform memories the waveform factors are stored as part of the record. These factors include: vertical sensitivity, vertical offset, sweep speed, and time delay. The fact that these factors are maintained allows you to make measurements on waveforms stored in these memories. These waveform records can store only one waveform at a time. If you store a waveform to a memory that contains a waveform record the first record will be written over and lost.

Pixel memories 5 and 6 are 256 by 501 bit memories and are constructed so that multiple waveforms can be stored in each. If more than one waveform is stored to a pixel memory the waveforms will be superimposed. Waveform factors are not maintained when a waveform is stored to a pixel memory, therefore measurements cannot be made on these waveforms. The first function key on the waveform save menu is the WAVEFORM/PIXEL MEMORY select key. When this key is pressed repeatedly the selected memory will cycle through waveform memories 1, 2, 3, 4, and pixel memories 5 and 6. This function is also slaved to the entry devices, that is, the key pad, step keys and the knob can be used to change the selected memory.



The second key allows you to display or not display the waveform(s) in the selected memory. This key also allows you to select either the upper or lower screen to display the memory when the instrument is in the split screen mode.

When memory 1, 2, 3, or 4 is selected the Source for Store key allows you to select the source of the waveform that is to be stored when the store key is pressed. The potential sources are chan 1, chan 2, func (function) 1 and func 2.

In order for a source to be available for the "source for store", it must be turned on. For example, in order to have func 1/2 as a source for store, the selected function first must be turned on using the Wfm Math menu.

When func 1 or 2 are turned on they replace chan 1 and chan 2 respectively, both in the chan 1/2 menus and the wfm save menu, therefore only two of the four sources can be active at any one time.

If you have selected one of the waveform memories i.e., 1-4, the last key on this menu will be the Store key. When you press this key the source will be stored in the selected waveform memory.

The four waveform memories are nonvolatile memories, that is, the data in these memories is retained when the instrument is turned off and then turned back on. The data in the two pixel memories is lost when the instrument is turned off.

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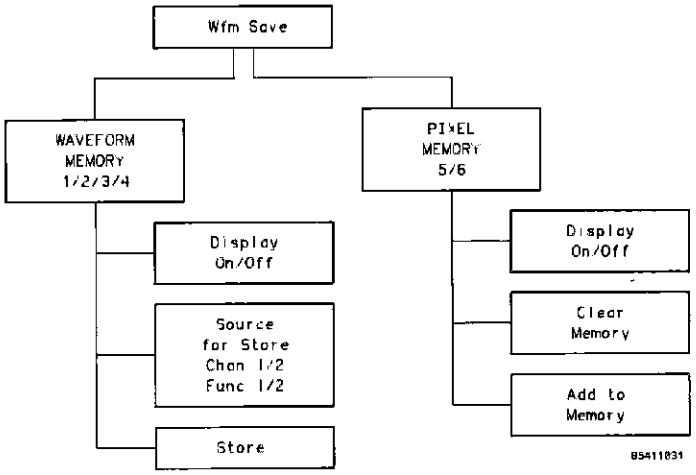


Figure 6-9. Wfm Save Menu

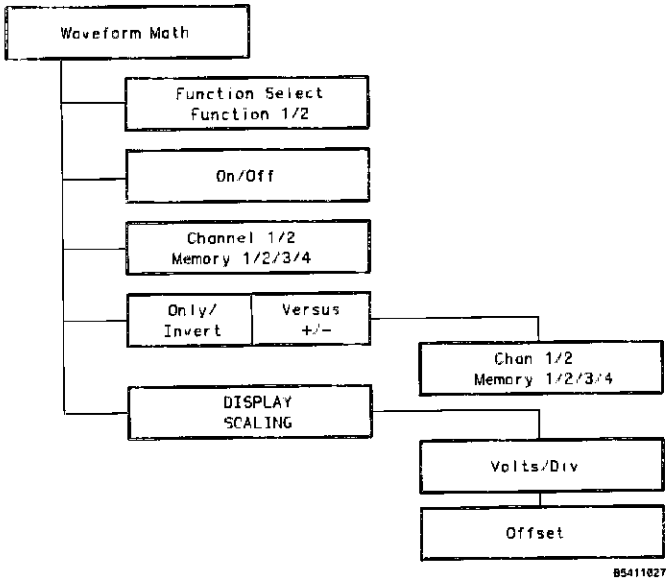


Figure 6-10. Waveform Math Menu

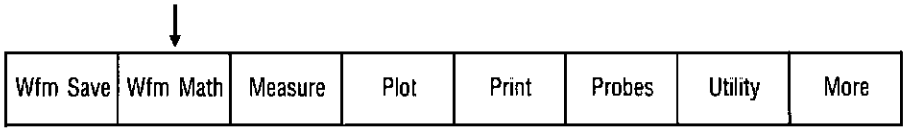
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If you select pixel memory 5 or 6 the function menu will change. The third key will change to the Clear Memory key and the fourth key will be the Add to Memory key.

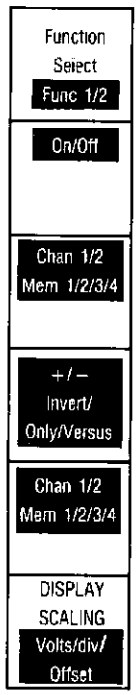
The clear memory key allows you to erase whatever is stored in the selected pixel memory.

When the add to memory key is pressed, whatever data is being displayed in the waveform display area (with the exception of the graticule and markers) will be written to the selected pixel memory, along with whatever data is already there.

6-15. WFM (WAVEFORM) MATH



The Wfm Math menu allow you to define two functions (Func 1 and 2) using the channels and waveform memories as operands. The operators are: +, -, Invert, Versus, and Only. This menu also allows you to determine the vertical offset and scaling for the function display. (See figure 6-10.)



The Function Select key allows you to select Func 1 or Func 2 as the active function. The color of the label and the trace of the selected function will correspond to the associated channel, that is, func 1 uses the same color as chan 1 and func 2 uses the same color as chan 2

The next key allows the display of the selected function to be turned on/off. When a function is turned on it takes the place of the associated channel. For example, if func 1 is turned on the trace on the display will change from chan 1 to func 1. If you select chan 1 menu the ch1 mode will indicate func1 on. If this key is pressed the ch1 mode will change to Normal, and func1 display will be replaced by chan 1. You may toggle the ch1 mode switch and cycle back to func1.

The next key allows the selection of the first operand. The fourth key is used to select the function operator. The choices are; +, -, Invert, Only and Versus. If Invert or Only are selected the second operand is not used.

The next key is used to select the second operand. Your choices are the same as for the first operand.

The last key on the wfm math menu is the DISPLAY SCALING key. This key allows you to slave either the vertical sensitivity (volts/div) or the vertical offset to the entry devices for the display of the selected function. The initial DISPLAY SCALING sensitivity and offset are based on the voltage range of the operands that define the function. When ever the operator or operands are changed the display scaling sensitivity and offset are set to the initial values.

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6-16. MEASURE



When you press the Measure menu select key, you will have access to three function menus which can be accessed by pressing the more key on the function menu. (See Figure 6-11.) If neither of the channels or the funcs are activated measure will default to chan 1 and measurements will automatically will activate the chan 1 display. In order to make automated measurements on chan 2, func 1, 2 or mem 1 through 4 they must be turned on. To make a measurement on a single waveform memory use the Wfm Save menu and turn the desired memory on. The instrument will not make measurements on a func if the operator is "Versus".

The second key in the first measure menu is the Precision Fine/Coarse. This instrument will perform two types of automatic measurements fine precision and coarse precision. Coarse measurements are made on displayed data. If there is insufficient data on screen, new data is acquired in order to make the measurement. Fine measurements begin with a coarse measurement to locate the edge(s). Each edge is then expanded to achieve maximum resolution. The coarse measurements take less time to accomplish, this should be considered if through-put is a more important issue than measurement resolution. Peak to peak, preshoot, and overshoot measurements are always coarse measurement and use on screen data.

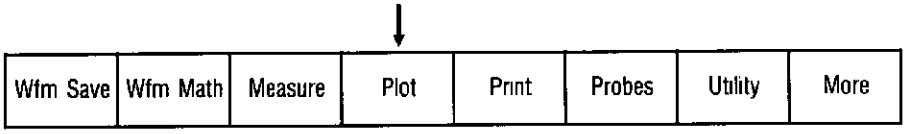
The next function key is the All key, when press the 54110D automatically makes the measurements below and lists the results in the factors area The More key at the bottom of the menu allows you to select the next measure menu when pressed.

Freq (Frequency)	+ Width	Peak-to-Peak Voltage
Period	- Width	Preshoot
	Duty Cycle	Overshoot
	Rise Time (10-90%)	RMS Voltage
	Fall Time (10-90%)	

The instrument will also make a course measurement, that is, using only data on screen, when the 54110D is in the STOP mode. The stop mode can be selected by pressing the STOP/SINGLE system control key. The instrument will only make course measurements on any of the waveform memories or functions that contain a waveform memory as an operand.

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6-17. PLOT

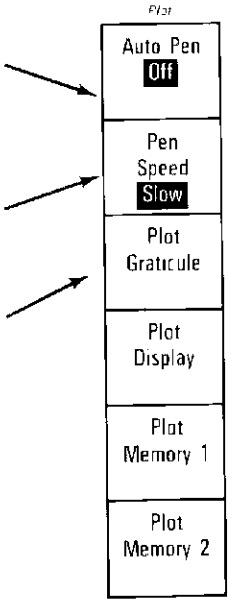


The plot menu allows display data to be output over HP-IB to a digital plotter that is HPGL (Hewlett Packard Graphics language) compatible. (See figure 6-12) The 54110D must be in "Talk Only" and the HP-GL plotter must be in the "Listen Only" mode. The HP-IB mode can be set by using one of the Utility function menus.

The first option on the plot menu is the Auto Pen selection. When this function is On a new pen will be selected when a different function is chosen to be plotted, that is, if the plotter has multi pen capability. If Auto Pen is Off the plotter will not load or change pens when a plot function selected.

The next plot option is Pen Speed You may choose Fast or Slow if your plotter has this feature. Use slow when you are making overhead transparencies. For best results use slow for Leroy pens.

When Plot Graticule is selected the displayed graticule, including display factors, will be output to the plotter.



If the Display menu is in the Averaged mode, the output from the 54110D will cause the plotter to draw a continuous line plot of the active display.

If the Display menu is in the Normal mode the output from the 54110D is formatted such that the plotter will plot the waveform in a pixel format, that is, dot by dot if you are plotting an active display

Waveform memories will always be plotted with a continuous line and pixel memories are always plotted dot by dot.

While a plot is being accomplished you can stop the plot by pressing the Abort Plot key. If you would like to stop for a moment and then continue press the Pause/Continue key.

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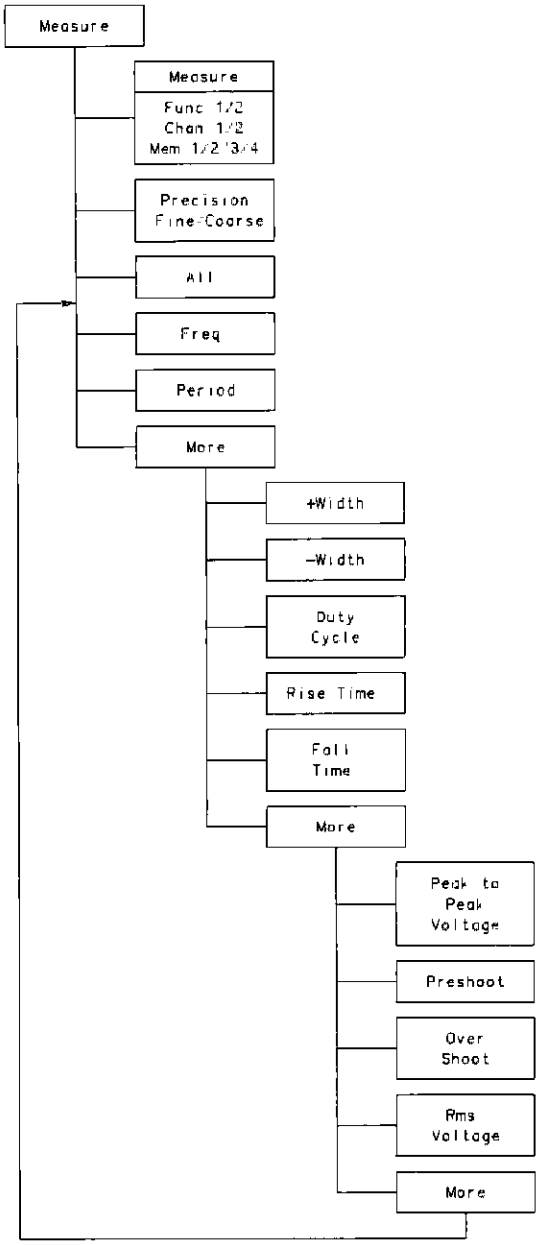


Figure 6-11. Measure Menu

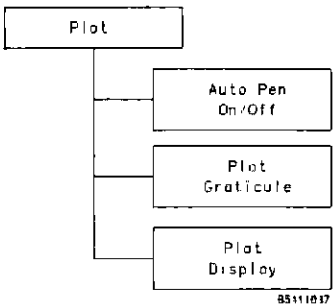
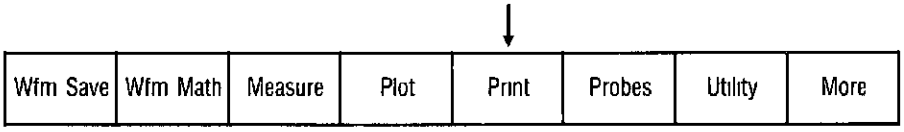
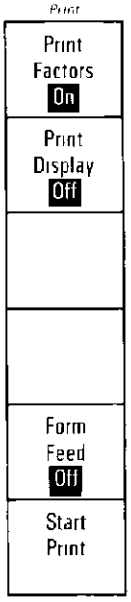


Figure 6-12. Plot Menu

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6-18. PRINT





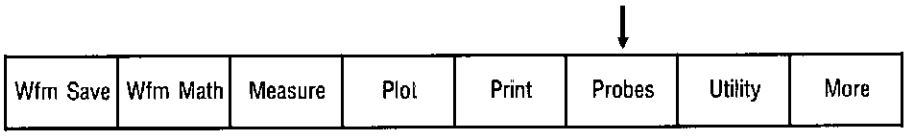
The Print menu allows display data to be output over HP-IB to a graphic printer that is compatible with Hewlett-Packard Raster Scan Standard. (See Figure 6-13.)

The 54110D must be in the "Talk Only" mode and the printer must be in the "Listen Only" mode. The 54110D can be set to talk only when in one of the Utility function menus.

The print function menu offers you two print options, an automatic form feed option and a Start Print key. The two print options allow the selection of the data that is to be output to the graphics printer Both sources, factors and display may be output separately or at the same time to the printer. The display data includes the graticule and the active display.

If you desire automatic form feed after a hardcopy, key this function on After the data has been selected for copying, press the Start Print key to initiate the hardcopy. Signal acquisition stops during printing. To stop printing press the Abort Print key.

6-19. PROBES





When the Probes menu is selected you can enter any arbitrary attenuation ratio from 1 to 1000 for any of the inputs. Any of the entry devices can be used, however, the key pad allows three digit resolution and can be used as a cal factor for Vmarker measurements. (See figure 6-14.)

When you define a Probe Attenuator Ratio the actual sensitivity at the input of the instrument does not change, all that is changed are the reference constants that are used for scaling the display factors and for automatic measurements, trigger levels, etc.

Attenuation ratios can be saved with the rest of the front panel set up in the Save/Recall registers, however, when power is cycled the attenuator ratios will automatically be reset to the nominal 1:1 for the 54002A and 54003A, and 10:1 for the 54001A active probe, since the 54110D queries the input pod receptacles to determine what pods are installed at power-up.

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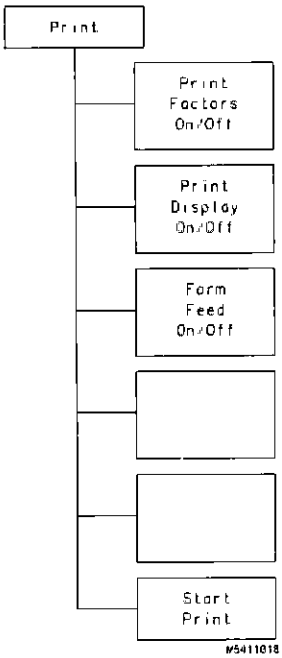


Figure 6-13. Print Menu

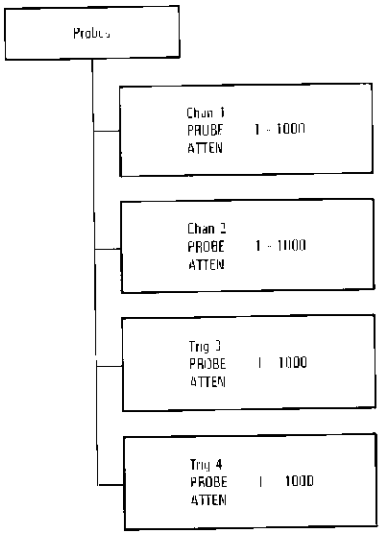


Figure 6-14. Probes Menu

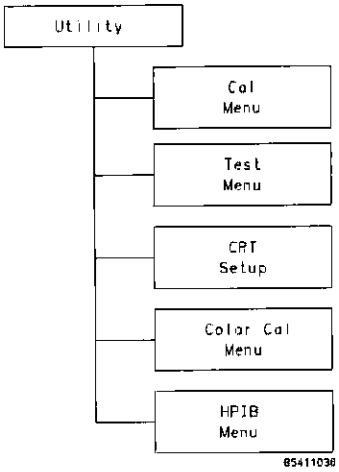
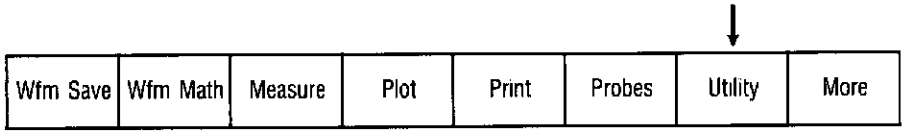


Figure 6-15. Utility Menu

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6-20. UTILITY



The Utility menu select key allows access to five submenus that can be selected by pressing the appropriate key at the right of the CRT. These submenus include:

1. Cal Menu
2. Test Menu
3. Crt Setup
4. Color Cal Menu
5. HP-IB Menu

The Test Menu and the Crt Setup Menu are discussed in the 54110D Service Manual and will not be covered here.

6-21. CAL MENU

The Cal menu is provided to so you can null differences between trigger and data acquisition paths. This would include acquisition differences internal and external to the instrument. See Appendix B for a discussion of this topic. (See figure 6-16.)

In order to obtain the proper cal for a particular system configuration it is necessary to adjust each channel's sensitivity, offset and trigger level as well as the external trigger levels to the values you intend to use. This will establish each input to the configuration that will be used in the actual measurement.

The objective of the cal procedure is to apply a fast edge simultaneously to inputs of the instrument and null out the systematic delay between these inputs. The fastest available edge source should be used (< 1 ns transition time is desirable), however, a signal of the same general characteristics as the signal you intend to measure is a reasonable alternative. For each cal step the inputs should be connected to the calibration source as closely to one another as possible. BNC Tee's and probe adapters are useful to accomplish this.

Be sure to set up all sensitivities, offsets, and trigger levels before beginning the cal menu. The cal menu function allows you to null any differences in propagation delay between signal paths in software in the 54110D This is important so that time-difference measurement results accurately reflect time referenced to the probe tips or the points where the input coaxial cables are connected to the circuit under test.

There are two cal signal outputs on the rear panel. Only one cal source should be used for the cal menu adjustment exercise because the two cal signals are separately buffered and the time differential between the outputs is not characterized.

Connect a BNC Tee to one of the cal signal outputs on the rear of the instrument and connect two equal length 50 ohm cables to the BNC Tee. Connect these two cables to the chan 1 and chan 2 inputs. Next, select the axes graticule

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For this exercise press AUTO-SCALE and set offset and trig level to equal values for chan 1 & 2. Move the signal input from chan 2 to trig 3 and then to trig 4 and set the trig level for trig src 3 and trig src 4 as close as possible to the trig level used for chan 1 & 2. Change the Trig Src back to Chan 1. Now move the input cable back to Chan 2.

Press the Utility key and then press the cal menu function key (top key) and follow the instructions on the CRT (but don't AUTO-SCALE again), press the TRIG DELAY-Chan 1 function key, again the top key. As the key is pressed TRIG DELAY will be highlighted and a single channel will be presented on the display.

Press the Expand Waveform function key several times until the waveform is expanded and approximates figure 6-17. Use the entry devices and adjust the position of the signal on the X-axis so that it intersects the crossing of the graticule at center screen. The value of chan 1 trigger delay is listed at the top of the waveform display area.

Press the top function menu key and the label will change to SKEW Ch to Ch, also the chan 1 & 2 signals will be in the split screen format and should resemble figure 6-18. The chan 1 signal is in the upper half of the display and chan 2 is in the lower half. The chan 1 signal should be positioned so that it intersects the graticule crossing, this is a result of the previous chan 1 trig delay adjustment. Press the expand waveform key for an appropriate display. Use the entry devices and adjust the chan 2 waveform on the X-axis so that it intersects the graticule crossing at center screen. When you make this adjustment you are nulling the difference in signal acquisition times from chan 1 to chan 2. Chan to chan skew time is listed at the top of the waveform display area.

The next adjustment to be made is the Chan 2 TRIG DELAY. Press the top function menu key, the label for this key will change to TRIG DELAY-Chan 2 and there will be a single signal on the display similar figure to 6-17. Use the entry devices and position the displayed signal on the x-axis so that it intersects the graticule crossing at the center of the display. The ch 2 trigger delay time will be listed at the top of the waveform display area

Press the top function menu key and the label will change to TRIG DELAY-Trig 3. Connect the cable that has been attached to chan 2 to trig 3. Adjust the entry devices and move the signal on the X-axis so that it intersects the graticule at the center crossing. The value of the trig 3 delay will be listed at the top of the waveform display area.

Press the top function menu key and the label will change to TRIG DELAY-Trig 4. Connect the cable that has been attached to Trig 3 to Trig 4. Adjust the entry devices and move the signal on the X-axis so that it intersects the graticule at the center crossing. The value of trig 4 delay will be listed at the top of the waveform display area. Press the top function menu key again and the label will change to Chan 1. You may now save the cal factors by pressing the Exit Cal Menu key.

Cal factors are kept as part of the SAVE/RECALL setup and different sets of factors may be kept with each front panel setup. When the instrument is powered down these factors will be maintained in nonvolatile memory

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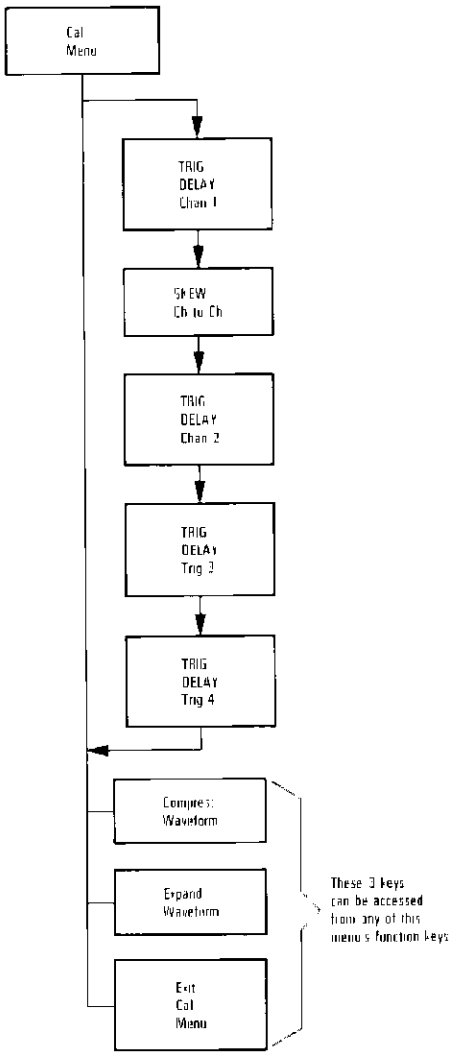


Figure 6-16. Cal Menu

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Figure 6-17. Trigger Delay

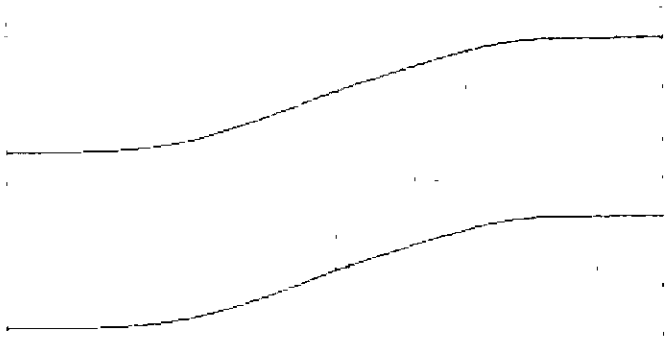


Figure 6-18. Chan to Chan Skew

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6-21. COLOR CAL MENU

The color cal menu provides a flexible system that allows you to define the 16 (0-15) colors that are available on this instrument. Colors 0-7 and 15 have specific functions on the instrument's display, colors 8-14 are not used. You may, however, use them for user definable text via HP-IB. All 16 colors can be individually modified to suit a specific need. Color selections are maintained in nonvolatile memory See figure 6-21 for a listing of the default colors and their uses.

After you have selected the utility menu and then in turn selected the color cal menu, the top key in the function menu will be the Selected Color key. When you press this key you will sequence the inverse video text field to the next color number After you have selected a color you can use the HUE, SATURATION, and LUMINOSITY functions to modify it.

The hue function allows you to change the gradation of color. The range of the hue function is from 0 to 100 with red located at 0/100, green at 33, and blue at 67. The hue can be varied by using the entry devices

The saturation function defines the percent of pure color that is to be mixed with white. The range of this function is from 0 to 100, with 0 being white (irregardless of the hue setting) and 100 being the pure color (determined by hue). Use the entry devices to change the saturation level.

The luminosity function defines the relative brightness of the color with 0 being black and 100 being maximum brightness. Luminosity is varied by using the entry devices.

The next key allows you to set all colors to their default states.

The bottom key allows you to exit the color cal menu and return to the utility menu.

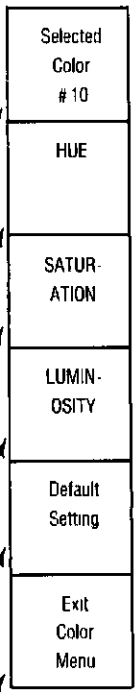


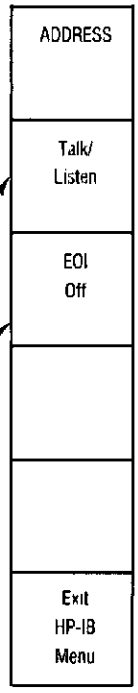
Figure 6-22 shows the HSL model (hue, saturation and luminosity) with the angular coordinate demonstrating the hue. Saturation is the height coordinate and the radial coordinate is the luminosity

6-22. HP-IB MENU

When you want to connect the 54110D to other HP-IB devices you would select the HP-IB menu. This menu allows you to establish the 54110D as a HP-IB talker, listener, or do both.

The EOI instruction can be sent at your discretion for such applications as binary dumps or when required by a controller when under program control.

When the instrument is in the Talk/Listen mode the HP-IB address can be changed by using the Entry devices. Refer to the programming section of this manual for a complete discussion of the HP-IB capabilities of the 54110D.



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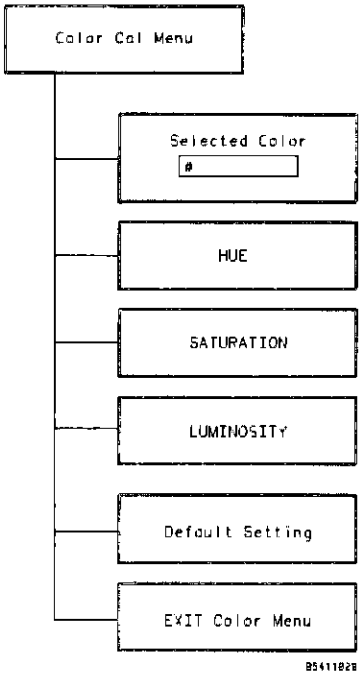


Figure 6-19. Color Cal Menu

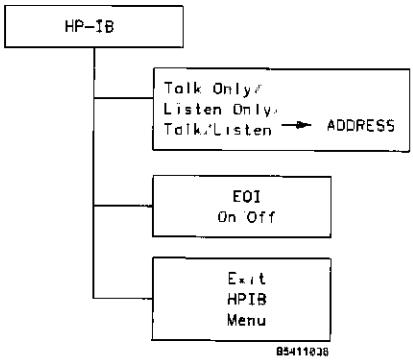


Figure 6-20. HP-IB Menu

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COLOR #	COLOR	USE	HUE	SATURATION	LUMINOSITY
0	Beige	Highlighting	11	51	100
1	Grey	Halfbright	0	0	55
2	Red	Advisory	0	100	100
3	Yellow	Chan 1	17	100	100
4	Green	Chan 2	33	100	100
5	Orange	Markers	8	100	100
6	Cyan	Stored waveforms	50	85	90
7	Magenta	Trace overlap	90	100	100
8	Pink	Not used	95	60	100
9	Lt Blue	Not used	58	40	100
10	Olive Drab	Not used	20	100	40
11	White	Not used	0	0	100
12	Brown	Not used	6	100	60
13	Blue	Not used	67	75	100
14	Mauve	Not used	83	100	100
15	Black	Background	0	0	0

Figure 6-21. Color Chart

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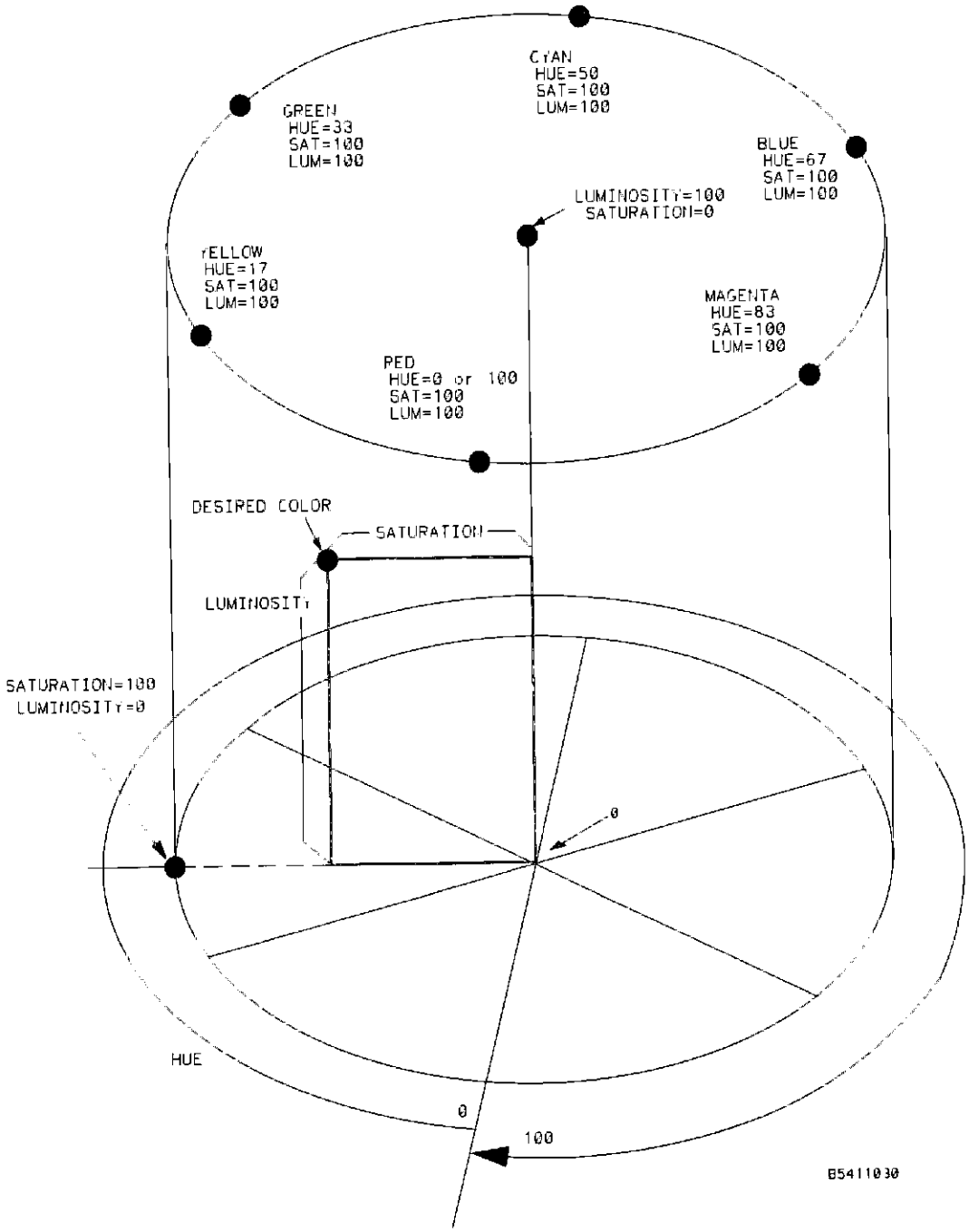


Figure 6-22 HSL Color Model

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SECTION 7
FRONT PANEL EXERCISES

7-1. INTRODUCTION

This section provides exercises that will help you to become more familiar with local (front panel operation. Section 6 includes a preliminary discussion on front panel operation and should be read before continuing with Section 7.

7-2. INPUTTING A SIGNAL

The 54110D has four inputs, two are vertical signal inputs and the third and fourth are external trigger inputs.

For the instrument to accept signals, input pods must be installed. Refer to section 3 for pod specifications. The characteristics of all inputs are dependent on the pod chosen. The appropriate input pod should be chosen after characterizing the source impedance, speed/bandwidth and magnitude of the signal to be measured.

7-3. FRONT PANEL REVIEW

Refer to figure 7-1 for a review of the front panel layout. The keys at the bottom of the CRT are referred to as the menu select keys. When one of these keys is pressed, the appropriate function menu will appear on the right side of the CRT. Additional control of the unit is available through the use of the SYSTEM CONTROL keys which are located at the top of the right side of the front panel. These SYSTEM CONTROL keys give you immediate access to those functions which are appropriate in any menu.

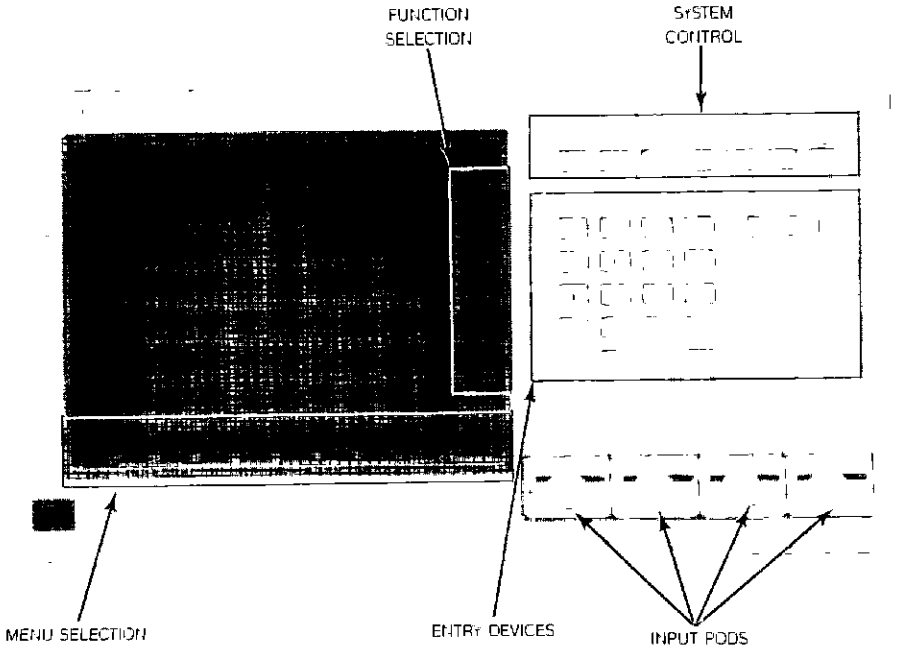


Figure 7-1. HP 54110D Front Panel

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The ENTRY devices are used to input values for variables. The input devices on this instrument include the key pad, step keys and the knob. If you need further in formation concerning the front panel refer to Section 6.

7-4. MAKE A VOLTAGE MEASUREMENT

This oscilloscope gives you the capability of making either a manual or automatic voltage measurement. In this discussion the instruments cal signal is used as the signal source. To make a voltage measurement manually you may use this procedure.

1. Connect the cal signal to channel 1.
2. Press AUTO SCALE
3. Select the Display menu
4. Insure the Display Mode is Averaged.
5. Press the Delta V menu key
6. Key the V markers on.
7. Position MARKER 1 at the top of the cal signal.
8. Position MARKER 2 at the base of the cal signal

The difference between the voltage levels of the two Vmarkers will be shown in the factors area at the bottom of the CRT labeled ΔV In this example the cal signal measured 444 mV p-p. The positive delta voltage indicates that MARKER 2 was more positive than MARKER 1. If the markers were reversed ΔV would indicate a negative voltage (see figure 7-2).

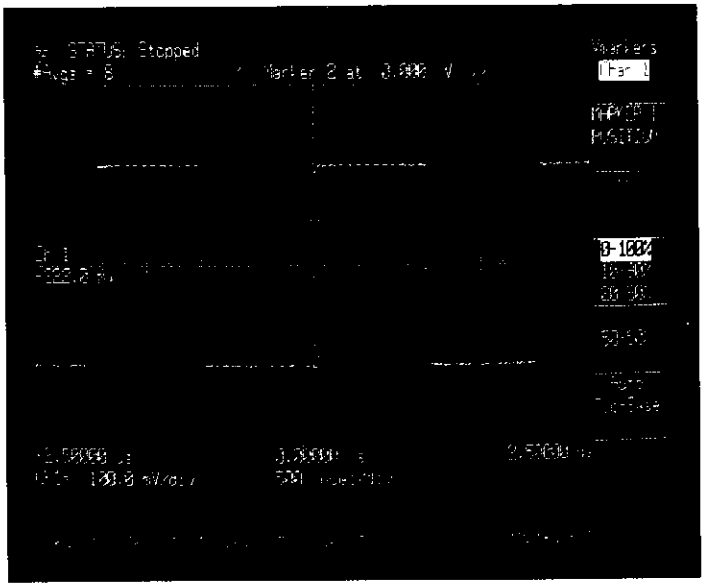


Figure 7-2. Manual Vmarker Measurement

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Another method of making this measurement would be to use the Auto Top-Base function on the Delta V menu. The instrument will make an automatic voltage measurement by evaluating a histogram of the data points that are displayed on the CRT (see figure 7-3). When the Auto Top-Base key is pressed, MARKER 2 moves to the top of the Cal signal and MARKER 1 moves to the base. ΔV will indicate approximately 444 mV, this indicates that MARKER 2 is 444 mV more positive than MARKER 1 (see figure 7-4). The results of the manual and the automated measurements in this case turned out to be identical. This is not always the case. The manual measurement is accomplished by using visual resolution and the automated results are acquired mathematically. Cal signals vary slightly from unit to unit, therefore, results may vary accordingly.

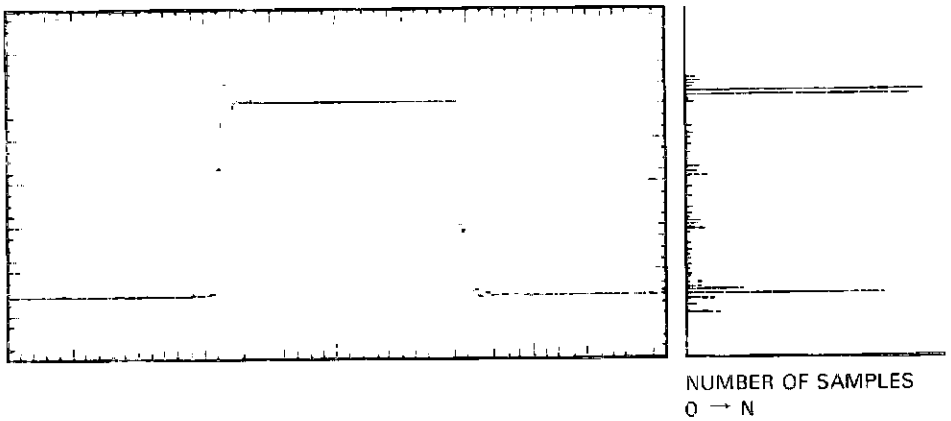


Figure 7-3. The Histogram of a Waveform

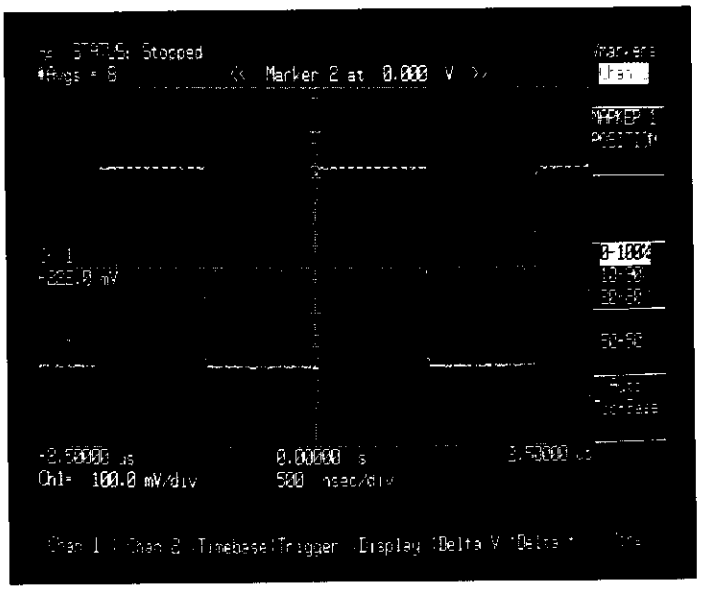


Figure 7-4. Auto Top-Base Voltage Measurement

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Another way to make voltage measurements would be to use the automated capability by using the the Peak-to-Peak Voltage function. When the Peak-to-Peak Voltage key is pressed, the unit determines the minimum and maximum voltage on the CRT, calculates the difference, and provides the answer in the factors area.

1. Press the More menu key (bottom of the CRT).
2. Select the Measure menu.
3. Press the More key (side of CRT) until the Peak-to-Peak label appears.
4. Press the Peak-to-Peak Voltage key.

Note the results in the factors are (P-P Volts). With the example unit the value was 446 mV. This is a slightly greater absolute value than we acquired when we used Auto Top-Base. This would be expected as the peak-to-peak voltage is the difference between the minimum and maximum voltages on the display and the Auto Top-Base measurement is derived from a histogram of the same data (see figure 7-5).

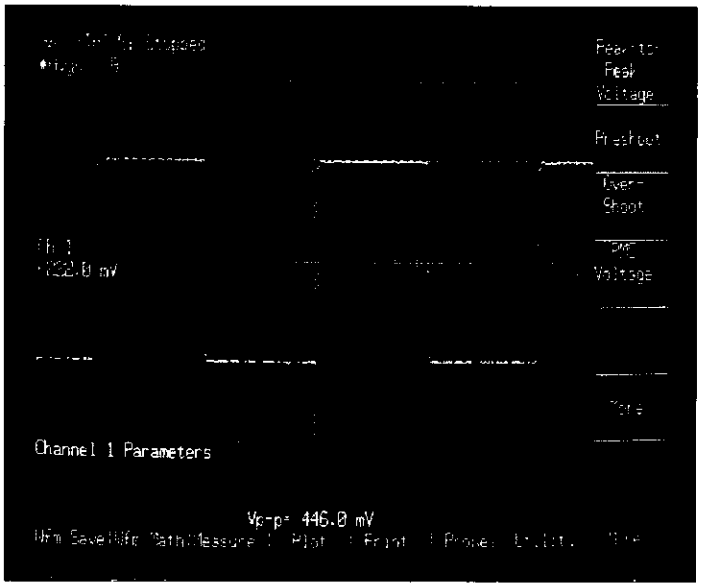


Figure 7-5. Peak-to-Peak Voltage

An important capability of the Vmarkers is that the Vmarkers can be assigned to chan 1 and chan 2 independently, i.e., marker 1 to chan 1 and marker 2 to chan 2. The next exercise will help clarify how this feature works:

1. Connect the cal signal to channel 1 & 2.
2. Press AUTO-SCALE.
3. Select the Delta V menu.
4. Turn the Vmarkers on.
5. Press the top key on the function menu twice. (Vmarkers Dual)
6. Position MARKER 1 and MARKER 2 randomly.

As the markers are moved you notice that MARKER 1 is associated with chan 1 and MARKER 2 is associated with chan 2. The DC voltage level of each marker as will as the difference between them (ΔV) is listed in the factors area. This feature allows comparisons to be made between signals on chan 1 and chan 2. To demonstrate this:

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1. Position MARKER 1 level with the top of the cal signal on chan 1.
2. Position MARKER 2 level with the base of the cal signal on chan 2.

NOTE

ΔV in the factors area lists the voltage difference between the two markers (see figure 7-6).

3. Select Chan 1.
4. Press the OFFSET function.
5. Move Chan 1 display using the entry devices.

As the chan 1 signal is positioned on the display, note that the Vmarker maintains its relative location with respect to the signal on the channel.

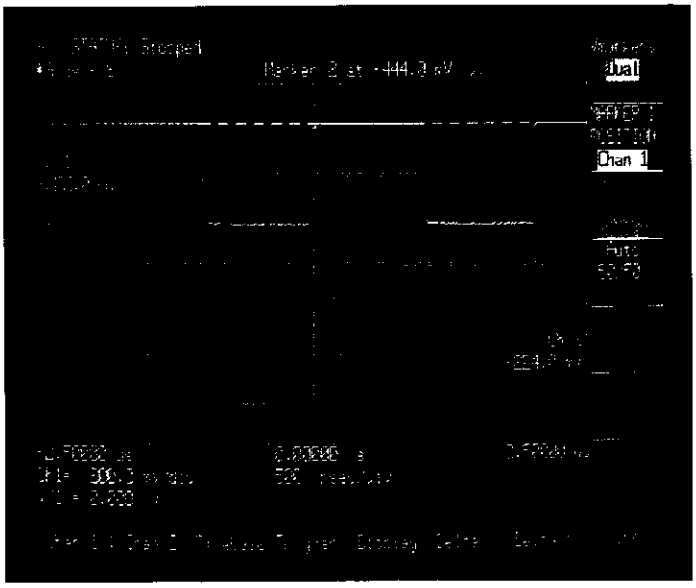


Figure 7-6. Delta Vmarkers on Split Screen.

7-5. TIME DOMAIN MEASUREMENTS

This section provides a discussion and exercises that demonstrate some of the time domain measurement capabilities of the 54110D.

The time domain is referenced to the 10 division CRT display with a resolution of 100 ps to 1 sec/div on the horizontal axis. The two time markers can be used as horizontal references to show where an automatic measurement is being made, or to relocate signals displayed time using the DELAY function; or they can be manually located on the display for timing measurements. To demonstrate the manual time interval measurement capability, complete the following exercise:

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1. Connect the cal signal to channel 1.
2. Press AUTO-SCALE.
3. Select the Delta t menu.
4. Key the Tmarkers on.

NOTE

Both Tmarkers will be located at the "0.000000S" Delay Ref. (trigger event). Auto-Scale sets the Delay Ref. at center screen.

5. Move the START MARKER to the leading edge of the first pulse.
6. Move the STOP MARKER to the trailing edge of the first pulse

The time intervals between each marker and the trigger point as well as the time interval between START MARKER and STOP MARKER to the trailing edge of the first (Δt) are listed in the factors area (see figure 7-7).

In this example the START MARKER is -2.00 us (before trigger) and the STOP MARKER is -1.00 us (before trigger) and Δt is 1 us.

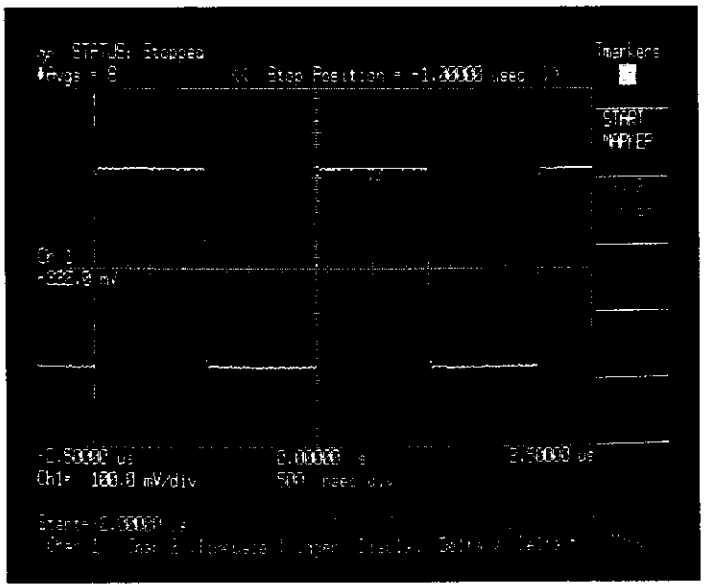


Figure 7-7. Manual Time Interval Measurement

Another method that can be used to make a time interval measurement is to take advantage of the automatic edge finding capability, which requires setting a reference with the Vmarkers for defining edges:

1. Select the Delta V menu.
2. Key Vmarkers on.
3. Press Auto Top-Base.
4. Press 50-50%.

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NOTE

Step 4 places the Vmarkers at the 50% level of the cal signal and provides references for the delta t measurements we are about to make, i.e., the unit senses the transition of the cal signal through the Vmarkers.

5. Select the Delta t menu.

NOTE

The Delta t menu has 3 additional functions; START ON EDGE, STOP ON EDGE and Precise Edge Find. These functions require the use of the Vmarkers and are only displayed when Vmarkers are on.

6 Set START ON EDGE to Pos 1.
7 Set STOP ON EDGE to Neg 1.

NOTE

When you select START ON EDGE or STOP ON EDGE as in steps 6 and 7, the first key stroke selects the function and the second changes the polarity of the edge

The unit will automatically locate the transition level (50-50%) on the first positive and negative edges and measure the time interval between the two and define the +pulse width. Check the factors area of the CRT for the results (Δt)(see figure 7-8).

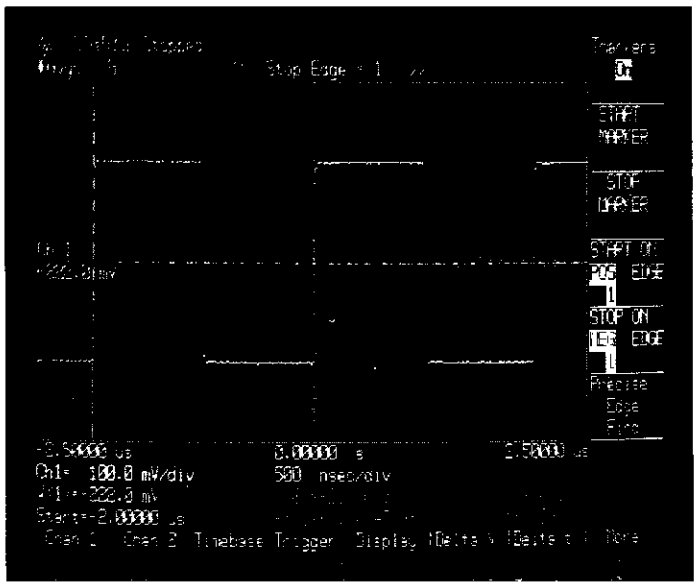


Figure 7-8. Edge Find

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When the START and STOP ON EDGE functions are used, the displayed waveform is used as the data base for developing the time interval measurements. This limits the resolution to 1/50th of a division.

Now press Precise Edge Find. This causes the unit to rescale the horizontal axis to a faster sweep speed while it locates the Vmarkers on the edge(s) of interest.

Because of the additional scaling, Precision Edge Find requires a longer period of time to acquire a result than does the START and STOP ON EDGE functions; this should be considered if throughput is a concern

Precise Edge Find uses averaging, which also makes it take longer. The number of averages selected in the Display menu will be acquired each time the timebase is rescaled to locate the edges. For greater precision, the NUMBER OF AVERAGES can be increased; for a faster result, the NUMBER OF AVERAGES can be reduced. Extremely low repetition rate signals will also slow down the precise edge finders.

To terminate the measurement routine at any time, just press any other front panel key.

Another method of measuring the +pulse width would be to use the automated capabilities available on the Measure menus.

1. Connect the cal signal to chan 1.
2. Press AUTO-SCALE.
3. Press More menu key (bottom of CRT)
4. Select Measure menu.
5. Select Fine Precision.
6. Press More (on the side of the CRT).
7. Press +Width.

The +Width value will be listed in the factors (see figure 7-9).

When any of the automated measurements in the measure menus require a time interval measurement, you have the choice making "Coarse" or "Fine" precision measurement. When a coarse measurement is executed the instrument makes the measurement on previously acquired data In most cases fine precision measurements, when executed, acquire new data and rescale the timebase for increased resolution.

NOTE

All fine precision measurements require an active signal input.

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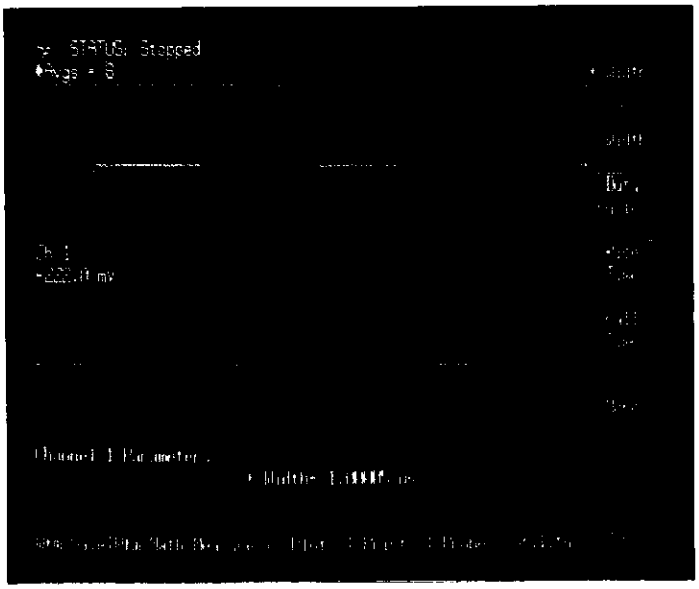


Figure 7-9. +Pulse Width

If measurement speed is a prime concern, you may make automated time interval measurements using coarse precision by setting the Precision key in the Measure menu to Coarse.

For demonstration purposes repeat the + width measurement with precision set to coarse. Notice the difference in time required for a coarse precision measurement vs. a fine precision measurement.

7-6. DELAY

The DELAY function provides horizontal windowing capability as well as calibrated pre and post triggering delays. Negative delay represents time before the trigger event and positive delay represents time after the trigger event. Try the following procedure to familiarize yourself with the DELAY function.

1. Connect the cal signal to channel 1.
2. Press AUTO-SCALE
3. Select the DELAY function.

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NOTE

In this exercise the Delay is referenced to center screen, the left or right side of the graticule could just as easily have been used as the reference.

4. Key in 2 sec delay using the key pad and the sec ENTER key. An error message will display "Value out of range.....Set to limit". The maximum + delay on this sweep speed (500 ns/div) is 1.6 sec.

5. Key in -1 second delay. Again the unit displays the error message and sets the delay to the limit. Maximum - delay on this sweep speed is 200ms.

NOTE

Maximum ± delays vary depending on sweep speeds and delay reference, e.g., on 1 sec/div sweep speed, maximum positive delay is 6 x 10E5 seconds, maximum negative delay is -10 seconds.

6. Press AUTO-SCALE.
7. Select DELAY.
8. Vary Delay by rotating the knob. CW rotation provides negative delay and CCW rotation provides positive delay.

The DELAY function allows viewing of the signal before and after the trigger event. In this last example, 1.6 seconds delay and 500 ns/div sweep speed were used. A small amount of time jitter would be obvious when viewing the delayed signal under these conditions, e.g., 1 cm of jitter represents approximately 3.2 ppm. To demonstrate the effect of time jitter, complete the following exercise

1. Connect the cal signal to channel 1
2. Press AUTO-SCALE.
3. Select the DELAY function.
4. Enter 1.6 sec. Delay using the key pad.
5. Select the display menu.
6. First view the signal in the normal mode with infinite persistence then switch the unit to the averaged mode (top key on the function menu).
7. Set Averages = 8 by using the entry devices.

NOTE

After the unit has been allowed to acquire data for a short period, the rising and falling edges of the pulse appear to slope (see figure 7-10); this is a function of the time jitter on the signal and the fact that the unit is in the averaged mode. In this example where time jitter is present and a relatively long delay is used, the averaged mode does not faithfully reproduce the input signal

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8. Change the display mode to normal

9. Set the DISPLAY TIME to Infinite using the entry devices. Notice that after several acquisitions, the leading and lagging edges are undefined (see figure 7-11). This is caused by time jitter on the input signal. Unless a signal source is extremely stable it is common to see time jitter of this magnitude when long delays are used. The sample unit that was used demonstrated approximately 500 ns time jitter with 1.6 sec delay. This technique is a perfectly valid measurement of the jitter in the source signal, which you might typically want to measure. This type of jitter measurement is made possible by the extremely stable crystal referenced timebase. See Section 3 for timebase jitter specifications.

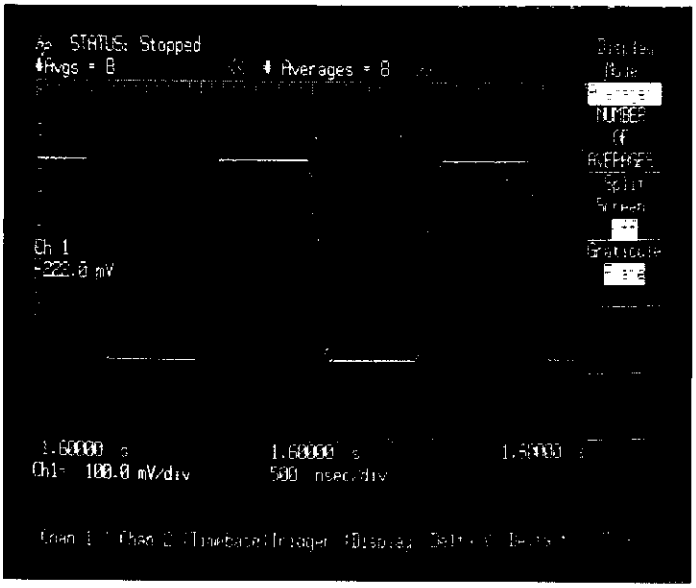


Figure 7-10. Time Jitter in the Averaged Mode

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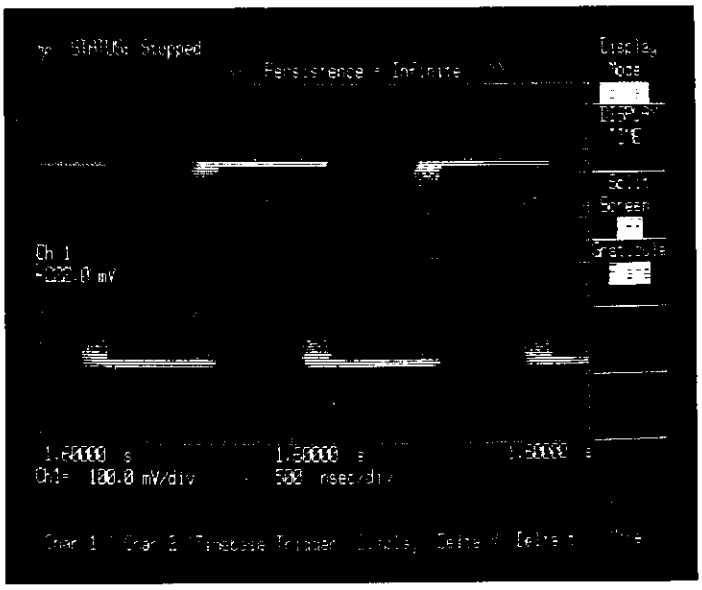


Figure 7-11. Time Jitter in the Normal Mode

Figure 7-12 compares the results obtained with the normal mode and the averaged mode when using a long delay with time jitter present.

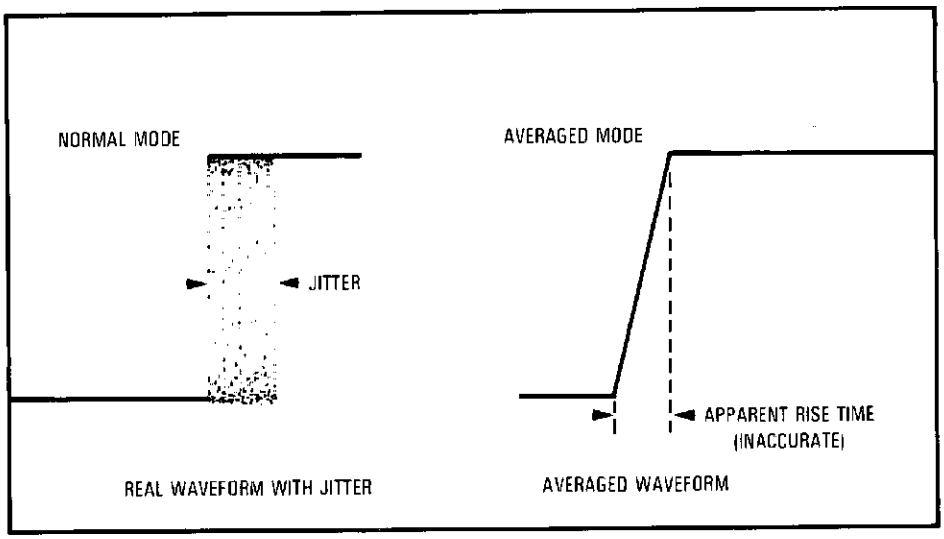


Figure 7-12. Time Jitter with Normal/Averaged Mode.

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The 54110D provides two additional techniques of delaying the display window by delaying the actual trigger; Event Delay and Time Delay. These two functions are part of the trigger menu and can be selected by pressing the trigger menu key. The are different from the Timebase delay in that they provide a trigger for the display after the Event/Time delay. This eliminates the time jitter that is seen when the timebase delay is used. Let's first look at event delay.

1. Connect the cal signal to channel 1.
2. Press AUTO-SCALE.
3. Change from Auto to Trg'd sweep.

NOTE

When AUTO-SCALE is pressed, the unit establishes itself in the auto sweep mode. If the trigger is delayed longer than approximately 50 ms, the auto sweep mode will cause the unit to sweep before the delay period has elapsed. The signal will appear untriggered (see figure 7-13). To eliminate this problem put the unit in the Trg'd mode

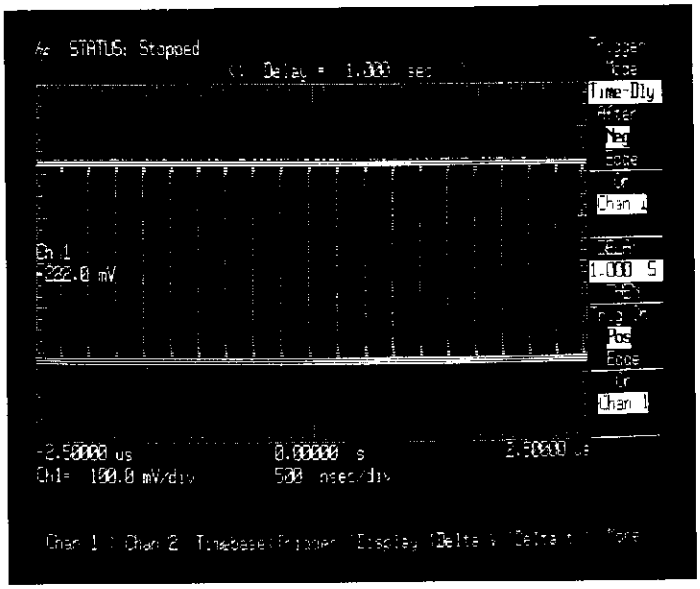


Figure 7-13. Auto Sweep Mode with Delay > 50 ms.

4. Select the Trigger menu.
5. Set the trigger mode to Event-Dly.
6. Using the function keys and entry devices, set the Event-Dly menu to read: "After Neg Edge On Chan 1, TRIG on 1,000,000 events Of Pos Edge on chan 1".
7. Press CLEAR DISPLAY

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NOTE

After a qualifying negative edge on chan 1, the unit will delay the defined number of pulses and then trigger on the last pulse. In this example the 1,000,000th pulse will be presented at center screen (if the delay is referenced to center screen). This mode would be used if it is necessary to look at a specific pulse in a train but the signal is not stable enough to use timebase delay.

The next method of delaying the display window would be Time Dly. To demonstrate time delay, perform the next exercise:

1. Connect the cal signal to channel 1.
2. Press AUTO-SCALE.
3. Select Trg'd sweep.
4. Select the Trigger menu.
5. Select the Time Dly trigger mode.
6. Using the function keys and entry devices, set the Time-Dly menu to read: "After Neg Edge on Chan 1 DELAY 1.000 S THEN Trig On Pos Edge On Chan 1".
7. Press the CLEAR DISPLAY key. In this mode the unit waits a defined period of time after a qualifying event, in this example 1 second, and then triggers on the edge selected.
8. Change the WAIT time to 0.5 sec. Notice that the acquisition rate is influenced by WAIT time because the effective trigger repetition rate is limited by WAIT time.

The Time-Delay mode would be used to view a signal that occurs a relatively long time after a sync signal. This would eliminate the time jitter (induced by the input signal) that would be present if the timebase delay were used. Event-Delay accomplishes essentially the same thing as Time-Delay except that events are used to delay the display window. The effect is similar when using either mode, i.e , the affect of time jitter is the source signal is eliminated.

The timebase delay on the 54110D is always referenced to the trigger edge that is generated in a particular trigger mode. Trigger delay, both event and time, should not be confused with the timebase delay as they are independent functions. Event-Delay and Time-Delay modes are a means of selecting which edge on the signal is used as a reference for timebase delay.

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7-7. TRIGGER

In this section some of the triggering capabilities of the 54110D will be discussed.

The edge mode is similar to the trigger on a conventional oscilloscope. The trigger level can be defined, the polarity of the trigger can be selected and the source of the trigger can be determined. This instrument has two external trigger inputs and provides four trigger sources.

In the pattern mode this instrument provides 4-channel pattern recognition capability. Try this exercise to demonstrate some of the triggering capabilities of the edge mode:

1. Connect the cal signal to channel 1 & 2.
2. Press AUTO-SCALE The unit will establish itself in the split screen mode with chan 1 at the top and chan 2 at the bottom of the display. Chan 1 will be defined as the trigger source
3. Select the trigger menu.
4. Select TRIG LEVEL. The trigger level will be indicated by a horizontal line through the chan 1 signal (see figure 7-14).
5. Change the trigger level by rotating the knob.

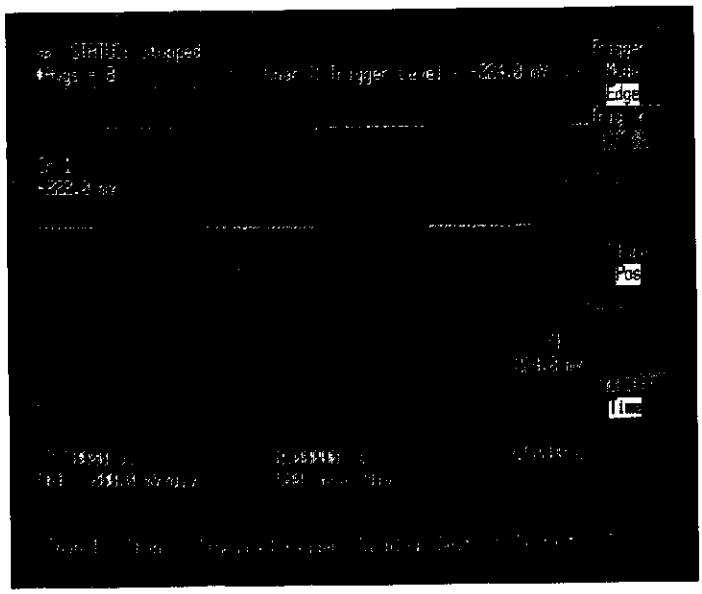


Figure 7-14. Split Screen with Trigger on Chan 1

NOTE

If the trigger level trace is moved above or below the chan 1 signal, the signals on chan 1&2 will loose sync. The step keys and the key pad may also be used to change the trigger level.

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6. Select chan 2 as the Trig Src. The unit is now triggering on chan 2. The line showing the trigger level will be on the chan 2 display. The trigger level on chan 2 can be varied by using the input devices (see figure 7-15). The trigger level function is shown at the top of the waveform display area and at the bottom of the display in the factors area.

7. Select Trig 3 as the trig src. Notice that the signals are untriggered.

8 Move the chan 1 input to trig 3 (trigger 3 input). The initial trigger level for trig 3 will be 0 V and the signal on the display will not be triggered. The cal signal is negative and does not cross through the 0 V threshold and therefore does not cause a trigger.

9. Vary trig level 3 until the signal on chan 2 triggers. Trig 3 is now being used as a trigger for the signal on chan 2. You could also use trig 4 as a trigger source in the edge mode.

NOTE

If any of the previously used inputs are selected as the trigger source, the trigger level remains where previously set for that source.

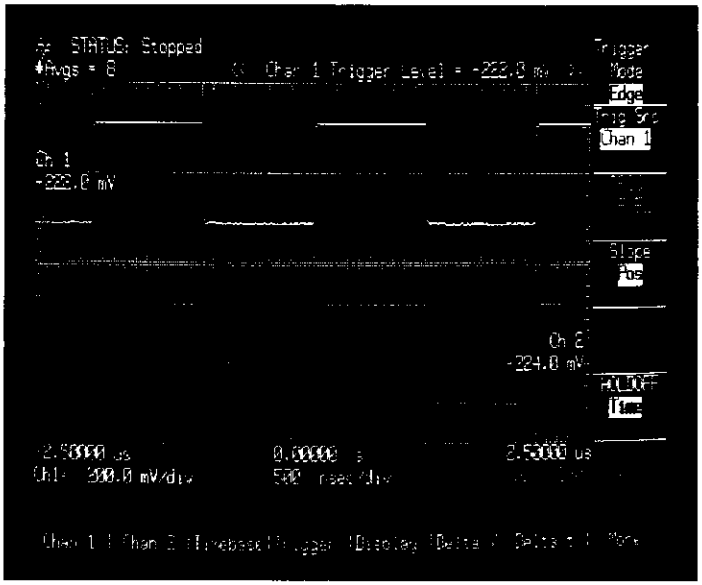


Figure 7-15. Split Screen with Trigger on Chan 2

7-8. PATTERN MODE

In the pattern trigger mode each input is converted to a digital signal which is high, or true, when the input signal is above its trigger threshold and is low, or false, when below its trigger threshold. The trigger can then be set to occur when a pattern of signal levels, relative to each inputs' trigger threshold, becomes true or false.

When the Pattern mode is used, insure that the trigger level for each input is adjusted so that the input signals cross each respective trigger level during transition. This is done in the edge mode. It should be noted that each input has a separately adjustable trigger level and is independent of the other. This feature allows mixing different types of logic signals. Use this example to become more familiar with the pattern trigger mode:

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1. Connect one cal signal to channel 1 using a m metre BNC cable.
2. Connect the other cal signal to channel 2 using 3 metres of BNC cable. 2 metres will work as well but will not give as much signal delay on channel 2.
3. Press AUTO-SCALE
4. Set the sweep speed to 5 ns/div.
5. Select the display menu and set split screen off.
6. Select the trigger menu.
7. Select the edge trigger mode.
8. Select chan 2 as the trigger source.

NOTE

In figures 7-16 and 7-17, the signal path for chan 2 is approximately 2 meters longer than that of the signal path for chan 1. This provides the time differential between the two signals

9. Set trigger mode to pattern.
10. Set Trig On PATTERN to read: "HHXX".

    H = High State (above trigger threshold)

    L = Low State (below trigger threshold)

    X = Don't Care

11. On the trigger menu insure "When Entered" is set. With the instrument in this configuration it will generate a trigger on the last edge that makes the pattern HHXX. In this example the positive edge on chan 2 is the trigger.

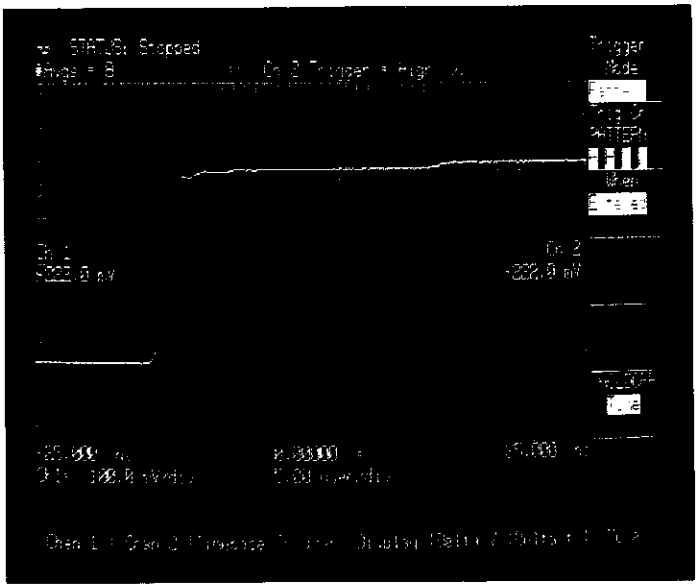


Figure 7-16. Pattern When Entered "HHXX"

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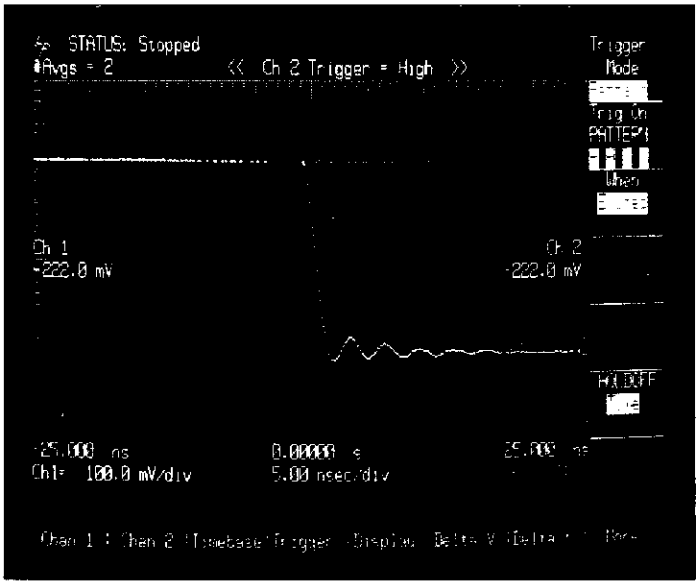


Figure 7-17. Pattern When Exited

This menu allows triggering when entering or exiting a defined logic pattern. If the When Entered function is selected, the unit will trigger on the last pulse edge that makes the pattern true (see figure 7-16). If the When Exited function is selected, the unit will trigger on the first pulse edge that makes the pattern false (see figure 7-17)

This trigger mode would be an advantage while troubleshooting logic circuitry, or any other application where it would be desirable to make parametric measurements while using logic sources for a trigger. In addition to the When Entered/Exited functions, time qualification is provided for the Pattern mode When Present> and When Present<. The When Present> mode allows the user to specify that the trigger pattern must be present for a minimum period of time (that the user defines) before being accepted as a trigger. If the pattern does not remain true long enough it will be ignored. The When Present < mode is just the opposite. Here the pattern will generate a trigger only if it remains true for less than the time specified. If the pattern is true longer than this time it will be ignored Both modes generate a trigger when the pattern is exited, only if the time qualifier is true. The range of the time qualifier is from 10 ns to 5 sec.

For the case of the simplest pattern, HXXX, the pattern is true when chan 1 is high and it is false when chan 1 is low. The time qualification can then be used to trigger on pulses that are wider than a specified time and ignore shorter ones (When Present>) or it can be used to trigger on pulses that are shorter than the time qualifier and ignore the longer ones (When Present<). Use this exercise to become familiar with the time qualification feature

1. Connect the cal signal to channels 1&2.
2. Press AUTO-SCALE
3. Select the Trigger menu
4. Select the Pattern Trigger mode.
5. Set the Trig On PATTERN to read HHXX.
6. Select the When Present> function
7. Set TIME to 1 5 us. This requires that the pattern be present for greater than 1.5 us to generate a trigger. In this example this will not be true as the + portion of the cal signal is approximately 1 us duration.

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8. Set TIME to .5 us. The display will now trigger.

The ability of this unit to qualify the trigger pattern with a min-max time interval provides an excellent technique for glitch detection.

7-9. STATE MODE

The next trigger mode is the State mode. This mode allows using simple edge detection combined with pattern recognition to generate a trigger. When this mode is selected, one of the four inputs is chosen as the edge source and the user determines a 3-bit pattern defined over the remaining three inputs.

A trigger will be generated when an appropriate (±) edge occurs only when the pattern is true (When Present) or false (When Not Present) as specified by the user. The State function differs from the Pattern Entered/Exited function in that the trigger is generated from a specified edge source for State, while in the Pattern Entered/Exited mode any input can initiate a trigger if it causes the pattern to be true/false To become more familiar with this function, complete the following exercise

1. Connect the cal signal to channels 1&2.
   For chan 1 use a 1 metre cable, for chan 2 use 2 or 3 metres.
2. Press AUTO-SCALE
3. Select the trigger menu.
4. Set the trigger mode to state.
5. Set Trig On Edge to Pos.
6. Set On Chan When to Chan 1.
7. Set PATTERN to -HXX
   - = Input being used for edge source.
   X = Don't care
   H = High State (above trigger threshold)
   L = Low State (below trigger threshold)
8. Set the Present/Not Present function to Not Present.
   The display should be triggered.

With the instrument in this configuration it will generate a trigger on a positive edge on chan 1 if chan 2 is low. Change Not Present to Present -- the display will loose it's trigger.

7-10. DISPLAY

The display menu provides control of how data is displayed on the CRT:

1 Whether data on the display is Normal or Averaged.
2. The type of graticule that is to be used, grid, frame or axis.
3 The format of the display, split screen On/Off.

7-11. NORMAL MODE

When the Normal mode is used, high speed A to D converters digitize the incoming signal and write it to a display memory that in turn provides information to the CRT. The data points that are acquired from the A to D converters are displayed on the CRT for a user-defined period of time from 200 ms to Infinity. To become more familiar with the Normal mode functions, complete the following exercise:

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1. Connect the cal signal to channel 1.
2. Press AUTO-SCALE.
3. Select the Display menu.
4. Select the Normal mode.
5. Set DISPLAY TIME to 200 ms. Data points written on the CRT will fade shortly thereafter unless they are refreshed by new input data.
6. Select the Timebase menu.
7. Change the sweep speed to 100 ps/div. This faster sweep speed allows the user to
8. more easily see the effects of changing the DISPLAY TIME. Select the display menu.
9. Change DISPLAY TIME to 1 sec Notice the change in persistence.
10. Change DISPLAY TIME to 11 sec. The unit will now have infinite persistence (any DISPLAY TIME greater than 10 sec defaults to Infinite).

The infinite persistence mode causes all acquired data to remain on the CRT until the function is changed.

Long persistence times work well for capturing low repetition rate, relatively fast or narrow (low duty cycle) signals. Infinite persistence also allows viewing worst case jitter, noise, and timing variations; or to view extremely infrequent glitches or other anomalies.

To see the effect of persistence on a low rep rate signal connect the cal signal to chan 1 and press AUTO-SCALE, go to the timebase menu and use 500 ns/div sweep speed with 1.6 sec DELAY. Return to the display menu and vary the DISPLAY TIME from 200 ms to 11 sec notice the differences.

In the infinite persistence mode the data points will remain on the display until the CLEAR DISPLAY key is pressed or until the display is moved with an instrument control such as, sweep speed, vertical sensitivity, or trigger level. Move one of these controls while in the infinite mode and notice the results.



Figure 7-18. Averaged Mode (8 Averages)

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7-12. AVERAGED

As the input signal is digitized, each data point is assigned a time coordinate relative to the trigger. In the averaging mode the unit calculates the average of the most recent data point with the previous values in the same time bucket. You can define the number of data points that are to be averaged from 1 to 2048. Each average is calculated from data acquired for each time slot--data for adjacent time slots is not averaged together.

If 8 is chosen for the number of averages, 1/8 of the vertical value of each new data point will be added to 7/8 of the value previously in the time bucket. If 16 averages had been selected, 1/16th of the new data would be averaged with 15/16ths of the previous value.

The effect of using the average mode is to cancel out all phenomena that is not related to the trigger event, i.e., noise and nonrecurring events.

To demonstrate some of the differences between the normal mode and the averaged mode, complete the following exercise:

1. Connect the cal signal to chan 1
2. Press AUTO-SCALE
3. Select the display menu.
4. Select the averaged mode.
5. Set NUMBER OF AVERAGES to 8. (See figure 7-18).
6. Select the normal mode (see figure 7-19). Compare figures 7-18 and 7-19 and notice the reduction of noise on the averaged display. The larger the number of averages the greater the reduction of the displayed noise and the longer it takes to respond to any change in the input signal.

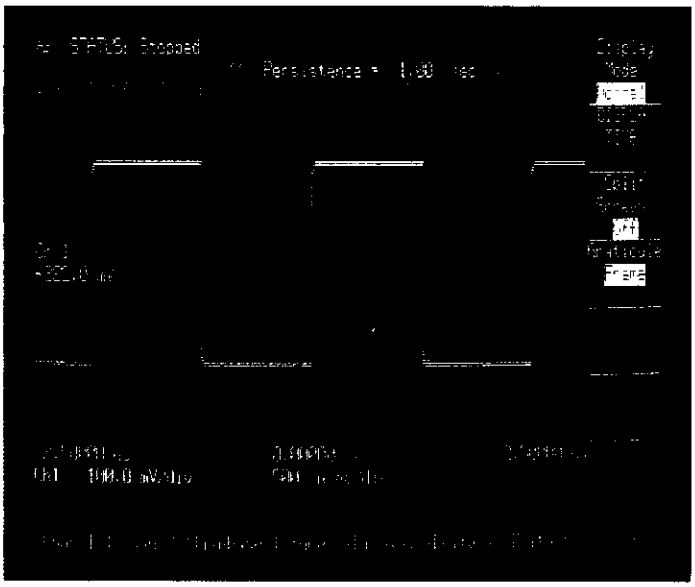


Figure 7-19. Normal Mode

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The next exercise shows the effect of the averaged mode and the use of the averaged mode in conjunction with the Magnify mode.

1. Connect the cal signal to chan 1
2. Press AUTO-SCALE
3. Select the display menu.
4. Select the normal mode.
5. Select chan 1 menu.
6. Select the magnify mode and adjust the WINDOW SIZE and POSITION so that the window is near the top of the cal signal (see figure 7-20).
7. Turn magnify on (see figure 7-21)
8. Select the display menu.
9. Set NUMBER OF AVERAGES = 2 (see figure 7-22).
10. Change NUMBER OF AVERAGES = 512 (see figure 7-23). Notice that with a greater NUMBER OF AVERAGES there will be less noise on the signal and the display will appear to be more stable.

NOTE

With only 1 or a small number of averages, the quantization levels of the A/D converter are also very evident. With a larger number of averages, the actual usable resolution increases as the display fills between quantization levels with averaged data.

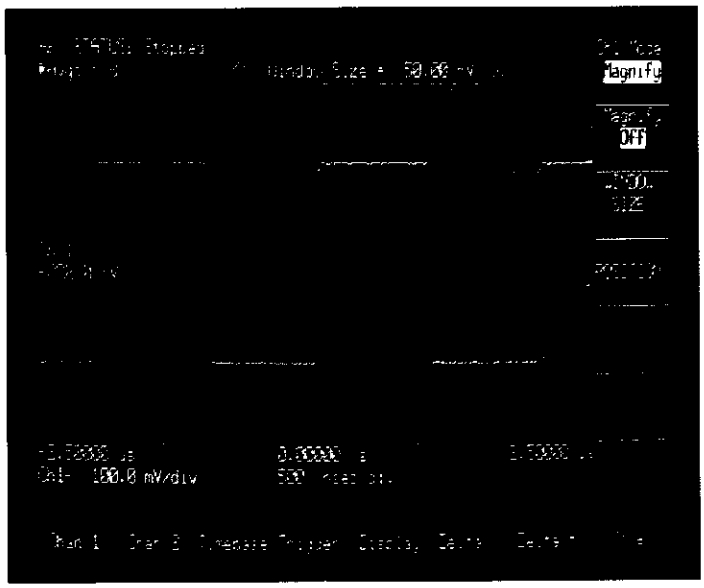


Figure 7-20. Magnify Window in the Normal Mode.

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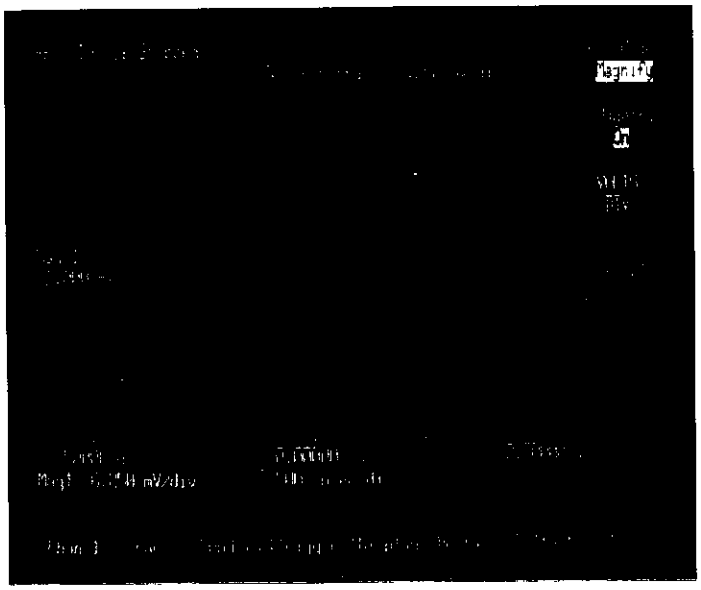


Figure 7-21. Magnify Using Normal Mode

The next exercise will help illustrate how averaging works.

1. Connect the cal signal to chan 1.
2. Press AUTO-SCALE.
3. Select the display menu.
4. Set NUMBER OF AVERAGES to 256.
5. Remove the cal signal from chan 1 and notice the reaction of the display.

As the input signal was removed, the existing values in each time bucket are now being averaged with the new data which is "0". If the number of averages were reduced, the display would converge to the new signal levels in a shorter period of time.

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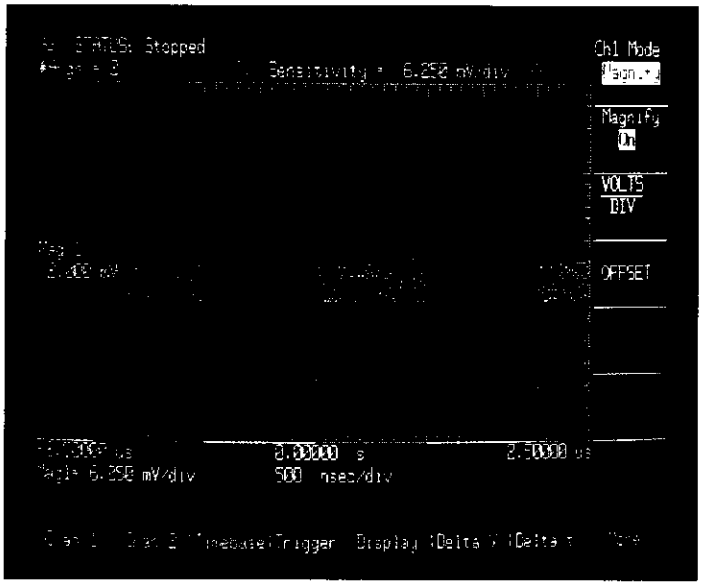


Figure 7-22. Magnify in the Averaged Mode with 2 Averages

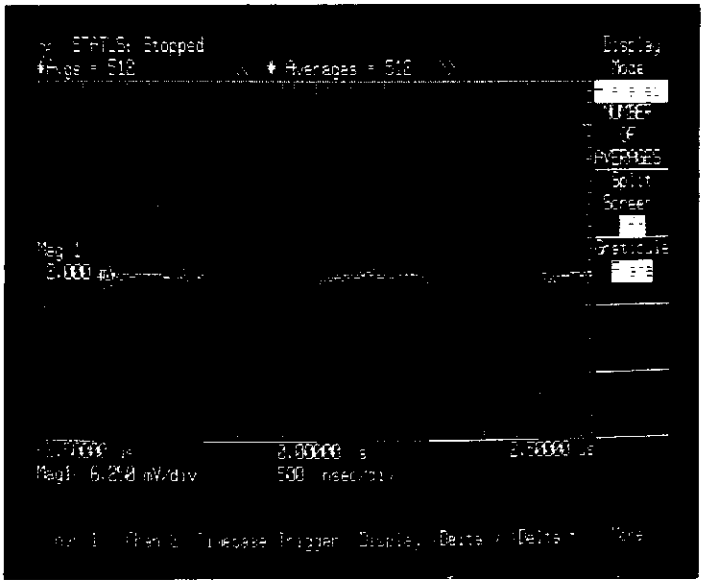


Figure 7-23. Magnify in the Averaged Mode with 512 Averages

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7-13. PROBES

This instrument provides you with the capability of changing the attenuation factor on any input. When this attenuation factor is changed, the actual voltage division ratio of the inputs does not change; however, the scale factors in firmware that are used to generate the answers for the automated parametric measurements and voltage related items on the screen are modified appropriately.

The variable Atten (attenuation) factors would be used so that the display factors would accurately reflect the actual voltage levels at the source when accessory probes or voltage dividers are being used.

The Atten factors are saved with the rest of the front panel setup when the Save/Recall registers are used. When the power is cycled the Atten Factors will automatically set themselves to the value appropriate for the input pod that is installed in each input. For the 54002A and the 54003A, the Atten Factors would be set to 1:1. If the 10:1 accessory probe that is supplied with the 54003A is used, set the Atten Factor for that input to 10:1 This will insure that the correct answers are provided in the factors area on the screen, and that the vertical scale factors previously set (VOLTS/DIV and OFFSET) are correctly referenced to the probe tip

When the 54001A active prove is used, the Atten Factors will automatically be set to 10:1 when the instrument power is turned on Use the following exercise to see the effect of changing the Atten Factors:

1. Connect the cal signal to chan 1 and press AUTO-SCALE.
2. Select the Delta V menu.
3. Select the Vmarkers for Chan 1 and press Auto Top-Base. Notice the voltage readings in the factors area.
4. Select the Probes menu The Ch1 Atten Factor will be set to 1.1 (if the 54002A or 54003A is used).
5. Set the Ch1 Atten Factor to 10:1 by using the entry devices. Notice that as the Atten Factor is changed, the voltage readings in the factors area will change to reflect the new ratio
6. Connect the cal signal to chan 1 and trig 3.
7. Select the trigger menu.
8. Set the Trig Src to Trig 3 and the TRIG LEVEL to approximately -200 mV (the signal should be triggered).
9. Return to the probes menu and set the Trig 3 PROBE ATTEN to 10:1.

NOTE

Factors can also be used, if you have a known source, to calibrate out systematic errors in gain and attenuation ratio of the 54001A, 54003A or other divider probes. The Atten Factor could be arbitrarily set to yield the correct answer.

10. Return to the trigger menu and notice that the trig 3 level reflects the new ratio.
11. Select the Measure menu and press the All function key. Notice that all of the voltage related factors reflect the 10:1 ratio that has been chosen.

The range of the Atten Factor is from 1 to 1000. The knob and the step keys will give you up to 3 digits of resolution and the key pad provides up to 4 digits of resolution for setting Atten Factor.

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7-14. WAVEFORM MATH

This oscilloscope gives you the capability of defining the two waveform functions using the signals on channel 1 and/or 2 and/or the four waveform memories. After you have defined a waveform function and displayed it you can make automated or manual measurements on that function following the same rules as you would use measuring a signal on a channel.

To demonstrate some of these capabilities perform the following exercises:

1. Connect a cal signal to chan 1 using a 1 metre BNC cable, connect the other cal signal to chan 2 using a 2 metre cable. The time delay between the signals that is created by the unequal cables is approximately 6.4 ns. (See figure 7-24)
2. Press the more key.
3. Select the Wfm Math menu
4. Insure Func 1 (function 1) is the selected function (see figure 7-25)
5. Insure that Func 1 is set to Chan 1 - Chan 2 with func 1 keyed on.

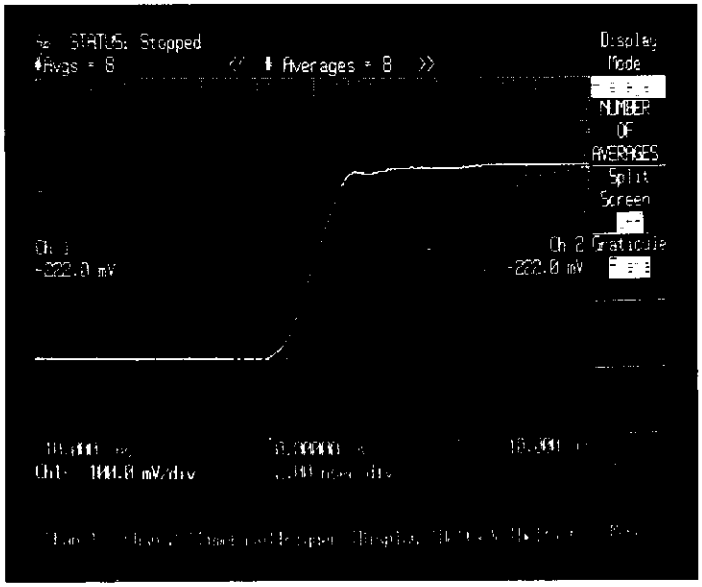


Figure 7-24. Time delay Chan 1 to Chan 2

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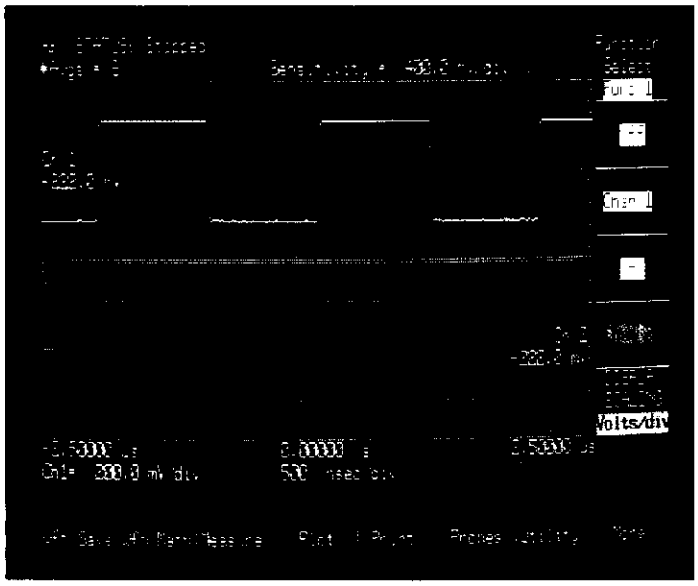


Figure 7-25. Selecting Func 1.

NOTE

Func 1 should be displayed in the top half of the split screen. At this sweep speed Func 1 appears as a narrow voltage spike occurring at the same time as the leading and trailing edges of the cal signal (see figure 7-26). The difference between chan 1 and chan 2 is created by the fact that the signal arrives at the chan 2 input after the signal arrives at chan 1. Remove the input from chan 2 and notice the effect on Func 1. To continue with this exercise reconnect chan 2 to the cal signal.

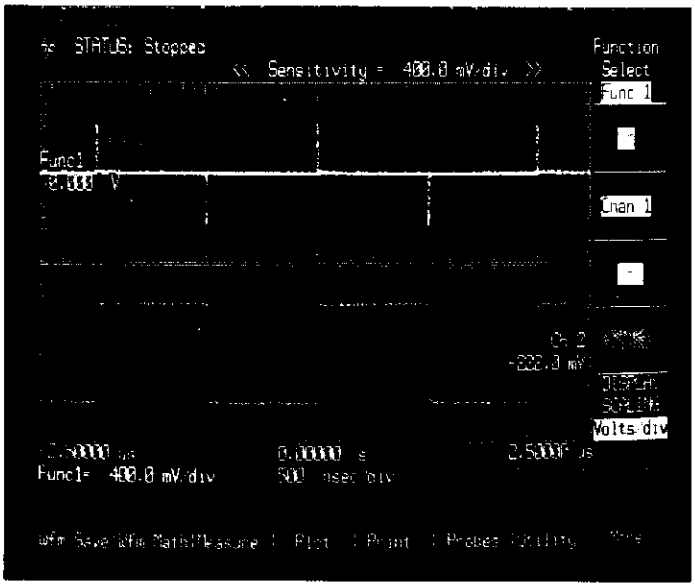


Figure 7-26. Func 1

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6. Set the function select to Func 2.
7. Define func 2 as chan 1 + chan 2 and key Func 2 on
8. Press the more key and select the timebase menu.
9. Set the sweep speed to 5 ns/div.

NOTE

The display should resemble figure 7-27 with func 1 (chan 1 - chan 2) at the top of the display and func 2 (chan 1 + chan 2). If you has stored one of these functions in a waveform memory, mem 1-4 could have been used as an operand instead of chan 1 or 2.

This instrument also has the capability of making automated measurements on func 1 & 2. This next exercise demonstrates making automated measurements on these function. Leave the instrument configured the same as it was for the previous exercise, that is, cal signals connected to chan 1 and 2 with 1 metre cable on chan 1 and a 2 metre cable on chan 2. Func 1 = chan 1 - chan 2 and func 2 = chan 1 + chan 2. The display should resemble 7-27. Do not change any of the instrument settings until you start the next exercise.

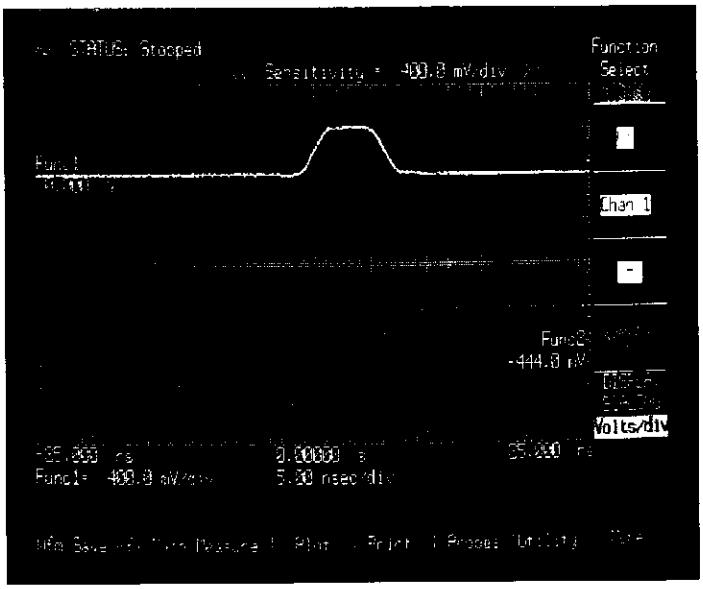


Figure 7-27 Waveform Math Func 1 & 2.

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This exercise shows you how to make some of the automated measurements on func 1 & 2.

1. Select the timebase menu and set the sweep speed to 500 ns/div.
2. Press the more key and select the measure function menu.
3. Insure that func 1 is the selected measure source. (top key)
4. Press the more key on the function menu twice, this will place the Peak-to-Peak voltage key at the top of the function menu.
5. Press the peak-to-peak key and notice Vmarker appear on the func 1 trace. Press this key repeatedly. (see figure 7-28)

NOTE

As you continue to press the peak-to-peak voltage key, notice that the Vmarkers change levels. This is caused by the fact that the voltage measurement is being made on the last acquired data and because of the narrowness of func 1 with respect to the display window. Because of this the sampled data may or may not occur at the actual peak value of the waveform. To increase the accuracy and repeatability you can increase the sweep speed.

6 Press the more key (bottom of CRT).
7. Select the timebase menu and set the sweep speed to 5 ns/div.

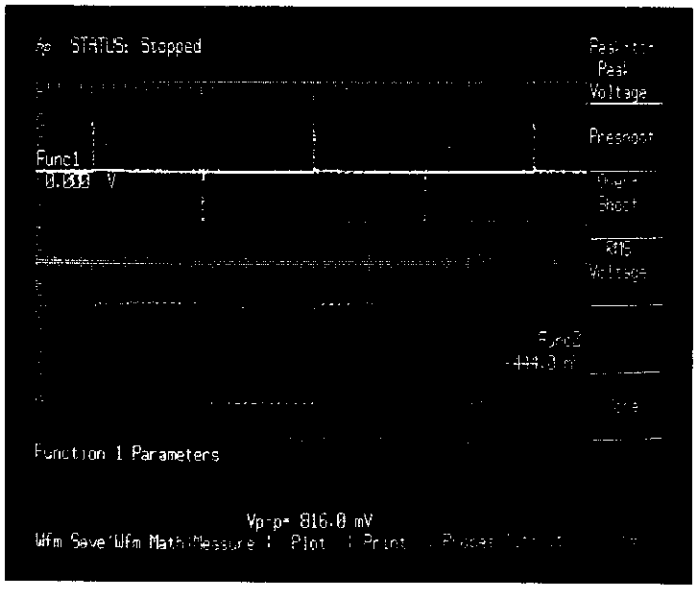


Figure 7-28. Measuring Func 1 Parameters

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8. Return to the measure menu and measure "All" parameters on func 1 (see figure 7-29). The instrument will make the measurements that it can using the the displayed data.
9. Select func 2 and again measure "All" parameters (see figure 7-30).

Notice that after the automated measurements were performed on func 2 that the Delta t and Delta V markers moved from func 1 to func 2.

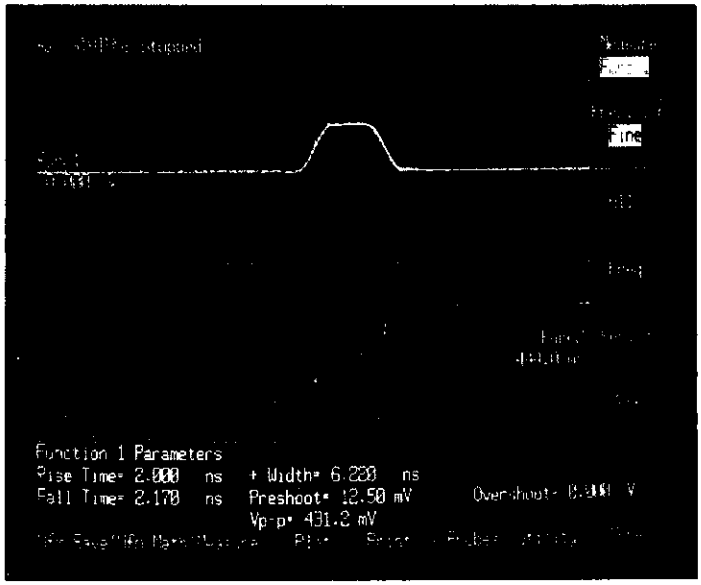


Figure 7-29. Automated Measurements on Func 1.

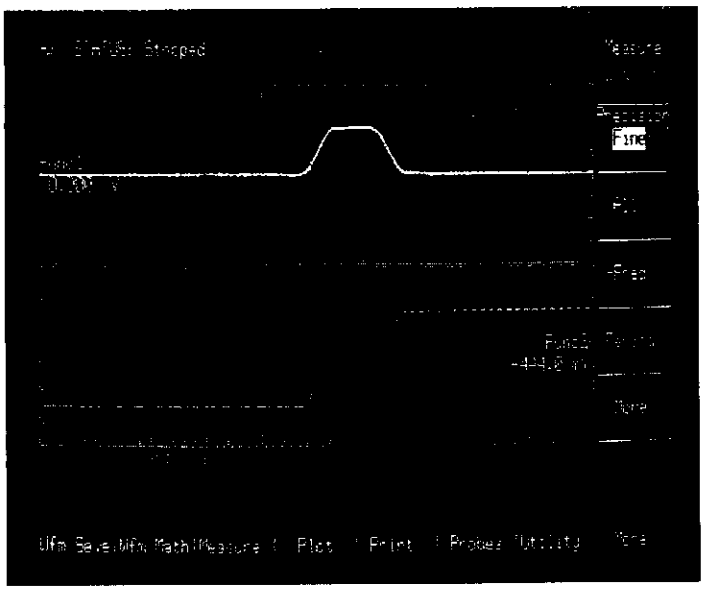


Figure 7-30. Automated Measurements on Func 2.

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The 54110D also provides the capability of making an X,Y or Versus measurements where channels 1 or 2, or memories 1,2,3 or 4 can be used as operands. In the following exercise, a versus measurement is made between channel 1 and channel 2. NOTICE THE REQUIREMENT FOR PRECISE TIME RESOLUTION ON THE WAVEFORM EDGES WHEN YOU ARE MAKING A VERSUS MEASUREMENT.

1. Place a BNC tee on a cal signal output on the rear panel of the instrument and connect 1 metre BNC cables from the tee to channel 1 and channel 2 inputs. It is important that these BNC cables be of equal length so that the cal signal arrives at the channel 1 & 2 inputs at approximately the same time.

2. Press AUTO-SCALE and perform a front panel calibration on the instrument. This nulls the differences between the trigger and data acquisition paths. See Section 6-21 for this procedure. See, also, Appendix B for a discussion of this topic.

3. Select the Display menu and set Mode to Normal and the Display Time to Infinite.

4. Select the Timebase menu and set the SEC/DIV to 1 nsec/div (Figure 7-31). Notice the more precise time resolution (number of data points) on the edges of the signal as compared to the low timing resolution.

5. Press the More key and select the Wfm Math menu. Turn Func 1 On and select Chan 1 Versus Chan 2 (See Figure 7-32).

If waveform edges are measured with inadequate time resolution, the resulting versus waveform will not look as predicted. For Example:

6. Turn Func 1 off and select the Timebase menu. Set the SEC/DIV to 10 nsec/div (see Figure 7-33). Note the near vertical edges, (this indicates lower time resolution)

7. Return to the Wfm Math menu and turn Func 1 on. The resulting chan 1 versus chan 2 (top of Figure 7-34) shows reclangular steps that occur when insufficient edge resolution is used. This is a result of the random repetitive sampling technique used in the 54110D, where by, many voltage points can be taken in the same time interval (as referenced to the trigger). Channel to channel timing skew may further aggravate this situation. To eliminate this phenomena, you should increase time resolution on the edges as shown in figures 7-31 and 7-32. These expanded waveforms allow for more data points on the given waveforms. The increased number of data points on the waveforms reduce the potential for inaccuracies.

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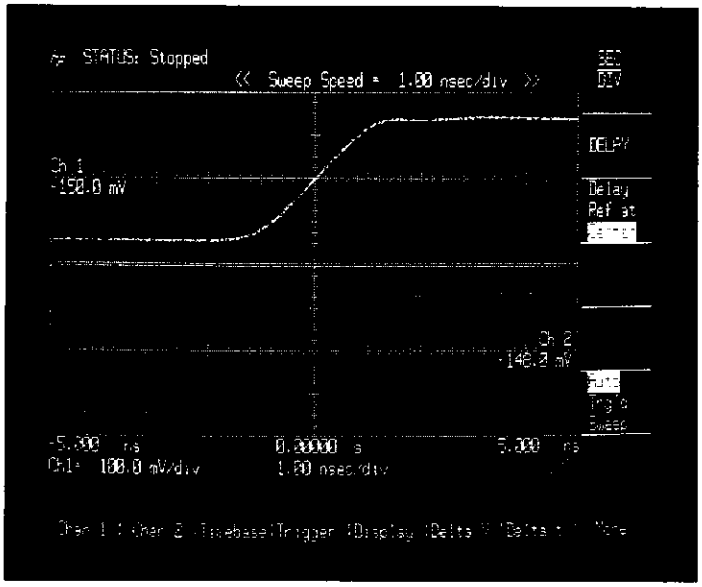


Figure 7-31. Precise Timing Resolution on Channels 1 & 2.

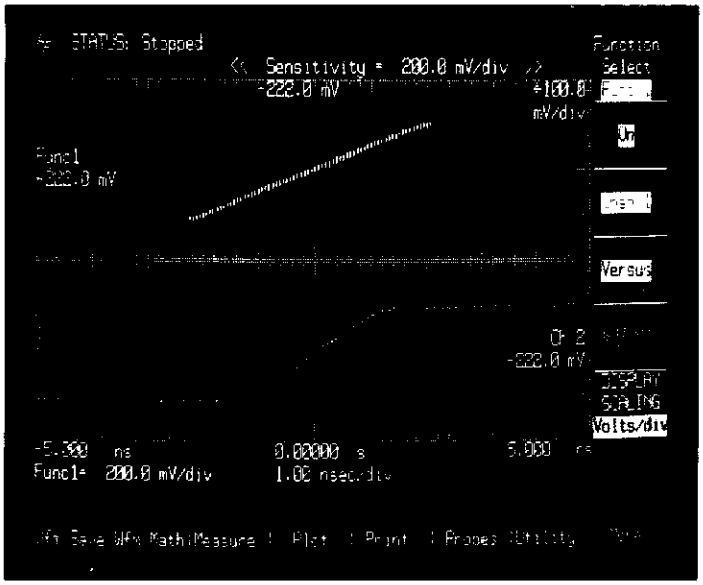


Figure 7-32. Chan 1 Versus Chan 2 with Precise Timing Resolution.

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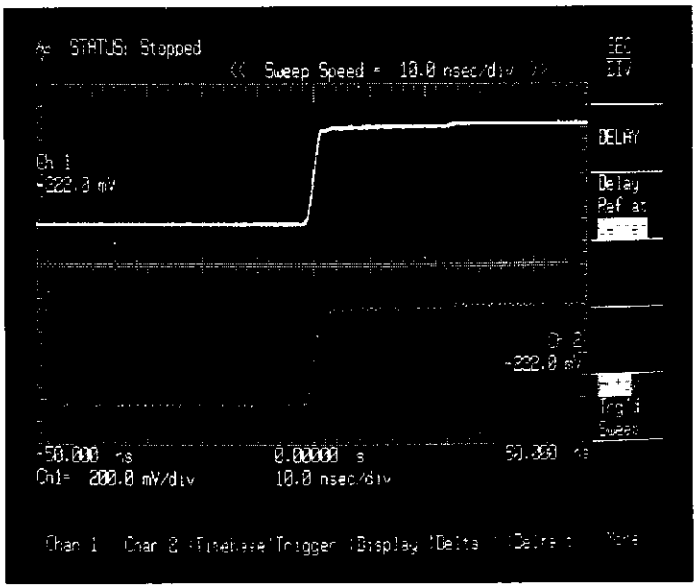


Figure 7-33. Low Timing Resolution on Channels 1 & 2.

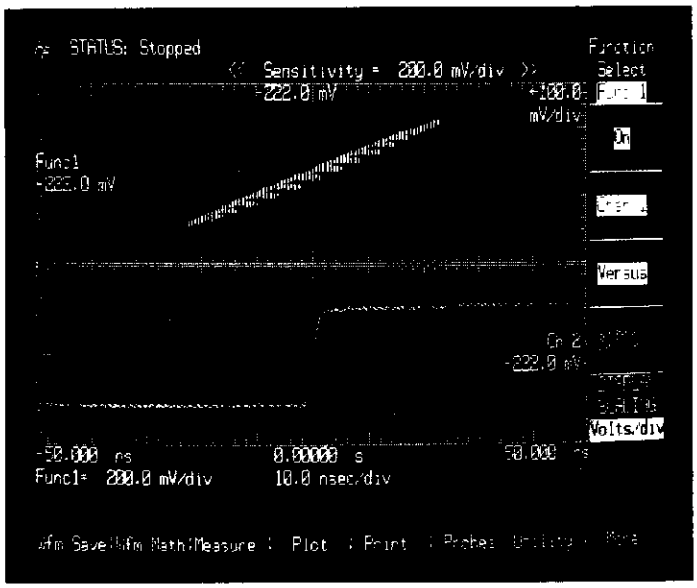


Figure 7-34 Chan 1 Versus Chan 2 with Low Timing Resolution.

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The calibration menu contains an adjustment for nulling the timing skew of channel 2 with respect to channel 1. The following exercise demonstrates how the channel-to-channel skew adjustment can effect waveform math functions:

1. Connect a BNC tee to a cal signal output on the rear panel of the instrument and connect 1 metre BNC cables from the tee to channel 1 and channel 2 inputs. It is important that these BNC cables be of equal length so that the cal signal arrives at the channel 1 & 2 inputs at approximately the same time.
2. Press AUTO-SCALE.
3. Select the Utility menu.
4. Press the Cal menu function
5. Press the top function key twice (SKEW Ch to Ch) will be selected.
6. Use the key pad and set the Ch to Ch SKEW to 10 ns.
7. Press the Exit Cal Menu Key.
8. Select the Timebase menu.
9. Set the sweep speed to 25 ns/div.
10. Press the STOP/SINGLE system control key.
11. Press the CLEAR system control key.
12. Press the STOP/SINGLE key to initiate a single acquisition. See Figure 7-35

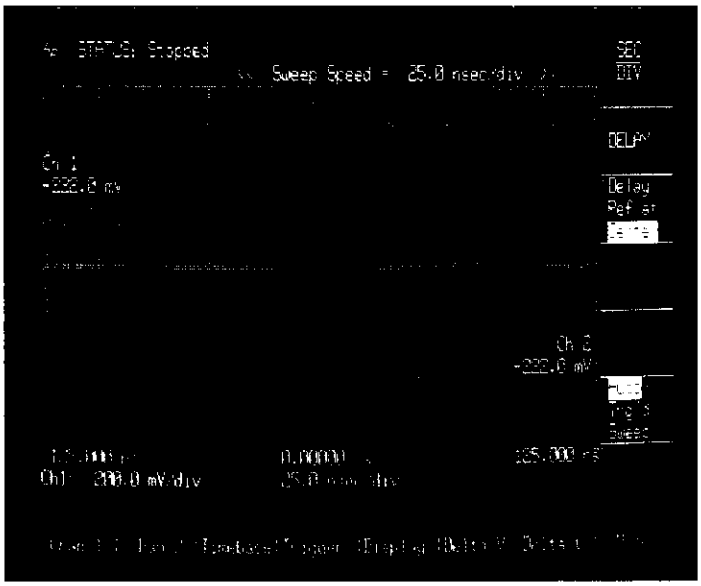


Figure 7-35. Effects of Ch to Ch SKEW on Waveform Math.

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The minimum sampling interval is 25 ns therefore will be 10 points displayed there will be 10 data points displayed on each channel and they will be one division apart. The data points for channel 2 were acquired at the same time as the channel 1 data points but are offset by 10 ns because of the channel to channel skew setting. (Press the RECALL key and the 1 key to restore the channel to channel skew cal factor once the display has been evaluated).

When the waveform math functions are used the screen is divided into 500 time buckets. Each pixel column on the screen corresponds to a time bucket. A function which has two operands is performed by matching the data points of one operand with the corresponding data points of the other.

There are several waveform math applications where non-zero channel to channel skew settings can effect the results.

1. A **single shot** measurement on a waveform function using two channels such as Channel 1 + Channel 2 may result in not displaying a waveform. This will occur when the data points acquired for Channel 1 do not correspond in time with the data points acquired for Channel 2.

2. **Common noise on differential signals** may not always cancel when when Channel 1 - Channel 2 function is used. This happens when the Channel 1 data points are matched with Channel 2 data points acquired on another sweep. This effect can be minimized by setting the display mode to Averaged.

3. **An untriggered Channel 1 versus Channel 2** function may result in a misleading display. Again, this happens when data points acquired for Channel 1 on one sweep are matched with data points from Channel 2 acquired on another sweep. In an untriggered mode there is no timing relationship between each sweep.

These effects are less pronounced at slower sweep speeds and disappear at sweep speeds slower than 2 μs/div. At 2 μs/div sweep speed and slower more than 500 data points are acquired on each acquisition

When making these measurements, it may be necessary to set the channel to channel skew to 0. This will allow the data acquired for channel 1 to align with the data acquired for channel 2 for each sweep.

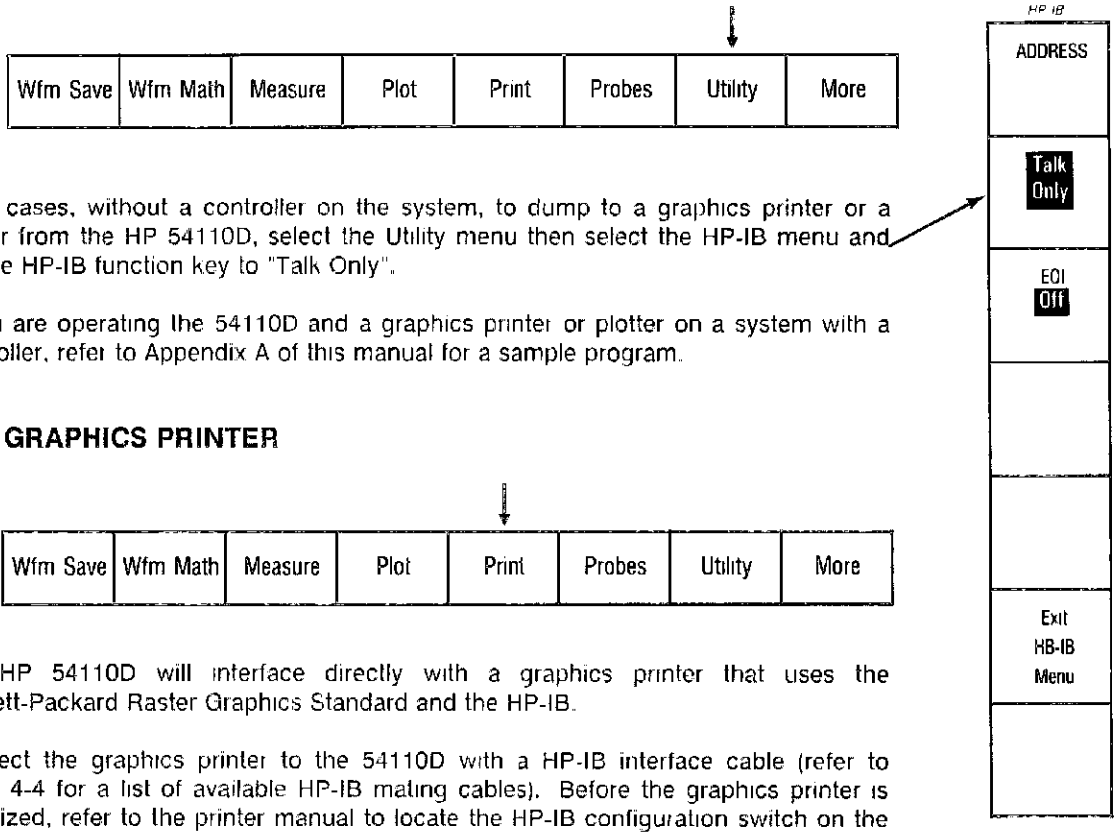
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SECTION 8
MAKING A HARDCOPY

8-1. INTRODUCTION

The HP 54110D has the capability of making a hardcopy dump to various HP-IB graphics printers and plotters without the use of a controller. This section will show how to use the HP 54110D with the graphics printers and plotters.

8-2. SETTING UP THE HP 54110D



In all cases, without a controller on the system, to dump to a graphics printer or a plotter from the HP 54110D, select the Utility menu then select the HP-IB menu and set the HP-IB function key to "Talk Only".

If you are operating the 54110D and a graphics printer or plotter on a system with a controller, refer to Appendix A of this manual for a sample program.

8-3. GRAPHICS PRINTER

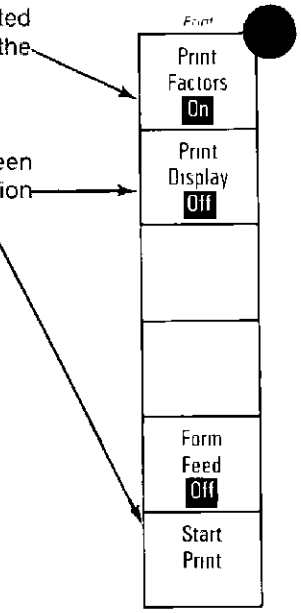
The HP 54110D will interface directly with a graphics printer that uses the Hewlett-Packard Raster Graphics Standard and the HP-IB.

Connect the graphics printer to the 54110D with a HP-IB interface cable (refer to figure 4-4 for a list of available HP-IB mating cables). Before the graphics printer is energized, refer to the printer manual to locate the HP-IB configuration switch on the printer and set the LISTEN ALWAYS(LISTEN ONLY) switch to the true (1) position. It is important that you set this switch before power is applied to the printer as most printers only read these switch settings when the power is first applied. If the switch settings have been changed, the printer must be turned off for several seconds and then back on before printing.

After the HP 54110D has been connected to the graphics printer and the configuration switch has been set to the LISTEN ALWAYS mode, select the Print menu on the HP 54110D.

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The print menu will be displayed on the right side of the CRT. The factors (listed below the signal display area) and the Display can be printed separately or at the same time depending of whether they are keyed On or Off



Data from all sources, i.e., the active display, or the the factors area, that have been selected, will be printed when the Start Print key is pressed. Waveform acquisition stops while print data is output to the printer.

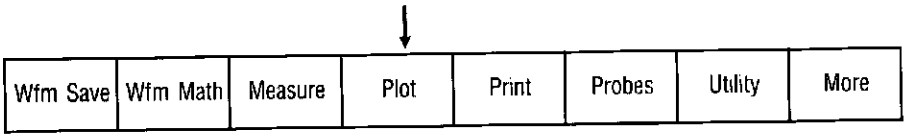
If you chose to stop the print while it is in process, press the Abort Print key.

8-4. COMPATIBLE PRINTERS

The Hewlett-Packard printers that are compatible with the 54110D include:

HP 2225A	HP 2932A	HP 9876A
HP 2671G	HP 2933A	
HP 2673A	HP 2934A	

8-5. PLOTTERS



The HP 54110D will interface directly with plotters that use the HEWLETT-PACKARD GRAPHICS LANGUAGE (HP-GL) and a HP-IB interface.

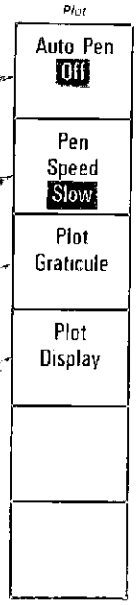
The HP 54110D must be in the "Talk Only" mode when making a graphics dump to a plotter. The status of the HP-IB on the HP 54110D is listed at the top of the display when you are in the Print or Plot menus; "Talk Only", "Listen Only", or the HP-IB address will be listed if the unit is in the Talk/Listen mode. The status of the HP-IB interface can be changed if you select the HP-IB menu.

The plotter must be in the Listen Always (Listen Only) mode. Check the plotter manual for the location of the HP-IB configuration switch and set the Listen Always switch to the true(1) position. Set this switch before the plotter is energized as most plotters read these switch settings when the power is first applied.

Connect the HP 54110D and the plotter using one of the HP-IB interface cables listed in figure 4-4.

After the HP 54110D is connected to the plotter and set to the correct HP-IB configuration for each instrument, select the Utility menu then select the Plot menu. Once this is done, the Plot function menu will be displayed at the right of the CRT.

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When the Auto Pen function is On, a new pen will be selected when a different function is chosen to be plotted, if the plotter has multi-pen capability. If Auto Pen is Off, the plotter will not load or change pens when the Plot function is selected. In this case, it will be necessary for the operator to load a pen before starting the plot.

The next function key, Pen Speed, allows you to select Fast or Slow, if the plotter in use has this feature. Slow is normally chosen when making transparencies For best results when using Leroy pens use the slow pen speed.

The next key allows you to plot the displayed graticule including the display factors at the bottom of the CRT.

When Plot Display is selected, all on-screen waveforms will be output to the plotter. This does not include the graticule or the display factors.

If the Display menu is in the Averaged mode, the output from the HP 54110D will cause the plotter to draw a continuous line plot of the active display.

If the Display menu is in the Normal mode the output from the HP 54100D is formatted such that the plotter will plot the waveform(s) in a pixel format, i.e., dot by dot if you are plotting an active display

Waveform memories will always be plotted with a continuous line and pixel memories are always plotted dot by dot.

While a plot is being accomplished you can stop the plot by pressing the Abort Plot key. If you would like to stop for a moment and then continue, press the Pause/Continue.

8-6. COMPATIBLE PLOTTERS

The Hewlett-Packard plotters that are compatible with the 54110D include:

HP 7470A	HP 7580B
HP 7475A	HP 7585B
HP 7550A	HP 7586A
HP 7480A	HP 7090A
HP 9872T	

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SECTION 9
REMOTE OPERATION

9-1. INTRODUCTION

This section discusses the remote operation of the 54110D over the Hewlett Packard Interface Bus (HP-IB). With the exception of the line switch, all the front panel functions and some instrument features that are remote only operations can be controlled by sending the appropriate commands over the HP-IB.

In this manual 54110D program codes are listed in ASCII code. Table 9-1 lists ASCII characters and some commonly used equivalent codes.

For additional information concerning HP-IB, refer to IEEE std. 488-1978 or the identical ANSI Standard MC1.1, "IEEE Standard Digital Interface for Programmable Instrumentation".

9-2. HP-IB COMPATIBILITY

The 54110D's HP-IB compatibility as defined in the IEEE std. 488-1978 appears in table 9-2.

Twelve HP-IB Meta messages are listed in the left hand column of table 9-2. The most significant of these is the Data message as they contain the program codes that set the instruments mode of operation.

9-3. HP-IB STATUS

The status of the 54110D's HP-IB interface is shown on the CRT by the HP-IB status message. This message describes the remote/local status, address status, and whether or not the instrument is requesting service via the SRQ control line.

9-4. REMOTE MODE

The 54110D communicates over HP-IB in both the local and remote modes. In the remote mode, all front panel controls except the LINE switch and the LOCAL key are disabled. When Local Lockout is enforced the LOCAL key is also disabled.

The 54110D can be addressed to listen or talk while in the remote mode. When addressed to listen, the instrument automatically stops talking and responds to Data messages. When addressed to talk, the instrument stops listening and sends either a Data message or the Status Byte. Whether addressed or not, The 54110D responds to the Local, Local Lockout, Clear Lockout/Set Local, Trigger, and Abort Messages. The instrument may also output a Require Service Message.

The local to remote mode change is accomplished when a remote message is sent to the 54110D. This message contains two parts:

- Remote enable (REN) bus control line true
- Device listen address (MLA) received once while REN is true.

All instrument settings remain unchanged with the local-to-remote transition. The local-to-remote transition disables the front panel with the exception of the power switch and the LOCAL key.

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Table 9-1. Commonly Used Code Conversions

HP-IB		ASCII	Decimal	Binary	Octal	Hexa-decimal	HP-IB		ASCII	Decimal	Binary	Octal	Hexa-decimal
Addressed Command Group (ACG)	GTL	NUL	0	00 000 000	000	00	Talk Address Group (TAG) Note 2	T0	@	64	01 000 000	100	40
		SOH	1	00 000 001	001	01		T1	A	65	01 000 001	101	41
		STX	2	00 000 010	002	02		T2	B	66	01 000 010	102	42
		ETX	3	00 000 011	003	03		T3	C	67	01 000 011	103	43
	SDC	EOT	4	00 000 100	004	04		T4	D	68	01 000 100	104	44
	PPC	ENQ	5	00 000 101	005	05		T5	E	69	01 000 101	105	45
		ACK	6	00 000 110	006	06		T6	F	70	01 000 110	106	46
		BEL	7	00 000 111	007	07		T7	G	71	01 000 111	107	47
	GET	BS	8	00 001 000	010	08		T8	H	72	01 001 000	110	48
	TCT	HT	9	00 001 001	011	09		T9	I	73	01 001 001	111	49
		LF	10	00 001 010	012	0A		T10	J	74	01 001 010	112	4A
		VT	11	00 001 011	013	0B		T11	K	75	01 001 011	113	4B
		FF	12	00 001 100	014	0C		T12	L	76	01 001 100	114	4C
		CR	13	00 001 101	015	0D		T13	M	77	01 001 101	115	4D
		SO	14	00 001 110	016	0E		T14	N	78	01 001 110	116	4E
		SI	15	00 001 111	017	0F		T15	O	79	01 001 111	117	4F
Universal Command Group (UCG)	LLO	DLE	16	00 010 000	020	10		T16	P	80	01 010 000	120	50
		DC1	17	00 010 001	021	11		T17	Q	81	01 010 001	121	51
		DC2	18	00 010 010	022	12		T18	R	82	01 010 010	122	52
		DC3	19	00 010 011	023	13		T19	S	83	01 010 011	123	53
	DCL	DC4	20	00 010 100	024	14		T20	T	84	01 010 100	124	54
	PPU	NAK	21	00 010 101	025	15		T21	U	85	01 010 101	125	55
		SYN	22	00 010 110	026	16		T22	V	86	01 010 110	126	56
		ETB	23	00 010 111	027	17		T23	W	87	01 010 111	127	57
	SPE	CAN	24	00 011 000	030	18		T24	X	88	01 011 000	130	58
	SPD	EM	25	00 011 001	031	19		T25	Y	89	01 011 001	131	59
		SUB	26	00 011 010	032	1A		T26	Z	90	01 011 010	132	5A
		ESC	27	00 011 011	033	1B		T27	[	91	01 011 011	133	5B
		FS	28	00 011 100	034	1C		T28	\	92	01 011 100	134	5C
		GS	29	00 011 101	035	1D		T29	]	93	01 011 101	135	5D
		RS	30	00 011 110	036	1E		T30	^	94	01 011 110	136	5E
		US	31	00 011 111	037	1F		UNT	_	95	01 011 111	137	5F
Listen Address Group (LAG) Note 1	L0	SP	32	00 100 000	040	20	Secondary Command Group (SCG) Note 3	S0	`	96	01 100 000	140	60
	L1	!	33	00 100 001	041	21		S1	a	97	01 100 001	141	61
	L2	"	34	00 100 010	042	22		S2	b	98	01 100 010	142	62
	L3	#	35	00 100 011	043	23		S3	c	99	01 100 011	143	63
	L4	$	36	00 100 100	044	24		S4	d	100	01 100 100	144	64
	L5	%	37	00 100 101	045	25		S5	e	101	01 100 101	145	65
	L6	&	38	00 100 110	046	26		S6	f	102	01 100 110	146	66
	L7	'	39	00 100 111	047	27		S7	g	103	01 100 111	147	67
	L8	(	40	00 101 000	050	28		S8	h	104	01 101 000	150	68
	L9	)	41	00 101 001	051	29		S9	i	105	01 101 001	151	69
	L10	*	42	00 101 010	052	2A		S10	j	106	01 101 010	152	6A
	L11	+	43	00 101 011	053	2B		S11	k	107	01 101 011	153	6B
	L12	,	44	00 101 100	054	2C		S12	l	108	01 101 100	154	6C
	L13	-	45	00 101 101	055	2D		S13	m	109	01 101 101	155	6D
	L14	.	46	00 101 110	056	2E		S14	n	110	01 101 110	156	6E
	L15	/	47	00 101 111	057	2F		S15	o	111	01 101 111	157	6F
	L16	0	48	00 110 000	060	30		S16	p	112	01 110 000	160	70
	L17	1	49	00 110 001	061	31		S17	q	113	01 110 001	161	71
	L18	2	50	00 110 010	062	32		S18	r	114	01 110 010	162	72
	L19	3	51	00 110 011	063	33		S19	s	115	01 110 011	163	73
	L20	4	52	00 110 100	064	34		S20	t	116	01 110 100	164	74
	L21	5	53	00 110 101	065	35		S21	u	117	01 110 101	165	75
	L22	6	54	00 110 110	066	36		S22	v	118	01 110 110	166	76
	L23	7	55	00 110 111	067	37		S23	w	119	01 110 111	167	77
	L24	8	56	00 111 000	070	38		S24	x	120	01 111 000	170	78
	L25	9	57	00 111 001	071	39		S25	y	121	01 111 001	171	79
	L26	:	58	00 111 010	072	3A		S26	z	122	01 111 010	172	7A
	L27	;	59	00 111 011	073	3B		S27	{	123	01 111 011	173	7B
	L28	<	60	00 111 100	074	3C		S28	|	124	01 111 100	174	7C
	L29	=	61	00 111 101	075	3D		S29	}	125	01 111 101	175	7D
	L30	>	62	00 111 110	076	3E		S30	~	126	01 111 110	176	7E
	UNL	?	63	00 111 111	077	3F		S31	DEL	127	01 111 111	177	7F

NOTES
1. L<n>=MLA assigned to device number <n>
2. T<n> = MTA assigned to device number <n>
3. Meaning defined by Primary Command Group code

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Table 9-2. HP-IB Message Reference Table

HP-IB Message	Applicable	Instrument Response	Related Commands and Control Lines	Interface Functions
Data	Yes	All front panel, menu, and remote functions except LINE switch. Also, all instrument settings may be read via the HP-IB	DAB MLA EOI UNL EOS MTA UNT OTA	L3 T5
Trigger	Yes	Responds as if the "RUN" System command were issued.	GET MLA	DT1
Clear	Yes	Responds by: - Terminating bus communication - Clearing serial poll bits - Clearing input and output buffers - Clearing error queue and key register - Stopping measurements and acquisitions.	DCL SDC	DC1
Remote	Yes	Enabled to remote mode when the REN bus control line is true. However, it remains in local until it is addressed to listen the first time.	REN MLA	RL1
Local	Yes	Returns from remote to local when it receives the Local message or the LOCAL key is pressed Settings remain unchanged after the remote-to-local transition.	GTL MLA	RL1
Local Lockout	Yes	When in remote, and local lockout is in effect, the front panel is disabled. Only the system controller can return the instrument to local.	LLO	RL1
Clear Lockout Set/ Local	Yes	Returns to local and local lockout is clear when the REN bus control line goes false.	REN	RL1
Pass/ Take Control	No	The controller subset is not implemented.	TCT	C0
Require Service	Yes	Sets the SRQ line true when one of the service request conditions occur, if it has been enabled to send the RQS message for that condition.	SRQ	SR1

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Table 9-2 HP-IB Message Reference Table (continued)

HP-IB Meta Message	Applicable	Instrument Response	Related Commands and Control Lines	Interface Functions
Status Byte	Yes	Responds to a Serial Poll Enable (SPE) bus command by sending an 8-bit byte when it is addressed to talk. Bit 6 (RQS bit) is true if the 54100A/D has set the SRQ bus control line true. The byte is cleared after it is read by the HP-IB controller if the RQS bit was set.	SPE SPD STB	T5
Status Bit	No	Does not respond to a parallel poll.	PPE PPC PPD PPU	PP0
Abort	Yes	Is unaddressed to listen or talk.	IFC	T5 L3

The unit must be in the Talk/Listen mode before the local to remote transition can be made.

The 54110D supports the following HP-IB interface functions: SH1, AH1, T5, TE0, L3, LE0, SR1, RL1, PP0, DC1, DT1, C0, E1.

9-5. LOCAL MODE

When the 54110D is in the local mode all the front panel controls are operational and the instrument will not respond to input data over the bus. If the unit is addressed to talk it can send data messages and the status byte. Whether addressed or not the 54110D will respond to the remote, local, local lockout, clear lockout/set local, trigger and abort messages. The unit can also output a require service message in the local mode.

This instrument always switches to local from remote whenever it receives the local message (GTL) or the clear lockout/set local message. The clear lockout/set local message sets the remote enable control line (REN) false. If the unit is in the local lockout mode the LOCAL key on the front panel will be disabled.

The instrument's settings remain unchanged during remote-to-local transition. The "Remote" indication on the HP-IB status line on the CRT will disappear as the remote-to-local change is made.

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9-6. LOCAL LOCKOUT

If the unit was under remote (program) control and the front panel LOCAL key were inadvertently pressed the instrument would return to local control. Data and/or settings could be changed. To prevent this you may use the local lockout message. This command allows return-to-local only under program control.

NOTE

Return-to-local can be accomplished by cycling the power switch, however, this technique has two potential disadvantages:

- *The system controller may loose control of the instrument.*
- *Other HP-IB conditions reset to default states at power up.*

9-7. ADDRESSING

If the bus is in the command mode i.e., the attention control line (ATN) is true, the 54110D interprets the byte on the eight data lines as an address or as a bus command. When the "Talk/Listen" HP-IB function is selected from the front panel the instrument may be addressed to talk or to listen.

If you address the instrument to listen it will remain configured to listen until it receives an abort message (IFC), its own talk address (MTA), or a universal unlisten command (UNL) from the controller.

If you address the instrument to talk it will remain configured to talk until it receives an abort message (IFC), another instrument's talk address (OTA), its own listen address (MLA), or a universal untalk command (UNT). The HP-IB status line on the CRT will indicate "Talk" when the instrument is addressed to talk and "Listen" when the instrument is addressed to listen.

The 54110D is shipped from the factory in the addressable mode, with the talk and listen addresses set to "7", i.e., T7 and L7 Refer to table 9-1 for equivalent address codes. The instrument can also be configured in the talk-only or listen-only mode. These modes enable limited bus operation without an HP-IB controller being connected. The instrument's address and addressing mode may be displayed or changed from the front panel. Refer to Section 6 for complete instructions.

If the instrument is set to the listen-only mode it responds to all data messages sent on the HP-IB. However, it cannot output data messages and is inhibited from responding to the remote, local, local lockout, clear lockout/ set local, or abort messages. In this mode the unit cannot issue the require service message and cannot respond to a serial poll.

NOTE

The front panel is enabled in the listen-only mode. This allows you to change settings while a program is executing.

If the instrument is set to the talk-only mode it does not respond to any of the bus messages. You would select this mode if the 54110D was to output data directly to an HP-IB plotter or printer without the aid of a HP-IB controller

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9-8. HP-IB TURN-ON DEFAULT CONDITIONS

Several HP-IB parameters are reset during power-up, however, both the unit's address and addressing mode are saved in nonvolatile memory.

HP-IB default conditions are:

- HP-IB local mode
- Local-lockout cleared
- Unaddressed (if in normal addressing mode)
- RQS mask set to decimal 32546 (bits 1,5,8,-14 set)
- Status byte register cleared
- WAVE FORMAT set to WORD
- EOI is asserted at the end of messages sent by 54110D
- LONGFORM is OFF
- HEADER is OFF
- ARGUMENT is NUMERIC

Refer to Section 10 for a complete discussion of the WAVE FORMAT, EOI, LONGFORM, HEADER, and ARGUMENT commands.

9-9. DATA MESSAGES

The 54110D communicates on the HP-IB primarily with data messages. The instrument interprets a byte on the eight data lines as a data message when the bus is in the data mode i.e., attention control line (ATN) is false.

This instrument can both receive and send data messages. Input data messages include the instrument's program commands (device dependent commands) used to program front panel functions and all remote functions Output data messages include instrument status information, the settings of of specific functions, measurement results, and the learn and cal strings.

The learn and cal strings are binary data strings that contain a condensed coding of the entire instrument state and the delay cal factors. Refer to paragraph 9-12 and the descriptions of the key words: SETUP, SETUP?, CALIBRATE, and CALIBRATE?, in Section 10.

9-10. RECEIVING THE DATA MESSAGE

The 54110D responds to data messages when it is in the remote mode (REN is true) and the unit is addressed to listen or when it is in the listen-only mode.

Input data messages contain a string of device dependent commands (program commands) and an end-of-string message. The program codes within a data message are executed after the EOS message is received. The following format rules must be observed for all input data messages:

- A linefeed (<LF>) or an EOI is used as the EOS message. Each data message must be terminated by a <LF> or by asserting the EOI (end or identify), bus signal line with the last byte in the message.

- The carriage return character (<CR>) is not required before <LF>.

- When more than one command is sent in a data message, a semicolon, colon, or a space must be used to separate the program commands.

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- Multiple arguments for a command must be separated by commas.
- The total length of a data message string may not exceed 300 characters.

Syntax errors in a data message are trapped and can be reported over HP-IB. Refer to key words "STATUS?", and "ERR?" in Section 10 for details concerning detecting and reporting format errors.

9-11. PROGRAM ORDER CONSIDERATIONS

Commands are interpreted and setups are changed in the 54110D's memory as they are received and found to be syntactically correct. The actual hardware settings are changed at the end of a message (EOS) unless a command to initiate a process is encountered. Process commands are immediate execution commands and include autoscale, system commands such as "DIGITIZE", and measurement commands. In these cases, hardware affected by commands preceding the process command is changed before the process is initiated. Program lines with more than 1 command are executed up to the point where an error is detected. This provides consistent operation whether commands are sent one per message or several per message.

If multiple pulse parameter measurement queries are sent in one message, the answers from those measurements will be queued for output in the order that the queries were received. Outputs in response to other queries are not queued. The last query will determine the message output by the 54110D when it is next addressed to talk.

9-12. PROGRAM COMMAND FORMAT

Program commands consist of a header followed by a parameter field. Headers can be of a long or short form. The long form allows easier understanding of program code and the short form allows more efficient use of the computer. Refer to Section 10 for a thorough discussion of short and long forms.

Program command parameters may be of four types:

Strings - Any group of ASCII characters, excluding quotation marks (decimal 34), surrounded by quotation marks

Blocks - A block of binary data in the #A format as defined in IEEE Std. 728-1982. This format is a binary block with the format:

<#><A><length word><DAB...DAB>

Length word is a 15-bit binary integer representing the number of DABs. DABs are the data bytes. <A> and <#> are ASCII bytes. 4) **Numeric** - Any integer, floating point, or exponential value. The characters <E> or <e> are used to delimit the mantissa of exponential parameters. Spaces are allowed between <+>, <->, or <E> and digits, but not between digits or <.> and digits.

Alpha - Some commands require or allow alpha arguments such as "ON", or "OFF". These arguments are ASCII strings that start with an alpha character and are followed by a printable character except a <SP>, <;>, <,>, <#>, <">, or <_> (delete).

The general rules for program command formatting are:

- The 54110D sends and receives data messages in standard ASCII code.

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- The instrument responds equally to upper and lower case characters.
- Parameter fields containing multiple parameters require a (,) to delimit individual parameters. Syntax errors in data messages are trapped and can be reported via HP-IB. Refer to Section 10 for a discussion of the key words "STATUS?" and "ERROR".

9-13. SENDING DATA MESSAGES

The 54110D can send data messages in local or remote mode, when addressed to talk, or when in the talk-only mode.

NOTE

Before the instrument is addressed to talk, the desired output data must be specified with the appropriate input data message. Otherwise, the instrument outputs the over range value "1E38" by default to complete the bus transaction. If the ERR service request is enabled, a service request will be generated with the "Output Buffer Empty" error in the ERRor queue.

Output data messages include the settings of individual functions, instrument status information, and binary learn string or cal string data. Excluding the learn and cal strings there are two output data types; integer and exponential. All output data messages contain a leading space (<SP>) or minus sign (<->) followed by the function value or status data. <CR> and <LF> are sent as the EOS message for all output data. An EOI can be sent with the <LF> if the EOI has been keyed on from the front panel or by the "EOI" program command.

Refer to Section 10 for a description of key words "LONGFORM", "HEADER", and "ARGUMENT".

NOTE

The 54110D outputs exponential values with the ASCII character "E" between the mantissa and the exponent e.g., 6.02E23.

9-14. LEARN AND CAL STRINGS

If a "SETUP?" command is sent to the 54110D and then the 54110D is addressed to talk the unit will output a learn string. The learn string consists of 236, 8-bit bytes containing information about front panel configuration. This binary data can be stored in the controller's memory for future use. The learn string includes only those parameters that determine the front panel setup of the instrument.

If a "CALIBRATE?" command is sent to the 54110D and then the unit is addressed to talk, it will output a cal string. The cal string consists of 24, 8 bit bytes containing the delay cal factors. This binary data can be stored in the controller's memory for future use

The learn string and cal string data comprise the same information that is in the instrument's SAVE/RECALL registers. Refer to Section 6 for additional information concerning these registers.

These binary data blocks i.e., the learn string and the cal string, can be returned to the 54110D by preceding the data blocks with the "SETUP" or "CALIBRATE" commands as appropriate. Refer to Section 10 for a discussion of these two key words.

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9-15. RECEIVING THE CLEAR MESSAGE

The 54110D responds to the clear message <DCL> and selected device clear message <SDC> by:

1. Clearing all serial poll status bits.
2. Clearing the input and output buffers.
3. Clearing the error queue and key register.
4. Stopping any measurement or acquisition processes except the normal background acquire-display cycle.

9-16. RECEIVING THE TRIGGER MESSAGE

The trigger message (GET bus command) causes the 54110D to make a single acquisition if the unit was in the STOP/SINGLE mode. If the unit is in the AUTO or TRigereD mode the trigger message will cause the instrument to enable the trigger repeatedly and display the data it acquires on the CRT See the RUN command in Section 10.

9-17. RECEIVING THE REMOTE MESSAGE

The remote message has two parts: The remote enable bus control line (REN) is held true, then the controller sends a device listen address <MLA>. Instrument settings are unchanged during the transition from local to remote. When the unit is in the remote mode the HP-IB status line on the CRT will indicate "Remote".

9-18. RECEIVING THE LOCAL MESSAGE

The local message returns the 54110D to front panel control. The local message (GTL bus command) addresses the instrument to listen and then switches it from remote to local. The HP-IB status line on the CRT will be eliminated when you go from remote to local. None of the instrument settings are changed during this transition.

Although the local message returns the instrument to front panel control, it does not clear the local lockout if it has been previously set.

9-19. RECEIVING THE LOCAL LOCKOUT MESSAGE

The local lockout message (LLO bus command) disables the 54110D's front panel LOCAL key. Local lockout can be set when the instrument is either in the local or remote modes. After the local lockout is set and the unit is in the remote mode, local lockout will be enforced. While the unit is in remote and the local lockout is set, the remote to local transition can only be made over HP-IB.

9-20. RECEIVING THE CLEAR LOCKOUT/SET LOCAL MESSAGE

The clear lockout/set local message sets the REN control line false and returns the instrument from the remote mode to the local mode and clears the local lockout condition. Instrument settings are not changed by this message. It can be sent when the instrument is either in the remote or local mode. The affect of sending this message when the instrument is in the local mode is to clear the local lockout if it is set

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9-21. SENDING THE REQUIRE SERVICE MESSAGE

The 54110D sends the require service message by setting the SRQ bus control line and bit 6 of the status byte true when a previously programmed condition occurs. The instrument can send the require service message in either local or remote mode. The require service message is cleared when a serial poll is executed by the system controller. During serial poll, the SRQ control line is reset immediately before the instrument places the status byte message on the bus. Table 10-1 includes the conditions that can be selected to cause the require service message. If no conditions are selected, the require service message is disabled.

The 54110D indicates having sent the require service message by displaying "SRQ" on the HP-IB status line. This indicator is turned off when, during a serial poll, the SRQ control line is reset

The 54110D will not send a require service message unless it is in the Talk/Listen mode.

9-22. THE STATUS WORD

The instrument status word is a 16-bit integer containing information about the instrument condition that set the ready bit in the status byte and/or generate a require service message. Refer to tables 10-1&2 for a description of the bits in the status word. The upper 8 bits of the status word are known collectively as the ready byte and the lower 8 bits correspond to the status byte sent during a serial poll.

The request mask is a 16-bit word that is used to specify both the conditions in the ready byte that set the ready bit in the status byte and the conditions in the status byte that generate the require service message

The bits in the request mask have the same meaning as those in the instrument status word. The ready bit in the status byte is set when all of the conditions corresponding to bits in the ready mask are true at the same time. This bit is actually set on the transition of the last required condition to become true

9-23. SENDING THE STATUS BYTE MESSAGE

The status byte message consists of one 8-bit byte. Refer to table 10-1 for the meaning of each bit. The 54110D sends the status byte message when it is addressed to talk and it receives the serial poll enable (SPE) bus command from the HP-IB system controller.

The instrument must be in the Talk/Listen mode in order to send the status byte or respond to the SPE or SPD (serial poll disable) commands.

Bits in the status byte are set depending on the state of the instrument. If a condition occurs that causes one of the bits in the status byte to be set and if its corresponding bit in the request mask is set, the require service message will be sent.

If the RQS bit is set, indicating that the instrument sent the require service message, and a serial poll is executed, all bits in the status byte will be cleared. If the RQS bit is clear and a serial poll is executed, the status byte will be left unchanged.

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If a condition that causes one of the bits in the status byte to be set is removed and if the corresponding bit in the request mask is clear, the corresponding bit in the status byte will be cleared.

To supplement the information in the status byte, the ERRor query can be used to determine what specific error occurred.

9-24. RECEIVING THE ABORT MESSAGE

The abort message (IFC control line true) halts all bus activity. When the 54110D receives the abort message, it becomes unaddressed and stops talking or listening. The require service message and the status byte are unaffected by the abort message.

NOTES:

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SECTION 10
COMMAND SET OVERVIEW

10-1. INTRODUCTION

With the exception of the line switch, all the front panel controls as well as some instrument features that are remote only operations can be controlled by sending the appropriate commands over the HP-IB

NOTE

Before you get started programming your 54110D make sure to review Section 4 for information concerning HP-IB address selection and HP-IB interconnections. You should also review Section 9 before continuing with this section.

10-2. COMMAND SET ORGANIZATION

The command set for the 54110D is conveniently divided into eleven separate groups, ten have been organized into functional groups such as the Trigger Subsystem, which contains all the HP-IB commands that control the instrument's triggering functions.

These subsystems include:

1. **Acquire Subsystem**

   The commands in The Acquire Subsystem determine the conditions for the DIGITIZE command.

2. **Channel Subsystem**

   The commands in the Channel Subsystem are used to control the two vertical inputs. (See the VIEW and BLANK System commands for viewing channels 1 & 2 on the CRT.)

3. **Display Subsystem**

   The commands in the Display Subsystem are used to control how data, time & voltage markers, text, and the graticules are displayed on the CRT.

4. **Function Subsystem**

   The commands in the Function Subsystem are used to control the waveform math features of the instrument.

5. **Graph Subsystem**

   The commands in the Graph Subsystem control the vertical magnifier on the instrument.

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6. Hardcopy Subsystem

The Hardcopy Subsystem commands control parameters used during the printing and plotting of waveforms from the 54110D.

7. Measure Subsystem

The commands in the Measure Subsystem control the automated measurements that can be made with the 54110D.

8. Timebase Subsystem

The commands in the Timebase Subsystem control the timebase section of the 54110D.

9. Trigger Subsystem

The commands in the Trigger Subsystem control the trigger modes of the 54110D.

10. Waveform Subsystem

The commands in the Waveform Subsystem Control the transfer of data to and from the HP-IB buffer memories in the 54110D.

The 11th group is the **System Commands.** They control the HP-IB operations as well as the basic operation of the 54110D

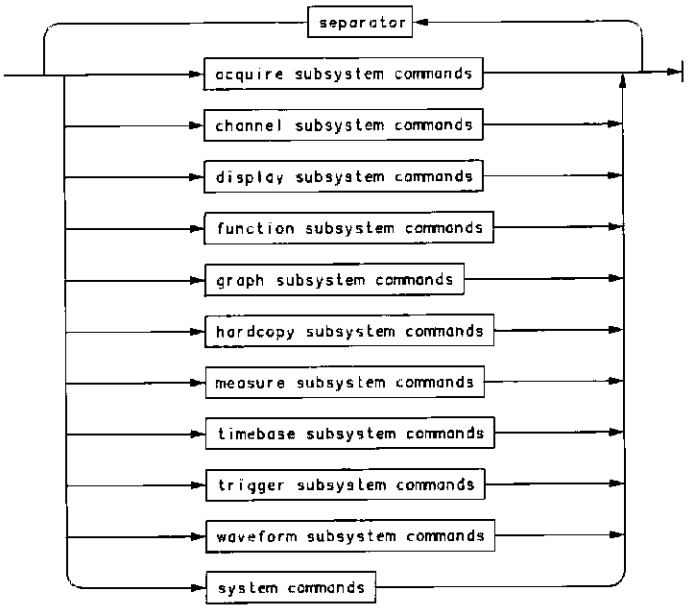
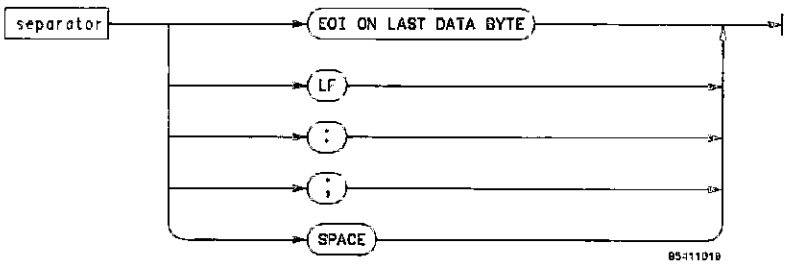


Figure 10-1 Command Set Syntax Diagram.

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Command Syntax Diagram (continued).

When programming the 54110D you can initially issue a Subsystem Select Command or a System Command from the controller to the 54110D. If you have selected a particular subsystem you may execute any number of the commands in that subsystem, call System commands indiscriminately or select another subsystem. Calling a System command does not change the Selected Subsystem. Refer to figure 10-1.

NOTE

System commands can be invoked at any time and do not change the subsystem selection.

NOTES:

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10-2. NOTATION CONVENTIONS AND DEFINITIONS

The following conventions are used in this manual in descriptions of remote (HP-IB) operation:

< > Angular brackets enclose words or characters that are used to symbolize a program code parameter or an HP-IB command, e.g., <A> represents the ASCII character "A".

| "or": Indicates a choice of one element from a list. For example, <A>|<B> indicates <A> or <B> but not both.

... Trailing dots (an ellipsis) are used to indicate that the preceding element may be repeated one or more times.

[ ] Square brackets indicate that the enclosed items are optional.

{ } When several items are enclosed by braces, one, and only one of these statements must be selected.

The following definitions are used:

d:: = A single ASCII character, 0-9.

n:: = A single ASCII character, 1-9.

<LF>:: = ASCII linefeed (decimal 10).

<CR>:: = ASCII carriage return (decimal 13).

<sp>:: = ASCII space (decimal 32)

10-3. COMMAND ABBREVIATIONS

Every command and every alpha parameter has at least two forms, a shortform and a longform, in some cases they will be the same. The shortform is obtained by using the following rule:

If the longform has more than 4 characters,
then if the 4th character is a vowel or the same as the 3rd character,
then truncate to 3 characters,
else truncate to 4 characters.

EXAMPLE - LONGFORM abbreviates to LONG.
SERIAL abbreviates to SER.
YOFFSET abbreviates to YOF.

In the case where two short forms would be identical, one of them will be changed slightly to differentiate between the two. In the command descriptions that follow, each command is given in both long and shortforms Some commands also have industry standard forms and these have been included in the instruction set. This means that some commands will have three forms.

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10-4. ALPHA AND NUMERIC ARGUMENTS

Most of the programming commands that require parameters can use either ALPHA or NUMERIC arguments for their parameters.

EXAMPLE - OFF is the same as 0.
ON is the same as 1.

10-5. DATA OUTPUT (QUERY) FORMAT

When a query command (command followed by a "?") is sent to the 54100A/D, a response message is generated and sent back to the controller the next time the 54100A/D is addressed to talk.

The command header will be returned if the HEADER command has been set ON and will not be returned if set to OFF.

The command argument will be returned as an alpha argument if the ARGUMENT command has been set to ALPHA and will be returned as a numeric argument if set to NUMERIC. Headers and alpha arguments will be returned in the longform if LONGFORM command has been set ON and will be returned in the shortform if set OFF.

All output fields are an even number of bytes in length. There are four types of output arguments; (1)Headers and Alpha arguments, (2) Integers, (3) Real numbers and (4) Enumerated output. The enumerated output may be alpha or integer depending on whether the ARGUMENT command is set to ALPHA or NUMERIC

10-6. COMMAND ORDER CONSIDERATIONS

Commands are interpreted and setups are changed in the 54100A/D as they are received and found to be syntactically correct. Commands preceding an error in multi-command messages are executed up to the point where the error is detected. This provides consistent operation whether commands are sent one per message or several per message.

When a query is executed the reply is placed in the output buffer of the 54100A/D. Multiple queries on one line result in the last reply overwriting the previous replies. The exception to this is when multiple parameter measurement queries are sent on one command line. In this case the replies to the measurement queries are buffered in the order that the queries occurred in the command line.

10-7. DEFAULT SETTINGS

When power is cycled on the instrument several interface parameters are put in the preset condition. Specifically the request mask (RQS mask) is set to 32546 (bit 1,5,8-14 set).

If you hold a front panel key down at the same time the unit is energized (key down power-up) the unit will initialize a more complete set of parameters. These include selecting arguments to be numeric, headers off and longform off, and EOI to be asserted with the last data byte of a message. This has the same effect as sending a "RESET" command except that the reset command does not change the EOI selection. If a deeper reset is required you may hold TWO front panel keys down at the same time the unit is energized, in addition to initializing the same set of parameters that a single key down power up did, it also erases all available nonvolatile RAM.

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10-8. STATUS WORD

The instrument status word is a 16-bit integer containing information about the instrument conditions that set the ready bit in the status byte and/or generate a Require Service message. See Tables 10-1 and 10-2 for a description of the bits in the Status Word. The upper 8 bits of the Status Word are known collectively as the ready byte The lower 8 bits correspond to the status byte sent during a serial poll.

A companion 16 bit word, the request mask, is used to specify both those conditions in the ready byte that set the ready bit in the status byte, and those conditions in the status byte that generate a Require Service Message. The bits in the request mask have the same meanings as those in the instrument status word. The ready bit in the status byte is set when all of the conditions corresponding to bits in the ready mask are true at the same time. This bit is actually set on the last transition of the last required condition to become true.

The "REQuest" programming command is used to specify the request mask while the "STAtus" programming query can be used to read the instrument status word.

NOTES:

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BIT	MASK WEIGHT	STATUS BIT CONDITION
7	128	MSG = High indicates that a message was displayed on the status line of the display. A MSG query is used to determine the message code.
6	64	RQS = Requesting service - High indicates that this instrument requested service.
5	32	ERR = Error - High indicates an error occurred. An ERROR query is used to determine error code.
4	16	RDY = Ready - High indicates the instrument is ready. This is based on the ready mask. A RDY query is used to determine condition.
3	8	LCL = Local switch or power cycle - High indicates that the instrument has been switched to local from the front panel or power was cycled off then on again.
2	4	FPS = Front panel service request - High indicates a front panel key has been pressed. A KEY query is used to determine the key code.
1	2	PWR = Not used, always 0.
0	1	RQC = Request control - Not used, always 0.

Notes:
1. To set the RQS bit and SRQ bus control line true, the condition must be enabled in the RQS mask.
2. If no condition is enabled, the 54110D can not set the SRQ bus control line nor the RQS bit true. However, bits 1-5 and 7 of the status byte are set to indicate which conditions have occurred.
3. The Ready bit (bit 4) is set when all conditions in the Ready Byte (Table 10-2) enabled in the request mask are true.

Table 10-1 The Lower Byte of the Status Word (The Status Byte)

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BIT	MASK WEIGHT	READY BIT CONDITION
15	32768	Not used, always 0.
14	16384	Cal = High indicates that self calibration has completed execution.
13	8192	Test = High indicates that the requested self test has completed execution.
12	4096	Hard = Hardcopy complete - High indicates that the last byte of printer or plotter dump has been sent and received
11	2048	Data = Data available - High indicates that something is in the buffer waiting to be read.
10	1024	Acq = Acquisition complete - High indicates that all waveforms are acquired.
9	512	Trig = Triggered - High indicates that the instrument is receiving triggers.
8	256	Parse = Parse complete - High indicates that the last command has completed parsing.
Note: The Ready bit (bit 4) of the Status Byte (Table 10-1) is set if all of the ready conditions specified in the RQS mask are true.		

Table 10-2. The Upper Byte of the Status Word (The Ready Byte)

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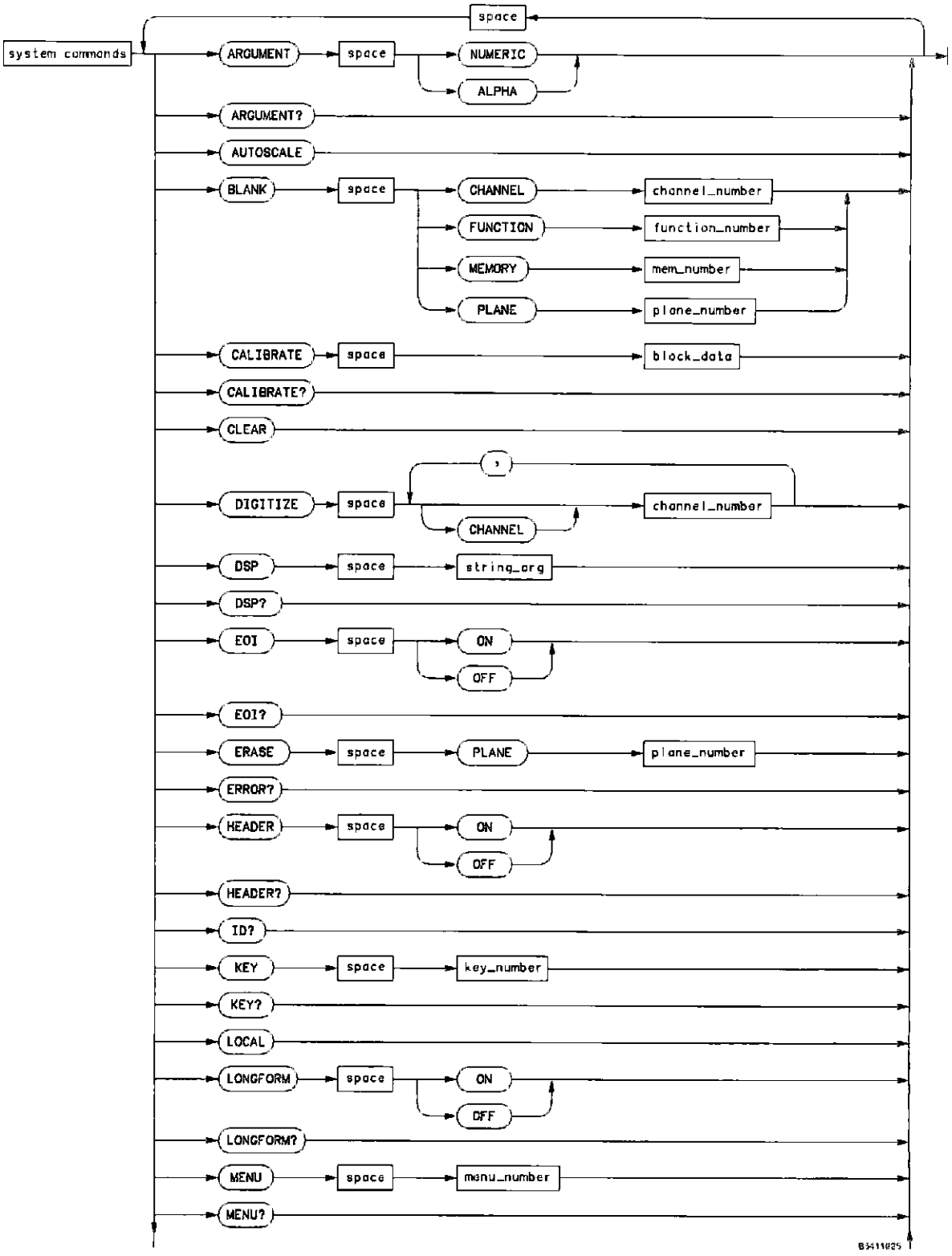


Figure 10-2. System Commands

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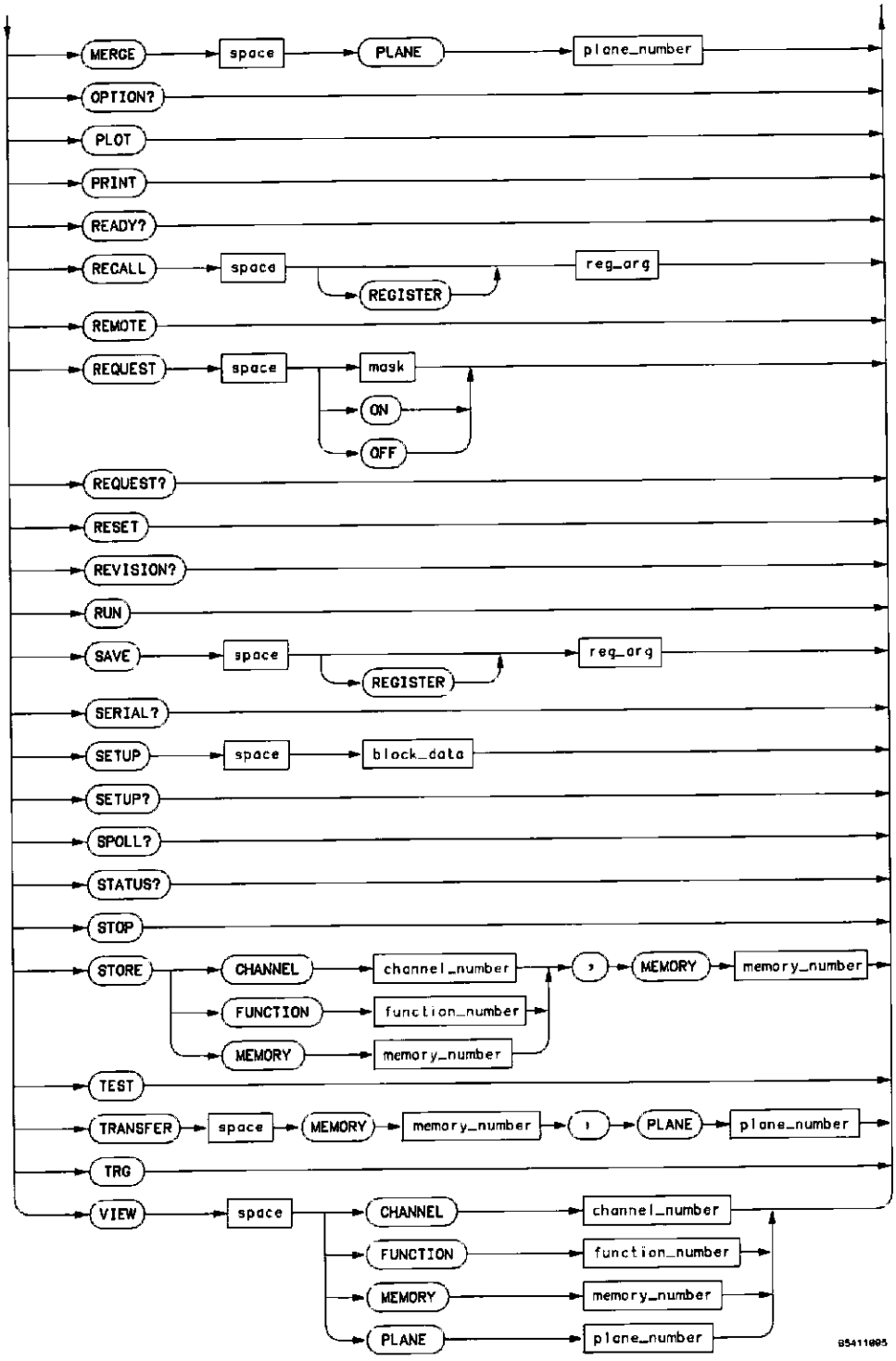


Figure 10-2. System Commands

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WHERE:

MENU_NUMBER = An integer from 1 to 14.

KEY_NUMBER = An integer from 1 to 63 (see table 10-3 for keycodes)

STRING_ARG = Any collection of ASCII characters excluding quotes, surrounded by quotes.

REG_ARG = An integer from 0-9.

MASK = An integer between 0 and 65535. This number is the sum of all the bits in the request mask corresponding to conditions that are to be enabled. See tables 10-1 and 10-2 for the bit definitions in the request mask.

BLOCK_DATA = A block of data in #A format as defined in IEEE Std 728-1982.

CHANNEL_NUMBER = An integer 1 or 2

PLANE_NUMBER = An integer from 0 to 2.

MEMORY_NUMBER = An integer from 1 to 4.

FUNCTION_NUMBER = An integer 1 or 2.

Figure 10-2. System Commands (cont'd)

10-9. SYSTEM COMMANDS

System commands control HP-IB operations as well as the basic operation of the oscilloscope. They can be called at anytime and when the system command has been executed the unit will return to the subsystem that it was in before the system command was executed. Refer to Figure 10-2 for syntax of these commands

---

ARGument

command/query

This command sets the output mode for the instrument's response to a query for commands that have both alpha and numerical arguments. If the alpha response is selected the arguments are returned in the alpha format and follow the same abbreviation rules as the commands. If the numeric response is selected the arguments are returned in the numeric format. This command does not affect the input data messages to the 54110D, that is, arguments maybe in either alpha or numeric form regardless of how the ARGUMENT command is set. The response to a query will be returned in the current argument mode

(continued on next page)

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ARGument (cont'd)

Command Syntax: ARGument {[ALPHa | 1]
[NUMeric | 0]}

Example: OUTPUT 707;"ARGUMENT NUMERIC"

Query Syntax: ARGument?

Returned Format: [ARGument]<argument><crlf>

Example: OUTPUT 707;"ARGUMENT?"
ENTER 707;Argument$
PRINT Argument$

AUToscale

command

The AUToscale command causes the instrument to automatically select the vertical sensitivity, vertical offsel, trigger level and sweep speed for a display of the input signal. If input signals are present at bolh vertical inputs the sweep will be triggered on Chan 1 and the display will go to the split screen mode and the vertical sensitivity for each channel will be scaled appropriately. If only one of the vertical inputs has a signal on it, the split screen function will be turned off. See Operating Characteristics for input signal requirements for proper AUToscale operation.

When the AUToscale cycle is complete, the Timebse menu will be selected, the input devices will be assigned to the SEC/DIV and the unit will be in the Remote Listen mode.

Command Syntax: AUToscale

Example: OUTPUT 707;"AUTOSCALE"

BLANk

command

The BLANk command causes the instrument to turn off, (stop displaying), an active channel display, function, pixel memory or waveform memory. If you want to turn off an active display channel use the parameter **Channel 1|2**, if you want to turn off a pixel memory use the parameter **Plane 1|2, where plane 1 = pixel memory 5 and plane 2 = pixel memory 6.**

Command Syntax: BLANk {[CHANnel { 1 | 2 }]
[PLANE { 1 | 2 }]
[FUNCTION { 1 | 2 }]
[MEMory { 1 | 2 | 3 | 4 }]}

Example: OUTPUT 707;"BLANK CHANNEL1"

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CALibrate

command/query

This command sends a Cal String to the instrument. A Cal String consists of 24 8-bit bytes containing the Delay Calibration factors that are setup in the Cal Menu. These Cal factors are also saved during a front panel SAVE operation and are recalled during a front panel RECALL operation. The CALibrate query sends the Cal String to the controller using the same format as required by the CALibrate command. This means that no modification needs to be made to the string between the time that it is received from the instrument after the query and the time that it is sent back to the instrument.

Command Syntax: CALibrate<Cal String>

Example: OUTPUT 707;"CAL"

Query Syntax; CALibrate?

Returned Format: [CALibrate]<Cal String><crlf>

```
Example:  DIM Cal$[24]
          OUTPUT 707;"EOI ON; HEADER OFF"
          OUTPUT 707;"CAL?"
          ENTER 707 USING "-K";Cal$
          OUTPUT 707;"CAL ";Cal$
```

CLEAR

command

The CLEAR command performs an operation similar to a Device Clear <DCL> or the Selected Device Clear<SDC>. The 54110D responds to the CLEAR message by:

1. Terminating all bus communications in process by untalking and unlistening.
2. Clearing all serial poll status bits
3. Clearing the input and output buffers
4. Clearing the error queue and key register.
5. Stopping any measurement or acquisition processes except the normal background acquire-display.

Command Syntax: CLEAR

Example: OUTPUT 707;"CLEAR"

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DIGitize

command

This command is used to acquire waveform data for transfer over the HP-IB. It causes an acquisition to take place on the specified channel(s) with the resulting data being stored in the corresponding waveform memory i.e., channel 1 data is stored to waveform memory 1 etc. If ACQuire TYPE is ENVELOPE, minimum and maximum data for channel 1 will go in waveform memories 1 and 3 respectively. Similarly, minimum and maximum data from channel 2 will go into waveform memories 2 and 4. The ACQUIRE subsystem commands are used to setup conditions such as TYPE, COMPLETION criteria, number of POINTS and the average COUNT for the next DIGITIZE command. See the ACQUIRE subsystem for a description of these commands.

Command Syntax: DIGitize [CHANnel]{ 1 | 2 | 1,2 }

```
Example:  OUTPUT 707;"DIGITIZE CHANNEL 1,2"
```

DSP

command/query

This command writes a string to the advisory line (line 15) on the CRT. The query returns the string last written to the advisory line. This may be a string written with a DSP command or an internally generated advisory.

Command Syntax: DSP<ASCII string>

```
Example:  OUTPUT 707;"DSP""COLOR DISPLAY"""
```

Query Syntax: DSP?

```
Returned Format:  [DSP]<string><crlf>

Example:  DIM Dsp$[40]
          OUTPUT 707;"DSP?"
          ENTER 707;Dsp$
          PRINT Dsp$
```


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EOI

command/query

This command specifies whether or not the last byte of a reply from the 54110D is to be sent with the EOI bus control line set true or not. The query returns the current status of EOI.

Command Syntax: EOI {[ON | 1] | [OFF | 0]}

```
Example:  OUTPUT 707;"EOI OFF"
```

Query Syntax: EOI?

```
Returned Format:  [EOI]<argument><crlf>

Example:  OUTPUT 707;"EOI?"
          ENTER 707;Eoi$
          PRINT Eoi$
```

ERASe

command

This command erases a specified display memory plane. Plane 1 is pixel memory 5. Plane 2 is pixel memory 6. Erasing plane 0 is the same as pressing the CLEAR DISPLAY front panel key. If the scope is running and being triggered and ERASe plane 0 is executed the instrument will momentarily stop acquiring data, clear the CRT and then continue with data acquisition.

Command Syntax: ERASe PLANE { 0 | 1 | 2 }

```
Example:  OUTPUT 707;"ERASE PLANE 0"
```

ERRor?

query

The query causes the 54110D to output the next error number in the error queue over HP-IB. This instrument has an error queue that is 16 errors deep and operates on a first-in first-out basis. Successively sending the query, ERROR? returns the error numbers in the order that they occur until the queue is empty. Any further queries then return 0's until another error occurs. See Table 10-2 for a list ERRor numbers.

Query Syntax: ERRor?

```
Returned Format:  [ERRor]<NR1><crlf>

Example:  OUTPUT 707;"ERROR?"
          ENTER 707 USING "-K";Error$
          PRINT USING "K";Error$
```


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The error numbers and definitions below are the ones reported during an ERROR? query.

ERROR NUMBER	DESCRIPTION
-100	Unknown command
-101	Invalid character received
-110	Command header error
-119	Command header expected
-120	Numeric argument error
-121	Numeric data expected
-123	Numeric overflow
-125	Numeric syntax error
-130	Non-numeric argument error
-131	Character data expected
-132	String data expected
-133	Block data (binary data) expected
-134	String length error
-135	Block length error
-142	Too many arguments
-143	Argument delimiter error
-144	Message unit delimiter error
-149	Missing argument
-150	Query expected
-151	Query not allowed
-201	Command not executable in local mode
-202	Setting lost on power up
-211	Settings conflict
-212	Argument out of range
-222	Insufficient capability/configuration
-230	Transmission aborted
-231	Input buffer full or overflow
-233	Output buffer empty
-301	Interrupt fault
-302	System error
-311	RAM failure (hard error)
-312	RAM data loss (soft error)
-321	ROM checksum error
-340	Self test failed
-350	Timer error
-360	Analog hardware error
-370	Digital hardware error
-399	Power supply failure

Table 10-3. Error Numbers

Positive error numbers are reported after a Self Test Failed error (-340). These refer to the internal self test loops that failed to pass self test.

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HEADer

command/query

This command sets the command echo mode for query responses. When HEADer is set to ON query responses will include the command header The query form of this command tells you whether the echo mode is ON or OFF.

Command Syntax: HEADer {[OFF | 0][ON | 1]}

```
Example:  OUTPUT 707;"HEADER ON"
```

Query Syntax: HEADer?

```
Returned Format:  [HEADer]<argument><crlf>

Example:  OUTPUT 707;"HEADER?"
          ENTER 707;Header$
          PRINT Header$
```

ID?

query

This query returns the instrument model number, 54110D.

Query Syntax: ID?

```
Returned Format:  [ID]<54110D><crlf>
Example:  DIM Id$[10]
          OUTPUT 707;"ID?"
          ENTER 707;Id$
          PRINT Id$
```

KEY

command/query

This command simulates the pressing of a specified front panel key. Keys may be pressed over the HP-IB in any order that is legal from the front panel. Use caution to insure that the instrument is in the desired mode before executing the KEY command. The query returns the key code for the last key pressed over the HP-IB. Key codes range from 1 to 63 with 0 representing no key (returned after power-up). See table 10-3 for a list of key codes.

Command Syntax: KEY<keycode>

```
Example:  OUTPUT 707;"KEY 48"
```

Query Syntax: KEY?

```
Example:  OUTPUT 707;"KEY?"
          ENTER 707;Key$
          PRINT Key$
```


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KEY	KEYCODE	KEY	KEYCODE
Menu Select 1	1	"-"(minus)	23
Menu Select 2	2	0	24
Menu Select 3	3	1	25
Menu Select 4	4	2	26
Menu Select 5	5	3	27
Menu Select 6	6	4	28
Menu Select 7	8	5	29
Menu Select 8	9	6	30
Function Select 1	15	7	31
Function Select 2	14	8	32
Function Select 3	13	9	33
Function Select 4	12	CLEAR DISPLAY	40
Function Select 5	11	RUN	41
Function Select 6	10	STOP/SINGLE	42
sec/Volt	16	SAVE	43
msec/mV	17	RECAL	44
µsec	18	LOCAL	45
nsec	19	AUTOSCALE	48
psec	20	↑→	56
CLEAR	21	←↓	63
"."(decimal pt.)	22	no key	0

NOTE

The Menu Select Keys are located at the bottom of the screen with menu select 1 at the lower left of the screen. The Function Select Keys are located at the right of the screen with function select 1 located at the upper right of the screen.

Table 10-4. 54110D Front Panel Key Codes

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LOCAL

command

This command performs a similar operation to the Clear Lockout/Set Local message. It is provided for controllers with limited HP-IB control capability. The HP-IB Clear Lockout/Set Local Message is the preferred method of switching the instrument from Remote to Local and clearing the Local Lockout. See paragraphs 9-6 and 9-18 for more information.

```
Command Syntax:  LOCAL

     Example:  OUTPUT 707;"LOCAL"
```

LONGform

command/query

This command sets the longform for the instrument's responses to queries. If the LONGform command is set OFF command headers and alpha arguments are sent from the 54110D in the abbreviated form. If the the LONGform command is set ON the whole word will be output. This command does not affect the input data messages to the 54110D -- headers and arguments may be input to the 54110D in either the long or short form regardless of how the LONGform command is set. The query returns the status of the LONGform command.

```
Command Syntax:  LONGform {[ OFF | 0 ]
                          [  ON | 1 ]}

     Example:  OUTPUT 707;"LONG 1"

Query Syntax:  LONGform?

     Returned Format:  [LONGform]<argument><crlf>

     Example:  OUTPUT 707;"LONGFORM?"
               ENTER 707;Long$
               PRINT Long$
```


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MENU

command/query

This command allows you to select one of the 14 menus on the front panel. The Query returns the current menu

Command Syntax: MENU {[1] -Channel 1
[2] -Channel 2
[3] -Timebase
[4] -Trigger
[5] -Display
[6] -Delta V
[7] -Delta t
[8] -Waveform Save
[9] -Waveform Math
[10] -Measurements
[11] -Plot
[12] -Print
[13] -Probes
[14]} -Utility

Example: OUTPUT 707;"MENU 4"

Query Syntax: MENU?

Returned Format: [MENU] <menu #><crlf>

Example: OUTPUT 707;"MENU?"
ENTER 707;Menu$
PRINT Menu$

MERGE

command

This command stores the contents of the active display to the specified pixel memory. Where plane 1 = pixel memory 5 and plane 2 = pixel memory 6.

Command Syntax: MERGE {[PLANE1 | PLANE2]}

Example: OUTPUT 707;"MERGE PLANE2"

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OPTion?

query

This query returns a list of options that are installed on your instrument. If no options are installed a "0" will be returned. (There are currently no internal options for the 54110D.)

Query Syntax: OPTion?

Returned Format: [OPTion] <0><crlf>

```
Example:  OUTPUT 707;"OPT?"
          ENTER 707;Opt$
          PRINT Opt$
```

PLOT

command

This command causes the 54110D to make a hardcopy dump of the display and/or the waveform memories to an HPGL compatible plotter as soon as the oscilloscope is next addressed to talk. The context of the output is controlled with the programming commands in the HARDCOPY subsystem.

Command Syntax: PLOT

Example:

```
CLEAR 707           ! Clear interface buffers.
OUTPUT 707;"PLOT"   ! Starts print buffer.
SEND 7;UNT UNL      ! Clears bus and
!                     sets ATN line at controller true.
SEND 7;LISTEN 5     ! Sets plotter at address 5 to listen.
SEND 7;TALK 7       ! Sets 54110D to talk mode.
SEND 7;DATA         ! Sets ATN line at controller false so
                    ! so data can be transferred.
WAIT 50             ! Wait 50 seconds for transfer to complete
```

NOTE

When programming the 54110D use the SRQ capabilities to determine if the transfer is complete. Attempting to program the instrument while making a hardcopy dump will cause errors.

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PRINt — command

This command causes the 54110D to make a hardcopy dump of the display and/or waveform memories using the HP RASTER GRAPHICS STANDARD when the oscilloscope is next addressed to talk. The content of the hardcopy dump is controlled with programming commands in the HARDCOPY subsystem.

Command Syntax: PRINt

Example:

```
CLEAR 707             ! Clears interface buffers.
OUTPUT 707;"PRINT"    ! Starts print buffer.
SEND 7;UNT UNL        ! Clears bus, sets ATN line at controller true.
SEND 7:LISTEN 1       ! Sets printer at address 1 to listen
SEND 7;TALK 7         ! Sets the 54110D to talk mode.
SEND 7;DATA           ! Sets ATN line at controller to false
!                       so data can be transferred.
WAIT 25               ! Wait 25 seconds for transfer to finish.
```

NOTE

When you are programming the 54110D use the SRQ capabilities to determine if the transfer is complete. Attempting to program this instrument while making a hardcopy dump will cause errors.

READy? | RDY? — query

This query returns the ready byte (the upper byte of the status word). See Table 10-2.

Query Syntax: { READy | RDY }?

Returned Format: [READy]<NR1><crlf>

```
Example:  OUTPUT 707;"READY?"
          ENTER 707;Ready$
          PRINT Ready$
```

RECall — command

This command recalls an instrument setup and color settings from a specified save-recall register.

Command Syntax: RECall[REGISTER]<d>

Example: OUTPUT 707;"RECALL0"

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REMOTE

command

This command performs a similar operation as a Remote message followed by a Local Lockout message. It is provided for use by controllers that have a limited HP-IB control capability. The HP-IB Remote and Local Lockout messages are the preferred method of switching the instrument from Local to Remote and invoking Local Lockout. Refer to paragraphs 9-17 and 9-20. If the REN line is false, the REMOTE command will have no affect.

Command Syntax: REMOTE

Example: OUTPUT 707;"REMOTE"

REQuest | RQS

command/query

The REQuest command sends an SRQ enable code which is an integer representing the binary weighted values of the condition bits in the ready mask and the RQS mask.

The ready mask determines what ready conditions cause the ready bit in the status byte to be set. The RQS mask determines what conditions will cause an SRQ to be issued.

Setting the SRQ enable code clears any pending SRQ, as well as all errors, messages and keys awaiting query. See paragraph 10-7 and Tables 10-1 and 10-2.

Another form of this command allows you to follow the REQUEST command with ON or OFF. This command enables or disables the ability of the 54110D to generate the require service message without changing the request mask. Any unmasked conditions that occur with REQUEST OFF will be saved until the REQUEST ON command is received. At that time, unmasked conditions that occurred before and after the REQUEST ON command will generate the require service message.

Command Syntax: { REQuest | RQS }
{ ON | OFF | SRQ enable code }

Example: OUTPUT 707;"REQUEST 36"

Query Syntax: { REQuest | RQS }?

Returned Format: [REQuest]<SRQ enable code><crlf>

Example: OUTPUT 707;"REQUEST?"
ENTER 707;Request$
PRINT Request$

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RESet | RST

command

This command presets the instrument to default settings. These settings are the same as those established during a key down power up. See Table 10-4 for a list of the default conditions.

Command Syntax: {RESet | RST}

```
Example:  OUTPUT 707;"RST"
```

REVision?

query

This query returns an integer corresponding to the revision date of the internal firmware.

Query Syntax: REVision?

```
Example:  OUTPUT 707;"REV?"
          ENTER 707;Rev$
          PRINT Rev$
```

RUN

command

This command causes the instrument to acquire data for the active waveform display on the CRT based on the timebase mode. If the time base mode is in SINGLE, the RUN command will cause the instrument to enable the trigger once and display the data it acquires on the active on the CRT. This is the same thing that happens when the front panel STOP/SINGLE key is pressed when the instrument is STOPPED. If the timebase mode is AUTO or TRIGGERED, the RUN command will cause the instrument to enable the trigger repeatedly and display the data it acquires continuously on the display. This is the same thing that happens when the front panel RUN key is pressed. See the TIMebase MODE command for a description of the various modes.

Command Syntax: RUN

```
Example:  OUTPUT 707:"RUN"
```


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RESET CONDITIONS FOR THE 54110D

Ch1/Ch2 Mode	-Normal
Ch1/Ch2 Display	-On
Ch1/Ch2 Volts/div.	-1.0 volts/div
Ch1/Ch2 Offset	-0.0 volts
Ch1/Ch2 Magnify	-Off
Ch1/Ch2 Magnify Window Size	-7.0 volts
Ch1/Ch2 Magnify Window Position	-0.0 volts
Seconds/div	-1.0 usec/div
Delay	-0.0 sec
Delay Reference	-Center Screen
Auto/Triggered Sweep	-Auto
Trigger Mode	-Edge
Trigger Source (edge mode)	-Channel 1
Trigger Level (all sources)	-0.0 volts
Trigger Slope (all sources)	-Positive
Holdoff Mode (edge mode)	-Time
Holdoff Events (edge mode)	-2
Holdoff Time (edge mode)	-70.0ns
Trigger Pattern(pattern mode)	-Ch1; High -Ch2; Dontcare -Trig3; Dontcare -Trig4; Dontcare
Pattern Edge (pattern mode)	-Entering
Holdoff Mode (pattern mode)	-Time
Holdoff Time (pattern mode)	-70.0ns
Holdoff Events (pattern mode)	-2
Display Mode	-Normal
Display Time/Persistence	-0.5s
Number of Averages	-8
Split Screen	-Off
Graticule	-Axes
Completion Criteria (For HP-IB DIGitize command)	-100%
Voltage Markers	-Off
Marker1 Position	--2.5 volts
Marker2 Position	-+2.5 volts
Topbase Reference	-100%

Table 10-5. Reset Conditions

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Time Markers	-Off
Start Marker Position	--3.5us
Stop Marker Position	-+3.5us
Start Marker Edge Slope	-Positive
Stop Marker Edge Slope	-Negative
Start Marker Edge Number	-1
Stop Marker Edge Number	-1
Waveform Memories	-Off
SOURce for Store	-Channel 1
Selected Memory	-Memory 1
Pixel memories	-Off
Waveform Data	-0V
Pattern Duration	-10.0ns
Pattern (pattern edge mode)	-Ch1; Clock -Ch2; Dontcare -Trig3; Dontcare -Trig4; Dontcare
Pattern Present/Not Present	-Present
Holdoff Time (pattern edge mode)	-70.0ns
Arming Slope (time delayed mode)	-Negative
Arming Channel (time delayed mode)	-Channel 1
Time Delay (time delayed mode)	-20.0ns
Trigger Slope (time delayed mode)	-Positive
Trigger Channel(time delayed mode)	-Channel 1
Arming Slope (event delayed mode)	-Negative
Arming Chan. (event delayed mode)	-Channel 1
Events Delay (event delayed mode)	-1
Trigger Slope (event delayed mode)	-Positive
Trigger Chan.(event delayed mode)	-Channel 1
Functions 1&2	-OFF
Functions (definition)	-(Chan 1 - Chan 2)
Functions (volts/div)	-2.0 volt
Functions (offset)	-0.0 volts

RESET VALUES FOR THE HP-IB FOR THE 54110D

Service Request Mode	-Disabled (RQS OFF)
Service Request Mask	-Decimal 32546
Serial Poll Status Byte	-Clear
Error Queue	-Empty
WAVeform Format	-WORD
EOI	-ON
LONGform	-OFF
HEADer	-OFF
ARGument	-NUMERIC

Table 10-5. Reset Conditions

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SAVE

command

This command saves an instrument setup and color settings in the specified save/recall register. It's action is the same as performing a SAVE operation from the front panel.

Command Syntax: SAVE[REGISTER]<d>

Example: OUTPUT 707;"SAVE1"

SERial?

query

This query returns the instrument serial number as a quoted string.

Query Syntax: SERial?

Example:
```
OUTPUT 707:"SER?"
ENTER 707; Ser$
PRINT Ser$
```

SETup

command/query

This command sets up the 54110D according to the learn string. The query returns the learn string from the oscilloscope

Command Syntax: SETup

Example:
```
OUTPUT 707;"SETUP ";Set$
```

Query Syntax: SETup?

Returned Format: [SETup]<block type A>

Example:
```
DIM Set$[276]
OUTPUT 707;"HEADER ON EOI ON"
OUTPUT 707;"SETUP?"
ENTER 707 USING "-K";Set$
OUTPUT 707;"SETUP ";Set$
```

NOTE

The logical order for this instruction would be to send the query first followed by the command at a time of your choosing. The query causes the learn string to be sent to the controller and the command causes the learn string to be returned to the 54110D.

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SPOLl? | STB?

query

This query returns the status byte (the lower byte of the status word). This command is similar in operation to conducting a serial poll from the controller except that all bits in the byte returned by this query are dynamic and reflect the state of the instrument at the time of the query. Bits in the byte returned by a serial poll stay set if the require service message was sent and are cleared after a serial poll. This command is provided for use by controllers that have a limited HP-IB control capability Using the serial poll is the preferred method of reading the status byte.

Query Syntax: { SPOLl | STB }?

```
Example:  OUTPUT 707;"STB?"
          ENTER 707;Stb$
          PRINT Stb$
```

STAtus

query

This query returns the instrument status word. The instrument status word is a 16-bit word which is returned as an integer, and contains information about the instrument conditions that set the ready bit in the status byte and/or generate a Require Service message. The upper 8 bits of the status word are known collectively as the ready byte, while the lower 8 bits correspond to the status byte sent during a serial poll The STATus query is used to read the status word representing the current status of the 54110D. Unlike the response to serial poll, the conditions are dynamic, not latched Therefore the status response reflects the current status

A companion 16 bit word, the request mask, is used to specify both those conditions in the ready byte that set the ready bit in the status byte, and those conditions in the status byte that generate a Require Service message. The bits in the request mask have the same meanings as those in the instrument status word. The ready bit in the status byte is set when all of the conditions corresponding the bits in the ready mask are true at the same time. This bit is actually set on the transition of the last condition to become true. The REQuest system command is used to specify the request mask.

Query Syntax: STATus?

```
Example:  OUTPUT 707;"STA?"
          ENTER 707;Sta$
          PRINT Sta$
```


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STOP

command

This command causes the instrument to stop acquiring data for the active display on the CRT. The RUN command must be executed in order to restart the acquisition.

Command Syntax: STOP

Example: OUTPUT 707;"STOP"

STORe

command

This command allows you to move stored waveforms from one place to another internal to the instrument. This command has two parameters. The first is the source of the waveform which can be Channel 1 | 2, Function 1 | 2, or Memory 1 | 2 | 3 | 4. The second parameter is the destination of the waveform which can be Memory 1 | 2 | 3 | 4.

Command Syntax:
```
STORe {[CHANnel 1 | 1]
       [CHANnel 2 | 2 ]
       [FUNCtion 1 | 9 ]
       [FUNCtion 2 | 10 ]
       [MEMory 1 | 11 ]
       [MEMory 2 | 12 ]
       [MEMory 3 | 13 ]
       [MEMory 4 | 14 ]}<,>
      {[MEMory 1 | 11 ]
       [MEMory 2 | 12 ]
       [MEMory 3 | 13 ]
       [MEMory 4 | 14 ]}
```

Example: OUTPUT 707;"STORE CHANNEL2,MEMORY4"

TEST | TST

command

This command causes the instrument to perform a self-test. This is the same test that is executed when the instrument is powered up. The Tst bit in the Status Word (bit 13) will go to a 1 when the test is complete.

Command Syntax: {TEST | TST}

Example: OUTPUT 707;"TEST"

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TRANsfer | XFER

command

This command allows the movement of waveform data from one of the waveform memories to one of the pixel memories so that it may be viewed on the CRT. This command has two parameters; the first parameter is MEMORYn where n=1 through 4 and designates the source of the data as waveform memory 1,2,3, or 4, the second parameter is PLANEn where n=1 or 2 and designates the destination of the data as pixel memory 5 or 6.

If one of the waveform display memories contains data and new data is written to that memory, the new data will be superimposed on the existing data.

NOTE

When using this command only the pixel data is transferred i.e., the waveform parameters are lost.

Command Syntax: TRANsfer [memory]<waveform memory #>, [plane]<plane #>

<waveform memory #> ::= { 1 | 2 | 3 | 4 }
<plane #> ::= { 1 | 2 }

Example: OUTPUT 707;"TRANSFER MEMORY 3,PLANE 2"

TRG | GET

command

The instrument responds to this command in the same way it responds to the RUN system command and the GET bus command, (paragraph 9-16).

This command causes the instrument to acquire data for the active waveform display based on the timebase mode. If the time base mode is in SINGLE, the TRG command will cause the instrument to enable the trigger once, and display this data on the CRT. This is the same thing that happens when you press the front panel STOP\SINGLE key when the instrument has STOPPED.

If the timebase mode is AUTO or TRIGGERED, the TRG command will cause the instrument to enable the trigger repeatedly and display the acquired data on the CRT. This is the same thing that happens when you press the front panel RUN key. See MODE under the TIMEBASE subsystem in paragraph 10-13.

Command Syntax: {TRG | GET}

Example: OUTPUT 707;"TRG"

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VIEW command

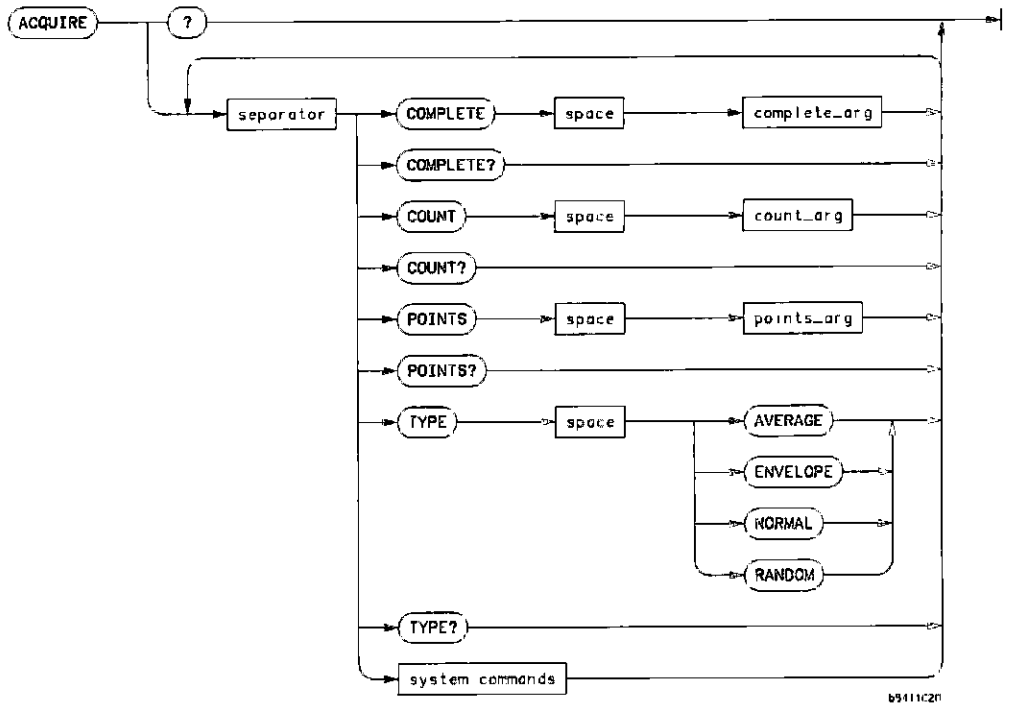
The VIEW command causes the instrument to turn on, (start displaying), an active channel, function, pixel memory or waveform memory. If you want to turn on an active display use the parameter Channel 1|2. If you want to turn on a pixel memory use the parameter PLANE 1 | 2, where plane 1 = pixel memory 5 and plane 2 = pixel memory 6. Using the VIEW MEMory { 1 | 2 | 3 | 4 } command in the split screen mode causes memories 1 and 3 to be displayed on the upper screen and memories 2 and 4 to be displayed on the lower screen.

```
Command Syntax:  VIEW {[CHANnel { 1 | 2 }]
                       [PLANe { 1 | 2 }]
                       [FUNCtion { 1 | 2 }]
                       [MEMory { 1 | 2 | 3 | 4 }]}

     Example:  OUTPUT 707;"VIEW CHANNEL 1"
```

NOTES:

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COMPLETE_ARG ::= An integer from 0 to 100, specifying, in percent, the number of buckets that must be filled before acquisition is considered complete.

COUNT_ARG ::= An integer from 1 to 2048 specifying the number of values to average for each point when in the averaged mode, and the number of values to use for each point when constructing the envelope.

POINTS_ARG ::= An integer specifying the number of points to be collected for each waveform record. Acceptable values are 128, 256, 500, 512, or 1024.

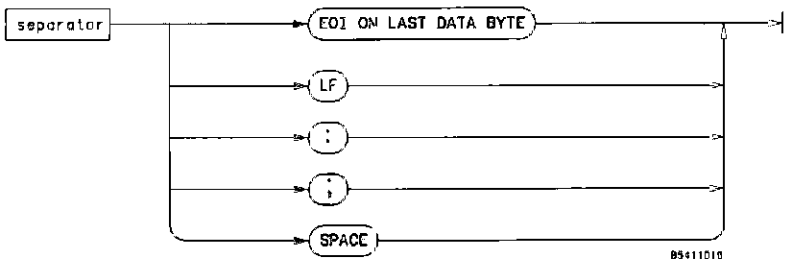


Figure 10-3. Acquire Subsystem Commands.

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10-10 THE ACQUIRE SUBSYSTEM

The Acquire subsystem commands are used to setup conditions that are used when a DIGITIZE system command is executed. This subsystem is used to select the type of data, the number of points desired, the completion criteria, and the number of averages. See figure 10-3.

ACQuire

command/query

The ACQuire command selects the acquire subsystem as the destination for the commands that follow.

The ACQuire query responds with the settings of the acquire subsystem.

Command Syntax: ACQuire

```
Example:  OUTPUT 707;"ACQUIRE"
```

Query Syntax: ACQuire?

```
Returned Format:  [ ACQuire <crlf> ]
                  [ TYPE ]<argument><crlf>
                  [ POINts ]<NR1>crlf>
                  [ COUNts ]<NR1><crlf>
                  [ COMPlete ]<NR1><crlf>

Example:  DIM Acquire$[70]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"ACQUIRE?"
          ENTER 707 USING "-K";Acquire$
          PRINT USING "K";Acquire$
```

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COMPlete

command/query

This command specifies the completion criteria for an acquisition. The parameter determines what percentage of the time buckets need to be "full" before an acquisition is considered completed. If you are in the NORMAL mode the instrument only needs one data bit in a time bucket to be considered full. In order for a time bucket to be considered full in the AVERAGED and ENVELOPE modes a specified number of data points (COUNT) must be acquired.

The parameter for this command has a range of 0 to 100 and indicates the the percentage of time buckets that have the required number of data bits i.e., are considered "full" before the acquisition is considered complete. When the completion criteria is set to 0, only a single acquisition cycle will be performed, except for sweep speeds below 2.5 ns/div where either 1 or no acquisition cycles may be performed.

Command Syntax: COMPlete <NR1>

```
Example:  OUTPUT 707;"COMPLETE 85"
```

Query Syntax: COMPlete?

```
Returned Format:  [COMPlete] <NR1><crlf>

Example:  OUTPUT 707;"COMPLETE ?"
          ENTER 707;Complete$
          PRINT Complete$
```

COUNt | CNT

command/query

When the acquisition type is AVERAGE, this command specifies the number of values to be averaged for a particular time bucket before acquisition is considered complete for that bucket. When the acquisition type is ENVELOPE, this command specifies the number of values to be used in each time bucket when constructing the envelope. This command has no effect if the TYPE is NORMAL or RANDOM. The query returns the last specified count value. The COUNt parameter can be an integer from 1 to 2048.

Command Syntax: {COUNt | CNT} <NR1>

```
Example:  OUTPUT 707;"COUNT 1854"
```

Query Syntax: {COUNt | CNT}?

```
Returned Format:  [COUNt | CNT]<NR1><crlf>

Example:  OUTPUT 707;"CNT?"
          ENTER 707;Cnt$
          PRINT Cnt$
```


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POINts | PNTS

command/query

This command specifies the number of points for each acquisition record. The command has one parameter and may be specified to be 128, 256, 500, 512 or 1024. 500 points is preferred if the acquired data is to be used for automatic measurements or function operands. There are two cases where the POINTS command has no affect:

For sweep speeds faster than 2 ns/div., the number of points is based on 10 ps resolution of the instrument's timebase. This means:

If (2.0 ns/div)>(time per div)>=(1.0 ns/div) then POINTS = 1000(500 if selected)
If (1.0 ns/div)>(time per div)>=(500 ps/div) then POINTS = 500
If (500 ps/div)>(time per div)>=(200 ps/div) then POINTS = 200
If (200 ps/div)>(time per div)>=(100 ps/div) then POINTS = 100

If the TYPE is RANDOM, the number of points is based on the number of complete data records (the points collected on each trigger) that can be gathered and not to exceed 1024. The data acquisition hardware allows the data points gathered after a trigger event to vary with time per division and delay. It can also vary by one data point from one trigger event to the next. This makes it difficult to predict the number of points that will be gathered for any DIGITIZE command when the TYPE is RANDOM. Before the data is read from the instrument with the WAVEFORM DATA? query, the WAVEFORM POINTS? query may be used to determine the actual number of points collected. The query returns the last specified value.

Command Syntax: {POINts | PNTS}

Example: OUTPUT 707;"PNTS 128"

Query Syntax: {POINts | PNTS}?

Returned Format: [POINts] <NR1><crlf>

```
Example:  OUTPUT 707;"POINTS?"
          ENTER 707;Points$
          PRINT Points$
```


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TYPE command/query

This command lets you select the type of acquisition that is to take place when a DIGITIZE system command is executed. This command has one parameter and may be one of the following:

NORMAL

Last data value to be collected in each acquisition bucket. The data is returned to the controller as a series of voltage values that represent the evenly spaced data points on the CRT.

RANDOM

The Random mode simulates the way the instrument collects data for display on the CRT. This data is returned to the controller as a list of time-voltage pairs.

AVERAGE

The average of the data values collected in each acquisition bucket. The data is returned to the controller as a series of voltage values that represent the evenly spaced data points on the CRT.

ENVELOPE

The max and min value in each acquisition bucket. The data is returned to the controller as two lists of voltage values, the min values first then the max values.

When you change TYPE to AVERAGE the front panel display mode is changed to averaged. Changing TYPE to NORMAL, ENVELOPE, or RANDOM switches the front panel display mode to Normal.

```
Command Syntax:  TYPE {[ NORMAL   | 1 ]
                      [ AVERAGE  | 2 ]
                      [ ENVELOPE | 3 ]
                      [ RANDOM   | 4 ]}

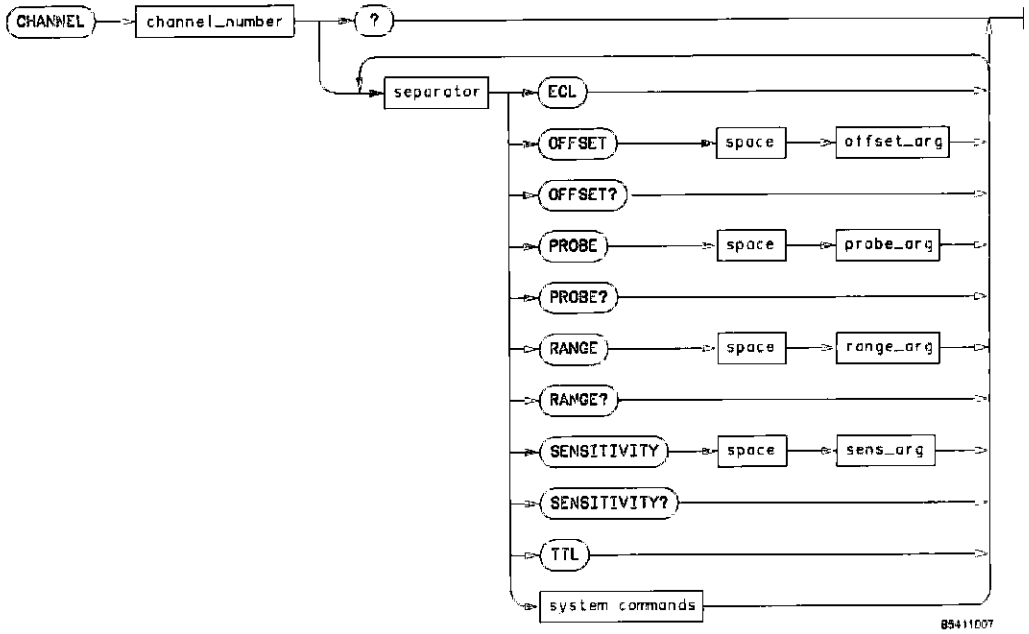
     Example:  OUTPUT 707;"ACQUIRE; TYPE RANDOM"

Query Syntax:  TYPE?

     Returned Format:  [TYPE]<argument><crlf>

     Example:  OUTPUT 707;"TYPE?"
               ENTER 707;Type$
               PRINT Type$
```


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CHANNEL_NUMBER = 1 or 2

OFFSET_ARG = A real number defining the voltage at the center of the voltage range smaller than 1.5 X voltage range.

PROBE_ARG = A real number from 1.0 to 1000.0 specifying the probe attenuation with respect to 1.

RANGE_ARG = A real number specifying the size of the acquisition window in volts. Acceptable values are 0.08, 0.16, 0.4, 0.8, 1.6, 4.0, 8.0. (With the probe attenuation ration set at 1:1)

SENS_ARG = A real number specifying the size of the acquisition window in volts/div. Acceptable values are 0.01, 0.02, 0.05, 0.1, 0.5, or 1.0 when the split screen display format is off. When the unit is in the split screen mode the acceptable values are: 0.02, 0.04, 0.1, 0.2, 0.4, 1.0, 2.0. (With the probe attenuation ratio set at 1:1)

Figure 10-4 Channel Subsystem Commands

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10-11. CHANNEL SUBSYSTEM

The CHANNEL subsystem allows you to control all vertical or Y axis functions of the 54110D. Channel 1 and channel 2 are independently programmable for all functions. See Figure 10-4.

CHANnel | CH

command/query

This command allows you to select the vertical subsystem with the specified channel designated as the destination for the subsystem commands. The query responds with all the settings for the specified channel.

Command Syntax: {CHANnel | CH} { 1 | 2 }

```
Example:  OUTPUT 707;"CHANNEL 1"
```

Query Syntax: {CHANnel | CH} { 1 | 2 }?

```
Returned Format:  [CHANnel | CH]<NR1><crlf>
                  [PROBe]<NR3><crlf>
                  [RANGe]<NR3><crlf>
                  [OFFSet]<NR3><crlf>
                  [COUPling]<DC><crlf>

Example:  DIM Chan$[100]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"CHANNEL 2?"
          ENTER 707 USING "-K";Chan$
          PRINT USING "K";Chan$
```

ECL

command

This command sets the vertical range and offset and the trigger level for the selected channel for optimum viewing of ECL signals. The offset and trigger level are set to -1.30 volts and the range will be set to 1.6 volts.

Command Syntax: ECL

```
Example:  OUTPUT 707;"ECL"
```


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OFFSet

command/query

This command allows you to set the voltage that is represented at center screen for the selected channel. The range of OFFSet is ± 1.5X RANGe of the selected channel.

Command Syntax: OffSet <OFFSET_ARG>

```
Example:  OUTPUT 707;"OFFSET 650E-3"
```

Query Syntax: OFFSet?

```
Returned Format:  [OFFSet] <NR3><crlf>

Example:  OUTPUT 707;"OFFSET?"
          ENTER 707;Offset$
          PRINT Offset$
```

PROBe

command/query

This command allows you specify the probe attenuation factor for the selected channel. The range of the probe attenuation factor is from 1.0 to 1000.0. This command does not change the actual input sensitivity of the 54110D, it changes the reference constants that are used for scaling the display factors and for automatic measurements, trigger levels, etc.

Command Syntax: PROBe <PROBE_ARG>

```
Example:  OUTPUT 707;"PROBE 15.5"
```

Query Syntax: PROBe ?

```
Returned Format:  [PROBe]<NR3><crlf>

Example:  OUTPUT 707;"PROBE?"
          ENTER 707;Probe$
          PRINT Probe$
```


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RANGe

command/query

This command allows you to define the full scale vertical axis of the selected channel. If you use a 1:1 probe attenuation factor the acceptable values for RANGe are: 0.08, 0.16, 0.4, 0.8, 1.6, 4.0, and 8.0. These values represent the full scale deflection factor of the vertical axis in volts. These values change as the probe attenuation factor is changed, e.g., if the probe attenuation factor is changed from 1:1 to 10:1 the Maximum RANGe value changes from 8 to 80 volts full scale. The query returns the current range setting.

Command Syntax: RANGe <RANGE_ARG>

```
Example:  OUTPUT 707;"RANGE 4"
```

Query Syntax: RANGe?

```
Returned Format:  [RANGe]<NR3><crlf>

Example:  OUTPUT 707;"RANGE?"
          ENTER 707;Range$
          PRINT Range$
```

SENSitivity

command/query

This command allows you to specify the vertical deflection in volts/division as opposed to volts full scale as specified with the RANGe command. With the probe attenuation ratio set to 1:1 the allowable values for SENSitivity when you are using the single display format are 0.010, 0.020, 0.050, 0.100, 0.200, 0.500, and 1.000. All of these values represent volts/vertical division when using the grid graticule. The SENSitivity command takes the probe attenuation ratio into account so the SENSitivity value programmed should be the desired sensitivity at the probe tip. The query returns the current sensitivity setting.

Command Syntax: SENSitivity <SENS_ARG>

```
Example:  OUTPUT 707;"SENSITIVITY 1"
```

Query Syntax: SENSitivity ?

```
Returned Format:  [SENSitivity] <NR3><crlf>

Example:  OUTPUT 707;"SENS?"
          INPUT 707;Sens$
          PRINT Sens$
```


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TTL command

This command sets the vertical range and offset and the trigger level for the selected channel for optimum viewing of TTL signals. Offset and trigger level will be set to 1.6 volts and the range will be set to 8.0 volts.

Command Syntax: TTL

```
Example: OUTPUT 707;"TTL"
```

NOTES:

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NOTES:

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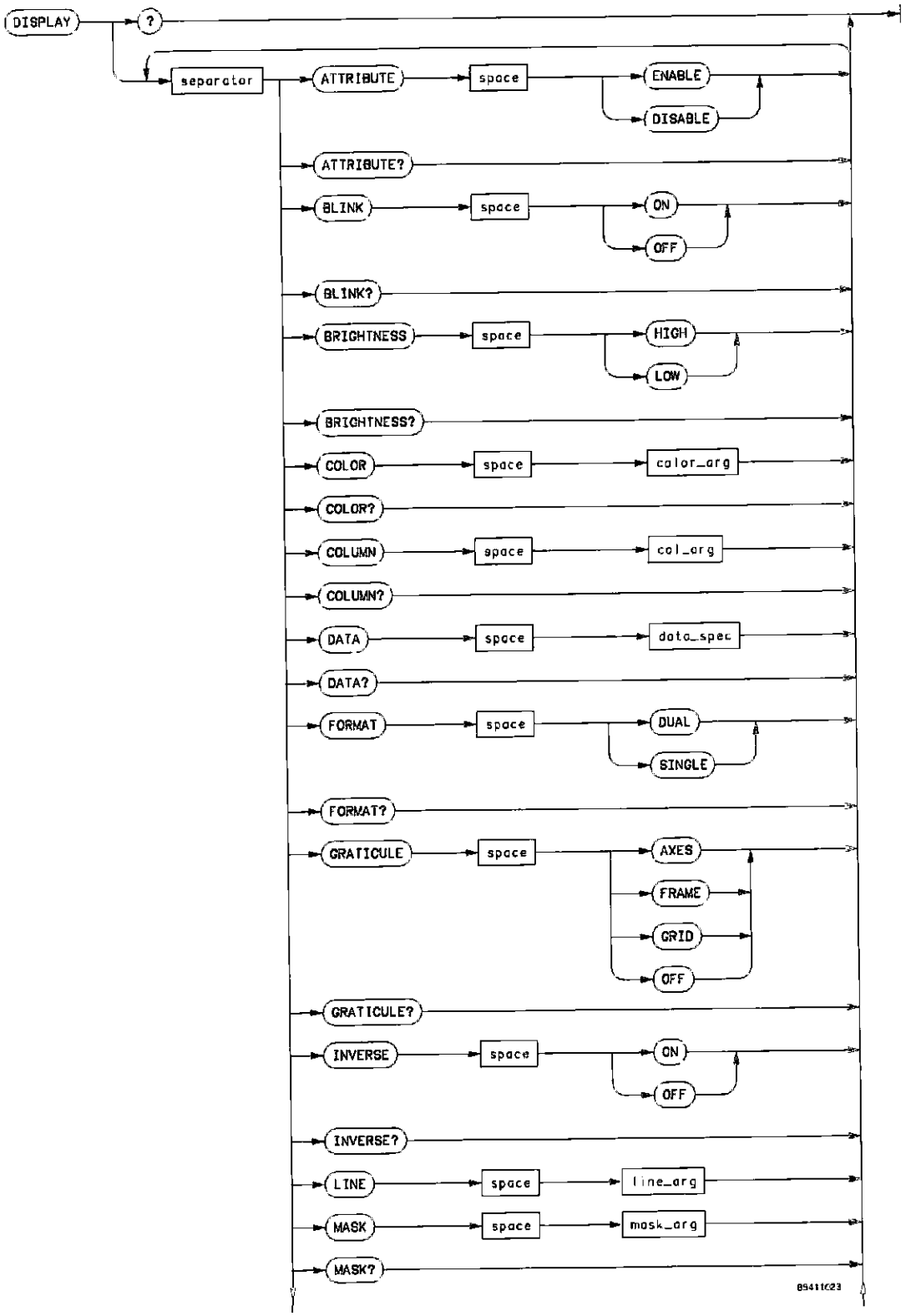


Figure 10-5 Display Subsystem Commands

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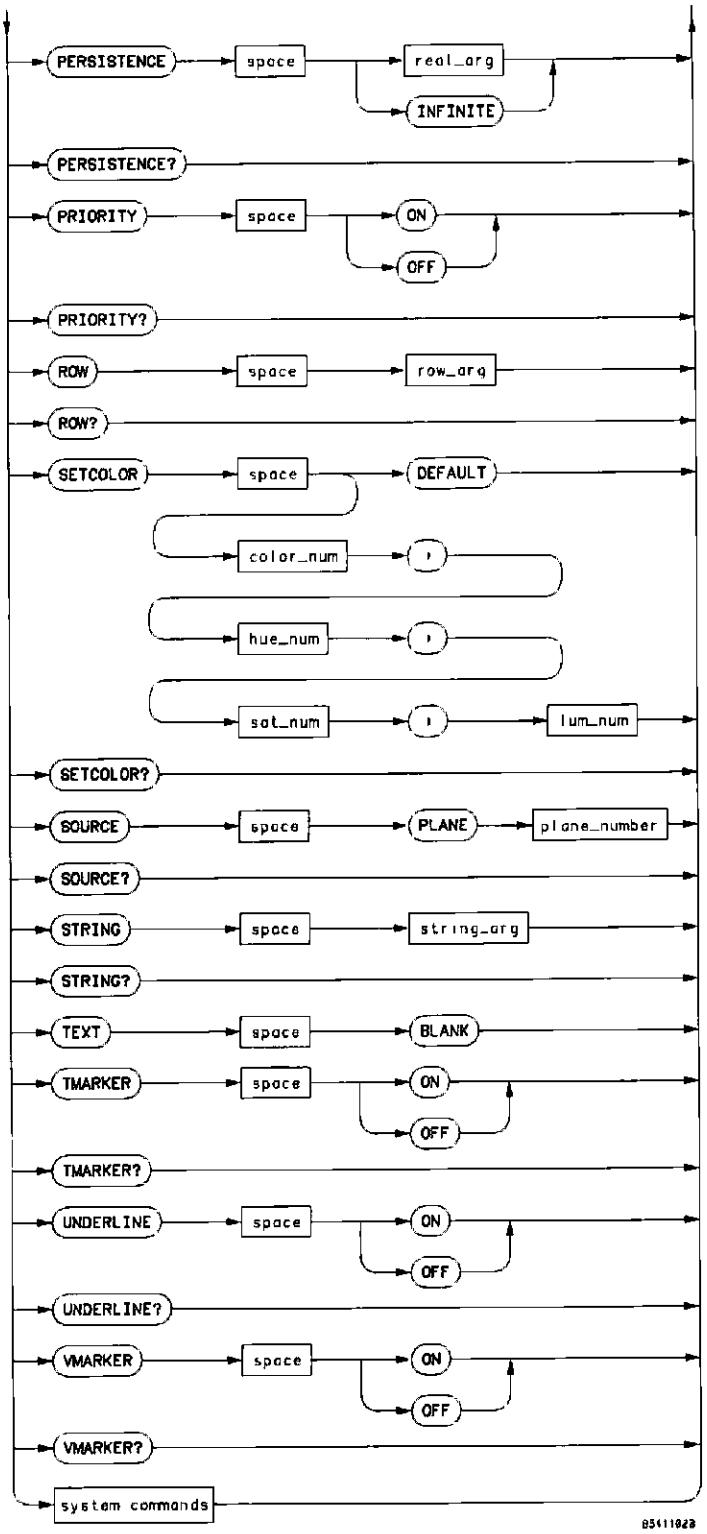


Figure 10-5. Display Subsystem Commands

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DATA_SPEC = A block of data in EA format as defined in IEEE Std. 728-1982.

PLANE_NUMBER An integer from 0 to 6.

REAL_ARG = A real number from 0.2 to 10.0 in steps of 0.1.

SCR_NUMBER = An integer from 0 to 71.

LINE_ARG = Any quoted string

ROW_NUMBER = An integer from 0 to 22.

STRING_ARG = Any quoted String.

COLOR_NUMBER = An integer from 0 to 15.

HUE_NUM = An integer from 0 to 100.

SAT_NUM = An integer from 0 to 100.

LUM_NUM = An integer from 0 to 100.

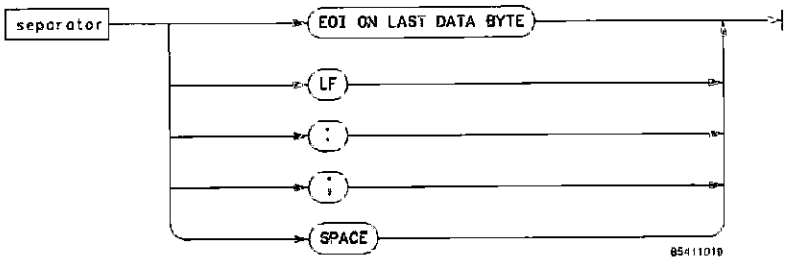


Figure 10-5. Display Subsystem Commands

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10-12. DISPLAY SUBSYSTEM

The Display subsystem is used to control the display of data, markers, text, graticules and the use of color. See Figure 10-5 for the syntax of the Display subsystem commands. The commands which control the display mode and number of averages are listed in the ACQUIRE subsystem as TYPE and COUNT.

DISPlay

command/query

This commands selects the display subsystem as the destination for the subsystem commands. The query returns all the parameters for this subsystem.

Command Syntax: DISPlay

Example: OUTPUT 707;"DISP"

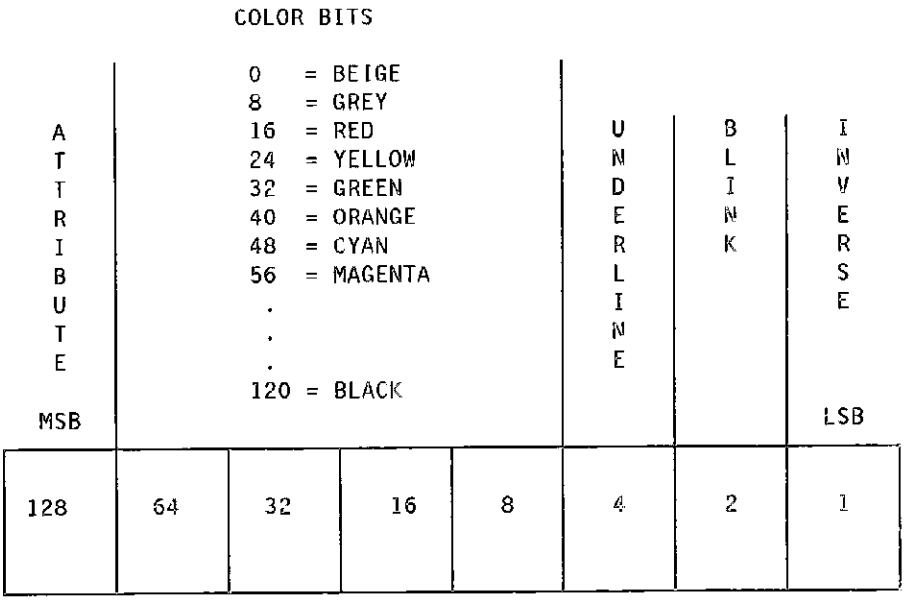
Query Syntax: DISPlay?

```
Returned Format:  [ DISPlay ]<crlf>
                  [ FORMat ]{[ SINGLE | 1 ]
                            [ DUAL | 2 ]}<crlf>
                  [ GRATicule ]{[ OFF | 0]
                               [ GRID | 1 ]
                               [ AXES | 2 ]
                               [ FRAME | 3 ]}<crlf>
                  [ ROW ]<NR1><crlf>
                  [ COLumn ]<NR1><crlf>
                  [ ATTRibute ]{[ DISABLE | 0 ]
                               [ ENABLE  | 1 ]}<crlf>
                  [ INVerse ]{[ OFF | 0 ]
                             [ ON |  1 ]}<crlf>
                  [ BLINk ]{[ OFF | 0 ]
                            [ ON  | 1 ]}<crlf>
                  [ BRIGhtness ]{[ LOW | 0 ]
                                 [ HIGH | 1 ]}<crlf>
                  [ VMARker ]{[ OFF | 0 ]
                              [ ON  | 1 ]}<crlf>
                  [ TMARker ]{[ OFF | 0 ]
                              [ ON  | 1 ]}<crlf>
                  [ PERSistence ]<NR3><crlf>
                  [ COLor ]<NR1>
                  [ PRIority ]{[ OFF | 0 ]
                               [ ON  | 1 ]}
                  [ SETColor ]  <NR1>  <NR1>  <NR1>  <NR1>
```

```
Example:  10 DIM Display$[500]
          20 OUTPUT 707;"EOI ON"
          30 OUTPUT 707;"DISPLAY?"
          40 ENTER 707 USING "-K";Display$
          50 PRINT USING "K";Display$
```

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ATTRIBUTE BYTE



When you want to set the attribute byte you must sum the binary values of the byte and send them via the HP-IB to the instrument. These selected attributes can be turned off/on by disabling/enabling the ATTRibute command. These attributes affect the text that is sent to the display of the instrument when you use the LINE or STRing commands. This example causes "HELLO" to be written in red in the upper left corner of the display using the inverse video and the blinking attributes.

```
OUTPUT 707,"DISPLAY TEXT BLANK ATTRIBUTE ENABLE"
OUTPUT 707 USING "8A,B,6A";"STRING """,128+16+2+1,"HELLO"""
```

Where 128 indicates that this is an attribute byte, 16 indicates the color red, 2 indicates the blink attribute, and 1 indicates the invert attribute. This could just as easily been output to the instrument as "147".

Figure 10-6 Attribute Byte

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ATTRibute

command/query

This command controls embedded attributes in the strings that are sent with the DISPLAY, LINE or STRING commands. Refer to Figure 10-6 for more information. These text attributes include:

INVerse
UNDerline
BLINk
COLOr

When this command is enabled the embedded attribute bytes in strings sent with the LINE or STRing commands will be used to override previously set attributes. The query returns the enable/disable state of the command.

Command Syntax: ATTRibute {[DISABLE | 0] [ENABLE | 1]}

```
Example:  OUTPUT 707;"ATTRIBUTE ENABLE"
```

Query Syntax: ATTRibute?

```
Returned format:  [ATTRibute]<argument><crlf>

Example:  OUTPUT 707;"ATTRIBUTE"
          ENTER 707;Attribute$
          PRINT Attribute$
```

BLINk

command/query

This command determines whether text sent with the DISPLAY, LINE or STRING commands is to be written with the BLINk attribute, that is, when the text is displayed it will flash on and off. The query returns the state of the BLINk attribute.

Command Syntax: BLINk {[OFF | 0]
[ON | 1]}

```
Example:  OUTPUT 707;"BLINK ON"
```

Query Syntax: BLINk?

```
Returned Format:  [BLINk]<argument><crlf>

Example:  OUTPUT 707;"BLINK?"
          ENTER 707;Blink$
          PRINT Blink$
```


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BRIGhtness

command/query

This command specifies whether text sent with the DISPLAY, LINE or STRING commands are to be displayed in beige or grey. LOW or 0 provides gray text and HIGH or 1 provides beige text. The query returns the HIGH/LOW state of the BRIGhtness attribute. This command overrides a previous COLOR commands.

```
Command Syntax:  BRIGhtness {[ LOW  | 0 ]
                            [ HIGH | 1 ]}

     Example:  OUTPUT 707;"BRIGHTNESS LOW"

Query Syntax:  BRIGhtness?

     Returned Format:  [BRIGhtness]<argument><crlf>

     Example:  OUTPUT 707;"BRIGHTNESS?"
               ENTER 707;Brightness$
               PRINT Brightness$
```

COLOr

command/query

This command specifies what color the text will be when sent with the DISPLAY, LINE or STRING commands. The query returns the color of the COLOr attribute. Colors 8-14 are not defined by the instrument but are available over HP-IB for user defined text strings. The COLumn uses the shortform COL. This command overrides a previous brightness command.

```
Command Syntax:  COLOr {[ 0 ]  (beige, highlighted text)
                       [ 1 ]  (grey, text fields & graticule)
                       [ 2 ]  (red, advisories & errors)
                       [ 3 ]  (yellow, channel 1 waveforms)
                       [ 4 ]  (green, channel 2 waveforms)
                       [ 5 ]  (orange, markers)
                       [ 6 ]  (cyan, stored waveforms)
                       [ 7 ]  (magenta, overlapped traces)
                       [ 15 ] (black, background)

     Example:  OUTPUT 707;"COLOR 2"

Query Syntax:  COLOr?

     Returned Format:  [COLOr]<argument><crlf>

     Example:  OUTPUT 707;"COLOR?"
               ENTER 707;Color$
               PRINT Color$
```


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COLumn

command/query

This command specifies the starting column for subsequent STRING and LINE commands. The query returns the column where the next LINE or STRING will start.

Command Syntax: COLumn <COL_NUMBER>
<COL_NUMBER> ::= 0..71

Example: OUTPUT 707;"COLUMN 50"

Query Syntax: COLumn?

Returned Format: [COLumn]<NR1><crlf>

```
Example:  OUTPUT 707;"COLUMN?"
          ENTER 707;Column$
          PRINT Column$
```

DATA

command/query

The DATA command is used to write to or from one of the seven pixel memory planes in the 54110D. The memory planes available are plane0 through plane6 and are specified by the DISPLAY SOURce command.

The DATA query causes the 54110D to output waveform data from the specified memory plane. If plane 0 is specified the 54110D will transfer the logical or of the channel 1 and channel 2 planes. In all other cases the specified plane will be transferred.

The DATA command is followed by a block of binary data that is transferred from the controller to a specific plane in the 54110D. If plane 0 is specified, that data will be transferred into the channel 1 plane. In all other cases the data will be transferred into the specified plane.

The data is in the form of 16032 bytes with four header bytes. The header contains:

```
<#> ::= (decimal 35)  = byte 1
<A> ::= (decimal 65)  = byte 2
        (decimal 62)  = byte 3
        (decimal 160) = byte 4
```

The third and fourth bytes make up a 16-bit integer whose value is decimal 16032, or the length of the binary block. This binary format complies with the "#A" Block Data Field in IEEE 728-1982.

(Data continued on next page)

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DATA (cont'd) command/query

Command Syntax: DATA <binary block type A>

Query Syntax: DATA?

Returned Format: [DATA]<2sp><#><A><decimal 62><decimal 160>
<binary waveform data>

```
Example:  10   CLEAR 707
          20   DIM Plane$ [17000]
          30   OUTPUT 707;"HEADER ON EOI ON"
          40   OUTPUT 707;"DISPLAY SOURCE PLANE0 DATA?"
          50   ENTER 707 USING "-K";Plane$
          60   OUTPUT 707;"SOURCE PLANE1"
          70   OUTPUT 707 USING"-K";Plane$
          80   END
```

This example transfers data from the active display memory to the controller and then back to pixel memory 5 in the 54110D.

FORMat command/query

This command allows you to turn the split screen mode on or off. FORMAT 1 turns the split screen mode off and uses 8 divisions for the full scale range FORMAT 2 turns the split screen mode on and uses 4 divisions for the full scale range. The query returns the current number of display areas on the screen.

```
Command Syntax:  FORMat { [ SINGLE | 1 ]
                         [ DUAL   | 2 ]}

     Example:  OUTPUT 707;"FORMAT SINGLE"

Query Syntax:  FORMat?

     Returned Format:  [FORMat]<argument><crlf>

     Example:  OUTPUT 707;"FORMAT?"
               ENTER 707;Format$
               PRINT Format$
```


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GRATicule

command/query

This command allows you to determine the type of graticule that is displayed. The query returns the type of graticule displayed.

Command Syntax: GRATicule {[OFF | 0]
[GRID | 1]
[AXES | 2]
[FRAME | 3]}

Example: OUTPUT 707;"GRATICULE AXES"

Query Syntax: GRATicule?

Returned Format: [GRATicule]<argument><crlf>

Example: OUTPUT 707;"GRATICULE?"
ENTER 707;Grat$
PRINT Grat$

INVerse

command/query

This command sets inverse video on or off for subsequent DISPLAY, LINE or STRING commands The query responds with the on/off state of this command.

Command Syntax: INVerse {[OFF | 0]
[ON | 1]}

Example: OUTPUT 707;"INVERSE OFF"

Query Syntax: INVerse?

Returned format: [INVerse]<argument><crlf>

Example: OUTPUT 707;"INVERSE?"
ENTER 707;Inv$
PRINT Inv$

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LINE command/query

This command causes the string parameter to be written to the screen, starting at the location established by the ROW and COLUMN commands. Text may be written up to column 62. If the characters in the string parameter does not fill the line, the rest of the line is blanked. If the string is longer than the available space on the current line the excess characters will be discarded In any case, ROW is incremented and COLUMN remains the same. The next LINE command will write on the next line of the display. After writing line 21, the last line in the display area, ROW is reset to 2 The query of this command outputs the quoted string at the current ROW and COLUMN values and causes ROW to be incremented by 1. The LINE command and query works on rows 2 through 21.

```
Command Syntax:  LINE < any quoted string >

     Example:  OUTPUT 707:"LINE ""ENTER PROBE ATTENUATION"""

Query Syntax:  LINE?

     Returned Format:  [LINE?] < quoted string ><crlf>

     Example:  DIM Line$[100]
     Example:  OUTPUT 707;"DISPLAY:ROW 12;COLUMN 14;LINE?"
               ENTER 707;Line$
               PRINT Line$
```


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MASK

command/query

This command inhibits the instrument from writing to selected areas of the screen. Text sent over the HP-IB using the line and string commands is not effected by this command. The purpose of the command is to allow HP-IB text to be written anywhere on screen and to prevent the instrument from overwriting the text through its normal operation.

The mask parameter is an 8 bit integer in which each bit controls writing to an area of the screen. A 0 inhibits writing to the area represented by the bit, and a 1 enables writing to the area. Note: This command's parameters will not be reset with a RESET command.

Command Syntax: MASK <NR1>

```
Example:  OUTPUT 707;"MASK 254" ! Inhibits advisories only
```

Query Syntax: MASK?

```
Returned Format:  [MASK]<NR1><crlf>

Example:  OUTPUT 707;"MASK?"
          ENTER 707;Mask$
          PRINT Mask$
```

Bit	Mask Weight	Screen Area Effected
7	128	Function Key Underlines - lines below the function softkeys. The underlines are turned on and off by the mask command.
6	64	Function Softkeys - Softkey labels on the right side of the display (rows 0-17, columns 62-71).
5	32	Menu Selection Softkeys - text on the bottom line of the display (row 22, columns 0-71).
4	16	Parameter Values - Text below the graticule (rows 18-21, columns 0-71)
3	8	Graticule Labels - text inside the graticule (rows 2-17, columns 0-61)
2	4	Value Label - displays value of selected knob function (row 1, columns 19-61).
1	2	Status Line - status information on the first two lines - (row 0, columns 0-71 and row 1, columns 0-18).
0	1	Advisory - Advisory and Error messages appear on row 15, columns 0-61.

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PERSistence

command/query

This command sets PERSistence for the acquired signal on the display in the Normal display mode. The display mode is set to Normal when the ACQuire TYPE is NORMAL, ENVELOPE, or RANDOM. The parameter for this command is the keyword INFINITE or a real number from 0.2 to 10.0 representing the persistence in seconds. Any value greater than 10 seconds will set the PERSistence to infinite. The query returns the value of the current persistence value. If persistence is set to infinite the query response will be 1.1E+1

Command Syntax: PERSistence { NR2 | INFINITE }

Example:
```
OUTPUT 707;"PERSISTENCE INFINITE"
```

Query Syntax: PERSistence?

Response Format: [PERSistence]<NR3><crlf>

Example:
```
DIM Pers$[30]
OUTPUT 707;"PERSISTENCE?"
ENTER 707;Pers$
PRINT Pers$
```


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PRIority

command/query

This command sets the priority on or off for subsequent DISPLAY, LINE, STRING commands. It allows you to determine whether text or graphics will be overwritten by the other on the CRT. When PRIority is ON text overwrites the displayed signal(s). When PRIority is OFF the displayed signal(s) overwrites any text in the display area.

Command Syntax: PRIority {[OFF | 0]
[ON | 1]}

Example: OUTPUT 707;"PRIORITY OFF"

Query Syntax: PRIority?

Returned Format: [PRIority]<argument><crlf>

Example: OUTPUT 707;"PRIORITY?"
ENTER 707;Pri$
PRINT Pri$

ROW

command/query

The ROW command specifies the starting row on the CRT for subsequent STRING and LINE commands. The ROW number remains constant until another ROW command is received or it is incremented by the LINE command. The single parameter for this command is an integer from 0 to 22. The query returns the row that the next LINE or STRING will start on.

Command Syntax: ROW <row number>

<row number>::= 0..22

Example: OUTPUT 707;"ROW 10"

Query Syntax: ROW?

Returned Format: [ROW]<NR1><crlf>

Example: OUTPUT 707;"ROW?"
ENTER 707;Row$
PRINT Row$

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SETColor

command/query

This command allows you to change one of the color selections on the CRT. This command has four parameters: Color Number, Hue, Saturation, and Luminosity.

The hue portion of this command allows you to determine the gradation of color. Hue can have a value of 0 to 100. As the hue number is increased, the selected color will cycle through the color spectrum. There is no difference between hue 0 and hue 100.

The saturation portion of this command allows you to choose the percentage of the pure color that gets mixed with white. The acceptable values for saturation are 0 to 100 where 0 is white and 100 is maximum saturation of the chosen hue.

The luminosity portion of this command determines the brightness of the chosen hue. The acceptable values for luminosity are 0 to 100 where 0 is black and 100 is maximum brightness. The SETColor command followed by DEFault sets all colors to the default settings. The query of this command returns the specified color number, hue, saturation, and luminosity. Refer to section 6 of this manual for more information concerning color. Note: This command's parameters will not be reset with a RESET command.

```
Command Syntax: SETColor{[<COLOR_NUM><,><HUE_NUM><,><SAT_NUM><,><LUM_NUM]
                         [ DEFault ]}

          COLOR_NUM ::= integer from 0 to 15

          HUE_NUM ::= integer from 0 to 100

          SAT_NUM ::= integer from 0 to 100

          LUM_NUM ::= integer from 0 to 100

          Example:  OUTPUT 707;"SETColor 0,0,100,50"

Query Syntax:  SETColor<color number>?

     Returned Format:  [SETColor] <NR1><,><NR1><,><NR1><,><NR1><crlf>

     Example:   DIM Set$[35]
                OUTPUT 707;"SETCOLOR 2?"
                ENTER 707;Set$
                PRINT Set$
```


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SOURce | SRC

command/query

This command allows you to specify the source or destination for the DISPLAY DATA query and command. The SOURce command has 1 parameter, PLANE0..PLANE6. The query returns the currently specified SOURce.

Command Syntax: { SOURce | SRC }
{[PLANE0 | 0] (active display)
[PLANE1 | 1] (pixel memory 5)
[PLANE2 | 2] (pixel memory 6)
[PLANE3 | 3] (graticule, markers)
[PLANE4 | 4] (displayed stored waveforms, markers)
[PLANE5 | 5] (channel 1)
[PLANE6 | 6] (channel 2)

Example:
```
10   CLEAR 707
20   DIM Plane$ [17000]
30   OUTPUT 707;"HEADER ON EOI ON"
40   OUTPUT 707;"DISPLAY SOURCE PLANE0 DATA?"
50   ENTER 707 USING "-K";Plane$
60   OUTPUT 707;"SOURCE PLANE1"
70   OUTPUT 707 USING "K";Plane$
80   END
```

This example transfers data from the active display memory to the controller and then back to pixel memory 5 in the 54110D.

Query Syntax: { SOURce | SRC }?

Returned Format: [SOURce]<argument><crlf>

Example:
```
OUTPUT 707;"SRC?"
ENTER 707;Src$
PRINT Src$
```


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STRing

command/query

This command allows you to write text to the CRT of the 54110D. The text will be written starting at the current ROW and COLUMN values. If the column limit is reached (71) the excess text is discarded. The query returns the text on the line defined by the ROW and COLUMN values.

Command Syntax: STRing <quoted string>

Example: OUTPUT 707;"STRING ""INPUT SIGNAL TO CHANNEL 2"""

Query Syntax: STRing?

```
Example:  DIM Str$[90]
          OUTPUT 707;"STRING?"
          ENTER 707;Str$
          PRINT Str$
```

TEXT

command

This command allows you to blank the user text area on the CRT. The user text area includes rows 2 through 17, columns 0 through 62, and rows 18 through 21, columns 0 through 71. This command has only one parameter, BLANk or 2.

Command Syntax: TEXT { BLANk | 2 }

```
OUTPUT 707;"TEXT 2"
```

TMARker

command/query

This command allows you to turn the time markers on or off. The query tells you whether they are on or off.

Command Syntax:
```
TMARKer{[ OFF | 0 ]
        [ ON  | 1 ]}
```

Example: OUTPUT 707;"TMAR OFF"

Query Syntax: TMARker?

Returned Format: [TMARker]<argument><crlf>

```
Example:  OUTPUT 707;"TMARKER?"
          ENTER 707;Tmar$
          PRINT Tmar$
```


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UNDerline

command/query

This command lets you underline subsequent text sent with the DISPLAY, LINE or STRING commands. The query tells you whether the UNDerline attribute is on or off.

Command Syntax: UNDerline {[OFF | 0]
[ON | 1]}

Example: OUTPUT 707;"UNDERLINE ON"

Query Syntax: UNDerline?

Returned Format: [UNDerline]<argument><crlf>

Example: OUTPUT 707;"UNDERLINE?"
ENTER 707;Under$
PRINT Under$

VMARker

command/query

This command allows you to turn the voltage markers on and off. The query tells you whether they are on or off.

Command Syntax: VMARker {[OFF | 0]
[ON | 1]}

Example: OUTPUT 707;"VMARKER ON"

Query Syntax: VMARker?

Returned Format: [VMARker]<argument><crlf>

Example: OUTPUT 707;"VMARKER?"
ENTER 707;Vmark$
PRINT Vmark$

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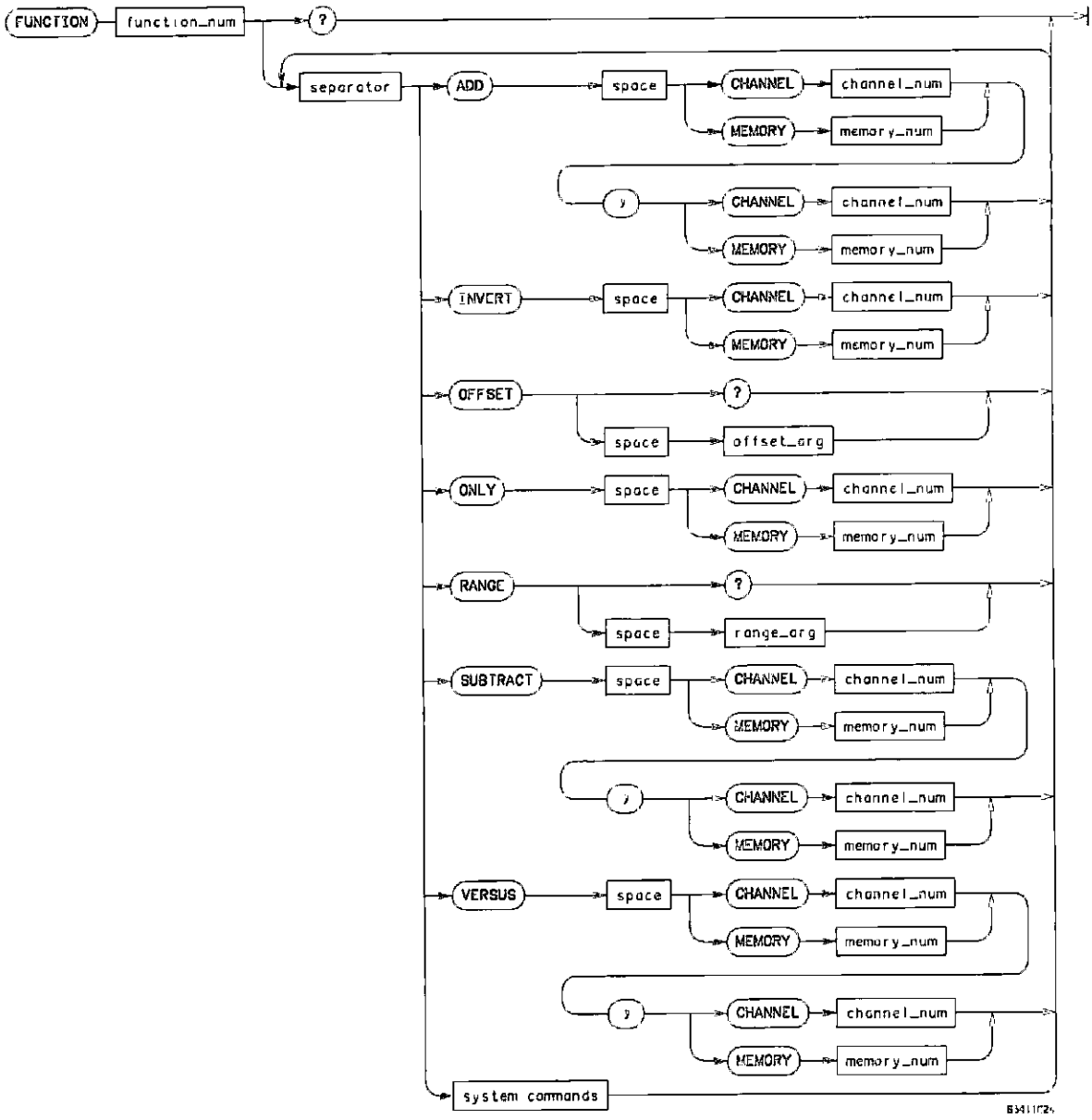


Figure 10-7. Function Subsystem Commands

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10-13. FUNCTION SUBSYSTEM

The Function subsystem allows you to define two functions using the displayed channels and/or the waveform memories as operands. The waveform operators are: ADDition, SUBTraction, INVErt, VERSus, and ONLY. The vertical scaling and offset and the display of these functions can be controlled remotely. See Figure 10-7 for a syntax diagram of the function subsystem commands.

When a function is first defined, it's initial vertical values are calculated with respect to the operands' vertical settings. The functions' range and offset may be changed using the range and offset commands. Changing any of the operands' vertical settings or redefining of the function will cause the the functions' vertical settings to be recalculated with respect to the new operand values. Any previously programmed vertical settings for the function will be lost.

The functions work on operands containing 500 points. If a function is defined and turned on, a memory which contains other than 500 points, the memory will be reformatted to 500 points. Also, memory operands that are in the RANDOM type will be reformatted to the NORMAL type with the number of points equal to 500.

FUNCtion

command/query

This command allows you to select the Function subsystem and define a waveform function. This command selects the function subsystem as the destination for the commands that follow. The query returns the definition of the selected function. Refer to Figure 10-7 for a syntax diagram of the Function subsystem commands.

Command Syntax: FUNCtion{ 1 | 2 }

```
Example:  OUTPUT 707;"FUNCTION1 ADD CHANNEL1 CHANNEL2
```

Query Syntax: [FUNCtion]{ 1 | 2 }?

```
Returned Format:  [FUNCtion]{ 1 | 2 }<crlf>
                  {ADD | INVErt| ONLY | SUBTract | VERsus}
                  {[CHANnel 1 | 2] | [MEMory 1 | 2 | 3 | 4]}<,>
                  [{[CHANnel 1 | 2] | [MEMory 1 | 2 | 3 | 4]}]<crlf>
                  [OFFSet]<NR3><crlf>
                  [RANGe]<NR3><crlf>

Example:  DIM Fun$[300]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"FUNCTION1?"
          ENTER 707 USING "-K";Fun$
          PRINT USING "K";Fun$
```

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ADD

command

The ADD command causes the unit to algebraically sum the two defined operands.

Command Syntax: ADD<operand1>[,<operand2>]

operand 1 & 2 ::= {channel 1 | channel 2 | memory 1 | memory 2 | memory 3 | memory 4}

Example: OUTPUT 707;"FUNCTION1 ADD MEMORY3,MEMORY4"

INVErt

command

This command allows you to invert the operand, that is channel 1 | 2, or memory 1 | 2 | 3 | 4. Note that the shortform of the command is INVE The INVERSE command in the display subsystem uses the short form INV.

Command Syntax: INVErt<operand>

Example: OUTPUT 707;"FUNCTION2 INVERT MEMORY3"

OFFSet

command/query

The OFFSet command allows you to define the vertical voltage at center screen for the selected function. The query returns the voltage at center screen for the defined function.

Command Syntax: OFFSet<Offset_Arg>

Example: OUTPUT 707;"FUNCTION1 OFFSET .05"

Query Syntax: OFFSet?

Returned Format: [OFFSet]<NR3>

```
Example: DIM Off$[30]
         OUTPUT 707;"FUNCTION2 OFFSET?"
         ENTER 707;Off$
         PRINT Off$
```


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ONLY

command

The ONLY command allows you to define a function as either channel 1 or 2, or memory 1, 2, 3, or 4. The ONLY command is useful for scaling channels and memories.

Command Syntax: ONLY<operand>

Example: OUTPUT 707;"FUNCTION1 ONLY MEMORY1"

RANGe

command/query

This command allows you to define the full scale vertical axis of a function's display.

Command Syntax: RANGe<Range_Arg>

Example: OUTPUT 707;"FUNCTION1 RANGE .01"

Query Syntax: RANGe?

Returned Format: [RANGe]<NR3>

```
Example:  DIM Range$[30]
          OUTPUT 707;"RANGE?"
          ENTER 707;Range$
          PRINT Range$
```

SUBTract

command

This command allows you to algebraically subtract one operand from another. Operand2 is subtracted from operand1.

Command Syntax: SUBTract <operand1><,><operand2>

```
operand1 & 2 ::= {channel1 |channel2 | memory1 |
                  memory2 | memory3 | memory4}
```

Example: OUTPUT 707;"FUNCTION2 SUBTRACT CHANNEL1,CHANNEL2"

(In this example channel 2 would be algebraically subtracted from channel 1.)

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VERSus **command**

This command allows X vs Y displays with two operands. The first operand defines the Y axis and the second defines the X axis. The Y axis range and offset is initially equal to the first operand's and can be adjusted using the range and offset commands in this subsystem. The X axis range and offset is always equal to that of the second operand. It can only be changed by changing the vertical settings of the second operand. This will also change the Y axis vertical sensitivity and offset.

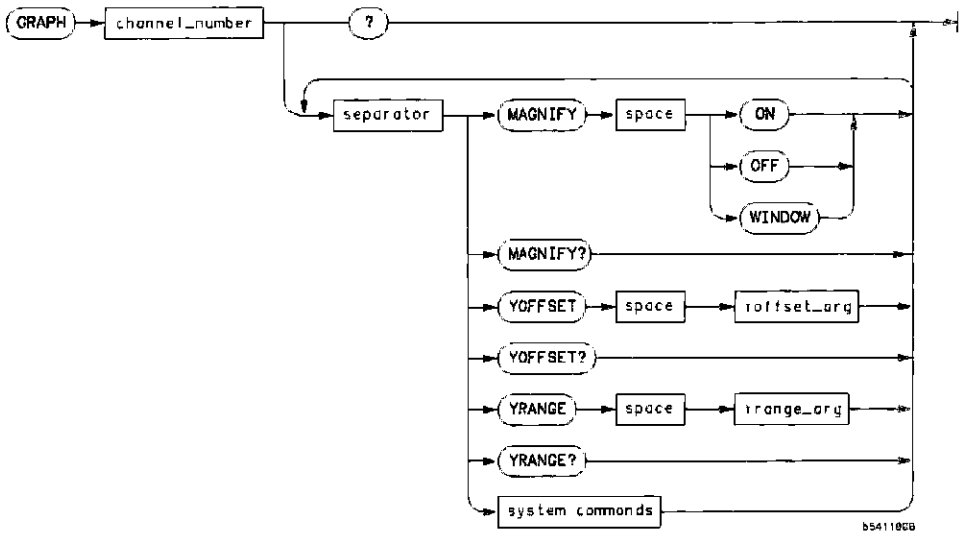
Command Syntax: VERSus<operand1><,><operand2>

operand1 & 2 ::= {channel 1 | channel 2 | memory 1 | memory 2 | memory 3 | memory 4}

Example: OUTPUT 707;"FUNCTION2 VERSUS CHANNEL1,MEMORY3"

NOTES:

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YOFFSET_ARG = A real number less than or equal to the vertical range.

YRANGE_ARG = A real number between 1/16(vertical range) and the vertical range.

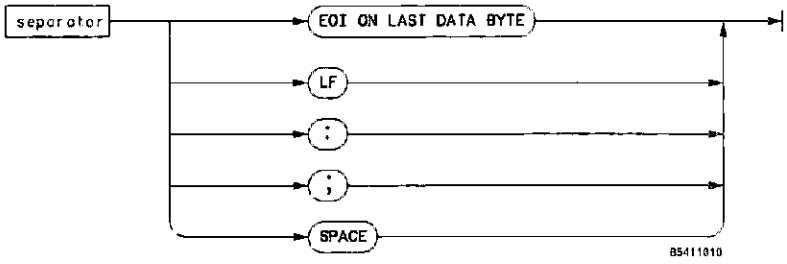


Figure 10-8 Graph Subsystem Commands

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10-14. GRAPH SUBSYSTEM

The Graph subsystem allows you to control y-axis windowing, offset and the magnification for the two channels. See Figure 10-8 for a syntax diagram of the GRAPh subsystem commands.

GRAPh

command/query

This command allows you select the graph subsystem and specify which input channel will be the destination for the graph subsystem commands that follow. The query responds with all the parameters in the subsystem.

Command Syntax: GRAPh { 1 | 2 }

Example: OUTPUT 707;"GRAPH1"

Query Syntax: GRAPh { 1 | 2 }?

Returned Format: [GRAPh]<NR1><crlf>
[MAGNify]<argument><crlf>
[YOFfset]<NR3><crlf>
[YRANge]<NR3><crlf>

```
Example:  DIM Graph$[100]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"GRAPH1?"
          ENTER 707 USING "-K";Graph$
          PRINT USING "-K";Graph$
```

MAGNify

command/query

This command controls the MAGNify function for a specific channel. This command has one parameter: OFF, ON, or WINDOW. Off specifies that the channel will be displayed on the CRT in the unmagnified form. On specifies that the channel will be displayed in the magnified form. Window specifies that the channel will be displayed in the unmagnified form with the magnifier window displayed. The window is only displayed when the menu for the specified channel is on.

Command Syntax: MAGNify {[OFF | 0][ON | 1][WINDOW | 2]}

Example: OUTPUT 707;"MAGNIFY OFF"

Query Syntax: MAGNify?

Returned Format: [MAGNify]<argument><crlf>

```
Example:  OUTPUT 707;"MAGNIFY?"
          ENTER 707;Mag$
          PRINT Mag$
```


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YOFfset

command/query

This command allows you to control the voltage at the center of the magnify window. This voltage must be within the vertical range that is setup with the CHANNELn RANGE and OFFSET commands. The query returns the current value of YOFfset.

Command Syntax: YOFfset { NR1 | NR2 | NR3 }

```
Example:  OUTPUT 707;"YOFFSET 1E-3"
```

Query Syntax: YOFfset?

```
Returned Format:  [YOFfset]<NR3><crlf>

Example:  OUTPUT 707;"YOFFSET?"
          ENTER 707;Y$
          PRINT Y$
```

YRANge

command/query

This command allows you to control the size (in volts) of the magnify window. The combination of this command and the YOFfset command must define a window that is completely enclosed by the vertical range that is setup with the CHANneln RANGe and OFFSet commands. The query returns the current value of YRANge.

Command Syntax: YRANge { NR1 | NR2 | NR3 }

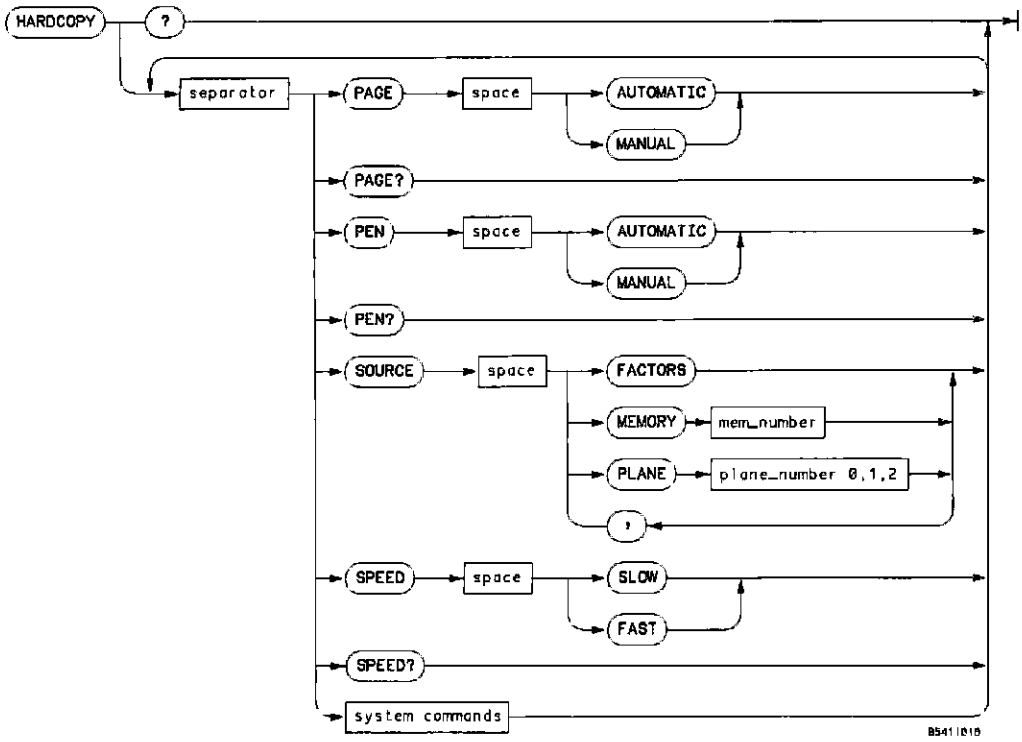
```
Example:  OUTPUT 707;"YRANGE .01"
```

Query Syntax: YRANge?

```
Returned Format:  [YRANge]<NR3><crlf>

Example:  OUTPUT 707;"YRANGE?"
          ENTER 707;Yr$
          PRINT Yr$
```


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MEM_NUMBER = An integer from 11 to 14.
PLANE_NUMBER = An integer from 0 to 2.

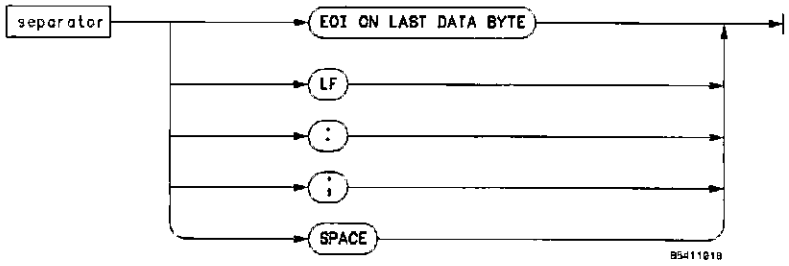


Figure 10-9. Hardcopy Subsystem commands

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10-15. HARDCOPY SUBSYSTEM

The commands in the HARDcopy subsystem allow you to set various parameters used during the plotting and printing waveforms from the 54110D. Refer to Figure 10-9 for the syntax diagram of the HARDcopy subsystem commands.

HARDcopy

command/query

The HARDcopy command selects the hardcopy subsystem as the destination for the commands that follow.

Command Syntax: HARDcopy

```
Example:  OUTPUT 707;"HARDCOPY"
```

Query Syntax: HARDcopy?

```
Returned Format:  [HARDcopy]<crlf>
                  [PAGE]<argument><crlf>
                  [PEN]<argument><crlf>
                  [SPEed]<argument><crlf>

Example:  DIM Hard$[100]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"HARDCOPY?"
          ENTER 707 USING "-K";Hard$
          PRINT USING "-K";Hard$"
```

PAGE

command/query

The page command allows you to send a form feed after a hardcopy dump to a printer. During a hardcopy dump the 54110D ignores page boundaries. The query returns the current state of the page command parameter.

Command Syntax: PAGE {[MANual | 0]
[AUTOmatic | 1]}

```
Example:  OUTPUT 707;"PAGE AUTO"
```

Query Syntax: PAGE?

```
Returned Format:  [PAGE]<argument><crlf>

Example:  OUTPUT 707;"PAGE?"
          ENTER 707;Page$
          PRINT Page$
```


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PEN

command/query

The PEN command allows you to set the 54110D's pen control function. When this command is set to AUTOmatic the unit assigns the following pen numbers to these functions:

Pen #	Usage
1	Graticule and timebase factors
2	Channel 1 and associated factors
3	Waveform memories and associated factors
4	Channel 2 and associated factors
5	Markers and delta measurement results
6	Pixel memories

When the command is put in the MANual mode the plotter will not be instructed to select a pen when a plot is requested, at the completion of the plot an instruction will be sent to cause the plotter to put away the pen. The query returns the state of the pen control parameter.

Command Syntax: PEN {[MANual | 0]
[AUTOmatic | 1]}

Example: OUTPUT 707;"PEN AUTOMATIC"

Query Syntax: PEN?

Returned Format: [PEN]<argument><crlf>

Example: OUTPUT 707;"PEN?"
ENTER 707;Pen$
PRINT Pen$

SOURce | SRC

command

The SOURce command specifies the source(s) to be output during a hardcopy dump. Commas should be used when specifying multiple sources.

Command Syntax: { SOURce | SRC }
{[PLANe0 | 0] (active display)
[PLANe1 | 1] (pixel memory 5)
[PLANe2 | 2] (pixel memory 6)
[FACTors | 4] (scale factors)
[MEMory1 | 11] (waveform memory 1)
[MEMory2 | 12] (waveform memory 2)
[MEMory3 | 13] (waveform memory 3)
[MEMory4 | 14]} (waveform memory 4)

Example: OUTPUT 707;"SOURCE PLANE2,MEMORY1"

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SPEed

command/query

The SPEed command allows you to specify the pen speed to be used during plotting. FAST is intended for use on normal paper and SLOW should be used when plotting transparencies. The query returns the current pen speed

Command Syntax: SPEed {[SLOW | 0]
[FAST | 1]}

Example: OUTPUT 707;"SPEED FAST"

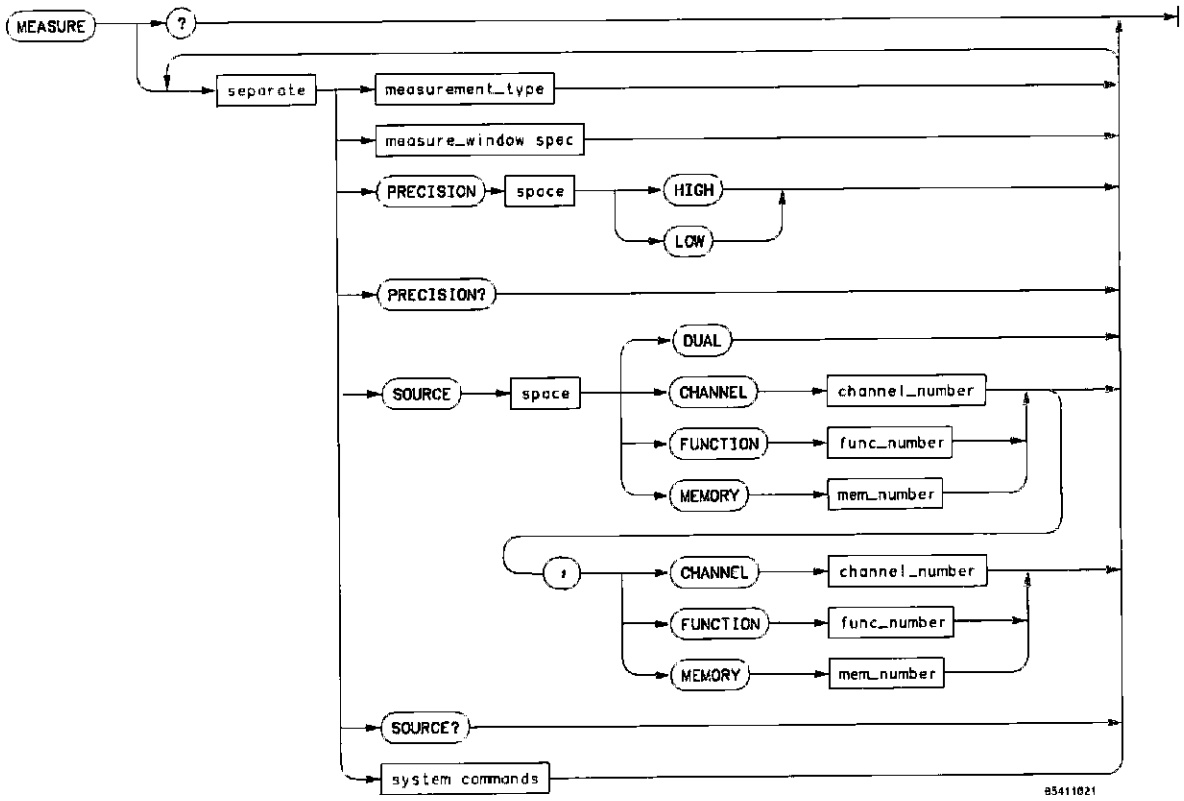
Query Syntax: SPEed?

Returned Format: [SPEed]<argument><crlf>

Example: OUTPUT 707;"SPEED?"
ENTER 707;Speed$
PRINT Speed$

NOTES:

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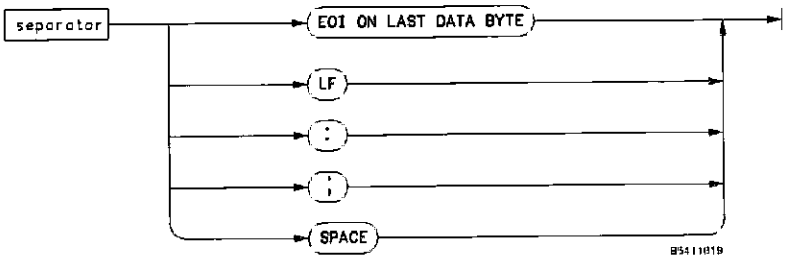


Figure 10-10. Measure Subsystem Commands

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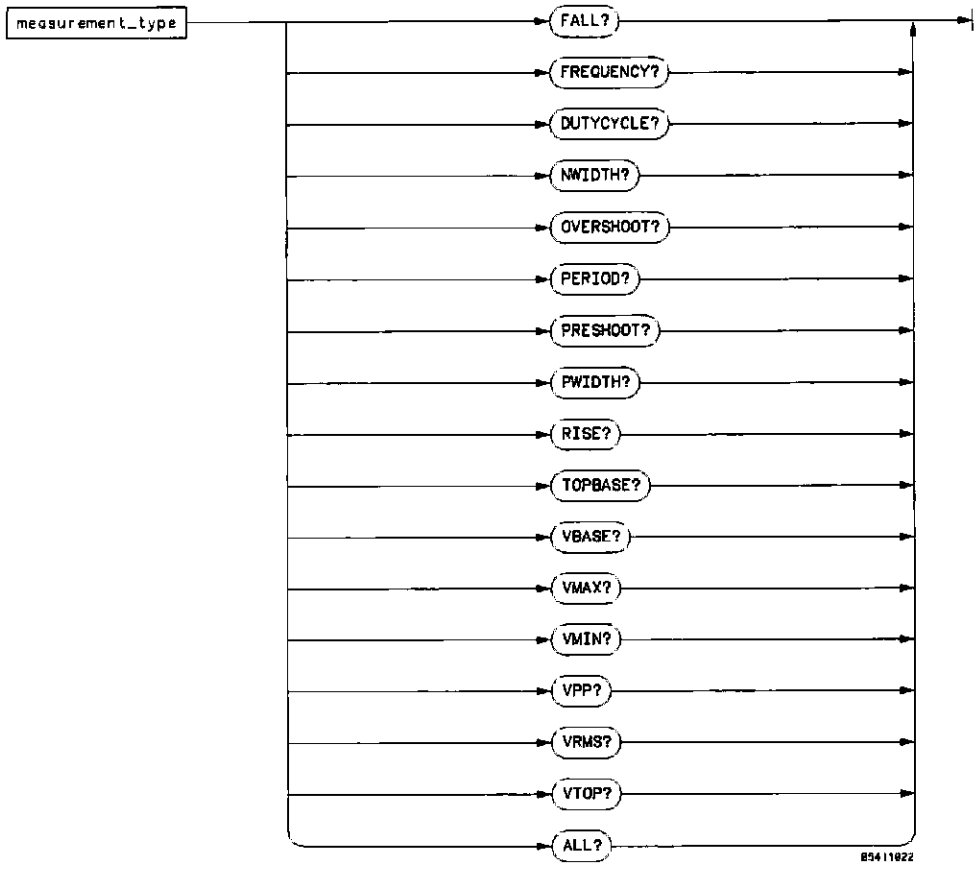


Figure 10-10. Measure Subsystem Commands

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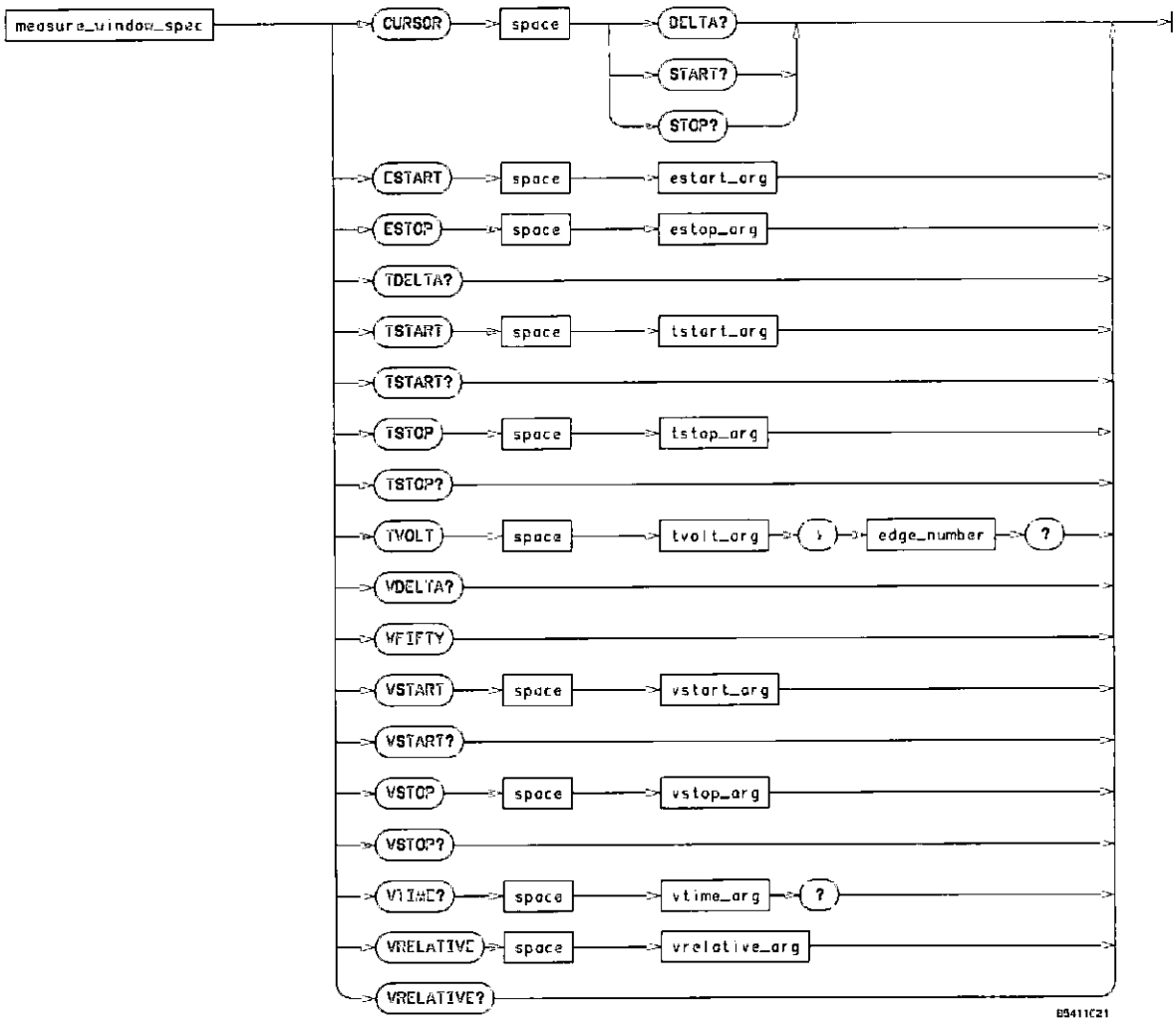


Figure 10-10. Measure Subsystem Commands

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CHANNEL_NUMBER = An integer, 1 or 2

EDGE_NUMBER = An integer from 1 to 100.

FUNC_NUMBER = An integer from 1 to 2.

MEM_NUMBER = An integer from 1 to 4.

VTIME_ARG = A real number that is within the horizontal display window.

VSTART_ARG = A real number <=2 X voltage range.

VSTOP_ARG = A real number <=2 X voltage range.

TSTART_ARG = A real number with the following restrictions:

```
Maximum is 60,000 X timebase range or 1.6sec, whichever is greater
If the delay reference is left
  then minimum is 200 ms or -(timebase range), whichever is smaller
Else if the delay reference is center
  then minimum is -5(timebase range) or -200 ms+(timebase range)
  whichever is smaller.
Else if the delay reference is right
  then minimum is 0 or -200 ms+10(timebase range),
  whichever is smaller.
```

TSTOP_ARG = A real number with the same restrictions as TSTART_ARG.

ESTART_ARG = An integer between 0 and 100.

ESTOP_ARG = An integer between 0 and 100.

VREL_ARG = An integer 0, 10, 20, 50.

Figure 10-10 Measure Subsystem Commands

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10-16. MEASURE SUBSYSTEM

The commands in the MEASure subsystem allow you to make pulse parameter and voltage measurements. You may also make custom measurements using the voltage and time markers. Pulse parameter measurements are made on the left side of the display. If there isn't enough signal present on the display to make a measurement, 1E38 is returned. Measurements are made using previously specified PRECision. If PRECision is set to LOW, the waveform will not be expanded. If PRECision is set HIGH the unit will attempt to increase the precision of the measurement by making the sweep faster. Low precision measurements typically are accomplished faster than high precision measurements because of the additional time required for expansion. All predefined pulse parameter measurements cause an Auto Top-Base operation to be preformed on the displayed signal. This operation determines the 10, 90, and 50 percent levels that are used to make the measurements. For more detailed information concerning the automated measurements refer to Appendix C. Refer to Figure 10-10 for a syntax diagram of the measure subsystem commands.

MEASure

command/query

The MEASure command selects the measure subsystem as the destination for the commands that follow. The query responds with selected measurement parameters.

Command Syntax: MEASure

```
Example:  OUTPUT 707;"MEASURE"
```

Query Syntax: MEASure?

```
Returned Format:  [MEASure]<crlf>
                  [SOURce][CHANnel]<NR1>[FUNCtion]<NR1>
                     [MEMory]<NR1><crlf>
                  [PRECision]<argument><crlf>
                  [VDELta]<NR3><crlf>
                  [VSTArt]<NR3><crlf>
                  [VSTOp]<NR3><crlf>
                  [TDELta]<NR3><crlf>
                  [TSTArt]<NR3><crlf>
                  [TSTOp]<NR3><crlf>

Example:  DIM Mea$[200]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"MEASURE?"
          ENTER 707 USING "-K";Mea$
          PRINT USING "K";Mea$
```

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ALL?

query

This query makes as many measurements as possible on the displayed signal and buffers the answers for output over HP-IB. If the measurement cannot be made the instrument will respond with 1.00000E+38.

Query Syntax: ALL?

Returned Format:
```
[FREQuency]<NR3><crlf>
[PERiod]<NR3><crlf>
[PWIDth]<NR3><crlf>
[NWIDth]<NR3><crlf>
[RISE]<NR3><crlf>
[FALL]<NR3><crlf>
[TOPBase]<NR3><crlf>
[VPP]<NR3><crlf>
[PREShoot]<NR3><crlf>
[OVERshoot]<NR3><crlf>
[DUTYcycle]<NR3><crlf>
[VRMS]<NR3><crlf>
[VMAX]<NR3><crlf>
[VMIN]<NR3><crlf>
[VTOP]<NR3><crlf>
[VBASe]<NR3><crlf>
```

Example:
```
DIM All$[500]
OUTPUT 707;"EOI ON"
OUTPUT 707;"ALL?"
ENTER 707 USING "-K";"All$"
PRINT USING "K";All$
```

CURSor?

query

This query returns time and voltage values of the specified marker as an ordered pair of time/voltage values. If delta is specified the instrument returns the value of delta V and delta T. If start is specified the positions of Vmarker1 and the start marker are returned. If stop is specified the positions of Vmarker2 and the stop marker are returned.

Query Syntax:
```
CURSor {[ DELTA | 0 ]
        [ START | 1 ]
        [ STOP  | 2 ]}?
```

Returned Format:
```
[CURSor]<NR3><,><NR3><crlf>
```

Example:
```
DIM Cursor$[30]
OUTPUT 707;"CURSOR1?"
ENTER 707;Cursor$
PRINT Cursor$
```


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DUTYcycle? | DUT?

query

This query causes the instrument to determine the duty cycle of the signal. The pulse width is measured at the 50% voltage point. The duty cycle is computed using the following formula:

duty cycle = (+pulse width/period) X 100

Query Syntax: { DUTYcycle | DUT }?

Returned Format. [DUTYcycle]<NR3><crlf>

```
Example:  DIM Dut$[30]
          OUTPUT 707;"DUTYCYCLE?"
          ENTER 707;Dut$
          PRINT Dut$
```

ESTArt

command/query

This command causes the instrument to position the start marker on the specified edge and slope at the voltage level corresponding to voltage marker 1. A positive integer looks for a specific positive transition and a negative integer looks for a specific negative transition through the voltage level equal to the voltage level of voltage marker 1. The query responds with the currently specified edge.

Command Syntax: ESTArt<NR1>

```
Example:  OUTPUT 707;"ESTART 2"
```

Query Syntax: ESTArt?

Returned Format: [ESTART]<NR1><crlf>

```
Example:  OUTPUT 707;"ESTART?"
          ENTER 707;Es$
          PRINT Es$
```


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ESTOp

command/query

This command causes the instrument to position the stop marker on the specified edge and slope at the voltage level corresponding to voltage marker 2. A positive integer looks for a specific positive transition and a negative integer looks for a specific negative transition through the voltage level equal the level of voltage marker 2. The query returns the currently specified edge.

Command Syntax: ESTOp

Example: OUTPUT 707;"ESTOP-2"

Query Syntax: ESTOP?

Returned Format: [ESTOP]<NRI><crlf>

```
Example:  OUTPUT 707;ESTOP?
          ENTER 707;Es$
          PRINT Es$
```


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FALL?

query

This query causes the instrument to measure the fall time of the first falling edge whose 10% and 90% points are on screen using the formula

fall time = time at 10% point - time at 90% point.

Query Syntax: FALL?

Returned Format: [FALL]<NR3><crlf>

```
Example:  OUTPUT 707;"FALL?"
          ENTER 707;Fall$
          PRINT Fall$
```

FREQuency?

query

This query causes the instrument to measure the frequency of the first complete period on screen using the 50% levels. The algorithm used is:

```
if first edge on screen is rising
     then
        frequency = 1/(time at second rising edge
                       - time at first rising edge)
     else
        frequency = 1/(time at second falling edge
                       - time at first falling edge)
```

Query Syntax: FREQuency?

```
Example:  DIM Freq$[30]
          OUTPUT 707;"FREQuency?"
          ENTER 707;Freq$
          PRINT Freq$
```


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NWIDth?

query

This query causes the instrument to measure the negative pulse width of the first negative pulse on screen using the 50% levels The algorithm used is:

```
if first edge on screen is rising
     then
        width = (time at second rising edge
                 - time at first falling edge)
     else
        width = (time at first rising edge
                 - time at first falling edge)
```

Query Syntax: NWIDth?

Returned Format: [NWIDth]<NR3><crlf>

```
Example:  DIM Nwid$[30]
          OUTPUT 707;"NWIDTH?"
          ENTER 707;Nwid$
          PRINT Nwid$
```

OVERshoot?

query

This query causes the instrument to measure the overshoot of a selected signal. Overshoot uses the first edge on screen using the following algorithm

```
if the first edge on screen is rising
   then
      overshoot = Vmax - Vtop
   else
      overshoot = Vbase - Vmin
```

Query Syntax: OVERshoot?

Returned format: [OVERshoot]<NR3><crlf>

```
Example:  DIM Over$[30]
          OUTPUT 707;"OVERSHOOT?"
          ENTER 707;Over$
          PRINT Over$
```


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PERiod?

query

This command causes the instrument to measure the period of the first complete cycle on screen using the 50% level. The algorithm is:

```
if first edge on screen is rising
   then
      period = (time at second rising edge
                - time at first rising edge)
   else
      period = (time at second falling edge
                - time at first falling edge)
```

Query Syntax: PERiod?

Returned format: [PERiod]<NR3><crlf>

```
Example:  DIM Period$[30]
          OUTPUT 707;"PERIOD?"
          ENTER 707;Period$
          PRINT Period$
```

PRECision

command/query

This command allows you to specify the precision that is used on subsequent measurements. When PRECision is set to HIGH the edges used for making a measurement are evaluated by making the sweep speed faster until the edge has a slope of approximately 45 degrees or the limit of the horizontal system has been reached. This increases the resolution of the measurement. When PRECision is set to LOW no horizontal expansion is accomplished. Low precision allows you increase measurement speed with the potential of reduced accuracy.

Command Syntax: PRECision {[LOW | 0]
[HIGH | 1]}

Example: OUTPUT 707;"PRECISION LOW"

Query Syntax: PRECision?

Returned Format: [PRECision]<argument><crlf>

```
Example:  DIM Prec$[30]
          OUTPUT 707;"PREC?"
          ENTER 707;Prec$
          PRINT Prec$
```


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PREShoot?

query

This query causes the instrument to measure the preshoot of the selected SOURce. The PREShoot command uses the first edge on screen using the following algorithm:

```
if the first edge on screen is rising
   then
      preshoot = Vbase - Vmin
   else
      preshoot = Vmax - Vtop
```

Query Syntax: PREShoot?

Returned Format: [PREShoot]<NR3><crlf>

```
Example:  DIM Pres$[30]
          OUTPUT 707;"PRESHOOT?"
          ENTER 707;Pres$
          PRINT Pres$
```

PWIDth?

query

This query causes the instrument to measure the positive pulse width of the first positive pulse on screen using the 50% levels. The algorithm used is:

```
if first edge on screen is falling
   then
      width = (time at second falling edge
               - time at first rising edge)
   else
      width = (time at first falling edge
               - time at first rising edge)
```

Query Syntax: PWIDth?

Returned Format: [PWIDth]<NR3><crlf>

```
Example:  DIM Pw$[30]
          OUTPUT 707;"PWIDTH?"
          ENTER 707;Pw$
          PRINT Pw$
```


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RISE? query

This query causes the instrument to measure the rise time of the first rising edge whose 10% and 90% points are on screen using the formula:

rise time = (time at 90% point - time at 10% point)

Query Syntax: RISE?

Returned Format: [RISE]<NR3><crlf>

```
Example:  OUTPUT 707;"RISE?"
          ENTER 707;Rise$
          PRINT Rise$
```

SOURce | SRC command/query

This command selects the source(s) to be used for subsequent measurements. If the source is specified as CHANnel1 or CHANnel2, that channel will be used as the source for subsequent MEASure commands. For dual measurements, 2 parameters are specified after the source command. Vmarker 1 the start marker will be assigned to the first and Vmarker 2 and the stop marker will be assigned to the second. If the keyword DUAL is used as the measurement source the markers will be assigned to chan 1 and 2 respectively. The marker measurement commands that work in DUAL are: ESTART, ESTOP, TSTART, TSTOP, TDELTA, VSTART, VSTOP, AND VDELTA.

```
Command Syntax: { SOURce | SRC }{[ DUAL | 0 ]          | [<,>
                                 [ CHANnel1 | 1 ]     | {[CHANnel1 | 1 ]
                                 [ CHANnel2 | 2 ]     |  [CHANnel2 | 2 ]
                                 [ FUNCtion1 | 9 ]    |  [FUNCtion1 | 9 ]
                                 [ FUNCtion2 | 10 ]   |  [FUNCtion2 | 10 ]
                                 [ MEMory1 | 11 ]     |  [MEMory1 | 11 ]
                                 [ MEMory2 | 12 ]     |  [MEMory2 | 12 ]
                                 [ MEMory3 | 13 ]     |  [MEMory3 | 13 ]
                                 [ MEMory4 | 14 ]}    |  [MEMory4 | 14 ]}]

     Example:  OUTPUT 707;"SOURCE CHANNEL1;MEMORY1"

Query Syntax:  { SOURce | SRC }?

     Returned Format:  [ SOURce | SRC ]<argument><crlf>

     Example:  DIM Src$[50]
               OUTPUT 707;"SRC?"
               ENTER 707;Src$
               PRINT Src$
```


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TOPBase?

query

This query returns the signal amplitude using the formula:

amplitude = Vtop -Vbase

Vtop and Vbase are located using a histogram of the voltage values of the waveform record. After a waveform record is collected the absolute min and max voltages are determined and a histogram of the voltage values is completed. Next, the waveform record is scanned to find the voltage values with the largest number of data points. If the maximum number of data points is greater than the limit criteria (approximately 5% of the maximum number of points in the record) that voltage level is used for the top or the base. If the limit criteria is not satisfied the absolute min, max values are used as the base and the top.

Query Syntax: TOPbase?

Returned Format: [TOPBase]<NR3><crlf>

```
Example:  DIM Top$[30]
          OUTPUT 707;"TOPBASE?"
          ENTER 707;Top$
          PRINT Top$
```

TDELta?

query

This query returns the time difference between the start and stop time markers, that is;

Tdelta = Tstop - Tstart

Where Tstart is the time at the start marker and Tstop is the time at the stop marker.

Query Syntax: TDELta?

Returned Format: [TDELta]<NR3><crlf>

```
Example:  DIM Td$[30]
          OUTPUT 707;"TDELTA?"
          ENTER 707;Td$
          PRINT Td$
```


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TSTArt

command/query

This command moves the start marker to the specified time with respect to the trigger time. The query returns the start marker position.

Command Syntax: TSTArt<start marker time>

```
Example:  OUTPUT 707;"TSTArt -.001"
```

Query Syntax: TSTArt?

```
Returned Format:  [TSTArt]<NR3><crlf>

Example:  DIM Ts$[30]
Example:  OUTPUT 707;"TSTART?"
          ENTER 707;Ts$
          PRINT Ts$
```

TSTOp

command/query

This command moves the stop marker to a specified time with respect to the trigger. The query returns the stop marker position.

Command Query: TSTOp<stop marker time><crlf>

```
Example:  OUTPUT 707;"TSTOP -1.0E-6"
```

Query Syntax: TSTOp?

```
Returned Format:  [TSTOp]<NR3><crlf>

Example:  DIM Ts$[30]
          OUTPUT 707;"TSTOP?"
          ENTER 707;Ts$
          PRINT Ts$
```


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TVOLt? query

When the TVOLt query is sent, the on screen signal is searched for the defined voltage level and transition. The time interval between the trigger event and this defined occurrence is returned as the response to this query.

The sign of <slope & occurrence> selects a rising(+) or falling(-) edge. The magnitude of this parameter defines the number of occurrences. For example, if <slope & occurrence> = +3 the on screen signal would be searched for the third occurrence of the specified voltage on a positive slope.

Query Syntax: TVOLt<voltage><,><slope & occurrence>?

Returned Format: [TVOLt]<NR3><crlf>

```
Example:  DIM Tvolt$[30]
          OUTPUT 707;"TVOLT -.250,+3 ?"
          ENTER 707;Tvolt$
          PRINT TVolt$
```

VBASe? query

This query returns the voltage level of the base of the waveform data. VBASe is determined by using a histogram of the voltage values of the waveform record. After a waveform record is collected the absolute min and max voltages are determined and a histogram of the voltage values is completed. Next, the waveform record is scanned to find the voltage values with the largest number of data points. If the maximum number of data points is greater than the limit criteria (approximately 5% of the maximum number of points in the record) that voltage level is used for the top or the base. If the limit criteria is not satisfied the absolute min, max values are used as the base and the top.

Query Syntax: VBASe?

Returned format: [VBASe]<NR3><crlf>

```
Example:  OUTPUT 707;"VBASE?"
          ENTER 707;Base$
          PRINT Base$
```


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VDELta? query

This query returns the difference in voltage between voltage marker 1 & 2. That is:

VDELta = Marker2 - Marker1

Where Marker1 is the voltage at marker 1 and Marker2 is the voltage at marker 2.

Query Syntax: VDELta?

Returned Format: [VDELta]<NR3><crlf>

```
Example:  OUTPUT 707;"VDELta?"
          ENTER 707;Vdelta$
          PRINT Vdelta$
```

VFIFty command

For a single source this command sets the voltage markers at the 50% level. For dual source measurements Vmarker1 is sent to the 50% level of the first source and Vmarker 2 is set to the 50% level of the second source. For a single source, this command has the same effect as pressing the front panel Auto Top-Base key and then pressing the 50-50% key.

Command Syntax: VFIFty

```
Example:  OUTPUT 707;"VFIFTY"
```

VMAX? query

This query returns the absolute maximum voltage present at the selected source

Query Syntax: VMAX?

Returned Format: [VMAX]<NR3><crlf>

```
Example:  OUTPUT 707;"VMAX?"
          ENTER 707;Vmax$
          PRINT Vmax$
```


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VMIN? query

This query returns the minimum voltage present on the selected source.

Query Syntax: VMIN?

Returned Format: [VMIN]<NR3><crlf>

```
Example:  OUTPUT 707;"VMIN?"
          ENTER 707;Vmin$
          PRINT Vmin$
```

VPP? query

This query returns the peak-to-peak voltage computed using the formula:

Vpp = Vmax - Vmin

Where Vmax and Vmin are the maximum and minimum voltages present on the selected source.

Query Syntax: VPP?

Returned Format: [VPP]<NR3><crlf>

```
Example:  OUTPUT 707;"VPP?"
          ENTER 707;Vpp$
          PRINT Vpp$
```


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VRELative

command/query

The VRELative command moves the voltage markers to defined percentage points of their last established positions. For example: after a TOPBase operation voltage marker 1 would be located at the base (0%) of the signal and voltage marker 2 would be at the top (100%) of the signal. If VRELative 10 command was executed, voltage marker 1 would be moved to the 10% level and voltage marker 2 would be moved to the 90% level the signal. VREL 100 would move the markers back to their original locations. VREL 50 would move both markers to the 50% point of their original positions. The query returns the current relative position of the markers i.e., 10, 20, 50, or 100.

Command Syntax: VRELative<percentage>

```
Example:  OUTPUT 707;"VRELative 20"
```

Query Syntax: VRELative?

```
Returned Format:  [VRELative]<NR1>

Example:  OUTPUT 707;"VREL?"
          ENTER 707;Vr$
          PRINT Vr$
```


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VRMS? query

This query returns the RMS voltage of the selected SOURce. The RMS voltage is computed over one complete period using the formula:

$$V_{rms} = \left[\frac{1}{n} \sum_{j=1}^{j=n} V_j^2 \right]^{\frac{1}{2}}$$

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Where there are n time buckets in 1 period and Vj is the voltage at bucket j of the period data Since it is rare for a period to fall precisely within an integral number of time buckets, the algorithm rounds to the nearest time bucket at the beginning and end and uses these as the limits.

Query Syntax: VRMS?

Returned Format: [VRMS]<NR3><crlf>

Example:
```
OUTPUT 707;"VRMS?"
ENTER 707;V$
PRINT V$
```

VSTArt command/query

This command moves voltage marker 1 to the specified voltage. The query returns the current voltage level of voltage marker 1.

Command Syntax: VSTArt<voltage level>

Example:
```
OUTPUT 707;"VSTART -.01"
```

Query Syntax: VSTArt?

Returned Format: [VSTArt]<NR3><crlf>

Example:
```
OUTPUT 707;"VSTART?"
ENTER 707;Vs$
PRINT Vs$
```


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VSTOp

command/query

This command moves voltage marker 2 to the specified voltage. The query returns the current voltage level of voltage marker 2.

Command Syntax: VSTOp<voltage level>

```
Example:  OUTPUT 707;"VSTOP -.1"
```

Query Syntax: VSTOp?

```
Returned Format:  [VSTOp]<NR3><crlf>

Example:  OUTPUT 707;"VSTOP?"
          ENTER 707;Vstop$
          PRINT Vstop$
```

VTIMe?

query

This query returns the voltage at a time, this time is referenced to the trigger event and must be on screen. The time may be + or - (before or after the trigger event). This command functions on single valued waveform records only. If the time with respect to the trigger event is off screen 1E38 will be returned. If the time bucket of interest does not contain any voltage values, due to the completion criteria being less than 100%, the VTIMe value will be interpolated using linear interpolation between the closest points before and after the time bucket.

Query Syntax: VTIMe?

```
Returned Format:  [VTIMe]<NR3><crlf>

Example:  OUTPUT 707;"VTIME -.001?"
          ENTER 707;Vt$
          PRINT Vt$
```


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VTOP?

query

This command returns the voltage at the top of a waveform. VTOP is calculated by using a histogram of the voltages of the waveform record. After a waveform record is collected the absolute min and max voltages are determined and histogram of the voltage values is completed Next, the waveform is scanned to find the voltage values with the largest number of data points. If the maximum number of data points is greater than the limit criteria (approximately 5%) of the maximum number of data points in the record, that voltage level is used for the top or the base. If the limit criteria is not satisfied the absolute min, max values are used as the base and the top.

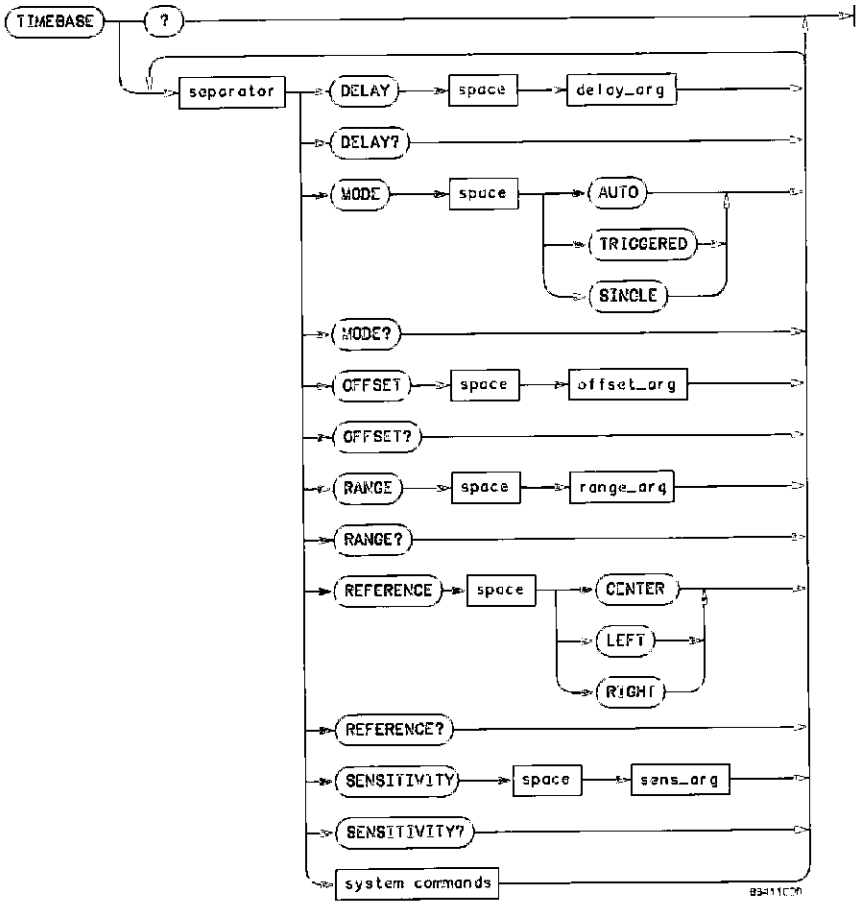
Query Syntax: VTOP?

Returned format: [VTOP]<NR3><crlf>

Example:
```
OUTPUT 707;"VTOP?"
ENTER 707;Vtop$
PRINT Vtop$
```

NOTES:

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RANGE_ARG = A real number with a range of 1 ns to 10 sec.

DELAY_ARG = A real number with the following restrictions:

```
Maximum delay is 60,000 X (timebase range) or 1.6 sec
   whichever is larger.
If the delay reference is left
   then minimum delay is 200 ms or -(timebase range)
   whichever is smaller.
Else if the delay reference is center
   then minimum delay is -5(timebase range) or
   -200 ms+5(timebase range) whichever is smaller.
Else if the delay reference is right
   then minimum delay is 0 or -200 ms+10(timebase range).
```

OFFSET_ARG = Same as DELAY_ARG.

SENS_ARG = A real number between 100 ps and 1 sec.

Figure 10-11. Timebase Subsystem Commands

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10-17. TIMEBASE SUBSYSTEM

The Timebase Subsystem commands control the horizontal axis, "X axis", oscilloscope functions. See Figure 10-11 for a syntax diagram of the timebase subsystem commands.

TIMebase

command/query

The TIMbase command selects the timebase as the destination for the commands that follow. The query responds with all the settings of the timebase.

Command Syntax: TIMebase

```
Example:  OUTPUT 707;"TIMEBASE"
```

Query Syntax: TIMebase?

```
Returned Format:  [TIMebase]<crlf>
                  [MODE]<argument><crlf>
                  [RANGe]<NR3><crlf>
                  [DELay]<NR3><crlf>
                  [REFerence]<NR3><crlf>

Example:  DIM Time$[100]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"TIMEBASE?"
          ENTER 707 USING "-K";Time$
          PRINT USING "K":Time$
```

DELay | DLY

command/query

This command sets the timebase delay. This delay is the time interval between the trigger event and the on screen delay reference point. The query returns the current delay value.

Command Syntax: {[DELay][DLY]}<timebase delay>

```
Example:  OUTPUT 707;"DELAY 2E-3"
```

Query Syntax: {[DELay][DLY]}?

```
Returned Format:  [DELay]<NR3><crlf>

Example:  OUTPUT 707;"DELAY?"
          ENTER 707;Del$
          PRINT Del$
```


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MODE

command/query

This command selects the timebase mode. If the AUTO mode is selected the unit will provide a baseline on the display in the absence of a signal. If a signal is present but is not triggered the display will be unsynchronized but will not be a baseline. If the TRIGGERED mode is selected and no trigger is present the unit will not sweep, and the data acquired on the previous trigger will remain on-screen. The SINGLE mode causes the unit to make a single acquisition when the next trigger event occurs. The query returns the current mode.

Command Syntax: MODE{[AUTO | 0]
[TRIGGERED | 1]
[SINGLE | 2]}

Example: OUTPUT 707;"MODE SINGLE"

Query Syntax: MODE?

Returned Format: [MODE]<argument><crlf>

Example: OUTPUT 707;"MODE?"
ENTER 707;Mode$
PRINT Mode$

OFFSet

command/query

This command sets the timebase delay. This delay is the time interval between the trigger event and the on screen delay reference point. The query returns the current delay value. This command performs exactly the same function as the DELay command.

Command Syntax: OFFSet<timebase delay>

Example: OUTPUT 707;"OFFSET 1E-4"

Query Syntax: OFFSet?

Returned Format: [OFFSet]<NR3><crlf>

Example: OUTPUT 707;"OFFSET?"
ENTER 707;Offs$
PRINT Offs$

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RANGe

command/query

This command defines the full scale horizontal time interval. RANGE = 10 X SENSITIVITY. The query returns the current range.

Command Syntax: RANGe<horizontal time interval>

```
Example:  OUTPUT 707;"RANGE 1"
```

Query Syntax: RANGe?

```
Returned Format:  [RANGe]<NR3><crlf>

Example:  OUTPUT 707;"RANGE?"
          ENTER 707;Range$
          PRINT Range$
```

REFerence

command/query

This command sets the delay reference to the left, center, or right side of the screen. The query returns the current delay reference.

Command Syntax: REFerence {[LEFT | 0]
[CENTER | 1]
[RIGHT | 2]}

```
Example:  OUTPUT 707;"REFERENCE LEFT"
```

Query Syntax: REFerence?

```
Returned Format:  [REFerence]<argument><crlf>

Example:  OUTPUT 707;"REFERENCE?"
          ENTER 707;Ref$
          PRINT Ref$
```


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SENSitivity

command/query

This command sets the horizontal time/division to the defined value.
SENSitivity = RANGe/10. The query returns the current time/division.

Command Syntax: SENSITIVITY<time/division>

Example: OUTPUT 707;"SENSITIVITY 1E-7"

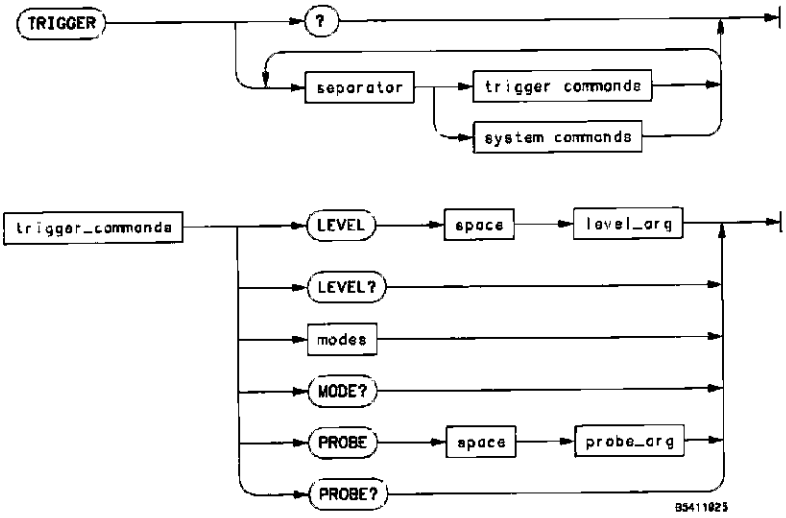
Query Syntax: SENSitivity?

Returned Format: [SENSitivity]<NR3><crlf>

Example:
```
OUTPUT 707;"SENSITIVITY?"
ENTER 707;Sens$
PRINT Sens$
```

NOTES:

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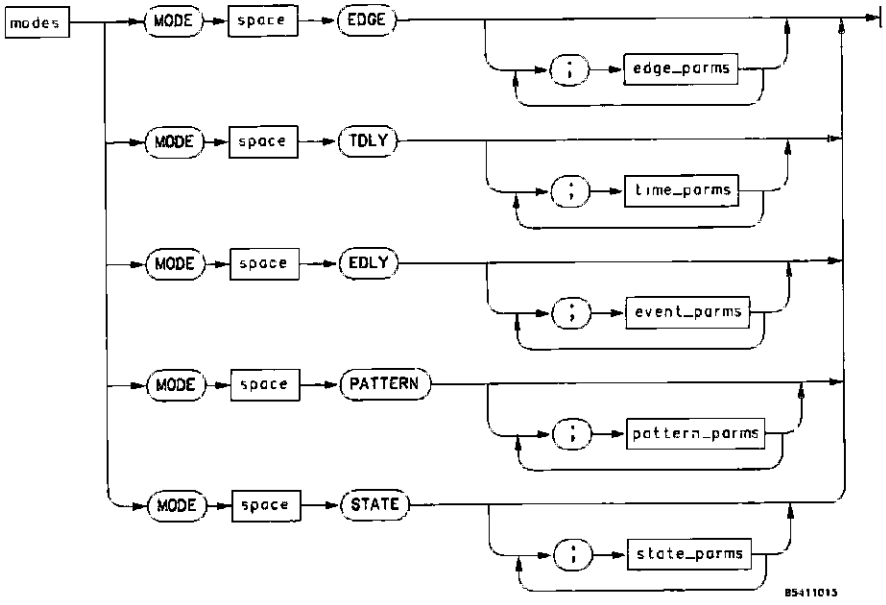
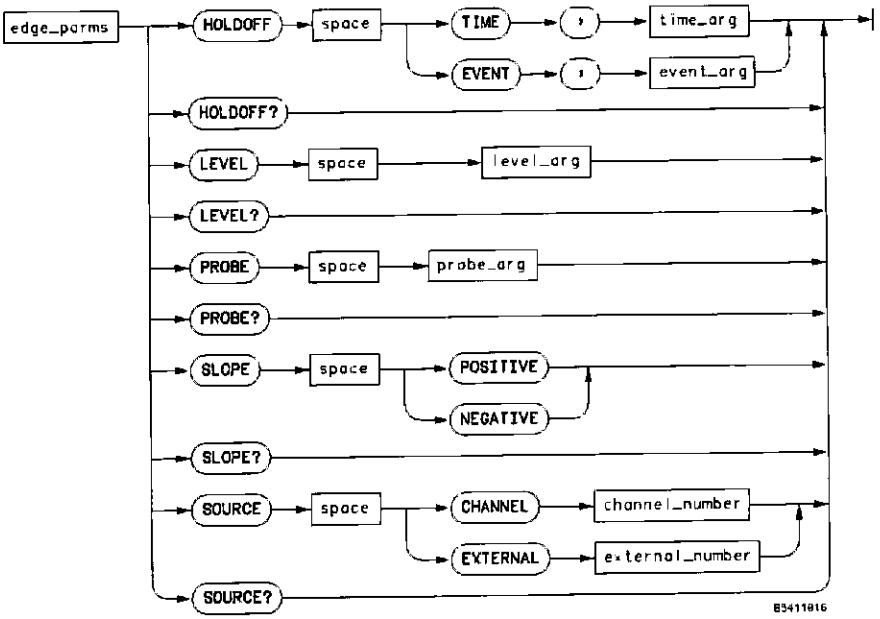


Figure 10-12 Trigger Subsystem Commands

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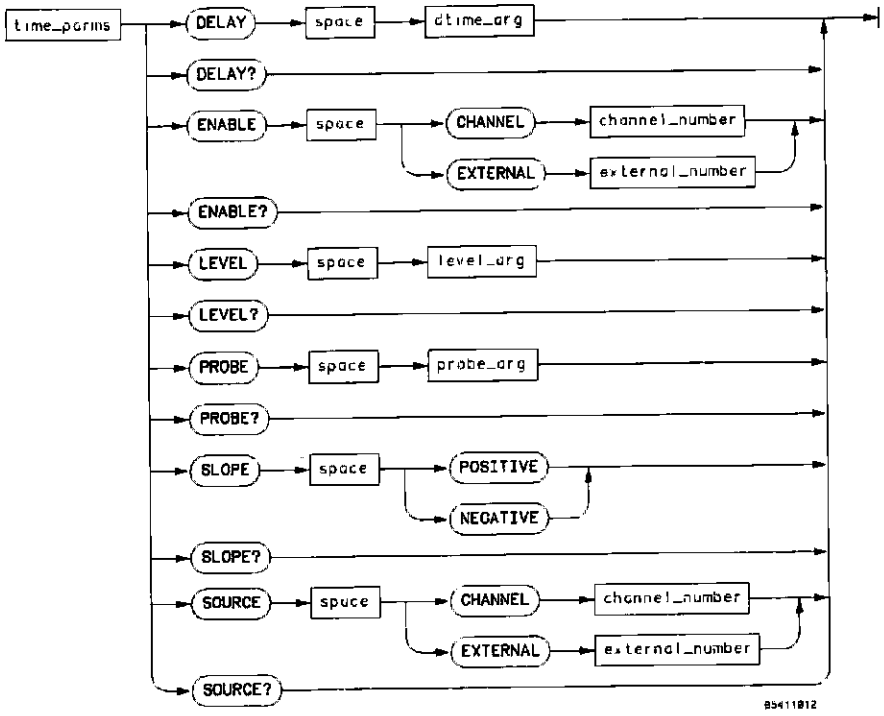


Figure 10-12 Trigger Subsystem Commands

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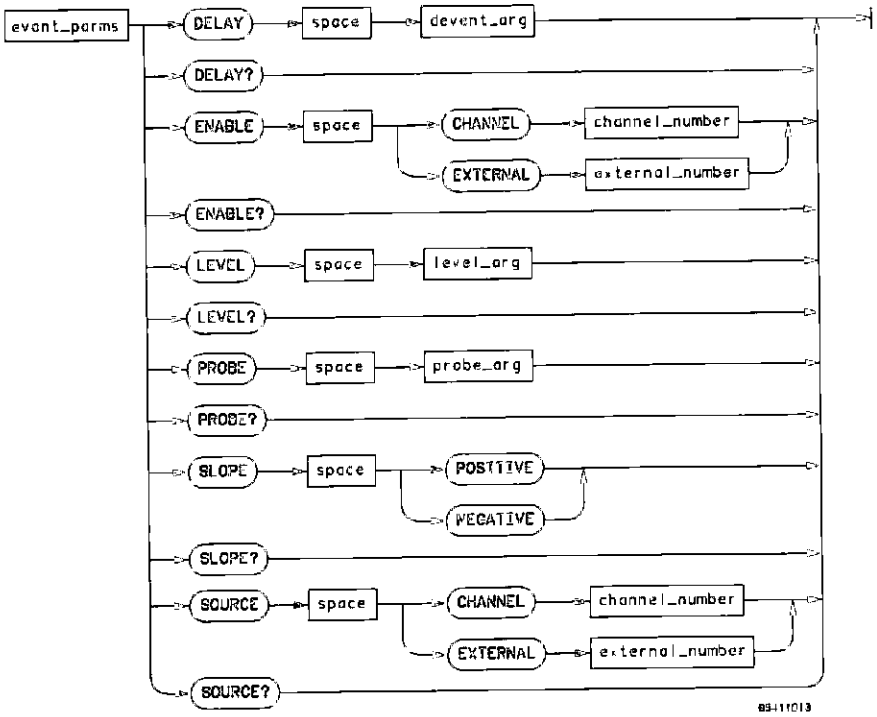


Figure 10-12 Trigger Subsystem Commands

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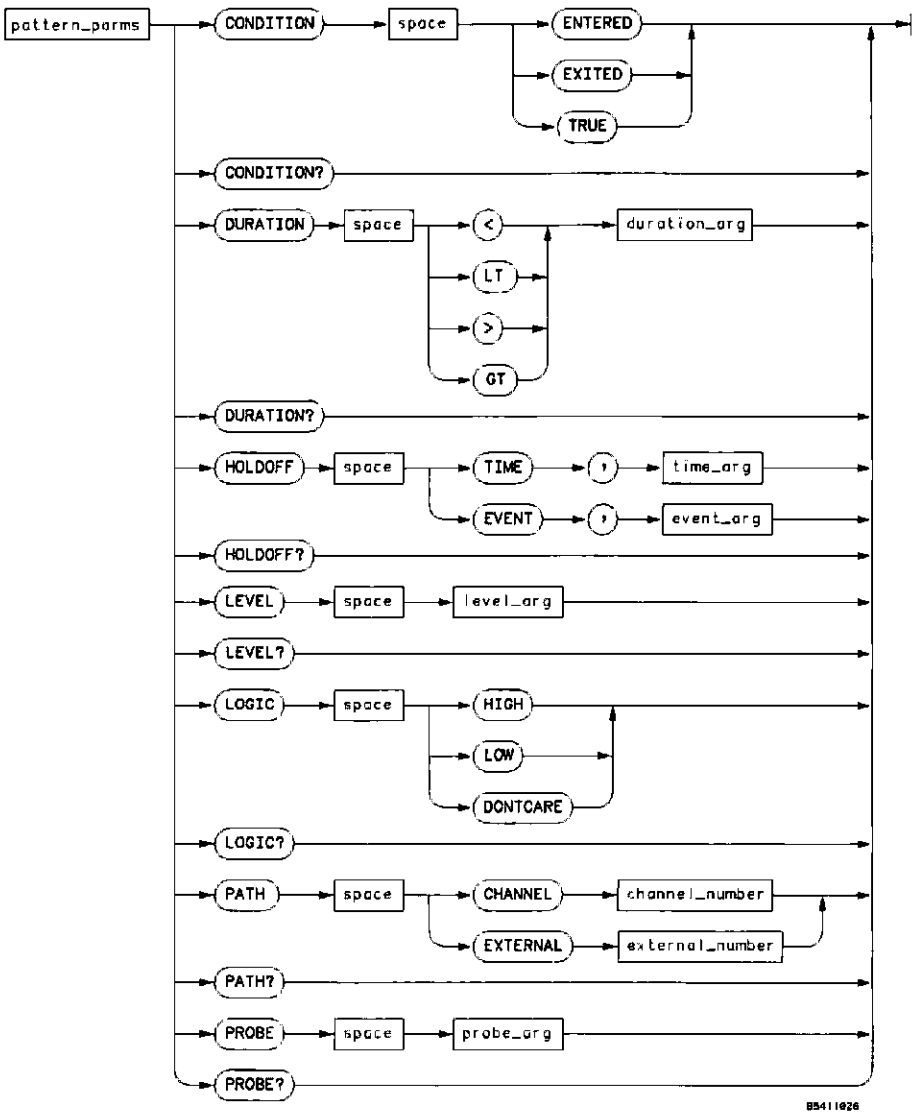


Figure 10-12 Trigger Subsystem Commands

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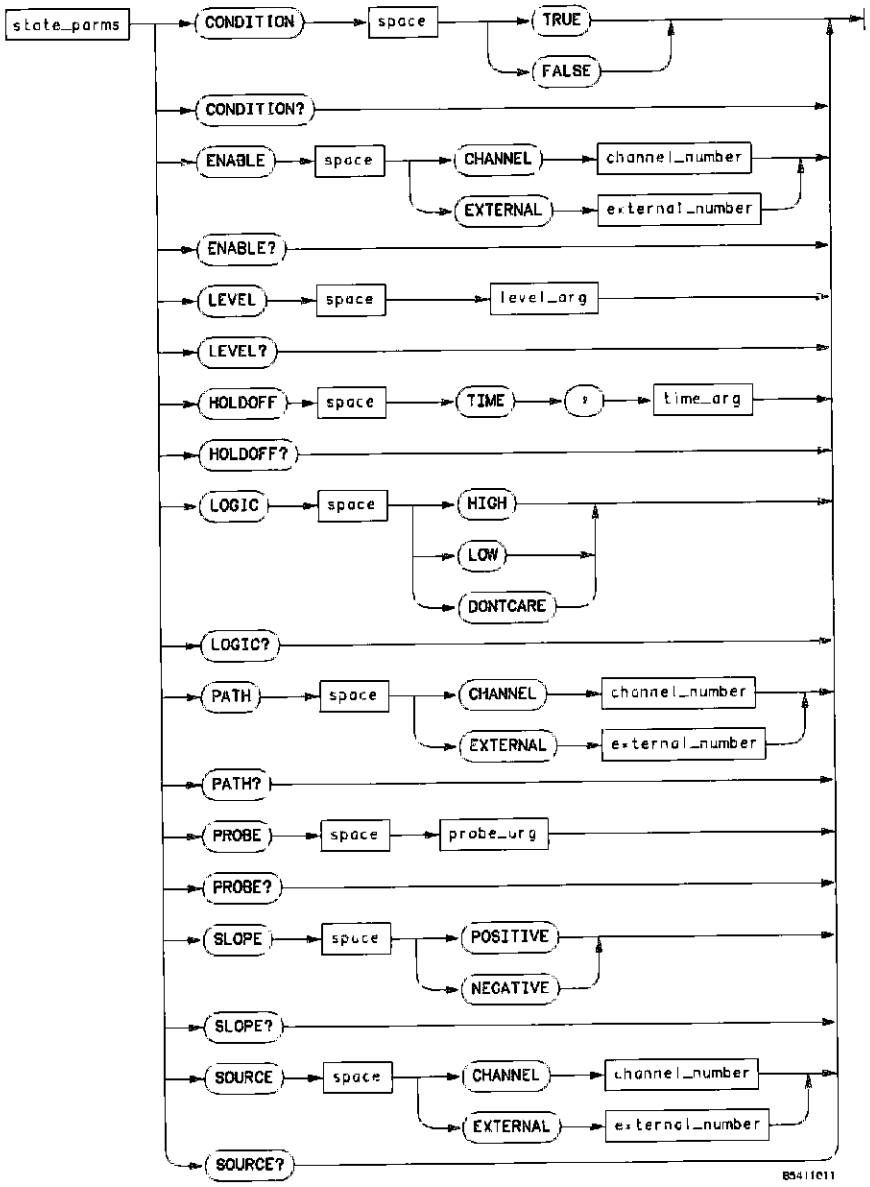


Figure 10-12 Trigger Subsystem Commands

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10-18. TRIGGER SUBSYSTEM

The commands in the Trigger Subsystem are used to define the conditions for a trigger. This instrument provides five trigger modes: EDGE mode, PATTERN mode, EVENT DELAY mode, TIME DELAY mode, and the STATE mode.

In the edge mode each trigger source has an associated level, slope, and probe attenuation factor which are used when it is selected as a trigger source. These levels and probe attenuation factors are applicable to other modes however, the slope will depend on the particular mode used.

The SOURCE, ENABLE and PATH commands are related in that they select the source for commands like LOGIC or LEVEL, however each is used in a slightly different way. The SOURCE command is used to specify the trigger source for the EDGE, STATE, TDLY, and EDLY modes. This is the source that the actual trigger is generated from. The ENABLE command is used in the TDLY and EDLY modes to specify the source that is used to qualify the trigger. The PATH command is used in the PATTERN and STATE modes to select a pattern element for setup.

Each individual trigger mode keeps track of the last referenced source and it is this source that is addressed by any SLOPE, LOGIC, etc. commands when that mode is re-entered.

See Figure 10-12 for Trigger Subsystem syntax diagram.

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TRIGger

command/query

The trigger command selects the trigger subsystem as the destination for the trigger commands that follow. The query responds with the subsystem parameters for the current trigger mode.

Command Syntax: TRIGger

Example: OUTPUT 707;"TRIGGER"

Query Syntax: TRIGger?

Returned Format:

```
MODE EDGE<crlf>
SOURce<path name><crlf>
PROBe<NR1><crlf>
LEVel<NR3><crlf>
SLOPe<argument><crlf>
{[HOLDoff TIME]<NR3><crlf> |
 [HOLDoff EVENTS]<NR1><crlf>}

MODE PATTERN<crlf>
CONDition<argument><crlf>
DURation<argument><crlf>
PATH<path name 1><crlf>
PROBe<NR3><crlf>
LEVel<NR3><crlf>
LOGic<argument><crlf>
PATH<path name 2><crlf>
PROBe<NR3><crlf>
LEVel<NR3><crlf>
LOGic<argument><crlf>
PATH<path name 3><crlf>
PROBe<NR3><crlf>
LEVel<NR3><crlf>
LOGic<argument><crlf>
PATH<path name 4><crlf>
PROBe<NR3><crlf>
LEVel<NR3><crlf>
LOGic<argument><crlf>
{[HOLDoff TIME]<NR3><crlf> |
 [HOLDoff EVENTS]<NR1><crlf>}
```

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TRIGger (cont'd)

```
                    MODE STATE<crlf>
                    CONDition<argument><crlf>
                    PATH<path name 1><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    LOGic<argument><crlf>
                    PATH<path name 2><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    LOGic<argument><crlf>
                    PATH<path name 3><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    LOGic<argument><crlf>
                    SOURce<path name 4><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    SLOPe<argument><crlf>
                    HOLDoff TIME<NR3><crlf>

                    MODE TDLY<crlf>
                    ENABle<path name 1><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    SLOPe<argument><crlf>
                    DELay<NR3><crlf>
                    SOURCE<path name 2><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    SLOPe<argument><crlf>

                    MODE EDLY<crlf>
                    ENABle<path name 1><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    SLOPe<argument><crlf>
                    DELay<NR1><crlf>
                    SOURCE<path name 2><crlf>
                    PROBe<NR3><crlf>
                    LEVel<NR3><crlf>
                    SLOPe<argument><crlf>
```

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TRIGger (cont'd)

```
Example:  DIM Trig$[700]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"TRIGGER?"
          ENTER USING "-K";Trig$
          PRINT USING "K";TRIG$
```

CONDition

command/query

This command/query is valid only when the trigger mode is PATTERN or STATE. In the PATTERN mode it specifies whether the trigger is generated on entry to the specified logic pattern or when exiting it. If TRUE is selected, duration is used as the qualifier for the PATTERN. In the STATE mode it specifies whether the trigger is generated when the pattern is present (true) or not present (false). The query returns the currently selected condition.

Command Syntax: CONDition

```
Example:  OUTPUT 707;"CONDITION EXIT"
```

Query Syntax: CONDition?

```
Returned Format:  [CONDition]{[ ENTER | 0 ]   (PATTERN mode)
                             [ EXIT  | 1 ]
                             [ TRUE  | 2 ]}

                  [CONDition]{[ FALSE | 0 ]   (STATE mode)
                             [ TRUE  | 1 ]}


Example:  OUTPUT 707;"CONDITION?"
          ENTER 707;Cond$
          PRINT Cond$
```


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DELay | DLY

command/query

This command/query is valid only in the events delay (EDLY) or time delay (TDLY) modes. In the time delay mode this command specifies the delay in seconds. In the events delay mode this command specifies the number of trigger events. The query returns the delay for the current mode.

Command Syntax: {DELay | DLY}{<event delay>|<time delay>}

Example: OUTPUT 707;"DELAY 10"

Query Syntax: DELay | DLY?

Returned Format: [DELay]{<NR1>|<NR3>}<crlf>

```
Example:  OUTPUT 707;"DELAY?"
          ENTER 707;Delay$
          PRINT Delay$
```

DURation

command/query

This command/query is valid only in the pattern mode. It specifies the time limit (minimum time for ">", or maximum time for "<") a pattern must be present to generate a trigger. Pattern duration trigger is implicitly an "EXITED" condition, that is, the trigger coincides with the first event that makes the pattern false. The query returns the current selections for duration type and time

```
Command Syntax:  DURation{[ LT | 1 | < ]
                          [ GT | 2 | > ]}

     Example:  OUTPUT 707;"DURATION LT 1E-3"

Query Syntax:  DURation?

     Returned Format:  [DURation]<argument><crlf>

     Example:  OUTPUT 707;"DURATION?"
               ENTER 707;Dur$
               PRINT Dur$
```


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ENABle

command/query

This command/query is valid in the STATE, TDLY, or EDLY modes. It is used to specify the source that is to be used as the trigger enable, which is also the source for subsequent SLOPE and PROBE commands. The query returns the current trigger enable source of the present mode.

Command Syntax: ENABle{[CHANnel1 | 1]
[CHANnel2 | 2]
[EXTernal1 | 3]
[EXTernal2 | 4]}

```
Example:  OUTPUT 707;"ENABLE CHANNEL3"
```

Query Syntax: ENABle?

```
Returned Format:  [ENABle]<argument><crlf>

Example:  OUTPUT 707;"ENABLE?"
          ENTER 707;Enable$
          PRINT Enable$
```

HOLDoff

command/query

This command allows you to specify the holdoff time in the EDGE, PATTERN, or the STATE modes, or the holdoff number of events in the EDGE or PATTERN modes. Each mode has its own holdoff parameters and "remembers" whether it was using holdoff by time or holdoff by events. The holdoff query is valid in the EDGE, PATTERN, or STATE modes and returns the current holdoff setting for the presently selected mode. Time holdoff ranges from 70 ns to 670 ms. Events holdoff ranges from 2 to 67,000,000 events.

Command Syntax: HOLDoff {[EVENT<# of events>]
[TIME<holdoff time>]}

```
Example:  OUTPUT 707;"HOLDOFF EVENT 100"
```

Query Syntax: HOLDoff?

```
Returned Format:  [HOLDoff]<current holdoff mode>
                           <holdoff value><crlf

Example:  DIM Hold$[40]
          OUTPUT 707;"HOLDOFF?"
          ENTER 707;Hold$
          PRINT Hold$
```


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LEVel | LVL

command/query

This command sets the trigger level of the selected SOURCE or PATH. The query returns the trigger level of the selected SOURCE or PATH.

Command Syntax: {[LEVel | LVL]} <trigger level>

```
Example:  OUTPUT 707;"LEVEL .1"
```

Query Syntax: {[LEVel | LVL]}?

```
Returned Format:  [LEVel]<NR3><crlf>

Example:  OUTPUT 707;"LEVEL?"
          ENTER 707;Level$
          PRINT Level$
```

LOGic

command/query

This command/query is valid in the STATE and PATTERN modes. The LOGic command is used to specify the relation between the signal and the predefined voltage level that must exist before that part of the pattern is considered valid. If the signal on a selected source or path is greater than the trigger level that signal is considered HIGH. If it less than the trigger level it is considered LOW. The query returns the last specified logic level of the currently enabled source.

Command Syntax:

```
LOGic{[ LOW | 0 ]
      [ HIGH | 1 ]
      [ DONTCARE | 2 ]}

Example:  OUTPUT 707;"LOGIC DONTCARE"
```

Query Syntax:

```
LOGic?

Returned Format:  [LOGic]<argument><crlf>

Example:  DIM Log$[40]
          OUTPUT 707;"LOGIC?"
          ENTER 707;Log$
          PRINT Log$
```


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MODE

command/query

This command allows you to select the trigger mode. The query returns the current trigger mode.

Command Syntax: MODE{[EDGE | 0]
[PATTERN | 1]
[STATE | 2]
[TDLY | 3]
[EDLY | 4]}

Example: OUTPUT 707;"MODE EDGE"

Query Syntax: MODE?

Returned Format: [MODE]<argument><crlf>

Example: OUTPUT 707;"MODE?"
ENTER YOU;Mode$
PRINT Mode$

PATH

command/query

This command/query is valid in the PATTERN and STATE modes. This command allows you select a pattern bit as the source for future probe and logic commands. The query returns the current trigger source of the present mode.

Command Syntax: PATH {[CHANNEL1 | CHAN1 | 1]
[CHANNEL2 | CHAN2 | 2]
[EXTERNAL1 | EXT1 | 3]
[EXTERNAL2 | EXT2 | 4]}

Example: OUTPUT 707;"PATH CHANNEL3"

Query Syntax: PATH?

Returned Format: [PATH]<argument><crlf>

Example: DIM Path$[30]
OUTPUT 707;"PATH?"
ENTER 707;Path$
PRINT Path$

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PROBe

command/query

This command specifies the attenuation factor for the last specified SOURCE or PATH for the current trigger mode. If the trigger source is also a channel, the last specified probe attenuation for that channel is the one used. See the CHANNEL PROBE command in Paragraph 10-10. The query returns the current source's probe attenuation factor.

Command Syntax: PROBe<attenuation ratio>

```
Example:  OUTPUT 707;"PROBE 10"
```

Query Syntax: PROBe?

```
Returned Format:  [PROBe]<NR3><crlf>

Example:  DIM Probe$[30]
          OUTPUT 707;"PROBE?"
          ENTER 707;Probe$
          PRINT Probe$
```

SLOPe

command/query

This command allows you to specify the trigger slope for the previously specified source. The query returns the current slope for the last selected source of the current mode

Command Syntax: SLOPe {[NEGATIVE | 0]
[POSITIVE | 1]}

```
Example:  OUTPUT 707;"SLOPE POSITIVE"
```

Query Syntax: OUTPUT 707;"SLOPE?"

```
Returned Format:  [SLOPe]<argument><crlf>

Example:  OUTPUT 707;"SLOPE?"
          ENTER 707;Slope$
          PRINT Slope$
```


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SOURce | SRC

command/query

This command /query is valid in the EDGE, STATE, TDLY or EDLY modes and is used to specify the trigger source. This command also identifies the source for any subsequent SLOPe and PROBe commands. The query returns the current trigger source of the present mode.

```
Command Syntax:  {[SOURce | SRC]} {[ CHANnel1 | 1 ]
                                  [ CHANnel2 | 2 ]
                                  [ EXTernal1 | 3 ]
                                  [ EXTernal2 | 4 ]}

     Example:  OUTPUT 707;"SOURCE CHANNEL1"

Query Syntax:  {[SOURce | SRC]}?

     Returned Format:  [SOURce]<argument><crlf>

     Example:  DIM Src$[30]
               OUTPUT 707;"SOURCE?"
               ENTER 707;Src$
               PRINT Src$
```

NOTES:

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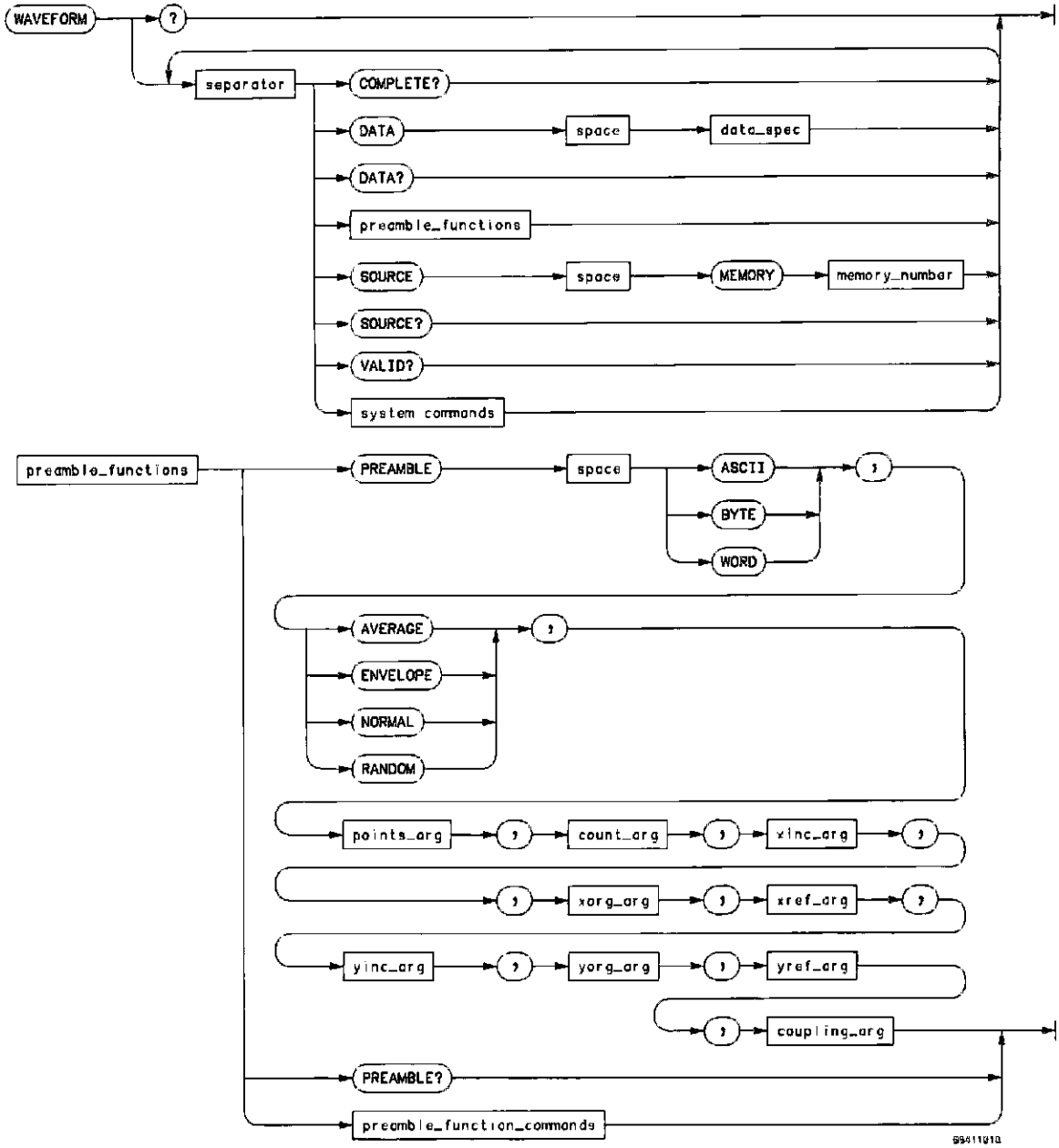


Figure 10-13. Waveform Subsystem Commands

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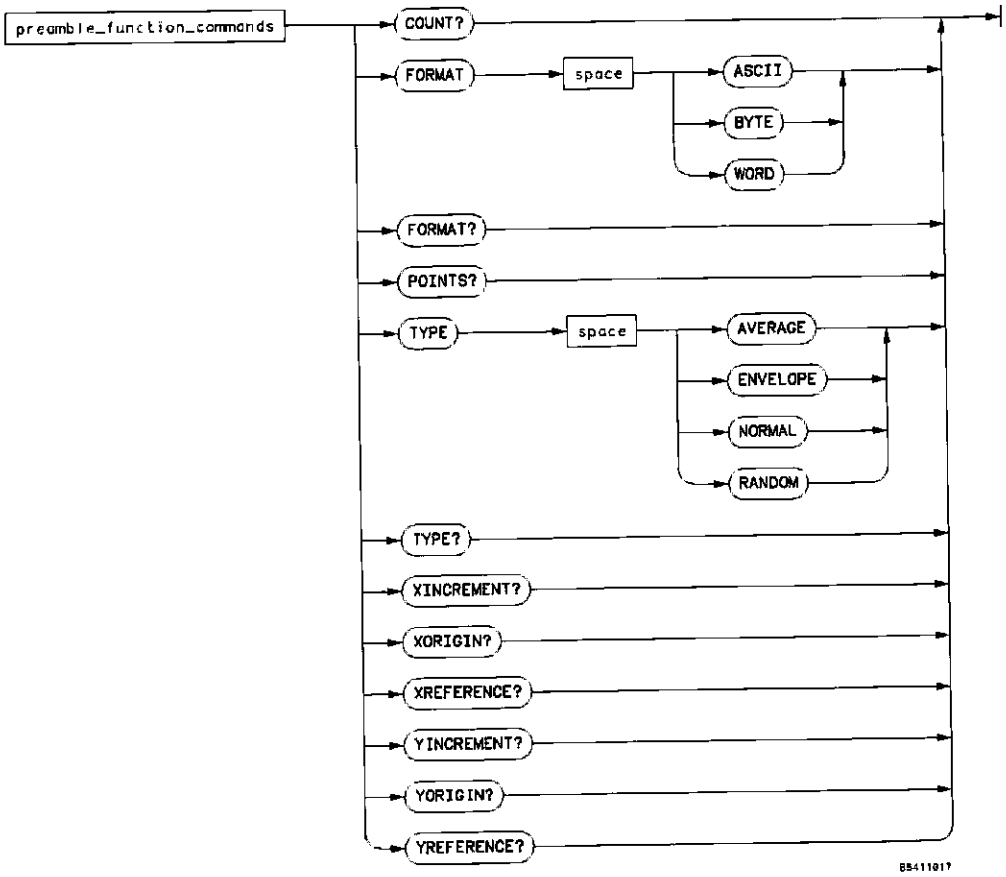


Figure 10-13. Waveform Subsystem Commands

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MEMORY_NUMBER = An integer 1 through 4.

DATA_SPEC = A block of data in #A format as defined in IEEE Std. 728-1982

POINTS_ARG = An integer = 128, 256, 500, 512, 1024.

COUNT_ARG = An integer from 1 to 2048.

XINC_ARG = A real number from 10 ps to 2 ms.

XORG_ARG = A real number with the following restrictions:
The maximum value is 60,000 X timebase range or 1.6 sec, which ever is greater.
If the delay reference is left then the minimum value is -200 ms or -(timebase range) whichever is smaller
Else if the delay reference is center
then the minimum value is the lesser of -5X(timebase range) and -200 ms + (10 X timebase range).
Else if the delay reference is right
then the minimum value is the lesser of 0 and -200 ms+(10Xtimebase range).

XREF_ARG = 0

YINC_ARG = A real number equal to 1/128 X voltage range.

YORG_ARG = A real number with a magnitude less than 1.5 X voltage range.

YREF_ARG = 64 for byte format, 16384 for word or ASCII format.

COUPLING = DCFIFTY or the integer 3.

Figure 10-13. Waveform Subsystem Commands

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10-19. WAVEFORM SUBSYSTEM

The waveform subsystem commands are used to transfer waveforms to and from the four waveform memories. Waveform data consists of a preamble and a data record. The preamble contains scaling information useful for interpreting the data record while the data record contains the actual waveform data values.

Each element of the waveform preamble can be individually set or queried. This can cause you problems if not done judiciously, for example, setting POINTS in the preamble to a value different from the actual number of points in the waveform could result in inaccurate data being sent. For this reason only the query form of most of the preamble commands is documented here.

The actual values set in the preamble are determined when the DIGITIZE command is executed and are based on the settings of variables in the ACQUIRE subsystem. For more information on the DIGITIZE process and the ACQUIRE subsystem variables, see Section 10-8. For Syntax diagrams of the waveform subsystem commands see Figure 10-13.

The four waveform types are:

NORMAL:

Normal data consists of the last data point (hit) in each time bucket. This data is transmitted over HP-IB in a linear fashion starting with time bucket 0 and going through time bucket n, where n is the number returned by the WAVeform POINts query. Time buckets that don't have data in them return -1. Only the voltage values of each data point transmitted, the time values correspond to the position in the data array. The first voltage value corresponds to the first time bucket on the left of the CRT and the last value corresponds to the next to last time bucket on the right side of the CRT.

AVERAGE:

Average data consists of the average of the first n hits in a time bucket, where n is the value returned by WAVeform COUNt query. Time buckets that have fewer than n hits return the average of what data they do have. Again, if a time bucket doesn't have any data in it, it will return -1. This data is transmitted over the HP-IB in a linear fashion starting with time bucket 0 and proceeding through time bucket n-1, where n is the number returned by the WAVeform POINts query. The first value corresponds to a point at the left side of the screen and the last value is one point away from the right side of the screen.

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ENVELOPE:

Envelope data consists of two arrays of data, one containing the minimum of the first n hits in each time bucket and the other consisting of the maximum of the first n hits in each time bucket, where n is the value returned by the count query. If a time bucket does not have any hits in it then -1 is returned for both the minimum and maximum values. The two arrays are transmitted one at a time over the HP-IB linearly, starting with time bucket 0 (on the left side of the CRT) and proceeding through time bucket m-1, where m is the value returned by the WAVeform POINts query. The array with the minimum values is sent first. The first value of each array corresponds to the data point on the left side of the CRT The last value is one data point away from the right side of the CRT.

When envelope data is acquired, the minimum and maximum data for channel 1 is stored in memories 1 and 3 respectively and the minimum and maximum data for channel 2 is stored in memories 2 and 4. Memories 1 and 2 are set to the envelope type and memories 3 and 4 are set to the normal type.

The data in the memories is transferred to a controller using the data query. The memory source for the transfer is specified by the waveform source command. When memory 1 is specified as the source, the minimum and maximum data from memories 1 and 3 is transferred over HP-IB, and when memory 3 is specified as the source, only the maximum data in memory 3 is transferred over HP-IB Similarly, when memory 2 is specified as the source, the data from memories 2 and 4 is transferred over HP-IB, and when memory 4 is specified as the source only the maximum data in memory 4 is transferred over the bus.

If it is desirable to transfer only the data in memory 1 or 2, it can be accomplished by changing the memory 1 or memory 2 type from envelope to normal using the waveform type command.

Data is transferred into the instrument from a controller using the waveform data command. Envelope data can be transferred into memory 1 or memory 2 by specifying the type for the memories as envelope. The data is then transferred as two arrays. If memory 1 is specified as the source, the first array is transferred into memory 1 and the second array is transferred into memory 3. Similarly, if memory 2 is specified as the source, the first array is transferred into memory 2 and the second array is transferred into memory 4.

RANDOM:

Random data consists of all the data that can be gathered, but not to exceed 1024 points. This data is transmitted over the HP-IB in ordered time-voltage pairs. You should not use the BYTE format for this mode since the time bucket numbers range up to 500 and it is impossible to represent numbers this large in a byte without loss of precision. The time data is acquired using 500 time buckets. If ASCII and WORD format are used these time values are multiplied by 64 allowing values from 0 to 32,000. If BYTE format is used the allowed values are from 0 to 125, this demonstrates how precision is lost in the BYTE mode.

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The three FORMATS that are used to transmit data over the HP-IB:

WORD:

Word formatted waveform records are transmitted using the binary block format (the #A format specified in IEEE STD. 728-1982). The character string "#A" is sent first, then followed by a two byte length value (16 bit binary) specifying the number of bytes to follow. The number of bytes is twice the number of words. The number of words is also the value returned by the WAVeform POINts query. This is followed by a sequence of bytes representing the data words, with the most significant byte of each word being transmitted first. The A/D conversion in the 54110D yields a 7 bit result and is contained in the upper half of the data words transmitted by the instrument The lower byte contains zeros unless the TYPE was average. In this case any increased resolution achieved through averaging will show up in the lower byte of the data. Values are always positive and between 0 and 32,767.

BYTE:

The BYTE formatted waveform records are transmitted over the HP-IB using the binary block format (the #A format specified in IEEE Std. 728-1982). The character string "#A" is sent first, then followed by a two byte length value (16 bit binary) specifying the number of bytes to follow. The number of bytes when the FORMat is BYTE is the same as the value returned by the WAVeform POINts query. BYTE formatted transfers run approximately twice as fast as WORD and ASCII transfers, but should be used with caution if there are any data values to be sent that are larger than decimal 127. If the data values have a larger range than 127 as is the case when TYPE is RANDOM,the values are shifted until they fit within a byte. For example, when TYPE is RANDOM, the X values normally range from 0 to 500. Trying to transmit RANDOM data in BYTE FORMAT results in the time bucket numbers being rescaled so that they range from 0 to 125. This lumps time buckets 0 through 3 into one x coordinate, time buckets 4 through 7 into the next X coordinate, etc.

ASCII:

ASCII formatted waveform records are transmitted one value at a time, separated by <cr><lf>s The data values transmitted are the same as would be sent in the WORD FORMAT except that they are converted to an integer ASCII format (six characters) before being sent over HP-IB

The data values can be converted to voltage and time values using the following formulas:

Voltage(j) = [(Yvalue(j) - Yreference)*Yincrement] + Yorigin

Time(j) = (j*Xincrement)+Xorigin (non-RANDOM type)

Time(j) = (Xvalue(j)*Xincrement) + Xorigin (RANDOM type)

Where Yvalue(j) is the value of the jth point and Yreference, Y increment, Yorigin, Xincrement, and Xorigin are the preamble values. In the RANDOM mode Xvalue(j) is the jth time point.

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WAVeform

command/query

The WAVeform command selects the waveform subsystem as the destination for the waveform commands that follow. The query returns the waveform subsystem parameters. The COUPLing parameter is always DC or 1 depending on whether argument is set to alpha or numeric.

Command Syntax: WAVeform

```
Example:  OUTPUT 707;"WAVEFORM"
```

Query Syntax: WAVeform?

```
Returned Format:  [WAVeform]<crlf>
                  [SOURce]<specified source><crlf>
                  [VALid]<NR1><crlf>
                  [FORMat]<argument><crlf>
                  [TYPE]<argument><crlf>
                  [POINts]<NR1><crlf>
                  [COUNt]<NR1><crlf>
                  [XINCrement]<NR3><crlf>
                  [XORigin]<NR3><crlf>
                  [XREFerence]<NR1><crlf>
                  [YINCrement]<NR3><crlf>
                  [YORigin]<NR3><crlf>
                  [YREFerence]<NR1><crlf>
                  [COUPling]<argument><crlf>
                  [COMPlete]<NR1><crlf>

Example:  DIM Wav$[300]
          OUTPUT 707;"EOI ON"
          OUTPUT 707;"WAVEFORM?"
          ENTER 707 USING "-K";Wav$
          PRINT USING "K";Wav$
```

COMPlete

query

This query returns the completion criterion that was used for the last acquisition to the currently selected memory from its preamble.

Query Syntax: COMPlete?

```
Returned Format:  [COMPlete]<NR1><crlf>

Example:  DIM Comp$[30]
          OUTPUT 707;"COMPLETE?"
          ENTER 707;Comp$
          PRINT Comp$
```


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COUNt? | CNT?

query

This query returns the count field of the waveform preamble. The count field contains the number of averages if the TYPE is AVERAGED, or if the TYPE is ENVELOPE it contains the number of hits in each time bucket.

Query Syntax: {[COUNt | CNT]}?

Returned Format: [COUNt]<NR1>

```
Example:  OUTPUT 707;"COUNT?"
          ENTER 707;Count$
          PRINT Count$
```

DATA

command/query

This command causes the instrument to accept a waveform data record over the HP-IB from the controller and store it in the previously specified waveform memory. Note: The record format must match the format previously specified for the memory by it's preamble. The query returns the waveform record stored in the previously specified waveform memory.

Command Syntax: DATA

```
Example:  OUTPUT 707;"DATA"
```

Query Syntax: DATA?

```
Returned format:  [DATA]#A<binary block length in bytes>
                          <binary block><crlf>
```

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DATA (cont'd)

The following program moves data from the 54110D to the controller and then back to the 54110D using the WAVEFORM DATA command and query. For this example program use the instrument's cal signal and connect it to channel 1.

```
10   CLEAR 707
20   OUTPUT 707;"RESET"
30   OUTPUT 707;"AUTOSCALE"
40   ASSIGN @Fast TO 707;FORMAT OFF
50   OUTPUT 707;"ACQUIRE"
60   OUTPUT 707;"TYPE ENVELOPE COUNT 256 COMPLETE 90"
70   OUTPUT 707;"DIGITIZE 1"
80   OUTPUT 707;"HEADER OFF"
90   OUTPUT 707;"WAVEFORM SOURCE MEMORY1 FORMAT WORD"
100  OUTPUT 707;"DATA?"
110  ENTER 707 USING "#,2A"Header$
120  ENTER 707 USING "#,W";Byte_len
130  Word_len=Byte_len/2
140  ALLOCATE INTEGER waveform(1:Word_len)
150  ENTER @Fast;Waveform(*)
160  DIM Preamble$[120]
170  OUTPUT 707;"LONGFORM OFF"
180  OUTPUT 707;"PREAMBLE";Preamble$
190  ENTER 707;Preamble$
200  OUTPUT 707;"PREAMBLE";Preamble$
210  Header$="DATA #A"
220  OUTPUT 707 USING "#,7A,W";Header$;Byte_len
230  OUTPUT @Fast;Waveform(*)
240  OUTPUT 707;"TRANSFER MEMORY2,PLANE2"
250  OUTPUT 707;"VIEW PLANE2 BLANK CHANNEL1"
260  END
```


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FORMat

command/query

This command allows you to set the data transmission mode for the waveform data points. When the ASCII mode is selected the data is sent as ASCII digits with each data value separated by a <crlf>. If the BYTE mode is selected the data is sent as eight bit integers, while a WORD formatted transfer transfers the data as 16 bit integers. The query returns the current transfer format for the previously specified memory.

Command Format; FORMat {[ASCII | 0]
[BYTE | 1]
[WORD | 2]}

Example: OUTPUT 707;"FORMAT WORD"

Query Syntax: FORMat?

Returned Format: [FORMat]<argument><crlf>

Example: OUTPUT 707;"FORMAT?"
ENTER 707;Format$
PRINT Format$

POINts? | PNTS?

query

This query returns the points value in the currently selected waveform preamble, which is the number of points acquired in the last DIGitize command to the selected waveform memory.

Query Syntax: {[POINts | PNTS]}?

Returned Format: [POINts]<NR1><crlf>

Example: OUTPUT 707;"POINTS?"
ENTER 707;Points$
PRINT Points$

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PREamble

command/query

This command sends a waveform preamble to the selected waveform memory in the instrument. The query returns the previously specified memory.

Command Syntax: PREamble <preamble block>

```
<preamble block> ::= <format>,
                     <type>,
                     <points>,
                     <count>,
                     <xincrement>,
                     <xorigin>,
                     <xreference>,
                     <yincrement>,
                     <yorigin>,
                     <yreference>,
                     <coupling>
```

Query Syntax: PREamble?

```
Returned Format:  [PREamble]<format parameter>,
                            <type parameter>,
                            <points NR1>,
                            <count NR1>,
                            <xincrement NR3>,
                            <xorigin NR3>,
                            <xreference NR1>,
                            <yincrement NR3>,
                            <yorigin NR3>,
                            <yreference NR1>,
                            <coupling parameter>
```

Example: This example program uses both the command and query form of the key word.

```
10  DIM Points$[120]
20  OUTPUT 707;"HEADER OFF"
30  OUTPUT 707;"WAVEFORM"
40  OUTPUT 707;"PREAMBLE?"
50  ENTER 707;Points$
60  PRINT Points$
70  OUTPUT 707 USING "#,K";"PREAMBLE",Points$
```


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SOURce | SRC

command/query

This command selects the memory that is to be used as the source in following waveform commands. The query returns the currently selected source.

Command Syntax: {[SOURce | SRC]} {[MEMory1 | 1]
[MEMory2 | 2]
[MEMory3 | 3]
[MEMory4 | 4]}

Example: OUTPUT 707;"SOURCE MEMORY3"

Query Syntax: SOURce?

Returned format: [SOURce]<argument><crlf>

Example: OUTPUT 707;"SOURCE?"
ENTER 707;Src$
PRINT Src$

TYPE

command/query

This command sets the data type for the currently selected memory. The query returns the data type for the previously specified memory.

Command Syntax: TYPE {[INVALID | 0] (query response only)
[NORMal | 1]
[AVErage | 2]
[ENVelope | 3]
[RANDom | 4]}

Example: OUTPUT 707;"TYPE ENVELOPE"

Query Syntax: TYPE?

Returned Format: [TYPE]<argument><crlf>

Example: OUTPUT 707;"TYPE?"
ENTER 707;Type$
PRINT Type$

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VALid?

query

This query returns 0 if there is not data in the memory. If there is valid data in the previously selected memory the response will be 1.

Query Syntax: VALid?

Returned format: [VALid] {[0 | 1]}

```
Example:  OUTPUT 707;"VALID?"
          ENTER 707;Va$
          PRINT Va$
```

XINCrement?

query

This query returns the x-increment value currently in the preamble. This value is the time difference between consecutive data points for NORMAL, AVERAGED, or ENVELOPE data.

Query Syntax: XINCrement?

Returned Format: [XINCrement]<NR3><crlf>

```
Example:  DIM Xin$[30]
          OUTPUT 707;"XINCREMENT?"
          ENTER 707;Xin$
          PRINT Xin$
```

XORigin?

query

The query returns the x-origin value currently in the preamble. This value is the time of the first data point in the memory with respect to the trigger point.

Query Syntax: XORigin?

Returned Format: [XORigin]<NR3><crlf>

```
Example:  DIM Xor$[30]
          OUTPUT 707;"XORIGIN?"
          ENTER 707;Xor$
          PRINT Xor$
```


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XREFerence? query

This query returns the current x-reference value in the preamble. This value specifies the data point that is associated with the x-origin data values.

Query Syntax: XREFerence?

Returned Format: [XREFerence]<NR1><crlf>

Example:
```
DIM Xr$[30]
OUTPUT 707;"XREFERENCE?"
ENTER 707;Xr$
PRINT Xr$
```

YINCrement? query

This query returns the y-increment value currently in the preamble. This value is the voltage difference between consecutive data points.

Query Syntax: YINCrement?

Returned Format: [YINCrement]<NR3><crlf>

Example:
```
DIM Yin$[30]
OUTPUT 707;"YINCREMENT?"
ENTER 707;Yin$
PRINT Yin$
```

YORigin? query

This query returns the y-origin currently in the preamble. This value is the voltage at center screen.

Query Syntax: YORigin?

Returned Format: [YORigin]<NR3><crlf>

Example:
```
DIM Yor$[30]
OUTPUT 707;"YORIGIN?"
ENTER 707;Yor$
PRINT Yor$
```


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YREFerence

query

This query returns the current y-reference value in the preamble. This value specifies the data point where the y-origin occurs.

Query Syntax: YREFerence?

Returned Format: [YREFerence]<NR1><crlf>

```
Example:  DIM Yref$[30]
          OUTPUT 707;"YREFERENCE?"
          ENTER 707;Yref$
          PRINT Yref$
```

Note

*For example: if the y reference is 64, and the y-origin is 1.1 V and the y-increment is 150 mV, then a data point whose y value is 93 would corresponds to a voltage of (93 - 64)*150 mV + 1.1 V or 5.45 V.*

NOTES:

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10-18. DATA MOVEMENT IN THE 54110D

Data in the 54110D may be moved inside the instrument between several different memories. Each of these memories has a specific function. These memories are diagrammed in Figure 10-14.

Fast ECL memory stores the data from the Analog to Digital converters for Channel 1 and Channel 2.

The active display memory contains the information that is currently being displayed on the 54110D's CRT. This memory is organized as 4 pixel arrays of 256 (vertical) by 501 (horizontal) bits or 64K bytes

The waveform memories are the same waveform memories that are accessible from the front panel. These memories may contain up to 1024 data points. If the ACQuire TYPE is ENVELOPE, minimum and maximum data for channel 1 will be stored in memories 1 and 3 respectively, similarly, minimum and maximum data from channel 2 will be stored in memories 2 and 4.

The pixel memories are used to store copies of pictures from the active display memory. These two memories are organized the same way as the active display memory.

The HP-IB commands that control the movement of data in the 54110D are listed below and are shown in Figure 10-14 in the data paths that they control.

RUN causes the 54110D to acquire data for the active display memory.

MERGE copies the contents of the active display memory into either pixel memory 5 or 6.

TRANsfer allows the movement of data from any of the 4 waveform memories to either of the pixel memories.

DIGitize instructs the instrument to acquire data based on the conditions setup in the ACQuire subsystem. Data from channel 1 is placed in waveform memory 1 and data from channel 2 is placed in waveform memory 2, unless the ACQuire TYPE is ENVELOPE, then minimum and maximum data from channel 1 is stored in waveform memories 1 and 3 respectively, similarly, minimum and maximum data from channel 2 will be stored in waveform memories 2 and 4.

DATA may be moved to and from the waveform memories with the WAVeform DATA(?) commands.

DATA may also be moved to and from the pixel storage memories or the active display memory with DISPlay DATA(?) commands.

Measurements (MEASure subsystem) are performed using data from the fast ECL memory when the source is an active channel or function.

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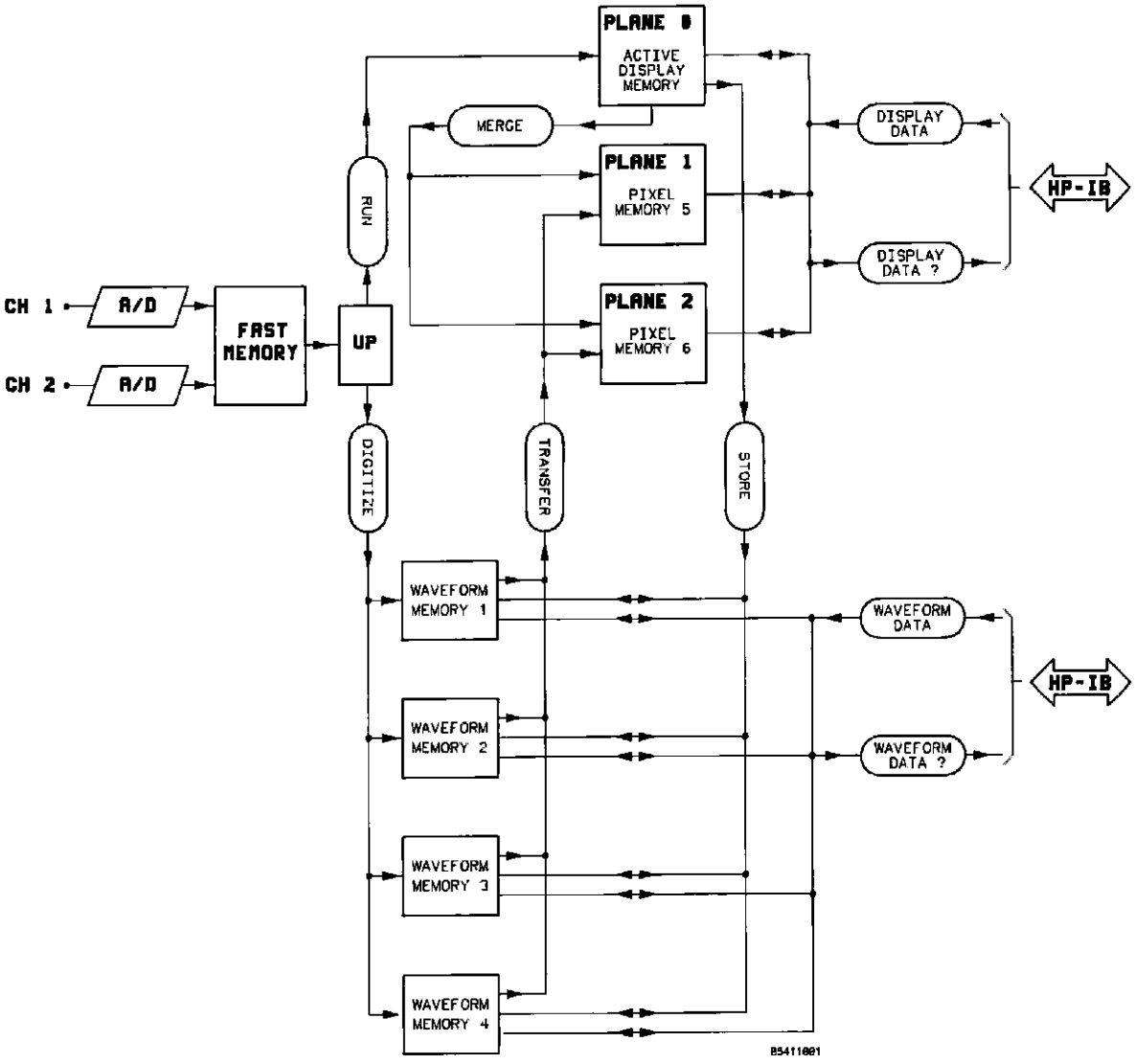


Figure 10-14. Data Flow

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Appendix A
Example/Demo Programs

INTRODUCTION

This section contains example programs using the command set for the 54110D. In general, they use the longform of the command with alpha, (as opposed to numeric), arguments with each command using a separate output statement for clarity. To optimize speed, switch to concatenated shortform numerics.

Throughout these examples the 54110D is assumed to be at address 7, the hardcopy devices are assumed to be at address 1, and the system bus is at 700. The input signal used is the calibration signal available from the rear panel of the instrument connected to channel 1.

All programs were developed on an HP 200 series scientific computer using HP Basic 4.0. Several examples use the BASIC command "ENTER 2". This pauses program execution until the "ENTER" key is depressed on the controller. This is used to separate different blocks in the example for feature dramatizations, for user interaction, or to wait for the 54110D to finish something such as a hardcopy dump or an acquisition

```
10    ! This sample program demonstrates some of the commands
20    ! used to set a vertical channel, in this case channel 1.
30    ! This program works well using the cal signal from the
40    ! rear panel of the instrument.  The program assumes that
45    ! the probe attenuation factor for channel 1 is 1.
50    CLEAR 707                          ! Device clear command,
60    !                                    initializes HP-IB registers.
70    !
80    OUTPUT 707;"AUTOSCALE"             ! Autoscales the unit
90    OUTPUT 707;"CHANNEL1"              ! Enter Ch1 subsystem
100   OUTPUT 707;"OFFSET 0.0"            ! Set offset to 0 volts
110   REAL Offset,Range
120   INTEGER J
130   Offset=0.                          ! Set offset variable to 0
140   FOR J=1 TO 11
150      OUTPUT 707;"OFFSET";Offset      ! Set next offset
160      Offset=Offset-.04
170      WAIT .3
180      NEXT J
190   !
200   !
210   !
```


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```
220   OUTPUT 707;"AUTOSCALE"            ! Does as it says
230   OUTPUT 707;"RANGE .080"           ! Set vertical range to 80 mvolts (min)
240   !                                    Can also use "SENSITIVITY" for
250   !                                    volts/div
260    Range=.08                        ! Set range variable to minimum range
270   !                                    or maximum sensitivity
280    FOR J=1 TO 7
290       OUTPUT 707;"RANGE";Range      ! Set new range
300       Range=Range*2
310       WAIT .3
320       NEXT J
330   !
340   !
360    OUTPUT 707;"GRAPH1"              ! Enter GRAPH subsystem
370    OUTPUT 707;"YOFFSET -.1"         ! Set magnified offset
380    OUTPUT 707;"YRANGE 4.0"          ! Set magnified range
390    OUTPUT 707;"MAGNIFY WINDOW"      ! Turns on magnify window
400    Range=4.0
410    FOR J=1 TO 5
420       OUTPUT 707;"YRANGE";Range     ! Set new magnified range
430       Range=Range/1.5               ! Automatically moves markers
440       WAIT .3                       ! to reflect new range
450       NEXT J
460    !
470    OUTPUT 707;"MAGNIFY ON"          ! Puts unit in the magnify mode.
480    LOCAL 707                        ! Returns the 54110D to local
490    END                              ! operation.
```

```
10    ! This is a sample program demonstrating the TIMEBASE
20    ! subsystem.  The rear panel cal signal works well
30    ! with this program.
40    CLEAR 707                              ! Device clear command
50    !                                        initializes the HP-IB registers.
60    !
70    OUTPUT 707;"AUTOSCALE"                 ! Does as it says.
80    REAL Sens,Delay
90    INTEGER J
100   OUTPUT 707;"TIMEBASE"                  ! Enter TIMEBASE subsytem.
110   OUTPUT 707;"SENSITIVITY 200E-9"        ! Set timebase to 200 nsec/div.
120   !                                        Can also use "RANGE" for
130   !                                        full scale setting.
140   !
150   OUTPUT 707;"DELAY 0.0 "                ! Set delay to 0.
160   OUTPUT 707;"REFERENCE LEFT"            ! Puts delay reference at left
170   !                                        side of graticule.
180   !
```


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```
190   Delay=0.                                  ! Sets delay to 0.
200   FOR J=1 TO 25
210      OUTPUT 707;"OFFSET ";Delay             ! "OFFSET" = "DELAY".
220      WAIT .23
230      Delay=Delay-1.00E-7
240      NEXT J
250   !
260   !
270   !
280   OUTPUT 707;"AUTOSCALE"                    ! Does as it says.
290   Range=.080                                ! Sets full scale to 80 msec
300   !                                           i.e., 8 ms/div.
310   FOR J=1 TO 25
320      OUTPUT 707;"RANGE";Range               ! Next full scale range.
330      Range=Range/2
340      WAIT .4
350      NEXT J
360   !
370   WAIT 1
380   !
390   !
400   !       NOTICE HOW DATA IS ACQUIRED AND
410   !       THAT DATA POINTS ARE 25 ns APART
420   !       FOR EVERY ACQUISITION.
430   !
440   !
441   OUTPUT 707;"HEADER OFF"                   ! Turn off headers in query reply.
450   OUTPUT 707;"AUTOSCALE"                    ! Does as it says.
460   OUTPUT 707;"SENSITIVITY?"                 ! Ask for time/div.
470   ENTER 707;Sens                            ! Read time/div.
480   Sens=Sens/8
490   OUTPUT 707;"SENSITIVITY";Sens             ! Set faster sweep speed.
500   OUTPUT 707;"STOP"                         ! Halt acquisition (system command)
510   OUTPUT 707;"ERASE PLANE0"                 ! Clears the active display plane
520   !                                           This is a system command.
530   OUTPUT 707;"MODE SINGLE"                  ! Sets for single shot operation.
540   FOR J=1 TO 20
550          OUTPUT 707;"RUN"                   ! One acquisition.
560   !
570          WAIT 1
580          NEXT J
590   !
600   !
610   OUTPUT 707;"MODE TRIGGERED"               ! Puts unit in the triggered mode.
620          OUTPUT 707;"RUN"                   ! Starts acquisition.
630   END
```


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```
10    ! This sample program demonstrates some of the commands in the
20    ! Hardcopy subsystem and the PLOT command.  It assumes that
30    ! the scope is at address 7, the printer is at address 1, and
40    ! that the system bus is 700.
50    CLEAR 707
60    OUTPUT 707;"HARDCOPY"                ! Puts the scope in the HARDCOPY
70    !                                      subsystem.
80    OUTPUT 707;"PEN AUTO"                ! Sets the 54110D to the auto
90    !                                      pen mode.
100   OUTPUT 707;"SOURCE PLANE0,FACTORS"   ! Selects the active display
110   !                                      (plane0) and the scale factors
120   !                                      for output.
130   !
140   OUTPUT 707;"PLOT"                    ! Outputs data to the plotter
150   SEND 7;UNT UNL                       ! Clears bus
160   SEND 7;LISTEN 1                      ! Tells printer to listen
170   SEND 7;TALK 7                        ! Sets scope to talk mode
180   SEND 7;DATA
190   WAIT 180                             ! Wait 3 minutes for transfer to
200   !                                      complete.
210   !                                      Note:  If programming, use the
220   !                                      SRQ capabilities of the 54110D
230   !                                      to determine when the transfer
240   !                                      is complete.
245   !                                      Attempting to program the
250   !                                      program the 54110D while making
260   END                                  ! a hardcopy dump will cause errors.
```

```
10    ! This sample program demonstrates some of the commands in the
20    ! Hardcopy subsystem.  The service request is used to detect
30    ! when printing is complete.  The program assumes that a
40    ! graphics printer is used and its address is set to 1.
50    CLEAR 707
60    OUTPUT 707;"REQUEST 4112"            ! Request mask where:
70    !                                      Bit 12 = Hardcopy complete = 4096
80    !                                      Bit  4 = Ready bit = 16
90    !                                       Set so bit 12 causes SRQ
100   OUTPUT 707;"REQUEST ON"              ! Enables scope's Service Request
110   ON INTR 7 GOTO 270                   ! Exit printing routine after SRQ
120   ENABLE INTR 7;2                      ! Enables SRQ on bus #7
130   DISABLE INTR 7                       ! Disables all interrupts on bus #7
140   OUTPUT 707;"HARDCOPY"                ! Puts the scope in the HARDCOPY
150   !                                      subsystem.
160   OUTPUT 707;"PAGE AUTO"               ! Sets the scope to automatically
170   !                                       output a formfeed
180   OUTPUT 707;"SOURCE PLANE0,FACTORS"   ! Selects the active display
190   !                                      (plane0) and the scale factors.
```


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```
200   OUTPUT 707;"PRINT"                    ! Starts print buffering
210   SEND 7;UNT UNL                        ! Clears bus
220   SEND 7;LISTEN 1                       ! Tells printer to listen
230   SEND 7;TALK 7                         ! Puts the scope in talk mode
240   SEND 7;DATA                           ! Lowers the ATN line @ controller
250   ENABLE INTR 7                         ! Enables SRQ interrupt
260   GOTO 260                              ! Loops until printing is complete
270   A=SPOLL(707)                          ! Clear service request
280   END
```

```
10    ! This sample program demonstrates using the memories for
20    ! measurements and performing measurements on single shot
40    ! data.  Before running the program, connect the cal signal
50    ! on the rear panel of the instrument to the Channel 1 input.
70    !
80    ! Setup signal.
90    !
100   CLEAR 707                           ! Initialize HP-IB registers.
110   OUTPUT 707;"AUTOSCALE"              ! Scale the signal.
120   OUTPUT 707;"TIMEBASE RANGE 250E-9"  ! Set to 25 nsecs/division.
130   !
140   ! Acquire single sweep of signal - 10 points.
150   !
160   OUTPUT 707;"ACQUIRE POINTS 500 "    ! Full screen is 500 points.
170   OUTPUT 707;"TYPE 1"                 ! Acquisition type is normal.
180   OUTPUT 707;"COMPLETE 0"             ! Acquire 1 sweep.
190   OUTPUT 707;"DIGITIZE CHANNEL 1"     ! Acquire Ch1 data to Memory 1.
200   OUTPUT 707;"BLANK CHANNEL 1"        ! Turn off Ch1.
210   !
220   ! Measure peak to peak voltage of memory 1.
230   !
240   OUTPUT 707;"MEAS SOURCE MEMORY1"    ! Set measurement source.
250   OUTPUT 707;"VPP?"                   ! Measure peak to peak voltage.
260   DIM Vpp$[20]
270   ENTER 707;Vpp$
280   PRINT Vpp$                          ! Print results.
290   END
```

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```
10    !
20    !  This program demonstrates some of the learn string capabilities.
30    CLEAR 707
40    !
50    !
60    DIM Setting$[276]               !  266 = # of bytes in learn string
70    !                                  plus 10 = "SETUP #A**"
80    !                                  Where SET = header
90    !                                         #A = indicates binary block
100   !                                         ** = 2 byte integer = length
110   OUTPUT 707;"LONGFORM ON"        ! Use longform of mnemonics.
120   OUTPUT 707;"HEADER ON"          ! Tells the 54110D to precede the
130   !                                 learn string with a header.
140   OUTPUT 707;"EOI ON "            ! Tells the 54110D to output an EOI
150   !                                   with the last byte.
160   OUTPUT 707;"SETUP?"             ! This asks the scope for the learn string
170   ENTER 707 USING "-K";Setting$   ! Reads in header and string.  (-K tells
180   !                                 computer to treat CR & LF as data).
190   LOCAL 707                       ! Puts scope in local operation.
200   !
210   !
220   !
230   ENTER 2                          ! This allows you to change the scope's
240   !                                  setup.
250   !                                  Hit 'ENTER' to continue
260   !
270   !
280   OUTPUT 707;Setting$              ! Outputs the learn string and header.
290   !                                  Scope is reset to previous setup.
300   !
310   LOCAL 707                        ! Returns scope to local operation.
320   !
330   END
```

```
10    ! This sample program demonstrates some of the commands in the
20    ! MEASURE Subsystem.
30    !
40    CLEAR 707
50    OUTPUT 707;"AUTOSCALE"                ! Does as it says
60    OUTPUT 707;"ACQUIRE TYPE NORMAL"      ! Sets display mode to Normal
70    OUTPUT 707;"DISPLAY"                  ! Selects DISPLAY Subsystem
80    OUTPUT 707;"TMARKER ON"               ! Turn on Tmarkers
90    !
100   !
110   OUTPUT 707;"MEASURE"                  ! Selects MEASURE subsystem
120   OUTPUT 707;"PRECISION HIGH"           ! Sets precision for maximum accuracy
130   OUTPUT 707;"SOURCE CHANNEL 1"         ! Channel 1 is the measurement source
```


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```
140  OUTPUT 707;"VSTART -.2"              ! Sets voltage markers to
150  OUTPUT 707;"VSTOP -.2"               !  -200 mV.  This will be used as a
160  !                                       reference for the edge find
170  !                                       function.
180  INTEGER J
190  FOR J=1 TO 2
200       OUTPUT 707;"ESTART +";J         ! Find Jth positive edge
210       WAIT .75
220       OUTPUT 707;"ESTOP -";J          ! Find Jth negative edge
230       WAIT .75
240       NEXT J
250  !
260  ENTER 2                              ! This statement causes a pause in the
270  !                                       program, press ENTER on the control-
280  !                                       ler to continue.
290  !
300  !
310  REAL Delay,Offset
320  Delay=2.4E-6                         ! Initialize delay variable
330  Offset=.4                            ! Initialize offset variable
340  FOR J=1 TO 20
350      OUTPUT 707;"TSTART";Delay        ! Move time start marker
360      OUTPUT 707;"TSTOP";-Delay        ! Move time stop marker
370      OUTPUT 707;"VSTART";-.19-Offset  ! Move voltage start marker
380      OUTPUT 707;"VSTOP";-.19+Offset   ! Move voltage stop marker
390      Offset=Offset-.04
400      Delay=Delay-2.40E-7
410      NEXT J
420  !
430  ENTER 2                              ! Same as line 230.
440  !
450  !
460  OUTPUT 707;"PRECISION LOW"           ! Sets the PRECISION flag low.
470  !                                       Low precision uses previously
480  !                                       acquired data for measurements.
490  !                                       This allows faster completion of
500  !                                       measurements at the expense of some
510  !                                       accuracy and repeatability.
520  OUTPUT 707;"ALL?"                    ! Measure all parameters. They will be
530  !                                       displayed on scope, and are
540  !                                       available over HP-IB.
550  !
560  !
570  !
580  ENTER 2                              ! Pause
590  !
600  !
```


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```
610  OUTPUT 707;"RISE?"                    ! Measure RISE time using low
620  !                                       precision.  You set precision
630  !                                       flag earlier.
640  ENTER 2                               ! Pause
650  !
660  !
670  OUTPUT 707;"PRECISION HIGH"           ! Set PRECISION flag high.
680  OUTPUT 707;"RISE?"                    ! Measure precise RISE time.
690  !                                       Watch the display during this
700  !                                       measurement.
710  !
720  !
730  !
740  OUTPUT 707;"PRECISION LOW"            ! Sets PRECISION flag low.
750  LOCAL 707                             ! Puts the 54110D in local operation.
760  END
```

```
10    !
20    ! This sample program demonstrates more uses of the Service
30    ! Requests (SRQ's).  This set of instructions uses: Hardcopy
40    ! Done, Local, Front Panel Service, Ready bit and  Ready Masks.
50    ! The scope  will monitor the front panel for SRQ's and echo
60    ! any activity. Any Advisories or Acquisitions initiated
70    ! by the front panel will be disclosed. These examples assume
80    ! the scope to be at address 7 and the plotter to be at address
90    ! 1 on bus #7.
100   !
110   CLEAR 707
120   PRINTER IS 1                          ! Display is PRINT destination
130   DIM K$[80],A$[80]
140   !
150   ON INTR 7 GOSUB Srq_svc               ! Goto 'Srq_svc' on Service Request
160   ENABLE INTR 7;2                       ! Enables SRQ on bus #7
170   DISABLE INTR 7                        ! Disables all interrupts on bus #7
180   !
190   PRINT
200   OUTPUT 707;"RESET"                    ! Resets 54110D.
210   OUTPUT 707;"AUTOSCALE"                ! Does as it says
220   OUTPUT 707;"ACQUIRE MODE AVERAGE"     ! Puts scope into averaged mode.
230   WAIT 4                                ! Wait for data accumulation
240   INTEGER Rqsmask
250   Rqsmask=4096+16+4                     ! request mask
260   !                                       4096 = Hardcopy done - bit 12
270   !                                         16 = Ready - bit 4
280   !                                          4 = Front Panel Service - bit 2
290   !                                              Set so bit 12 causes an SRQ
```


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```
300   OUTPUT 707;"REQUEST";Rqsmask          ! Send Request Mask
310   OUTPUT 707;"REQUEST ON"               ! Sets RQS - bit 6 on request mask
320   OUTPUT 707;"LONGFORM ON"              ! Sets longform for headers.
330   OUTPUT 707;"HEADER ON"                ! Sets headers on for queries.
340   Stat=SPOLL(707)                       ! Serial Poll scope, should be 0.
350   PRINT "Result of Serial Poll is ";Stat
360   !
370   Dump_flag=0
380   OUTPUT 707;"HARDCOPY SOURCE PLANE0,FACTORS" ! Selects active display and
390   !                                             scale factors for output.
400   OUTPUT 707;"PEN AUTO"                       ! Sets auto pen on.
410   OUTPUT 707;"PRINT"                          ! Starts Plot.
420   SEND 7;UNT UNL                              ! Turns off entire bus.
430   SEND 7;LISTEN 1                             ! Sets plotter to listen.
440   SEND 7;TALK 7                               ! Sets scope to talk.
450   SEND 7;DATA                                 ! Lower ATN line 0 controller
460   !
470   ENABLE INTR 7                               ! Enables interupts on bus #7.
480   !
490   IF Dump_flag=0 THEN
500      PRINT
510      PRINT " Waiting for hardcopy transfer to complete."
520      PRINT " Time available for other tasks."
530      PRINT " !!!!    Bus is  NOT  available      !!!!!"
540      WAIT 2
550      GOTO 490
560   END IF
570   GOTO 570
580   !
590   !
600   !
610   ! Service request interrupt routine.
620   !
630 Srq_svc:!
640   Stat=SPOLL(707)                           ! Perform serial poll
650   !                                           and clear SRQ.
660   INTEGER J
670   PRINT
680   PRINT "Service Request Status= ";Stat
690   !
700   !
710   IF BIT(Stat,0) THEN                       ! 54110D is not a controller.
720   PRINT "RQC should not be set - PROBLEM"   !  RQC cannot be set by 54110D.
730   END IF
740   !
750   !
760   IF BIT(Stat,1) THEN                       ! RAM power failure
770   PRINT "PWR status has been set-WHY?"
780   END IF
790   !
800   !
```


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```
810   IF BIT(Stat,2) THEN                          ! Front Panel Service
820     PRINT "FPS status has been set"
830     OUTPUT 707;"KEY?"                          ! Asks for key code.
840     ENTER 707;K$                               ! Reads key code.
850     OUTPUT 707;K$                              ! Outputs key code.
860     PRINT "      "&K$
870   END IF
880   !
890   !
900   IF BIT(Stat,3) THEN                          ! Local operation occurred.
910      PRINT "LCL operation has occured"
920   END IF
930   !
940   !
950   IF BIT(Stat,4) THEN                          ! Ready bit - only bit active
960      PRINT "Hardcopy Complete  !!"             ! in the Ready byte is Hardcopy
970      IF Dump_flag=0 THEN                       ! Complete.
980          SEND 7;UNT UNL
990          Dump_flag=1
1000     END IF
1010     PRINT "Now try pressing keys, they will echo from controller"
1020  END IF
1030  !
1040  !
1050  IF BIT(Stat,5) THEN                       ! Go read the errors.
1060    REPEAT
1070      OUTPUT 707;"ERR?"                     ! Asks for next error in queue.
1080      ENTER 707;A$                          ! Reads next error.
1090      PRINT "Error was : ";A$               ! Prints next error.
1100    UNTIL VAL(A$[9,12])=0                   ! Until error queue is empty.
1110  END IF
1120  !
1130  !
1140  IF BIT(Stat,6) THEN                       ! A SRQ was generated by someone.
1150    OUTPUT 707;"REQUEST?"                   ! Asks for mask value.
1160    ENTER 707;A$                            ! Reads mask value.
1170    PRINT A$&" is the mask value"
1180  END IF
1190  !
1200  !
1210  IF BIT(Stat,7) THEN                       ! Advisory has been initiated
1220    OUTPUT 707;"DSP?"                       ! Asks for advisory.
1230    ENTER 707;A$                            ! Reads advisory.
1240    PRINT A$&" is the Advisory"             ! Prints advisory.
1250  END IF
1260  !
1270  !
1280  ENABLE INTR 7
1290  RETURN
1300  !
1310  END
```


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```
10    !
20    ! This sample program demonstrates some of the uses of
30    ! Service Requests (SRQ's).  This set of instructions uses
40    ! the Acquisition Done, Local, Front Panel Service,
50    ! Ready and Ready masks.  An acquisition that will produce
60    ! buffered results will be started.  When a SRQ is sent the
70    ! results will be read and displayed.  The scope will then
80    ! monitor the front panel keys using SRQ's and echo any
90    ! activated.   Any Advisories or Acquisitions initiated from
100   ! the front panel will be disclosed.
110   !
120   CLEAR 707
130   !
140   PRINTER IS 1                          ! Display is PRINT destination
150   DIM B$(1:16)[30],K$[80],A$[80]
160   !
170   ON INTR 7 GOSUB Srq_svc               ! Goto 'Srq_svc' on Service Request.
180   ENABLE INTR 7;2                       ! Enables SRQ on bus #7.
190   DISABLE INTR 7                        ! Disables all interuppts on bus #7.
200   !
210   PRINT
220   OUTPUT 707;"RESET"                    ! Resets 54110D
230   OUTPUT 707;"AUTOSCALE"                ! Does as it says.
240   INTEGER Rqsmask
250   Rqsmask=1024+16+4                     ! Request mask where:
260   !                                       1024 = Acquisition done - bit 10.
270   !                                         16 = Ready - bit 4.
280   !                                          4 = Front Panel Service - bit 2.
290   !
300   OUTPUT 707;"REQUEST";Rqsmask          ! Sends Request Mask.
310   OUTPUT 707;"REQUEST ON"               ! Sets RQS - bit 6 in Request mask.
320   OUTPUT 707;"LONGFORM ON"              ! Turns on longform for headers.
330   OUTPUT 707;"HEADER ON"                ! Turns headers on for queries.
340   Stat=SPOLL(707)                       ! Serial Poll scope, should be 0
350   PRINT "Result of Serial Poll is ";Stat
360   !
370   Meas_flag=0
380   OUTPUT 707;"MEASURE "                 ! Enters MEASURE subsystem.
390   OUTPUT 707;"SOURCE CHANNEL 1"         ! Channel 1 is source for measurement
```


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```
400   OUTPUT 707;"PRECISION HIGH; ALL?"     ! Sets PRECISION flag high and
410   !                                       measures all.
420   ENABLE INTR 7                         ! Enables interuppts on bus #7.
430   !
440   PRINT " Waiting for measurement to complete."
450   PRINT " Time available for other tasks."
460   PRINT " Bus is available."
470   !
480   GOTO 480                              ! Loop until Service Request occurs.
490   !
500   !
510   !
520   ! Service Request Interuppt Routine
530   !
540 Srq_svc:                                !
550   Stat=SPOLL(707)                       ! Performs a Serial Poll
560   !                                       and clears SRQ.
570   INTEGER J
580   PRINT
590   PRINT "Service Request Status= ";Stat
600   !
610   !
620   IF BIT(Stat,0) THEN                   ! Request Control - 54110D is
630      PRINT "RQC should not be set - PROBLEM" !  not a controller and
640   END IF                                !  cannot send a RQC.
650   !
660   !
670   IF BIT(Stat,1) THEN                   ! RAM power failure.
680      PRINT "PWR status has been set.  WHY?"
690   END IF
700   !
710   !
720   IF BIT(Stat,2) THEN                   ! Front Panel Service.
730     PRINT "FPS status has been set"
740     OUTPUT 707;"Key?"                   ! Asks for key code.
750     ENTER 707;k$                        ! Reads key code.
760     OUTPUT 707;K$                       ! Outputs key code.
770     PRINT "      "&K$
780   END IF
790   !
800   !
810   IF BIT(Stat,3) THEN                   ! Local operation occurred
820      PRINT "LCL operation has occured"
830   END IF
840   !
850   !
```


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```
860   IF BIT(Stat,4) THEN                          ! Ready bit - only bit active
870      PRINT "Acquisition done !"                ! in the Ready byte is Acq done
880      IF Meas_flag=0 THEN                       ! first time through
890           FOR J=1 TO 16                        !
900           ENTER 707;B$(J)                      ! Reads measurement results
910           PRINT B$(J)                          ! and prints them.
920           NEXT J
930           Meas_flag=1
940           PRINT
950           PRINT "Press some keys.  The key number will be printed."
960      END IF
970   END IF
980   !
990   !
1000  IF BIT(Stat,5) THEN                     ! Go read the errors.
1010    REPEAT
1020      OUTPUT 707;"ERR?"                   ! Asks for next error in queue.
1030      ENTER 707;A$                        ! Reads error.
1040      PRINT "Error was : ";A$             ! Prints error.
1050    UNTIL VAL(A$[3,12])=0                 ! Until error queue is empty.
1060  END IF
1070  !
1080  !
1090  IF BIT(Stat,6) THEN                     ! A SRQ has been generated.
1100    OUTPUT 707;"REQUEST?"                 ! Ask for mask value.
1110    ENTER 707;A$                          ! Reads mask value.
1120    PRINT A$&" is the mask value"         ! Prints mask value.
1130  END IF
1140  !
1150  !
1160  IF BIT(Stat,7) THEN                     ! Advisory has been initiated.
1170    OUTPUT 707;"DSP?"                     ! Asks for advisory.
1180    ENTER 707;A$                          ! Reads advisory.
1190    PRINT A$&" is the Advisory"           ! Prints the advisory.
1200  END IF
1210  !
1220  !
1230  ENABLE INTR 7                           ! SRQ disables interrupts.
1240  RETURN                                  ! This reenables them.
1250  !
1260  END
```


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```
10    !
20    ! This sample program demonstrates some of the uses of
30    ! Service Requests (SRQ's).  This set of instructions uses
50    ! the Acquisition Done, Local, Front Panel Service,
60    ! Ready and Ready masks.  An acquisition that will produce
65    ! buffered results will be started.  When a SRQ is sent the
75    ! results will be read and displayed.  The scope will then
80    ! monitor the front panel keys using SRQ's and echo any
90    ! activity.  Any Advisories or Acquisitions initiated from
100   ! the front panel will be disclosed.
110   !
120   CLEAR 707
130   !
140   PRINTER IS 1                          ! Display is PRINT destination
150   DIM B$(1:16)[30],K$[80],A$[80]
160   !
170   ON INTR 7 GOSUB Srq_svc               ! Goto 'Srq_svc' on Service Request.
180   ENABLE INTR 7;2                       ! Enables SRQ on bus #7.
190   DISABLE INTR 7                        ! Disables all interuppts on bus #7.
200   !
210   PRINT
220   OUTPUT 707;"RESET"                    ! Resets 54100A/D.
230   OUTPUT 707;"AUTOSCALE"                ! Does as it says.
240   INTEGER Rqsmask
250   Rqsmask=1024+16+4                     ! Request mask where:
260   !                                       1024 = Acquisition done - bit 10.
270   !                                         16 = Ready - bit 4.
280   !                                          4 = Front Panel Service - bit 2.
290   !                                              Set so bit 10 causes an SRQ
300   OUTPUT 707;"REQUEST";Rqsmask          ! Sends Request Mask.
310   OUTPUT 707;"REQUEST ON"               ! Sets RQS - bit 6 in Request mask.
320   OUTPUT 707;"LONGFORM ON"              ! Turns on longform for headers.
330   OUTPUT 707;"HEADER ON"                ! Turns headers on for queries.
340   Stat=SPOLL(707)                       ! Serial Poll scope, should be 0
350   PRINT "Result of Serial Poll is ";Stat
360   !
370   Meas_flag=0
380   OUTPUT 707;"MEASURE "                 ! Enters MEASURE subsystem.
381   OUTPUT 707;"SOURCE CHANNEL 1"         ! Channel 1 is source for measurement
390   OUTPUT 707;"PRECISION HIGH; ALL?"     ! Sets PRECISION flag high and
400   !                                       measures all.
410   ENABLE INTR 7                         ! Enables interuppts on bus #7.
420   !
430   PRINT " Waiting for measurement to complete."
440   PRINT " Time available for other tasks."
450   PRINT " Bus is available."
460   !
470   GOTO 470                              ! Loop until Service Request occurs.
480   !
```


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```
490   !
500   !
510   ! Service Request Interuppt Routine
520   !
530 Srq_svc:!
540   Stat=SPOLL(707)                        ! Performs a Serial Poll
550   !                                        and clears SRQ.
560   INTEGER J
570   PRINT
580   PRINT "Service Request Status= ";Stat
590   !
600   !
610   IF BIT(Stat,0) THEN                  ! Request Control - 54110D is
620      PRINT "ROC should not be set - PROBLEM" !  not a controller and
630   END IF                                  !  cannot send a RQC.
640   !
650   !
660   IF BIT(Stat,1) THEN                    ! RAM power failure.
670      PRINT "PWR status has been set.  WHY?"
680   END IF
690   !
700   !
710   IF BIT(Stat,2) THEN                    ! Front Panel Service.
720     PRINT "FPS status has been set"
730     OUTPUT 707;"Key?"                    ! Asks for key code.
740     ENTER 707;K$                         ! Reads key code.
750     OUTPUT 707;K$                        ! Outputs key code.
760     PRINT "      "&K$
770   END IF
780   !
790   !
800   IF BIT(Stat,3) THEN                    ! Local operation occurred
810      PRINT "LCL operation has occured"
820   END IF
830   !
840   !
850   IF BIT(Stat,4) THEN                    ! Ready bit - only bit active
860      PRINT "Acquisition done !"          ! in the Ready byte is Acq done
870      IF Meas_flag=0 THEN                 ! First time thru?
880           FOR J=1 TO 16                  !
890           ENTER 707;B$(J)                ! Reads measurement results
900           PRINT B$(J)                    ! and prints them.
910           NEXT J
920           Meas_flag=1
930           PRINT
940           PRINT "Press some keys.  The key number will be printed out."
950      END IF
960   END IF
970   !
980   !
```


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```
990   IF BIT(Stat,5) THEN                    ! GO read the errors.
1000    REPEAT
1010      OUTPUT 707;"ERR?"                  ! Asks for next error in queue.
1020      ENTER 707;A$                       ! Reads error.
1030      PRINT "Error was : ";A$            ! Prints error.
1040    UNTIL VAL(A$[9,12])=0                ! Until error queue is empty.
1050  END IF
1060  !
1070  !
1080  IF BIT(Stat,6) THEN                    ! A SRQ has been generated.
1090    OUTPUT 707;"REQUEST?"                ! Ask for mask value.
1100    ENTER 707;A$                         ! Reads mask value.
1110    PRINT A$&" is the mask value"        ! Prints mask value.
1120  END IF
1130  !
1140  !
1150  IF BIT(Stat,7) THEN                    ! Advisory has been initiated.
1160    OUTPUT 707;"DSP?"                    ! Asks for advisory.
1170    ENTER 707;A$                         ! Reads advisory.
1180    PRINT A$&" is the Advisory"          ! Prints the advisory.
1190  END IF
1200  !
1210  !
1220  ENABLE INTR 7                          ! SRQ disables interrupts.
1230  RETURN                                 ! This reenables them.
1240  !
1250  END
```


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```
10    ! This sample program demonstrates some of the text commands
20    ! in the Display subsystem.
40    !
50    ! Disable the instrument from writing text to the screen and
60    !   set the colors.
70    !
80    CLEAR 707
90    OUTPUT 707;"DISPLAY MASK 0"    ! Disable the instrument from
100   !                                writing text to the screen
105   OUTPUT 707;"ATTRIBUTE ENABLE" ! Enable embedded attributes
110   OUTPUT 707;"PRIORITY ON"      ! Text overwrites graphics
120   OUTPUT 707;"SETCOLOR DEFAULT" ! Turn on the default colors
130   !
140   ! Write a color block to each position on screen
150   !
160   FOR Row=0 TO 22
170   FOR Column=0 TO 71
180     Attribute=129                ! Use the inverse video attribute
190     Attribute=Attribute+8*((Row+Column) MOD 16) ! Set the color
200     OUTPUT 707;"ROW ";Row;"COLUMN ";Column ! Send row and column
210     ! Output a single character block with its attribute
220     OUTPUT 707 USING "8A,B,2A";"STRING """,Attribute," """
230   NEXT Column
240   NEXT Row
250   !
260   ! To get back to the normal display, turn the instrument off
270   ! and then on again.  This resets the display MASK.
290   !
300   END
```


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Appendix B
SOFTWARE DELAY CALIBRATION AND TRIGGER DELAY OPTIMIZATION

The trigger delay and channel to channel skew calibrations in the Cal menu on the 54110D are provided to null delay differences in the trigger and data acquisition paths of the trigger and the data. This would include acquisition time differences both internal and external to the instrument.

Channel to channel skew adjustment is used to change the placement of the channel 2 data relative to channel 1 so delay differences in the data acquisition paths do not introduce offsets in channel-to-channel time interval measurements.

Differences in internal delays as well as differences in external delays caused by dissimilar probes, cable lengths etc. can be nulled. This is done by injecting the cal signal at the probe tips or other desired points when performing the calibrations.

The trigger delay calibrations are used to position waveforms horizontally so that the zero reference corresponds with the trigger event. When both the internal and external delays have been compensated for, the instrument provides a timebase delay that is calibrated in an absolute sense to the trigger point. The timebase delay tells you where the display window is located relative to the trigger.

Trigger delay calibrations do not affect channel-to-channel measurements as the vertical inputs are always displayed relative to each other depending on the setting of the ch-to-chCC Skew cal factor. As long as the Ch-to-Ch Skew cal factor is set correctly you can make accurate channel-to-channel measurements even if the trigger delay cal factors are not set correctly.

The delay calibration feature, a consequence of the 54110D's negative time and digital architecture, is convenient for referencing measurements to the probe tips, or other points, even if different types of probes or a probe multiplexer is used. To calibrate a given probe configuration inject a fast risetime signal at the probe tips, or wherever you want your measurement to be referenced and follow the instructions in the Cal menu. Refer to Section 6 for a discussion of the cal menu.

Once the cal procedure is completed the trigger edge will be displayed at the time-zero reference, and if you use an external trigger the time-zero reference will correspond to the time of the trigger event at the Trig 3 or 4 probe tip, or other point of interest. The cal factors are stored in the nonvolatile SAVE/RECALL registers. This allows the instrument to retained calibrations for up to 10 different probe or measurement configurations. By using the time interval measurements built into the 54110D, the display skew and trigger delay cal factors can be determined and programmed via the HP-IB.

The trigger delay calibrations compensate for delays to a first order approximation. Actual trigger delays, in addition to probe length, are function of signal characteristics such as risetime, amplitude, and rep. rate. If these signal characteristics are not the same when making measurements as they were during calibration, the trigger edges will be displaced from time-zero. The error, however, will be small and will rarely result in any confusion as to which edge is the

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trigger. For fast risetime signals (<3 ns) this displacement will be less than ±400 ps. Because of these second order affects it should not be assumed that the trigger edge is at precisely time-zero when making time interval measurements unless the edges are fast and 400 ps error can be tolerated. These effects apply only to trigger delays as channel-to-channel skew has no dependency on signal characteristics.

For signals with slower edge speeds, trigger hysteresis can cause a displacement from time-zero, however, compared to the sweep speed at which the signal would be viewed the displacement usually would be small. Trigger hysteresis on the 54110D is 1 minor division on channels 1 & 2 and 10 mV (with 50 ohm pods) on Trig 3 & 4. The trigger level is at the center of the hysteresis band and the trigger comparator actually begins to switch when the input voltage is 1/2 a minor division from the programmed threshold. This causes the actual threshold crossing to be displaced from time-zero by the amount of time it takes the signal to traverse 1/2 a minor division vertically. The direction of the displacement depends on the trigger slope. At sweep speeds where the signal appears as anything but a near-horizontal line, this displacement is not significant for viewing but can affect time interval measurements if ignored.

With trigger delay calibration captured signals can be correctly plotted relative to the time-zero reference with a small error caused by the second order effects. This applies for the Edge, State, Time-Delayed, and Event-Delayed modes. In the Pattern mode, however, the instrument does not know which input will provide the trigger and does not know which cal factor to use. In this case the average of Channel 1 and Channel 2 trigger delay cal factors is used as a compromise. This will result in a minimal displacement when the trigger edge comes from one of the vertical channels but a large displacement can result if the trigger comes from Trig 3 or 4.

Large delay differences in the signal paths for channel 1 and channel 2 will result in a large displacement, so it is desirable to match these paths as close to one another as possible if an accurate time-zero reference is needed in the pattern mode. Also of concern, when you are in the pattern mode is the relative skew between the inputs. This skew results from delay differences in the acquisition paths internal and external to the instrument. For example, when using the time qualified pattern, skew can cause the pattern true-time seen by the filter timer to be different that the actual time at the probe tips. Just how much skew, or differential delay, exists between paths is reflected in the trigger delay cal factors(assuming the instrument is calibrated) because the cal factor for each input is referenced to the same channel (channel 1). The difference in the cal factors is equal to the amount of skew in the trigger paths. A more negative cal factor means that the trigger path delay for that channel is longer

The differential delay between channel 1 & 2 and between Trig 3 & 4 is usually less than 400 ps. This assumes the use of 54002A 50 ohm pods and is referenced to the BNC connectors.

The delay through Channel 1 & 2 is nominally 1.6 ns longer than the delay through Trig 3 & 4. This can cause erroneous pattern triggering unless the extra delay is compensated for by inserting extra delay by using longer cables on Trig 3 and Trig 4. Inserting delay(s) to reduce skew for pattern triggering will also reduce time-zero offset in the Pattern mode.

While skew is not of concern with respect to the time-zero reference in other than Pattern mode, it can affect the operation of the other modes. For example, the setup and hold times in the State mode can be different at the probe tips than they are at the instrument's inputs because of dissimilar probes or cable lengths. This is caused by the fact that the trigger circuitry operates on signals in real-time, thus ruling out software calibration.

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Appendix C
Detailed Operation of the Automatic Measurements

INTRODUCTION

The automatic parameter and time interval measurements resident in the 54110D are designed to allow you to optimize measurement speed and accuracy for your application. Depending upon a number of factors such as display mode, number of averages, type of measurement, and state of the precision key or the PRECISION flag (HP-IB), the instrument uses different criteria for establishing how much data needs to be acquired for measurement.

DISPLAY MODE CONSIDERATIONS

The measurements are based on the data that is on the screen. The instrument maintains internal copies of the screen data, on which the measurements are made. If the unit is in the Normal mode it uses only the most recent y axis information in each time bucket to make the measurement.

The waveform area of the screen is 256 pixels high by 501 pixels wide. For most measurements 501 time buckets are used, however, if the sweep is faster than 500 ps/div the number of time buckets is equal to (10 * (time_per_div_/10 ps))+1. The reason for this is that the maximum time resolution for the 54110D is 10 ps.

Most of the measurements use 90% criterion. In the normal mode at least 90% of the time buckets have one data point. In the averaged mode the 90% criterion means that at least 90% of the time buckets have received N data points where N is the number of averages.

One method of trading measurement speed for accuracy is to increase the number of averages in average mode. The larger the number of averages, the more time that will be required to make a measurement, but also, the better the accuracy and repeatability.

FINE PRECISION AND COARSE PRECISION MEASUREMENTS

The 54110D performs two types of automatic measurements; coarse and fine (coarse precision and fine precision). Coarse measurements are made based on the data on screen. If there is insufficient data on the screen, then new data is acquired in order to make the measurement. Fine measurements begin with a course measurement to locate the edge(s). Each edge is then expanded to achieve maximum resolution.

The coarse measurements are. the voltage measurements; the front panel start on edge and stop on edge time interval measurementsag high or low instrument is "Stopped", and all HP-IB measurements when the PRECISION flag is low.

The precise measurements are; the front panel Precise Edge Find measurement, the front panel parameter measurements when the instrument is "Running, and HP-IB time related measurements when the PRECISION flag is high.

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The coarse measurements are as accurate as the precise measurements when the waveforms are fully expanded (edges at a 45 degree angle) and the display data is 90% complete.

COARSE MEASUREMENTS

As mentioned above, coarse measurements use the data on screen unless there is insufficient data. For front panel coarse measurements only 5 data points need to be present on the screen. For HP-IB coarse measurements the screen data must meet the 90% completion criterion. If the data is insufficient, the instrument acquires new data until the 90% completion criterion is met before the measurement is made.

Coarse measurements are faster but their accuracy, unlike precise measurements depends on the sweep speed. The front panel measurements can be made on very limited amount of data. This is important for single shot signals and low rep rate signals when only a limited amount of data has been acquired.

It is a good programming practice to clear the screen when the input signal is changed before making a coarse measurement. This is especially true when a high number of averages or a long persistence has been selected. (Note: in many cases the screen will be cleared automatically when an instrument setting is changed. The exceptions are changes in settings that don't effect the waveform e.g., moving the time or voltage markers.)

PRECISE MEASUREMENTS

Precise measurements in general, but not always, automatically rescale the timebase to expand signal edges for maximum resolution. This technique provides maximum accuracy and results that are independent of the initial sweep speed setting.

When a precise time interval measurement is made the instrument will first perform a coarse calculation to locate the edge(s) of interest. Next, for each edge, the display window will be positioned so that the edge of interest is at center screen and the sweep speed is increased causing the signal to be expanded on the horizontal axis. The instrument will continue to do this until one of three conditions is met: (1) The slope of the signal is 45 degrees or less. (2) The sweep speed equals 500 ps/div (maximum resolution). (3) Signal jitter at the current sweep speed makes it pointless to increase the sweep speed further. At each faster sweep speed a calculation is made to determine of any of these conditions are met. If so, expansion is stopped and the edge crossing time is determined.

If the sweep speed is 500 ps/div or faster or if the measurement requires only a single edge that already has less than 45 degrees slope as displayed, a precise measurement will revert to a coarse measurement.

LOCATING THE EDGE

The edges are measured at the point where the waveform edge crosses the voltage level. For the time interval measurements the level is defined by the voltage markers. For the parameter measurements, the level is defined by the measurement at 10%, 50%, or 90% level on the waveform relative to the top and base.

The measurement routine uses a dual threshold technique. The upper threshold id defined to be 2 A/D values above the level and the lower threshold is defined to be 2 A/D values below the level.

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In terms of the screen, the threshold region is one minor division wide in the full screen mode and half a minor division in the split screen mode. The advantage of this technique is that edges can be determined accurately in the presence of a limited amount of noise.

The edge is determined by performing a linear regression (curve fit) on the points that fall inside the threshold region plus the first point below the threshold region and the first point above the threshold region. The edge crossing is defined as the point where the line generated by the linear regression crosses the level. In many cases, there are no points inside the threshold region and the linear regression becomes a linear interpolation between the two points above and below the threshold region. (e.g., nearly perpendicular edges).

A limitation of this technique is that there are cases which may result in the edge not being found, notably very small signals and measurements made near the top of waveforms.

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