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Errata

Title & Document Type:

Manual Part Number:

Revision Date:

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

We've added this manual to the Agilent website in an effort to help you support your product. This manual provides the best information we could find. It may be incomplete or contain dated information, and the scan quality may not be ideal. If we find a better copy in the future, we will add it to the Agilent website.

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Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

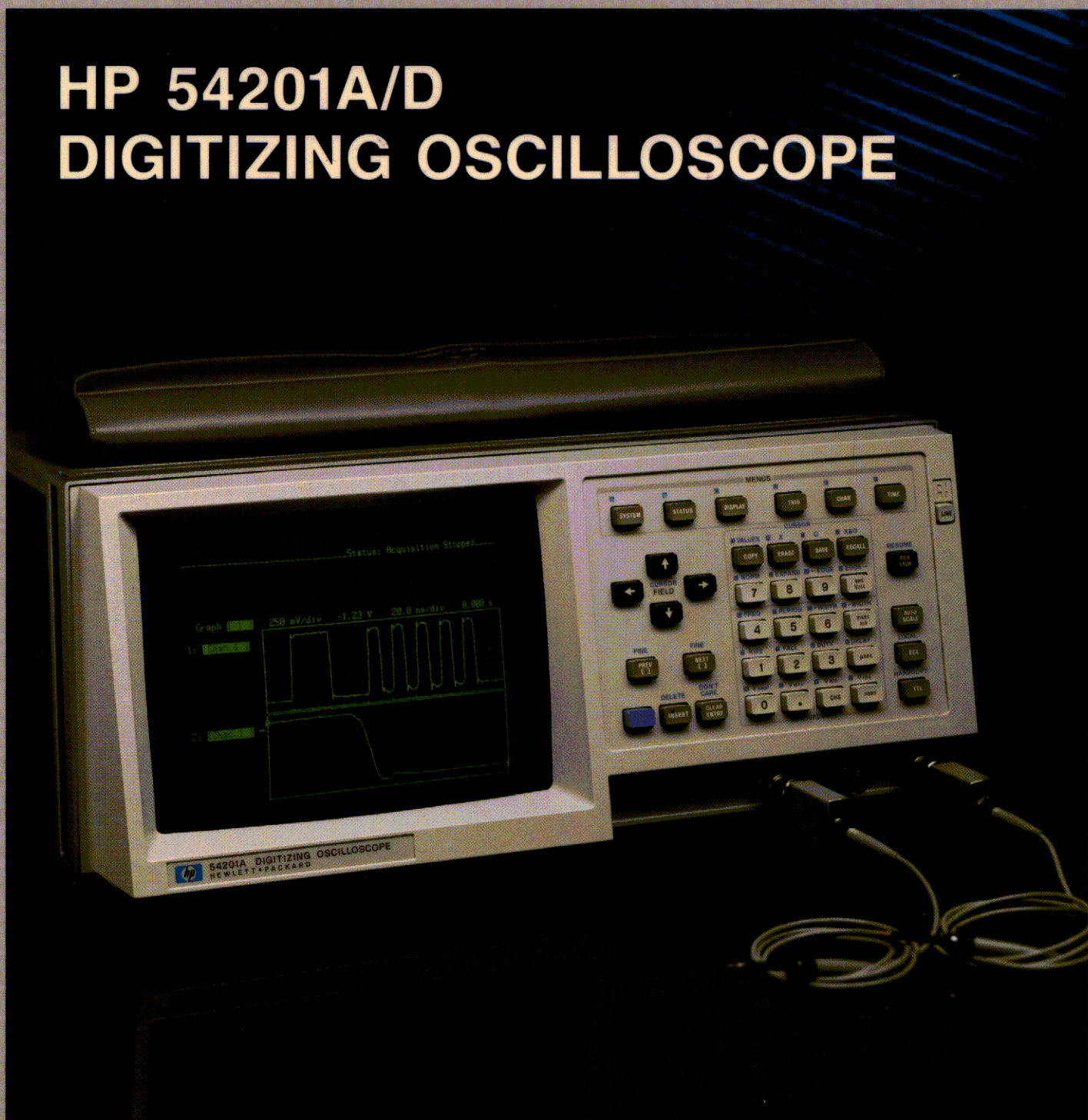
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SERVICE MANUAL

HP 54201A/D
DIGITIZING OSCILLOSCOPE



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SERVICE MANUAL

HP 54201A/D
DIGITIZING OSCILLOSCOPE

SERIAL NUMBERS

This manual applies directly to instruments with serial number prefixes:

HP 54201A; 2602A
HP 54201D; 2602A

For additional important information about serial numbers, see INSTRUMENTS COVERED BY MANUAL in Section I.

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Manual Part No. 54201-90902
Microfiche Part No. 54201-90802

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SAFETY CONSIDERATIONS

GENERAL - This is a Safety Class I instrument (provided with terminal for protective earthing).

OPERATION - BEFORE APPLYING POWER verify that the power transformer primary is matched to the available line voltage, the correct fuse is installed, and Safety Precautions are taken (see the following warnings). In addition, note the instrument's external markings which are described under "Safety Symbols."

WARNING

- Servicing instructions are for use by service-trained personnel. To avoid dangerous electric shock, do not perform any servicing unless qualified to do so.
- BEFORE SWITCHING ON THE INSTRUMENT, the protective earth terminal of the instrument must be connected to the protective conductor of the (mains) powercord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. The protective action must not be negated by the use of an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- If this instrument is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the power source.
- Any interruption of the protective (grounding) conductor (inside or outside the instrument) or disconnecting the protective earth terminal will cause a potential shock hazard that could result in personal injury.
- Whenever it is likely that the protection has been impaired, the instrument must be made inoperative and be secured against any unintended operation.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short circuited fuseholders. To do so could cause a shock or fire hazard.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Adjustments described in the manual are performed with power supplied to the instrument while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
- Any adjustment, maintenance, and repair of the opened instrument under voltage should be avoided as much as possible, and when inevitable, should be carried out only by a skilled person who is aware of the hazard involved.
- Capacitors inside the instrument may still be charged even if the instrument has been disconnected from its source of supply.

SAFETY SYMBOLS



Instruction manual symbol. The product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the product.



Indicates hazardous voltages.



Earth terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in personal injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood or met.

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SECTION 1
GENERAL INFORMATION

WARNING

Service information included in this manual is for use of trained service personnel. To avoid electrical shock, do not perform any service procedures in the manual or do any servicing to the HP 54201A/D unless you are qualified.

1-1. INTRODUCTION

This manual contains technical information concerning the installation, performance testing, adjustments, and servicing of the HP 54201A and HP 54201D Digitizing Oscilloscopes. When information concerns both models the system will be referred to as the HP 54201A/D.

1-2. MANUAL ORGANIZATION

Section 1, General Information. This section contains a description of this manual and the instrument. This section also gives the specifications, general characteristics, operating characteristics and recommended test equipment for the HP 54201A/D.

Section 2, Installation. This section explains how to prepare the HP 54201A/D for use.

Section 3, Performance Tests. This section describes both the self test capabilities of the HP 54201A/D as well as the procedures for the full Performance Test.

Section 4, Adjustments. The HP 54201A/D requires several adjustments to restore specified performance after some major repairs have been made. This section provides the necessary adjustment procedures.

Section 5, Replaceable Parts. This section contains ordering information and a list of all replaceable parts in the HP 54201A/D system.

Section 6, Service. This section contains disassembly and assembly procedures and documentation and procedures for isolation and replacement of faulty circuit boards.

Service Group 6A, Power Supply. This section contains block diagrams and component level theory, troubleshooting and schematic information necessary to service the HP 54201A/D power supply.

Appendix A, Self Test Documentation. This section contains an overview of how the HP 54201A/D self tests work and what portions of the HP 54201A/D circuitry they check.

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1-3. INSTRUMENTS COVERED BY THIS MANUAL

Attached to the instrument is a serial number sticker. The serial number is in the form 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix and the last five digits are the suffix. The prefix is the same for all identical HP 54201A or HP 54201D instruments; the prefix only changes when a change is made to the instrument. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual applies to instruments with serial number prefix(es) listed under SERIAL NUMBERS on the title page. The serial number is also displayed on the HP 54201A/D screen when the SYSTEM Peripherals menu is selected.

An instrument manufactured after the printing of this manual may have a serial number prefix not listed on the title page. This unlisted serial prefix indicates the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a yellow Manual Changes supplement. The supplement contains "change information" that explains how to adapt the manual to the newer instrument.

In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement is identified by the manual print date and part number, both of which appear on the manual title page. Complimentary copies of this supplement are available on request.

Shown on the title page is a microfiche part number. This number can be used to order 4 X 6 inch microfilm transparencies of this manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

1-4. DESCRIPTION

The HP 54201A and HP 54201D Digitizing Oscilloscopes are dedicated, two-channel, simultaneous, waveform acquiring digital storage oscilloscopes with full HP-IB programmability, digitized waveform data output, and resident parametric waveform measurements.

The HP 54201A/D is a general purpose digitizing oscilloscope with 300 MHz repetitive bandwidth and a single-shot digital storage bandwidth of 50 MHz (200 megasamples/second) with infinite store time and waveform data output. It also provides parametric information about the analog characteristics of waveforms.

The HP 54201D has all the features of the HP 54201A with the addition of parallel and serial logic trigger qualification capabilities. The HP 54201D includes 3 pods, each containing 8 bit + 1 parity bit + clock organization.

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The key features of the HP 54201A/D Digitizing Oscilloscopes are:

- 300 MHz repetitive bandwidth with ±200 ps time-interval accuracy.
- 200 megasamples/second sample rate, 50 MHz single-shot bandwidth using post capture data interpolation.
- Capture two channels simultaneously.
- Holdoff-by-events to trigger acquisition after a specified number of events.
- Pre-trigger viewing.
- All front panel controllable parameters can be programmed via HP-IB.
- Continuously updated automatic waveform parameter measurements with user-defined thresholds.
- Waveform math: Ch1+Ch2 and Ch1-Ch2.
- Set up aids such as automatic waverform scaling, ECL/TTL preset levels, and save/recall of front-panel setups.
- One button hardcopy to HP-IB printers and plotters.
- Digital logic trigger qualification (HP 54201D only).

1-5. ACCESSORIES SUPPLIED

The following accessories are supplied with the instruments:

HP 54201A/D: Two HP 10017A 10:1 divider probes.
One BNC to probe tip adapter.
One 2.3 meter (7.5 ft) power cord.
One Operating and Programming Manual.
One Service Manual.

HP 54201D (only): Three HP 10271A 10-bit State Data Probes.

1-6. SPECIFICATIONS

Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested.

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Table 1-1. Specifications

HP 54201A and HP 54201D [1,2]

VERTICAL (CHANNEL 1 AND 2)

Range: 40 mV to 16 V full-scale, calibrated with two digit resolution.

Gain Accuracy: ±2% of full-scale. [3]

Analog to Digital Conversion (ADC) Accuracy: ±1.6% of full-scale.

Dc Offset Accuracy:

Channel Range	Offset Accuracy
40 mV to 790 mV	±1% of offset ±5 mV
800 mV to 16 V	±1% of offset ±100 mV

Dc Offset Range/Resolution:

Channel Range	Offset Range	Offset Resolution
40 mV to 790 mV	±1.5 V	1 mV
800 mV to 16 V	±30 V	20 mV

Voltage Measurement Accuracy (DC):

Single Cursor (X or O): Gain Accuracy + ADC Accuracy + Offset Accuracy

Dual Cursor (X to O measurements on the same waveform): Gain Accuracy + 2 * (ADC Accuracy)

Bandwidth (-3 dB):

Coupling	Real Time Sampling	Repetitive Sampling
Dc	Dc to 50 MHz	Dc to 300 MHz
Ac	10 Hz to 50 MHz	10 Hz to 300 MHz

Transition Time (10% to 90%):
(Calculated from: Bandwidth X Transition Time = 0.35)
Real Time Sampling: 7 ns
Repetitive Sampling: 1.2 ns

Input Coupling: ac or dc.

Input RC (Nominal): 1 MΩ shunted by approximately 10 pF (ac or dc)
50Ω dc

Input Operating Range (dc + peak ac): ±1 vertical range from center.

Maximum Safe Input Voltage: 1 MΩ ac or dc: ±40 V (dc + peak ac)
50Ω dc: 5 Vrms or ±40 V (dc + peak ac), whichever is less

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Table 1-1. Specifications (continued)

TIME BASE (HORIZONTAL)

Range (10 divisions, in a 1-2-5 sequence): Real Time Sampling: 50 ns to 10 s full-scale
Repetitive Sampling: 10 ns to 20 μs full-scale

Time Base Accuracy (Single and Dual Cursors):
Real time: ±2 ns or ±0.2% of time range, whichever is greater. [4]
Repetitive Sampling: ±200 ps or ±0.2% of time range, whichever is greater. [4]

DELAY (TIME OFFSET)

Pre-Trigger Range:

Sampling Mode	Time Range	Pre-Trigger Range
Real Time	50 ns to 5 μs	Up to 10 μs
	10 μs to 10 s	Up to 2 screen diameters
Repetitive	10 ns to 20 μs	Up to 2 screen diameters

Post-Trigger Range: At least 200 screen diameters.

Pre/Post-Trigger Resolution: Adjustable in steps of 0.1 (coarse) and 0.001 (fine) screen diameters, or the least significant digit, whichever is greater.

TRIGGER (ANALOG)

Sources: Channel 1, channel 2, or External trigger input.

	Channel 1, Channel 2	External Trigger
Level Accuracy: (full scale)	±3% ±5 mV (40 mV to 790 mV) ±3% ±100 mV (800 mV to 16 V)	±3% ±30 mV
Sensitivity:	1/8 of full scale (dc to 250 MHz)	100 mV_{P-P} (dc to 250 MHz, 50Ω coupled) 1 V_{P-P} (dc to 100 MHz, .2 MΩ [5] coupled)
Range:	1.5 times full scale	±2 V
Resolution:	0.02 times full scale	20 mV

External Trigger Input:

Input Coupling: Dc

Input Resistance: 50Ω or .2 MΩ [5]

Maximum Safe Input Voltage: .2 MΩ dc: ±40 V (dc + peak ac)
50Ω dc: 5 Vrms or ±40 V (dc + peak ac), whichever is less

Input Operating Range: ±5 V (dc + peak ac)

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Table 1-1. Specifications (continued)

HP 54201D (only)

STATE TRIGGER MODE

Clock Repetition Rate:

Single Phase: 25 MHz maximum with single clock and single edge specified; 20 MHz maximum with any ORed combination of clocks and edges.

Multiplexed: Master-slave clock timing; master clock must follow slave clock by at least 10 ns and precede next slave clock by 50 ns or more.

Minimum Clock Pulse Width: 20 ns at threshold.

Minimum Setup Time: 20 ns, the time data must be present prior to the clock transition.

Minimum Hold Time: 0 seconds, the time data must be present after the clock transition.

HP 10271A STATE PROBES

Input RC: 100 kΩ ±2% shunted by approximately 5 pF at the probe body.

Minimum Input: 600 mV p-p.

Minimum Input Overdrive: 250 mV or 30% of input amplitude whichever is greater.

Maximum Safe Input: ±40 V peak.

Threshold Range: -9.9 V to +9.9 V in 100 mV increments.

Threshold Accuracy: ±2.5% ±120 mV.

Dynamic Range: ±10 V about threshold.

Notes

1. Specifications apply after a 30 minute warm up period.
2. Real-time reconstruction uncertainty ±1 ns (applies to time ranges of 50 ns to 2 μs).
3. Specifications apply within ±10° C of Auto-calibration temperature.
4. Dual cursor specifications apply for measurements made on the same or simultaneously acquired waveforms.
5. Provides 10:1, 1 MΩ input at HP 10017A or HP 10018A probe tip.

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1-7. GENERAL CHARACTERISTICS

Table 1-2 lists general characteristics, not specifications, but typical characteristics included as additional information for the user.

Table 1-2. General Characteristics

REAR-PANEL BNC OUTPUTS

One output BNC is located on the rear panel with TTL output levels. High is ≥2 V into 50Ω; low is ≤0.4 V into 50Ω. This output maybe programmed from the front panel or remotely via HP-IB to provide the following output waveforms:

HP 54201A and HP 54201D

- Constant low
- Constant high
- 2.000 kHz probe compensation source
  (If used without 50Ω dc coupling, falling edge must be used for compensation)
- High on trigger
- High on frame complete
- High on acquisition complete

HP 54201D only

- Pulse on state sequence true
- High on state sequence true
- Pulse on state master clock

POWER REQUIREMENTS

Voltage: 115/230 Vac, -22% to +10%; 48 to 66 Hz.

Power: 275 W maximum.

ENVIRONMENTAL CONDITIONS

Temperature: Operating: 0 to +55°C (+32 to +131°F).
Non-operating: -40 to +75°C (-40 to +167°F).

Humidity: Operating: Up to 90% relative humidity at +40°C (non-condensing).

Non-operating: Up to 95% relative humidity at +65°C.

Altitude: Operating: Up to 4600 meters (15 000 feet).
Non-operating: Up to 15 300 meters (50 000 feet).

Vibration: Vibrated in three planes for 15 minutes each with 0.38 mm (0.015 inch) excursions at 5 to 55 Hz.

X-RAY EMISSION: Less than 0.05 mr/hr measured with Victorean Model 440RF/C.

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Table 1-2. General Characteristics (Continued)

WEIGHT

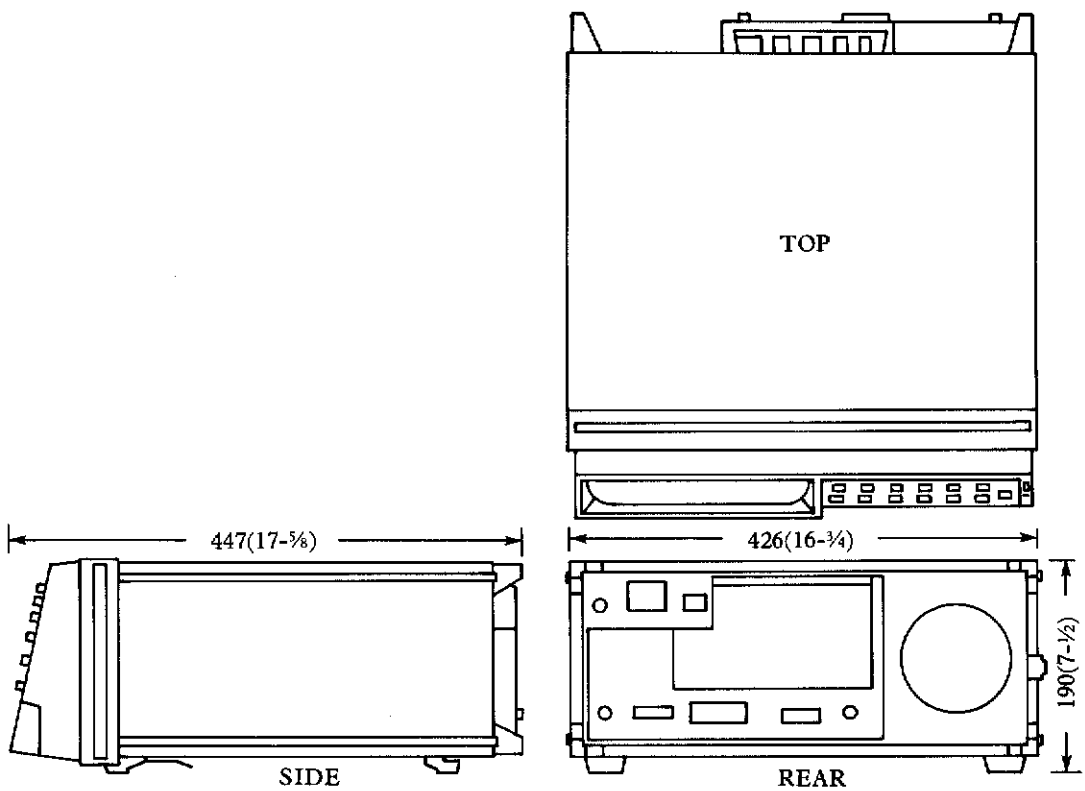
HP 54201A: net 11.4 kg (25 lbs); shipping 15.9 kg (35 lbs).
HP 54201D: net 12.7 kg (28 lbs); shipping 21.8 kg (38 lbs).

DIMENSIONS

Notes:

1. Dimensions are for general information only. If dimensions are required for building special enclosures, contact your HP field engineer.

2. Dimensions are in millimetres and (inches).



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1-8. OPERATING CHARACTERISTICS

Table 1-3 lists the Operating Characteristics, a summary of the HP 54201A/D operating capabilities.

Table 1-3. Operating Characteristics

HP 54201A and HP 54201D

DIGITIZER

Digitizing Technique:

Real-Time Digitizing: all data points are acquired on a single acquisition.

Random Repetitive Digitizing: data points are acquired on multiple acquisitions.

Digitizing Rate: 100 samples/second to 200 megasamples/second (determined by the time base range setting and acquisition mode).

Resolution: 6 bits; 1 part in 64; effective resolution may be increased up to 7 bits by using data filtering and averaging.

Acquisition Record Length: 1001 samples (1000 intervals).

CHANNEL 1 and 2 INPUTS (VERTICAL)

Probe Factors: 1:1, 2:1, 5:1, 10:1, 20:1, 50:1, or 100:1 probe attenuation factors may be entered to scale the voltages as seen by the probe tips.

Channel Isolation: 50 dB from dc to 50 MHz
40 dB from 50 MHz to 300 MHz
with channels set to equal voltage ranges

TIMEBASE (HORIZONTAL)

Expand Mode: X and O cursors can be used to window an area of interest and expand it to full screen.

Reference Location: The reference point can be positioned at the left edge, center, or right edge of the display. The reference point is that point where the time is offset from the trigger point by the delay time.

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Table 1-3. Operating Characteristics (Continued)

TRIGGER (ANALOG)

Level Range:

Centered Mode: Trigger level tracks the offset level of the internal trigger source selected (tracks either channel 1 or 2).

Adjust Mode: Trigger level may be adjusted independently of the offset level, when an internal trigger source has been selected.

Edge: Positive or negative slope may be selected for any source.

Holdoff-by-events: Range of events counter is from 1 to 59999 events. Maximum counting rate is 50 MHz. An event is defined as anything that satisfies the triggering conditions selected.

DISPLAY

Data Display Formats: One, two or four waveforms can be displayed at the same time. They can be live waveforms (Channel 1 or Channel 2) or stored waveforms (from waveform memories 0, 1, 2, or 3) in any combination.

Display/Store Modes:

Normal: The display is repetitively updated with each new waveform acquisition.

Accumulate: All successive waveform acquisitions are displayed until erased. Erasure modes are manual, slow (after 64 acquisitions) and fast (after 16 acquisitions).

Envelope: Provides a display of the running maximum and minimum voltage at each sample point for a repetitive input waveform.

Average: Provides a display of the average voltage at each sample point for 4, 16, 64, or 256 user defined waveform acquisitions. On each acquisition, 1/n times the new data is added to (n-1)/n of the previous value at each time coordinate. Operates in a continuous mode.

Connect-the-dots: Provides a display of the sample points connected by straight lines.

Reference Lines: Two horizontal reference lines may be defined and displayed for each graph. Reference lines may be positioned in terms of voltage or percent of waveform amplitude. When making automatic measurements, these lines indicate the upper and lower measurement thresholds.

Graticules: Full grid or frame with tic marks.

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Table 1-3. Operating Characteristics (Continued)

MEASUREMENT AIDS

Automatic Measurements: The following waveform measurements can be performed automatically on real-time or stored waveforms. The standard measurement thresholds are the 10%, 50%, and 90% points of the waveform. In the User Defined mode; voltages, percentages, or ECL and TTL presets may be used to define the upper and lower thresholds. Measurements are continuously updated with each new acquisition.

Frequency	Duty Cycle
Period	Delay (average, max, min, and last)
Positive Pulse Width	Vamplitude
Negative Pulse Width	Vmaximum
Rise Time	Vminimum
Fall Time	Vrms

Waveform Math: Waveform subtraction (channel 1 − channel 2) and waveform addition (channel 1 + channel 2) may be selected as an acquisition mode.

Cursors: Two cursors (X and O) are provided for making voltage and time measurements on displayed waveforms. Both absolute and differntial values are provided. Dual cursor measurements can be made between two points on the same waveform or between two points on different waveforms.

Waveform Memories: Four memories are provided for waveform storage. All memories are non- volatile. Labels may be assigned to each memory.

SETUP AIDS

Auto-Scale: Pressing the Auto-Scale key sets the vertical and horizontal ranges, offset level, and trigger level to display the input signals. Period, + pulse, - pulse, rising edge, or falling edge may be selected as the horizontal display criteria. Requires a duty cycle of >1%, frequency >50 Hz, and amplitude >20 mV peak. Vertical, horizontal, and trigger auto scaling functions may be selectively enabled or disabled.

Presets: Scales the vertical range, offset and trigger level to predetermined values for displaying ECL or TTL waveforms.

Setup Memories: Four front panel setups (0 through 3) may be saved in non-volatile memory. Labels may be assigned to each setup.

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Table 1-3. Operating Characteristics (Continued)

PROGRAMMABILITY

All instrument settings and operating modes including automatic waveform measurements may be remotely programmed via HP-IB (IEEE-488). HP-IB programming complies with the recommendations of IEEE Std. 728-1982, "Recommended Practice for Code and Format Conventions".

HARDCOPY OUTPUT

The CRT display, including menus, can be transferred directly to HP-GL compatible digital plotters and HP-IB raster graphics printers. The peripheral used must have listen-only mode.

HP 54201D (Only)

STATE TRIGGER MODES[1]

State Only: Triggers waveform acquisition immediately after the state sequence specification has been fulfilled.

State Arms Analog: Arms the analog trigger when the state sequence specification has been fulfilled.

ASSIGNMENT

State Modes:

Normal: State patterns up to 27 channels wide may be defined as trigger qualification. Up to four unique state patterns can be qualified on in a user defined sequence.

Qualified: State sequence search does not begin until after the qualify clock has occurred. The slave clock is defined as the qualify clock.

Missing Bit: Predefines the last state in the sequence specification to detect a missing bit in a string of serial data and triggers the acquisition.

Extra Bit: Predefines the last state in the sequence specification to detect an extra bit in a string of serial data and triggers the acquisition.

Clocks: Three ORed clocks operate in a single-phase or two-phase demultiplexing mode. Clock edge is selectable as positive, negative, or both edges for each clock. Different edge selections may be made on the same clock if it is used in each phase of the multiplexed mode.

Labeling: Up to eight different five-character labels may be designated for any combination of input lines for ease in setting specifications.

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HP 54201A/D - General Information

Table 1-3. Operating Characteristics (Continued)

SEQUENCE

Resources: Four user-defined terms (a,b,c, and d) plus the "not equal" of these terms (≠a, ≠b, ≠c, ≠d), Any State, or No State may be used in any combination. A term is the AND combination of bit patterns in each label. Each term can be the combination of up to eight user defined labels. Terms may be used as often as desired.

Trigger: Up to four resource terms may be used in any sequence to establish the state trigger specification. The last term in the sequence may use up to four resource terms in an ORed or ANDed format.

Occurrence: Occurrence of the last event in the sequence may be specified up to n = 59999.

Restart: One to four resource terms may be used in an ORed condition for a sequence restart condition.

Notes

1. State Trigger Modes use HP 10271A probes for state inputs.

1-9. RECOMMENDED TEST EQUIPMENT

Table 1-4 lists the equipment required to adjust, performance test, and troubleshoot the HP 54201A/D. Other equipment may be substituted if it meets or exceeds the critical specifications given in table 1-4.

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Table 1-4. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL	USE*
Signature Multimeter	HP-IB controllable, with DVM Range: -50 V to +50 V DC Accuracy: 0.5%	HP 5005B	A,T
Pulse Generator	Dual channel Repetition rate: 100 MHz Transition time: 1.3 ns, variable Amplitude: 5 volts Basic timing accuracy: ≤3%	HP 8161A Opt 020	P,A
Signal Generator	Frequency: 100 kHz to 300 MHz Output Level Accuracy: ±1 dB	HP 8656B	P
Power Meter	Accuracy: ±3% to 300 MHz (must match power sensor used)	HP 436A	P
Power Sensor	———	HP 8482A	P
Power Splitter	50Ω	HP 11667A	P
Dc Power Supply	Range: ±100 mV to ±5 V Accuracy: ±0.1%	HP 6114A	P
Blocking capacitor	0.18 μF, 200V	HP 10240B	P
50Ω Terminator	Accuracy: ≤1%	HP 10100C	P,A
Product Support Kit	No Substitute	HP Part No. 54200-69501	P,A,T
Resistive Divider Kit	100:1 resistive divider	HP 10020A	A
Adapter	BNC(f)-to-Dual banana	HP Part No. 1251-2277	P
Adapter	Type N(m)-to-BNC(f)	HP Part No. 1250-1476	P
Adapter	Type N(m)-to-BNC(m)	HP Part No. 1250-0082	P
Adapter	BNC(f)-to-BNC(f)	HP Part No. 1250-0080	P,A
BNC Tee (Qty 2)	1 male, 2 female	HP Part No. 1250-0781	P,A
BNC Cable (Qty 2)	9-inch	HP 10502A	P,A
BNC Cable (Qty 4)	48-inch	HP 10503A	P,A
Type N(m) Cable	24-inch	HP 11500B	P

* P=Performance Testing, A=Adjustments, T=Troubleshooting

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SECTION 2
INSTALLATION

2-1. INTRODUCTION

This section contains the initial operation information for the HP 54201A/D. Included are power and grounding requirements, operating environment requirements, cleaning methods and storage and shipment requirements.

2-2. PREPARATION FOR USE

2-3. Power Requirements

The HP 54201A/D requires a power source of either 115 or 230 VAC -22% to +10%; single phase, 48 to 66 Hz; 275 watts maximum.

CAUTION

The instrument may be damaged if the Line Voltage Select Switch is not properly set to match the input voltage.

2-4. Line Voltage Selection

Before turning ON the instrument verify that the Line Voltage Select Switch on the rear panel matches the input line voltage. The 6 Amp fuse installed satisfies both voltage settings of 115 and 230 VAC.

2-5. Power Cable

This instrument is equipped with a three-wire power cable. When connected to an appropriate AC power outlet, this cable grounds the instrument cabinet. The type of power cable plug shipped with the instrument depends on the country of destination. See figure 2-1 for option numbers of power cables and plug configurations available. Part numbers for each cable option are listed in the replaceable parts section of this manual.

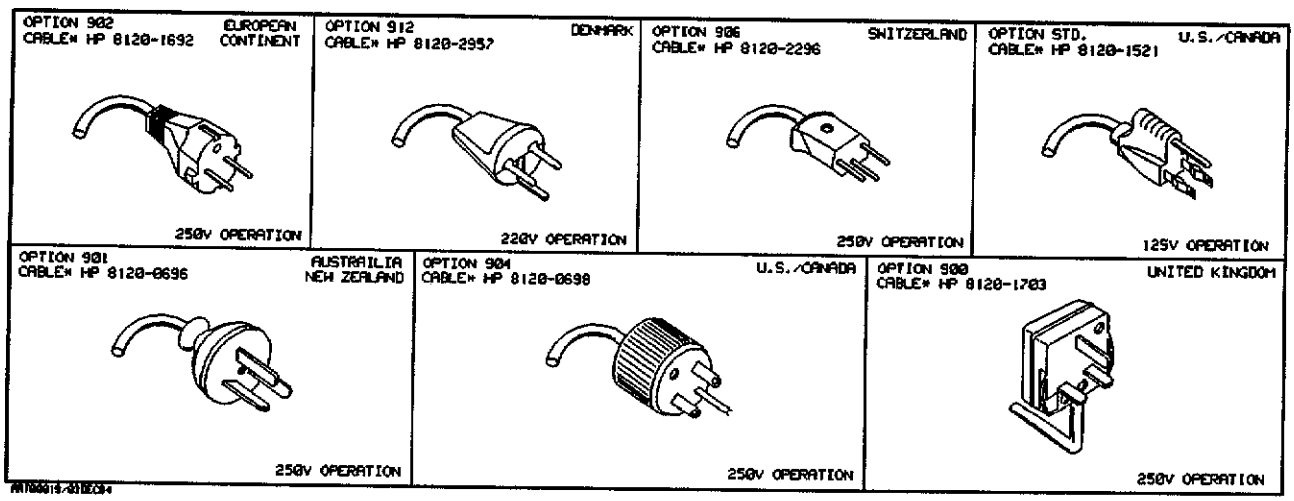


Figure 2-1. Power Cord Configurations

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2-6. OPERATING ENVIRONMENT

The operating environment is noted in table 1-2. Note should be made of the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Protection should be provided against internal condensation.

The HP 54201A/D will operate to all specifications, within the temperature and humidity range given in table 1-2. However, reliability is enhanced by operating the instrument within the following ranges.

Recommended Temperature: +20 to +35° C (+68 to +95° F)
Recommended Humidity: 20% to 80% non-condensing

High temperature/humidity combinations should be avoided.

2-7. CLEANING REQUIREMENTS

When cleaning the HP 54201A/D, CAUTION must be exercised on which cleaning agents are used. USE MILD SOAP AND WATER. If a harsh soap or solvent is used, the water-base paint finish WILL BE damaged.

CAUTION

BE CAREFUL when cleaning the keyboard. Water can damage the keyboard circuitry if it seeps under the keys.

2-8. STORAGE AND SHIPMENT

2-9. Environment

The instrument may be stored or shipped in environments within the following limits:

Temperature: ..... -40° C to +75° C
Humidity: ..... Up to 90% at 65° C
Altitude: ..... Up to 15 300 metres (50 000 Feet)

The instrument should also be protected from temperature extremes which cause condensation within the instrument. Condensation within the instrument may cause malfunction if the instrument is operated under these conditions.

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2-10. Packaging

2-11. TAGGING FOR SERVICE. If the instrument is to be shipped to a Hewlett-Packard office for service or repair, attach a tag showing owner (with address), complete instrument serial number, and a description of the service required.

2-12. ORIGINAL PACKAGING. If the original packing material is not available or is unserviceable, material identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is to be shipped to a Hewlett-Packard office for servicing, attach a tag showing owner (with address), model number, complete instrument serial number, and a description of the service required. Mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and serial number.

2-13. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials.

a. Wrap instrument in heavy paper or plastic.

b. Use a strong shipping container. A double-wall carton made of 350 lb. test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside the container. Protect control panel with cardboard.

d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

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SECTION 3
PERFORMANCE TESTS

3-1. INTRODUCTION

This section describes the HP 54201A/D Self Tests and Performance Test Procedures. The Self Tests, resident in ROM, are a series of tests that confirm proper function of the mainframe hardware and firmware. While the Self Tests provide the user with a confidence level of greater than 90%, it does not verify the critical specifications given in table 1-1 of Section 1. The Performance Tests test for complete instrument compliance to these critical specifications.

3-2. EQUIPMENT REQUIRED

The only equipment required for the Self Test is a standard BNC cable, 1 meter in length. The equipment required to perform the Performance Tests is listed in table 3-1. Other equipment may be substituted if it meets or exceeds the critical specifications listed in table 3-1.

3-3. TEST RECORD

Results of performance tests may be tabulated on the Performance Test Record (table 3-2) at the end of this section. The Test Record lists all of the tested specifications and their acceptable limits. The results recorded at incoming inspection can be used for comparison in periodic maintenance and troubleshooting and after repairs or adjustments.

Note

Allow instrument to warm up for at least 30 minutes prior to beginning performance tests.

3-4. RECOMMENDED TEST EQUIPMENT

Table 3-1 lists the equipment required to performance test the HP 54201A/D. Other equipment may be substituted if it meets or exceeds the critical specifications given in table 3-1.

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Table 3-1. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Pulse Generator	Dual channel Repetition rate: 100 MHz Transition time: 1.3 ns, variable Amplitude: 5 volts Basic timing accuracy: ≤3%	HP 8161A Opt 020
Signal Generator	Frequency: 100 kHZ to 300 MHz Output level accuracy: ±1 dB	HP 8656B
Power Meter	Accuracy: ±3% to 300 MHz (must match power sensor used)	HP 436A
Power Sensor	———	HP 8482A
Power Splitter	50Ω, dc to 300 MHz	HP 11667A
Dc Power Supply	Range: ±100 mV to ±5 V Accuracy: ±0.1%	HP 6114A
Blocking capacitor	0.18 μF, 200V	HP 10240B
50Ω Terminator	Accuracy: ≤1%	HP 10100C
Product Support Kit	No Substitute	HP Part No. 54200-69501
Adapter	BNC(f)-to-Dual banana	HP Part No. 1251-2277
Adapter	Type N(m)-to-BNC(f)	HP Part No. 1250-1476
Adapter	Type N(m)-to-BNC(m)	HP Part No. 1250-0082
Adapter	BNC(f)-to-BNC(f)	HP Part No. 1250-0080
BNC Tee (Qty 2)	1 male, 2 female	HP Part No. 1250-0781
BNC Cable (Qty 2)	9-inch	HP 10502A
BNC Cable (Qty 4)	48-inch	HP 10503A
Type N(m) Cable	24-inch	HP 11500B

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3-5. SELF TEST FUNCTIONAL VERIFICATION

The Self Tests, resident in ROM, are a series of tests that confirm proper function of the mainframe hardware and firmware. While the Self Tests provide the user with a confidence level of greater than 90%, they do not verify the critical specifications given in table 1-1 of Section 1. Perform the Performance Tests for complete instrument compliance to these critical specifications.

To execute the self tests, press the SYSTEM menu key, then press the NEXT/PREV key until the Test & Service menu is displayed as shown below. Using the Field arrow keys, move the blinking cursor to the Execute Selftest field. Enter either 0, 1, or 2 and follow the instructions displayed on screen. An audible beep will be heard when each self test has been completed.

A failure of a self test should be followed by resident SYSTEM menu calibration routines 0, 5, and 6 (in this order). The self tests should then be re-selected to check whether the self-calibration routines corrected the error. Repeated failure of a self-test, or failure of a self-calibration routine may dictate the need of a particular hardware adjustment.

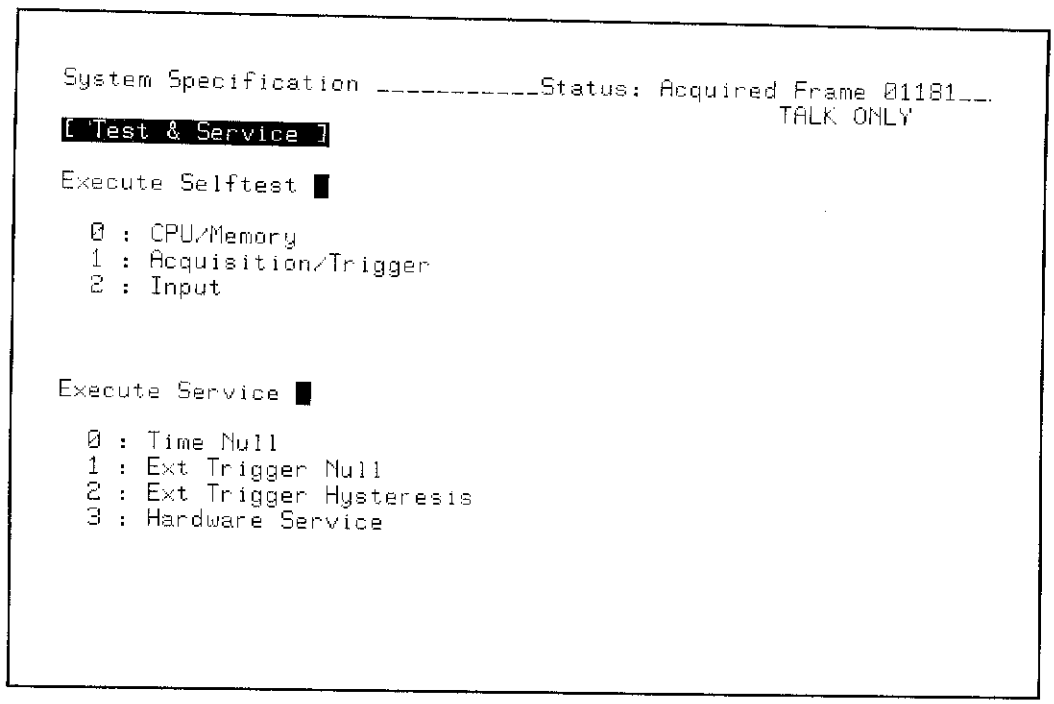


Figure 3-1. SYSTEM Self Tests Menu

PERFORMANCE TESTS

After the instrument has warmed up at least 30 minutes, perform a key-down power-up reset. This will preset the HP 54201A/D to a predetermined condition and clear the display memory. Hold any front panel key down while applying power to the instrument. Hold the key down long enough for the power-up tune to be completed.

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PERFORMANCE TESTS

3-6. DC OFFSET ACCURACY TEST

Specification:

Channel Range	Offset Accuracy
40 mV to 790 mV	±1% of offset ±5 mV
800 mV to 16 V	±1% of offset ±100 mV

Equipment Required:

DC Supply ..... HP 6114A
BNC(f)-to-Dual Banana Adapter ..... HP Part No. 1251-2277

Procedure:

1. Configure STATUS Configuration menu as shown in figure 3-2.
2. Connect the output of the DC Supply to Channel 1 input of the HP 54201A/D.
3. Apply +1.00 V from DC Supply to Channel 1 input.
4. Press the DISPLAY menu key and select one graph with Channel 1 displayed.
5. The display should appear similar to figure 3-3.
6. Select the V_{min} and V_{max} measurements for Channel 1 on the HP 54201A/D. The limits are 0.98 V and 1.02 V.
7. Apply -1.00 V from the DC Supply to Channel 1 input.
8. Set HP 54201A/D Channel 1 offset to -1.00 V.
9. The limits of V_{min} and V_{max} for Channel 1 are -0.98 V and -1.02 V.
10. Set HP 54201A/D Channel 1 voltage range to 800 mV.
11. The limits of V_{min} and V_{max} for Channel 1 are -0.89 V and -1.11 V.
12. Apply +1.00 V from the DC Supply to Channel 1 input.
13. Set HP 54201A/D Channel 1 offset to +1.00 V.
14. Limits of V_{min} and V_{max} for Channel 1 are 0.89 V and 1.11 V.
15. Repeat steps 3 through 14 substituting Channel 2 for Channel 1.

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PERFORMANCE TESTS

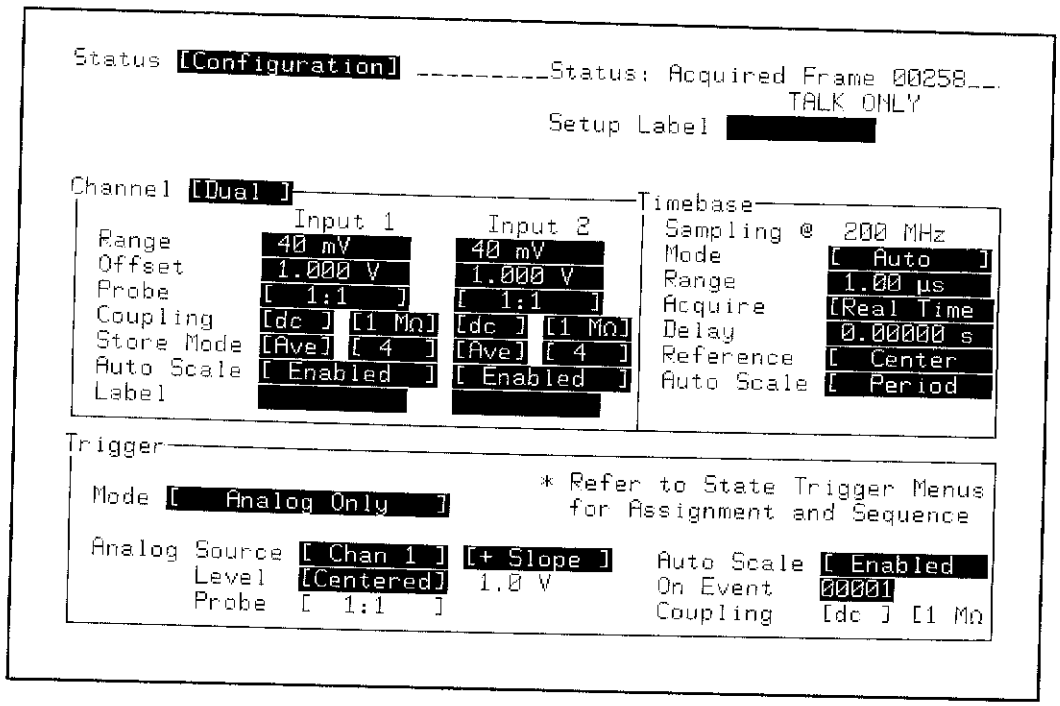


Figure 3-2. STATUS Configuration Menu

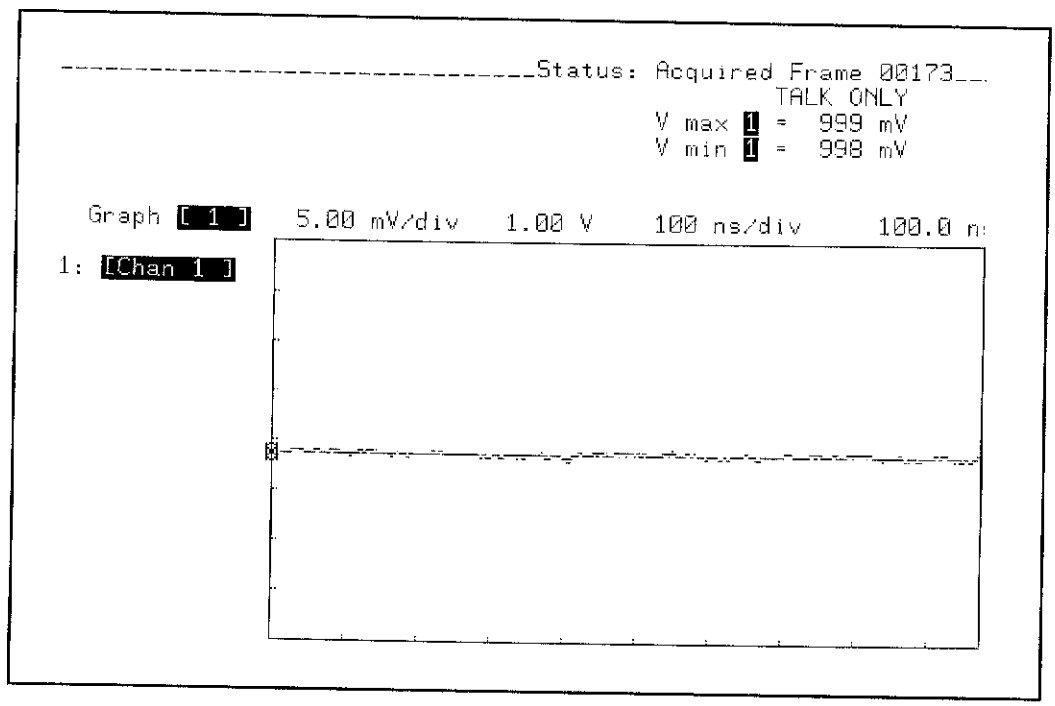


Figure 3-3. DISPLAY Waveform

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PERFORMANCE TESTS

3-7. VOLTAGE MEASUREMENT ACCURACY TEST
Single Cursor (X or O)

Specification:

Gain Accuracy	+ ADC Accuracy	+ Offset Accuracy
= (±2% of full scale)	+ (±1.6% of full scale)	+ (±1% of offset ±5 mV) 40 mV to 790 mV range (±1% of offset ±100 mV) 800 mV to 16 V range

Equipment Required:

DC Supply ..... HP 6114A
BNC(f)-to-Dual Banana Adapter ..... HP Part No. 1251-2277

Procedure:

1. Configure STATUS Configuration menu as shown in figure 3-4.
2. Connect the output of the DC Supply to Channel 1 input of the HP 54201A/D.
3. Apply +100 mV from DC Supply to Channel 1 input.
4. Press the DISPLAY menu key and select one graph with Channel 1 displayed.
5. The display should appear similar to figure 3-5.
6. Display the cursor values by pressing the VALUES key on the 54201A/D. The limits of Vx are 84 mV to 116 mV.
7. Apply -100 mV from DC supply to Channel 1 input.
8. Limits of Vx are -84 mV to -116 mV.
9. Apply -5.00 V from DC Supply to Channel 1 input.
10. Set HP 54201A/D Channel 1 voltage range to 16 V.
11. Limits of Vx are -4.32 V to -5.68 V.
12. Apply +5.00 V from DC Supply to Channel 1 input.
13. Limits of Vx are 4.32 V to 5.68 V.
14. Repeat steps 2 through 13 substituting Channel 2 for Channel 1.

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PERFORMANCE TESTS

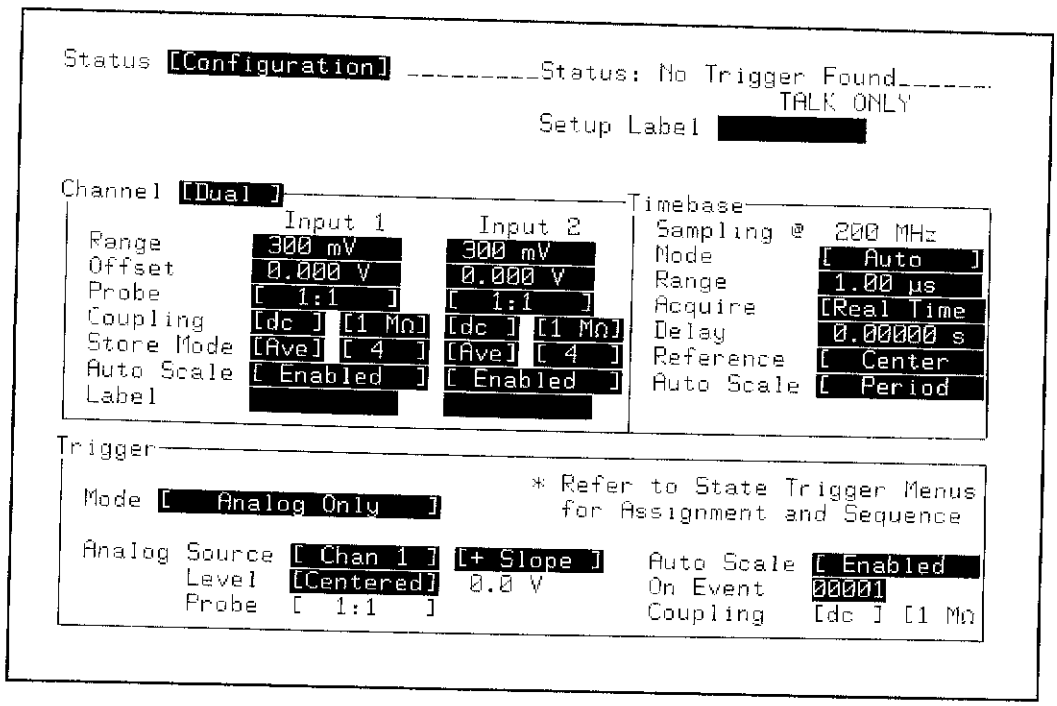


Figure 3-4. STATUS Configuration Menu

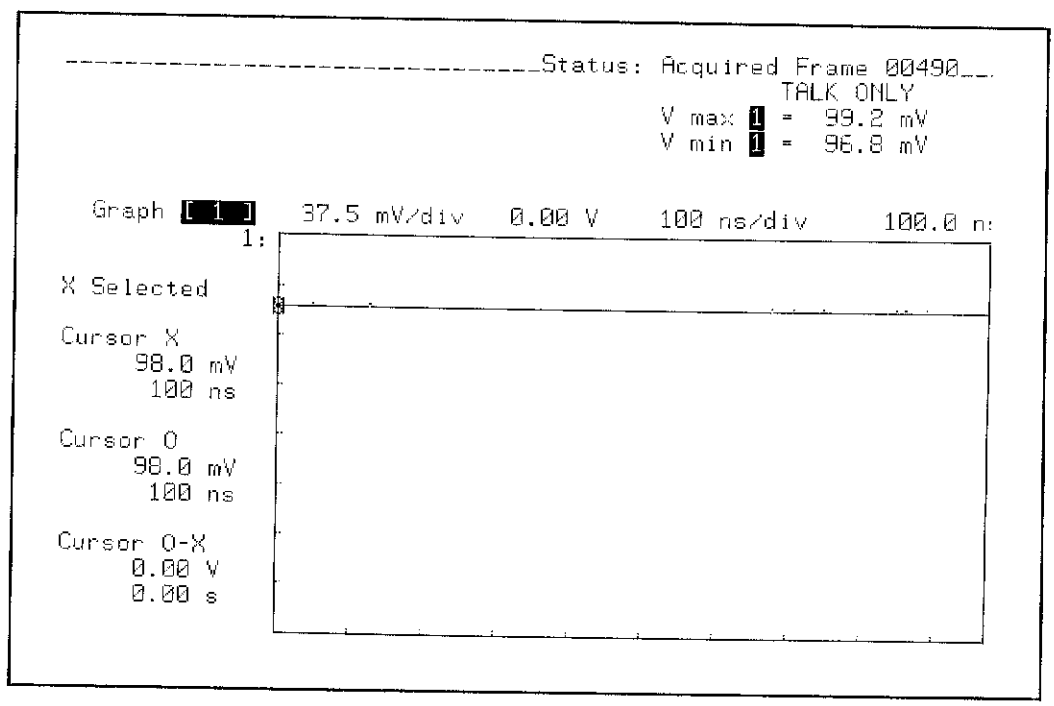


Figure 3-5. DISPLAY Waveform

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PERFORMANCE TESTS

3-8. BANDWIDTH (-3dB) TEST

Specification:

Coupling	Real Time Sampling	Repetitive Sampling
Dc	Dc to 50 MHz	Dc to 300 MHz
Ac	10 Hz to 50 MHz	10 Hz to 300 MHz

Equipment Required:

Signal Generator ..... HP 8656B
Power Meter ..... HP 436A
Power Sensor ..... HP 8482A
50Ω Power Splitter ..... HP 11667A
Type N(m) Cable, 24-inch ..... HP 11500B
Type N(m)-to-BNC(m) Adapter ..... HP Part No. 1250-0082

Note

Ensure that Power Meter has been zeroed and calibrated to match Power Sensor.

Procedure:

Real Time

1. Configure STATUS Configuration menu as shown in figure 3-6.
2. Configure test equipment as shown in figure 3-7.
3. Set Signal Generator sinewave output to 200 kHz, 0.5 V amplitude.
4. Set Power Meter Cal Factor % to 200 kHz value from cal chart, then press dB[REF] to set a 0 dB reference.
5. Put the HP 54201A/D O cursor on maximum peak of displayed waveform and put X cursor on minimum peak of displayed waveform. Record this Vo-x voltage number.
6. Change frequency of Signal Generator to 50 MHz and change Cal Factor % on Power Meter to the 50 MHz value from cal chart.
7. Change Timebase Range of HP 54201A/D to 200 ns Real Time.
8. Put O cursor on maximum peak of waveform and X cursor on minimum peak of waveform.
9. Adjust amplitude of Signal Generator so that Vo-x has same reading as the number recorded in step 5. Step 8 may need to be repeated to keep the cursors at the waveform peaks. The Power Meter reading must be ≤3 dB.
10. Repeat steps 1 through 9 for Channel 2, specifying Channel 2 as the trigger source.

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PERFORMANCE TESTS

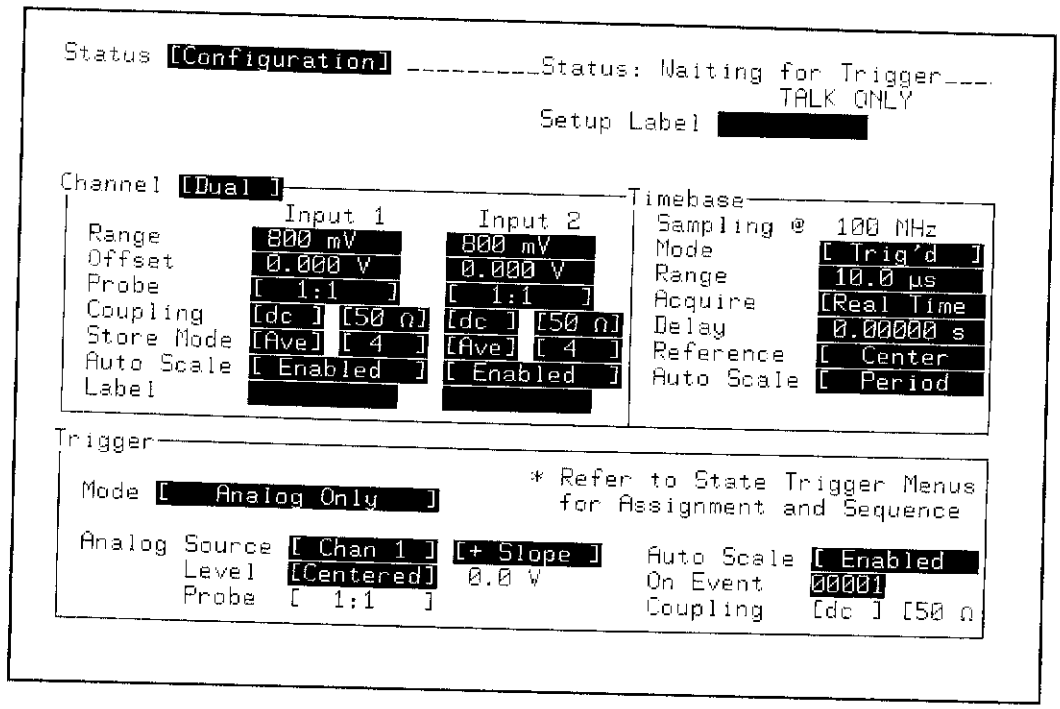


Figure 3-6. STATUS Configuration Menu

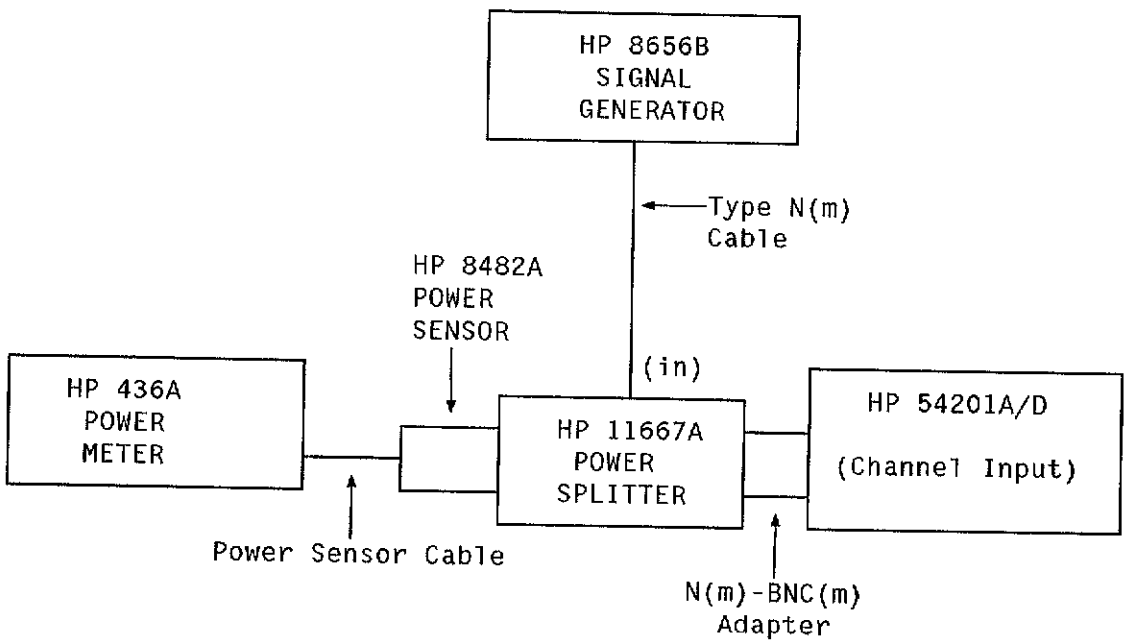


Figure 3-7. Bandwidth Test Connections.

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PERFORMANCE TESTS

Repetitive

11. Change frequency of Signal Generator to 200 kHz, 0.5 V amplitude.

12. Change Timebase Range of HP 54201A/D to 10 μs Repetitive mode.

13. Set Power Meter Cal Factor % to 200 kHz value from cal chart, then press dB[REF] to set a 0 dB reference.

14. Put the HP 54201A/D O cursor on maximum peak of displayed waveform and put X cursor on minimum peak of displayed waveform. Record this Vo-x voltage number.

15. Change frequency of Signal Generator to 300 MHz and change Cal Factor % on Power Meter to the 300 MHz value from cal chart.

16. Change Timebase Range of HP 54201A/D to 10 ns.

17. Put O cursor on maximum peak of waveform and X cursor on minimum peak of waveform.

18. Adjust amplitude of Signal Generator so that Vo-x has same reading as the number recorded in step 14. Step 17 may need to be repeated to keep the cursors at the waveform peaks. The Power Meter reading must be $\leq$3 dB.

19. Repeat steps 11 through 18 for Channel 1, specifying Channel 1 as the trigger source.

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PERFORMANCE TESTS

3-9. TIME MEASUREMENT ACCURACY TEST (DUAL CURSORS)

Specification: Real Time Sampling: ±2 ns or ±0.2% of time range, whichever is greater.
Repetitive Sampling: ±200 ps or ±0.2% of time range, whichever is greater.

Equipment Required:

Signal Generator ..... HP 8656B
Type N(m)-to-BNC(f) Adapter ..... HP Part No. 1250-1476

Procedure:

1. Set the output of Signal Generator to 2.5 MHz, 500 mV amplitude.
2. Configure STATUS Configuration menu as shown in figure 3-8.
3. Connect a BNC cable from the RF output of the Signal Generator to Channel 1 input of the HP 54201A/D.
4. Press the VALUES key to display cursor values.
5. Position the X cursor approximately halfway up the first rising slope, and position the O cursor on the second rising slope such that Vo-x is as small a value as possible. The display should appear similar to figure 3-9.
6. Read the Cursor O-X time value on the display. The limits of Cursor O-X time are 398 ns and 402 ns.
7. Change the frequency of the Signal Generator to 250 MHz.
8. Change the 54201A/D time range to 10 ns, and set Data Filter in DISPLAY menu to OFF.
9. Position the X cursor approximately halfway up the first rising slope, and position the O cursor on the second rising slope such that Vo-x is as small a value as possible.
10. Read the Cursor O-X time value on the display. The limits of Cursor O-X time are 3.8 ns and 4.2 ns.

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PERFORMANCE TESTS

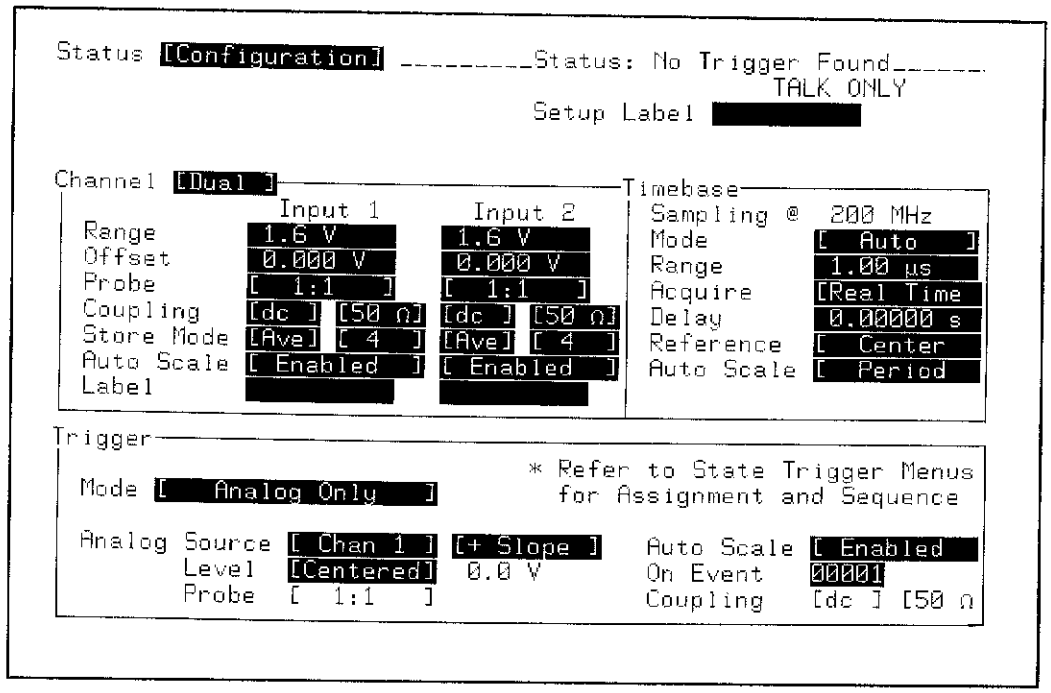


Figure 3-8. STATUS Configuration Menu

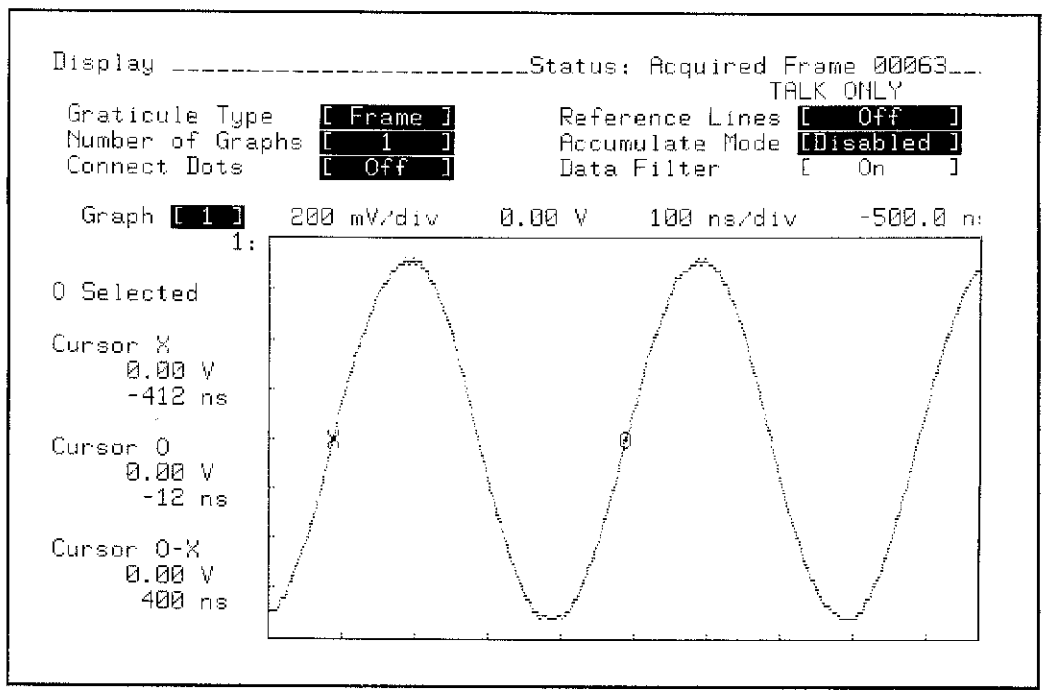


Figure 3-9. DISPLAY Waveform

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PERFORMANCE TESTS

3-10. TRIGGER (ANALOG) LEVEL ACCURACY TEST

Specification: Channel 1, Channel 2 Trigger

±3% of channel range ±5 mV (40 mV to 790 mV channel range)
±3% of channel range ±100 mV (800 mV to 16 V channel range)

Equipment Required:

Pulse Generator	HP 8161A
BNC Tee	HP Part No. 1250-0781
BNC Cable, 9-inch (Qty 2)	HP 10502A
BNC Cable, 48-inch	HP 10503A
BNC(f)-to-BNC(f) Adapter	HP Part No. 1250-0080

Equipment Setup: HP 8161A

Period (PER): 10 µs

	A Output	B Output
Width (WID):	5 µs	5 µs
Leading Edge (LEE):	2.49 µs	2.49 µs
Trailing Edge (TRE):	2.49 µs	2.49 µs
High Level (HIL):	+1.5 V	+1.5 V
Low Level (LOL):	-1.5 V	-1.5 V
Delay (DEL):	0.00 ns	0.00 ns
Output mode:	Enable	Disable

Procedure:

1. Configure STATUS Configuration menu as shown in figure 3-10.
2. Connect a BNC cable from the A output of Pulse Generator to Channel 1 input of HP 54201A/D.
3. Press DISPLAY menu key and select one graph with Channel 1 displayed. The waveform should appear similar to figure 3-11.
4. Move the X cursor to the position where Tx is equal to 0.
5. Limits of Vx are 283 mV and 317 mV.
6. Change HP 54201A/D Channel 1 offset to -300 mV and trigger slope to negative.
7. With the X cursor at the position where Tx = 0, the limits of Vx are -283 mV and -317 mV.
8. Change HP 54201A/D Channel 1 voltage range to 800 mV.
9. With the X cursor at the position where Tx is equal to 0, the limits of Vx are -176 mV and -424 mV.
10. Change HP 54201A/D Channel 1 offset to 300 mV and trigger slope to positive.
11. With the X cursor at the position where Tx = 0, the limits of Vx are 176 mV and 424 mV.
12. Repeat steps 2 through 11 for Channel 2, specifying Channel 2 as the trigger source.

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PERFORMANCE TESTS

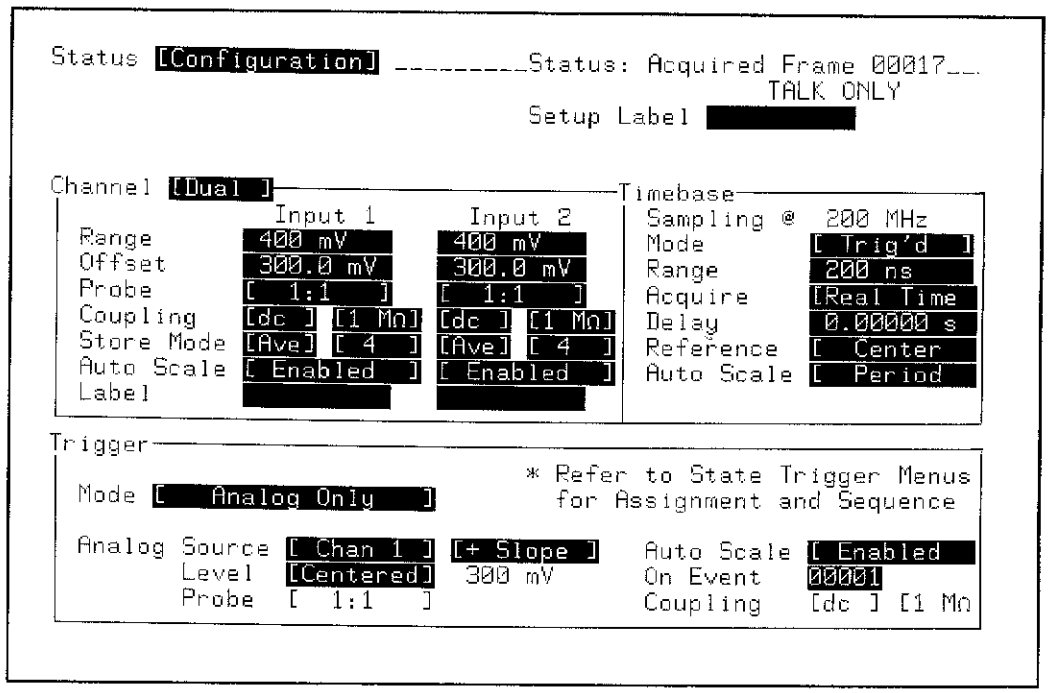


Figure 3-10. STATUS Configuration Menu

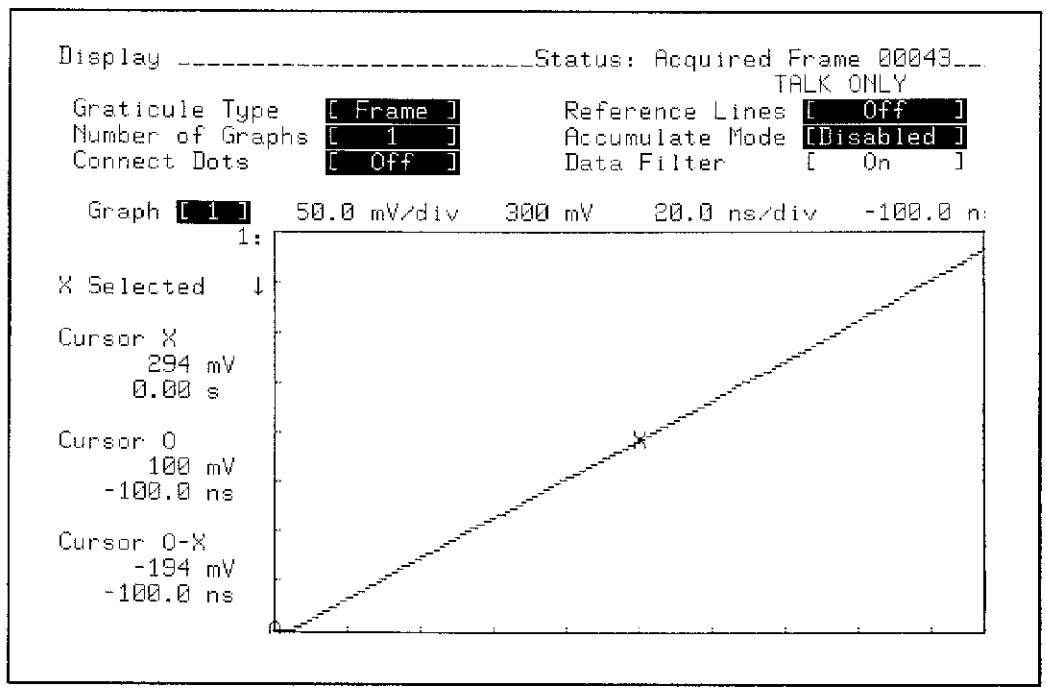


Figure 3-11. DISPLAY Waveform

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PERFORMANCE TESTS

3-11. TRIGGER SENSITIVITY TEST

Specification: Internal: 1/8 of full scale.

External: 100 mVP-P (dc to 250 MHz, 50Ω coupled)
1 VP-P (dc to 100 MHz, .2 MΩ coupled)

Equipment Required:

Pulse Generator	HP 8161A
Signal Generator	HP 8656B
Power Meter	HP 436A
Power Sensor	HP 8482A
Power Splitter	HP 11667A
50Ω Terminator	HP 10100C
BNC Cable, 9-inch	HP 10502A
BNC Cable, 48-inch	HP 10503A
Type N(m)-to-BNC(f) Adapter	HP Part No. 1250-1476
Type N(m)-to-BNC(m) Adapter	HP Part No. 1250-0082
Type N(m) Cable, 24-inch	HP 11500B

Equipment Setup:

HP 8161A

Period (PER): 1 ms

	A Output	B Output
Width (WID):	500 µs	500 µs
Leading Edge (LEE):	249 µs	1 ns
Trailing Edge (TRE):	249 µs	1 ns
High Level (HIL):	+2.5 V	+2.5 V
Low Level (LOL):	-2.5 V	-2.5 V
Delay (DEL):	0.00 ns	0.00 ns
Output mode:	Enable	Disable

Procedure:

Internal Trigger

1. Configure STATUS Configuration menu as shown in figure 3-12.
2. Connect 48-inch BNC cable from the A output of Pulse Generator to Channel 1 input of the HP 54201A/D.
3. Display Channel 1. The triggered waveform should appear similar to figure 3-13.
4. Move the X cursor to the Tx = 0.0 s position.
5. Note the value of Vx.
6. Change the trigger slope to [-slope] and note the value of Vx.

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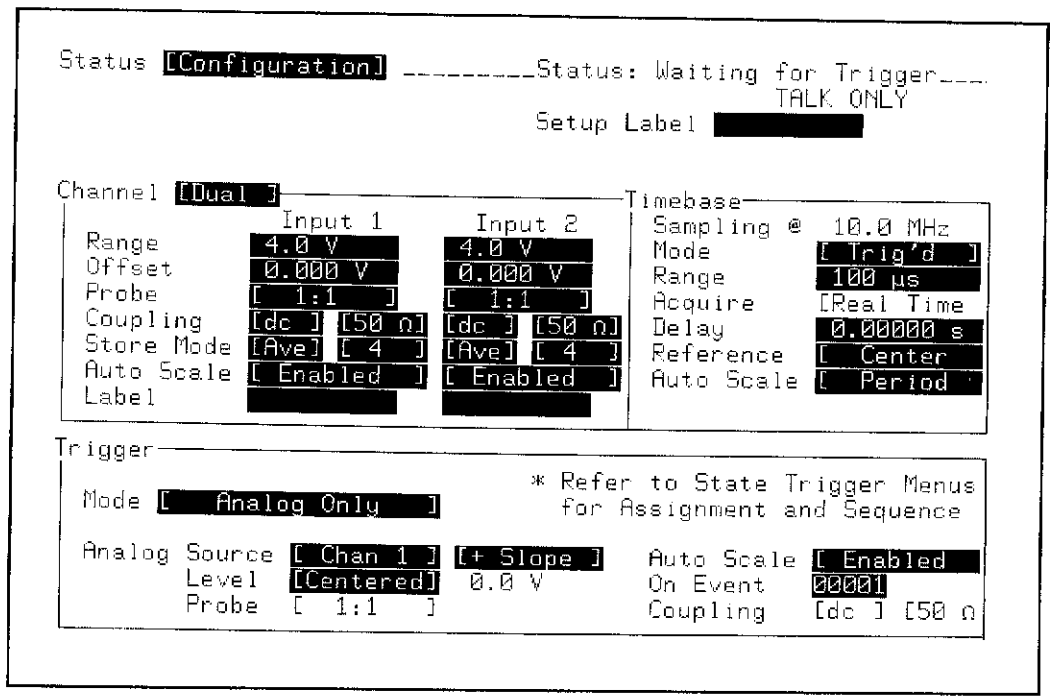


Figure 3-12. STATUS Configuration Menu

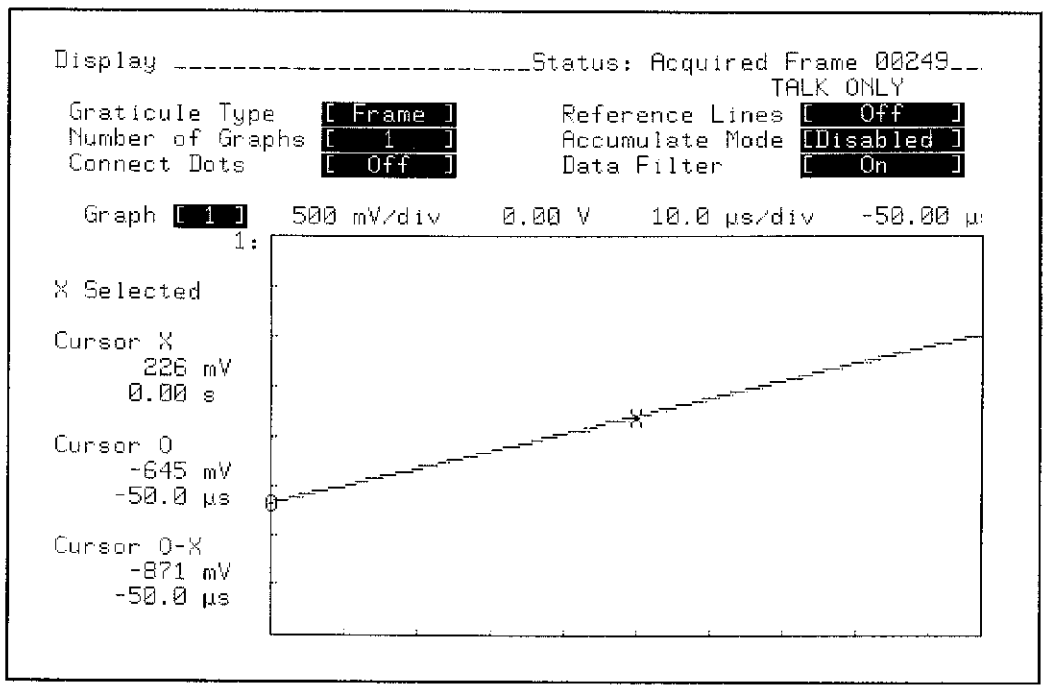


Figure 3-13. DISPLAY Waveform

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PERFORMANCE TESTS

7. The difference in the Vx value { Vx[+slope] minus Vx[-slope] } should be no more than 2V.

8. Repeat steps 1 through 7 for Channel 2, specifying Channel 2 as the trigger source.

9. Disconnect Pulse Generator from HP 54201A/D.

External Trigger

10. Configure STATUS Configuration menu as shown in figure 3-14.

Note

Ensure that Power Meter has been zeroed and calibrated to match Power Sensor.

11. Connect test equipment as shown in figure 3-15, except without the 50Ω terminator.

12. Set Signal Generator sinewave output to 250 MHz, 70 mV amplitude.

13. Set Power Meter Cal Factor % to 250 MHz value from cal chart.

14. Adjust Signal Generator output for a reading of 25 μW on Power Meter (25 μW into 50Ω provides 100 mV_{P-P}).

15. Disconnect Power Sensor from Power Splitter and connect that port of Power Splitter to Channel 1 input of HP 54201A/D using the Type N(m)-to-BNC(f) adapter and the 9-inch BNC cable.

16. Display Channel 1 and verify that a stable sine wave is displayed.

17. Configure STATUS Configuration menu as shown in figure 3-16.

18. Connect test equipment as shown in figure 3-15.

19. Set Signal Generator output to 100 MHz, 700 mV amplitude.

20. Set Power Meter Cal Factor % to 100 MHz value from cal chart.

21. Adjust Signal Generator output for a reading of 2.5 mW on Power Meter (2.5 mW into 50Ω provides 1 V_{P-P}).

22. Repeat steps 15 and 16 to verify triggering.

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PERFORMANCE TESTS

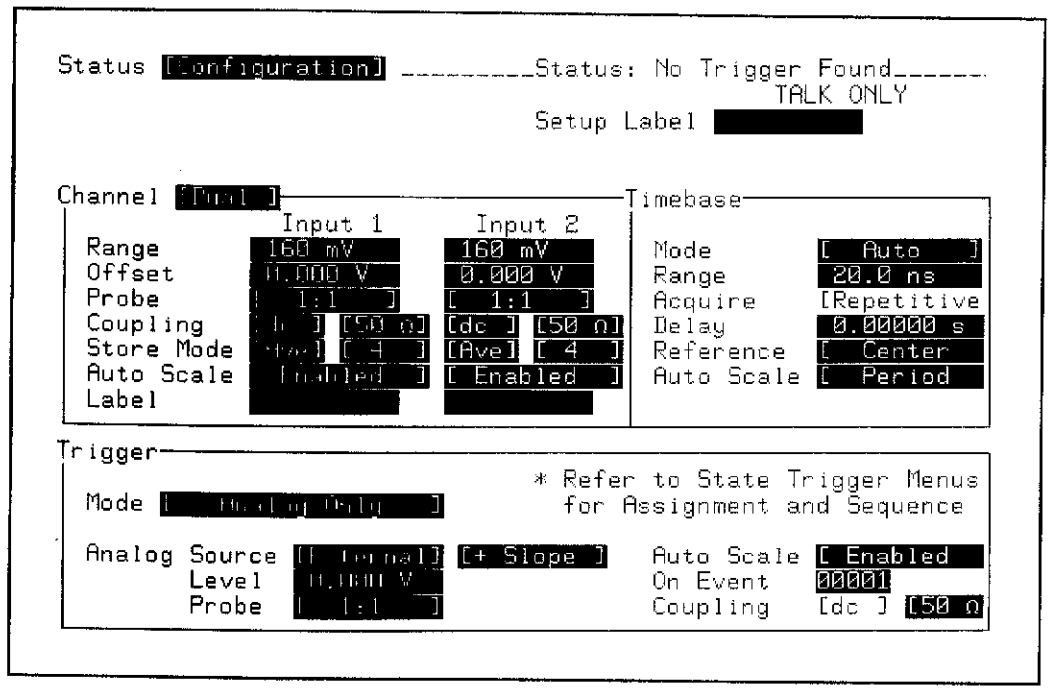


Figure 3-14. STATUS Configuration Menu

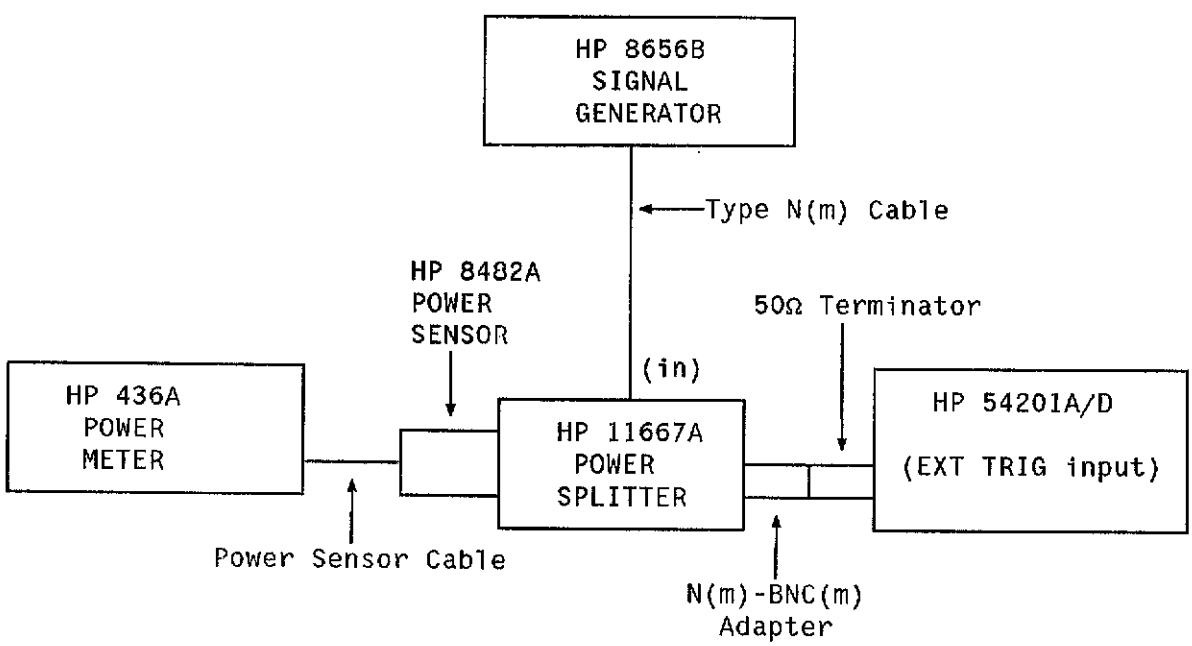


Figure 3-15. External Trigger Sensitivity Test Connections.

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PERFORMANCE TESTS

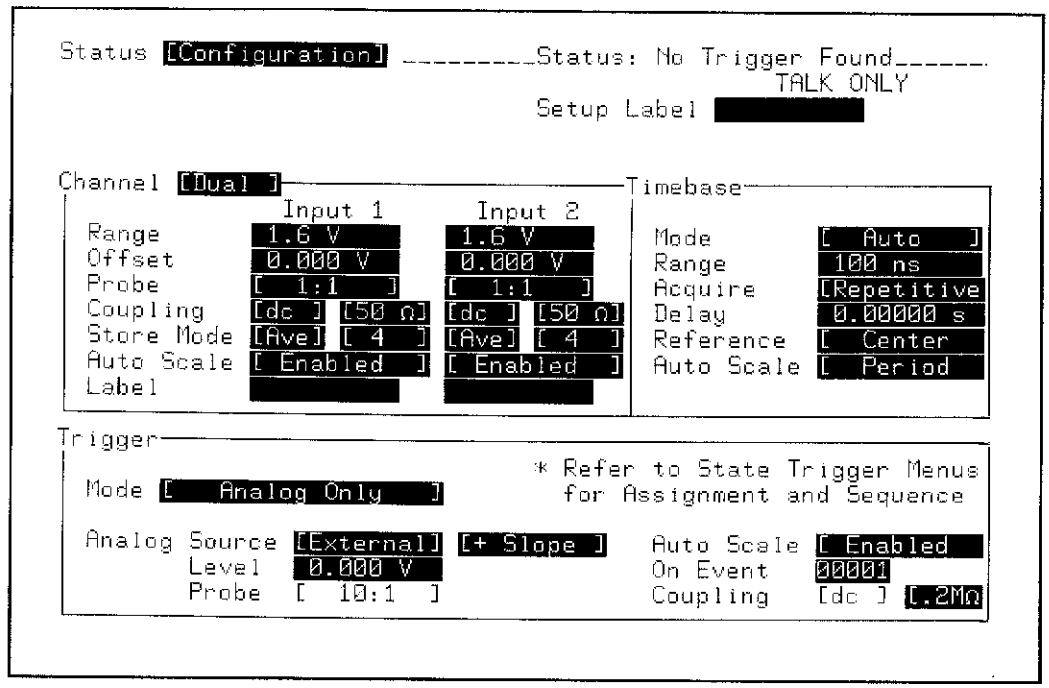


Figure 3-16. STATUS Configuration Menu

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PERFORMANCE TESTS

3-12. MINIMUM SETUP TIME TEST (HP 54201D Only)

Specifications: 20 ns, The time data must be present prior to the clock transition.

Equipment Required:

Pulse Generator ..... HP 8161A Opt. 020
Product Support Kit ..... HP Part No. 54200-69501
BNC Tee (Qty 2) ..... HP Part No. 1250-0781
BNC Cable, 9-inch (Qty 2) ..... HP 10502A
BNC Cable, 48-inch (Qty 3) ..... HP 10503A

Equipment Setup:

HP 8161A

Ext Slope:	Pos	
Period (PER):	200 ns	
	A Output	B Output
Width (WID):	100 ns	50 ns
Leading Edge (LEE):	1.3 ns	1.3 ns
Trailing Edge (TRE):	1.3 ns	1.3 ns
High Level (HIL):	+4 V	+4 V
Low Level (LOL):	0 V	0 V
Delay (DEL):	75 ns	0.00 ns
Output mode:	Enable	Enable

Procedure:

1. Configure the STATUS Configuration menu as shown in figure 3-17.

2. Configure the STATUS Measurement menu as shown in figure 3-18.

3. In the SYSTEM Peripherals menu select Rear Panel BNC: [Pulse On State Sequence True].

4. Configure the TRIGGER State / Define [Assignment] menu as shown in figure 3-19. Use the INSERT key to insert new line for POD1 and POD2.

5. Configure the TRIGGER State / Define [Sequence] menu as shown in figure 3-20.

6. Connect POD 0 to the State Board Test fixture, HP Part No 54200-63801 (part of Product Support Kit).

7. Connect a BNC tee to the BNC labeled "CLOCK" on the State Board Test fixture.

8. Connect a BNC cable from the "B" output of the pulse generator to the "CLOCK" BNC tee, and a short BNC cable from the "CLOCK" BNC tee to the Channel 2 input of the HP 54201D.

9. Connect a BNC tee to the BNC labeled "DATA" on the State Board Test fixture.

10. Connect a BNC cable from the "A" output of the pulse generator to the "DATA" BNC tee, and a short BNC cable from the "DATA" BNC tee to the Channel 1 input of the HP 54201D.

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PERFORMANCE TESTS

11. Connect a BNC cable from the rear panel BNC of the HP 54201D to the front panel EXT TRIG input of the HP 54201D.

12. Configure the display as shown in figure 3-21. Observe the waveforms displayed. They should appear similar to those shown in figure 3-21. If not, repeat steps 1 through 11.

13. Exchange the BNC cables connected to Channel 2 and External Trigger inputs. The display should appear similar to figure 3-22.

14. While observing the pulses displayed on Channel 2, increment the pulse generator output "A" delay in 1 ns steps until the pulses on Channel 2 display disappear.

15. Now decrement the delay in 1 ns steps until the pulses reappear on that channel.

16. Exchange the BNC cables conencted to Channel 2 and External Trigger inputs. The display should appear similar to figure 3-21.

17. Select the DELAY measurement on the HP 54201D and set to "Delay 1 to 2". The DELAY measurement should read ≤20 ns.

18. Change the output "A" delay of the pulse generator to 75 ns.

19. Reconfigure the TRIGGER State/Define [Sequence] menu in figure 3-20 with "Occurrences of [b]".

20. Connect POD 1 to the State Board Test fixture and repeat steps 12 through 17 for POD 1.

21. Change the output "A" delay of the pulse generator to 75 ns.

22. Reconfigure the TRIGGER State/Define [Sequence] menu in figure 3-20 with "Occurrences of [c]".

23. Connect POD 2 to the State Board Test fixture and repeat steps 12 through 17 for POD 2.

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PERFORMANCE TESTS

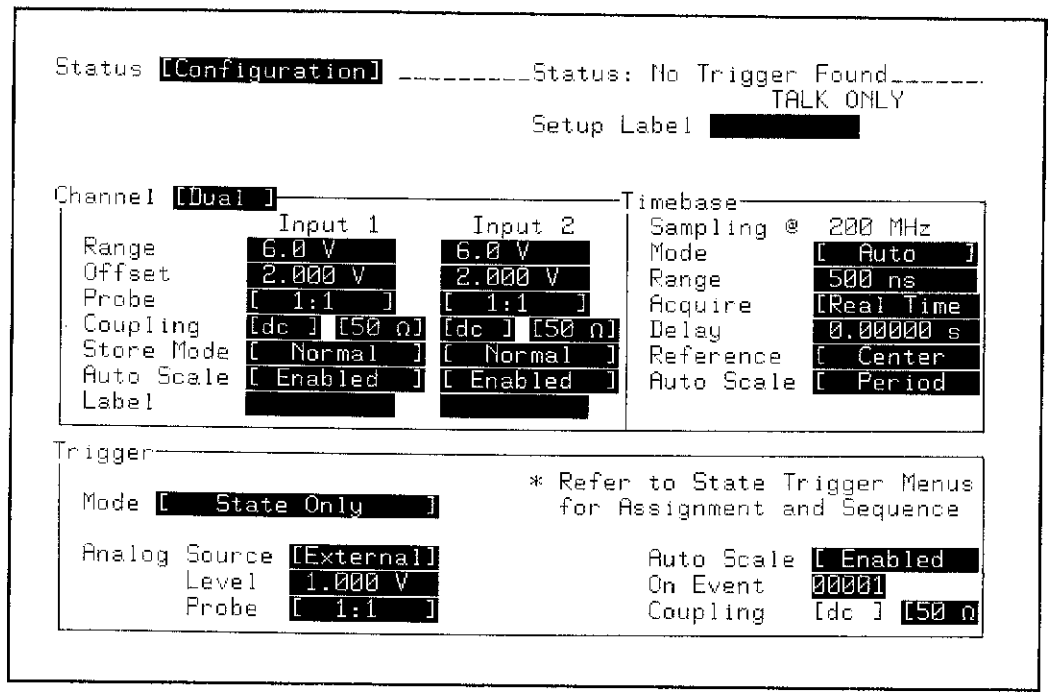


Figure 3-17. STATUS Configuration Menu

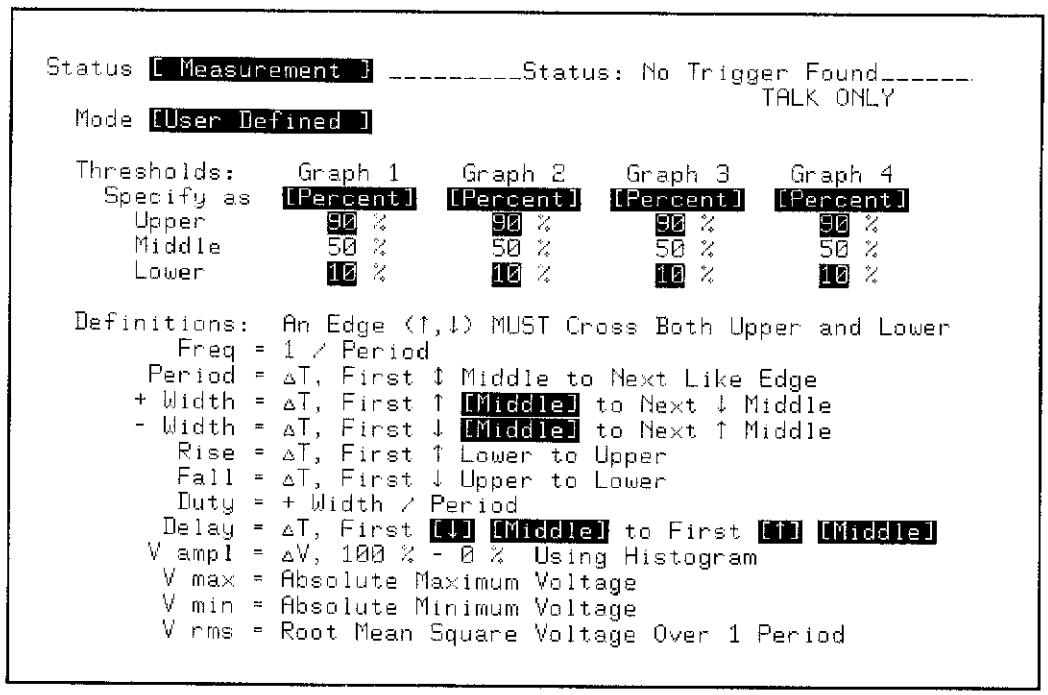


Figure 3-18. STATUS Measurement Menu

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PERFORMANCE TESTS

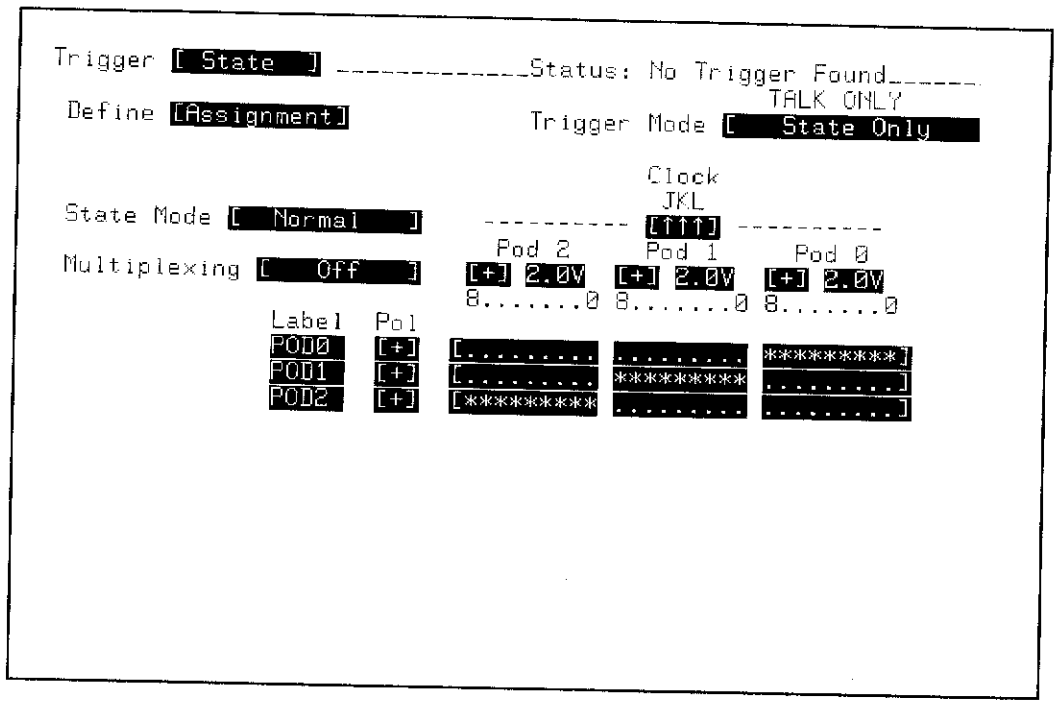


Figure 3-19. TRIGGER State / Define [Assignment] Menu

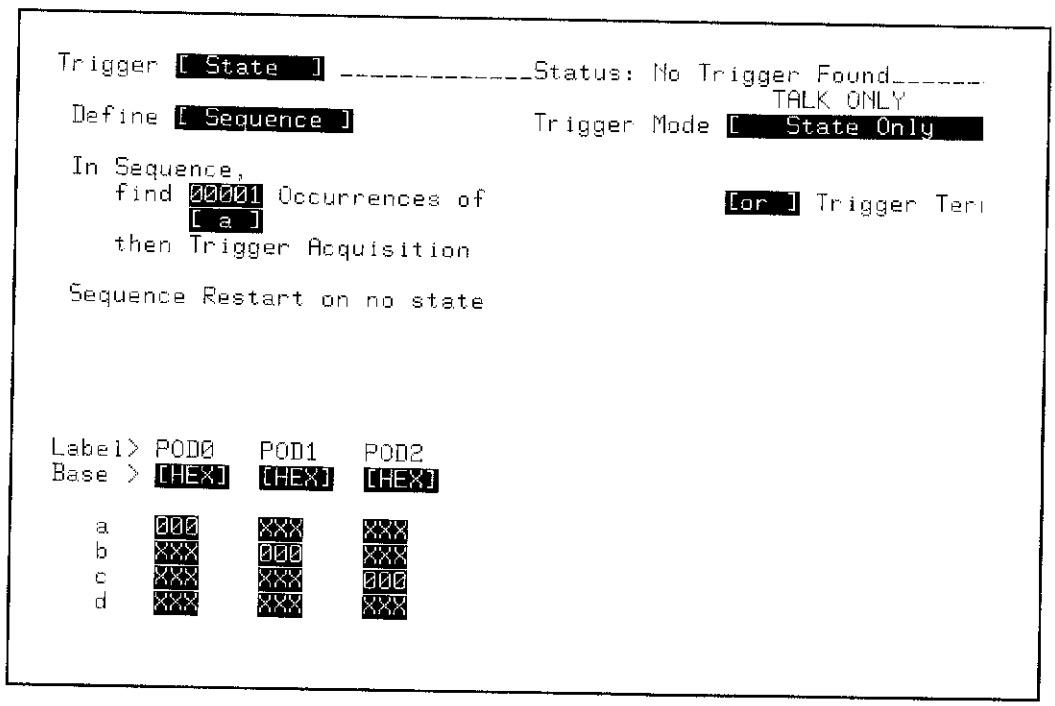


Figure 3-20. TRIGGER State / Define [Sequence] Menu

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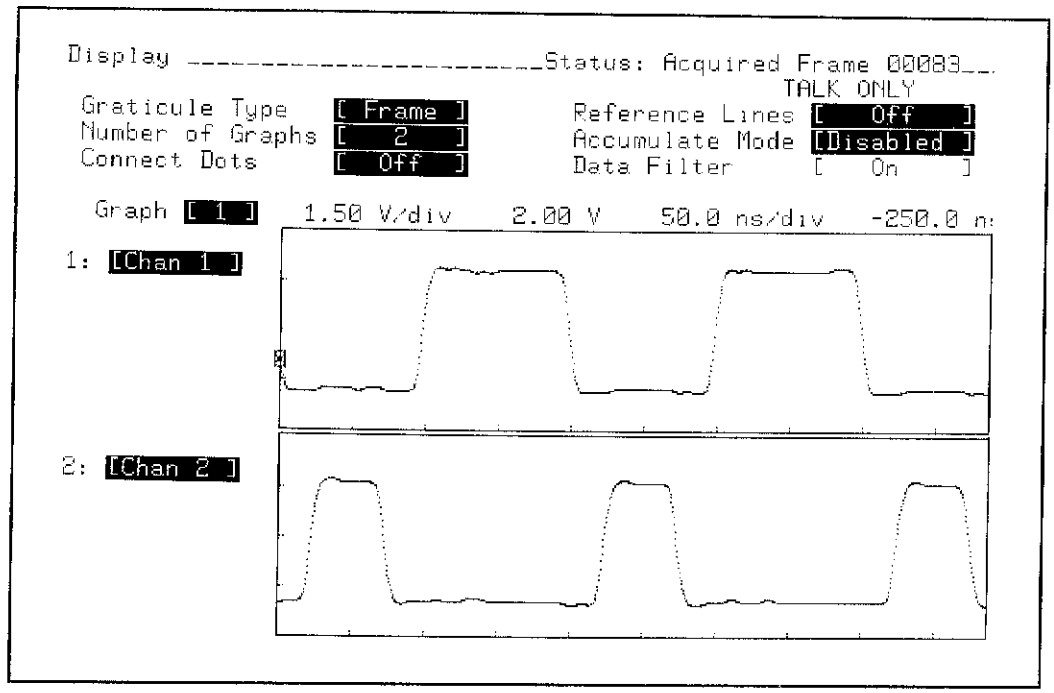


Figure 3-21. Display Configuration and Minimum Setup Time Test Waveforms

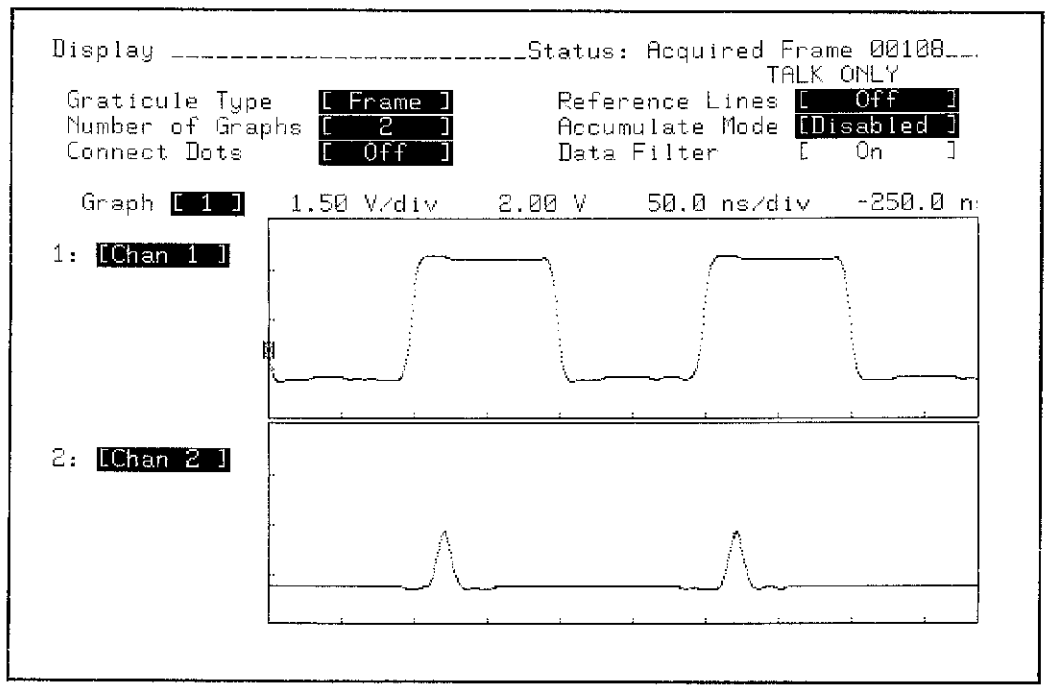


Figure 3-22. Minimum Setup Time Waveforms

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PERFORMANCE TESTS

3-13. MINIMUM HOLD TIME TEST (HP 54201D Only)

Specifications: 0 seconds, the time data must be present after the clock transition.

Equipment Required:

Pulse Generator	HP 8161A Opt. 020
Product Support Kit	HP Part No. 54200-69501
BNC Tee (Qty 2)	HP Part No. 1250-0781
BNC Cable, 9-inch (Qty 2)	HP 10502A
BNC Cable, 48-inch (Qty 3)	HP 10503A

Equipment Setup:

HP 8161A

Ext Slope:	Pos
Period (PER):	200 ns

	A Output	B Output
Width (WID):	100 ns	50 ns
Leading Edge (LEE):	1.3 ns	1.3 ns
Trailing Edge (TRE):	1.3 ns	1.3 ns
High Level (HIL):	+4 V	+4 V
Low Level (LOL):	0 V	0 V
Delay (DEL):	105 ns	0.00 ns
Output mode:	Enable	Enable

Procedure:

1. Configure the STATUS Configuration menu as shown in figure 3-23.
2. Configure the STATUS Measurement menu as shown in figure 3-24.
3. In the SYSTEM Peripherals menu select Rear Panel BNC: [Pulse On State Sequence True].
4. Configure the TRIGGER State / Define [Assignment] menu as shown in figure 3-25.
5. Configure the TRIGGER State / Define [Sequence] menu as shown in figure 3-26.
6. Connect POD 0 to the State Board Test fixture, HP Part No. 54200-63801 (part of Product Support Kit).
7. Connect a BNC tee to the BNC labeled "CLOCK" on the State Board Test fixture.
8. Connect a BNC cable from the "B" output of the pulse generator to the "CLOCK" BNC tee, and a short BNC cable from the "CLOCK" BNC tee to the Channel 2 input of the HP 54201D.
9. Connect a BNC tee to the BNC labeled "DATA" on the State Board Test fixture.
10. Connect a BNC cable from the "A" output of the pulse generator to the "DATA" BNC tee, and a short BNC cable from the "DATA" BNC tee to the Channel 1 input of the HP 54201D.

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PERFORMANCE TESTS

11. Connect a BNC cable from the rear panel BNC of the HP 54201D to the front panel EXT TRIG input of the HP 54201D.

12. Configure the display as shown in figure 3-27. Observe the waveforms displayed. They should appear similar to those shown in figure 3-27. If not, repeat steps 1 through 11.

13. Exchange the BNC cables connected to Channel 2 and External Trigger inputs. The display should appear similar to figure 3-28.

14. While observing the pulses displayed on Channel 2, decrement the pulse generator output "A" delay in 1 ns steps until the pulses on Channel 2 display disappear.

15. Now increment the delay in 1 ns steps until the pulses reappear on that channel.

16. Exchange the BNC cables connected to Channel 2 and External Trigger inputs. The display should appear similar to figure 3-27.

17. Select the DELAY measurement on the HP 54201D and set to "Delay 2 to 1". The DELAY measurement should read ≤0 ns.

18. Change the output "A" delay of the pulse generator to 105 ns.

19. Reconfigure the TRIGGER State/Define [Sequence] menu in figure 3-26 with "Occurrences of [b]".

20. Connect POD 1 to the State Board Test fixture and repeat steps 12 through 17 for POD 1.

21. Change the output "A" delay of the pulse generator to 105 ns.

22. Reconfigure the STATE Sequence menu in figure 3-26 with "Occurrences of [c]".

23. Connect POD 2 to the State Board Test fixture and repeat steps 12 through 17 for POD 2.

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PERFORMANCE TESTS

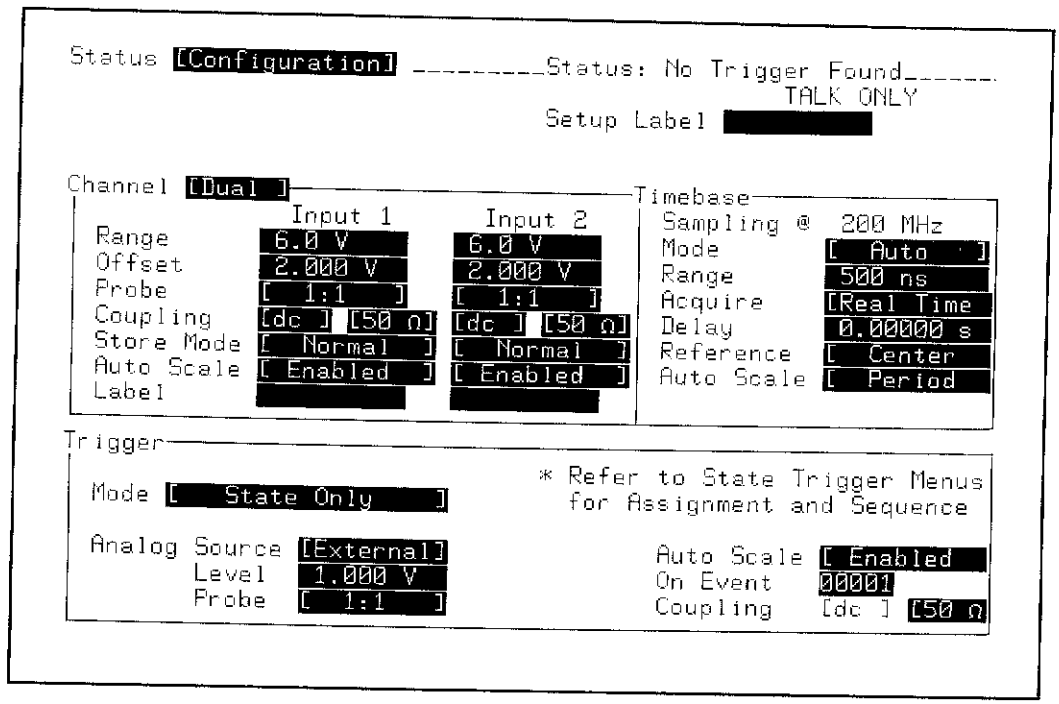


Figure 3-23. STATUS Configuration Menu

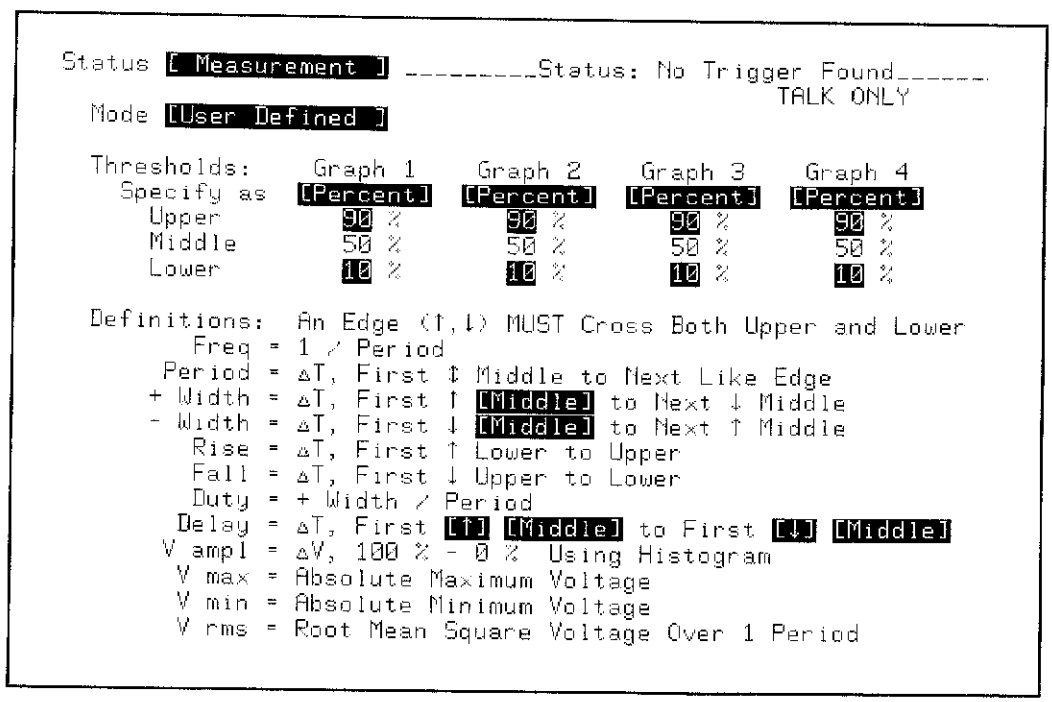


Figure 3-24. STATUS Measurement Menu

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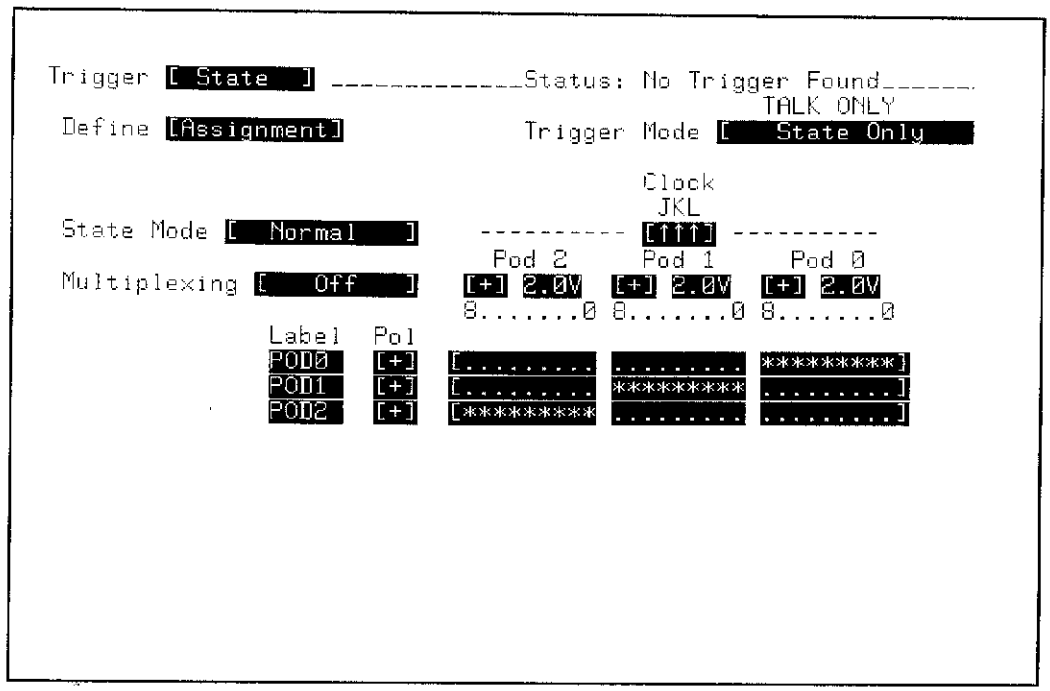


Figure 3-25. TRIGGER State / Define [Assignment] Menu

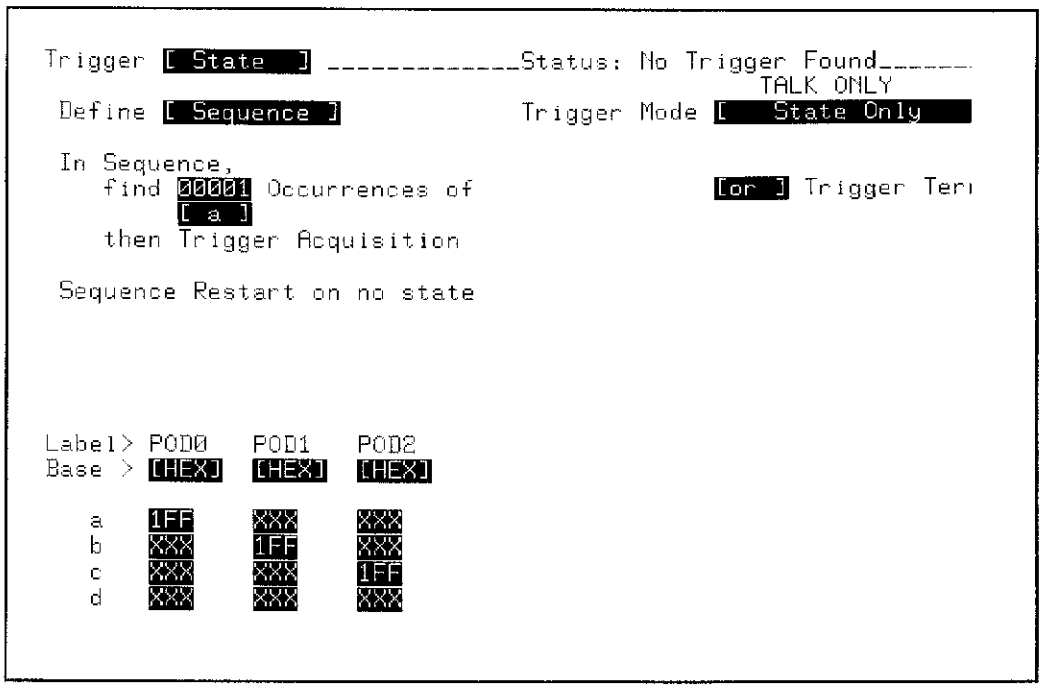


Figure 3-26. TRIGGER State / Define [Sequence] Menu

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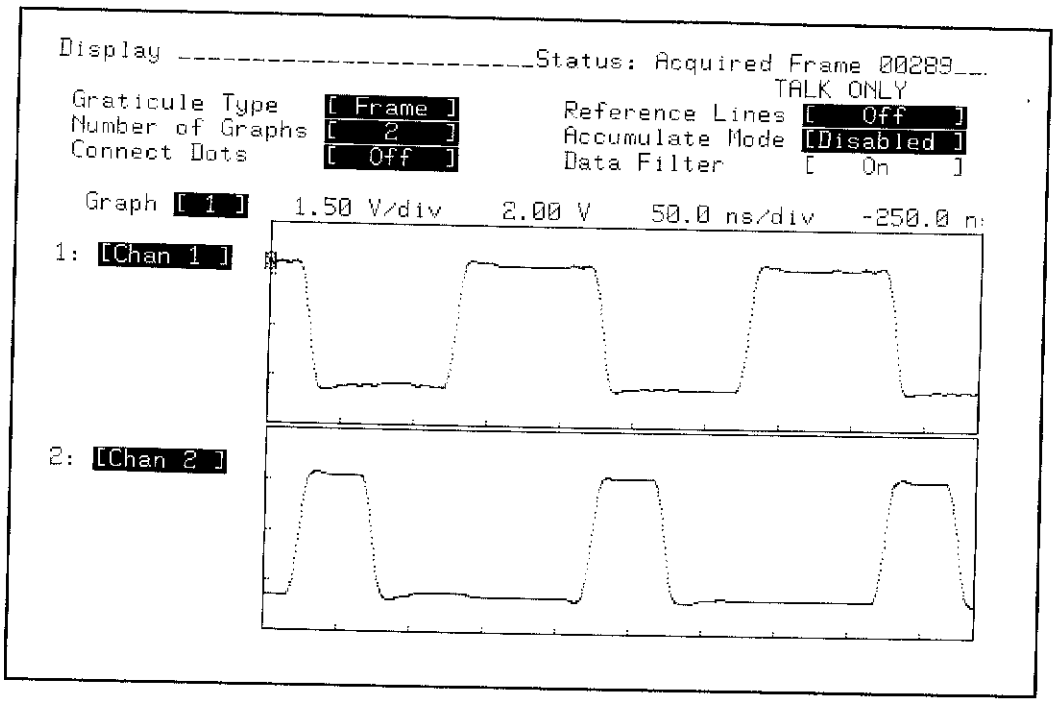


Figure 3-27. Display Configuration and Minimum Hold Time Test Waveforms

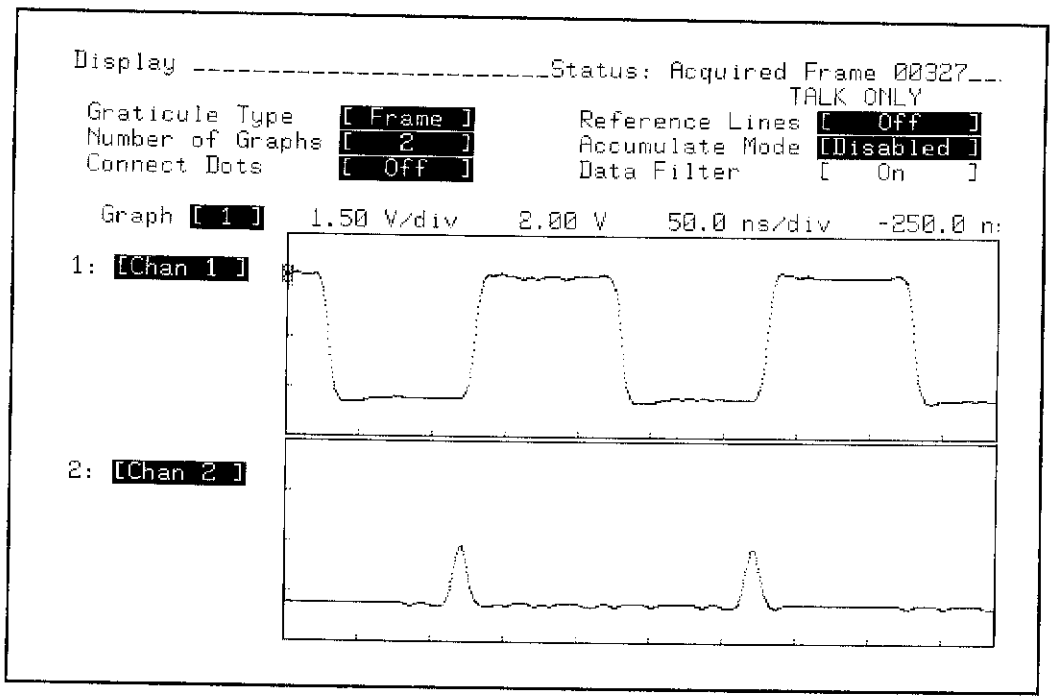


Figure 3-28. Minimum Hold Time Test Waveform

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PERFORMANCE TESTS

3-14. MINIMUM CLOCK PULSE WIDTH TEST (HP 54201D Only)

Specifications: 20 ns at threshold.

Equipment Required:

Pulse Generator ..... HP 8161A Opt. 020
Product Support Kit ..... HP Part No. 54200-69501
BNC Tee ..... HP Part No. 1250-0781
BNC Cable, 9-inch ..... HP 10502A
BNC Cable, 48-inch (Qty 2) ..... HP 10503A

Equipment Setup:

HP 8161A

Period (PER):	200 ns	
	A Output	B Output
Width (WID):	25 ns	25 ns
Leading Edge (LEE):	1.3 ns	1.3 ns
Trailing Edge (TRE):	1.3 ns	1.3 ns
High Level (HIL):	+4 V	+4 V
Low Level (LOL):	0 V	0 V
Delay (DEL):	0 ns	0 ns
Output mode:	Disable	Enable

Procedure:

1. Configure the STATUS Configuration menu as shown in figure 3-29.
2. Configure the STATUS Measurement menu in Standard mode.
3. In the SYSTEM Peripherals menu select Rear Panel BNC: [Pulse On State Sequence True].
4. Configure the TRIGGER State / Define [Assignment] menu as shown in figure 3-30.
5. Configure the TRIGGER State / Define [Sequence] menu as shown in figure 3-31.
6. Connect POD 0 to the State Board Test fixture, HP Part No. 54200-63801 (part of Product Support Kit).
7. Connect a BNC tee to the BNC labeled "CLOCK" on the State Board Test fixture.
8. Connect a BNC cable from the "B" output of the pulse generator to the "CLOCK" BNC tee, and a short BNC cable from the "CLOCK" BNC tee to Channel 2 input of the HP 54201D.

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PERFORMANCE TESTS

Note

The 9 data channels of the POD do not have a signal input during this test.

9. Connect a BNC cable from the rear panel BNC of the HP 54201D to the front panel Channel 1 input on the HP 54201D.

10. Configure the display as shown in figure 3-32. Observe the two waveforms displayed on the HP 54201D. The two waveforms should appear similar to those shown in figure 3-32.

11. While observing the pulses displayed on Channel 1, decrement the pulse generator output "B" width in 1 ns steps until the pulses on Channel 1 display disappear, or until the pulse generator reaches its narrowest width.

12. Increment the width until Channel 1 pulses reappear (if necessary).

13. Select the + WIDTH measurement on the HP 54201D and insert "2".

14. The measurement should read ≤20 ns.

15. Change the "B" output width of the pulse generator to 25 ns.

16. Disconnect POD 0 and connect POD 1. Repeat steps 10 through 14.

17. Change the "B" output width of the pulse generator to 25 ns.

18. Disconnect POD 1 and connect POD 2. Repeat steps 10 through 14.

19. Change the "B" output width of the pulse generator to 25 ns.

20. Select the complement mode for the "B" output of the pulse generator.

21. In the TRIGGER State / Define [Assignment] menu (figure 3-30), change the J, K, and L clocks to the falling (↓) edge.

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22. Disconnect POD 2 and connect POD 0.

23. The waveforms displayed on screen should be similar to figure 3-33.

24. Repeat steps 11 through 15 using the - WIDTH measurement of the HP 54201D instead of the + WIDTH measurement.

25. Disconnect POD 0 and connect POD 1.

26. The waveforms displayed on screen should be similar to figure 3-33.

27. Repeat steps 11 through 15 using the - WIDTH measurement of the HP 54201D instead of the + WIDTH measurement.

28. Disconnect POD 1 and connect POD 2.

29. The waveforms displayed on screen should be similar to figure 3-33.

30. Repeat steps 11 through 14 using the - WIDTH measurement of the HP 54201D instead of the + WIDTH measurement.

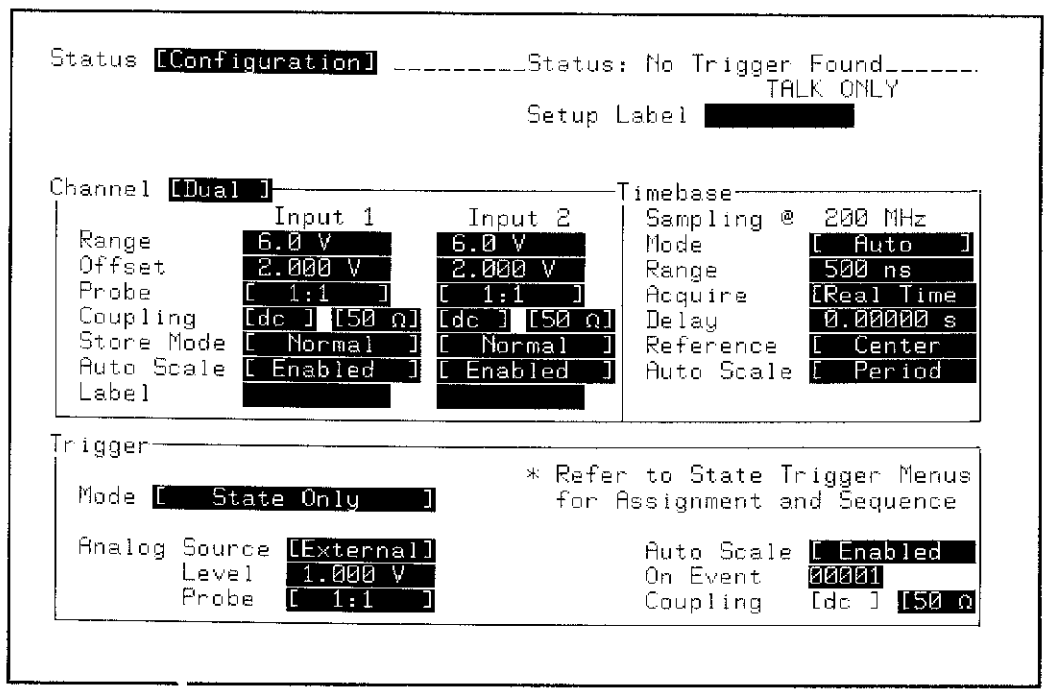


Figure 3-29. STATUS Configuration Menu

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PERFORMANCE TESTS

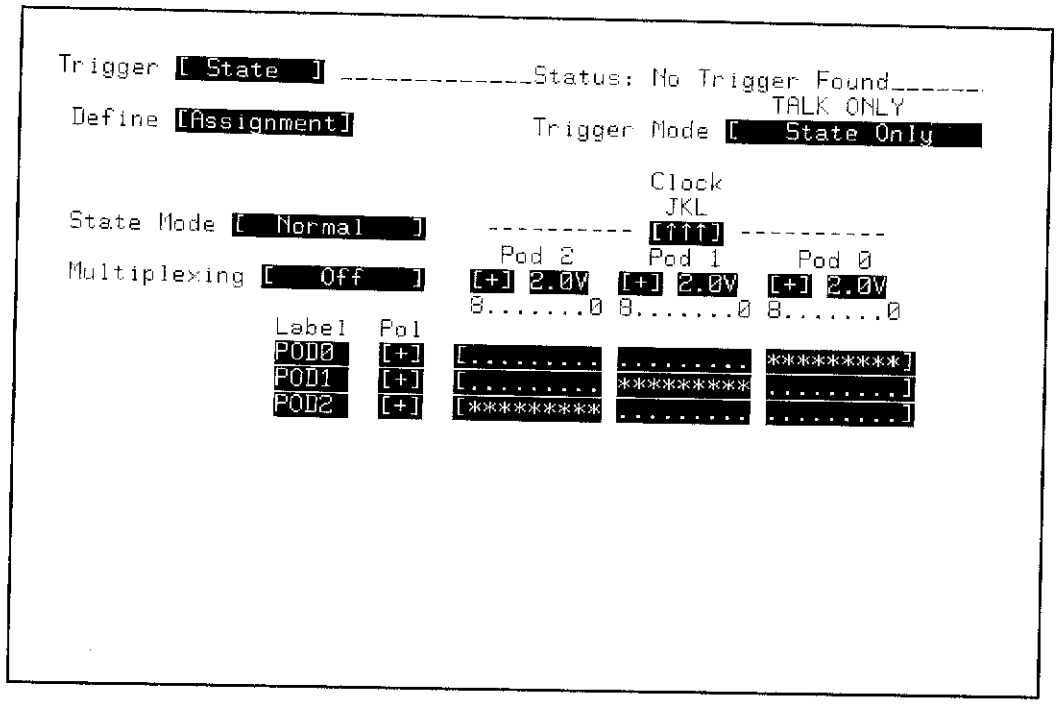


Figure 3-30. TRIGGER State / Define [Assignment] Menu

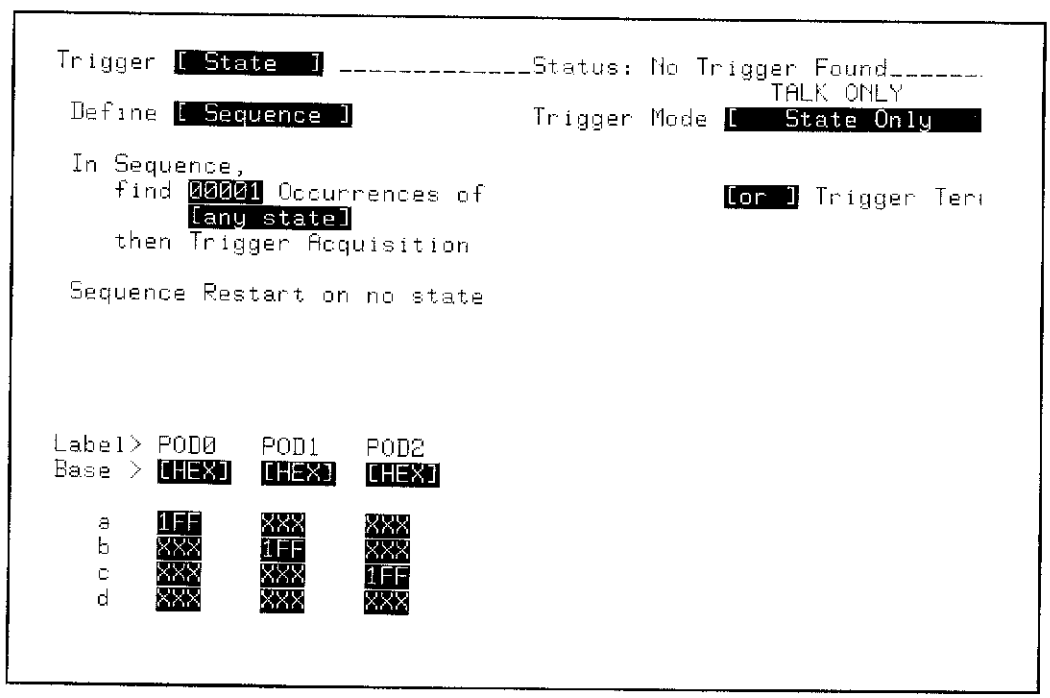


Figure 3-31. TRIGGER State / Define [Sequence] Menu

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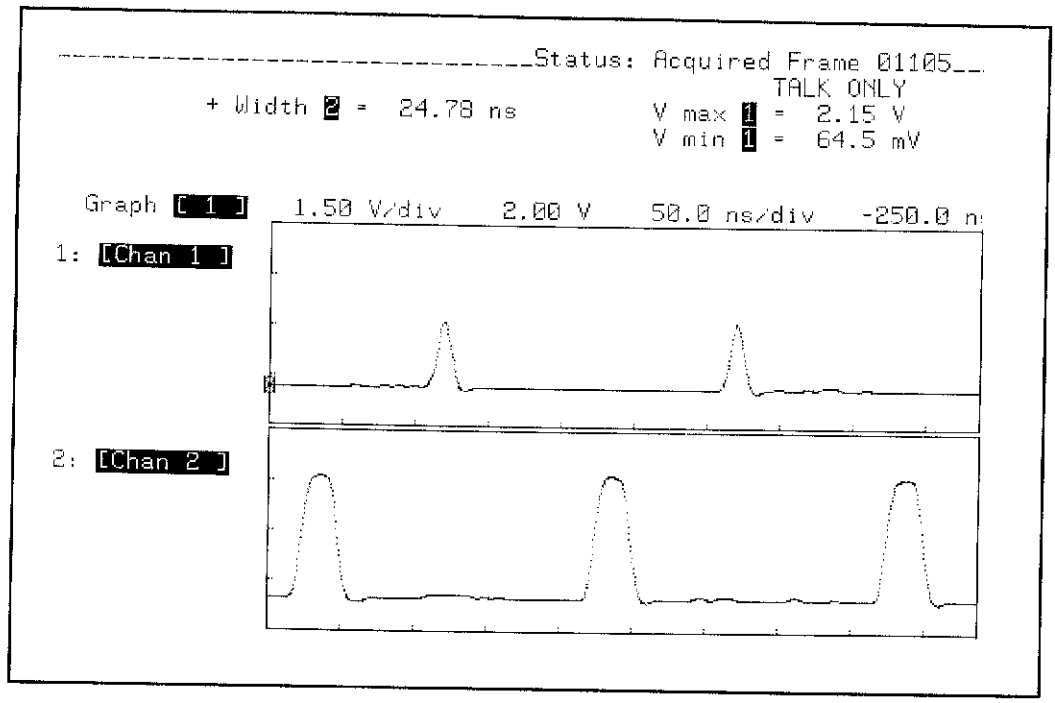


Figure 3-32. DISPLAY Configuration and Clock Pulse Width Test Waveforms

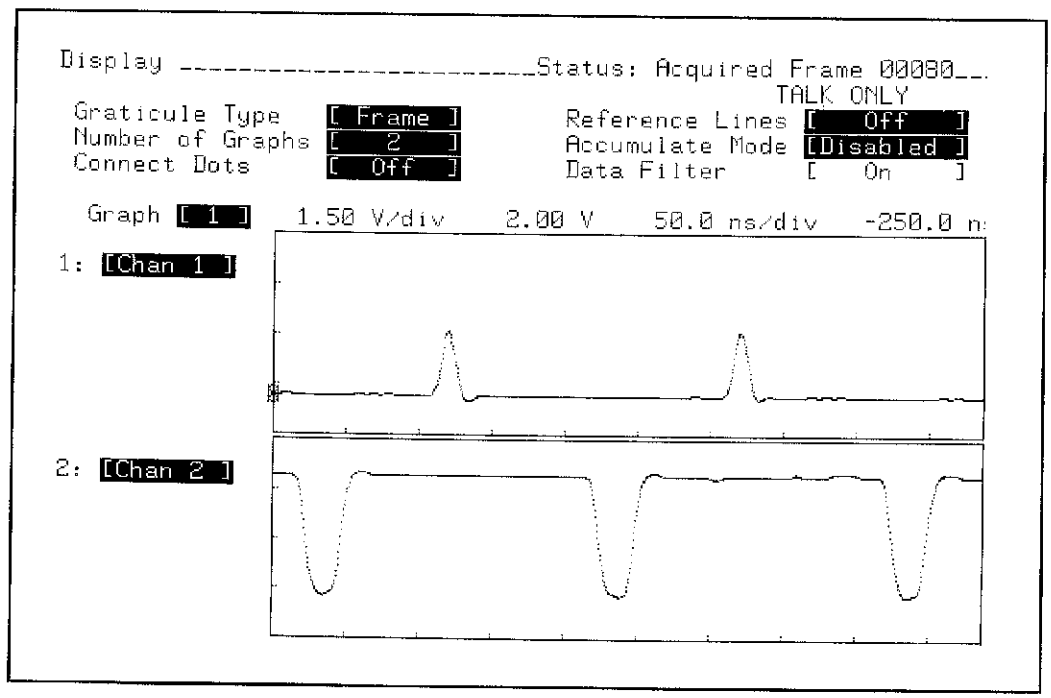


Figure 3-33. Clock Pulse Width Test Waveforms

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PERFORMANCE TESTS

3-15. CLOCK REPETITION RATE TEST (HP 54201D Only)

Specifications: Single phase - 25 MHz maximum with single clock and single edge specified.

Equipment Required:

Pulse Generator	HP 8161A Opt. 020
Product Support Kit	HP Part No. 54200-69501
BNC Tee	HP Part No. 1250-0781
BNC Cable, 9-inch	HP 10502A
BNC Cable, 48-inch (Qty 2)	HP 10503A

Equipment Setup:

HP 8161A

Period (PER):	50 ns	
	A Output	B Output
Width (WID):	15 ns	15 ns
Leading Edge (LEE):	1.3 ns	1.3 ns
Trailing Edge (TRE):	1.3 ns	1.3 ns
High Level (HIL):	+4 V	+4 V
Low Level (LOL):	0 V	0 V
Delay (DEL):	0 ns	0 ns
Output mode:	Enable	Enable
Norm/Compl	Normal	Normal

Procedure:

1. Configure the STATUS Configuration menu as shown in figure 3-34.
2. Configure the STATUS Measurement menu in Standard mode.
3. In the SYSTEM Peripherals menu select Rear Panel BNC: [Pulse On State Sequence True].
4. Configure the TRIGGER State / Define [Assignment] menu as shown in figure 3-35.
5. Configure the TRIGGER State / Define [Sequence] menu as shown in figure 3-36.
6. Connect POD 0 to the State Board Test fixture, HP Part No. 54200-63801 (part of Product Support Kit).
7. Connect a BNC tee to the BNC labeled "CLOCK" on the State Board Test fixture.
8. Connect a BNC cable from the "B" output of the pulse generator to the "CLOCK" BNC tee, and a short BNC cable from the "CLOCK" BNC tee to Channel 2 input of the HP 54201D.

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Note

The 9 data channels of the POD do not have a signal input during this test.

9. Connect a BNC cable from the rear panel BNC of the HP 54201D to the front panel Channel 1 input on the HP 54201D.

10. Configure the display as shown in figure 3-37. Observe the two waveforms displayed on the HP 54201D. The two waveforms should appear similar to those shown in figure 3-37.

11. While observing the pulses displayed on Channel 1, decrement the pulse generator period in 1 ns steps until the Channel 1 waveform begins to drop pulses as shown in figure 3-38.

12. Increment the period of the pulse generator "B" output until the Channel 1 waveform pulses are again present.

13. Select the FREQ measurement on the HP 54201D and for graph 2. The frequency should be ≥25 MHz.

14. Set the period of the pulse generator to 50 ns.

15. Disconnect POD 0 and connect POD 1. Repeat steps 10 through 13.

16. Set the period of the pulse generator to 50 ns.

17. Disconnect POD 1 and connect POD 2. Repeat steps 10 through 13.

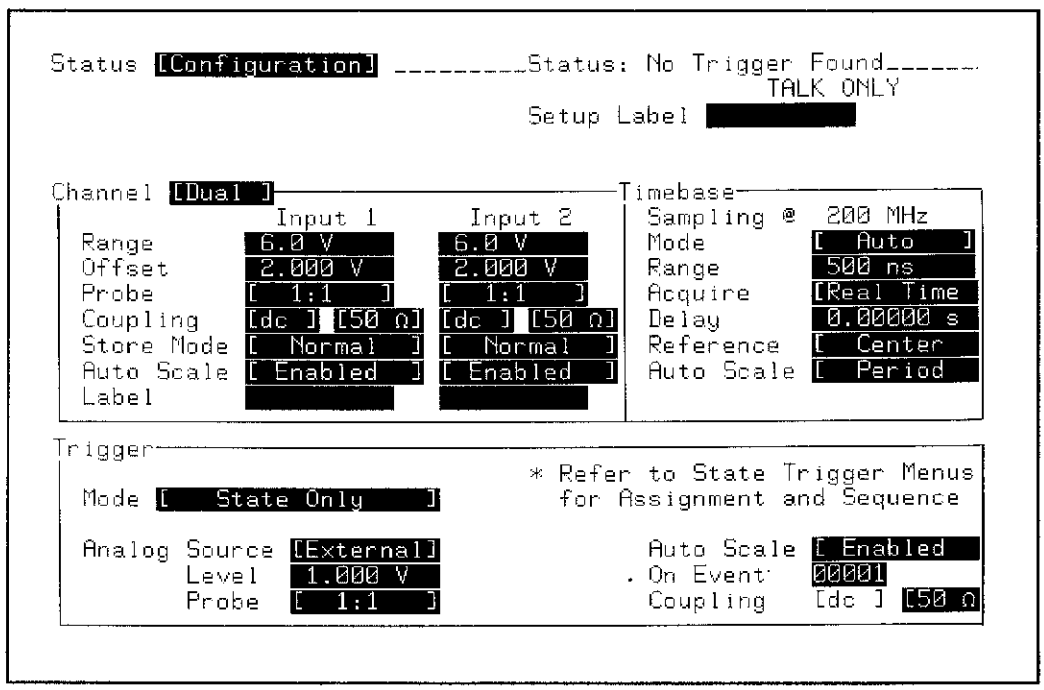


Figure 3-34. STATUS Configuration Menu

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PERFORMANCE TESTS

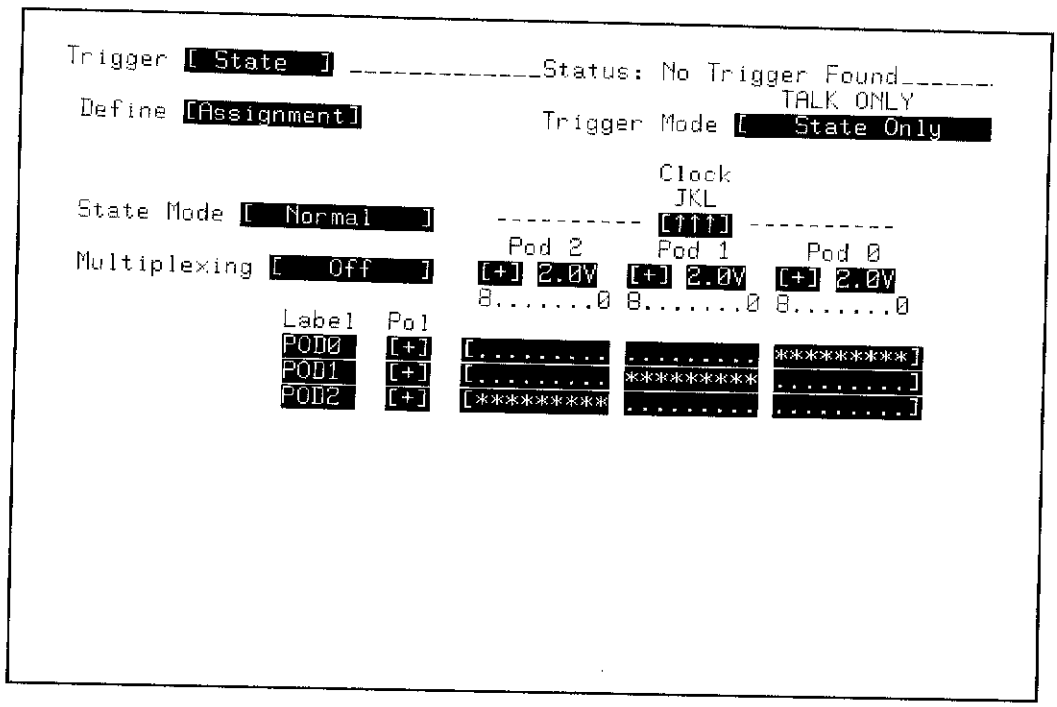


Figure 3-35. TRIGGER State / Define [Assignment] Menu

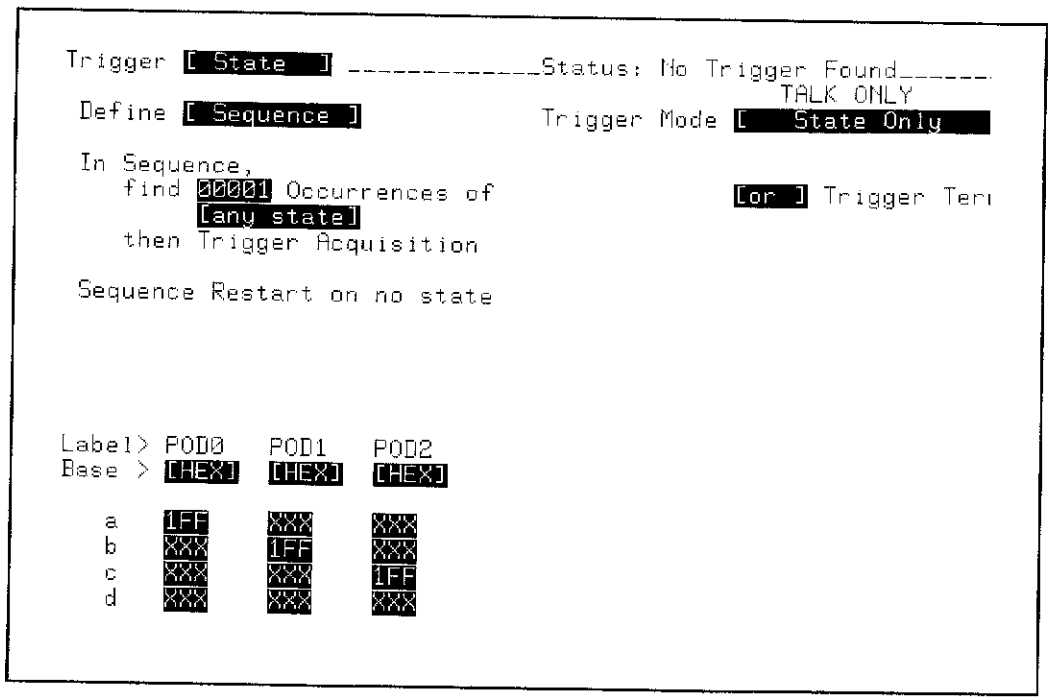


Figure 3-36. TRIGGER State / Define [Sequence] Menu

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PERFORMANCE TESTS

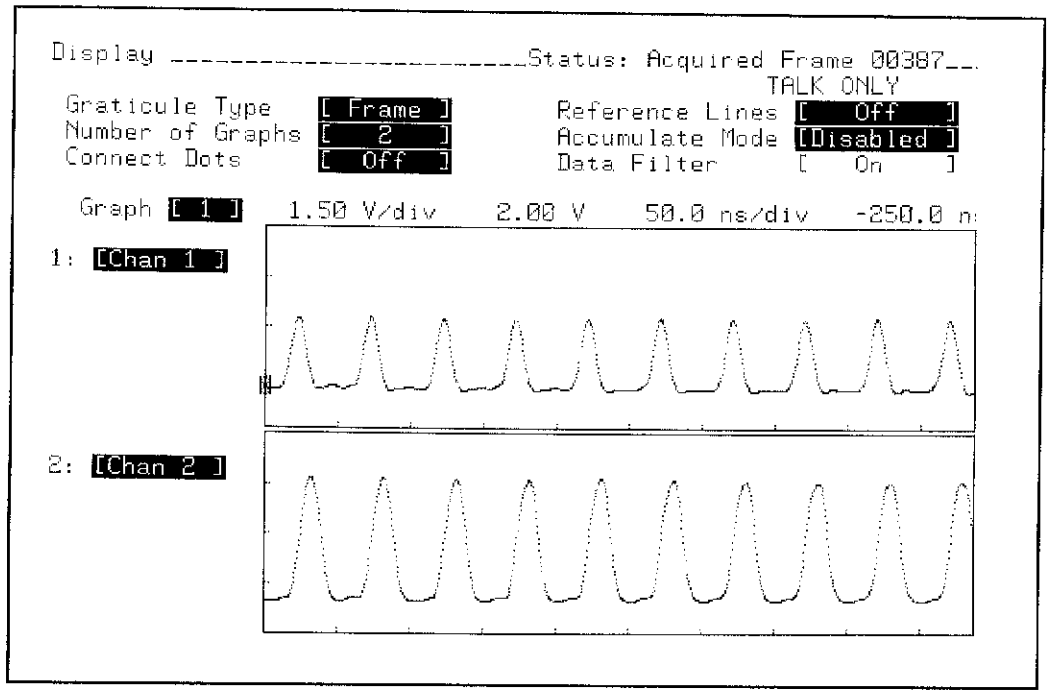


Figure 3-37. DISPLAY Configuration and Clock Repetition Rate Test Waveforms

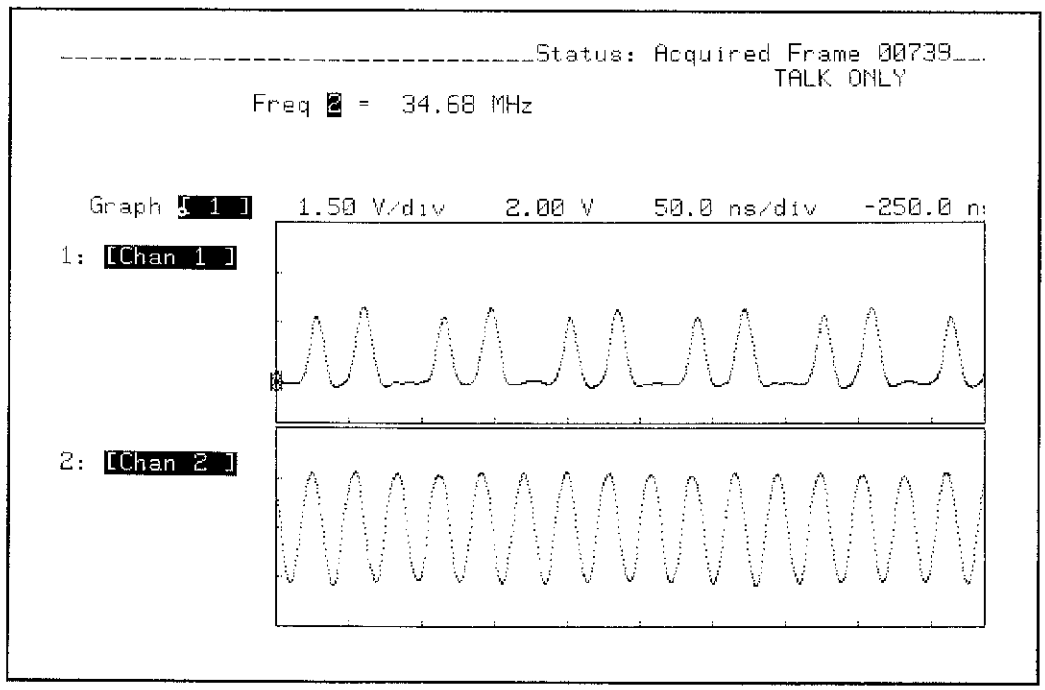


Figure 3-38. Clock Repetition Rate Test Waveforms

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PERFORMANCE TESTS

3-16. MINIMUM INPUT TEST (HP 54201D Only)

Specifications: 600 mV peak-to-peak

Equipment Required:

Pulse Generator	HP 8161A Opt. 020
Product Support Kit	HP Part No. 54200-69501
Blocking Capacitor	HP 10240B
BNC Tee	HP Part No. 1250-0781
BNC Cable, 9-inch	HP 10502A
BNC Cable, 48-inch (Qty 2)	HP 10503A

Equipment Setup:

HP 8161A

Period (PER):	100 ns	
	A Output	B Output
Width (WID):	50 ns	50 ns
Leading Edge (LEE):	1.3 ns	1.3 ns
Trailing Edge (TRE):	1.3 ns	1.3 ns
High Level (HIL):	+0.65 V	+0.65 V
Low Level (LOL):	0 V	0 V
Delay (DEL):	0 ns	0 ns
Output mode:	Disable	Enable

Procedure:

1. Configure the STATUS Configuration menu as shown in figure 3-39.
2. In the SYSTEM Peripherals menu select Rear Panel BNC: [Pulse On State Sequence True].
3. Configure the TRIGGER State / Define [Assignment] menu as shown in figure 3-40.
4. Configure the TRIGGER State / Define [Sequence] menu as shown in figure 3-41.
5. Connect POD 0 to the State Board Test fixture, HP Part No. 54200-63801 (part of Product Support Kit).
6. Connect a BNC tee to the BNC labeled "CLOCK" on the State Board Test fixture.
7. Connect the blocking capacitor to the "B" output of the pulse generator.
8. Connect a BNC cable from the Blocking Capacitor to the "CLOCK" BNC tee, and a short BNC cable from the "CLOCK" BNC tee to Channel 2 input of the HP 54201D.

Note

The 9 data channels of the POD do not have a signal input during this test.

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9. Connect a BNC cable from the rear panel BNC of the HP 54201D to the front panel Channel 1 input on the HP 54201D.

10. Configure the display as shown in figure 3-42. The displayed waveforms should appear similar to those shown in figure 3-42.

11. While observing the pulses displayed on Channel 1, decrement the High Level (HIL) B output of the pulse generator period in 0.01 volt steps until the waveform on Channel 1 starts to drop pulses.

12. Increment the High Level (HIL) B in 0.01 volt steps until all pulses are again present.

13. The High Level (HIL) B readout on the pulse generator should be ≤0.6 V.

14. Change the High Level (HIL) B of the pulse generator to 0.65 V.

15. Disconnect POD 0 and connect POD 1. Repeat steps 10 through 13.

16. Change the High Level (HIL) B of the pulse generator to 0.65 V.

17. Disconnect POD 1 and connect POD 2. Repeat steps 10 through 13.

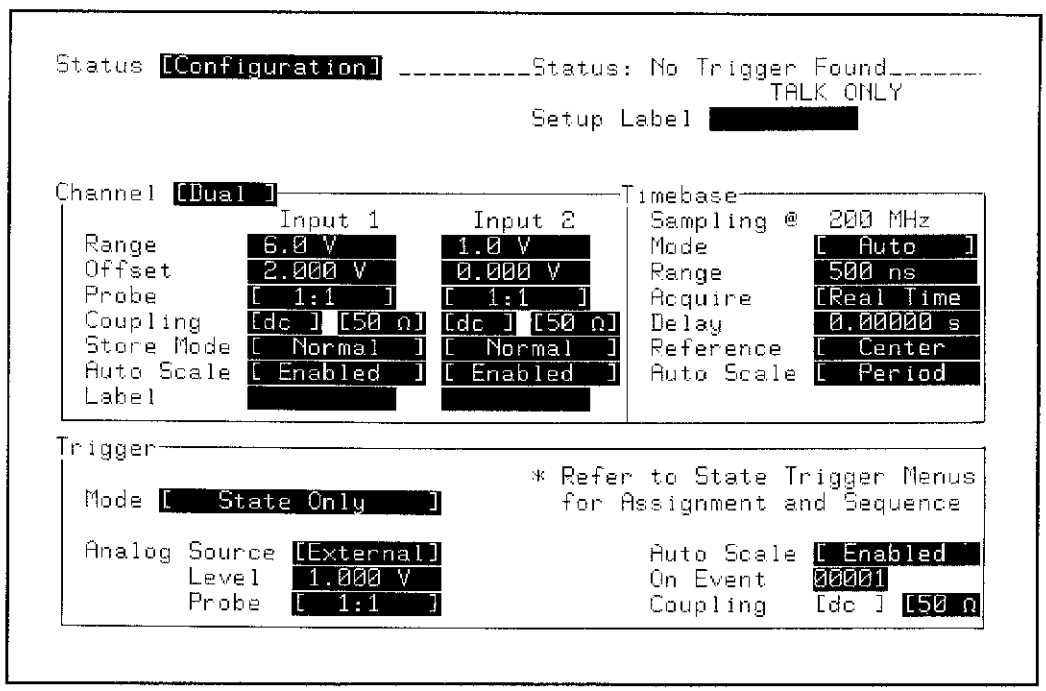


Figure 3-39. STATUS Configuration Menu

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PERFORMANCE TESTS

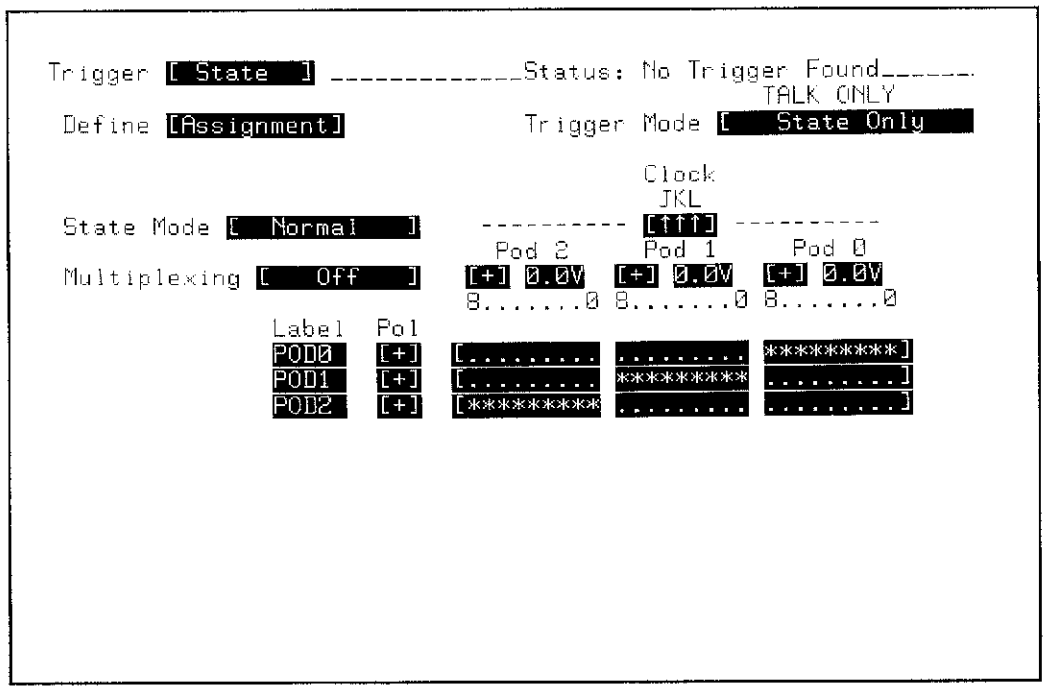


Figure 3-40. TRIGGER State / Define [Assignment] Menu

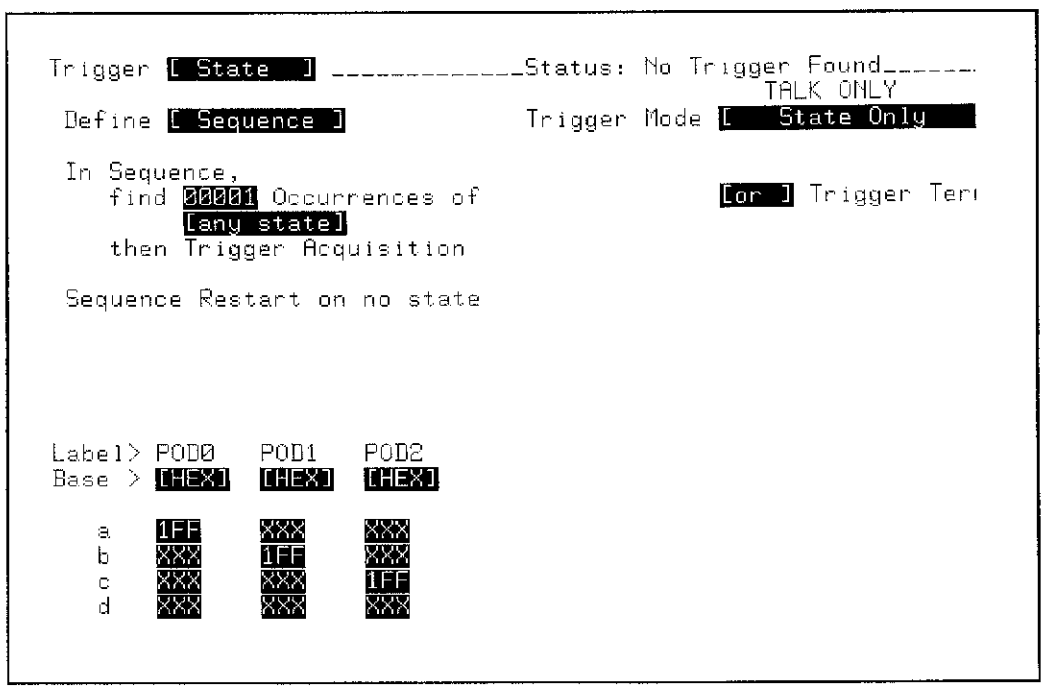


Figure 3-41. TRIGGER State / Define [Sequence] Menu

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PERFORMANCE TESTS

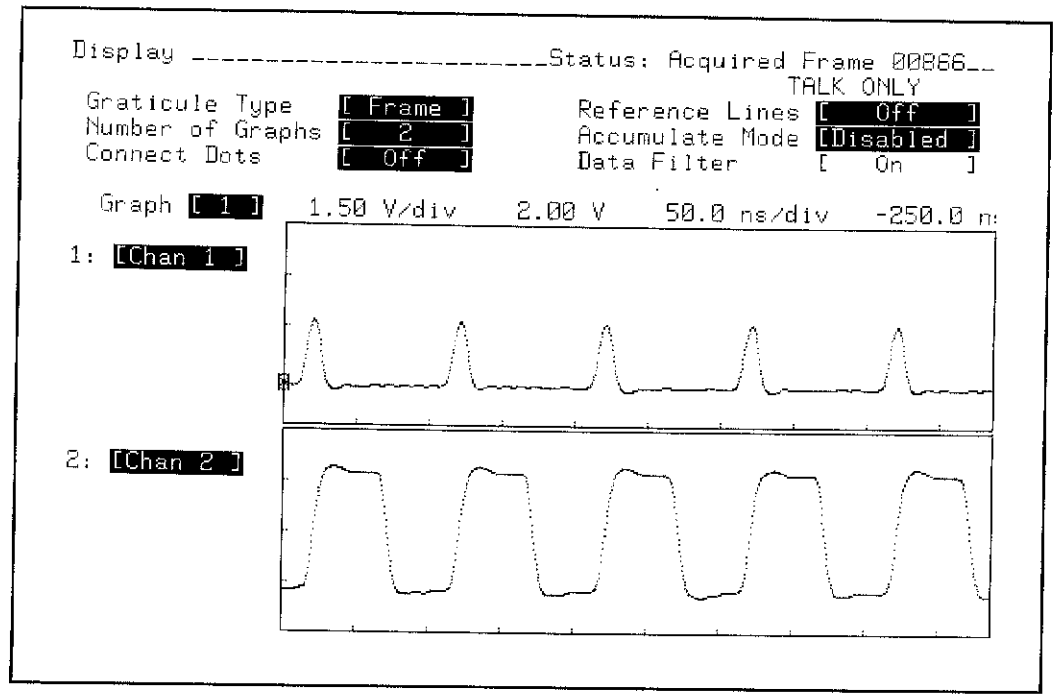


Figure 3-42. DISPLAY Configuration and Minimum Input Test Waveform

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PERFORMANCE TESTS

3-17. THRESHOLD ACCURACY TEST (HP 54201D Only)

Specifications: ±2.5% ±120 mV.

Equipment Required:

Dc Supply ..... HP 6114A
Pulse Generator ..... HP 8161A Opt. 020
Product Support Kit ..... HP Part No. 54200-69501
BNC Tee ..... HP Part No. 1250-0781
BNC Cable, 9-inch ..... HP 10502A
BNC Cable, 48-inch (Qty 4) ..... HP 10503A
BNC(f)-to-Dual Banana Adapter ..... HP Part No. 1251-2277

Equipment Setup:

HP 8161A

Period (PER): 100 ns

	A Output	B Output
Width (WID):	50 ns	50 ns
Leading Edge (LEE):	1.3 ns	1.3 ns
Trailing Edge (TRE):	1.3 ns	1.3 ns
High Level (HIL):	+5 V	+5 V
Low Level (LOL):	0 V	0 V
Delay (DEL):	0 ns	0 ns
Output mode:	Disable	Enable

HP 6114A

Output: +4.3 V

Procedure:

1. Configure the STATUS Configuration menu as shown in figure 3-43.

2. In the SYSTEM Peripherals menu select Rear Panel BNC: [Pulse On State Sequence True].

3. Configure the TRIGGER State / Define [Assignment] menu as shown in figure 3-44.

4. Configure the TRIGGER State / Define [Sequence] menu as shown in figure 3-45.

5. Connect a BNC(f)-to-dual banana adapter and BNC tee to the DC Supply. Connect a BNC cable from the DC Supply BNC tee to the Channel 1 input of the HP 54201D. Connect another BNC cable from the DC Supply BNC tee to the "DATA" input on the State Board Test fixture, HP Part No. 54200-63801 (part of Product Support Kit).

6. Connect POD 0 to the State Board Test fixture.

7. Connect a BNC tee to the BNC labeled "CLOCK" on the State Board Test fixture.

8. Connect a BNC cable from the "B" output of the pulse generator to the "CLOCK" BNC tee, and a short BNC cable from the "CLOCK" BNC tee to Channel 2 input of the HP 54201D.

9. Connect a BNC cable from the rear panel BNC of the HP 54201D to the front panel EXT TRIG input of the HP 54201D.

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PERFORMANCE TESTS

10. Configure the display as shown in figure 3-46. The waveforms should appear similar to those shown in figure 3-46.

11. Exchange the BNC cables connected to Channel 2 and External Trigger inputs. The display should appear similar to figure 3-47.

12. Decrease the output of the DC Supply in 0.01 volt steps until the Channel 2 waveform begins to drop pulses.

13. Increase the output of the DC Supply until the Channel 2 pulses reappear as shown in figure 3-47. The DC Supply should read ≥3.78 V and ≤4.22 V.

14. Change the output level of the DC Supply to +4.3.

15. Reconfigure the TRIGGER State/Define [Sequence] menu shown in figure 3-45 with "Occurrences of [b]". Disconnect POD 0 and connect POD 1. Repeat steps 12 through 14.

16. Reconfigure the TRIGGER State/Define [Sequence] menu shown in figure 3-45 with "Occurrences of [c]". Disconnect POD 1 and connect POD 2. Repeat steps 12 and 13.

17. Reconfigure the "B" output of the pulse generator as follows:

    High Level (HIL): 0 V
    Low Level (LOL): -5.00 V

18. Change the output of the DC Supply to provide -4.3 V.

19. Reconfigure the STATUS menu shown in figure 3-43 for Channel 1 offset of -2.5 V.

20. Disconnect POD 2 and connect POD 0.

21. Reconfigure the TRIGGER State/Define [Sequence] menu in figure 3-45 with "Occurrences of [a]".

22. Reconfigure the TRIGGER State/Define [Assignment] menu in figure 3-44 with thresholds of -4.0 V.

23. The Channel 2 pulses should be missing on the display.

24. Decrease the magnitude of the output level of the DC Supply in 0.01 volt steps until the Channel 2 waveform appears as shown in figure 3-47. The DC Supply should read ≤ -3.78 V and ≥ -4.22 V.

25. Change the output level of the DC Supply to -4.3 V.

26. Reconfigure the TRIGGER State/Define [Sequence] menu in figure 3-45 with "Occurrences of [b]". Replace POD 0 with POD 1 and repeat steps 23 through 25.

27. Reconfigure the TRIGGER State/Define [Sequence] menu in figure 3-45 with "Occurrences of [c]". Replace POD 1 with POD 2 and repeat steps 23 and 24.

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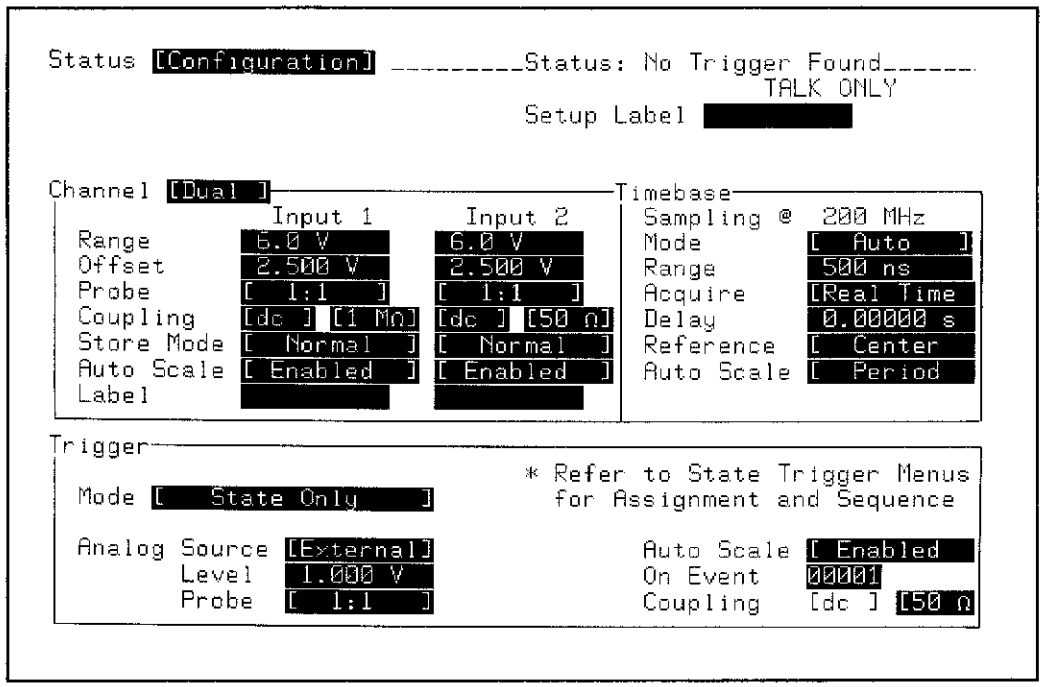


Figure 3-43. STATUS Configuration Menu

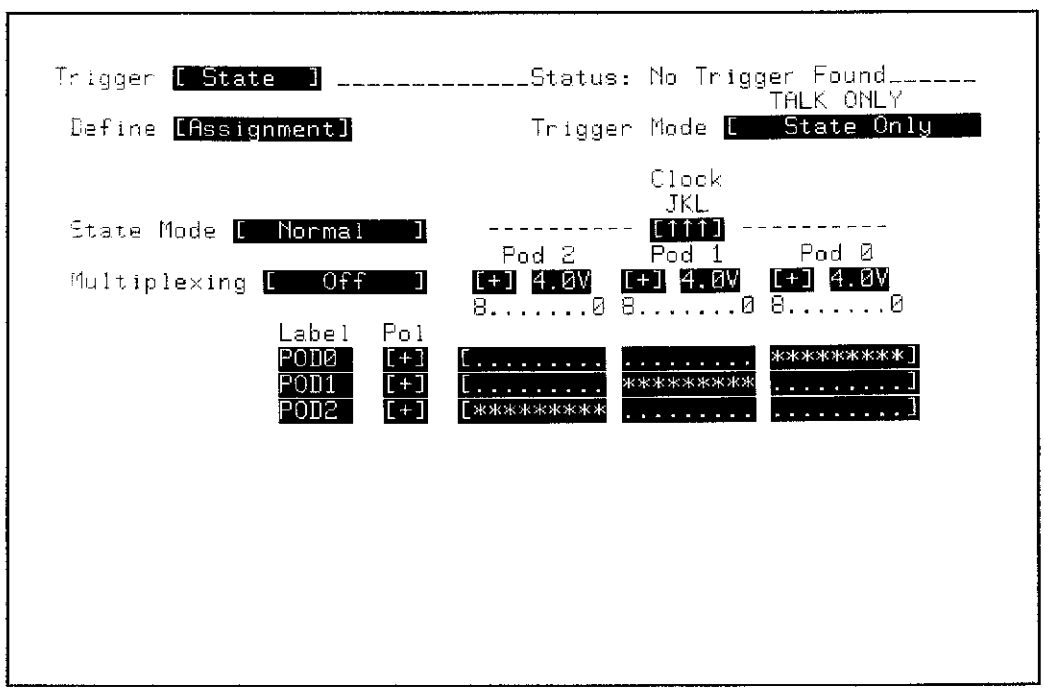


Figure 3-44. TRIGGER State / Define [Assignment] Menu

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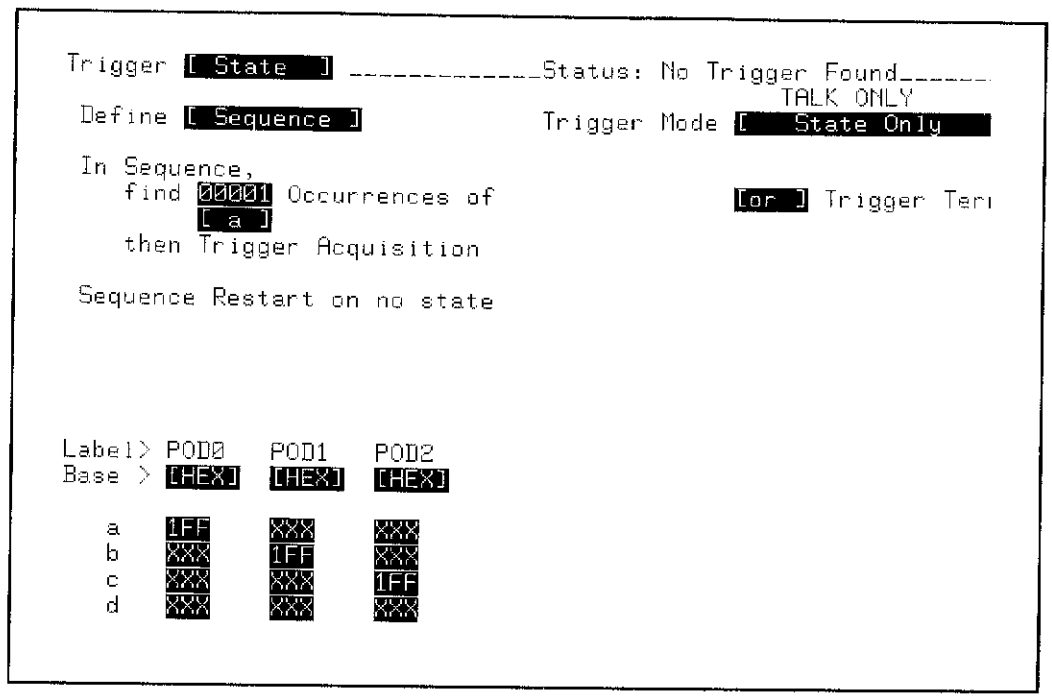


Figure 3-45. TRIGGER State / Define [Sequence] Menu

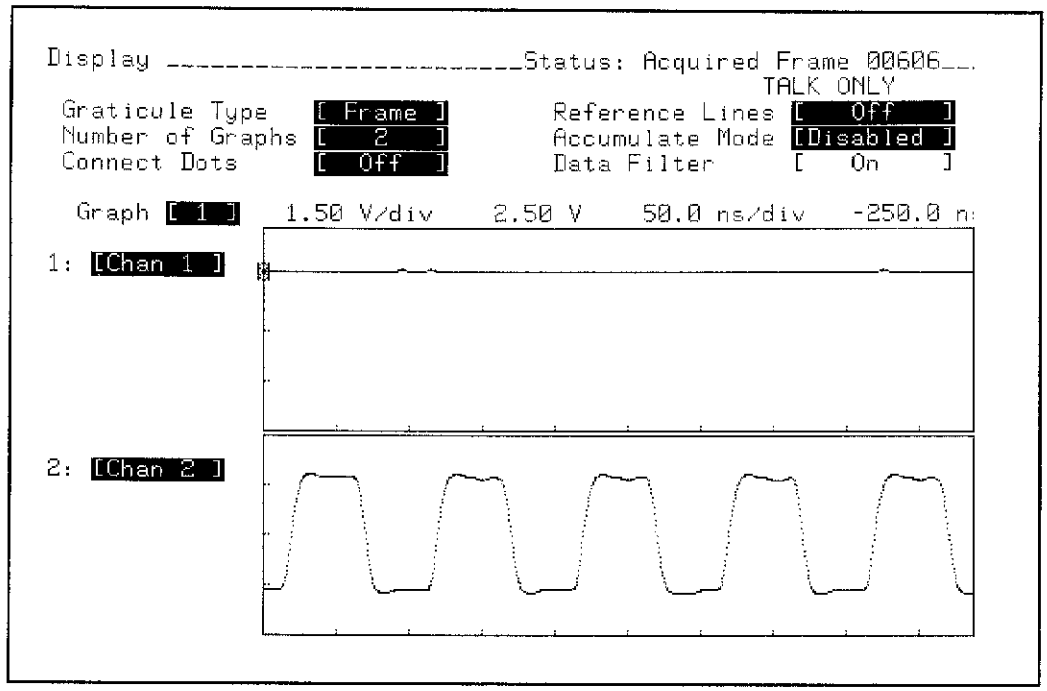


Figure 3-46. DISPLAY Configuration and Threshold Accuracy Test Waveforms

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PERFORMANCE TESTS

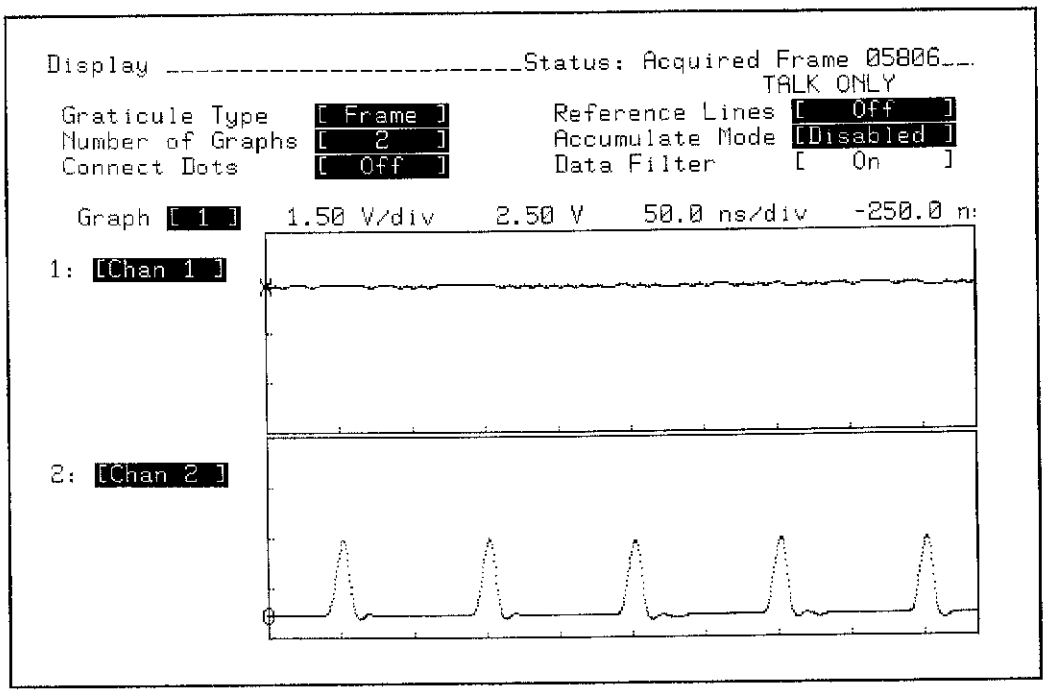


Figure 3-47. Threshold Accuracy Test Waveform

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Table 3-2. HP 54201A/D Performance Test Record

TEST	LIMITS	MEASURED
3-6. DC OFFSET ACCURACY	0.98 V to 1.02 V	VMIN VMAX CH.1_____ _____ CH.2_____ _____
	-0.98 V to -1.02 V	CH.1_____ _____ CH.2_____ _____
	-0.89 V to -1.11 V	CH.1_____ _____ CH.2_____ _____
	0.89 V to 1.11 V	CH.1_____ _____ CH.2_____ _____
3-7. VOLTAGE MEASUREMENT ACCURACY	84 mV to 116 mV	CH.1_____ CH.2_____
	-84 mV to -116 mV	CH.1_____ CH.2_____
	-4.32 V to -5.68 V	CH.1_____ CH.2_____
	4.32 V to 5.68 V	CH.1_____ CH.2_____
3-8. BANDWIDTH (-3dB)	Real Time ≤3 dB	CH.1_____ CH.2_____
	Repetitive ≤3 dB	CH.1_____ CH.2_____
3-9. TIME MEASUREMENT ACCURACY	Real Time 398 ns to 402 ns	_____
	Repetitive 3.8 ns to 4.2 ns	_____

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Table 3-2. HP 54201A/D Performance Test Record

TEST	LIMITS	MEASURED
3-10. TRIGGER (ANALOG) LEVEL ACCURACY	283 mV to 317 mV -283 mV to -317 mV -176 mV to -424 mV 176 mV to 424 mV	CH.1_____ CH.2_____ CH.1_____ CH.2_____ CH.1_____ CH.2_____ CH.1_____ CH.2_____
3-11. TRIGGER SENSITIVITY	Internal ≤2 V	CH.1_____ CH.2_____
	External 50Ω coupling .2 MΩ coupling	PASS_____ FAIL_____ PASS_____ FAIL_____
3-12. MINIMUM SETUP TIME (HP 54201D)	≤20 ns	POD0_____ POD1_____ POD2_____
3-13. MINIMUM HOLD TIME (54201D)	≤0 ns	POD0_____ POD1_____ POD2_____
3-14. MINIMUM CLOCK PULSE WIDTH (HP 54201D)	≤20 ns	+WIDTH -WIDTH POD0_____ _____ POD1_____ _____ POD2_____ _____
3-15. CLOCK REPETITION RATE (HP 54201D)	≥25 MHz	POD0_____ POD1_____ POD2_____
3-16. MINIMUM INPUT (HP 54201D)	≤0.60 V	POD0_____ POD1_____ POD2_____
3-17. THRESHOLD ACCURACY (HP 54201D)	3.78 V to 4.22 V -3.78 V to -4.22 V	POD0_____ POD1_____ POD2_____ POD0_____ POD1_____ POD2_____

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SECTION 4
ADJUSTMENTS

4-1. INTRODUCTION

This section contains front-panel calibration procedures and adjustment procedures for the power supply, display driver, analog board, and state trigger board. Table 4-1 lists the table of Recommended Test Equipment.

4-2. CALIBRATION INTERVAL

There is no recommended calibration interval. Adjustment needs are defined by the pass/fail status of resident self-tests and calibration routines. A failure of a SYSTEM menu self test should be followed by resident SYSTEM menu calibration routines 0, 5, and 6 (in this order). The self tests should then be re-selected to check whether the self-calibration routines corrected the error. Repeated failure of a self-test, or failure of a self-calibration routine may dictate the need of a particular hardware adjustment. Refer to table 6-3 in Section 6 for appropriate adjustments.

Certain adjustments should be checked after a repair has been made. Refer to table 6-1 for adjustments needed for a particular board repair. Performance tests that may be affected by these adjustments are also listed in table 6-2.

Always end the adjustment session with SYSTEM menu calibration routines 0, 5, and 6 (in this order), and then perform the SYSTEM menu self tests to assure proper operation of the HP 54201A/D. Although self tests check for correct functional operation, they do not serve as a performance verification. Persistent failure of one of the self tests is an indication of a faulty board; refer to the troubleshooting procedures in this manual.

Note

Allow instrument to warm up for at least 30 minutes prior to beginning front-panel calibration or adjustment procedures.

WARNING

Read the safety summary at the front of this manual before performing adjustment procedures.

CAUTION

The adjustments are performed with the top, bottom, and side covers removed. Use care to avoid shorting or damaging internal parts of the instrument.

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4-3. FRONT-PANEL CALIBRATION

4-4. SYSTEM Calibration Menu

Front-panel calibration allows the user to execute automatic gain, offset, trigger hysteresis, trigger level, and delay calibration for Channel 1 and Channel 2. A rear-panel switch protects the calibration factors from inadvertent changes. This CAL switch must be set to the UNPROTECTED position before executing automatic calibration. Error message "Cal RAM Write Protected" will be displayed if calibration is attempted with the switch in the protected position.

Calibration 0 calibrates gain, offset, trigger hysteresis, and trigger level for Channel 1 and Channel 2 and takes about 4 1/2 minutes to execute. Individual gain and offset calibration for a channel may be executed by choosing 1 or 2 which takes about 1 1/2 minutes each to execute. Calibration 3 selects trigger hysteresis and calibration 4 selects trigger level and take about 15 seconds each to execute. Calibration 5 and 6 calibrate delay for channel 1 and channel 2 and also take about 15 seconds to execute. Calibration 7, 8, and 9 set service default calibration factors and execution is immediate. A normal calibration would require calibrations 0, 5, and 6 (in this order) to be executed. Calibrations 7, 8, and 9 are used for service setup and would be used after a major repair to the instrument for initial setup procedures.

To execute the calibration routines, press the SYSTEM menu key, then press the NEXT/PREV key until the Calibration menu is displayed as shown in figure 4-1. Move the blinking cursor to the Execute Calibration field and enter the number of the routine you wish to execute. Follow the instructions displayed on screen and watch the status line at the end of the calibration to see if the instrument calibrated successfully. An audible beep will be heard when the selected calibration routine is complete.

When front-panel calibration is complete, set the rear-panel CAL switch to the PROTECTED position.

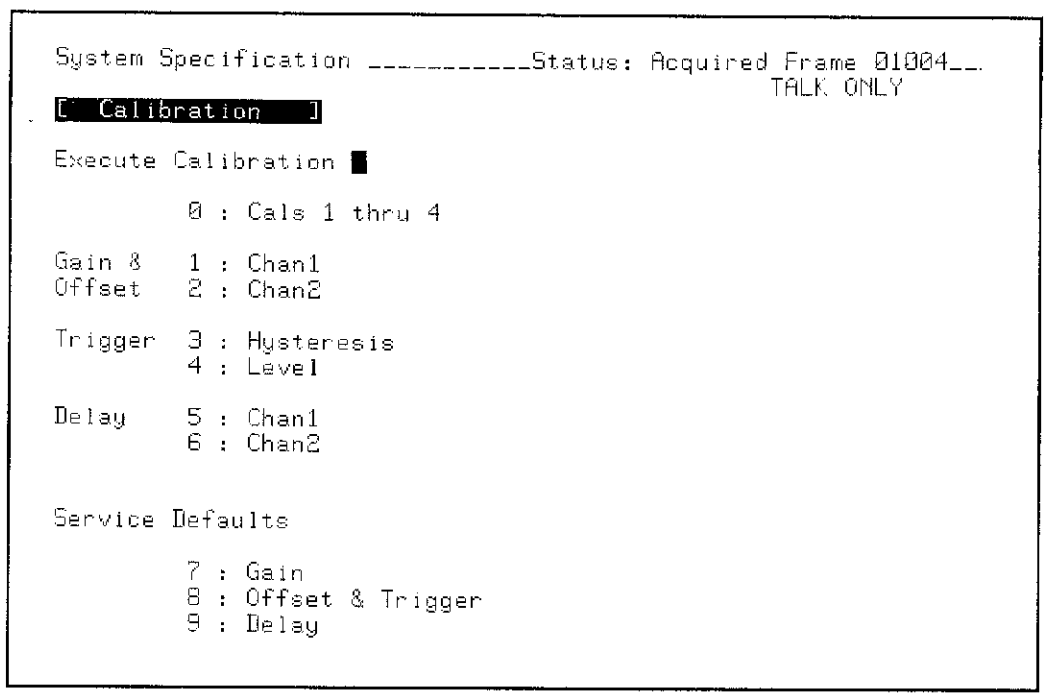


Figure 4-1. SYSTEM Calibration Menu

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4-5. SYSTEM Test & Service Menu Calibration

Execute Service routines 0, 1, and 2 (figure 4-2) provide very precise calibration of time and trigger for the HP 54201A/D, and need only be performed in order to make highly accurate measurements. These procedures are not a part of normal calibration and are not required for the HP 54201A/D to function properly or to meet specifications. These routines should only be performed after SYSTEM Calibrations routines 0, 5, and 6 (in this order) have been performed.

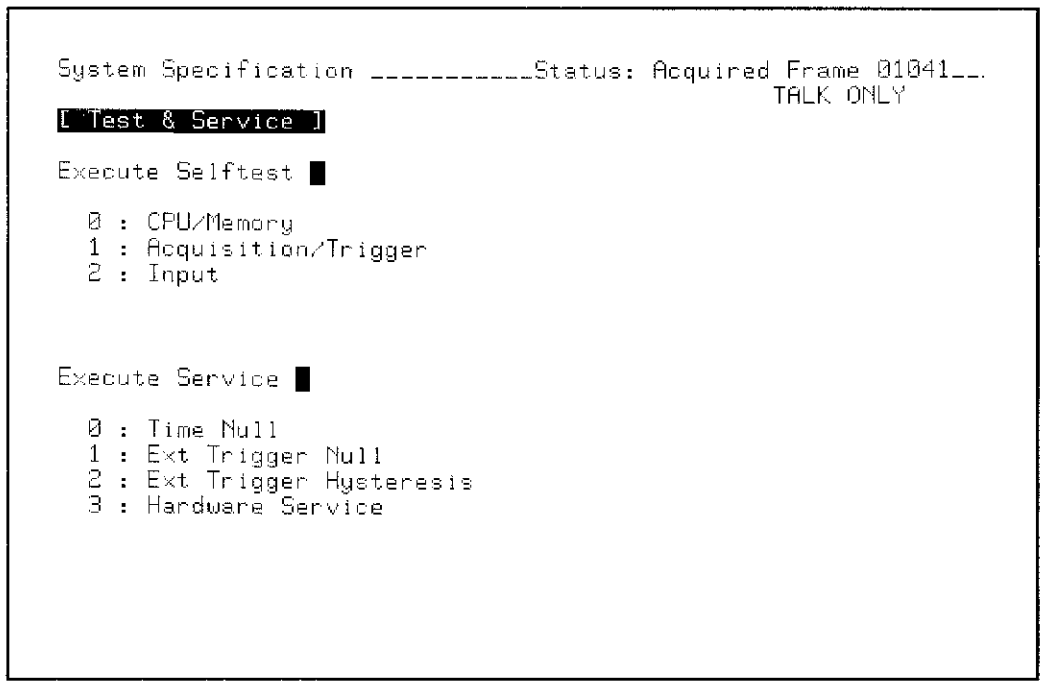


Figure 4-2. SYSTEM Test & Service Menu Calibration

Equipment Required:

Pulse Generator ..... HP 8161A
BNC Tee ..... HP Part No. 1250-0781
BNC(f)-to-BNC(f) Adapter ..... HP Part No. 1250-0080
BNC Cable, 9-inch (Qty 2, matched set) ..... HP 10502
BNC Cable, 48-inch HP10503
Resistive Divider Kit ..... HP 10020A
50Ω Terminator ..... HP 10100C

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TIME NULL

The Time Null routine nulls out very small internal delay differences between the two input channels of the HP 54201A/D.

Equipment Setup:

HP 8161A

Period (PER):	200 ns	
	A Output	B Output
Width (WID):	100 ns	100 ns
Leading Edge (LEE):	1.3 ns	1.3 ns
Trailing Edge (TRE):	1.3 ns	1.3 ns
High Level (HIL):	+4.5 V	+4.5 V
Low Level (LOL):	-0.25 V	-0.25V
Output mode:	Enable	Disable

Procedure:

1. Connect the 9-inch BNC cables to the BNC tee. Connect the 48-inch cable to the BNC tee with the BNC(f)-to-BNC(f) adapter. Connect the other end of the 48-inch cable to the A output of the Pulse Generator. Connect the 9-inch cables to the Channel 1 and Channel 2 inputs of the HP 54201A/D.

2. Press the SYSTEM menu key and press the NEXT/PREV key until the SYSTEM Test & Service menu is displayed.

3. Move the blinking cursor to the Execute Service field and enter 0 for Time Null.

4. Press the INSERT key on the HP 54201A/D to start procedure. The procedure will take about 15 seconds to execute.

EXT TRIGGER NULL

The Ext Trigger Null routine nulls out very small internal delay differences between the EXT TRIG input and the input channels of the HP 54201A/D. This routine should always be performed after the Time Null routine and never as a stand-alone routine.

Equipment Setup: Same as Time Null

Procedure:

1. Move 9-inch BNC cable from Channel 2 input to the EXT TRIG input of the HP 54201A/D.

2. Enter 1 in the Execute Service field for Ext Trigger Null.

3. Press the INSERT key on the HP 54201A/D to start procedure. The procedure will take about 15 seconds to execute.

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EXT TRIGGER HYSTERESIS

The Ext Trigger Hysteresis routine adjusts an internal hysteresis DAC in the HP 54201A/D until the Pulse Generator signal will no longer trigger the instrument.

Equipment Setup:

HP 8161A

Period (PER): 1 μs

	A Output	B Output
Width (WID):	500 ns	500 ns
Leading Edge (LEE):	100 ns	100 ns
Trailing Edge (TRE):	100 ns	100 ns
High Level (HIL):	+400 mV	+400 mV
Low Level (LOL):	-400 mV	-400 mV
Output mode:	Enable	Disable

Procedure:

1. Connect 50Ω terminator to the EXT TRIG input of the HP 54201A/D.
2. Connect the 100:1 divider from the Resistive Divider kit to the kit cable assembly. Connect the BNC adapter tip from the kit to the 100:1 divider.
3. Connect the divider end of the cable to the 50Ω terminator on the EXT TRIG input of the HP 54201A/D, and connect the other end of the cable to the output of the Pulse Generator.
4. Enter 2 in the Execute Service field to select Ext Trig Hysteresis routine.
5. Press the INSERT key on the HP 54201A/D to start procedure. The procedure will take about 15 seconds to execute.

4-6. EQUIPMENT REQUIRED FOR ADJUSTMENTS

Table 4-1 lists the equipment required to adjust the HP 54201A/D. Other equipment may be substituted if it meets or exceeds the critical specifications given in table 4-1.

Table 4-1. Recommended Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED MODEL
Digital Voltmeter	Accuracy: 0.5%	HP 5005B
Pulse Generator	Repetition rate: 100 kHz Transistion time: 1.3 ns Amplitude: 5 V	HP 8161A
Product Support Kit	No substitute	HP Part No. 54200-69501

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After the instrument has warmed up at least 30 minutes, perform a key-down power-up reset. This will preset the HP 54201A/D to a predetermined condition and clear the display memory. Hold any front panel key down while applying power to the instrument. Hold the key down long enough for the power-up tune to be completed.

4-7. POWER SUPPLY ADJUSTMENT

Description:

This procedure checks all dc power supply voltages voltages to ensure they are within limits. These limits apply for any combination of line voltage and instrument board sets.

Equipment Required:

Digital Voltmeter ..... HP 5005B

Equipment Setup:

Set HP 5005B Mode to DC Volts.

Procedure:

1. Disconnect HP 54201A/D power cord and remove top cover.
2. Connect voltmeter ground lead to GND on Power Supply board test connector A1TP2 (figure 4-3).
3. Apply power to HP 54201A/D.
4. Check each of the supplies at A1TP2 with the voltmeter to make sure they are within the following limits:

SUPPLY	LIMITS
+15 V	+14.25 to +15.75V
+12V	+11.4 to +12.6
+5V	+4.75 to +5.25V
-2.4 V	-2.16 to -2.64V
-5.2	-5.2 to -5.7
-12 V	-11.4 to -12.6V

5. Adjust VOLT ADJ (A1R43) if necessary to bring supplies into limit range.
6. Disconnect the HP 54201A/D power cord.

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ADJUSTMENTS

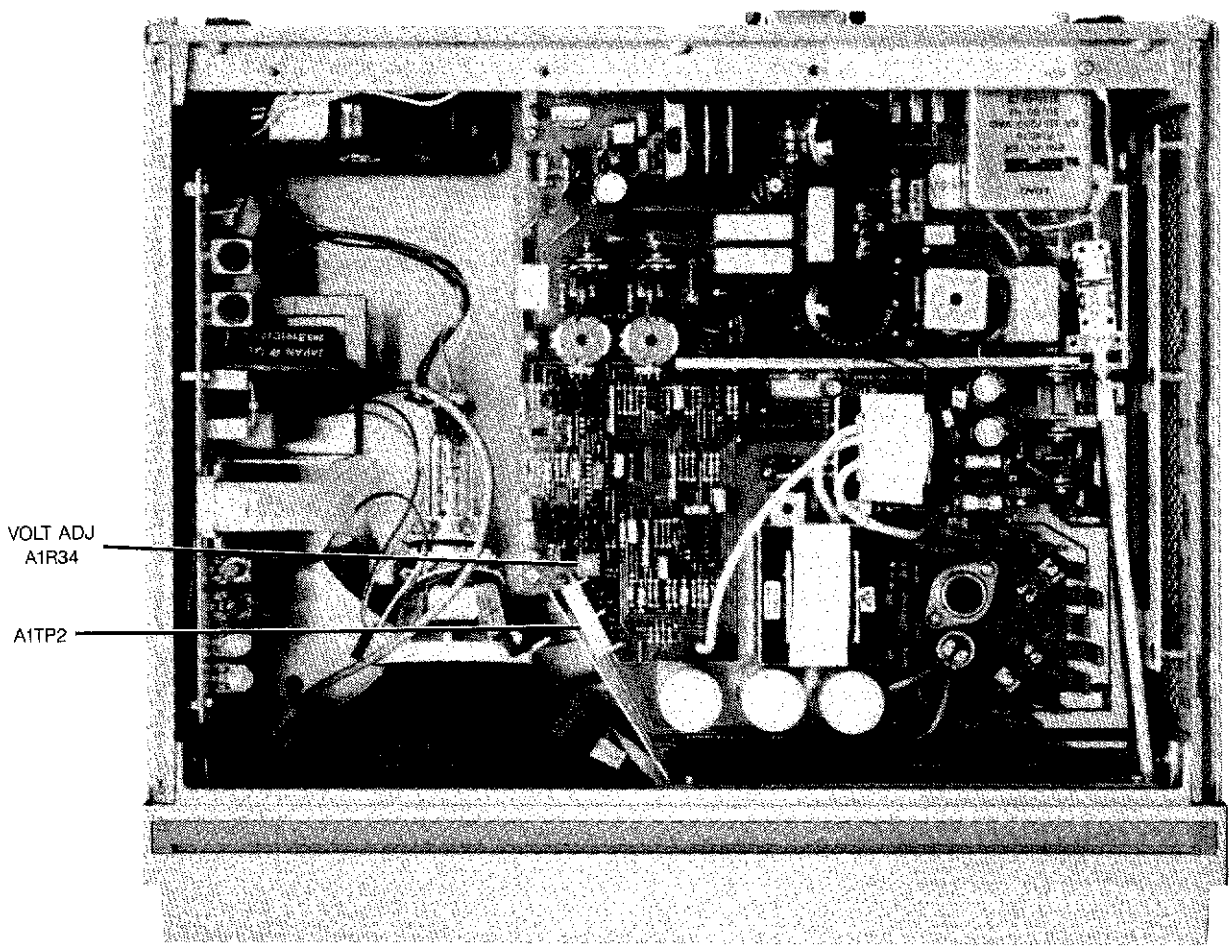


Figure 4-3. Power Supply Adjustment

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ADJUSTMENTS

4-8. DISPLAY SYSTEM ADJUSTMENT

Description:

This procedure is in two parts, yoke adjustment and display driver adjustment. The Yoke adjustment procedure must be must be performed if any part of the Display System is replaced (CRT, display driver, or yoke) or if a display cannot be aligned on the CRT screen using the Display Driver Adjustment Procedure. If the Yoke Adjustment Procedure is performed, the Display Driver Adjustment must then be performed. The Display Driver Adjustment Procedure can be a stand-alone adjustment.

Note

It is recommended the test pattern be used and the Display Driver Adjustments be optimized if necessary to determine the need for the Yoke Adjustment.

WARNING

Hazardous potentials exist on the power supply, the CRT, and on the display driver board. To avoid electrical shock, the following procedures should be closely adhered to.

4-8a. Yoke Adjustment Procedure:

Equipment Required:

None

Procedure:

1. Disconnect power from HP 54201A/D and remove top cover.

2. Before applying power, ensure that yoke is firmly pressed against bell of CRT. If not, loosen yoke neck screw attaching yoke to CRT and slide yoke against CRT. Gently tighten screw until firm.

3. Apply power to HP 54201A/D.

4. Press SYSTEM menu key, then press the NEXT or PREV key until Test & Service menu is displayed. Move blinking cursor to Execute Service field, then enter 3 for Hardware Service.

5. Enter 1 in the Execute Hardware Test field to select display pattern as shown in figure 4-4.

6. Check that display pattern is square with the edges of the CRT. If not, loosen yoke neck screw and rotate yoke to square up the pattern while keeping the yoke firmly pressed against the bell of the CRT. Then gently tighten the screw until firm.

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ADJUSTMENTS

7. Remove power from the HP 54201A/D. Disconnect two yoke connectors from display driver board.

8. While holding flexible straight edge from front lower-left corner to front upper-right corner of CRT, make a mark about one inch long with a water soluble felt pen across center of CRT (figure 4-5).

9. Repeat above step for upper-left corner and lower-right corner, forming an "X" in center of CRT (figure 4-5).

10. Adjust BRIGHTNESS control pot to minimum (full counter-clockwise). See figure 4-6 for display adjustment locations.

11. Apply power to HP 54201A/D.

12. Adjust BRIGHTNESS control pot until a dot appears on CRT.

13. Dot should appear within a 0.3 cm (1/8 inch) radius of intersection of two lines. If not, align dot using centering rings on yoke.

14. Remove power from HP 54201A/D and clean CRT screen with mild soap and water.

15. Reconnect two connectors from yoke to display driver board.

16. Perform Display Driver Adjustment Procedure.

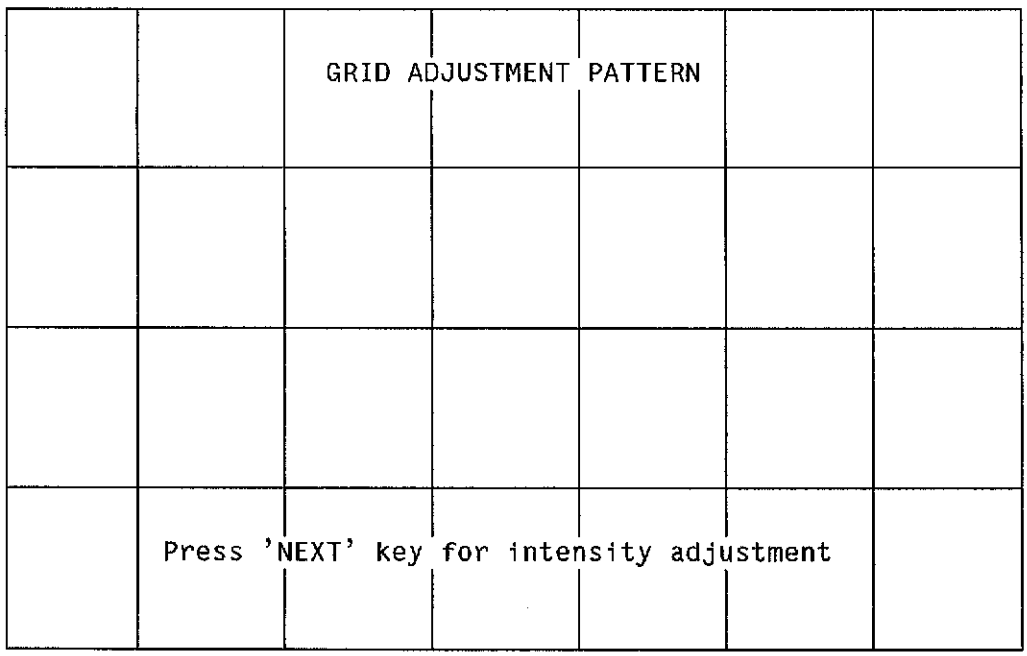


Figure 4-4. Grid Adjustment Pattern

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ADJUSTMENTS

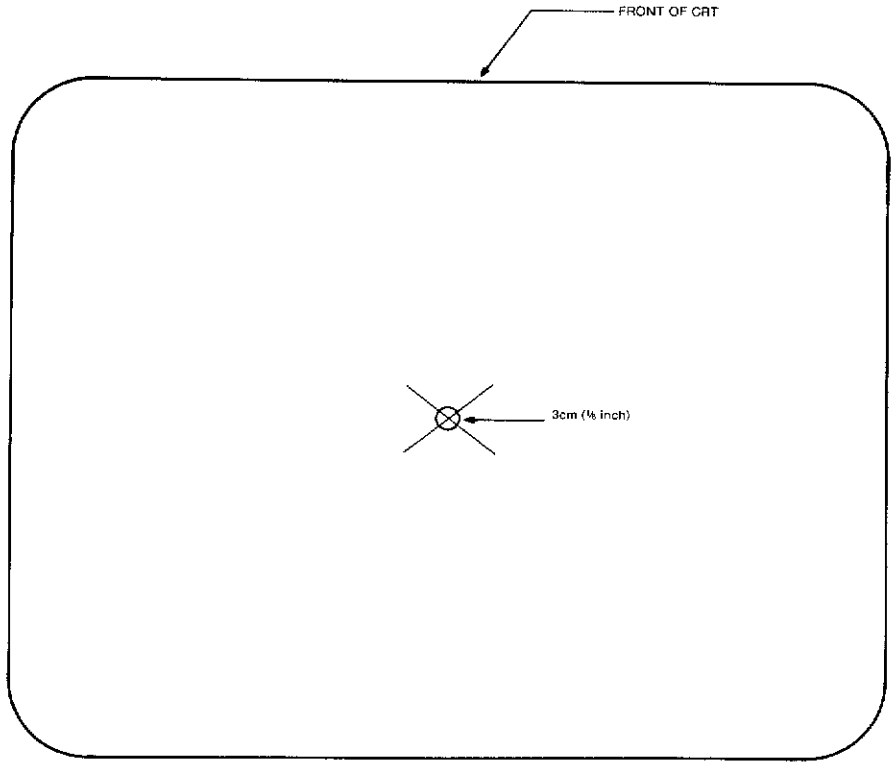


Figure 4-5. Yoke Centering Adjustment.

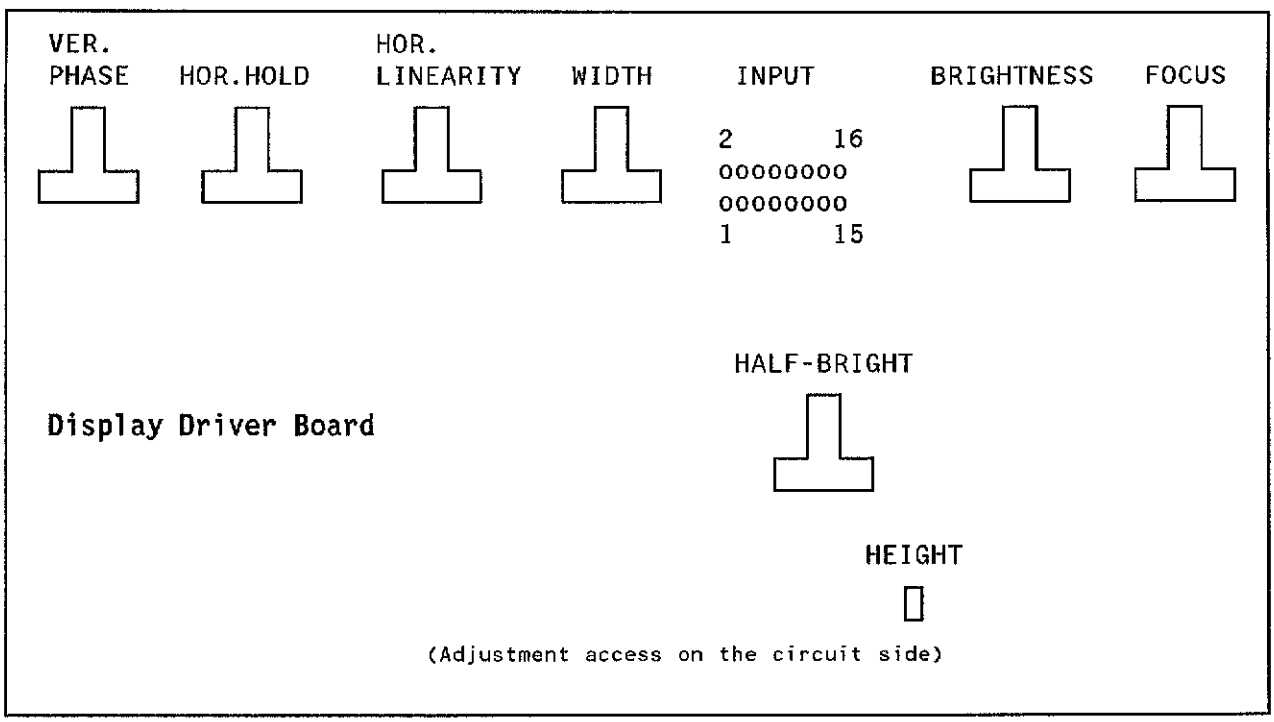


Figure 4-6. Display Adjustment Locations

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ADJUSTMENTS

4-8b. Display Driver Adjustment Procedure:

Equipment Required: None

Procedure:

1. Disconnect power from HP 54201A/D and remove top cover.
2. Remove two screws that attach handle and left side cover to frame. Remove side cover.
3. Apply power to HP 54201A/D.
4. If necessary, adjust BRIGHTNESS control pot until display pattern is visible. See figure 4-6 for display adjustment locations.
5. Press SYSTEM menu key, then press NEXT/PREV key until Test & Service menu is displayed. Move blinking cursor to Execute Service field, then enter 3 for Hardware Service.
6. Enter 1 in Execute Hardware Test field to select Display Pattern as shown in figure 4-7.

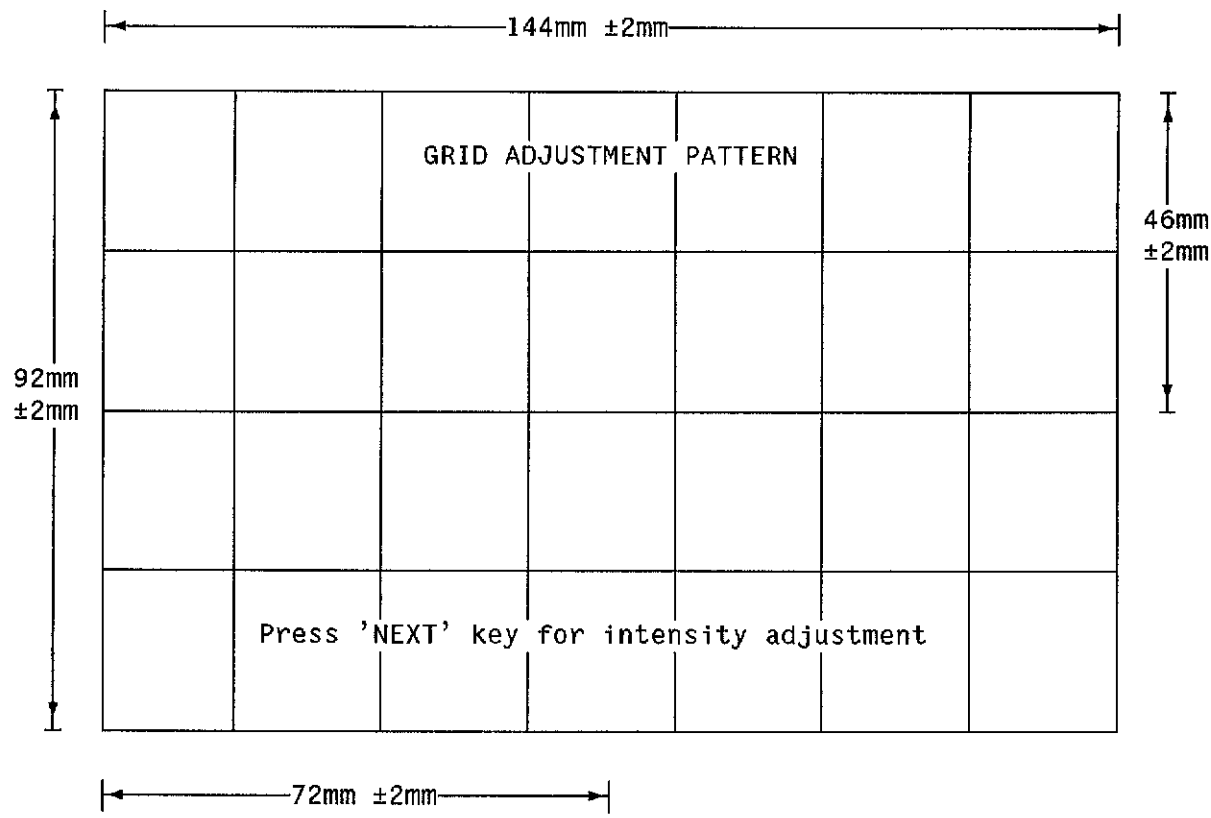


Figure 4-7. Grid Adjustment Pattern

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ADJUSTMENTS

7. Adjust HEIGHT and VER. PHASE (position) until test Test Pattern fills screen vertically.

8. Adjust HOR. LINEARITY until width of each square is the same.

9. Adjust WIDTH until total picture width is same as width of the outer boundary marks shown in figure 4-7. Note that outer edges of the display may NOT align with outer boundary marks.

Note

Adjustments in steps 8 and 9 interact; reiteration of these two steps may be necessary for best results.

10. Now adjust horizontal position by rotating centering rings on yoke. Adjust rings for horizontal movement while minimizing vertical movement of display. Left and right edges should NOW align with outer boundary marks described in previous step.

11. Adjust VER. PHASE to vertically center test pattern (figure 4-7). This should only require minor adjustment.

12. Activate the Intensity Adjust Pattern as shown in figure 4-8 by pressing the NEXT key.

13. If a photometer is available, adjust BRIGHTNESS control until reading of Full Bright area is 39 to 41 foot-lamberts, and adjust HALF-BRIGHT control until reading of Half Bright area is 19 to 21 foot-lamberts. If no photometer is available, adjust to a comfortable viewing level.

14. Adjust FOCUS control to achieve best display in area of test pattern labeled "Focus Area".

15. Verify area of test pattern labeled "Blinking Cursor" does contain a blinking rectangular cursor flashing several times per second. If there are two different video levels but no flashing, CPU board is defective. If there is no difference in video levels, display board is defective.

16. HOR.HOLD adjustment has been pre-adjusted by manufacturer and should not need to be changed.

17. Replace the side cover and top cover on the HP 54201A/D.

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ADJUSTMENTS

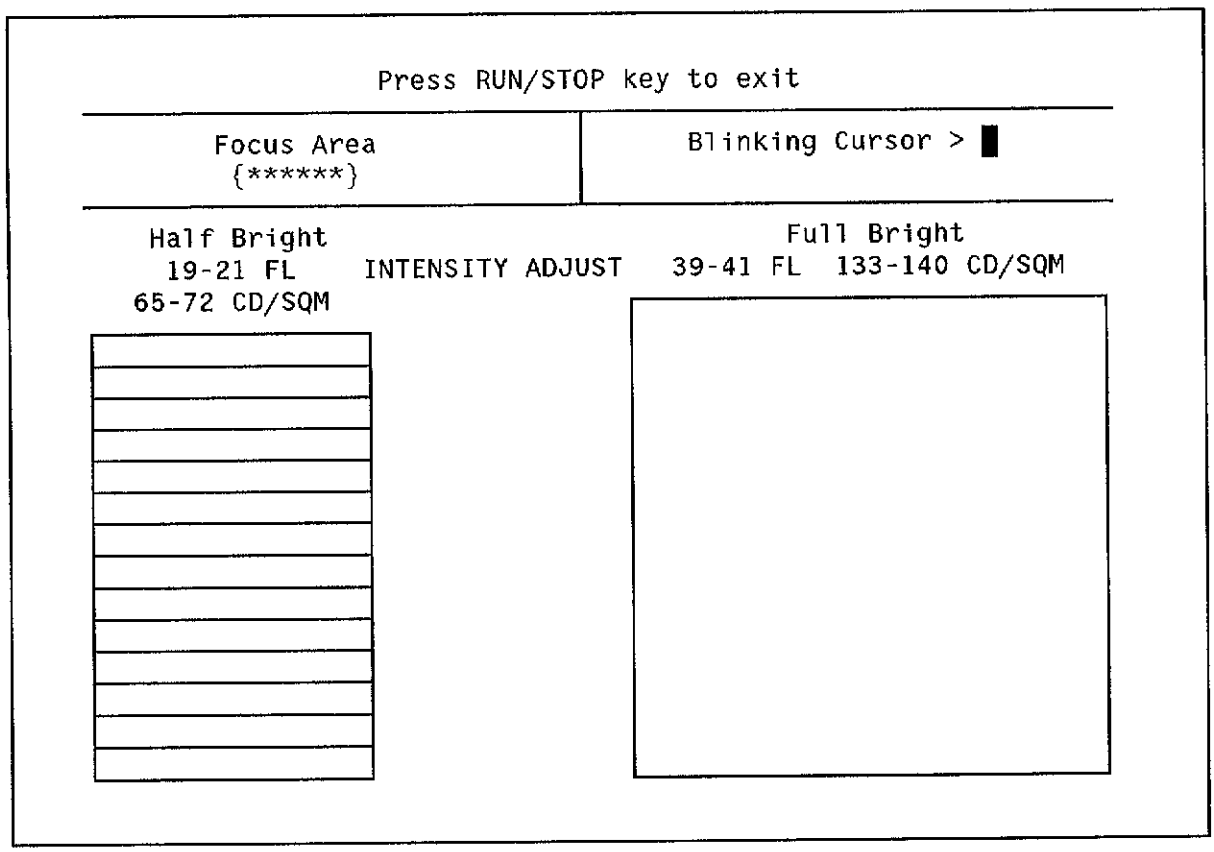


Figure 4-8. Intensity Adjust Pattern

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ADJUSTMENTS

4-9. ANALOG BOARD ADJUSTMENTS

Description:

The following Analog Board procedures adjust: analog amplifiers for proper offset (Offset Adjustment), input attenuator compensation and gain for best square wave response (Input Compensation and Gain Adjustment).

4-9a. Offset Adjustment Procedure:

Equipment Required: None

Procedure:

1. Set HP 54201A/D rear-panel CAL switch in UNPROTECTED position (down).
2. Remove bottom cover and disconnect all inputs.
3. In SYSTEM Calibration menu, select and execute Service Default Gain (7), then execute Service Default Offset & Trigger (8).
4. Configure STATUS Configuration menu as shown in figure 4-9.
5. Display Channel 1 (single graph with grid graticule) and position trace to center graticule using CH1 ZERO OFFSET (A4R239) (figure 4-10).

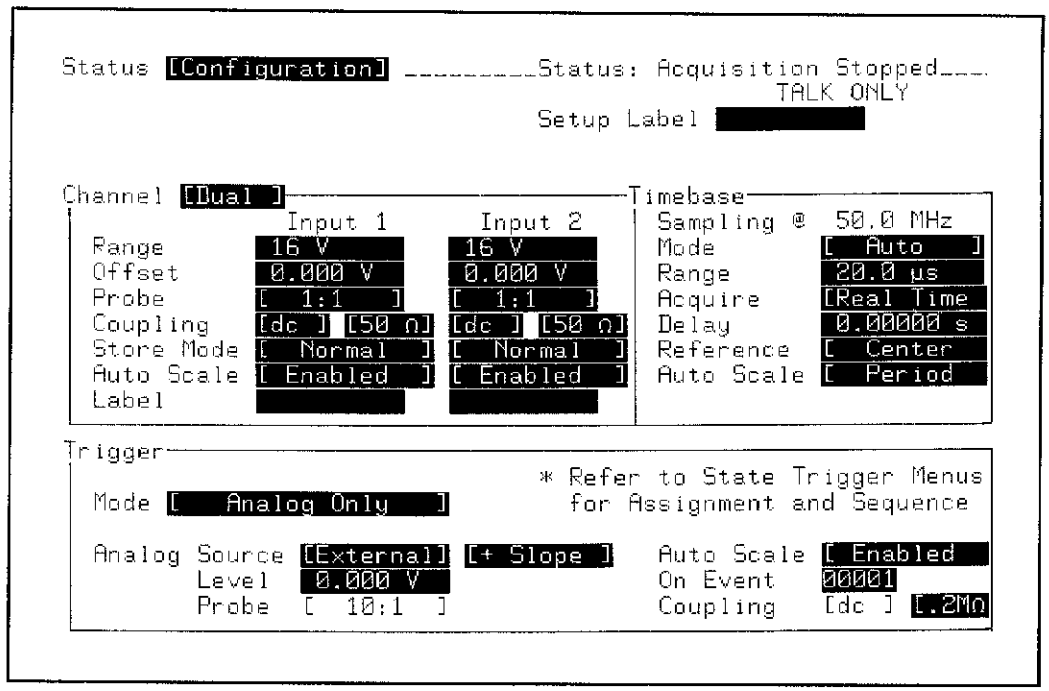


Figure 4-9. HP 54201A/D STATUS Configuration Menu

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ADJUSTMENTS

6. Note position of trace on screen.

7. Select TIME menu and move blinking cursor to Real Time field. Press NEXT key to change field to Repetitive.

8. While switching between Repetitive and Real Time, adjust CH1 DC OFFSET (A4R116) for smallest shift. Dc offset can only be adjusted in Repetitive mode.

9. Switch back to Real Time and repeat steps 5 through 8 for Channel 2 using CH2 ZERO OFFSET (A4R238) and CH2 DC OFFSET (A4R32).

10. Select SYSTEM Calibration menu. Execute Calibration 0 (all gain & offset). Calibration 0 will take about 2 1/2 minutes to execute.

11. When Calibration 0 is complete, set the HP 54201A/D rear-panel CAL switch to the PROTECTED position (up).

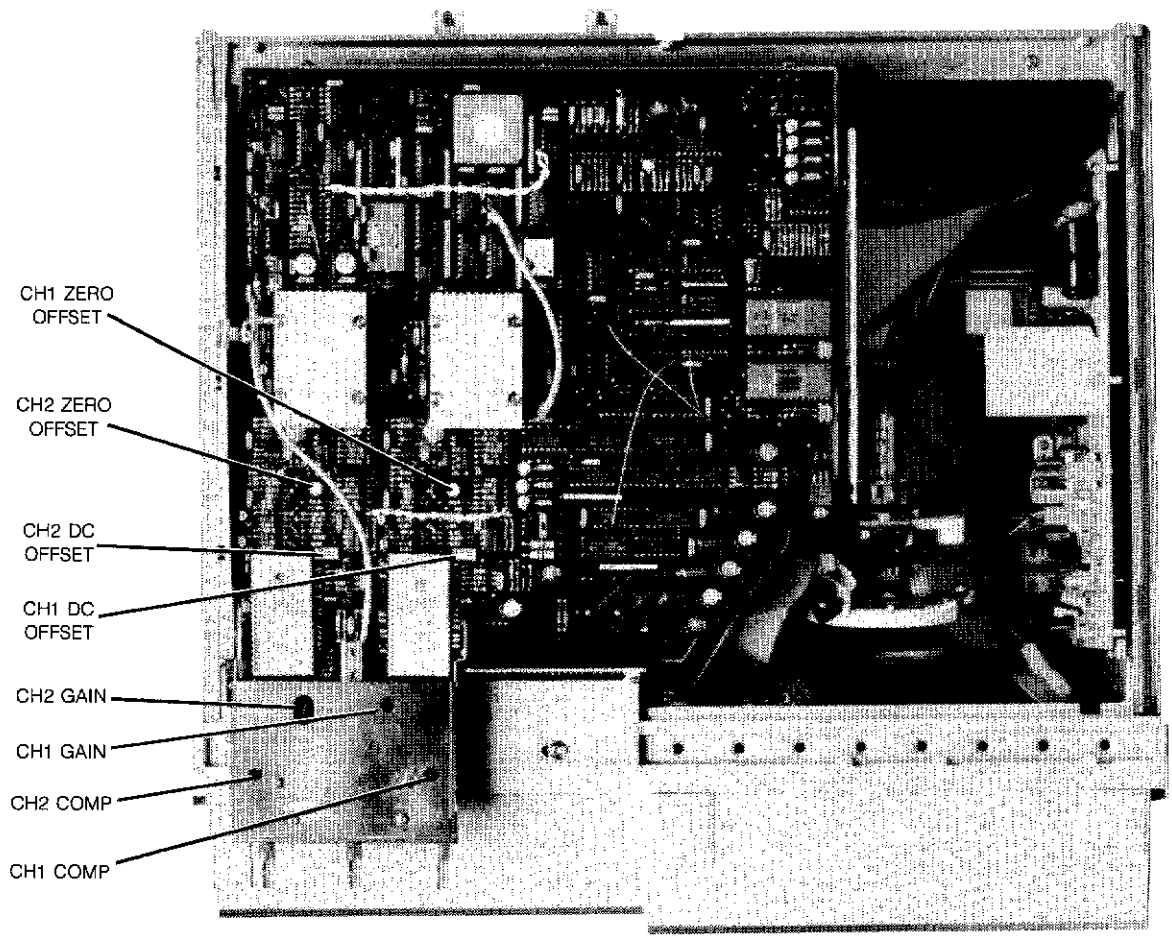


Figure 4-10. Analog Board Adjustment Locations.

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ADJUSTMENTS

4-9b. Input Compensation and Gain Adjustments:

Note

The following procedure adjusts the input compensation and gain of the attenuators, however, these adjustments DO NOT usually drift. It is recommended the input compensation and gain be checked prior to adjustment to determine if adjustment is necessary.

Equipment Required:

Pulse Generator ..... HP 8161A
Product Support Kit ..... HP Part No. 54200-69501

Equipment Setup:

Set HP 8161A A output to 10-kHz square wave, 3 Vp-p, 0 V offset as follows:

Period (PER)	100 μs
	A Output
Width (WID)	50 μs
Leading edge (LEE)	1.3 ns
Trailing edge (TRE)	1.3 ns
High Level (HIL)	1.5 V
Low Level (LOL)	-1.5V
Output	Enable

Procedure:

1. Set HP 54201A/D power OFF and remove Analog Board Assembly (A4). Refer to Analog Board Removal in Section 6.

2. Install Analog Extender Board and Analog Board Support Brackets from Product Support Kit into HP 54201A/D as shown in figure 4-11; then install Analog Board assembly into Extender Board.

3. Set HP 54201A/D power ON.

4. Configure STATUS Configuration menu as shown in figure 4-12.

5. Display Channel 1.

6. Connect pulse generator A output to HP 54201A/D INPUT 1 BNC and adjust CH1 COMP (A4C43) (figure 4-9) for maximum square wave flatness using an insulated adjustment tool.

7. Set pulse generator A output to Period = 2ms and Width = 1 ms (500-Hz square wave).

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ADJUSTMENTS

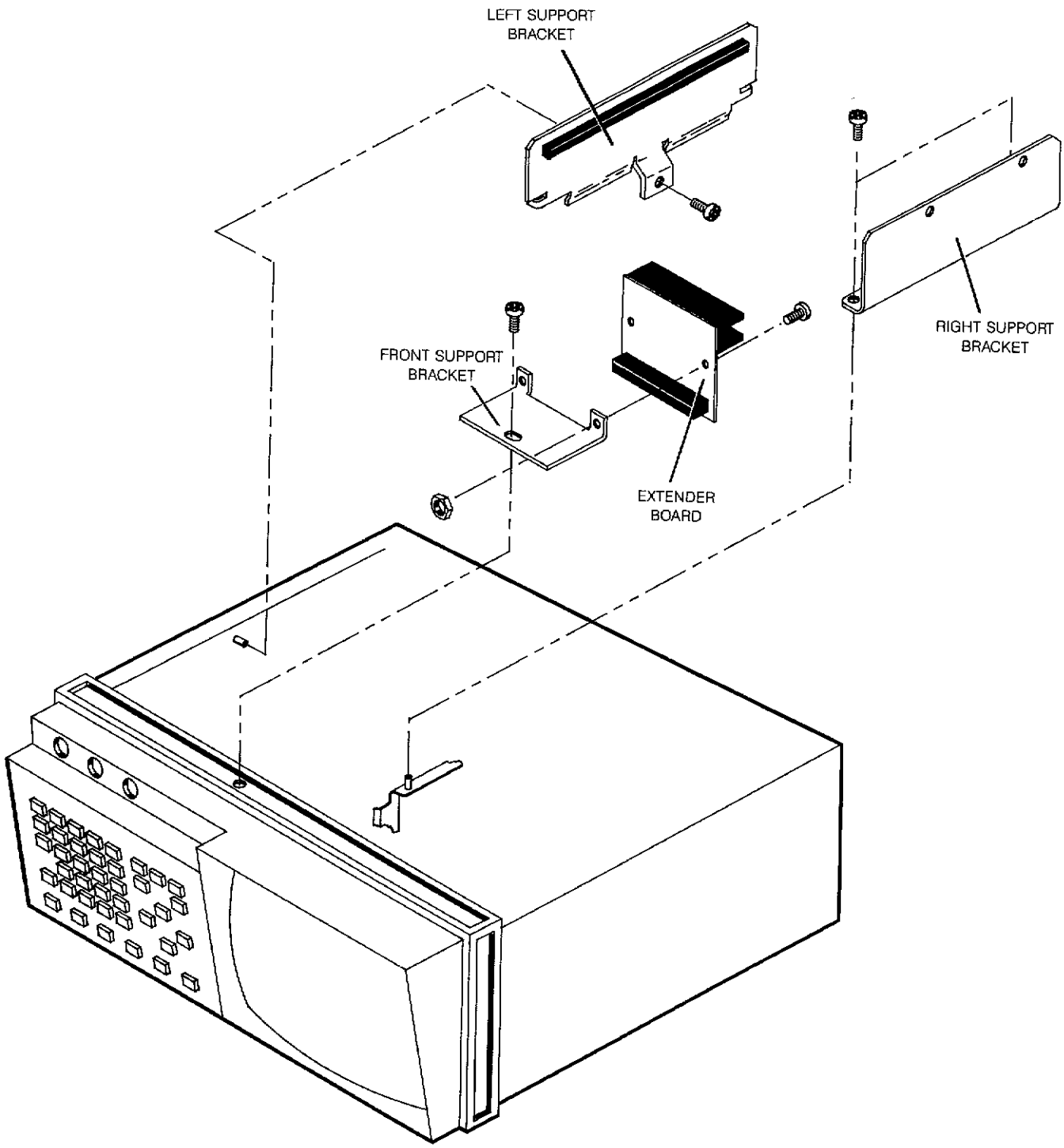


Figure 4-11. HP 54201A/D Product Support Kit Analog Extender Assembly

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ADJUSTMENTS

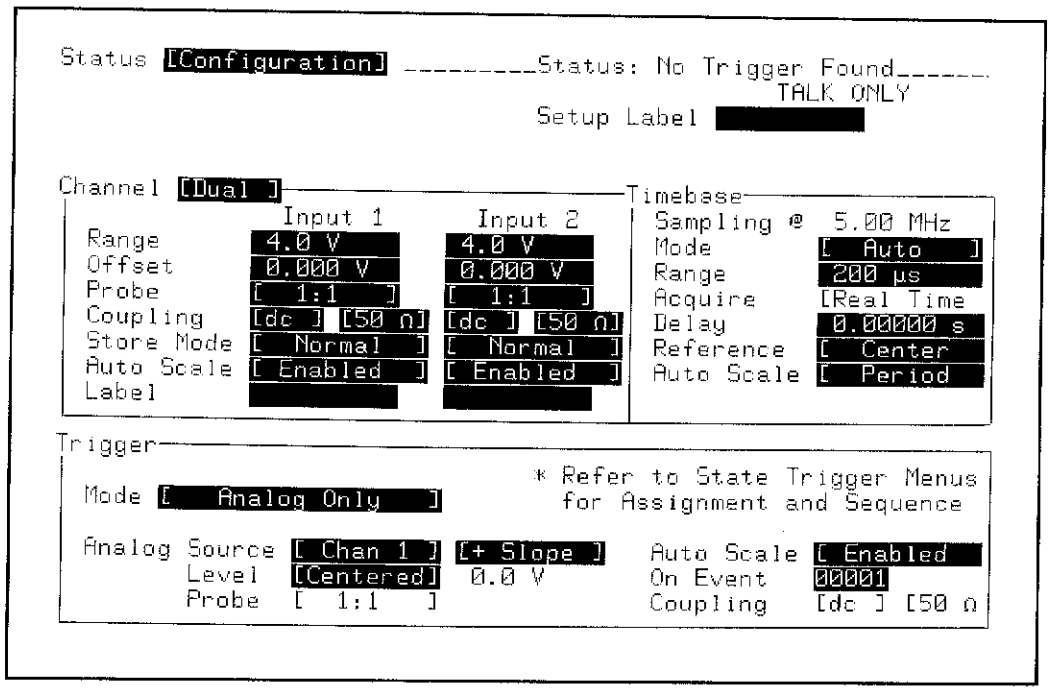


Figure 4-12. HP 54201A/D STATUS Configuration Menu

8. Change HP 54201A/D timebase range to 5 ms.

9. Adjust CH1 GAIN (A4R84) for maximum square wave flatness.

Note

The adjustments in steps 6 and 9 interact; reiteration of these steps may be necessary for best results.

10. Display Channel 2. Change HP 54201A/D trigger source to Channel 2.

11. Set pulse generator A output to Period = 100 µs and Width A = 50 µs (10-kHz square wave).

12. Change HP 54201A/D timebase range to 200 µs.

13. Connect pulse generator A output to HP 54201A/D INPUT 2 BNC. Adjust CH2 COMP (A4C4) (figure 4-9) for maximum square wave flatness.

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ADJUSTMENTS

14. Set pulse generator A output to Period = 2 ms and Width = 1 ms (500-Hz square wave).
15. Change HP 54201A/D timebase range to 5 ms.
16. Adjust CH2 GAIN (A4R13) for maximum square wave flatness.

Note

The adjustments in steps 13 and 16 interact; reiteration of these steps may be necessary for best results.

17. Set HP 54201A/D power to OFF and disconnect power cord.
18. Remove extender board and supports and reinstall Analog Assembly into mainframe.
19. Replace bottom cover on HP 54201A/D.

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ADJUSTMENTS

4-10. STATE TRIGGER BOARD ADJUSTMENT (HP 54201D Only)

Description:

This procedure adjusts the State Trigger Board clock circuitry for proper phase and delay to ensure compliance with setup and hold specifications.

Equipment Required:

Pulse Generator ..... HP 8161A
10:1 Divider Probes (Qty. 2, supplied with HP 54201A/D) ..... HP 10017A
Product Support Kit ..... HP Part No. 54200-69501

Equipment Setup:

Set HP 8161A A output to 100-kHz square wave, 5 Vp-p, 2.5 V offset as follows:

Period (PER)	10 μs
	A Output
Width (WID)	5 μs
Leading edge (LEE)	1.3 ns
Trailing edge (TRE)	1.3 ns
High Level (HIL)	5.0 V
Low Level (LOL)	0 V
Output	Enable

Procedure:

1. Configure STATUS Configuration menu as shown in figure 4-13.
2. Configure TRIG State Assignment menu as shown in figure 4-14.
3. Ensure STATUS Measurement menu is set to Standard Mode.
4. Connect POD 0 to State Board Test Fixture, HP Part No. 54200-63801 (part of Product Support Kit).
5. Connect a BNC cable from CLK BNC on the State Board Test Fixture to output of function generator.
6. Remove cover from right side of HP 54201D.
7. Unscrew and remove the black insulating sleeve from the front of the probes to allow probe tips to fit through the side rail and into the test points. Connect the 10:1 divider probes to State Trigger Board test points as follows (refer to figure 4-15):

   A8TP2 to HP 54201D INPUT 1
   A8TP1 to HP 54201D INPUT 2

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ADJUSTMENTS

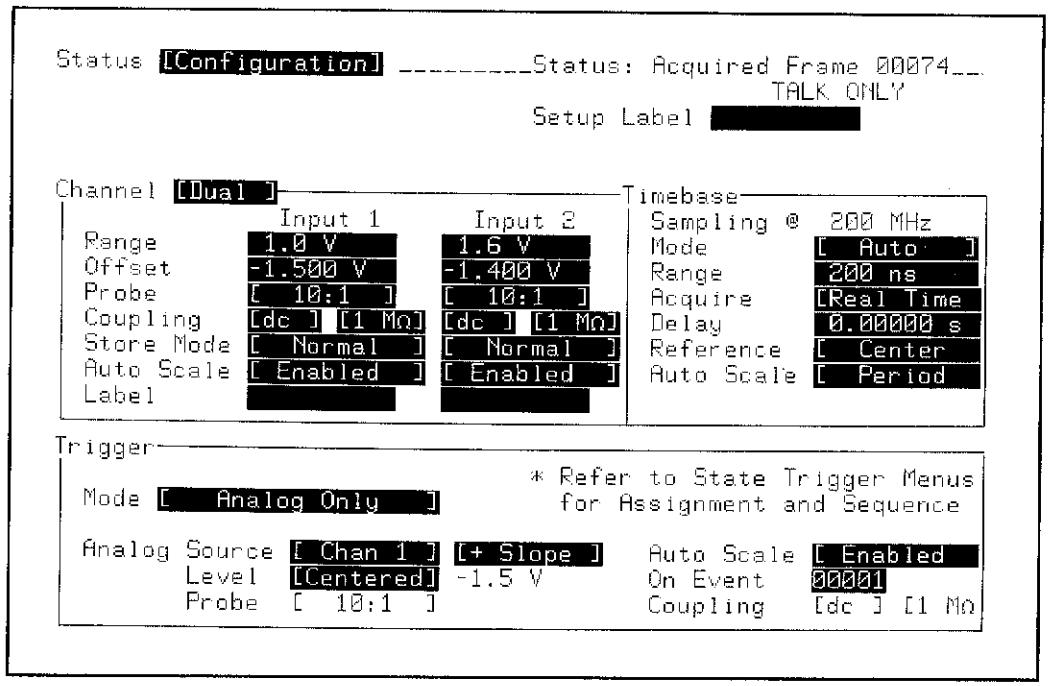


Figure 4-13. HP 54201D STATUS Configuration Menu

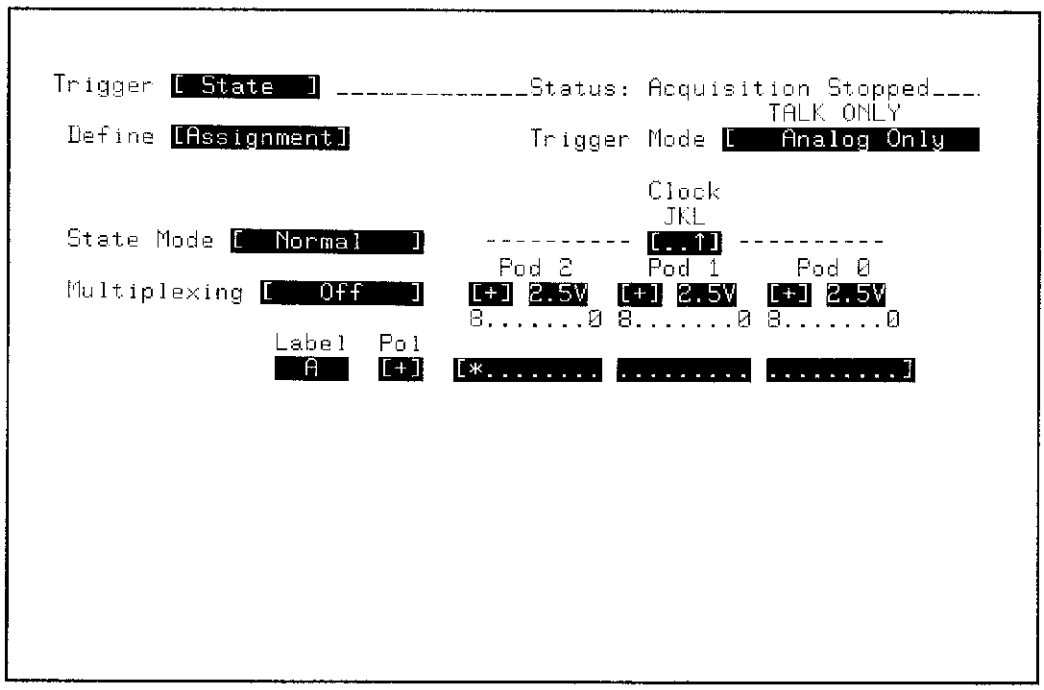


Figure 4-14. HP 54201D TRIG State Assignment Menu

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ADJUSTMENTS

8. Display channel 1 and channel 2. Select front panel measurement DELAY 2 to 1. Display should appear similar to figure 4-16. If triggered waveforms do not appear, adjust HP 54201A/D trigger level.

9. Adjust A8R20 (figure 4-15) until leading edge of ICK (A8TP2) is delayed 42 to 43 ns from leading edge of MCK (A8TP1).

10. Move HP 54201D Input 2 probe from A8TP1 to A8TP3. The display should appear similar to figure 4-17. Adjust A8R28 until DELAY measurement from 2 to 1 is approximately zero seconds (±1 ns).

11. Disconnect probes and replace side cover on HP 54201D.

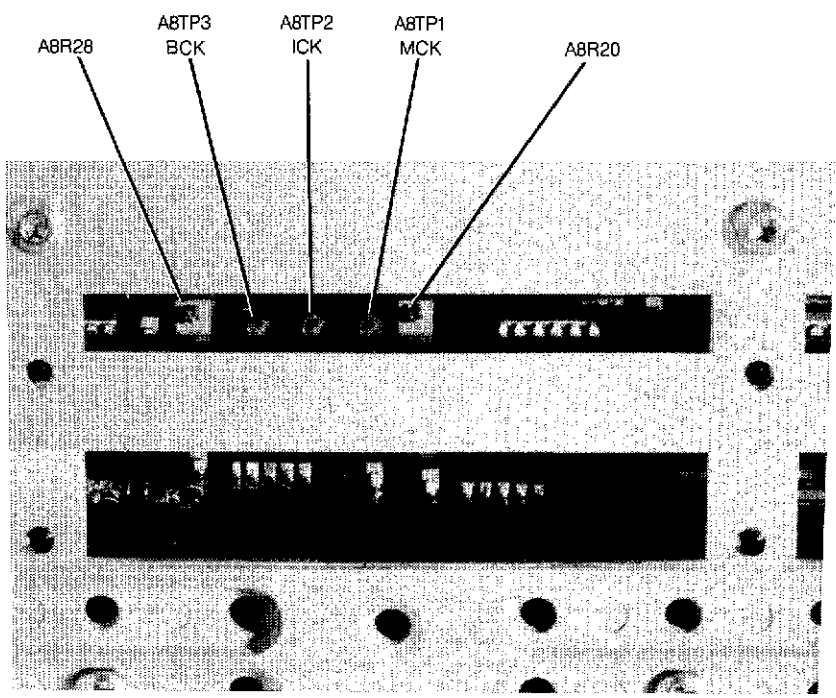


Figure 4-15. State Trigger Board Adjustment Locations

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ADJUSTMENTS

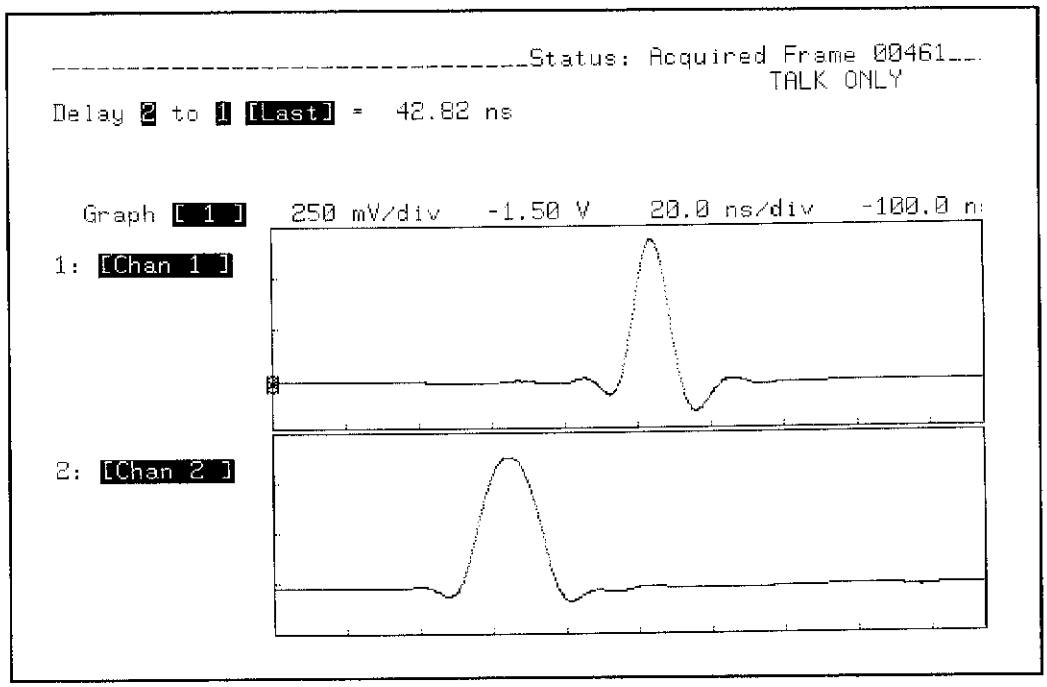


Figure 4-16. A8TP2 to A8TP1 Delay Waveform

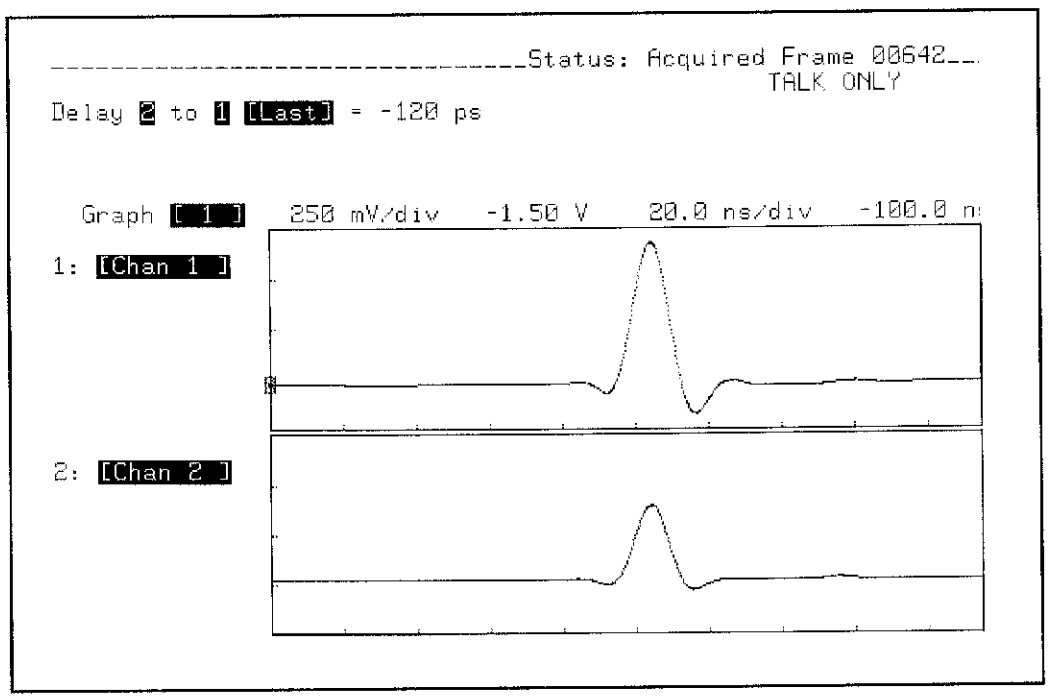


Figure 4-17. A8TP3 to A8TP2 Delay Waveform

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SECTION 5
REPLACEABLE PARTS

5-1. INTRODUCTION

This section contains information for ordering parts. Table 5-1 lists abbreviations used in the parts lists. Table 5-2 lists all replaceable parts in reference designator order. Table 5-3 contains the names and addresses that correspond to the manufacturer code numbers. Figure 5-1 shows the mainframe parts locations.

5-2. ABBREVIATIONS

Table 5-1 lists abbreviations used in the parts lists, the schematics, and throughout this manual. The abbreviations in the parts list are always capital letters. However, in other parts of the manual abbreviations may be used with both lowercase and uppercase letters.

5-3. REPLACEABLE PARTS LIST

Table 5-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Electrical assemblies and their components in alphanumerical order by reference designation.

The information given for each part consists of the following:

a. Reference designation.

b. Hewlett-Packard part number.

c. Part number Check Digit (CD).

d. Total quantity (QTY) in instrument (or on assembly). The total quantity is given only once at the first appearance of the part number in the list.

e. Description of part.

f. Typical manufacturer of part in an identifying five-digit code.

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5-4. ORDERING INFORMATION

To order a part listed in the material lists, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales/Service Office.

To order a part that is not listed in the material lists, include the instrument model number, instrument serial number, a description of the part (including its function), and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

5-5. DIRECT MAIL ORDER SYSTEM

Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

a. Direct ordering and shipment from the Hewlett-Packard Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local Hewlett-Packard office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices.

To provide these advantages, a check or money order must accompany each order.

Mail order forms and specific ordering information are available through your local Hewlett-Packard office. Addresses and phone numbers are located at the back of this manual.

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Table 5-1. Reference Designators and Abbreviations.

REFERENCE DESIGNATORS

A	= assembly	F	= fuse	MP	= mechanical part	U	= integrated circuit
B	= motor	FL	= filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	IC	= integrated circuit	Q	= transistor		
C	= capacitor	J	= jack	R	= resistor	VR	= voltage regulator
CP	= coupler	K	= relay	RT	= thermistor	W	= cable
CR	= diode	L	= inductor	S	= switch	X	= socket
DL	= delay line	LS	= loud speaker	T	= transformer	Y	= crystal
DS	= device signaling (lamp)	M	= meter	TB	= terminal board	Z	= tuned cavity network
E	= misc electronic part	MK	= microphone	TP	= test point		

ABBREVIATIONS

A	= amperes	H	= henries	N/O	= normally open	RMO	= rack mount only
AFC	= automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	= root-mean square
AMPL	= amplifier	HEX	= hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	HR	= hour(s)				
BE CU	= beryllium copper	HZ	= hertz	NPN	= negative-positive-negative	S-B	= slow-blow
BH	= binder head					SCR	= screw
BP	= bandpass	IF	= intermediate freq	NRFR	= not recommended for field replacement	SE	= selenium
BRS	= brass	IMPG	= impregnated			SECT	= section(s)
BWO	= backward wave oscillator	INCD	= incandescent	NSR	= not separately replaceable	SEMICON	= semiconductor
		INCL	= include(s)			SI	= silicon
CCW	= counter-clockwise	INS	= insulation(ed)			SIL	= silver
CER	= ceramic	INT	= internal	OBD	= order by description	SL	= slide
CMO	= cabinet mount only			OH	= oval head	SPG	= spring
COEF	= coeficient	K	= kilo=1000	OX	= oxide	SPL	= special
COM	= common					SST	= stainless steel
COMP	= composition	LH	= left hand			SR	= split ring
COMPL	= complete	LIN	= linear taper	P	= peak	STL	= steel
CONN	= connector	LK WASH	= lock washer	PC	= printed circuit		
CP	= cadmium plate	LOG	= logarithmic taper	PF	= picofarads=10^{-12} farads	TA	= tantalum
CRT	= cathode-ray tube	LPF	= low pass filter			TD	= time delay
CW	= clockwise			PH BRZ	= phosphor bronze	TGL	= toggle
		M	= milli=10^{-3}	PHL	= phillips	THD	= thread
DEPC	= deposited carbon	MEG	= meg=10^{6}	PIV	= peak inverse voltage	TI	= titanium
DR	= drive	MET FLM	= metal film	PNP	= positive-negative-positive	TOL	= tolerance
		MET OX	= metallic oxide			TRIM	= trimmer
ELECT	= electrolytic	MFR	= manufacturer	P/O	= part of	TWT	= traveling wave tube
ENCAP	= encapsulated	MHZ	= mega hertz	POLY	= polystyrene		
EXT	= external	MINAT	= miniature	PORC	= porcelain	U	= micro=10^{-6}
		MOM	= momentary	POS	= position(s)		
F	= farads	MOS	= metal oxide substrate	POT	= potentiometer	VAR	= variable
FH	= flat head	MTG	= mounting	PP	= peak-to-peak	VDCW	= dc working volts
FIL H	= fillister head	MY	= "mylar"	PT	= point		
FXD	= fixed			PWV	= peak working voltage	W/	= with
		N	= nano (10^{-9})			W	= watts
G	= giga (10^{9})	N/C	= normally closed	RECT	= rectifier	WIV	= working inverse voltage
GE	= germanium	NE	= neon	RF	= radio frequency		
GL	= glass	NI PL	= nickel plate	RH	= round head or or right hand	WW	= wirewound
GRD	= grounded					W/O	= without

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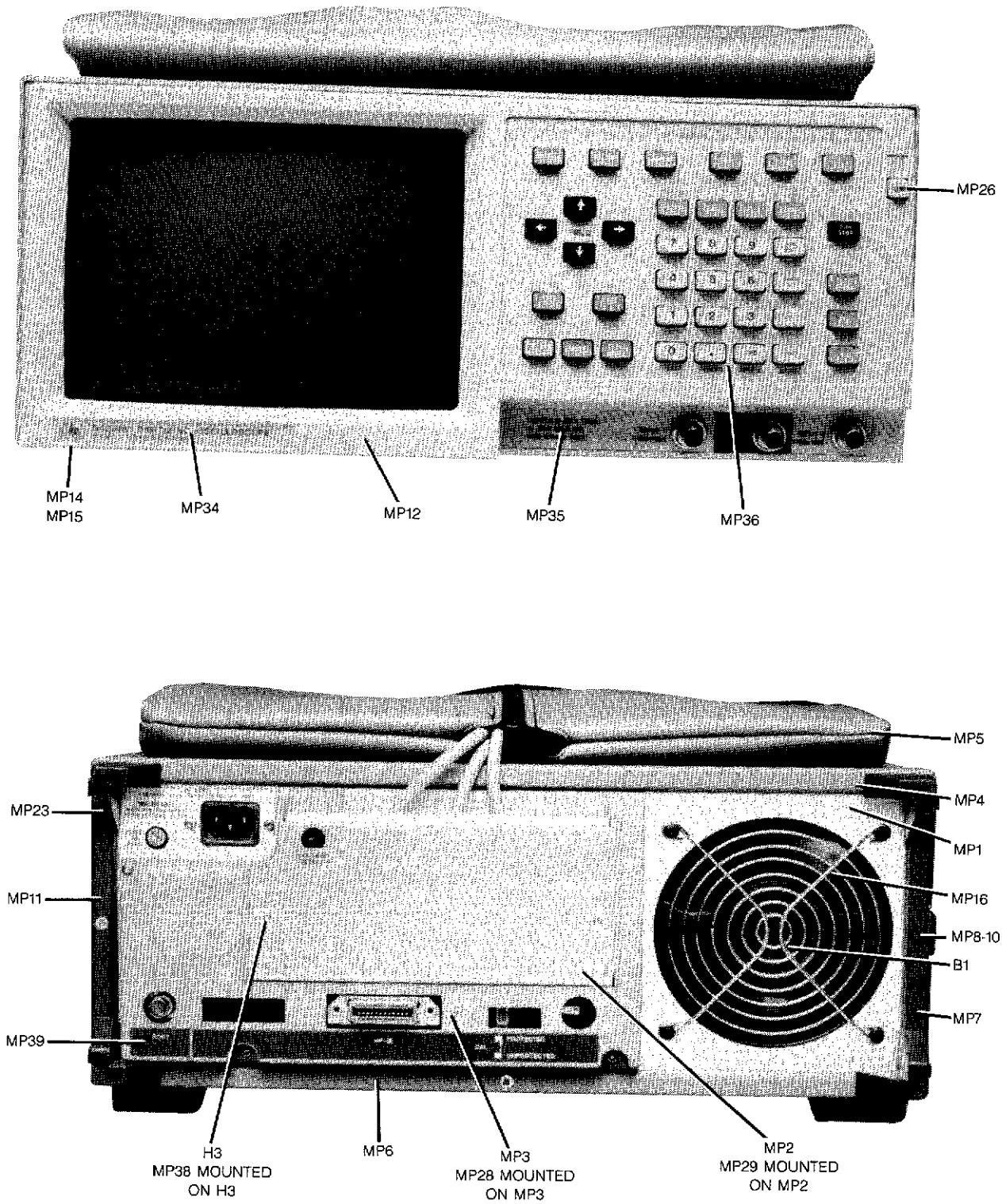


Figure 5-1. Mainframe Parts Location (Sheet 1 of 3)

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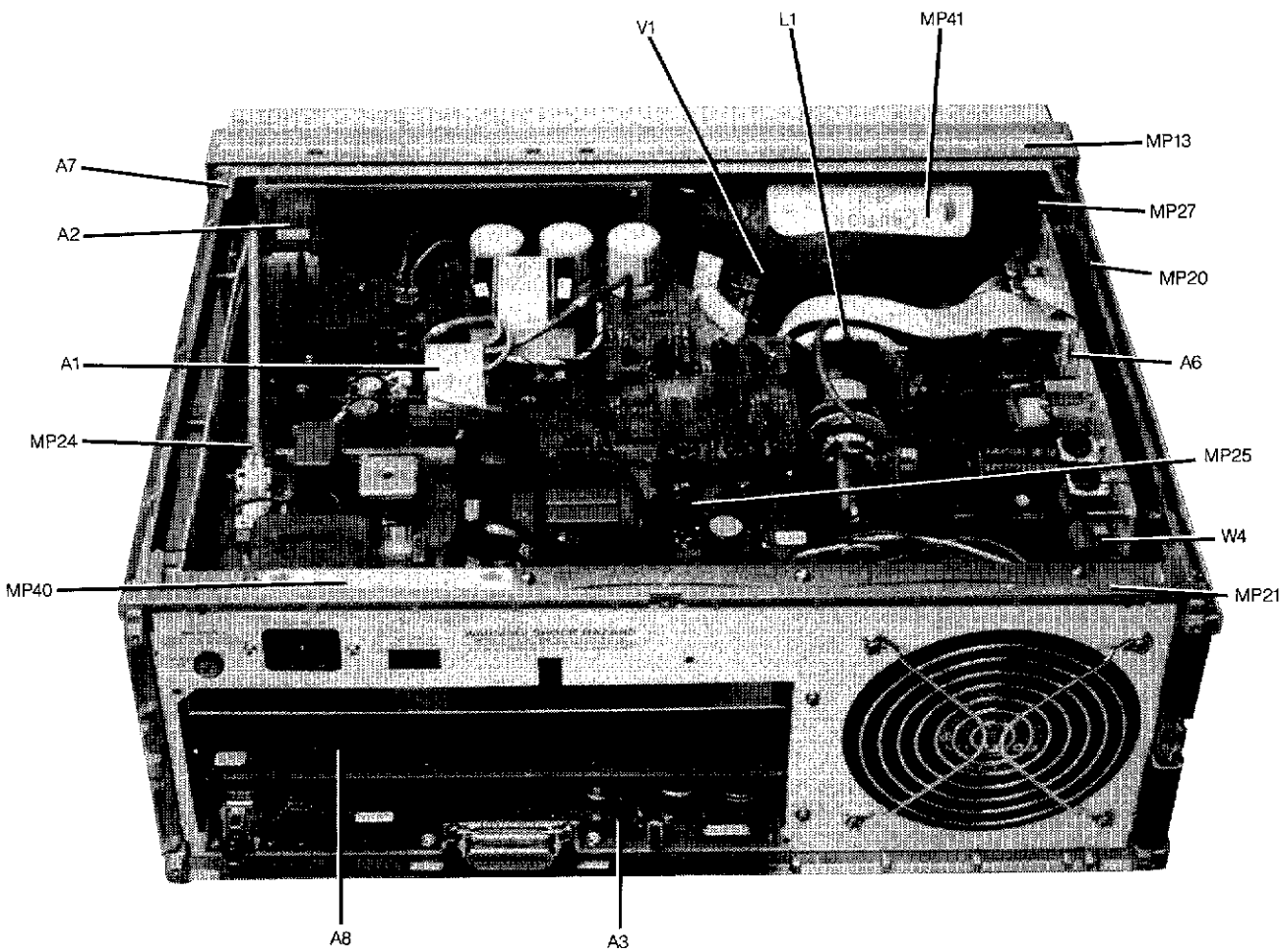


Figure 5-1. Mainframe Parts Location (Sheet 2 of 3)

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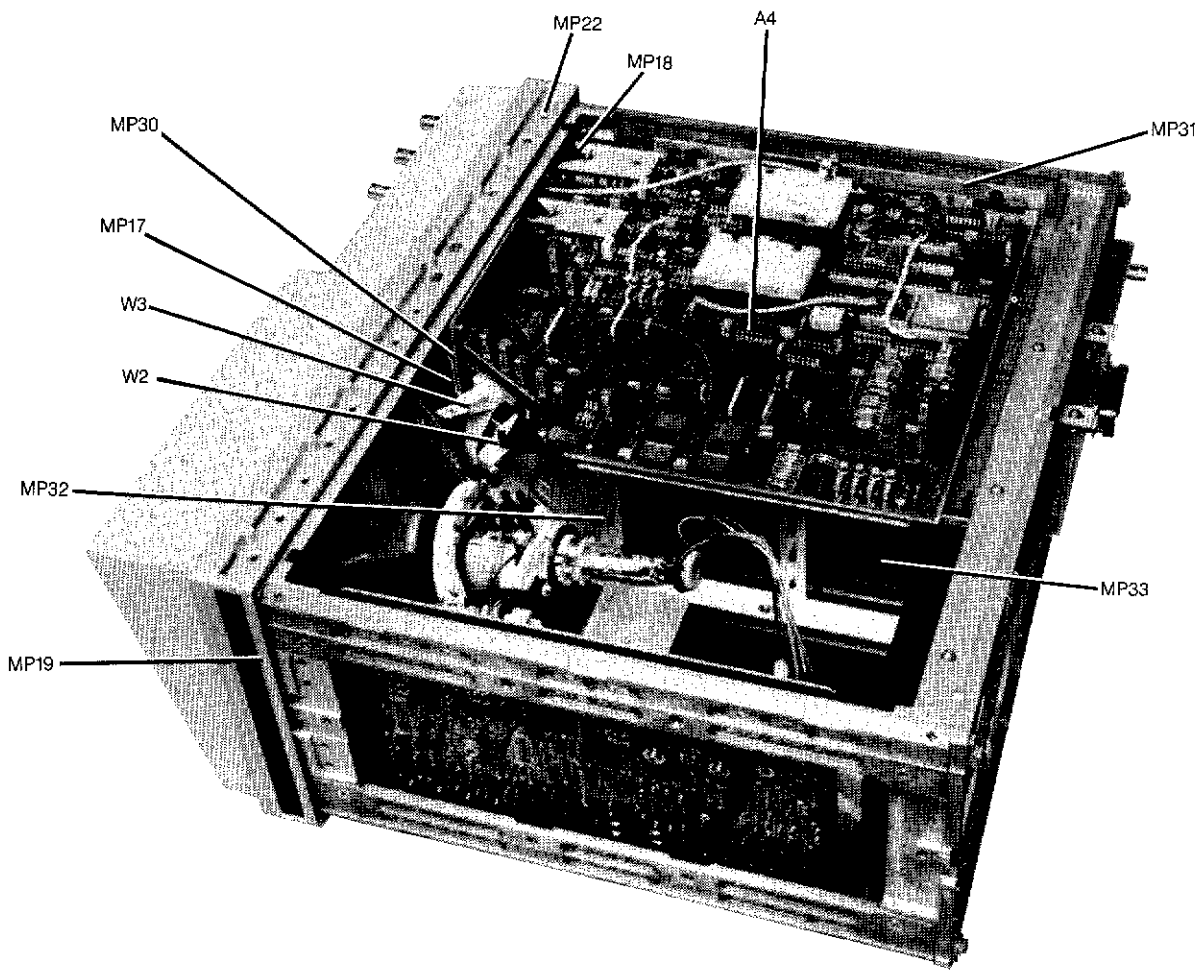


Figure 5-1. Mainframe Parts Location (Sheet 3 of 3)

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Table 5-2. Replaceable Parts

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01630-66529	8	1	POWER SUPPLY BOARD ASSY	28480	01630-66529
A2	54201-66501	6	1	MOTHER BOARD ASSY	28480	54201-66501
A3	54201-69502	3	1	CPU BOARD ASSY	28480	54201-69502
A4	54201-69503	4	1	ANALOG BOARD ASSY	28480	54201-69503
A6	0950-1692	3	1	DISPLAY DRIVER BOARD ASSY	28480	0950-1692
A7	01630-66531	0	1	KEYBOARD BOARD ASSY	28480	01630-66531
A8	54200-69505	5	1	STATE TRIGGER BOARD ASSY (54201D ONLY)	28480	54200-69505
B1	3160-0455	2	1	FAN-TUBEAXIAL 108-CFM 12VDC .6KV DIEL	28480	3160-0455
H1	0515-0430	3	30	SCREW-MACHINE ASSEMBLY M3 X 0.5 6MM-LG	28480	0515-0430
H2	0515-0641	8	12	SCREW-THD-RLG M4 X 0.7 10MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
H3	0570-1171	7	2	SCREW-SPCL 6-32 .468-IN-LG UNCT 100	00000	ORDER BY DESCRIPTION
H4	0590-1611	2	3	NUT-KNRLD-R 1/2-28-THD .094-IN-THK	28480	0590-1611
H5	0624-0598	5	4	SCREW-TPG 8-16 .625-IN-LG PAN-HD-TORX	28480	0624-0598
H6	0624-0520	3	4	SCREW-TPG 6-19 .5-IN-LG PAN-HD-TORX T10	28480	0624-0520
H7	0624-0644	2	4	SCREW-TPG 8-32 .5-IN-LG PAN-HD-TORX T15	28480	0624-0644
H8	0515-1403	2	16	SCREW-MACH M4 X 0.7 8MM-LG 90 DEG-TORX	28480	0515-1403
H9	0515-1384	8	2	SCREW-MACH M5 X 0.8 10MM-LG 90 DEG-TORX	28480	0515-1384
H10	3050-0071	5	1	WASHER-FL MTLC NO. 8 .189-IN-ID	28480	3050-0010
H11	3050-0003	3	4	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
H12	3050-0006	6	3	WASHER-SHLDR NO. 10 .2-IN-ID .5-IN-OD	28480	3050-0006
H13	3050-1016	0	3	WASHER-FL MTLC 1/2 IN .625-IN-ID	28480	3050-1016
H14	0515-0374	4	12	SCREW-MACH M3 X 0.5 10MM-LG	00000	ORDER BY DESCRIPTION
H15	0515-0943	3	13	SCREW-MACH M4 X 0.7 12MM-LG 100 DEG	00000	ORDER BY DESCRIPTION
H16	0515-1035	6	2	SCREW-MACH M3 8MM-LG TORX T10	00000	ORDER BY DESCRIPTION
H17	2190-0476	9	2	WASHER-LK 82 CTSK EXT T NO. 4 .116-IN-ID	28480	2190-0476
H18	0515-1402	1	4	SCREW-MACH M3 X 0.6 8MM-LG PAN-HD-TORX	28480	0515-1402
H19	0515-0365	3	10	SCREW-MACH M2 X 0.4 4MM-LG	00000	ORDER BY DESCRIPTION
H20	0515-0372	2	9	SCREW-MACH M3 X 0.5 8MM-LG	00000	ORDER BY DESCRIPTION
H21	0515-0433	6	1	SCREW-MACH M4 X 0.7 8MM-LG	00000	ORDER BY DESCRIPTION
L1	9140-0720	8	1	YOKE	28480	9140-0720
MP1	01630-00203	5	1	PANEL-REAR	28480	01630-00203
MP2	01630-64103	8	1	REAR DOOR	28480	01630-64103
MP3	01630-44102	5	1	COVER REAR FIN	28480	01630-44102
MP4	01630-04105	4	1	TOP COVER	28480	01630-04104
MP5	01630-84501	2	1	POUCH	28480	01630-84501
MP6	5061-9445	0	1	BOTTOM COVER	28480	5061-9445
MP7	5060-9882	7	1	COVER-SIDE	28480	5060-9882
MP8	5060-9802	1	1	STRAP HANDLE 12	28480	5060-9802
MP9	5041-6819	4	1	CAP-STRP HNDL	28480	5041-6819
MP10	5041-6820	7	1	CAP-STRP HNDL	28480	5041-6820
MP11	5061-9915	5	1	COVER-SIDE PERFORATED	28480	5061-9915
MP12	7101-0694	1	1	BEZEL-FRONT	28480	7101-0694
MP13	5040-7202	9	1	TRIM STRIP-TOP	28480	5040-7202
MP14	5040-7201	8	4	FEET	28480	5040-7201
MP15	1460-1345	5	2	TILT STAND SST	28480	1460-1345
MP16	3160-0092	3	1	FINGER GUARD-FAN	28480	3160-0092
MP17	54201-00603	1	1	SHIELD- POWER SUPPLY	28480	54201-00603
MP18	54201-60601	5	1	SHIELD-ATTENUATOR ASSY	28480	54201-60601
MP19	5001-0440	1	2	TRIM-SIDE	28480	5001-0440
MP20	5021-5835	0	4	STRUT-CORNER	28480	5021-5835
MP21	5021-5806	5	1	FRAME-REAR	28480	5021-5806
MP22	5021-5805	4	1	FRAME-FRONT	28480	5021-5805
MP23	5040-7221	2	4	STANDOFF R PANEL	28480	5040-7221
MP24	5041-3170	4	1	SWITCH SHAFT	28480	5041-3170
MP25	01630-00601	7	1	SHIELD-POWER SUPPLY PLASTIC	28480	01630-00601
MP26	5041-2799	1	1	KEYCAP-LINE	28480	5041-2799
MP27	0360-2109	8	1	GROUND LUG	28480	0360-2109
MP28	8160-0486	4	5	RFI STRIP-FINGERS BE-CU ZINC PLATED	28480	8160-0486
MP29	0403-0179	0	3	BUMPER FOOT-ADH MTG	28480	0403-0179
MP30	54201-01201	3	1	BRACKET-MOTHER BOARD	28480	54201-01201
MP31	01630-01202	6	1	BRKT CD GDE	28480	01630-01202
MP32	01630-01203	7	1	BRKT CTR GDE	28480	01630-01203
MP33	0403-0512	5	10	PC CARD GUIDE	28480	0403-0512
MP34	54201-94303	5	1	LBL IDENT 54201A (54201A ONLY)	28480	54201-94303
MP34	54201-94304	6	1	LBL IDENT 54201D (54201D ONLY)	28480	54201-94304
MP35	54201-94301	3	1	LABEL-FRONT	28480	54201-94301
MP36	54200-94304	5	1	LABEL-KEYBOARD	28480	54200-94304
MP38	0510-0043	4	2	RETAINER-RING E-R EXT .141-IN-DIA STL	28480	0510-0043
MP39	54200-94305	6	1	LABEL-REAR PANEL	28480	54200-94305
MP40	7121-3659	6	1	LABEL-WARNING MYLAR	28480	7121-3659
MP41	7121-4002	5	1	LABEL-CRT CAUTION	28480	7121-4002

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Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
V1	2090-0066	1	1	TUBE-ELECTRON	28480	2090-0066
W1	8120-0696	4	1	CABLE ASSY 3-CNDCT GRA-JKT 7.62-MM-OD AUSTRALIA/NEW ZEALAND	28480	8120-0696
W1	8120-1521	6	1	CABLE ASSY 18AWG 3-CNDCT JGK-JKT 115V USA/CANADA	28480	8120-1521
W1	8120-1692	2	1	CABLE ASSY 3-CNDCT MGP-JKT EUROPEAN CONTINENT	28480	8120-1692
W1	8120-1703	6	1	CABLE ASSY 3-CNDCT MGP-JKT UNITED KINGDOM	28480	8120-1703
W1	8120-2296	4	1	CABLE ASSY 3-CNDCT GRA-JKT SWITZERLAND	28480	8120-2296
W1	8120-2957	4	1	POWER CORD SET 3-COND 2-MM-LG DENMARK	28480	8120-2957
W2	8120-3785	8	1	FLAT RIBBON ASSY 16-COND 12-IN-LG	28480	8120-3785
W3	8120-3784	7	1	FLAT RIBBON ASSY 14-COND	28480	8120-3784
W4	01630-81301	4	1	WR-SGL BLK	28480	01630-81301
A1	01630-66529	6	1	POWER SUPPLY BOARD ASSEMBLY	28480	01630-66529
A1C1	0180-0291	3	14	CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1C2	0180-0291	3		CAPACITOR-FXD 1UF+-10% 35VDC TA	56289	150D105X9035A2
A1C3	0180-2946	9	3	CAPACITOR-FXD 330UF+50-10% 35VDC AL	28480	0180-2946
A1C4	0160-5473	1	10	CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C5	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C6	0160-5347	8	3	CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C7	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C8	0140-0180	5	7	CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C9	0160-5347	8		CAPACITOR-FXD 1.0UF 400VDC	28480	0160-5347
A1C10	0180-3224	8	2	CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C11	0180-3224	8		CAPACITOR-FXD 560MF 200VDC	28480	0180-3224
A1C12	0160-4048	4	1	CAPACITOR-FXD .022UF +-20% 250VAC(RMS)	C0633	PME 271 M 522
A1C13	0160-4962	1	1	CAPACITOR-FXD 1.0UF 250VDC	28480	0160-4962
A1C14	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C15	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C16	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C17	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C18	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C19	0140-0199	8	1	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A1C20	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C21	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C22	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C23	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C24	0160-0164	7	3	CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C25	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C26	0180-2946	9		CAPACITOR-FXD 330UF +50-10% 35VDC AL	28480	0180-2946
A1C27	0160-0164	7		CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C28	0160-0164	7		CAPACITOR-FXD .039UF +-10% 200VDC POLYE	28480	0160-0164
A1C29	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C30	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C31	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C32	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C33	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C34	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 3000VDC MICA	72136	DM19F202G0300WV1CR
A1C35	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C36	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C37	0160-2202	8	1	CAPACITOR-FXD 75PF +-5% 300VDC MICA	28480	0160-2202
A1C38	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C39	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C40	0140-0180	5		CAPACITOR-FXD 2000PF +-2% 300VDC MICA	72136	DM19F202G0300WV1CR
A1C41	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C42	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C43	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C44	0160-5473	1		CAPACITOR-FXD .01UF 400VDC	28480	0160-5473
A1C45	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C46	0180-0291	3		CAPACITOR-FXD 1UF +-10% 35VDC TA	56289	150D105X9035A2
A1C47	0180-3046	2	3	CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1C48	0180-3046	2		CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1C49	0180-3046	2		CAPACITOR-FXD 3300UF +75-10% 6.3VDC AL	28480	0180-3046
A1CR1	1906-0006	9	1	DIODE-FW BRDG 400V 1A	18546	VE48
A1CR2	1901-0719	1	2	DIODE-PWR RECT 400V 3A 300NS	04713	MR854
A1CR3	1901-0719	1		DIODE-PWR RECT 400V 3A 300NS	04713	MR854

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Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1CR4	1906-0224	3	1	DIODE-FW BRDG 600V 25A	04713	MDA2506
A1CR5	1901-0028	5	1	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A1CR6	1901-0050	3	10	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR7	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR8	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR9	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR10	1906-0051	4	1	DIODE-FW BRDG 100V 1A	28480	1906-0051
A1CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR12	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR13	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR14	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR15	1906-0079	6	1	DIODE-FW BRDG 100V 10A	18546	VJ148X
A1CR16	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR17	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
A1CR18	1906-0239	0	1	DIODE-CT-RECT 45V 30A	01281	SD-241
A1CR19	1906-0263	0	1	RFCT VSK 12	28480	1906-0263
A1CR20	1906-0262	9	1	RECT USE 2402	28480	1906-0262
A1DS1	1990-0652	8	1	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
A1E3	2110-0642	3	1	FUSEHOLDER	28480	2110-0642
A1F1	2110-0056	3	1	FUSE 8A 250V NTD 1.25X.25 UL IEC	75915	312006
A1FL1	9135-0175	6	1	FILTER-LINE	28480	9135-0175
A1H1	01830-23201	3	1	COUPLER-SW EXTN	28480	01830-23201
A1H2	0403-0285	9	1	BMPR FT-ADH MTG	28480	0403-0285
A1H3	0515-0372	2	10	SCREW-MACH M3 X 0.5 8MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1H4	0515-1025	4	1	SCREW-MACH M3 X 0.5 28MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1H5	0515-0374	4	2	SCREW-MACH M3 X 0.5 10MM-LG PAN-HD	00000	ORDER BY DESCRIPTION
A1H7	2420-0001	5	1	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
A1H8	3050-0003	3	1	WASHER-FL NM NO. 6 .141-IN-ID .375-IN-OD	28480	3050-0003
A1L1	9140-0624	1	1	INDUCTOR 270UH 10% .725DX.818LG	28480	9140-0624
A1L2	9100-4192	2	1	TRANSFORMER-BALUN	28480	9100-4192
A1MP1	1205-0490	9	4	HEAT SINK 6022BS	28480	1205-0490
A1MP2	2110-0565	9	1	FUSEHOLDER CAP 12A MAX FOR UL	28480	2110-0565
A1MP3	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1MP4	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1MP5	1600-1330	6	1	STIFFENER-PCB	28480	1600-1330
A1MP6	1205-0489	6	2	HEAT SINK 6021BS	28480	1205-0489
A1MP7	1205-0489	6		HEAT SINK 6021BS	28480	1205-0489
A1MP8	1205-0490	9		HEAT SINK 6022BS	28480	1205-0490
A1MP9	1205-0486	3	1	HEAT SINK	28480	1205-0486
A1Q1	1854-0827	1	2	TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1Q2	1854-0827	1		TRANSISTOR NPN SI TO-220AB PD=100W	04713	MJE-13009
A1P1	1251-7986	9	1	CONNECTOR-50 CONTACT (MALE)	28480	1251-7986
A1P2	1251-3675	5	3	CONNECTOR-MALE	28480	1251-3675
A1R1	0757-0394	0	3	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R2	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R3	0698-3615	8	1	RESISTOR 47 5% 2W MO TC=0+-200	27167	FP42-2-TOO-47R0-J
A1R4	0757-0367	7	2	RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R5	0757-0367	7		RESISTOR 100K 1% .5W F TC=0+-100	28480	0757-0367
A1R6	0757-0059	4	1	RESISTOR 1M 1% .5W F TC=0+-100	28480	0757-0059
A1R7	0757-0409	8	2	RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R8	0757-0415	6	2	RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R9	0757-0409	8		RESISTOR 274 1% .125W F TC=0+-100	24546	C4-1/8-TO-274R-F
A1R10	0757-0415	6		RESISTOR 475 1% .125W F TC=0+-100	24546	C4-1/8-TO-475R-F
A1R11	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R12	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R13	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1001-F
A1R14	0757-0442	9	4	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R15	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-TO-51R1-F
A1R16	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-7502-F
A1R17	0757-0437	2	3	RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R18	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-TO-1002-F
A1R19	0698-8959	3	1	RESISTOR 619K 1% .125W F TC=0+-100	28480	0698-8959
A1R20	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R21	0757-0281	4	1	RESISTOR 2.74K 1% .125W F TC=0+-100	24546	C4-1/8-TO-2741-F
A1R22	0757-0441	8	1	RESISTOR 8.25K 1% .125W F TC=0+-100	24546	C4-1/8-TO-8251-F
A1R23	0757-0437	2		RESISTOR 4.75K 1% .125W F TC=0+-100	24546	C4-1/8-TO-4751-F
A1R24	0757-0795	5	1	RESISTOR 75 1% .5W F TC=0+-100	19701	MF-1/2-TO-75R0-F
A1R25	0698-3603	4	3	RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-TOO-12R0-J

See introduction to this section for ordering information

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Table 5-2. Replaceable Parts (Cont'd)

Reference Designator	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R26	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-T00-12R0-J
A1R27	0698-3603	4		RESISTOR 12 5% 2W MO TC=0+-200	27167	FP42-2-T00-12R0-J
A1R28	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R29	0757-0288	1	1	RESISTOR 9.09K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-9091-F
A1R30	0757-0468	9	2	RESISTOR 130K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1303-F
A1R31	0757-0450	9	1	RESISTOR 22.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2212-F
A1R32	0757-0440	7	2	RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A1R33	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R34	2100-3211	7	1	RESISTOR-TRMR 1K 10% C TOP-ADJ 1-TRN	28480	2100-3211
A1R35	0698-8961	7	1	RESISTOR 909K 1% .125W F TC=0+-100	28480	0698-8961
A1R36	0757-0283	6	1	RESISTOR 2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2001-F
A1R37	0698-3160	8	2	RESISTOR 31.6K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3162-F
A1R38	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R39	0757-0459	8		RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5622-F
A1R40	0757-0468	9		RESISTOR 130K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1303-F
A1R41	0757-0440	7		RESISTOR 7.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7501-F
A1R42	0757-0479	2	1	RESISTOR 392K 1% .125W F TC=0+-100	19701	MF4C1/8-T0-3923-F
A1R43	0811-1672	5	1	RESISTOR 3.3 5% 2W PW TC=0+-100	04672	BWH2-3R3-J
A1RP1	1810-0488	8	3	NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP2	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RP3	1810-0488	8		NETWORK-RES 8-SIP4.7K OHM X 4	28480	1810-0488
A1RT3	0837-0172	2	1	THERMISTOR DISC 2.5-OHM	15454	SG-3
A1RV1	0837-0120	0	1	VARISTOR-130VAC	28480	0837-0120
A1RV2	0837-0261	0	1	VARISTOR-220VAC	28480	0837-0261
A1SW1	3101-2582	6	1	SWITCH-SLIDE	28480	3101-2582
A1SW2	3101-2150	4	1	SWITCH-PB DPDT ALTNG 5A 250VAC	28480	3101-2150
A1SW3	3103-0091	2	1	SWITCH-THRM FXD +110C 6A OPN-ON-RISE	28480	3103-0091
A1T1	9100-4271	8	1	TRANSFORMER-CONT	28480	9100-4271
A1T2	9100-4265	0	2	TRANSFORMER-BASE DRIVE	28480	9100-4265
A1T3	9100-4265	0		TRANSFORMER-BASE DRIVE	28480	9100-4265
A1T4	9100-4163	7	1	TRANSFORMER	28480	9100-4163
A1T5	9100-4266	1	1	TRANSFORMER-POWER	28480	9100-4266
A1T6	9100-4267	2	1	CHOKE-COUPLED	28480	9100-4267
A1TP1	1251-3618	6	1	CONNECTOR 2-PIN M POST TYPE	28480	1251-3618
A1TP2	1251-3900	9	1	CONNECTOR 8-PIN F POST TYPE	28480	1251-3900
A1TP3	1251-7826	6		CONNECTOR-MALE	28480	1251-7826
A1U1	1826-0718	0	1	IC-MC1404	28480	1826-0718
A1U2	1820-2111	9	1	IC DRVR TTL INV	01295	SN75468N
A1U3	1826-0468	7	2	IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U4	1826-0468	7		IC COMPARATOR GP 8-DIP-P PKG	04713	MC3423P1
A1U5	1826-0565	5	1	IC-TL494	28480	1826-0565
A1U6	1826-0161	7	1	IC OP AMP GP QUAD 14-DIP-P PKG	04713	MLM324P
A1VR1	1826-0147	9	2	IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR2	1826-0106	0	1	IC 7815 V RGLTR TO-220	04713	MC7815CP
A1VR3	1826-0147	9		IC 7812 V RGLTR TO-220	04713	MC7812CP
A1VR4	1826-0221	0	1	IC V RGLTR TO-220	04713	MC7912CT

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Table 5-3. List of Manufacturer Codes

Mfr No.	Manufacturer Name	Address		Zip Code
C0633	RIFA	BROMMA	SE	
S0167	FUJITSU LTD	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01281	TRW INC SEMICONDUCTOR DIV	LAWNDALE	CA	90260
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
02111	SPECTROL ELECTRONICS CORP	CITY OF IND	CA	91745
02114	FERROXCUBE CORP	SAUGERTIES	NY	12477
03888	K D I PYROFILM CORP	WHIPPANY	NJ	07981
04672	TRW INC PHILADELPHIA DIV	PHILADELPHIA	PA	19108
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
06665	PRECISION MONOLITHICS INC	SANTA CLARA	CA	95050
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
1B546	VARO SEMICONDUCTOR INC	GARLAND	TX	75040
11236	CTS OF BERNE INC	BERNE	IN	46711
15454	AMETEK/RODAN DIV	ANAHEIM	CA	92806
18324	SIGNETICS CORP	SUNNYVALE	CA	94086
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
25403	N.V. PHILIPS-ELCOMA DEPARTMENT	EINDHOVEN	HL	02876
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
27167	CORNING GLASS WORKS (WILMINGTON)	WILMINGTON	NC	28401
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
72136	ELECTRO MOTIVE CORP	FLORENCE	SC	06226
75915	LITTELFUSE INC	DES PLAINES	IL	60016
80031	MEPCO/ELECTRA CORP	MORRISTOWN	NJ	07960

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SECTION 6
SERVICE

6-1. INTRODUCTION

The service section provides removal and installation procedures for HP 54201A/D mainframe components and troubleshooting information for isolating faulty circuit boards.

Service Group 6A at the end of this section provides block and component level theory, troubleshooting and schematic information necessary to service the HP 54201A/D power supply board.

6-2. SAFETY CONSIDERATIONS

Read the Safety Summary at the front of this manual before servicing this instrument. Before performing each procedure, review it for cautions and warnings. For example, when working around the power supply and display circuitry, caution should be taken to avoid potentially lethal voltages.

6-3. LOGIC CONVENTION

Logic states are defined as follows:

0 – False, negated, inactive, or unasserted state.
1 – True, active, or asserted state.

Voltage levels representing logic states:

LOW (L) – The more negative of two voltage levels.
HIGH (H) – The more positive of two voltage levels.

Signals may be either HIGH true, or LOW true, as indicated by the mnemonics on the schematics.

The HP 54201A/D includes both TTL and ECL ICs. Worst case voltage levels for troubleshooting and signature analysis purpose are as follows (IC data sheet specifications may be more accurate):

TTL Voltage Levels

Level	Voltage
LOW	less than 0.8 V
HIGH	greater than 2.0 V

ECL Voltage Levels

Level	Voltage
LOW	less than -1.50 V
HIGH	greater than -1.10 V

6-4. ECL ATTRIBUTES

Because ECL inputs are pulled down inside the IC, an unconnected ECL input is LOW. ECL outputs may be tied together in the same way as open-collector TTL outputs. Thus, they may be wire-ANDed or wire-ORed.

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6-5. REMOVAL AND INSTALLATION OF MAINFRAME COMPONENTS

This section contains removal instructions for the system PC boards and the CRT. Read the Safety Summary at the front of this manual before servicing this instrument. Refer to figure 6-1 for location of HP 54201A/D circuit boards.

WARNING

Hazardous potentials exist on the power supply, the CRT, and on the display driver board. To avoid electrical shock the following procedures should be closely adhered to. Wait at least three minutes for the capacitors on the power supply and display driver boards to discharge before servicing this instrument. Wear safety glasses!!!

CAUTION

Never install or remove any circuit board with the power switched ON. Component damage may occur!!!

Note

When a board is installed verify that it is fully seated into the connector.

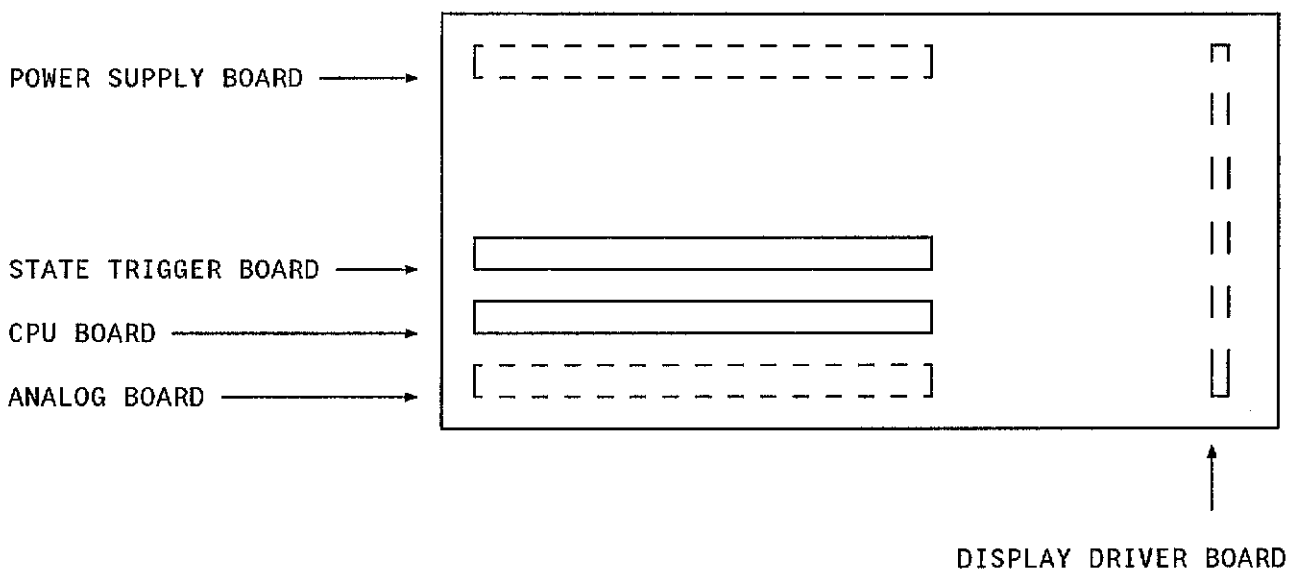


Figure 6-1. HP 54201A/D Circuit Board Location Diagram (Rear View)

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6-6. State Trigger Board Removal (HP 54201D only)

a. Switch power OFF and disconnect AC power cord.

b. Loosen two captive screws securing rear door. Remove rear door.

c. Carefully remove probe cable plugs by pulling on their plastic housing.

d. Remove four screws securing rear cover and remove cover.

e. Carefully remove State Trigger board by inserting board puller from HP 54201A/D Product Support Kit into removal holes located at top-center of board.

The State Trigger board can be installed by reversing removal procedure.

6-7. CPU Board Removal

a. Switch power OFF and disconnect AC power cord.

b. Loosen two captive screws securing rear door. Remove rear door.

c. Carefully remove probe cable plugs (HP 54201D only) by pulling on their plastic housing

d. Remove four screws securing rear cover and remove cover.

e. Remove two screws securing CPU board to rear panel.

f. Remove two plastic standoffs and loosen captive screw securing bottom cover.

g. Carefully tilt instrument on its side and remove bottom cover.

h. Disconnect two cables from the CPU board that go to keyboard and display driver board.

i. Carefully remove CPU board by inserting board puller into appropriate removal holes located at the rear of board.

The CPU board can be installed by reversing CPU board removal procedure.

6-8. Power Supply Board Removal

WARNING

Hazardous voltages are present in the power supply, the CRT, and on the display driver board, even with the main line power switch set in the OFF position and power cord removed. Use extreme caution while servicing the unit with the top cover removed. Wait three minutes for the capacitors on the power supply and display driver boards to discharge to a safe voltage.

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CAUTION

Be certain that the perforated side cover is installed on the right-hand side of the instrument (as you face the front of the unit). If the side covers are mis-installed, insufficient air flow will result and component damage may occur.

a. Switch power OFF and disconnect AC power cord.

b. Loosen two captive screws securing rear door. Remove door.

c. Carefully remove probe cable plugs (HP 54201D only) by pulling on their plastic housing

d. Remove four screws securing rear cover and remove cover.

e. Remove two screws securing CPU board to rear panel.

f. Remove four plastic standoffs and loosen two captive screws securing top and bottom covers, and remove covers.

g. Loosen screw securing perforated side panel and remove.

h. Remove two screws attaching handle and side cover to frame. Remove cover.

i. Carefully tilt instrument on its side and remove four screws holding rear panel to bottom of frame.

j. Disconnect two cables from CPU board that go to keyboard and display driver boards.

k. Lay instrument back on its base. Carefully remove State board (HP54201A/D only) and CPU board from frame by inserting board puller into appropriate removal holes located at rear of each board.

l. CAREFULLY remove power switch shaft with a 1/4 inch wrench.

m. Remove two screws by line plug and two screws securing rear panel to card cage.

n. Remove four screws attaching plastic power supply cover and ground strap to top of frame.

o. Unplug fan from power supply and gently push out on each corner of rear panel from inside of rear panel. Rear panel and fan assembly should remove as one unit.

p. Remove three screws securing power supply board to card cage bracket.

q. Pull Power Supply board straight back from motherboard connector and remove from frame.

The power supply board can be installed by reversing removal procedure. See figure 6-1 for card cage slot for each board.

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6-9. Analog Board Removal

a. Switch power OFF and disconnect AC power cord.

b. Remove two bottom plastic standoffs from rear of instrument.

c. Loosen captive screw securing bottom cover and remove cover.

d. Remove two screws securing Analog board to card cage.

e. Remove three nuts and three washers securing BNC connectors to front panel.

f. Carefully pry up hybrid heat sink clip from card cage.

g. Remove 2 screws from front main frame casting which are directly behind input BNC's.

h. Gently pull analog board back while rocking board from side to side, to separate connector from Motherboard.

i. Pull Analog board back from Motherboard connector, then rotate Analog board slight clockwise while removing from frame.

j. Slide ground shield out from under BNC shield at front of Analog board.

The Analog board can be installed by reversing removal procedure.

6-10. Motherboard Removal

a. Remove State Trigger board (HP 54201D only), CPU board, Power Supply board, and Analog board as detailed previously.

b. Remove six screws that secure motherboard to keyboard cover.

The Motherboard can be installed by reversing removal procedure.

6-11. Keyboard and CRT Removal

WARNING

Hazardous voltages are present in the power supply, the CRT, and on the display driver board, even with the main line power switch set in the OFF position and power cord removed. Use extreme caution while servicing the unit with the top cover removed. Wait three minutes for the capacitors on the power supply and display driver boards to discharge to a safe voltage.

a. Switch power OFF and disconnect AC power cord.

b. Remove four plastic standoffs and loosen two captive screws securing top and bottom covers. Remove covers.

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c. Carefully lay unit in top-down position and remove 4 screws from front panel frame.

d. Carefully lay unit in bottom-down position.

e. Carefully pry up and remove top plastic trim strip from front panel frame and remove screws under trim strip.

f. Slowly peel away two side vinyl adhesive trim strips, being careful not to tear them.

CAUTION

Discharge the post accelerator lead to the grounding lug ONLY. Component damage will occur if discharged to other areas.

Note

The CRT may charge up by itself even while disconnected. Discharge the CRT by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead before handling.

g. Short out charge on CRT by connecting a jumper lead between ground lug of CRT and shaft of a screwdriver. Ground lug is at top left corner of CRT and has black wire attached to it. Slip screwdriver under protective rubber cup of post accelerator lead and then momentarily touch screwdriver to metal clip of post accelerator lead.

h. Disconnect post accelerator lead from CRT by firmly squeezing on rubber cup until metal clip disengages from CRT.

i. Disconnect cable at rear of CRT neck connecting cathode of CRT to display driver board.

j. Disconnect two cables connecting four CRT yoke wires to display driver board.

k. Carefully pull and remove black wire connecting CRT ground lug to display driver board.

l. Remove 3 BNC nuts and washers from front panel.

m. Remove keyboard cable from CPU board.

n. Remove four side screws (two screws on each side) that securing front bezel to frame. These are located under adhesive side trim strips.

o. Carefully pull front bezel (CRT is attached) away from frame being careful not to scratch bezel or break line switch shaft.

p. Remove four screws and washers connecting keyboard to front bezel.

q. Remove four screws and washers connecting CRT to front bezel.

To install the Keyboard and CRT, reverse removal procedure.

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6-12. Display Driver Board Removal

a. Switch power OFF and disconnect AC power cord.

b. Remove two top plastic standoffs from rear of instrument and loosen captive screw securing top cover to frame. Remove top cover.

c. Remove two screws connecting handle and side panel to frame. Remove side cover.

CAUTION

Discharge the post accelerator lead to the grounding lug ONLY. Component damage will occur if discharged to other areas.

Note

The CRT may charge up by itself even while disconnected. Discharge the CRT by shorting the post accelerator terminal of the CRT to the ground lug with a jumper lead before handling.

d. Short out charge on CRT by connecting a jumper lead between ground lug of CRT and shaft of a screwdriver. Ground lug is at top left corner of CRT and has black wire attached to it. Slip screwdriver under protective rubber cup of post accelerator lead and then momentarily touch screwdriver to metal clip of post accelerator lead.

e. Disconnect post accelerator lead from CRT by firmly squeezing on rubber cup until metal clip disengages from CRT.

f. Disconnect cable at rear of CRT neck connecting cathode of CRT to display driver board.

g. Disconnect two cables connecting four CRT yoke wires to display driver board.

h. Carefully pull and remove black wire connecting CRT ground lug to display driver board.

i. Remove six screws mounting display driver board to two corner struts and remove board.

To install the Display Driver board, reverse removal procedure.

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6-13. TROUBLESHOOTING

Troubleshooting faulty circuit boards in the HP 54201A/D is accomplished with covers removed from the HP 54201A/D. All stimulus necessary to troubleshoot the HP 54201A/D is accessed from the keyboard of the HP 54201A/D. No external stimulus is required.

Before entering the troubleshooting procedures, perform all adjustments in Section 4 and execute self-calibration routine 0, 5, and 6 in Section 4.

The HP 54201A/D assembly numbers referenced throughout this section are as follows:

A1 Power Supply Board Assembly
A2 Motherboard Assembly
A3 CPU Board Assembly
A4 Analog Board Assembly
A6 Display Driver Board Assembly
A7 Keyboard Assembly
A8 State Trigger Board Assembly (HP 54201D only)
V1 CRT
L1 CRT Yoke

Service Group 6A at the end of this section provides block and component level theory, troubleshooting and schematic information necessary to service the HP 54201A/D Power Supply board.

These troubleshooting procedures are performed with covers removed from the instrument. Read the Safety Summary at the front of this manual before troubleshooting this instrument.

WARNING

Hazardous potentials exist on the power supply, the CRT, and on the display driver board. To avoid electrical shock the following procedures should be closely adhered to. Wait at least three minutes for the capacitors on the power supply and display driver boards to discharge before servicing this instrument. Wear safety glasses!!!

CAUTION

Never install or remove any circuit board with the power switched ON. Component damage may occur!!!

Note

When a board is installed verify that it is fully seated into the connector.

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6-14. Self Test Failures

The following text assumes the self test functional verification routine from Section 3 has failed and all adjustment and self-calibration routines have been performed. Complete self test documentation is given in Appendix A at the end of this manual.

Self test 0 failed - The CPU board most likely failed, but proceed with troubleshooting flowchart to confirm.

Self test 1 failed Chan1, Chan2, Auto scale, or Interpolator test - The Analog board most likely failed, but proceed with troubleshooting flowchart to confirm.

Self test 1 failed State Pod test (HP 54201D only) - A 1-digit decimal number will be displayed indicating which HP 10271A Pod has failed. If a pod fails, first check to see if the pod connector is fully seated into the State board connector and that the pins on the State board connector are not bent.

NUMBER DISPLAYED	FAILED POD		
	2	1	0
1			■
2		■	
3		■	■
4	■		
5	■		■
6	■	■	
7	■	■	■

Self test 1 failed State Sequence, Qual/Clk, Occurrence, Restart, or Bit Fault test (HP 54201D only). The state board has most likely failed, proceed with troubleshooting flowchart.

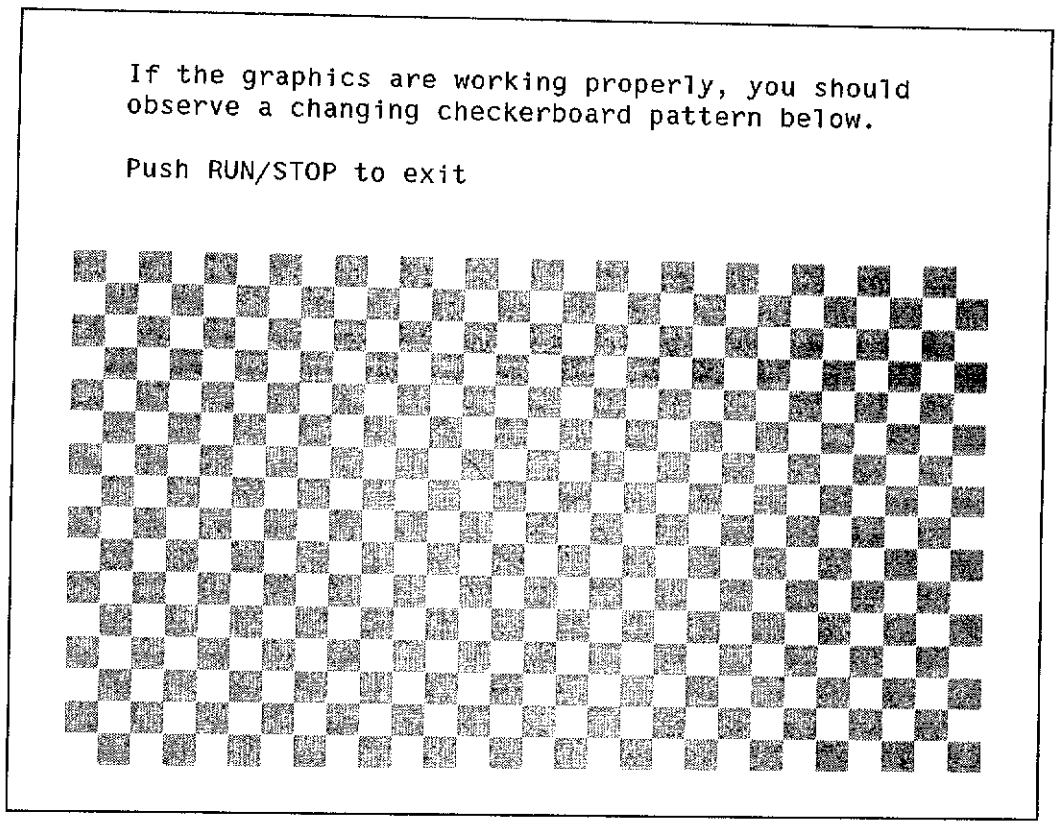
Note

Except for State Occurrence test, all pods must be connected to the HP 54201D for the State and Pod tests to pass.

Self Test 2 failed - The Analog board has most likely failed, however, the signal used for the test comes through the rear-panel BNC and originates on the CPU board. Proceed with troubleshooting flowchart to confirm.

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Graphics Test - This test is accessed from the SYSTEM Test & Service menu. Enter a 3 in the Execute Service field for Hardware Service, then enter 2 in the Execute Hardware Test field to execute the graphics test. When the graphics test is executed, the following graphics pattern will be displayed.



If this test fails, the failure could be in either the CPU board or in the display system assemblies. Go on to the troubleshooting flowchart procedures.

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6-15. Board Replacement

After board replacement, there are certain guidlines to follow to assure the new board is properly calibrated to the system. The 6-1 lists the adjustment step from Section 4 to perform when an assembly has been repaired for replaced. Table 6-2 lists the adjustment step from Section 4 to perform if a performance test from Section 3 fails.

After adjustment, always execute front-panel calibration routines 7 and 8 (service defaults), followed by routines 0, 5, and 6 (in this order).

After self-calibration, execute front panel self tests 0, 1, and 2. Table 6-3 lists which adjustments from Section 4 can affect the pass/fail status of the self tests.

Table 6-1. Assembly Replacement-to-Adjustment Cross Reference

	ASSEMBLY EXCHANGED/REPAIRED							
ADJUSTMENT TO PERFORM AFTER REPLACEMENT	A1	A2	A3	A4	A6	A7	A8	V1/ L1
4-7. Power Supply								
4-8a. Yoke								
4-8b. Display Driver								
4-9a. Offset								
4-9b. Input Comp & Gain								
4-10. State Trigger								

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Table 6-2. Performance Test Failure-to-Adjustment Cross Reference

PERFORMANCE TEST THAT MAY BE AFFECTED BY ADJUSTMENT	ADJUSTMENT STEP					
	4-7	4-8a	4-8b	4-9a	4-9b	4-10
3-6. DC Offset						
3-7. Voltage Measurement						
3-8. Bandwidth						
3-9. Time Measurement						
3-10. Trigger Level-Analog						
3-11. Trigger Sensitivity						
3-12. Setup Time						
3-13. Hold Time						
3-14. Clock Pulse Width						
3-15. Clock Repetition Rate						
3-16. Minimum Input						
3-17. Threshold Accuracy						

Table 6-3. Self-Test/Adjustment Interaction

ASSEMBLY	ADJUSTMENT	SELF TEST		
		0	1	2
Power Supply	4-7	N	N	N
Display System	4-8	N	N	N
Analog	4-9a	N	N	N
	4-9b	N	Y	Y
State Trigger	4-10	N	N	N

N = Adjustment does not affect pass/fail status of self-test

Y = Adjustment affects pass/fail status of self-test. If self test fails, this adjustment should be checked.

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6-16. Product Support Kit

Table 6-4 is a list of the components contained in the Product Support Kit, HP Part No. 54200-69501 (used with HP 54200A/D and HP 54201A/D).

Table 6-4. Product Support Kit Parts List

DESCRIPTION	HP PART NO
PC BOARD EXTRACTOR	0403-0493
STATE BOARD TEST FIXTURE	54200-63801
SERVICE SLOT SUPPORT BRACKET-LEFT	5001-3575
SERVICE SLOT SUPPORT BRACKET-RIGHT	5001-3576
SERVICE SLOT EXTENDER BOARD	01630-66550
ANALOG BD SUPPORT BRACKET-LEFT	5001-3577
ANALOG BD SUPPORT BRACKET-RIGHT	5001-3578
ANALOG BD SUPPORT BRACKET-FRONT	5001-3579
ANALOG EXTENDER BOARD	5061-6136
SERVICE SOFTWARE *	54200-12001 *
ANALOG BRACKET INSTRUCTIONS *	5958-3781 *
SERVICE BRACKET INSTRUCTIONS *	5958-3782 *
* Used for HP 54200A/D only	

6-17. ANALOG BOARD EXTENDER. The analog board is extended into the service position by using the following steps:

1. Set HP 54201A/D power OFF and remove Analog board.
2. Install Analog Extender Board and Analog board support brackets into HP 54201A/D as shown in figure 6-2.
3. Install Analog board into extender board.

6-18. SERVICE SLOT EXTENDER. The Service Slot Extender allows signals from the motherboard to be monitored, and allows the CPU board and State board (HP 54201A/D only) to be extended from the instrument for servicing. Install the extender by using the following steps:

1. Set HP 54201A/D power OFF.
2. Loosen captive screw securing top cover to instrument and remove cover.
3. Insert Service Slot Extender board into connector on motherboard as shown in figure 6-3.
4. Carefully pry up and remove top plastic trim strip from front panel frame.
5. Install left and right service slot support brackets into instrument as shown in figure 6-3.
6. Remove desired board from mainframe and slide into position on service slot extender board.

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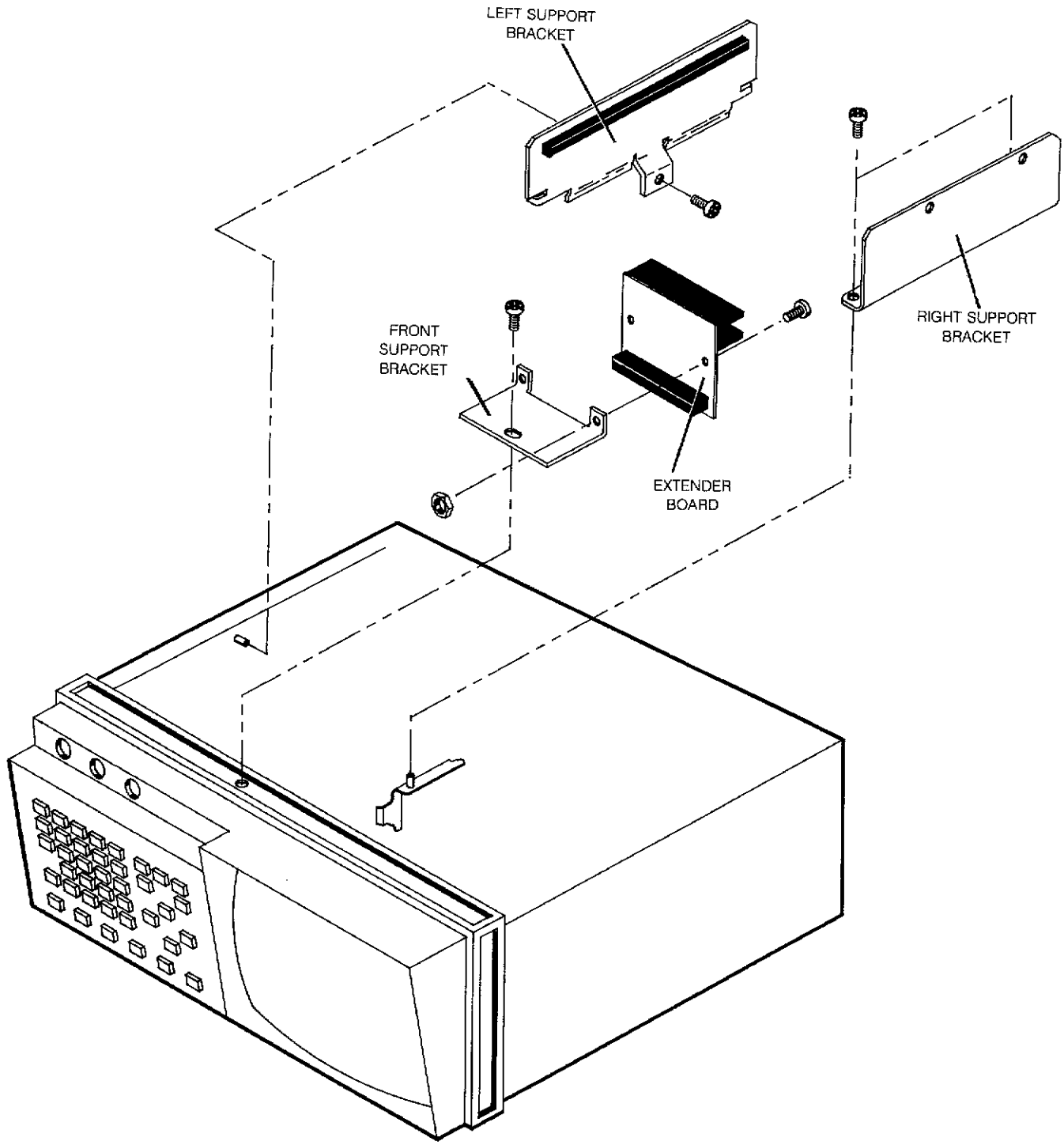


Figure 6-2. Analog Board Extender Assembly

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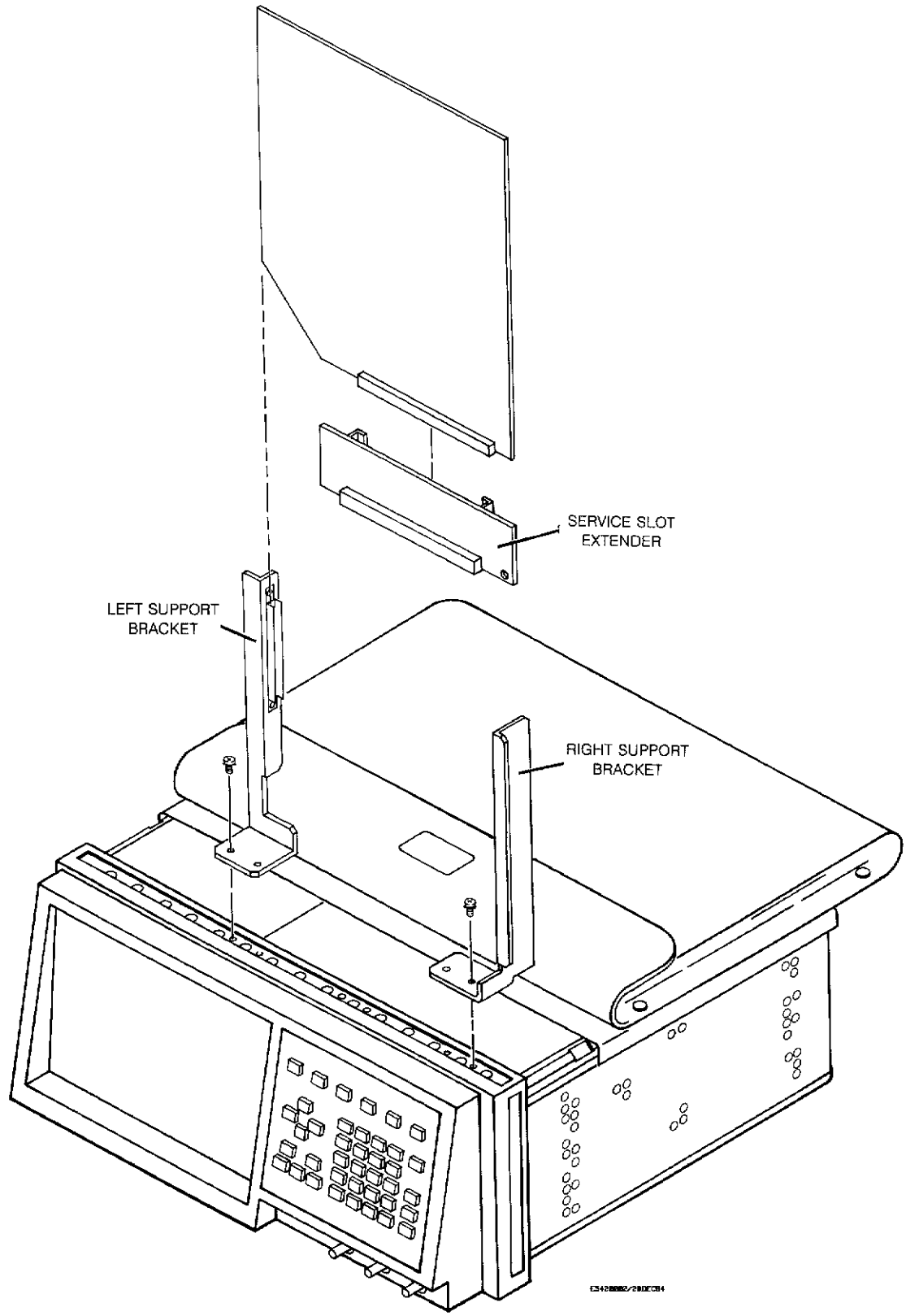


Figure 6-3. Service Slot Extender Assembly

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6-19. Key-Down Power-Up Reset

Holding any key down during power-up will clear out the display RAM and preset the HP 54201A/D to a predetermined condition. Key-down power-up reset is a very important feature to use to clear the instrument if the instrument experiences a lockup state and will not respond to any key press, or when the display is garbled or nothing is displayed. Hold the key down long enough for the power-up tune to be completed. These preset conditions are:

CONDITION	SETTING
TIMEBASE:	
Sweep mode	Auto
Time range	10 μs
Reference	Center
Delay	0.0 s
Autoscale	Period
Acquire mode	Real time
CHANNELS:	
Mode	Dual Channel
Range	5.0 V
Offset	0.0 V
Store mode	Normal
Labels	(blank)
Coupling	1 MΩ dc
Probe attenuation	1:1
Autoscale	Enabled
TRIGGER:	
Mode	Analog
Source	Channel 1
Level	0.0 V Centered
Slope	Positive
Label	(blank)
Autoscale	Enabled
On Event	00001
DISPLAY:	
Graticule	Frame
# of graphs	2
Graph sources	
1	Channel 1
2	Channel 2
Connect dots	Off
Reference lines	Off
Accumulate mode	Disabled
Data filter	On
MEASUREMENTS:	Standard
OTHER:	
Running	True
HP-IB address/mode	Not changed
Hardcopy device	Printer
Rear BNC	Constant low
Beeper	On
Setup labels	(blank)
Stored setups	Unprotected
Stored waveforms	Cleared

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STATE SETTINGS:

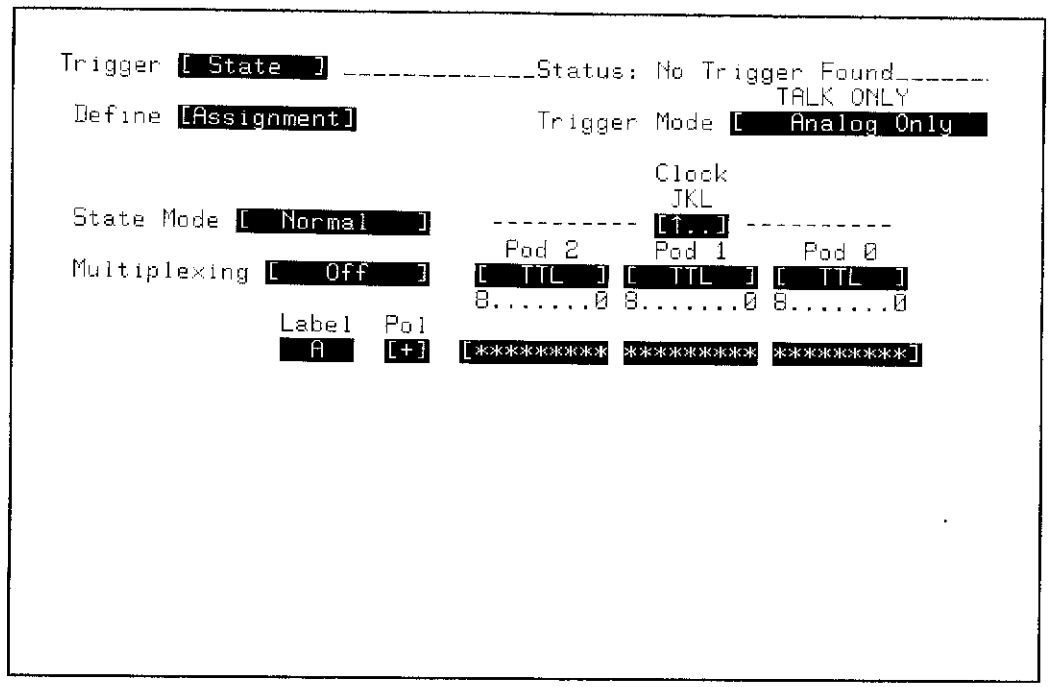


Figure 6-4. Trigger State Assignment Menu after Key-Down Power-Up Reset

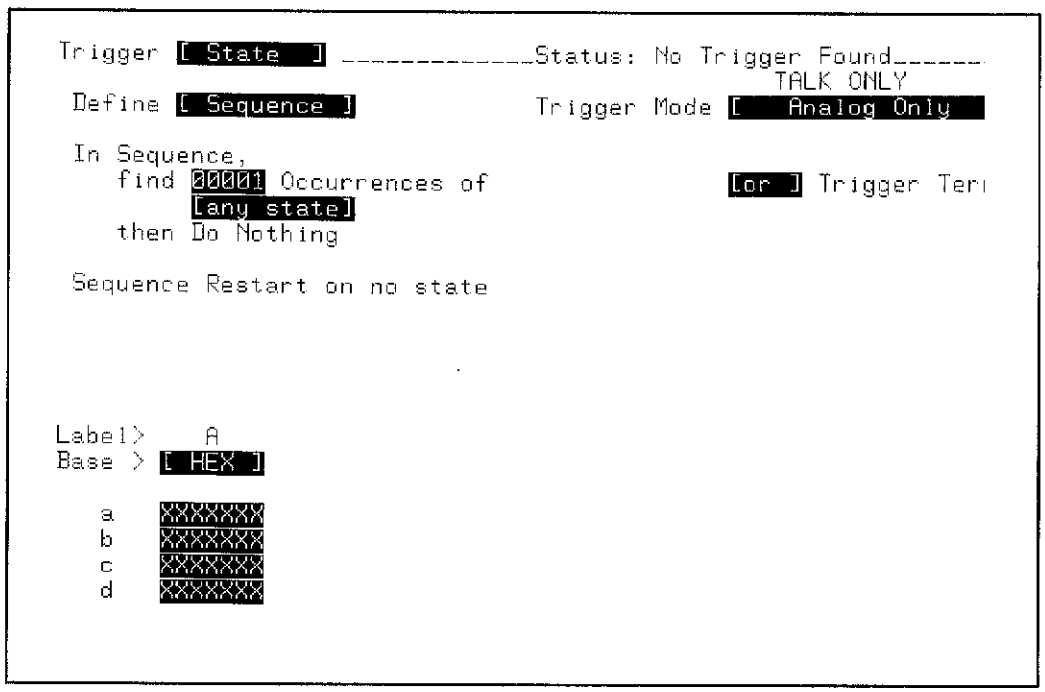


Figure 6-5. Trigger State Sequence Menu after Key-Down Power-Up Reset

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6-20. Troubleshooting Flowchart

The flowchart given in figure 6-6 will aid in troubleshooting malfunctioning assemblies in the HP 54201A/D. Figure 6-6 is supported by several procedures, figures, and tables following the flowchart, which are not meant to be stand alone aids. Bubbles on the flowchart direct you to the next flowchart entry point and the sheet of figure 6-6 where the entry point is located.

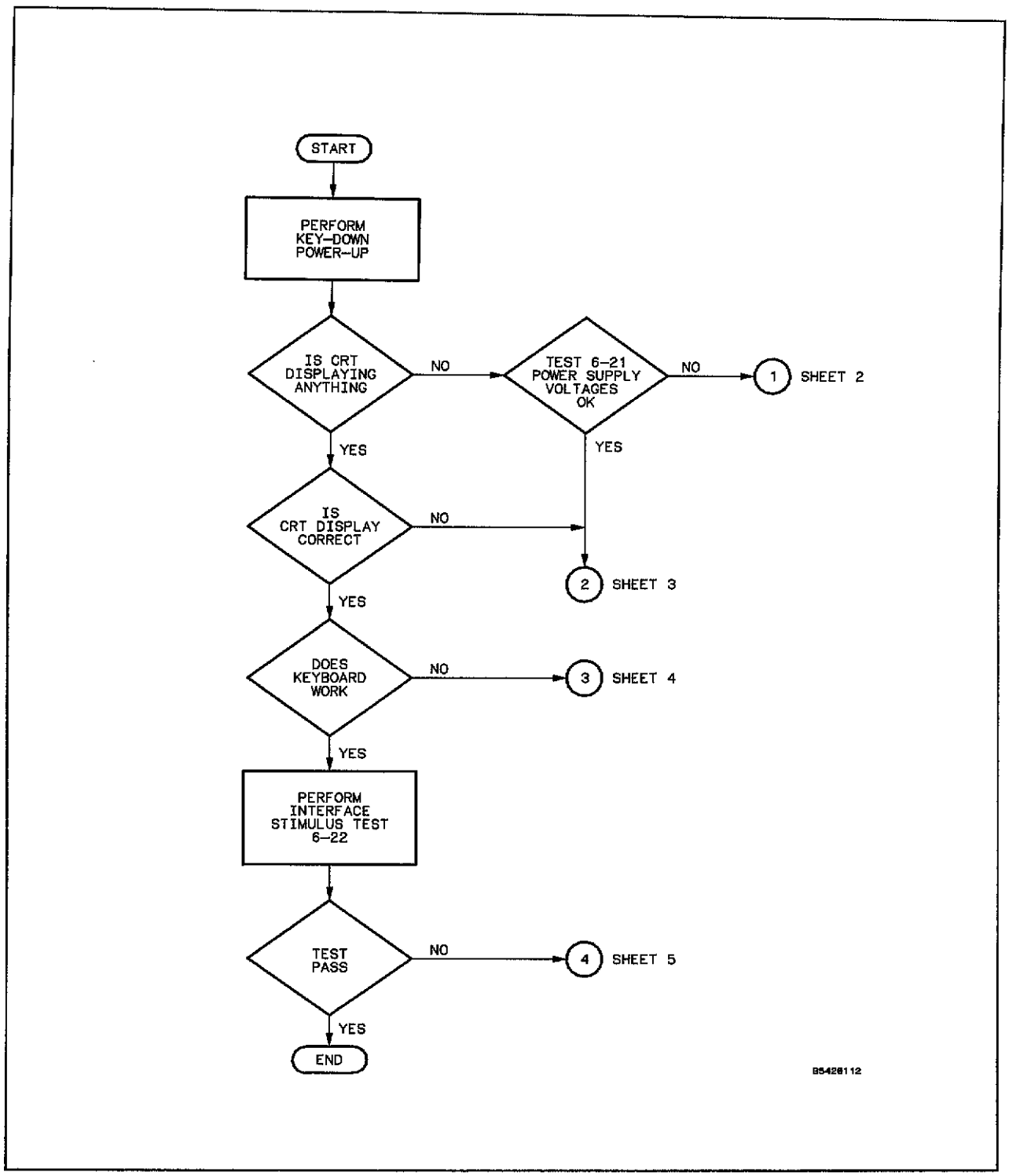


Figure 6-6. HP 54201A/D Troubleshooting Flowchart (Sheet 1 of 5)

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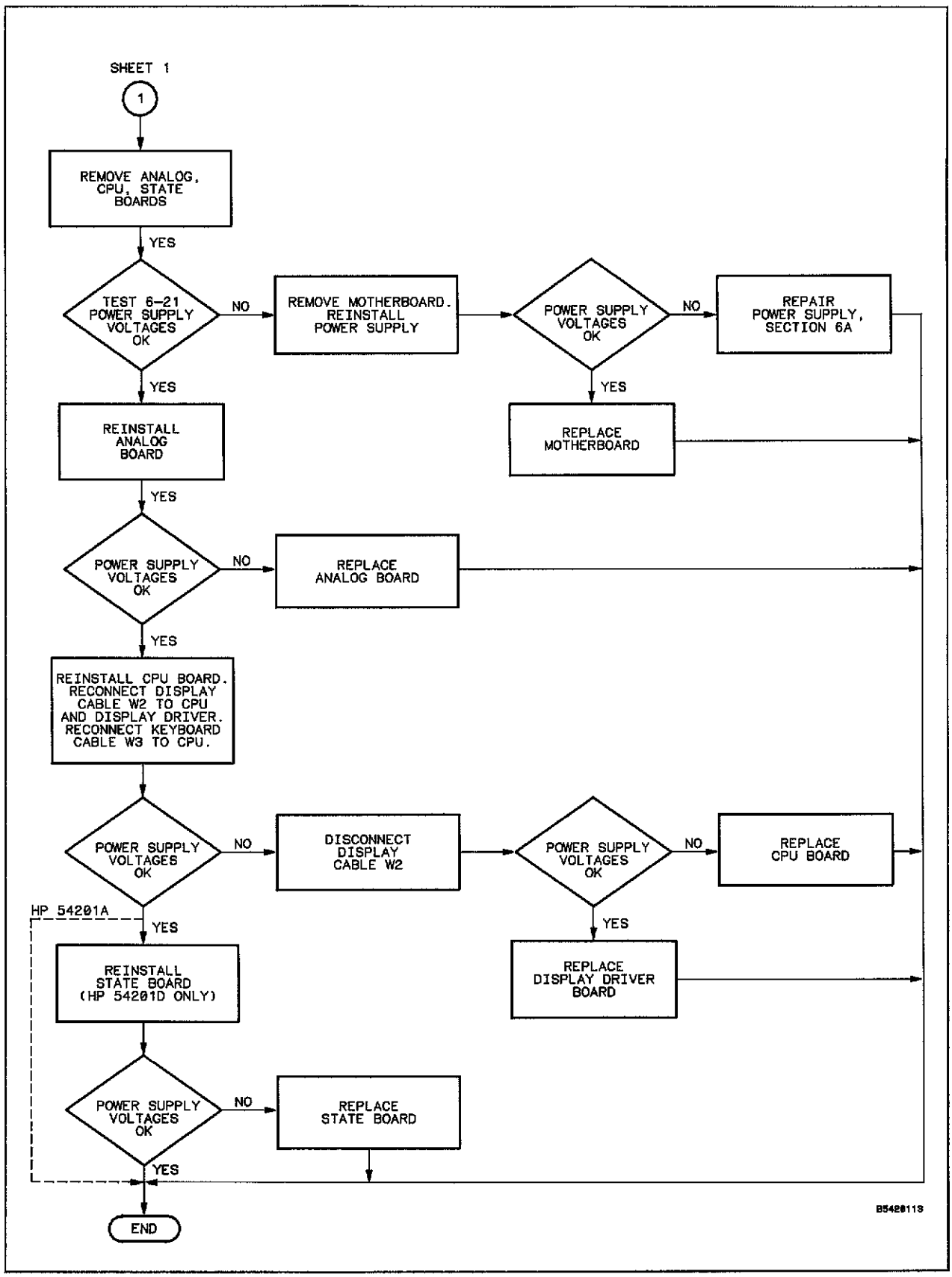


Figure 6-6. HP 54201A/D Troubleshooting Flowchart (Sheet 2 of 5)

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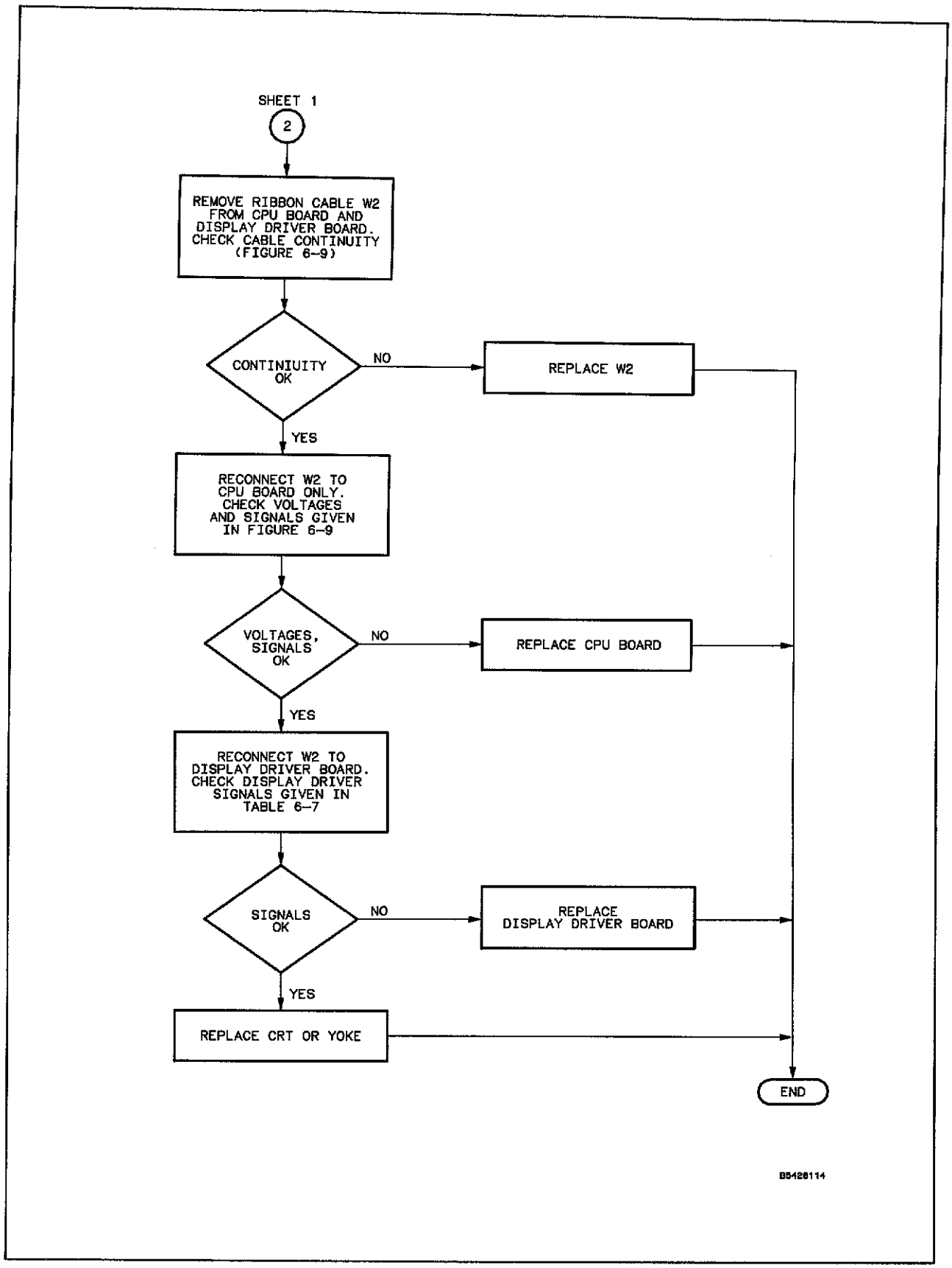


Figure 6-6. HP 54201A/D Troubleshooting Flowchart (Sheet 3 of 5)

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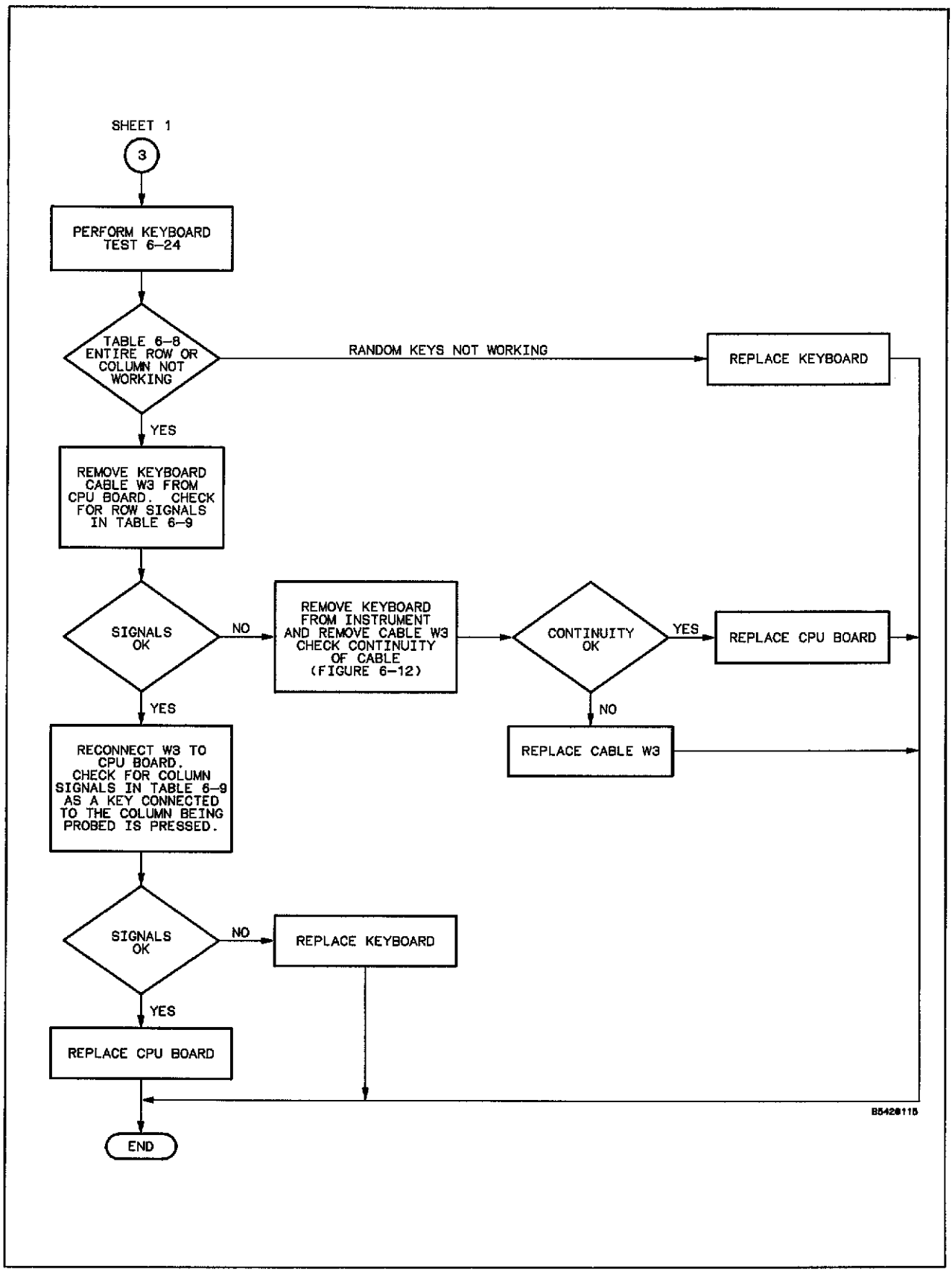


Figure 6-6. HP 54201A/D Troubleshooting Flowchart (Sheet 4 of 5)

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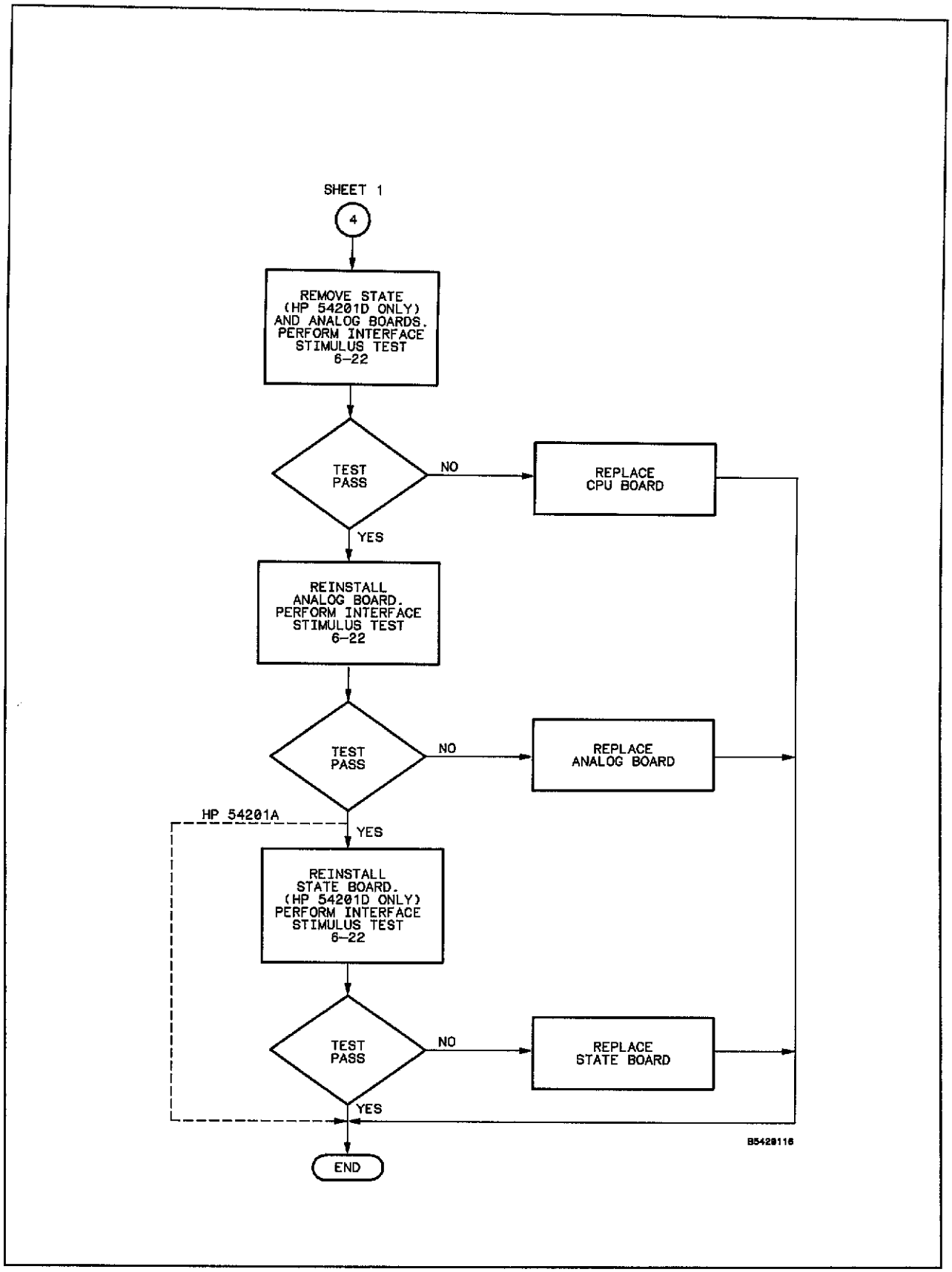


Figure 6-6. HP 54201A/D Troubleshooting Flowchart (Sheet 5 of 5)

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6-21. Power Supply Voltage Check

1. Disconnect power cord.
2. Remove two plastic standoffs from top rear of instrument.
3. Loosen captive screw securing top cover and remove top cover.
4. Apply power to HP 54201A/D.
5. Check dc voltages shown below on power supply test connector A1TP2 (figure 6-7).

SUPPLY VOLTAGE	LIMITS
+15 V	+14.25 to +15.75 V
+12 V	+11.4 to +12.6 V
+5 V	+4.75 to +5.25 V
-2.4 V	-2.16 to -2.64 V
-5.2 V	-5.2 to -5.7 V
-12 V	-11.4 to -12.6 V

6. Adjust VOLT ADJ (A1R34), if required, to bring supplies into limit range.

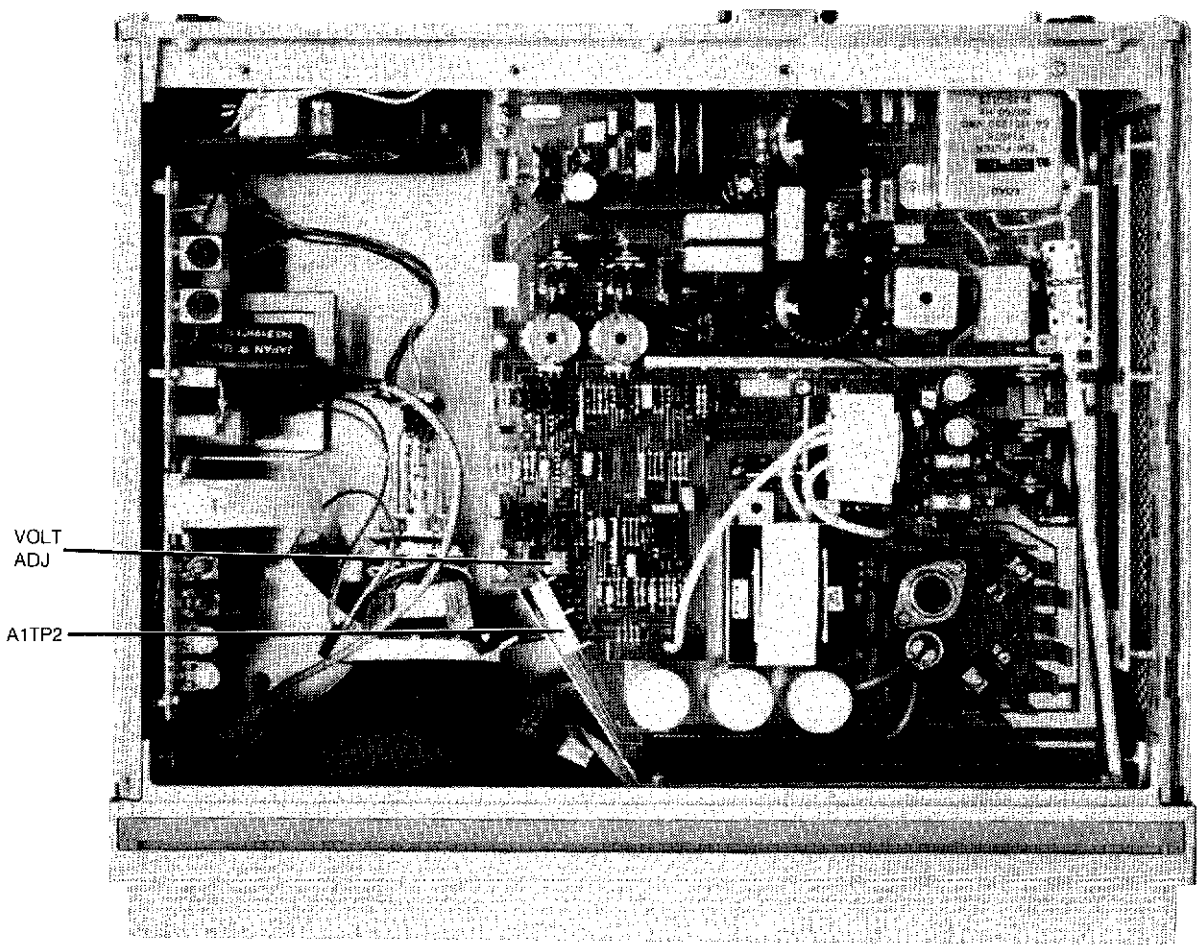


Figure 6-7. Power Supply Test Points.

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6-22. Interface Stimulus Test

This test puts the HP 54201A/D in a test loop and allows you to take signatures to detect possible board failures. The display and keyboard must be functional to perform this test. The test requires the HP 5000B Signature Analyzer and the Service Slot Extender board from the HP 54201A/D Product Support Kit.

1. Remove two plastic standoffs from top rear of instrument.
2. Loosen captive screw securing top cover and remove top cover.
3. Loosen two captive screws securing rear door and remove door.
4. Carefully remove probe cable plugs (HP54201D only) by pulling on their plastic housing.
5. Remove four screws securing rear cover and remove cover.
6. Install service slot extender board into service slot on motherboard as shown in figure 6-8.
7. Set up the HP 5005B Signature Analyzer as shown in table 6-5.
8. Power up HP 54201A/D with key-down power-up.
9. Go to SYSTEM menu and select Test & Service submenu. Move blinking cursor to the Execute Service field and enter 3 for Hardware Service.
10. Enter 4 in the Execute Hardware Test field to start Interface Stimulus test.

The HP 54201A/D is now in a test loop, and will stay in this loop until the INSERT key is pressed. Verify each signature in table 6-6 by probing the corresponding Service Extender board pin number with the Signature Analyzer probe. If any of the signatures are wrong, the test fails. When completed with the test, press the INSERT key to terminate the test.

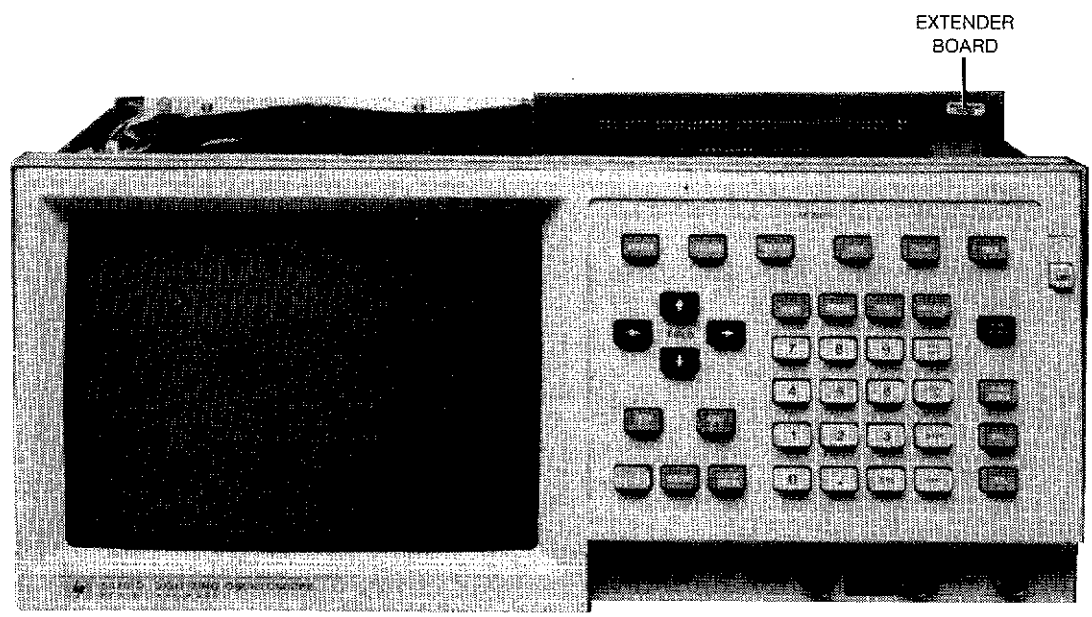


Figure 6-8. Service Slot Extender Board

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Table 6-5. HP 5005B Signature Analyzer Setup

FUNCTION	THRESHOLD	POLARITY	TIMING POD	
			FROM	TO
SIGNATURE QUAL	DATA ECL	CLK ⌠	STOP/QUAL (red)	+5V
	CLOCK TTL	START ⌠	START/ST/SP (grn)	S/S
	ST/SP/QUAL TTL	STOP ⌠	LTB (yel)	CLOCK
		QUAL HI	GND (blk)	GND
TO connections are on connector J2 on CPU board between HP-IB connector and CAL switch				

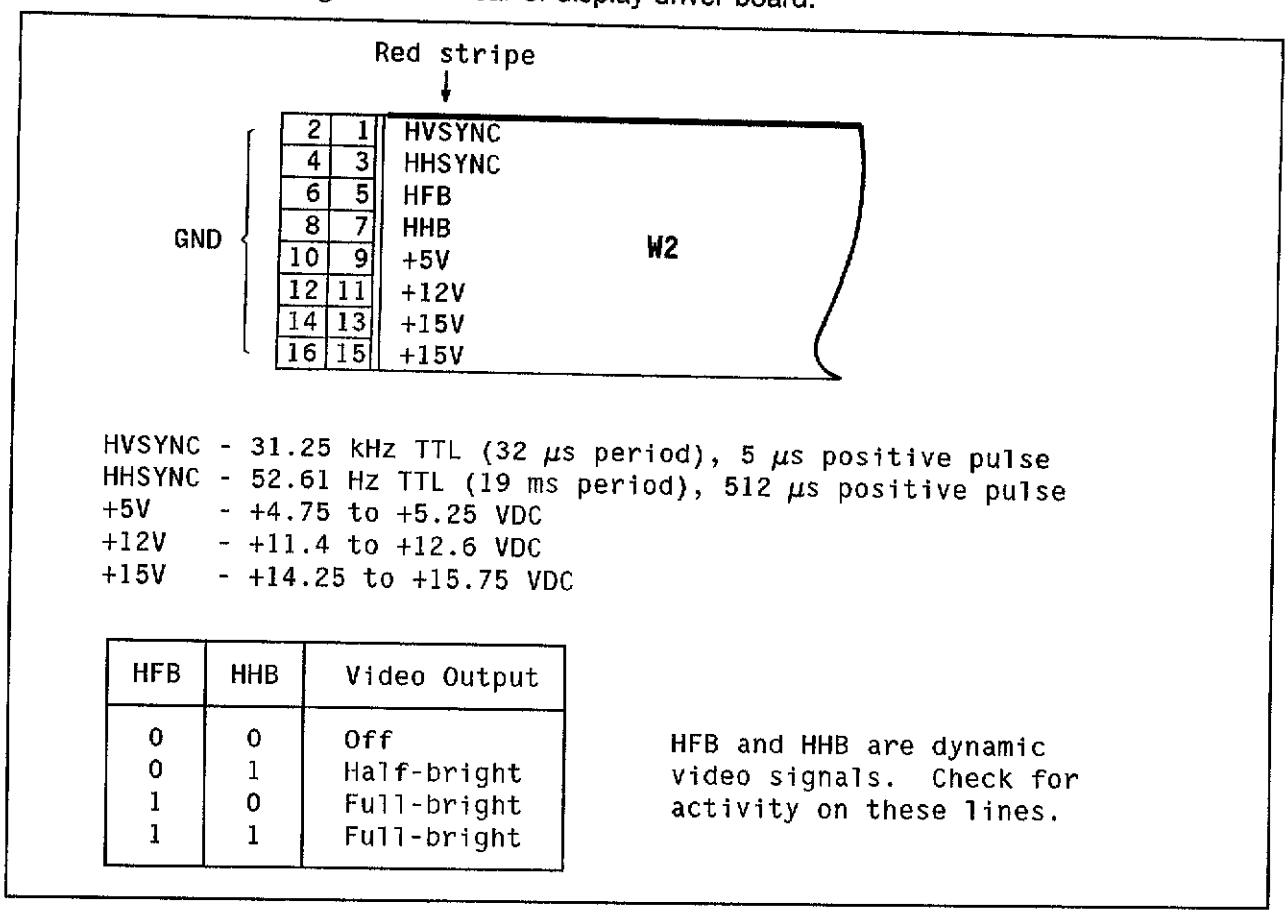
Table 6-6. Interface Stimulus Signatures

SIGNAL NAME	SERVICE CONNECTOR PIN NUMBER	SIGNATURE
GND	40	57P8
-5.2	61	0000
A5	27	2CU4
A4	28	34A5
A3	31	6PF3
A2	32	C0P3
A1	33	8AH3
A0	34	F04C
D7	37	C5UU
D6	38	UU5F
D5	41	PFAC
D4	42	6P52
D3	43	97C6
D2	44	CCAF
D1	45	3510
D0	46	464A

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6-23. Display Driver Signals.

Figure 6-9 and table 6-7 are used in conjunction with flowchart figure 6-6. To check signals in figure 6-9, the top cover must be removed. To check neck pin signals in table 6-7, remove the left side cover and check signals from rear of display driver board.



HFB	HHB	Video Output
0	0	Off
0	1	Half-bright
1	0	Full-bright
1	1	Full-bright

Figure 6-9. Display Driver Board-to-CPU Board Ribbon Cable (W2)

Table 6-7. Display Driver Board to CRT Signals

	WIRE	SIGNAL
CRT Neck Pins	Blue	0 to 400 Vdc
	Red	500 to 800 Vdc (700 Vdc typical)
	Black	0 Vdc
	Brown	12 Vdc (13.2 Vdc typical)
	Yellow	48 to 82 Vdc
	Green	0 Vdc
Yoke	Blue	Dynamic video signals. Check for activity on these lines.
	Red	
	Yellow	
	Green	
Post Accelerator (large red wire to CRT body) is 8 kVdc to 12 kVdc (10 kVdc typical)		

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6-24. Keyboard Test

This test verifies the functionality of the keyboard. The text follows along with flowchart figure 6-6.

1. Power up the HP 54201A/D with key-down power-up.

2. Go to SYSTEM menu and select Test & Service submenu. Move blinking cursor to the Execute Service field and enter 3 for Hardware Service.

3. Enter 3 in the Execute Hardware Test field to start keyboard test.

4. The HP 54201A/D should now display all the front-panel keys as shown in figure 6-10. Press each key on the keyboard. The keys that are working properly will disappear from the screen when pressed.

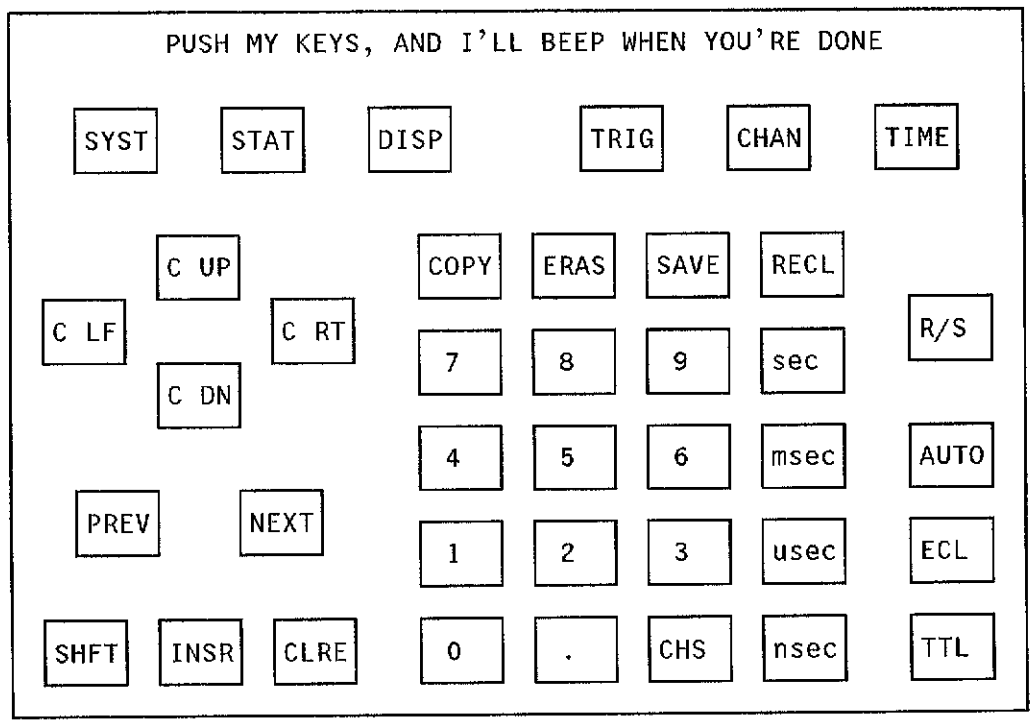


Figure 6-10. Hardware Service Keyboard Test Display

If a key or keys are not working, check if an entire row or column of keys is not working. Row and column assignments are shown in table 6-8. If a row or column is bad, remove the CPU board from the mainframe and install in the service slot (figure 6-11). Then continue with flowchart figure 6-6 procedure.

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Table 6-8. Keyboard Row/Column Assignments

ROW	COLUMN							
	0 (KBC0)	1 (KBC1)	2 (KBC2)	3 (KBC3)	4 (KBC4)	5 (KBC5)	6 (KBC6)	7 (KBC7)
1 (KBR1)	CURSOR ↑	SYSTEM	STATUS	DISPLAY	TRIG	CHAN	TIME	—
2 (KBR2)	CURSOR →	COPY	ERASE	SAVE	RECALL	—	—	—
3 (KBR3)	CURSOR ←	CURSOR ↓	7	8	9	sec Volt	RUN STOP	—
4 (KBR4)	PREV	—	4	5	6	msec mV	AUTO SCALE	—
5 (KBR5)	ECL	NEXT	1	2	3	µsec	TTL	—
6 (KBR6)	—	INSERT	CLEAR ENTRY	0	•	CHS	nsec	(Blue)

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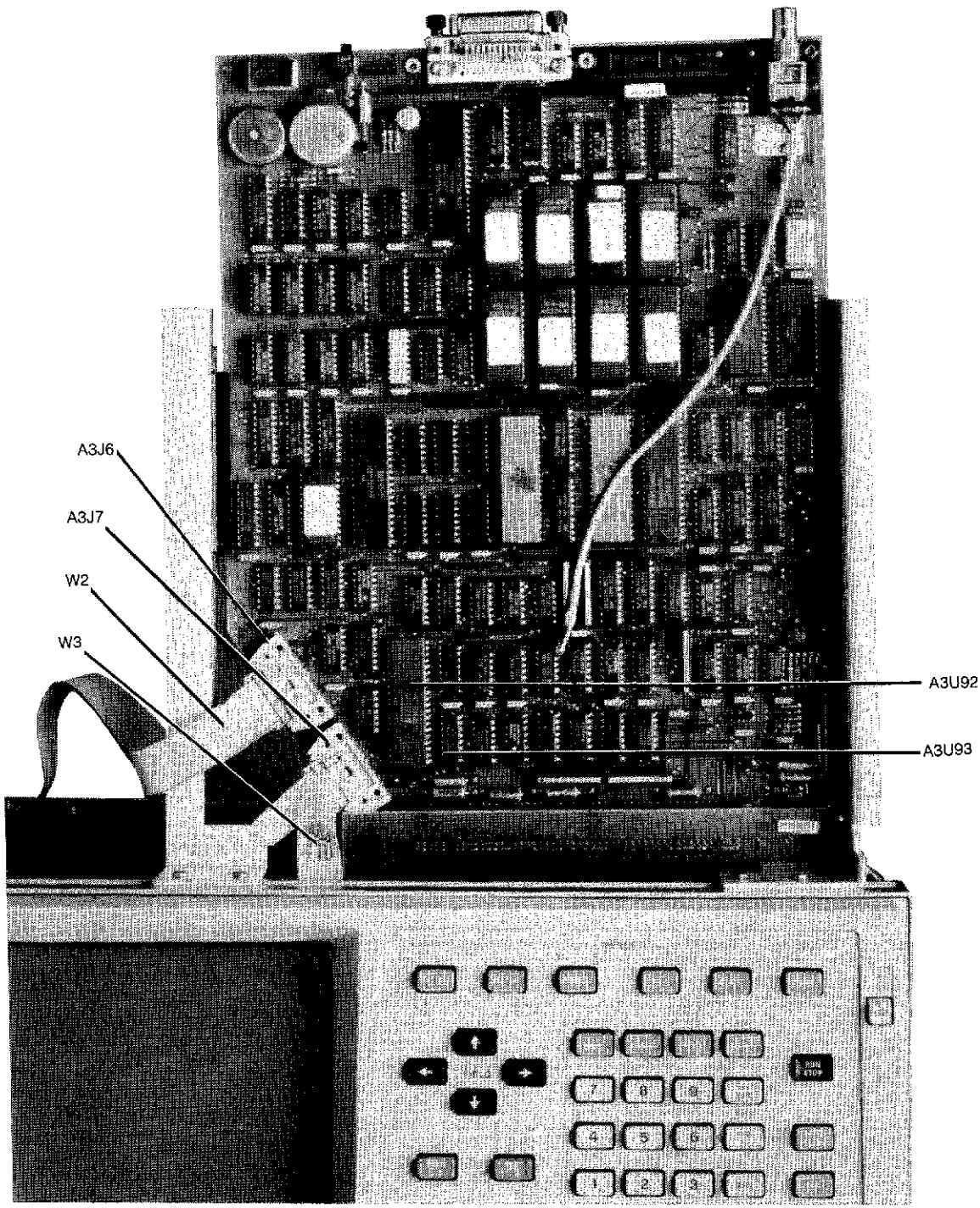


Figure 6-11. CPU Board Extended in Service Slot

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Table 6-9. Keyboard Signals

	SIGNAL	SIGNAL LOCATION	
Row Signals	KBR1	A3U93-14	A3J7-7
	KBR2	A3U93-13	A3J7-3
	KBR3	A3U93-12	A3J7-1
	KBR4	A3U93-11	A3J7-9
	KBR5	A3U93-10	A3J7-11
	KBR6	A3U93-9	A3J7-13
Column Signals	KBC0	A3U92-38	A3J7-5
	KBC1	A3U92-39	A3J7-4
	KBC2	A3U92-1	A3J7-2
	KBC3	A3U92-2	A3J7-6
	KBC4	A3U92-5	A3J7-8
	KBC5	A3U92-6	A3J7-14
	KBC6	A3U92-7	A3J7-12
	KBC7	A3U92-8	A3J7-10

A3U92, U93, and J7 are shown in figure 6-11. Pin 1 is at lower right of all IC's when oriented as shown. Pin 1 of J7 is by triange on connector body. Even pins of J7 are nearest the circuit board and odd pins are away from circuit board.

A signal of 195.3 Hz TTL (5.12 ms period), 640 μs negative pulse width should be on all KBR (keyboard row) lines at all times. This signal is present on KBC (keyboard column) lines only when key attached to specific KBC line pressed. See table 6-8 for key row and column assignments and figure 6-13 for keyboard schematic diagram.

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SERVICE GROUP 6A
POWER SUPPLY

6A-1. INTRODUCTION

This Service Group contains block and component level theory, troubleshooting and schematic information necessary to service the HP 54201A/D power supply. Service group 12A is separated into two sections: theory and troubleshooting.

6A-2. SAFETY CONSIDERATIONS

WARNING

Hazardous potentials exist on the power supply, the CRT, and on the display driver board. To avoid electrical shock the following procedures should be closely adhered to. Wait at least three minutes for the capacitors on the power supply and display driver boards to discharge before servicing this instrument. Wear safety glasses!!!

Several parts of the power supply have lethal voltage and current potentials associated with them. Primary filter capacitors C10 and C11 are very large and have 300 volts across them, + or - 150 Vdc to ground. This provides a great deal of potential energy. With their respective bleeders R4 and R5, the discharge time constant is 60 seconds so even with the supply turned OFF it can be dangerous! Therefore, wait at least three minutes for the supply to discharge before servicing.

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6A-3. SPECIFICATIONS

The power supply used in the HP 54201A/D is a switching power supply that converts the AC line input to six regulated DC voltages. Table 6A-1 contains individual specifications for each voltage.

Table 6A-1. Power Supply Specifications

INPUT

115 volt range: 90 to 127 VAC Input Imax = 4 Amps
230 volt range: 180 to 253 VAC Input Imax = 2 Amps
Frequency Range: 48 to 66 Hz in either voltage range.

OUTPUT

Volts	% Tolerance	Maximum Current (Amps)
+15	5	0.8
+12	5	0.25
+5	5	6.0
-2.4	10	8.0
-5.2	-5, +10	25.0
-12	5	0.25

6A-4. POWER SUPPLY BLOCK DIAGRAM (figure 6A-1)

The HP 54201A/D power supply is separated into three basic sections; Primary, Control and Secondary. The following is a brief outline of each section.

PRIMARY SECTION. The primary section is responsible for providing a rectified and conditioned switching source of approximately plus and minus 150 VDC, along with transformation for control power. The primary section also provides protection to the supply from AC input surge current and overvoltage conditions.

CONTROL SECTION. Control voltage generation, modulation and switching are the main functions of the control section. However, LED failure indication and failure execution is also a function of this section.

SECONDARY SECTION. The secondary section is responsible for filtering, rectification and feedback for the DC power supplies. Also, this section outputs all of the supplies to the test connector and the motherboard.

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6A-5. POWER SUPPLY THEORY OF OPERATION

The theory of operation gives detailed operation of the circuitry on the power supply board. Refer to power supply Schematic 6A-1.

6A-6. Primary Section

The power supply begins operation when the power switch (SW2) is turned ON providing AC line to FL1 which filters the AC for radio frequency interference (RFI). According to the setting of the line select switch (SW1), the primary section will operate in two modes, either 115 VAC or 230 VAC.

6A-7. 115 VAC OPERATION. Notice the way that the neutral line is wired to the primary output of the bridge rectifier (CR4), only two of the diodes of CR4 are used. These are the two that connect to the AC line input of CR4. This configuration produces ≃300V across the + and - outputs of CR4. During the 115 VAC mode this circuitry forms a half wave voltage doubler. Furthermore, while in the 115 VAC mode the primaries of T1 are in parallel so there is 115 VAC across each primary. The outputs of T1 are in parallel and have the same voltage across them during either the 115 or 230 VAC modes.

6A-8. 230 VAC OPERATION. When SW1 is in the 230 VAC mode, all four diodes in the bridge rectifier (CR4) are used. However, the voltage across the + and - outputs of CR4 is still ≃300V. During the 230 VAC mode this circuitry forms a full wave rectifier. While in the 230 VAC mode the primary inputs of T1 will be in series and still have 230 VAC across each primary winding.

The varistors RV1 and RV2 on the primary side of T1 are for transient suppression. The thermistor, RT3, provides surge current protection for CR4.

6A-9. SURGE CURRENT PROTECTION. Because input filter capacitors C10 and C11 are connected directly across the rectified line, a form of surge current protection is provided to limit line surges during turn on. RT3 provides this protection.

6A-10. RFI SUPPRESSION. RFI is generated by unwanted frequency energy caused by the switching components in the power supply. Inductors L2 (balun) and L1 prevent this radio frequency interference from being conducted back into the AC line.

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6A-11. Control Section

The control section mainly consists of the circuitry needed to control the operation of the pulse width modulator (PWM). Also covered is the error detection and execution circuitry needed to control modulation.

6A-12. PWM OVERVIEW (figure 6A-2). A pulse width modulator (PWM) requires four signals for proper modulation: a reference voltage, a feedback from the output to compare with the reference voltage for error detection, feedback current from the output for output current limiting, and a predetermined switching frequency.

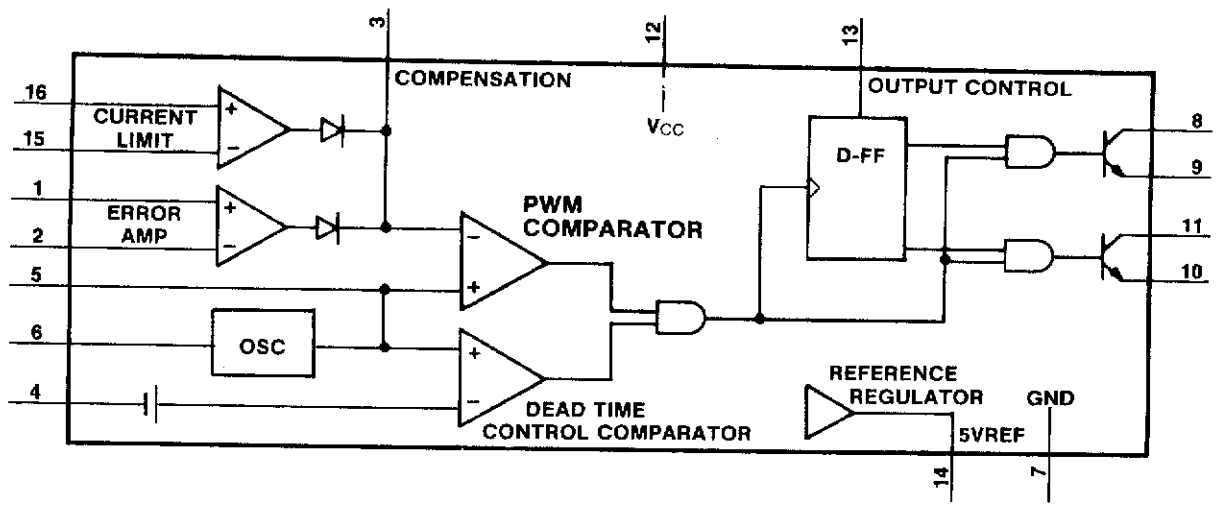


Figure 6A-2. Functional Block Diagram of a PWM

A PWM modulates it's output transistors pulse width (ON time) according to the demands of the system. In this manner it controls the amount of current each switching transistor delivers and therefore controls the power. The PWM configuration used by this supply is for push-pull modulation. Push-pull modulation means that each internal open collector output transistor is turned ON alternately by the pulse-steering flip-flop. This configuration is determined by the output control input (OC) pin 13 being tied to the PWM's internal 5V reference regulator, pin 14.

6A-13. MODULATION CONTROL. If the +5V feedback voltage at pin 1, U5, is higher than the reference voltage at pin 2, the PWM determines that the output voltage is too high. It then reduces its output transistors pulse widths to within limits.

6A-14. PWM SOFT START. When AC is switched ON, capacitor C21 has not charged. This forces the dead-time control input, pin 4 of U5, to follow the 5V reference regulator output, pin 14. Note, when dead-time is high, both outputs are disabled (100% dead-time). While C21 is charging through RP2 (pins 5 and 6), the output pulse widths are allowed to modulate slowly until dead-time is low and 100% modulation is allowed. Soft start is used to prevent large current surges which may occur on power up. Also, a soft start prevents a false signal, possibly created by the control circuitry, from resetting the PWM during power up.

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6A-15. PWM SWITCHING FREQUENCY. The 42 KHz internal oscillation frequency of the PWM is determined by the RC time constant of R21 and C22 connected to pins 6 and 5 of U5. Therefore, each open collector output transistor (pins 8 and 11) is turning ON and OFF alternately at about 21 KHz.

6A-16. CURRENT SWITCHING OPERATION (schematic 6A-1). The open collector outputs, pins 11 and 8 of U5, are complementary and non-overlapping. For zero on-time (zero modulation time), both outputs are high. As demand increases, each output stays low (at different times, non-overlapping) for a longer period until one is going high as the other is going low or until one of the feedback signals limits the pulse duration. Each output is inverted through U2F,G, another open collector device, and alternately causes changing current through the primaries of T2 and T3. These transformers alternately turn Q1 and Q2 ON and OFF which causes the current in the primary of T5 to alternate.

The signals CC1 and CC2 (from U2B,C) prevent or delay the switching of Q1 and Q2. For example, suppose the following condition exists. The power supply is experiencing a heavy demand and must allow close to 100% modulation to meet it. Q1 has turned ON per the request of the PWM and has pulled the one node of T5 to the + primary voltage. Then the PWM tells Q1 to turn OFF and Q2 to turn ON. Q2 can turn ON immediately, but Q1 cannot turn OFF that quickly because of charge storage. The CC2 signal is a feedback signal from the secondary of T5 senses this condition and and will not allow Q2 to turn ON until Q1 turns OFF and the voltage on the secondary of T5 stabilizes. To allow Q2 to turn ON sooner would have the effect of shorting the + primary voltage to the - primary voltage for a short period of time (an enormous waste of power not to mention damage to components).

6A-17. Control Power Supply

As soon as AC is switched ON, CR1 rectifies AC and starts charging C3, a ripple filter for the 12 volt regulator VR1. The output of VR1 lags the input by about 1 V on power up until it stabilizes at +12 V. VR1 is the power supply for +12C (a control power supply used only on the power supply board). +12C supplies U1 which is the +5 reference source (+5REF).

6A-18. PWM Failure Modes

6A-19. PWM FAILURE EXECUTION. There are seven failure execution circuits in the HP 54201A/D power supply. One of these failures, -5.2 current limit, affects the current limit input, U5 pins 15 and 16, of the PWM. Four of the failures affect the Compensation/PWM Comparator input (COMP) pin 3, U5. The COMP input must be allowed to float during normal operation. If an error occurs with the +5 or -2.4 current limit, primary current limit, or thermal shutdown pin 3 will be pulled high and the PWMs' output transistors will be shut OFF. Two of the failures, +5 and -5.2 overvoltage act directly on the drive lines to the Primary Base Drive Transformers.

Several of these failures have LED indicators which indicate the nature of the failure.

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6A-20. PWM CURRENT LIMITING. This power supply uses fold-back current limiting (figure 6A-3). The actual current limit value is determined by sensing the DC voltage developed across the internal resistance of T6 pins 2,11 and 3,10 (T6 contains six internal inductors). Current limiting of the -5.2V supply works by developing a voltage across C20 that is equivalent to the maximum load current times the internal resistance of T6 pins 2,11 and 3,10. The voltage across C20 is then compared to the reference voltage at pin 15 of U5. The foldback of the maximum current limit value is determined by the decrease in the voltage across R17. When the voltage across R17 decreases, the voltage required across C20 also decreases. The decrease across C20 causes the PWMs internal comparator to go more positive and reduce modulation until the -5.2 output voltage across R16 increases, allowing C20 to charge to the value of the reference voltage.

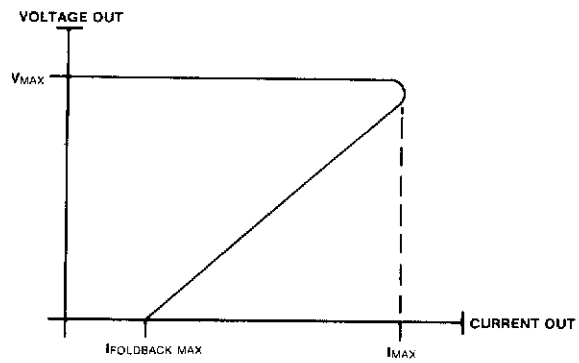


Figure 6A-3. Foldback Current Limiting

6A-21. +5 CURRENT LIMIT. This circuit also operates similarly to the PWM except: the DC component is taken from T6 pins 1 and 12; C43 sets the current limit value; R36 sets the foldback limit; and P/O RP3 pins 4 and 3 adjust the foldback limit. When current limit occurs, pin 14 of U6D goes high and biases CR17, which makes pin 3 of U5 more positive and reduces modulation.

6A-22. -2.4 CURRENT LIMIT. This circuit operates similarly to the PWM except: the DC component is taken from T6 pins 4 and 9; C45 sets the current limit value; P/O RP3 pins 5 and 6 set the foldback limit; and R40 adjusts the foldback limit. When a current limit occurs, pin 8 of U6C goes high and biases CR16, which makes pin 3 of U5 more positive and reduces modulation.

6A-23. U3 AND U4 OPERATION. U3 and U4 are overvoltage sensors. U3 and U4 will turn ON LEDs if an error condition is detected, and both will generate SHUTDOWN. U3 and U4 work in the following manner. When the voltage at pin 2 exceeds the voltage at pin 7 by 2.6 volts, the output pin 8 latches high to turn ON the failure LED and generate SHUTDOWN. The capacitor on pin 3 and pin 4 of U3 and U4 determine the minimum amount of time that an error must exist before they turn ON, thus providing transient protection.

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6A-24. PRIMARY CURRENT LIMIT. U4 detects an error via T4. The primary side of T4 is in the return loop of the minus primary voltage for the switching transistors. The change of current through the primary of T4 establishes a voltage drop in the secondary, rectified by CR10, divided by R14 and R15, and detected at pin 2 of U4. If the voltage at pin 2 of U4 is greater than 2.6 volts, (a slight delay is provided by C19), U4 latches and turns ON the primary current limit LED "PL" and sets SHUTDOWN high which turns OFF U5.

6A-25. THERMAL SHUTDOWN. The circuitry for U3 detects an over temperature condition and generates SHUTDOWN. A normally closed thermal switch (SW3) is mounted on heatsink MP9. When the heatsink exceeds 105 C, the thermal switch opens and U3 detects an error. When pin 8 latches high, the thermal shutdown LED "TH" is turned ON. Then SHUTDOWN is generated and U5 is turned OFF.

6A-26. +5 OVERVOLTAGE. An overvoltage failure occurs when the +5 volt supply exceeds 6 volts making the voltage at pin 3 of U6A greater then the 5V reference on pin 2. This in turn makes pin 1 of U6A go high forcing two operations to occur. The first operation biases CR13 which keeps pin 3 of U6A high regardless of the overvolt condition. The second operation biases CR11, thus making the outputs of U2A, U2D and U2E low. With U2E low, the "OV" (overvoltage) LED (P/O DS1) goes ON indicating an overvoltage failure. Furthermore, with U2A and U2D low, U2F and U2G are be unable to deliver a switching frequency to the base drive transformers. This turns OFF the supplies. Note, that if an overvoltage failure occurs, the power must be cycled OFF/ON in order to reset the overvoltage circuitry.

6A-27. -5.2 OVERVOLTAGE. Except for polarity considerations, the -5.2 overvoltage circuitry operates the same as the +5 overvoltage circuit. This circuit turns OFF at -6.2 volts.

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6A-28. Secondary Section

6A-29. +5, -5.2, AND -2.4 SECONDARIES. Three of the four switching supply secondaries operate relatively the same. The +5 supply will be used as an example of their operation.

The alternating voltage in the center tapped secondary of T5 is full wave rectified by two Schottky diodes (CR20) mounted on a heatsink (MP9). The R27/C28 combination is a snubber network that limits the dv/dt to protect the diodes. CC1 and CC2 (cross conduction 1 and 2) prevent both switching transistors from being ON at the same time and shorting the + and - primary voltages together. P/O T6 and C49 are the filter for the supply. The LED "NORM" being ON indicates that the supply is operating properly.

Except for polarity and the lack of an LED indicator, the -2.4 and -5.2 supplies are the same as the +5 supply.

6A-30. +15, +12, AND -12 SECONDARIES. The alternating voltage of T5 is full wave rectified by CR15. R24 and C23 form a snubber network to protect CR15. P/O T6, C25 and C26 filter the outputs of CR15 before they are regulated by VR2, VR3 and VR4. The outputs of the regulators are filtered by C29-31 before the +15, +12 and -12 voltages are supplied to the motherboard.

6A-31. LED FAILURE INDICATIONS

Figure 6A-4 is a flow chart that guides the user to the faulty circuit(s) indicated by a power supply failure LED.

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6A-32. MNEMONICS

Signals on the HP 54201A/D power supply board have been assigned mnemonics that describe the function of the signal. A prefix letter (H, or L) is used to indicate the active state of the signal and the remaining letters indicate its function. An "H" prefix indicates that the function is active in the "high" state; an "L" prefix indicates that the function is active in the "low" state. The following table is a listing of the mnemonics used on the schematic.

Table 6A-2. Mnemonics

Mnemonic	Description
+12VC	+12 V Control. This is the control voltage used throughout the supply. If +12C is not in regulation, the supply will not operate properly.
CC1,2	Cross Conduction 1 and 2. Complementary signals used to prevent both switching transistors from being ON at the same time.
NORM	Normal. When this LED is ON, the power supply is working correctly.
OV	Over Voltage. When this LED is ON, either the +5 or -5.2 volt supply has exceeded its voltage limits. When asserted, the PWM U5 will be shut OFF.
PL	Primary Limit. When this LED is ON, a non-linear surge in current has occurred in the primary section. When asserted, the PWM U5 will be shut OFF.
PWM+5VREF	Pulse Width Modulator +5V Reference. A +5 volt reference from U5 internal reference regulator.
+5VRET	Return +5V. The voltage on this line is the DC component of the +5 volt supply. It is used to set the current foldback limit of the +5 current limit circuit.
-2.4VRET	Return -2.4V. The voltage on this line is the DC component of the -2.4 volt supply. It is used to set the current foldback limit of the -2.4 current limit circuit.
-5.2VRET	Return -5.2V. The voltage on this line is the DC component of the -5.2 volt supply. It is used by the PWM U5 to set the foldback current limit of the -5.2 volt supply.
SHUTDOWN	This signal is generated in several places and is responsible for turning OFF the PWM U5 by pulling pin 3 high.
TH	Thermal. Thermal switch SW3 opens when the internal temperature of the supply is greater than 105 degrees C. When the TH LED is ON, PWM U5 is turned OFF.

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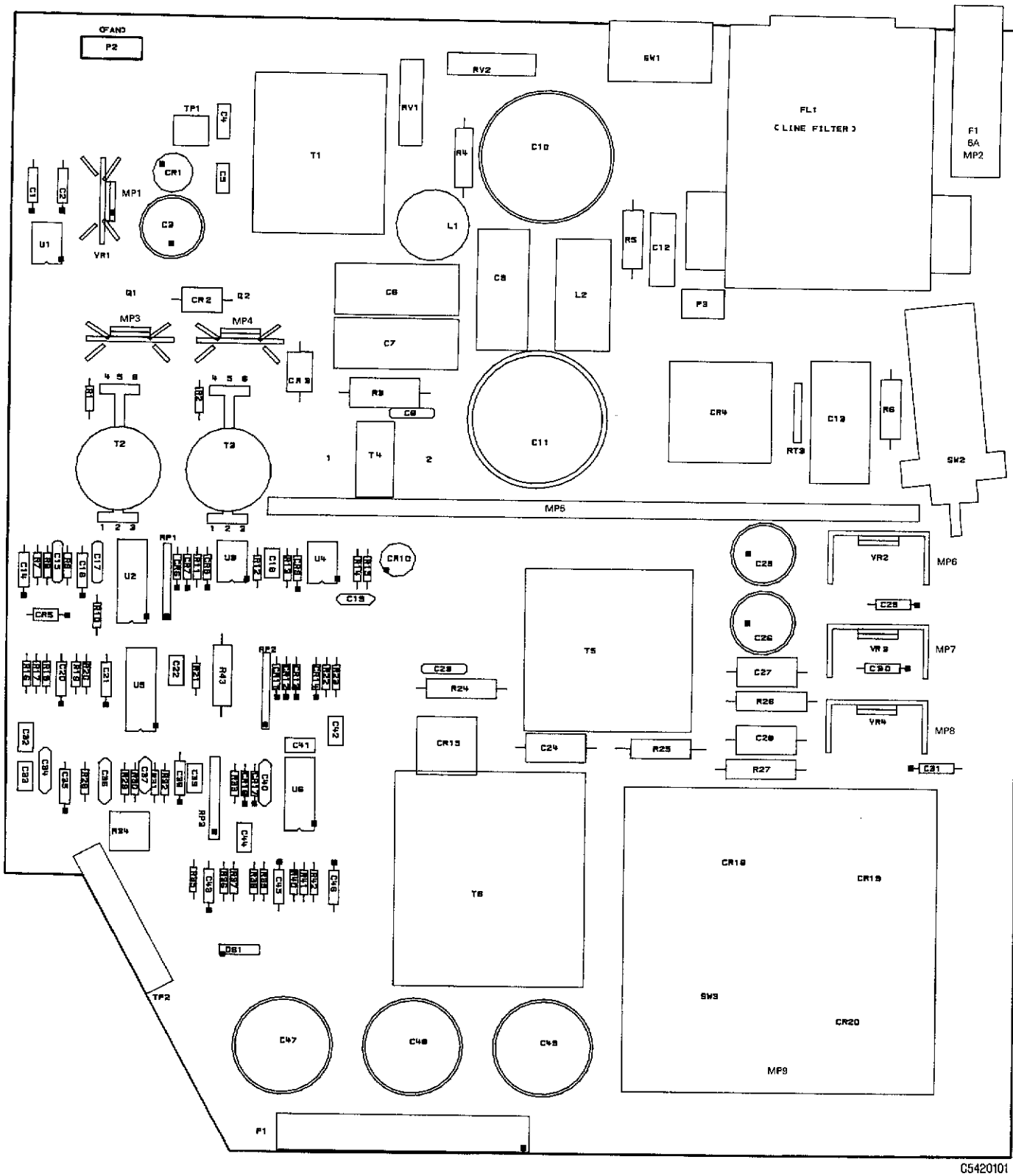


Figure 6A-5. Power Supply Board Component Locator

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APPENDIX A
SELF TEST DOCUMENTATION

A-1. INTRODUCTION

This section provides a brief explanation of how the HP 54201A/D Self Tests work and the portions of circuitry they check. The tests are accessed by selecting the HP 54201A/D front panel SYSTEM Self Tests menu or by executing the System TEST command over HP-IB. The Self Tests, resident in ROM, are a series of tests that confirm proper function of the mainframe hardware and firmware. While the Self Tests provide the user with a confidence level of greater than 90%, it does not verify the critical specifications given in table 1-1 of Section 1. Perform The Performance Tests test for complete instrument compliance to these critical specifications.

A-2. SELF TEST 0 - CPU/MEMORY

The CPU/Memory Self Test consists of three tests for the CPU board:

- Control Test
- ROM Test
- RAM Test

Control Test. The Control Test consists of a timing test and an HP-IB test.

Timing Test: The CPU board has a circuit with five counters that are preset to a value and then are started counting simultaneously. After a loop count is decremented to zero, the five counters are stopped, and the value of each counter is checked against a final value. If any of the counters do not equal this final value, the error message ***FAILED Control test-U61*** is displayed.

HP-IB Test: The HP-IB test is only performed if Self Test 0 was requested from the front panel of the HP 54201A/D. If Self Test 0 is requested over the HP-IB bus, this portion of the test is skipped since it will change status of the bus. The HP-IB test resets the HP-IB circuitry on the CPU board and returns the instrument to Local mode. The circuitry is then set to Listen-only and checked to see if the instrument is in Listen-only mode, then the circuitry is set to Talk-only and checked to see if the instrument is in Talk-only mode. If either portion of the test fails the error message ***FAILED Control test-HPIB*** is displayed.

If both portions of Self-Test 0 pass, the message ***PASSED Control test*** is displayed.

ROM Test. The ROM test performs 16-kbyte checksums of the CPU board ROMs. If the checksum result is different than the checksum stored in ROM7, then the following message is displayed:

FAILED ROM test
#XX Checksum:YY Was:ZZ

where XX = ROM #(0-7)
YY = Correct checksum stored in ROM7
ZZ = Checksum calculated by this test

If no ROM errors are detected the message ***PASSED ROM test*** is displayed. The ROM test only reports the first error found.

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RAM Test. The RAM test verifies read/write performance for the 64-kbyte dynamic RAM, the 8-kbyte static waveform/setup RAM (A3U38), and the 8-kbyte RAM (A3U39) which contains 2-kbyte of calibration factors. All three RAM groups are on the CPU board and are tested in the same manner. If the rear-panel switch on the HP 54201A/D is set to the Protected position, the 2-kbyte portion of the calibration factor RAM is not tested.

The RAMs are tested by writing a 2-kbyte block of rolling 1's pattern. The block is then read and if all bytes are the same as written in, the next block is tested by rewriting the data. If there is a failure, the test is stopped and the following error message is displayed:

FAILED RAM test
XXX At Loc: ddddH Wrote:YY Read:ZZ

where: XXX = RAM identifier (U39, U38, or 64K)
dddd = Location in RAM (0-1FFF,0-1FFF, 0-FFFF)
YY = Value written to RAM
ZZ = Value read from RAM

If there were no RAM errors, the message ***PASSED RAM test*** is displayed. The RAM test only reports the first error found. Stored waveforms and setups are not altered by this test.

A-3. SELF TEST 1 - ACQUISITION/TRIGGER

The Acquisition/Trigger Self Test consists of four tests for the Analog board in the HP 54201A/D and an additional six tests for the State board in the HP 54201D. These tests are:

ACQUISITION BOARD

- Channel 1 Test
- Channel 2 Test
- Auto scale Test
- Interpolator Test

STATE BOARD (HP 54201D only)

- State Pod Test
- State Sequence Test
- State Qualified Mode/Clock Test
- State Occurrence Test
- State Restart Test
- State Bit Fault Test

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A-4. Analog Board Self Tests

Channel 1 and Channel 2 Tests. These tests check each channel's gain and offset capability. Several voltage ranges are tested. At each voltage range the offset D/A converter output from the Analog board is set to 1/4 of the set voltage range. This voltage value is then checked for allowable error margin. A q level is defined to be 1/64 of the voltage range.

RANGE CHECKED	ALLOWABLE ERROR
40 mV	±8 q levels
80 mV	±4 q levels
160 mV	
400 mV	

Auto Scale Test. The offset D/A converter on the Analog Board is configured to fluctuate six times about a trigger level, thereby causing six trigger signals. Frequency counters count the number of triggers. If the count does not match the six triggers generated, the text fails.

Interpolator Test. The offset D/A converter on the Analog Board is configured to fluctuate many times about a trigger level, thereby causing trigger signals. The time from trigger point to the next system clock is then checked to see if the time is within a maximum and minimum value.

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A-5. State Board Self Tests

For all of the State board tests, input conditions (states) are simulated by setting pod threshold levels to their maximum high level (+9.9 V) or their maximum low level (-9.9 V). For example, if pod 1 threshold is set to +9.9 V, then all of the data inputs from pod 1 will appear low (0). Conversely, if pod 2 threshold is set to -9.9 V, then all of the data inputs from pod 2 will appear high (1).

Clock inputs are simulated by two different methods. One way is by toggling threshold levels. When this method is used, all data inputs from that pod must be "don't cares". In addition, the number of clocks generated by toggling one time is indeterminate. With the pods left open and floating, the toggling of thresholds causes ringing which produce multiple clocks for each transition of the pod threshold. The second method of generating clocks is achieved through special test circuitry and software and the clocks are called CPU clocks.

Note

Except for the State Occurrence test, all pods must be connected to the HP 54201D for the State tests to pass.

State Pod Test. This test sets all of the pods to their low level and then checks to see if the inputs appear high. All pods are then set to their high level and checked to see if the inputs appear high. If the State Pod Test fails, a one-digit decimal number will be displayed indicating which HP 10271A Pod has failed.

NUMBER DISPLAYED	FAILED POD		
	2	1	0
1			■
2		■	
3		■	■
4	■		
5	■		■
6	■	■	
7	■	■	■

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State Sequence Test. The following is the sequence specification which is tested:

```
In Sequence
   find [a]
   then [b]
   then [c]
   then Count [00003] occurrences of
        [d]

Sequence Restart on [no state]

    [  OCT  ]
a = 000777777
b = 777000777
c = 777777000
d = 777777777
```

Input states are simulated by setting pod thresholds appropriately. After each change of input state, a CPU clock is generated. After each CPU clock, the test program checks to see if a trigger has been generated. The test begins by setting the condition up so that state "d" is present (all pod thresholds low). The test continues changing states in the following order:

```
1.   d then clock
2.   c then clock
3.   b then clock
4.   a then clock   (first state found)
5.   d then clock
6.   c then clock
7.   b then clock   (second state found)
8.   a then clock
8.   d then clock
10.  c then clock   (third state found)
11.  b then clock
12.  a then clock
13.  d then clock   (fourth state found first time)
14.  c then clock
15.  b then clock
16.  a then clock
17.  d then clock   (fourth state found second time)
18.  c then clock
19.  b then clock
20.  a then clock
21.  d then clock   (fourth state found third time)
```

The trigger should be generated only after the sixth time state "d" is present. If the trigger is generated before, after, or not at all, the test will fail.

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State Qualified Mode/Clock Test. The following is the sequence specification which is tested:

```
In Sequence, Qualify on Slave Clock, then
   find [00001] Occurrences of
        [ any state ]
```

All data inputs are "don't cares" in this test and pod thresholds are toggled to generate clocks. This test involves six parts in which both master and slave clocks are assigned all edges of each clock. The following are the combinations tested:

	Master Clock	Slave Clock
a.	L↓	J↓
b.	L↑	J↑
c.	J↓	K↓
d.	J↑	K↑
e.	K↓	L↓
f.	K↑	L↑

Each part of the test involves clocks generated in this order:

1. Master clock
2. Master clock
3. Master clock
4. Slave clock (qualifier)
5. Master clock (trigger events)

The test program checks for a trigger after each master or slave clock. The trigger should be generated only after the master clock which follows the slave clock (step #5). If it occurs at any other time or not at all for any of the six parts of this test (a through f), the test will fail.

State Occurrence Test. The following is the sequence specification which is tested:

```
In Sequence,
   find [65535] Occurrences of
        [ any state ]
```

This test doesn't use any of the inputs or clocks from any of the pods. CPU clocks are generated to simulate each occurrence of "any state". The test program begins by generating 65,534 clocks and then checks to see if a trigger had occurred as a result of any of the past clocks. If the test detects a trigger at this point, then the test will fail, since the number of occurrences specified is 65,535. If a trigger has not occurred, the test generates one more clock and checks for the occurrence of the trigger once more. If a trigger has not occurred, the test will fail.

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State Restart Test. The following is the sequence specification which is tested:

```
In Sequence,
   find [c]
   then [b]
   then Count [00001] Occurrences of
        [a]

Sequence Restart on [d]

    [  OCT  ]
a = 000777777
b = 777000777
c = 777777000
d = 777777777
```

This test is very similar to the State Sequence Test. Input states are simulated by setting pod thresholds and clocks are generated internally (CPU clocks).

The following states are set up in this order:

1. c then clock (first state found)
2. b then clock (second state found)
3. d then clock (sequence restart)
4. a then clock
5. c then clock (first state found)
6. b then clock (second state found)
7. a then clock (trigger state found)

The test checks for a trigger after each state condition. A trigger should be generated only after the second time "a" occurs (step #7). If the trigger occurs at any other time, or not at all then the test will fail.

State Bit Fault Test. The following is the sequence specification which is tested:

```
In Sequence,
   find [00001] Occurrences of
        a Missing Bit
```

All data inputs are "don't cares" and clocks are generated by toggling pod thresholds. Toggling pod 0 threshold generates an L clock which is serial data and toggling pod 1 threshold generates a K clock which is the reference clock cell. The following is the order in which clocks are generated:

1. L clock (serial data)
2. K clock (reference clock)
3. K clock (reference clock and trigger)

The test program checks for a trigger after step #1 and step #3. The trigger should be present only after the second K clock. If the trigger occurs at any other time or not at all, the test will fail. This test also checks the extra bit case since the only difference is a software reconfiguration for user interface.

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A-6. SELF TEST 2 - INPUT

This self test checks the ability of the HP 54201A/D to acquire a signal through the front panel BNC and then store it in memory. This test is performed in both Random Repetitive mode (RR) and Real Time mode (RT). Once in memory, the data waveform is checked for acceptable amplitude and frequency. The HP 54201A/D is preset to 50Ω mode:

```
Channel Range:    4 V
Channel Offset:   1.5 V
```

The timebase is setup to 2 μs Range and 0 second Delay. When performed from the front panel, the test prompts the user to connect a BNC cable from the rear-panel BNC to each of the channel BNCs, one at a time. If this test is run over the HP-IB bus, the inputs must be properly configured before the System TEST command is issued. When the test is started, a 2-MHz TTL square wave is output from the rear-panel BNC, acquired through the selected front-panel BNC, and stored in memory. Period, Vtop, and Vbase measurements are made on the acquired data.

The period measurement must be 500 ns ±20ns to pass.

The Vtop measurement must be ≥2 V to pass.

The Vbase measurement must be ≤500 mV to pass.

If all the above tests pass, the message **PASSED Test 2** appears. If there are any failures, a 2-digit number follows the advisory, for example:

FAILED Chan 1 test RR [23]

The first digit indicates a voltage measurement failure;

1 - the lower value (Vbase) was greater than 0.5 V

2 - the upper value (Vtop) was less than 2 V

3 - both upper and lower value failed, or there was no valid signal present

The second digit indicates a period measurement failure:

1 - the period measurement was too low

2 - the period measurement was too high

3 - no valid signal was present

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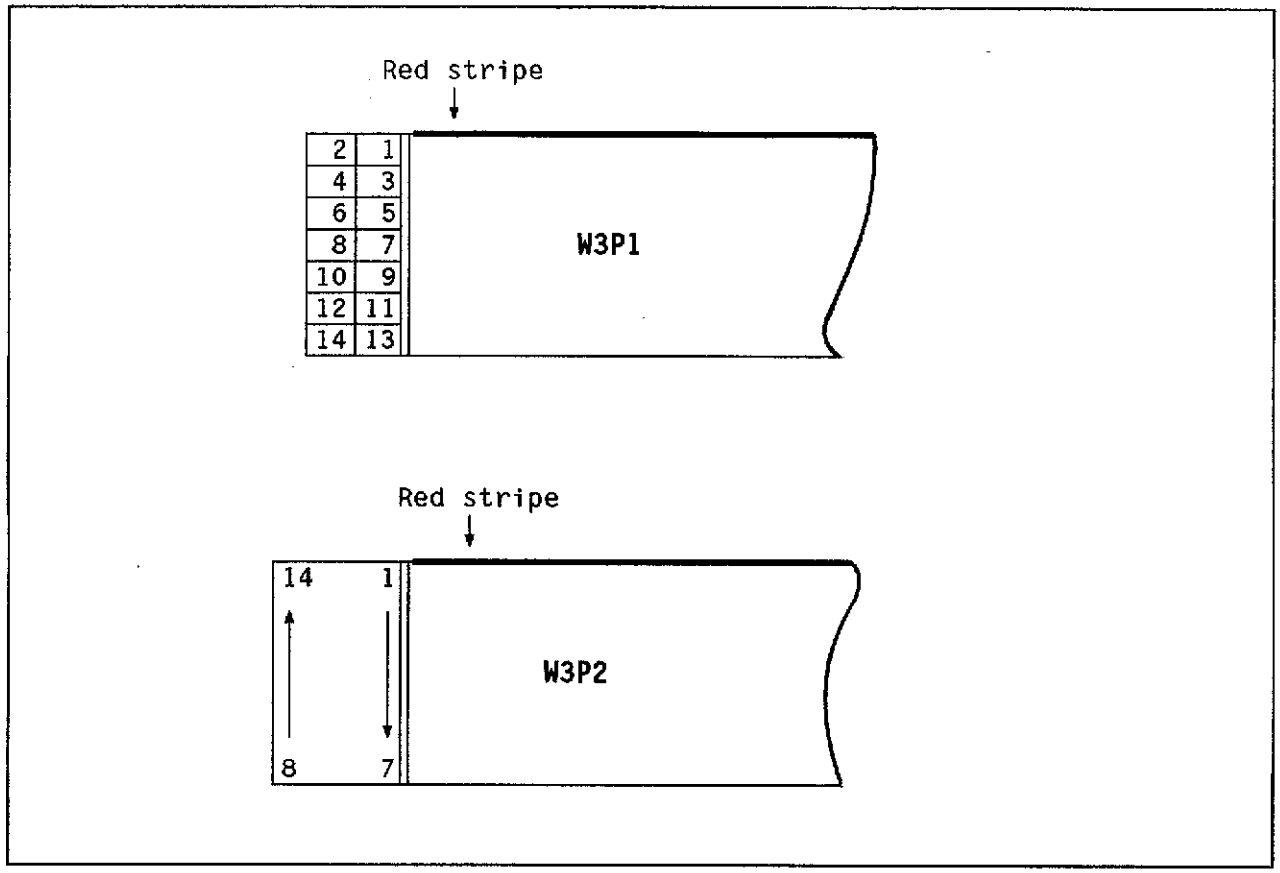
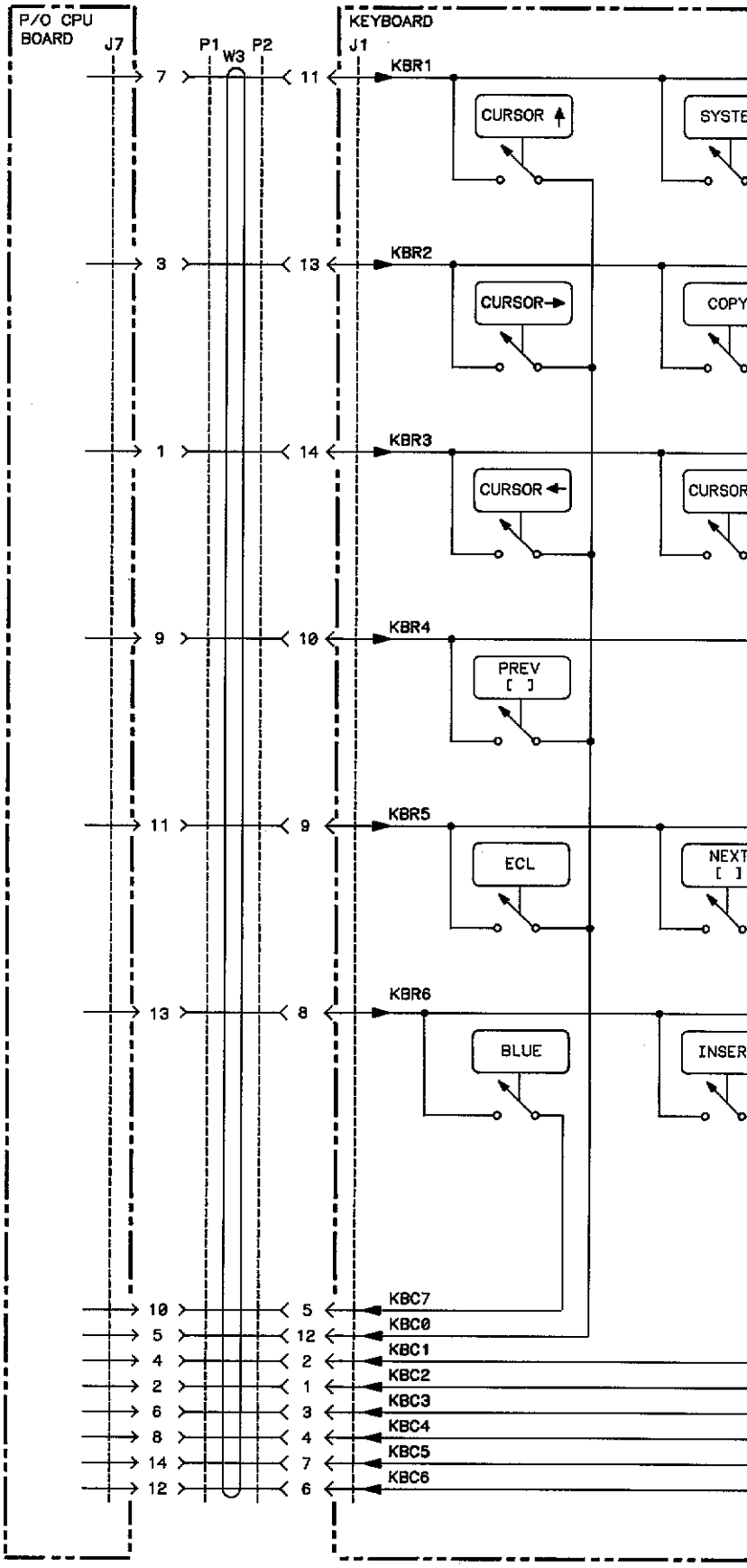


Figure 6-12. Keyboard-to-CPU Board Ribbon Cable (W3)

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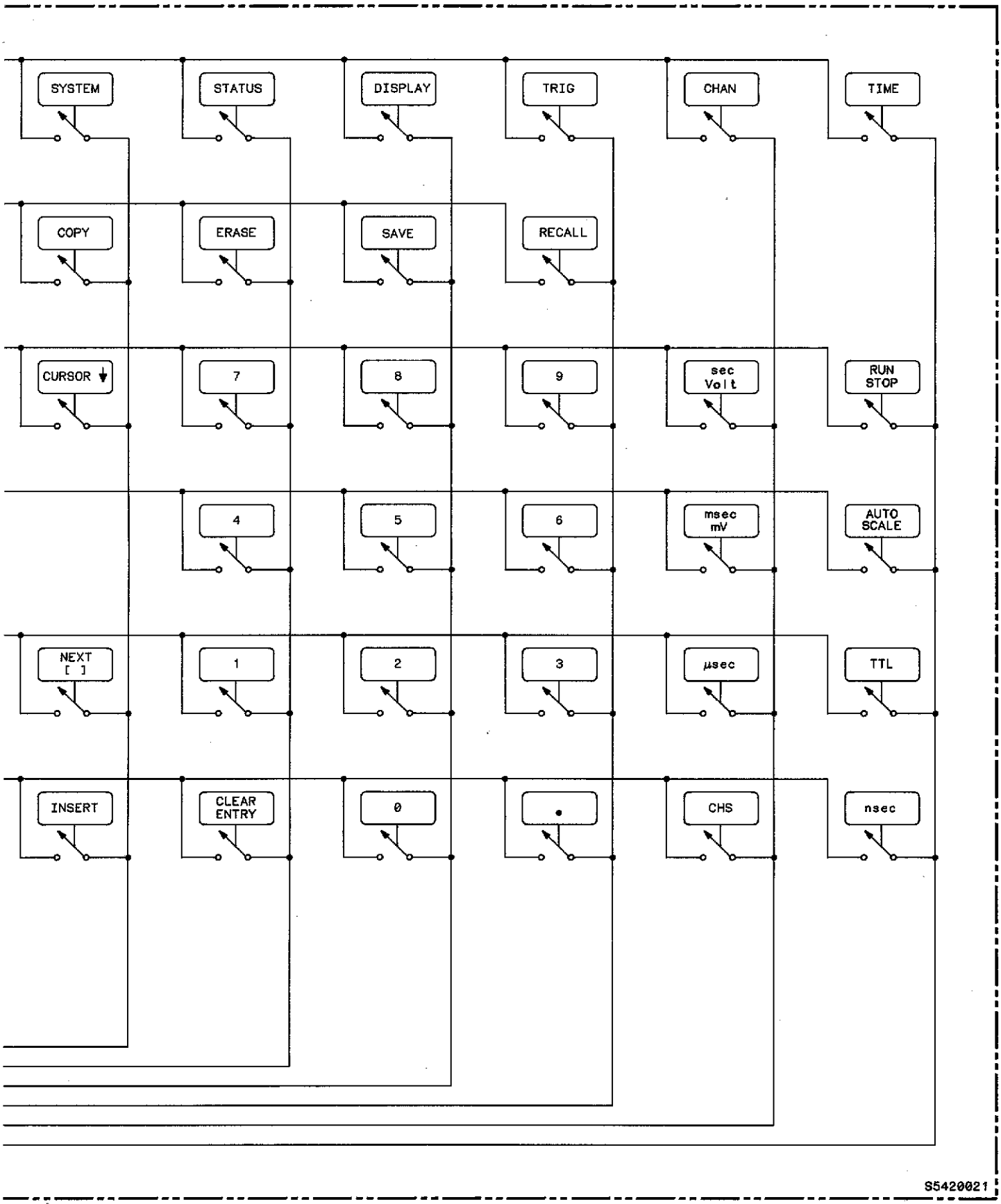
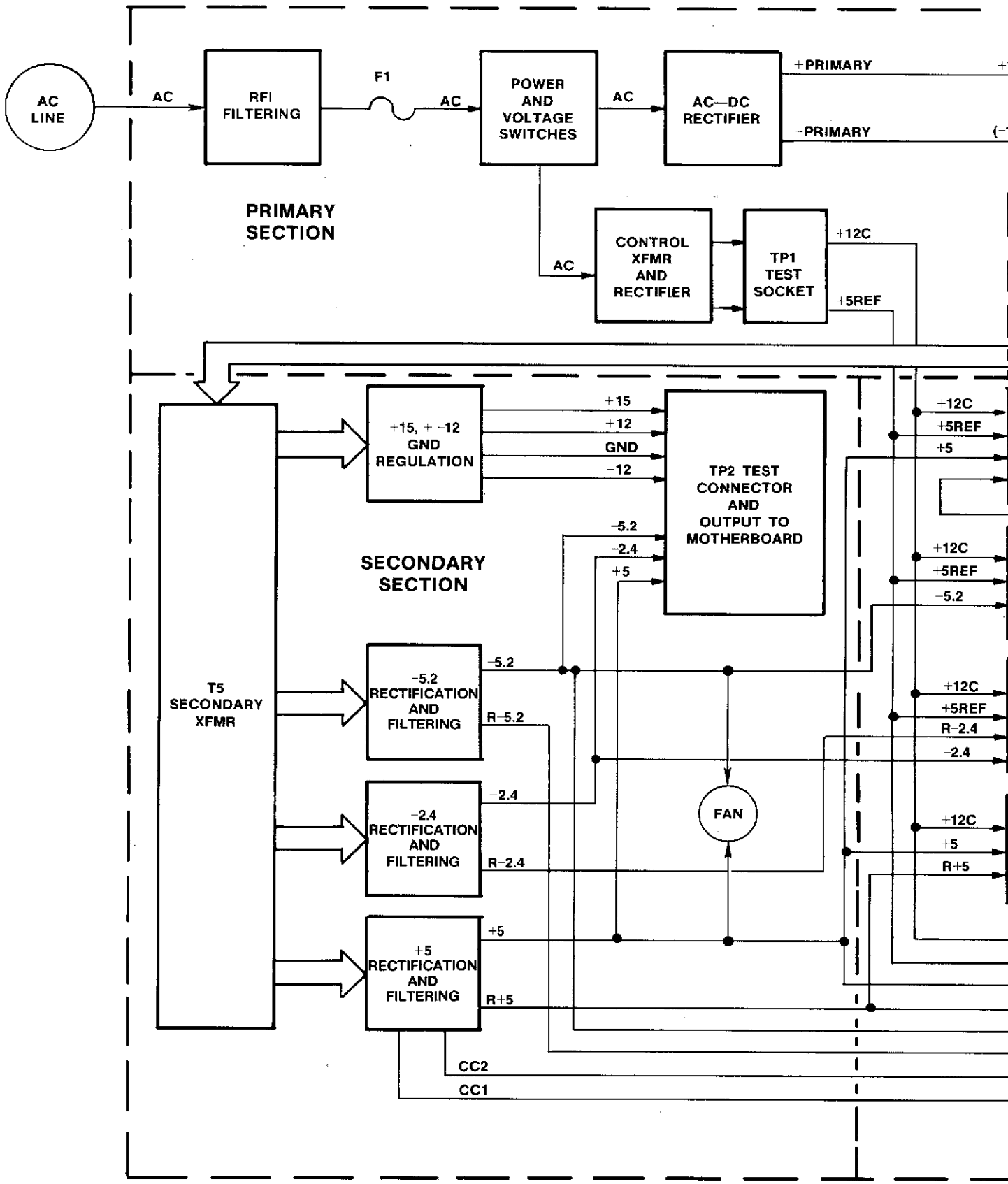


Figure 6-13. Keyboard Schematic Diagram

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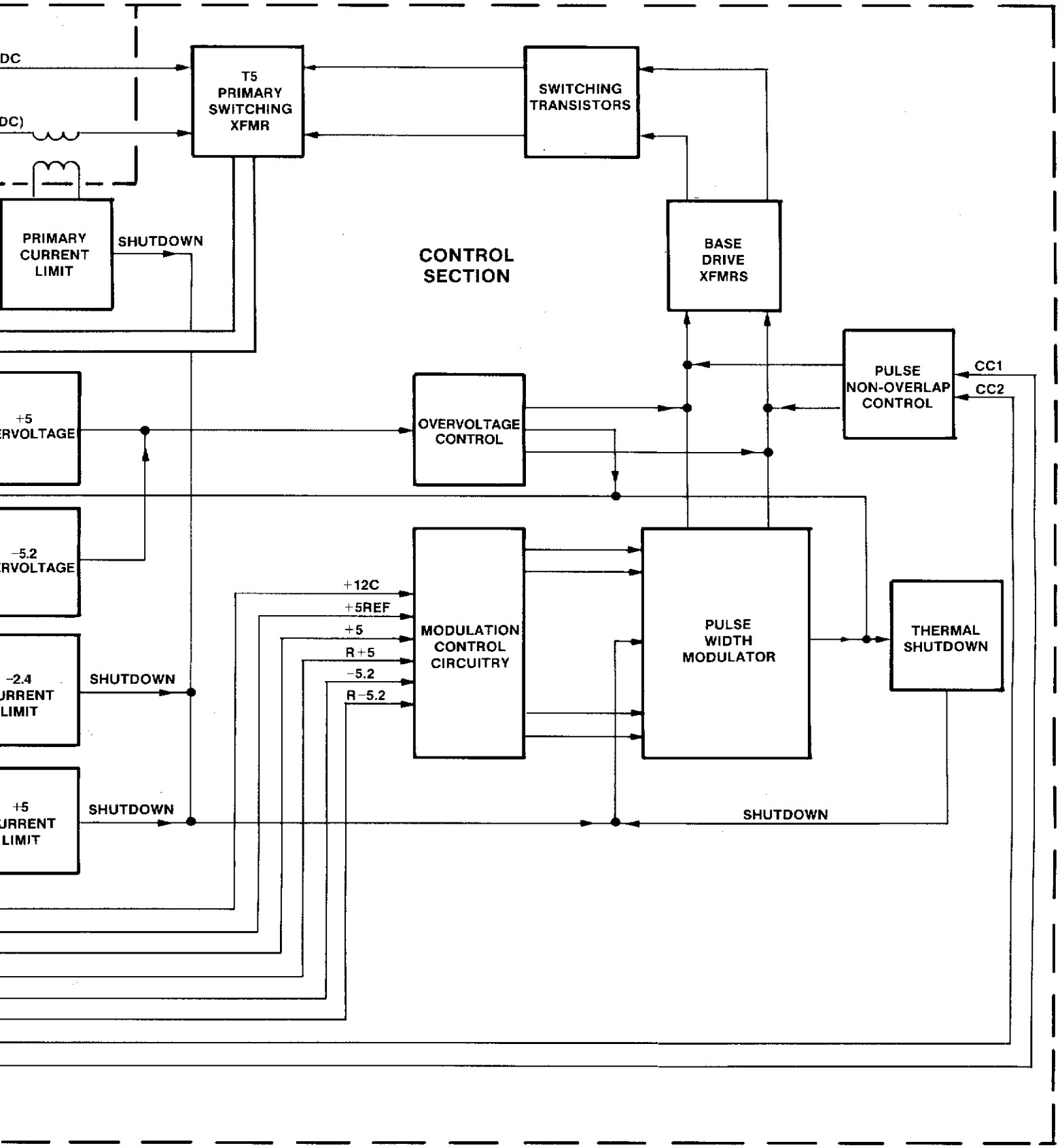
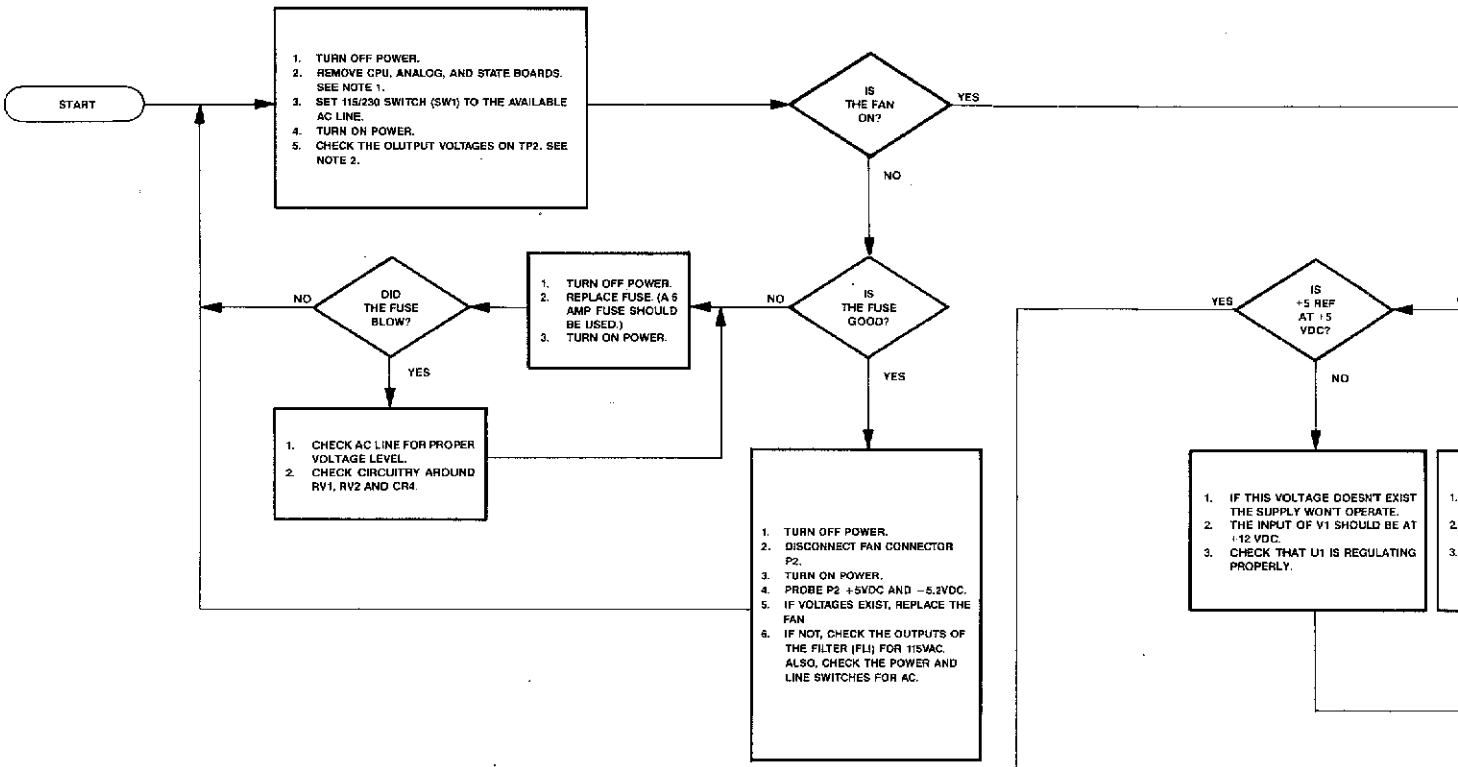
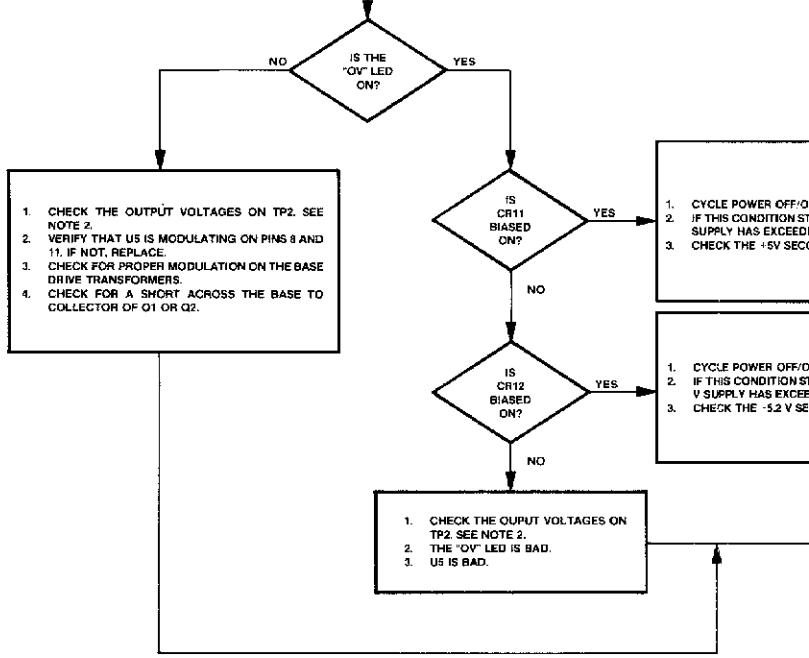


Figure 6A-1
Power Supply Block Diagram

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WARNING

R4/C10 and R5/C11 have a discharge time constant of 60 seconds. The primary voltage lines have ~300 volts across them, + or − 150 Vdc to ground. The main filter bank, C6 and C7, contains enough energy to be a potential hazard to life, even with the supply turned OFF! Therefore wait at least three minutes for capacitors to discharge before servicing the power supply board.

NOTE 1

When troubleshooting the power supply all system boards should be removed to prevent possible damage while servicing the power supply. The output voltages will stay in regulation without a load on the supply. However, when making final tolerance measurements the system boards should be installed.

NOTE 2

Power Supply Specifications

INPUT

115 volt range: 90 volts to 127 volts, Input Imax = 4 Amps.
230 volt range: 180 volts to 253 volts, Input Imax = 2 Amps.
Frequency Range: 48 Hz to 66 Hz in either voltage range.

OUTPUT

Volts	% Tolerance	Maximum Current (Amps)
+15	5	.8
+12	5	.25
+5	5	6.0
−2.4	10	8.0
−5.2	−5, +10	25.0
−12	5	.25

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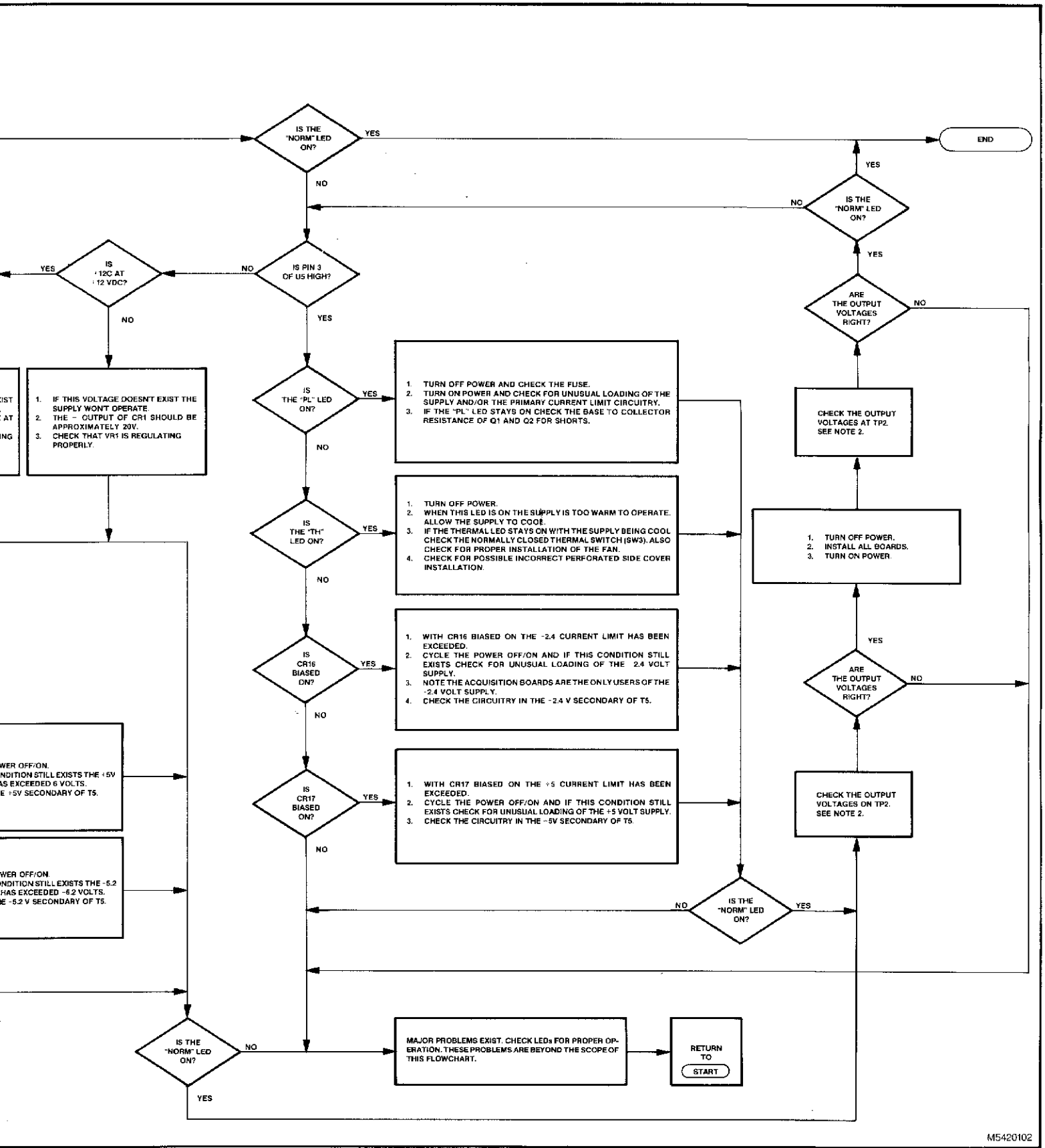


Figure 6A-4
Troubleshooting Flow Chart for LED Failure Indicators

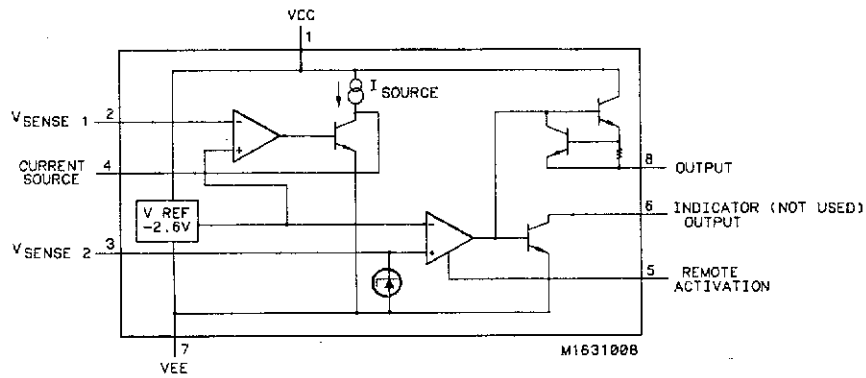
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NOTE 1

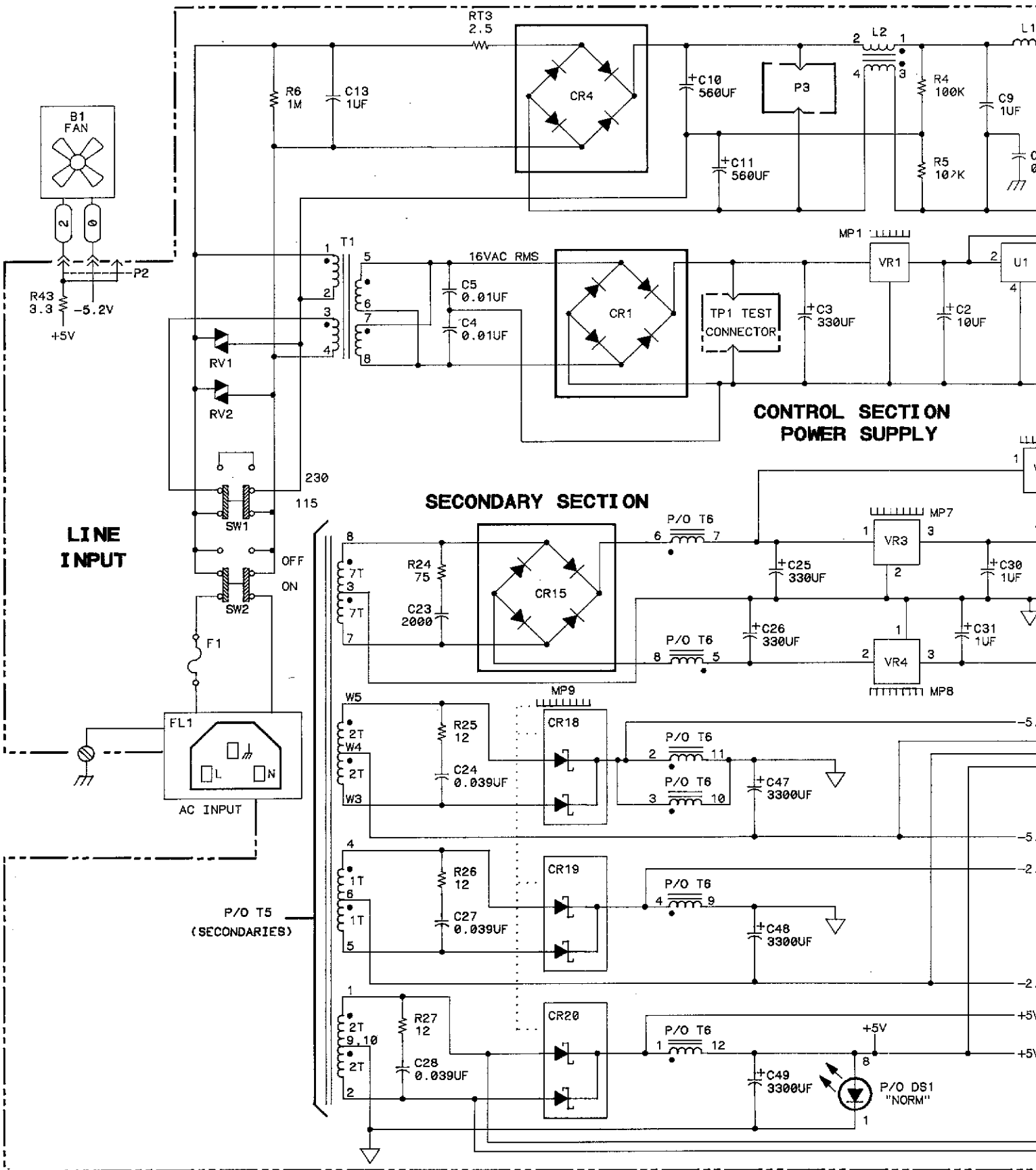
PROBING THESE PINS MAY CAUSE UNWANTED SYMPTOMS.

NOTE 2

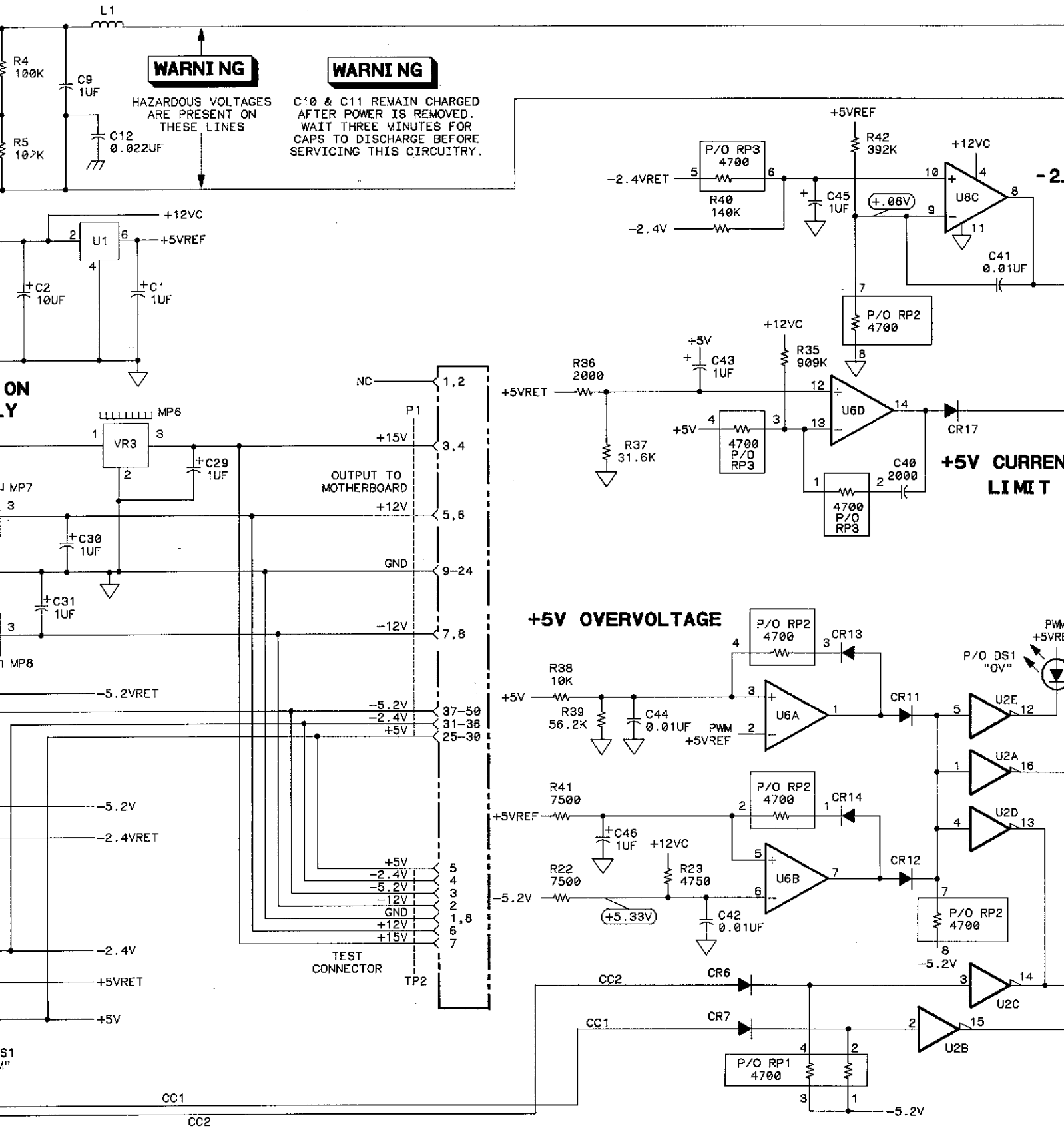
FUNCTIONAL DIAGRAM FOR U3 AND U4.



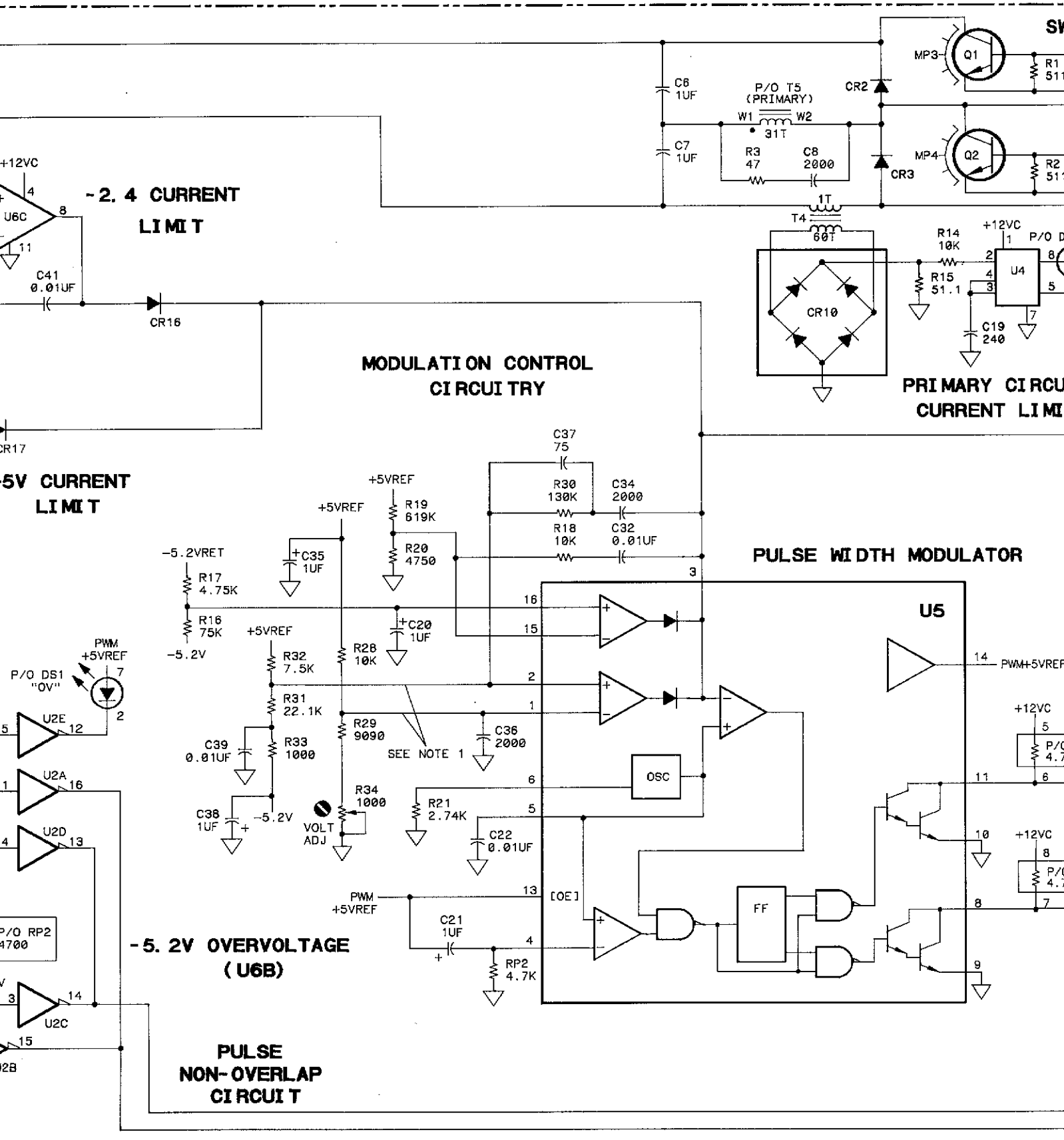
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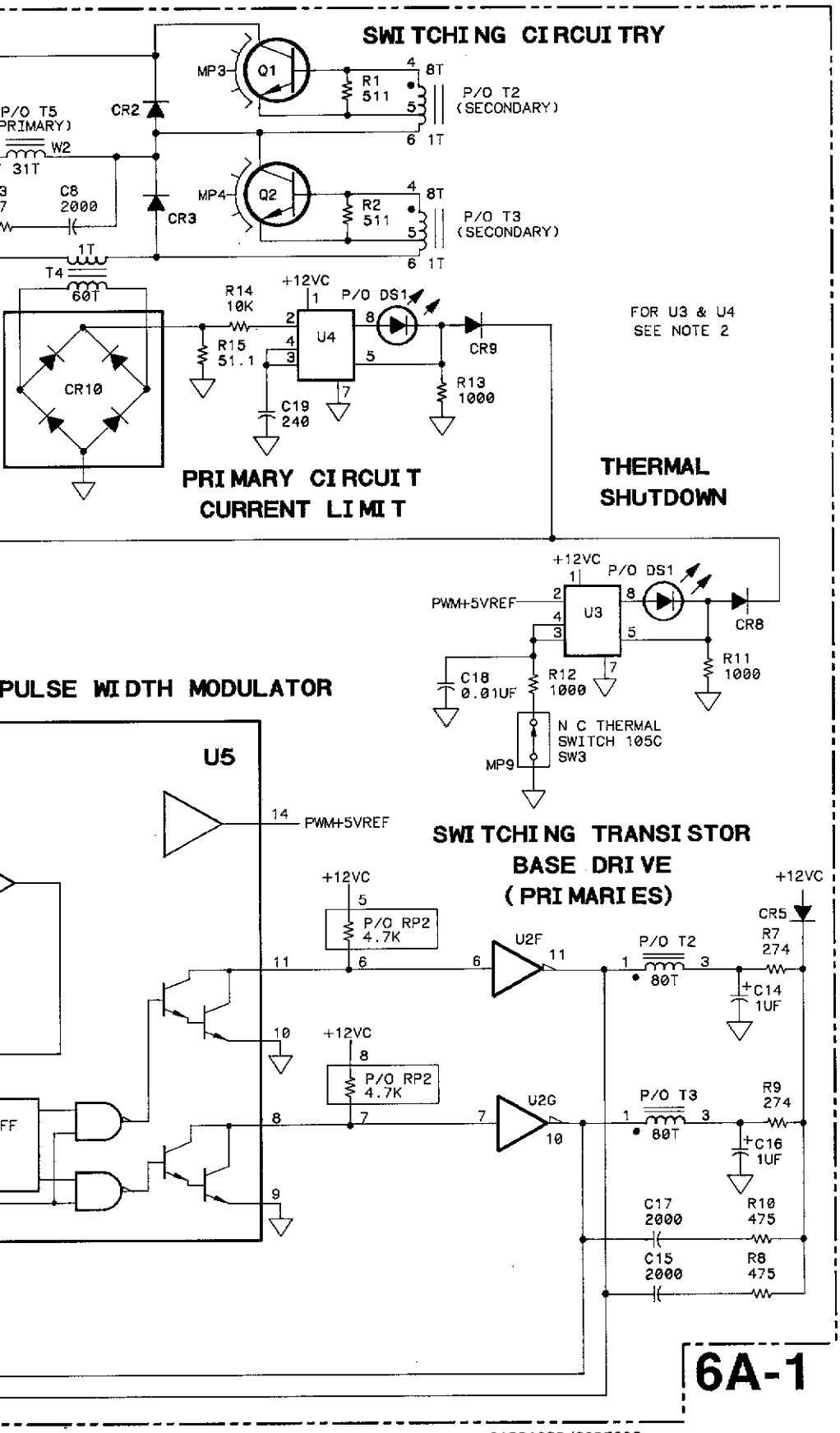
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Schematic 6A-1
Power Supply
6A-15/(6A-16 blank)

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