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Agilent 75000 SERIES C

Agilent E1450 160MHz Timing Module

Hardware Manual

Agilent Technologies

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Edition 2
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Documentation History

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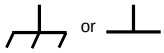
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Instruction manual symbol affixed to product. Indicates that the user must refer to the manual for specific WARNING or CAUTION information to avoid personal injury or damage to the product.



Indicates the field wiring terminal that must be connected to earth ground before operating the equipment—protects against electrical shock in case of fault.



Frame or chassis ground terminal—typically connects to the equipment's metal frame.



Alternating current (AC).



Direct current (DC).



Indicates hazardous voltages.

WARNING Calls attention to a procedure, practice, or condition that could cause bodily injury or death.

CAUTION Calls attention to a procedure, practice, or condition that could possibly cause damage to equipment or permanent loss of data.

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CE

Manufacturer's Name: Agilent Technologies, Incorporated
Manufacturer's Address: 815 – 14th St. SW
Loveland, Colorado 80537
USA

Declares, that the product

Product Name: 160 MHz Timing Module
Model Number: E1450A and associated timing pods E1453A and E1455A
Product Options: *This declaration covers all options of the above product(s).*

Conforms with the following European Directives:

The product herewith complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC (including 93/68/EEC) and carries the CE Marking accordingly.

Conforms with the following product standards:

EMC	Standard	Limit
	IEC 61326-1:1997+A1:1998 / EN 61326-1:1997+A1:1998	
	CISPR 11:1990 / EN 55011:1991	*Group 1 Class A*
	IEC 61000-4-2:1995+A1:1998 / EN 61000-4-2:1995	*4kV CD, 8kV AD*
	IEC 61000-4-3:1995 / EN 61000-4-3:1995	*3 V/m, 80-1000 MHz*
	IEC 61000-4-4:1995 / EN 61000-4-4:1995	*0.5kV signal lines, 1kV power lines*
	IEC 61000-4-5:1995 / EN 61000-4-5:1995	*0.5 kV line-line, 1 kV line-ground*
	IEC 61000-4-6:1996 / EN 61000-4-6:1996	*3V, 0.15-80 MHz I cycle, 100%*
	IEC 61000-4-11:1994 / EN 61000-4-11:1994	*Dips: 30% 10ms; 60% 100ms* *Interrupt > 95%@5000ms*
	Canada: ICES-001:1998	
	Australia/New Zealand: AS/NZS 2064.1	
	The product was tested in a typical configuration with Agilent Technologies test systems.	
Safety	*IEC 61010-1:1990+A1:1992+A2:1995 / EN 61010-1:1993+A2:1995* *Canada: CSA C22.2 No. 1010.1:1992* *UL 3111-1: 1994*	

1 June 2001
Date

Ray Corson
Product Regulations Program Manager

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Chapter 1
Hardware Descriptions

Agilent E1450 Timing Module Description

The Agilent E1450 160 MHz Timing Module is a two-slot, C-size VXIbus register-based module containing a timebase, timing generators, trigger circuits, wait-for-condition circuit, end-if-ready circuits, marker circuits, and sequencer. These circuits supply cycle-by-cycle timing and control information to the Pattern I/O Modules and the device under test. These circuit elements are shown in the block diagram on the following page.

The E1450 provides control signals for the DUT (Device Under Test) and timing for the sequence of patterns that are generated or measured by the E1451/E1452 Pattern I/O modules. The Timing Module can be externally synchronized with external triggers from the DUT or other instrumentation. Triggers can be received from the VXIbus backplane, front panel SMB connectors, or the DUT. Ten qualifier input lines ("Q" lines) and three expression evaluators permit the system to wait for conditions (Boolean

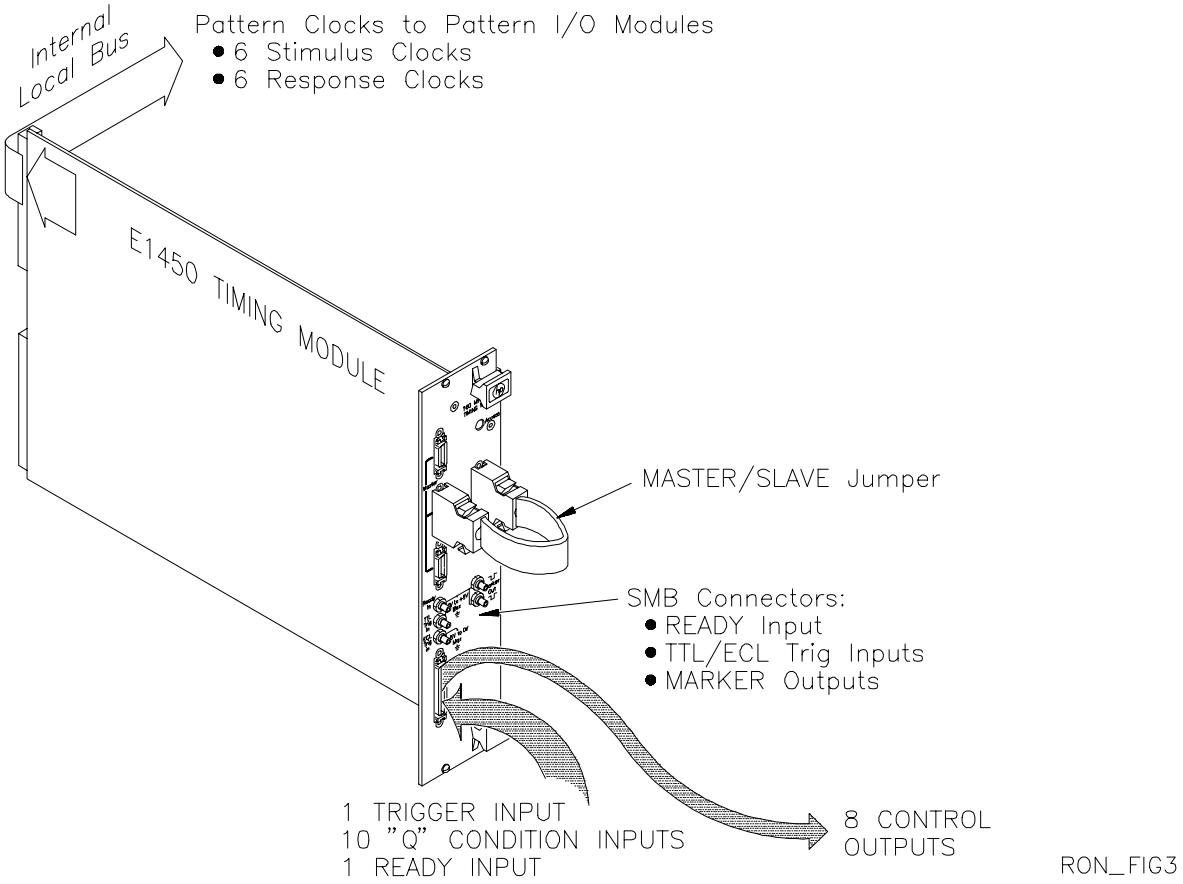


Figure 1-1. Agilent E1450 Timing Module

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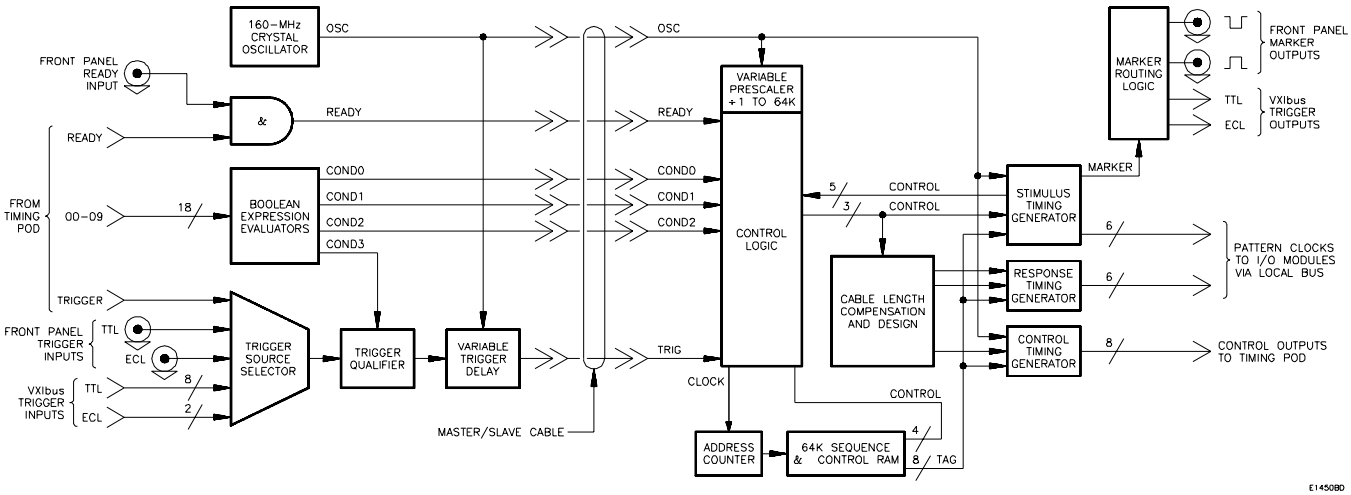


Figure 1-2. Timing Module Block Diagram

combinations of the 10 "Q" lines) within a test. An additional expression evaluator is provided for trigger qualification.

Programmable marker outputs available from SMB connectors on the front panel of the Timing Module or the VXIbus trigger bus lines, can be used to trigger other VXIbus or GP-IB instruments. Bus "wait states" can be implemented with the end-if-ready function in conjunction with the ready input. Emulation of complex bus cycles is made possible with up to 256 timing cycles. The Timing Module also supplies eight general-purpose control signals for strobes, clocks, etc., to the DUT.

The Agilent E1450 provides 12 pattern clocks (six for stimulus, six for response) to one or more E1451/E1452 Pattern I/O Modules in the same VXIbus mainframe for synchronizing ports that must clock together. For large test systems exceeding the capacity of one VXIbus mainframe, a second or third mainframe may be connected using the Agilent E1482 VXIbus Extender. One E1450 Timing Module located in the root mainframe can act as a master for two additional E1450 slaves located in the extended mainframes. Control of a total of 30 Pattern I/O Modules (960 pins) is possible given that the mainframe can deliver sufficient power. Master/slave assignment is done by connecting a master/slave cable from a master connector on the master module to the slave connector on each of the slaves.

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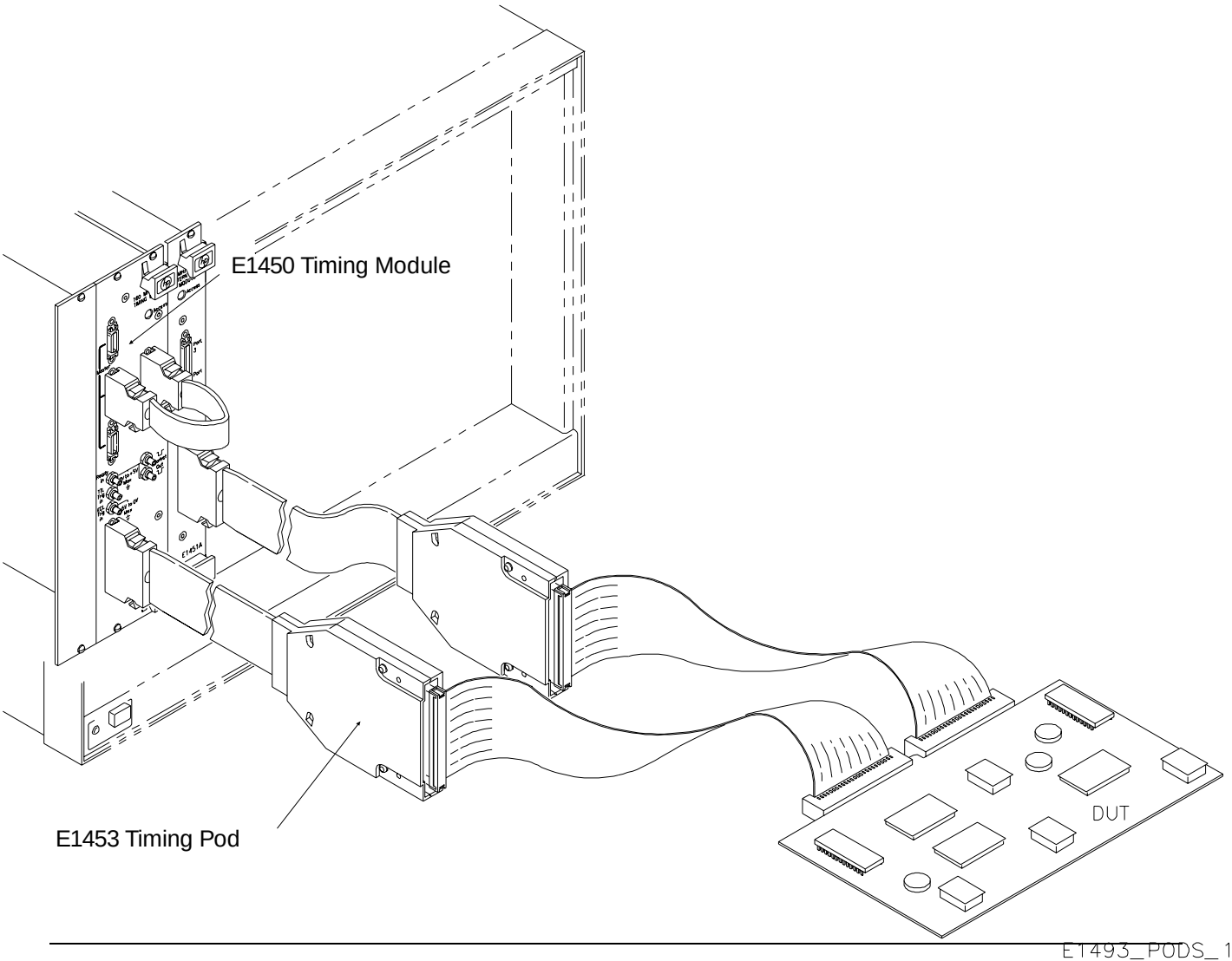
Agilent E1453 Timing Pod Description

The optional E1453 Timing Pod (Figure 1-3) extends measurement accuracy to a DUT located up to two meters from the front panel of the Model D20. The pods are active devices which not only improve the Model D20's ability to drive DUT inputs, but also minimize loading on DUT outputs. Signal delay in the pod and cable is automatically compensated for by the Timing Module when power is applied.

The timing pod buffers the eight control signals out to the DUT as well as the 10 "Q" lines, a ready line and a trigger line into the E1450 module. When the E1453 is not used, the Control and "Q" lines can be accessed via the E1450's pod connector; trigger and ready lines are available on SMB connectors. The pod is supplied with a 2.1-meter cable.

Note

More detailed information about each of the inputs and outputs of the Timing Module is contained in "Specifications", Chapter 3.



E1493_PODS_1

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Chapter 2
Configuration and Wiring

Using this Chapter

This chapter contains configuration and wiring information for the Agilent E1450 Timing Module, the optional Agilent E1453 Timing Pod, and the optional module to DUT interface cables. For complete details on installing this equipment in a C-Size mainframe, refer to the "Agilent 75000 Model D20 Hardware Installation Guide" and the "C-Size VXIbus Systems Installation and Getting Started Guide".

WARNING

SHOCK HAZARD. Only service-trained personnel who are aware of the hazards involved should install, remove, or configure the system. Before you perform any procedures in this guide, disconnect AC power and field wiring from the mainframe.

Caution

STATIC ELECTRICITY. Static electricity is a major cause of component failure. To prevent damage to the electrical components in the mainframe and plug-in modules, observe anti-static techniques whenever handling a module.

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Configuration Information

This section contains information on the module's logical address switch and master/slave cable(s).

Logical Address Guidelines

- The E1450 Timing Module must have a Logical Address that is an Instrument Identifier. An Instrument Identifier is a Logical Address that is an exact multiple of 8 (i.e., 8, 16, 24, 32, . . . 240).
- E1451 Pattern I/O and E1452 Terminating I/O modules must have successive Logical Addresses (LA) beginning with the address of the Instrument Identifier. The LA order must correspond to slot order (that is, lowest LA in lowest numbered slot; highest LA in highest numbered slot). The E1452 Terminating I/O Module must have the highest LA (last in the list).

Logical Address Switch

Figure 2-1 shows a Logical Address Switch. Notice that the switch is made up of 8 switches each having a decimal value. To determine the Logical Address, add the decimal values of all set switches. For example, if you set switches 7 and 3 to "1" (see Figure 2-1), the logical address is 128 + 8 = 136. The GPIB Secondary Address is determined by dividing the Instrument Identifier by 8. For example, if the Instrument Identifer logical address is 136, the Secondary Address is 136 / 8 = 17. Figure 2-2 shows how to set the Logical Address switch.

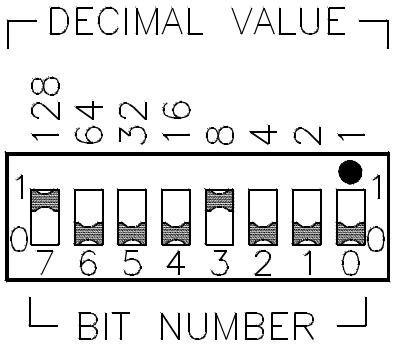


Figure 2-1. Logical Address Switch

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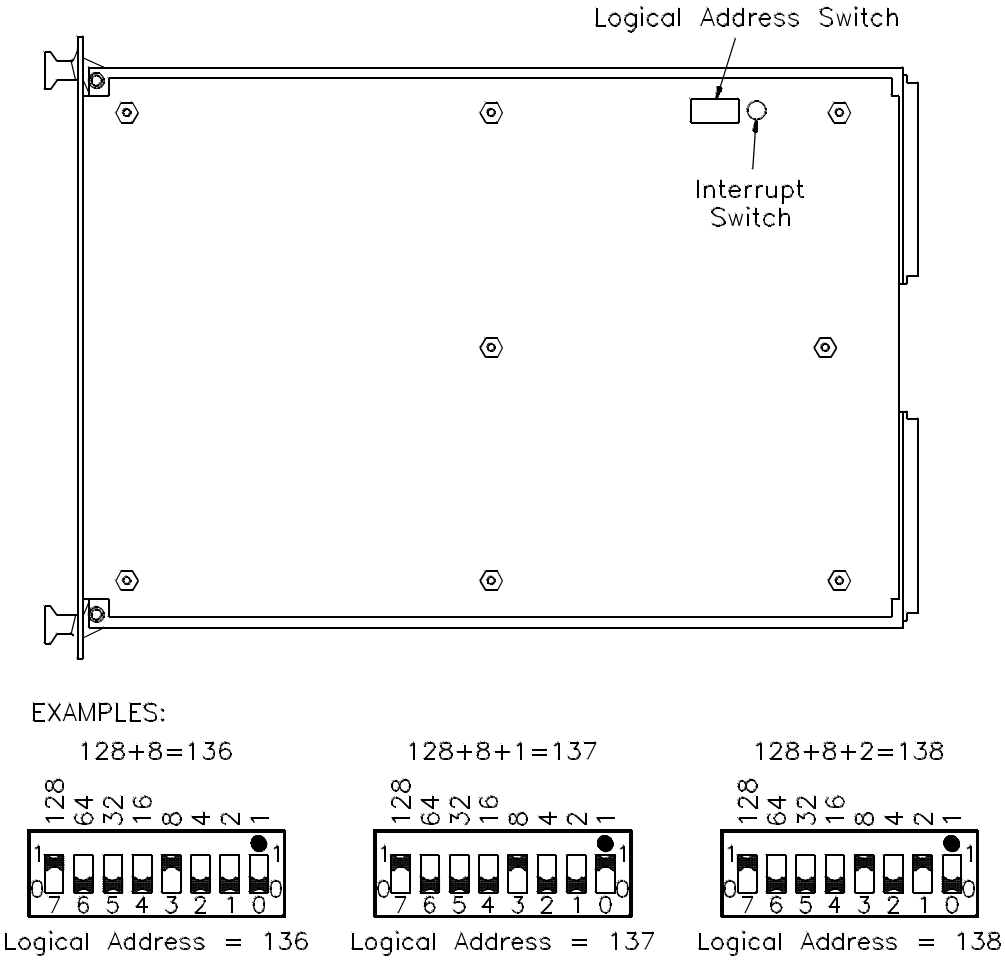


Figure 2-2. Setting a Logical Address Switch

NOTE

Plug-in modules also contain Interrupt Switches. We recommend that you leave these switches set to 1 (factory setting). This causes the modules to use interrupt line 1 which is the default line for most interrupt handlers (command module, embedded controller, etc.). Refer to the "C-Size VXIbus Systems Installation and Getting Started Guide" if you need more information on Interrupt Switches.

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Master/Slave Cables

NOTE

Refer to the "Using Multiple Mainframes Installation and Programming Note" for multiple mainframe Master/Slave Cable information

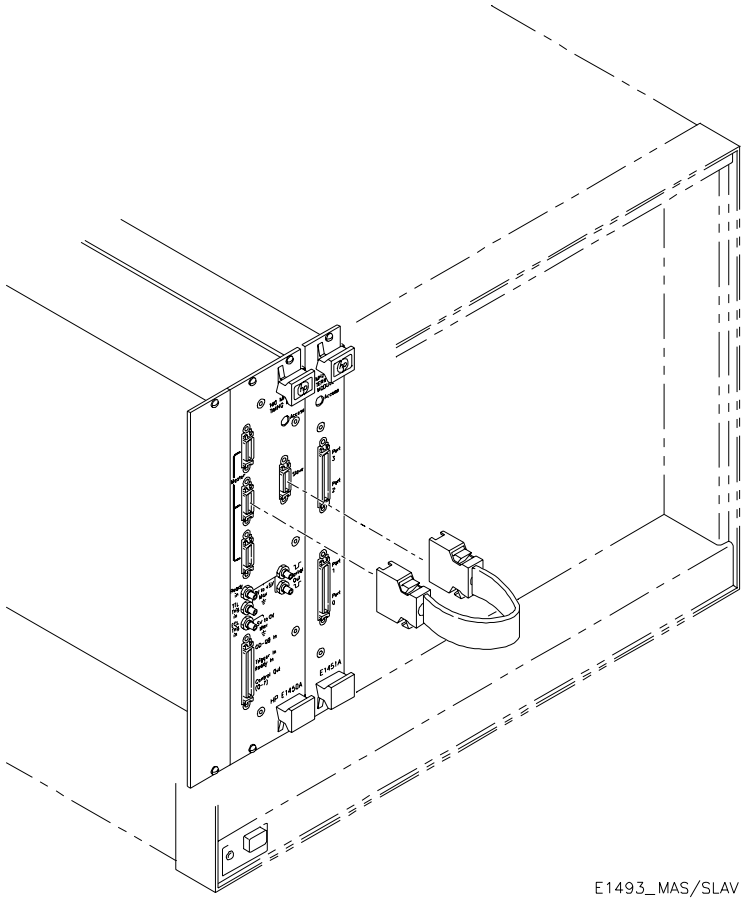


Figure 2-3. Master/Slave Cable Installation (1 Frame)

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Wiring Information

This section shows the module's front panel connector pin-out, the optional E1453 Timing Pod connector pin-out (DUT side), and the optional DUT interface cable wiring.

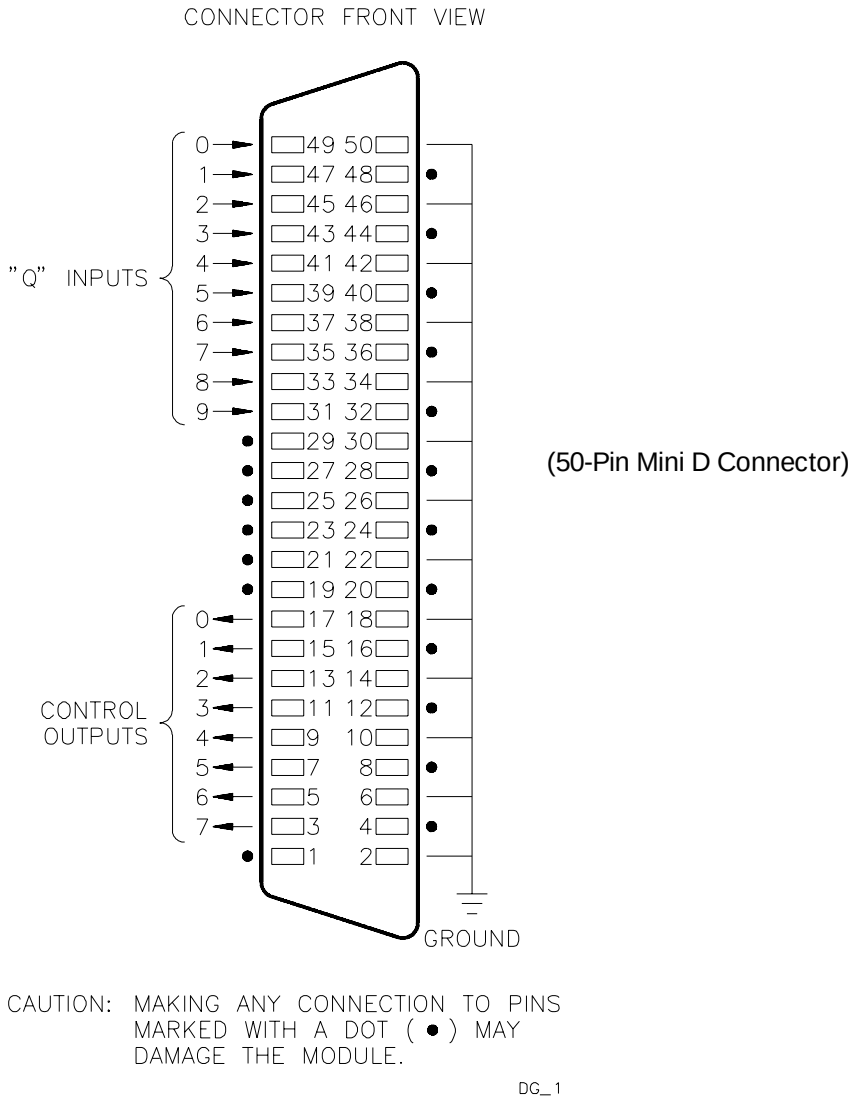


Figure 2-4. E1450 Front Panel DUT Connector

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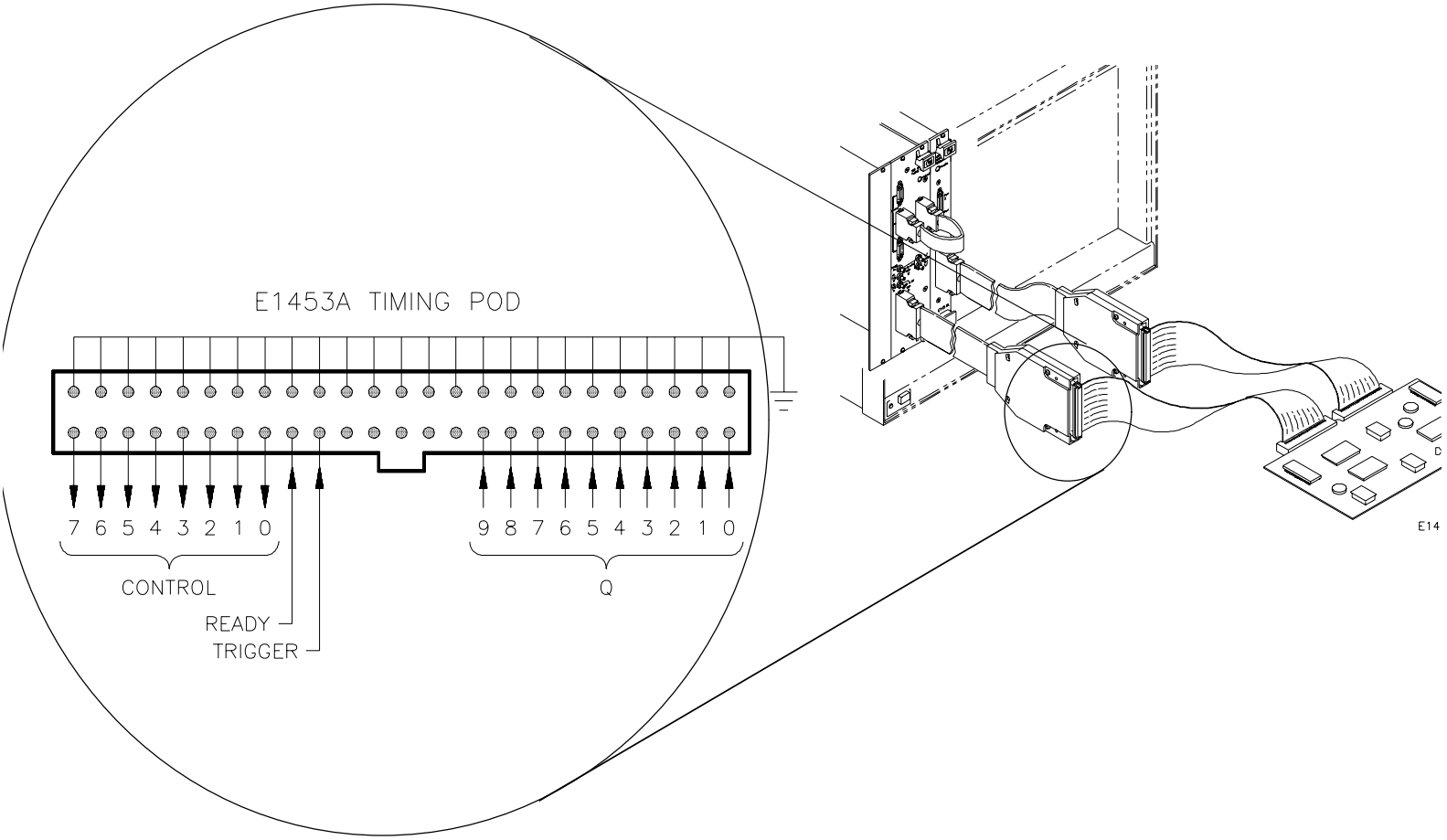
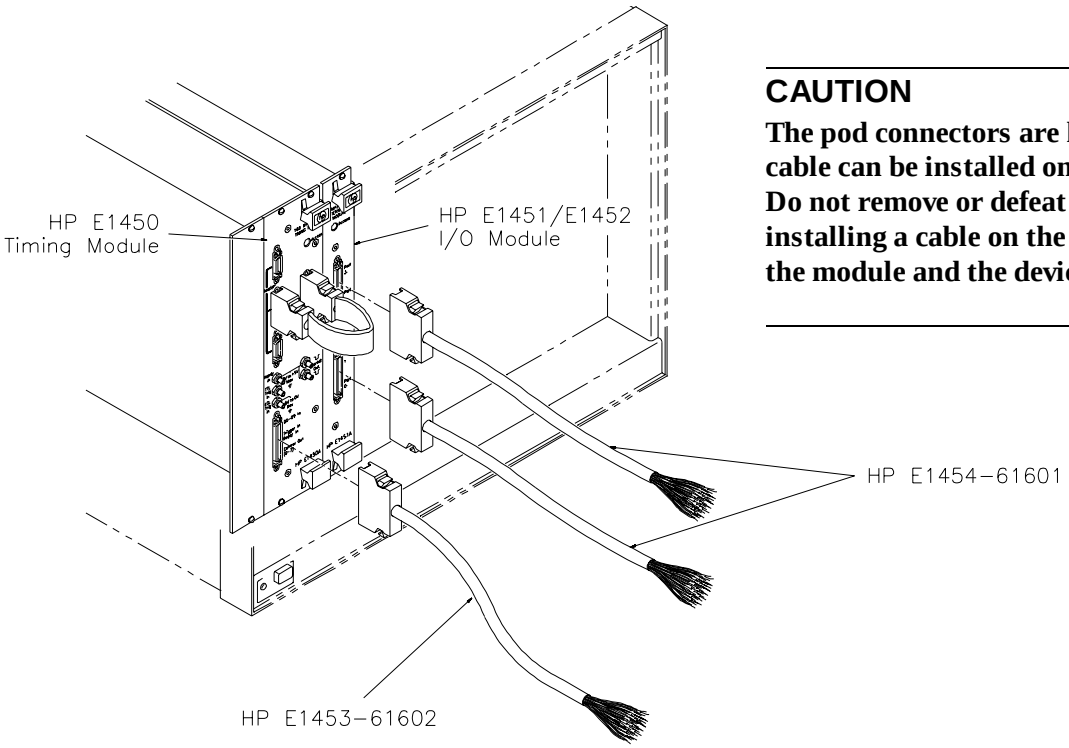


Figure 2-5. E1453 Timing Pod DUT Connector

CAUTION

The pod connectors are keyed so that only the correct pod can be installed on a particular plug-in module. Do not remove or defeat the keys. Defeating a key and installing a pod on the wrong module will damage the module and the pod.

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CAUTION

The pod connectors are keyed so that only the correct cable can be installed on a particular plug-in module. Do not remove or defeat the keys. Defeating a key and installing a cable on the wrong module may damage the module and the device under test.

Figure 2-6. Module to DUT Interface Cables

Table 2-1. Timing Cable (E1453-61602) Wiring

Pin	Color	Signal	Pin	Color	Signal
1	NC		2	YELLOW/BLUE	GROUND
3	BLACK/BROWN	CONTROL 7	4	NC	
5	YELLOW/BROWN	CONTROL 6	6	BLUE/YELLOW	GROUND
7	BLACK/ORANGE	CONTROL 5	8	NC	
9	YELLOW/ORANGE	CONTROL 4	10	YELLOW/GRAY	GROUND
11	BLACK/GREEN	CONTROL 3	12	NC	
13	BLACK/BLUE	CONTROL 2	14	GRAY/YELLOW	GROUND
15	YELLOW/GREEN	CONTROL 1	16	NC	
17	BLACK/GRAY	CONTROL 0	18	VIOLET/BLUE	GROUND
19	NC		20	NC	
21	NC		22	BLUE/VIOLET	GROUND
23	NC		24	NC	
25	NC		26	VIOLET/ORANGE	GROUND
27	NC		28	NC	
29	NC		30	ORANGE/VIOLET	GROUND
31	RED/BLUE	Q9	32	NC	
33	WHITE/BROWN	Q8	34	VIOLET/GREEN	GROUND
35	RED/ORANGE	Q7	36	NC	
37	WHITE/ORANGE	Q6	38	GREEN/VIOLET	GROUND
39	RED/GREEN	Q5	40	NC	
41	WHITE/GREEN	Q4	42	VIOLET/BROWN	GROUND
43	WHITE/BLUE	Q3	44	NC	
45	RED/BROWN	Q2	46	BROWN/VIOLET	GROUND
47	WHITE/GRAY	Q1	48	NC	
49	RED/GRAY	Q0	50	VIOLET/GRAY	GROUND

Notes: NC = No Connection. Colors listed as main body color/stripe color. For example, WHITE/BROWN is a white wire with a brown stripe.

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Recommended Fixturing Techniques

- The pod mating connector (DUT side) is a 50-pin (2 x 25) male dual in-line connector with 0.025-inch (0.64mm) round or square pins on 0.100-inch (2.54mm) centers. This connector is not supplied with the product but is available from electronic supply houses.

- Do not connect the device under test (DUT) directly to the pod connector. Whenever possible, use intermediate wiring between the pod mating connector and the test fixture connector (such as the PC Board Edge Connector shown below). This minimizes the number of insertions/removals made to the pod connector which extends its lifetime.

- Keep all wiring to the DUT as short as possible.

CAUTION

Clearly label the wiring and connectors to identify timing connections and I/O connections. Equipment or DUT damage can occur if these connections are accidentally reversed.

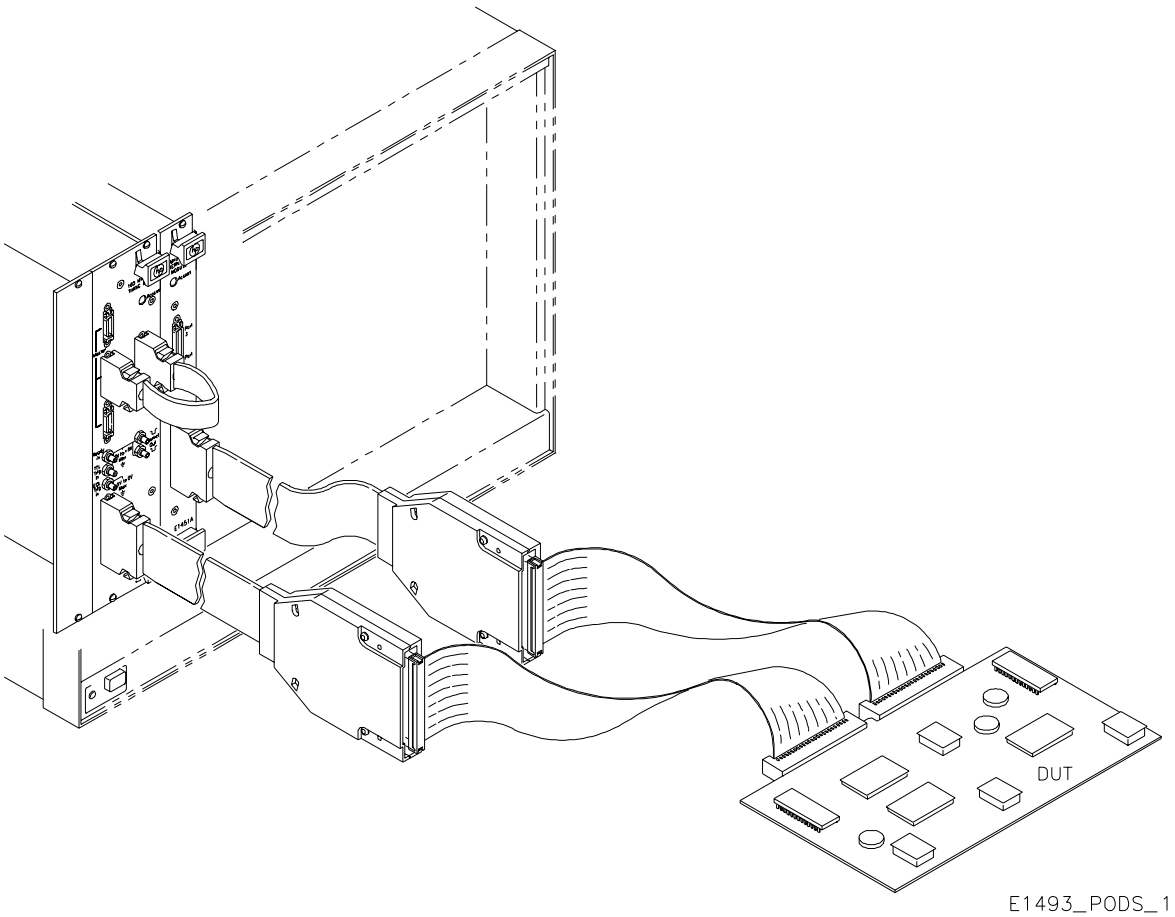


Figure 2-7. Typical Pod to DUT Wiring

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Chapter 3
Register Maps

Using This Chapter

The Agilent E1450 module is a register-based device. This chapter contains the register information for this module.

CAUTION

The register maps in this chapter are included for reference information only. WE DO NOT RECOMMEND THAT YOU ATTEMPT TO PROGRAM THE MODEL D20 AT THE REGISTER LEVEL. Register-based programming of this product is difficult, requires in-depth knowledge of the internal workings of the product, and can result in the erasure of calibration constants requiring the product to be serviced at an Agilent Technologies Service Center. REPAIRS MADE TO THE PRODUCT TO REPLACE CALIBRATION CONSTANTS ERASED BY REGISTER-BASED PROGRAMMING ARE NOT COVERED BY THE PRODUCT WARRANTY.

Register Addresses

The following table shows the E1450 register offset values within the A16 address space (note that a base address must be added to the register offset value to produce the register address).

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Table 2-1. E1450 Registers within A16 Address Space.

Address (Hex)	Register Description
3E - 30	(Unused)
2E	Marker Output Control
2C	Timing Generator Delay
2A	Stimulus T.G. Memory Address
28	Prescaler Divide Ratio
26	Response T.G. Memory Data
24	Stimulus T.G. Memory Data
22	Command Register
20	Status Register 2
1E	Trigger Delay
1C	Q- In & External Trigger Direct Access
1A	Control Output Direct Access
18	Control T.G. Memory Data
16	Truth Table Memory Data
14	Hi-Speed Memory Address
12	Sequencer Memory Data
10	Sequencer Memory Address
0E	Calibration Memory
0C	Branch Destination
0A	(Unused)
08	Trigger In Control
06	Status/Control Register 1
04	VXI Status/Control Register
02	Device Type
00	ID Register

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The Base Address

To access a register, you must specify the register address in either hexadecimal or decimal. The register address consists of a base address plus a register offset. The base address depends on whether the A16 address space is accessed via the Series C E1405 Command Module or via some other controller.

A16 Address Space when not using the E1405 Command Module

When the Command Module or Mainframe is not part of your VXIbus system (ie., you are using an embedded controller), the module's base address is computed by adding the following to the controller specific offset:

hexadecimal	decimal
C000h + (LADDR * 64)h	49,152 + (LADDR * 64)

where C000h (49,152) is the starting location of the register addresses, LADDR is the module's logical address, and 64 is the number of address bytes per register-based module. For example, the module's factory set logical address is 136. If this address is not changed, the module will have a base address consisting of the controller specific offset with the following added to it:

hexadecimal	decimal
C000h + (136 * 64)h C000h + 2200 = E200h	49,152 + (136 * 64) 49,152 + 8704 = 57,856

A16 Address Space Using the Command Module

When the A16 address space is accessed via the Command Module, the module's base address is computed as:

hexadecimal	decimal
1FC000h + (LADDR * 64)h	2,080,768 + (LADDR * 64)

where 1FC000h (2,080,768) is the starting location of the register addresses, LADDR is the module's logical address, and 64 is the number of address bytes per register-based module. For example, the module's factory set logical address is 136. If this address is not changed, the module will have a base address of:

hexadecimal	decimal
1FC000h + (136 * 64)h 1FC000h + 2200h = 1FE200h	2,080,768 + (136 * 64) 2,080,768 + 8704 = 2,089,472

Register Offset

The register offset is the register's location in the block of 64 address bytes (see Table 2-1). For example, the module's Command register has an offset of 22h. When writing a value to this register, this offset is added to the base address to form the register address:

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Address Space	Hexadecimal Register Address	Decimal Register Address
Outside the command module	OFFSET + E200h + 22h = OFFSET + E222h	OFFSET + 57,856 + 34 = OFFSET + 57,890 + 34 = 52,258
Inside the command module	1FE200h + 22h = 1FE222h	2,089,472 + 34 = 2,089,506

Important

These modules are D16-only devices. That is, they may only be accessed via 16-bit words on even addresses. Attempts to access these modules via 8-bit bytes (D8) or 32-bit words (D32) will result in a bus error.

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Register Definitions

All addresses are given in hexadecimal. Unless otherwise noted, register contents are unaffected by hard or soft resets. An "X" denotes bits which are "don't-care".

ID Register (Read Only)

This register defines the module's device class, addressing mode and manufacturer's ID according to the VXIbus specification. Reading this location always gives $FFFF_H$ (corresponding to a register-based device using the A16 address space only and manufactured by Agilent).

Address: Base + 00_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Device Type (Read Only)

This register defines the module's memory requirements and model code according to the VXIbus specification. Reading this location always gives 0152_H (138_{10}).

Address: Base + 02_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	0	0	0	0	0	1	0	1	0	1	0	0	1	0

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VXI Status/Control (Read)

Reading this register gives the module's VXI status.

Read Registers Address: Base + 04_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	MODID*	1	1	1	1	1	1	IEN*	See Below*			1	1	1	1

Bit Definitions

- Bit 15: 0 (= A24/A32 inactive)
- Bit 14: MODID* -- A 1 in this field indicates the device is not selected via the P2 MODID line. A 0 indicates that the device is selected by a high state on the P2 MODID line. Reset value is 1.(the logical complement of the module's MODID input from the Slot-0 module)
- Bits 13-8: 1
- Bit 7: IEN* -- Interrupt Enabled. Enables the Timing I/O Module to interrupt on the VXI backplane. Value of 1 = disabled; 0 = enabled. This bit is set (interrupt disabled) by a hard reset.
- Bits 6-4: INTERRUPT LEVEL--indicate the setting of the interrupt switch:
  001 = Level 1,
  010 = Level 2,
  .
  .
  111 = Level 7)
- Bit 3: 1 (= Ready) Bit 2: 1 (= Passed) Bits 1-0: 1 (E1450 has no built-in self-test)

VXI Status/Control (Write)

Set the Timing Module VXI control bits.

Address: Base + 04_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	IEN*	X	X	X	X	X	X	Soft Reset

Bit Definitions

When writing to this register, all bits are "don't-care" except the following.

- Bit 7: IEN* (0 = Enable interrupts; set to 1 by hard reset)
- Bit 0: SOFT RESET Writing a 1 and then a 0 to this field performs a soft reset of the Timing I/O Module. Notice that bit 7 is set and bit 0 is cleared by a hard reset but not by a soft reset.

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Status/Control # 1 (Read)

Bit 15 of this register is "don't-care" when writing and gives 0 when read. Bits 14-12 are "don't-care" when writing but give status information when read. Bits 11-0 contain various configuration and mode bits and give the last values written when read. Bits 13-0 are set to 0 by hard or soft reset; Bits 13-12 are also cleared by the INIT command.

Address: Base + 06_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	POD PRE-SENT	EOS	BRKPT	INVERT READY	CTG OE	EIDA REG EN	READ POD CAL.	OSC EN*	BRA MODE	AUTO-INCR. ENABLE RD	WR	SEQ. MSB WE*	SEQ. LSB WE*	HSMA MODE	HSMA/ SEQ*

NOTE: All bits are set to 0 after a hard or soft reset.

Bit Definitions

- Bit 14: POD PRESENT (1= there is a pod attached to the module)
- Bit 13: EOS -- End of Sequence--(1 = the sequencer has encountered an end-of-sequence)
- Bit 12: BRKPT -- Breakpoint-- (1 = the sequencer has encountered a breakpoint)
- Bit 11: INVERT READY (1 = both front-panel and pod "Ready" inputs are active low)
- Bit 10: CTG OE (1 = control timing generator outputs are enabled; 0 = the outputs are tri-state)
- Bit 9: EIDA REG EN (1 = External Input Direct Access register is enabled, allowing it to drive various external inputs)
- Bit 8: READ POD (1 = normal pod operation is suspended and the module's control outputs and Q inputs can be used to read the calibration ROM in the pod)
- Bit 7: OSC EN* (0 = master oscillator is enabled)
- Bit 6: BRANCH MODE (1 = the "Marker" bit in sequencer memory also serves as a branch point for looping)
- Bit 5: AUTO-INCR EN (RD) (1 = Sequencer Memory Address is post-incremented each time the sequencer memory, register 12H, is read)
- Bit 4: AUTO-INCR EN (WR) (1 = Sequencer Memory Address is post-incremented each time the sequencer memory, register 12H, is written to)
- Bit 3: WRITE EN* (MSB) (1 = most-significant byte of sequencer memory cannot be written to)
- Bit 2: WRITE EN* (LSB) (1 = least-significant byte of sequencer memory cannot be written to)
- Bit 1: HSMA MODE (1 = normal operation is suspended and the three timing generator memories as well as the truth table memory can be addressed from the High-Speed Memory Address register)
- Bit 0: HSMA/SEQ* (0 = normal operation; 1 = the High-Speed Memory Address register replaces the normal sequencer output)

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Status/Control # 1 (Write)

Address: Base + 06_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	INVERT READY	CTG OE	QDA REG. EN	READ POD CAL.	OSC EN*	BRA MODE	AUTO-INCR. ENABLE RD	AUTO-INCR. ENABLE WR	SEQUENCER WRITE ENABLE MSB	SEQUENCER WRITE ENABLE LSB	HSMA MODE	HSMA/ SEQ*

NOTE: All bits are set to 0 after a hard or soft reset.

Bit Definitions

- INVERT READY -- 0 to 1 = ready. 1 to 0 = ready.
- CTG OE -- Control timing generator output enable. 1 = outputs enabled.
- QDA REG. EN -- 1 = contents of register $1C_H$ are placed permitted to drive certain module inputs (see "External Input Direct Access" register, later in this chapter).
- READ POD CAL. -- 1 = Pod CAL ROM can be read on "Q" inputs.
- BRA MODE -- 0 = normal operation for MARKER sequence bit. 1 = MARKER bit becomes branch function.
- AUTO INCR. ENABLE -- 1 = Sequencer Memory Address (address = 10_H) increments after sequence RAM is read (bit 5) or written (bit 4).
- SEQUENCER WRITE ENABLE -- 1 in either MSB or LSB means that byte in sequencer cannot be written to.
- HSMA MODE -- 0 = normal high-speed memory addressing. 1 = read/write from VXI allowed.
- HSMA/SEQ* -- 1 = high-speed memory address register (14_H) replaces normal sequencer output. Set this bit along with Bit 1 to access the Truth Table RAM (16_H), Control Timing Generator RAM (18_H), Stimulus Timing Generator RAM (24_H), and Response Timing Generator RAM (26_H).

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Trigger Control (Read/Write)

Bits 15-8 of this register are "don't-care" when writing and give 1's when read. Bits 7-0 configure the trigger subsystem and give the last values written when read.

Address: Base + 08_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	QUAL OFF*	TRIG IMMED	TRIG EN.	TRIG SOURCE SELECT				

Bit Definitions

- Bit 7: QUAL OFF* (1 = trigger qualifier is forced to be true regardless of the contents of the truth table memory, resulting in unqualified triggering)
- Bit 6: TRIG IMMED (0-to-1 transition causes an immediate trigger, overriding all other sources)
- Bit 5: TRIG EN (0 = all sources except "Immediate" are disabled)
- Bits 4-0: TRIG SOURCE SELECT (select the trigger source and slope):

00000 = Pod, rising edge
00001 = Pod, falling edge
00010 = Front-panel TTL, rising edge
00011 = Front-panel TTL, falling edge
00100 = Front-panel ECL, rising edge
00101 = Front-panel ECL, falling edge
00110 = VXIbus Backplane ECLTRG0, rising edge
00111 = VXIbus Backplane ECLTRG1, rising edge
01000 = VXIbus Backplane TTLTRG0, falling edge
01001 = VXIbus Backplane TTLTRG1, falling edge
.
.
01111 = VXIbus Backplane TTLTRG7, falling edge
1XXXX = Immediate (module is triggered immediately upon being armed).

Branch Destination (Read/Write)

When Branch Mode is enabled (Bit 6 of Status/Control # 1 is set to 1), then this register supplies the location to which the jump is made when the sequencer encounters a Marker. All 16 bits are significant, and reading this location gives the last value written.

Address: Base + $0C_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Branch Destination															

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Calibration ROM (Read/Write)

CAUTION

DO NOT WRITE TO THIS REGISTER. DOING SO MAY ALTER THE CALIBRATION ROM'S CONTENTS, CAUSING THE MODULE TO FAIL AND REQUIRE FACTORY REPAIR.

Address: Base + $0E_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	X	X	X	X	DATA OUT (Read Only)	DATA IN	CS	SHIFT CLK

NOTE: Bits 0 - 2 are cleared by a hard or soft reset.

Sequencer Memory Address (Read/Write)

This register contains the current address into the sequencer memory. It is used when reading and writing to that memory and it should be set to the first location of a sequence prior to starting that sequence. All 16 bits are significant. If bit 4 of the Status/Control Register # 1 is set (1), the sequencer memory address value will increment by 1 whenever the Sequencer Memory Data register is written to. If bit 5 of the Status/Control Register # 1 is set (1), the sequencer memory address value will increment by 1 whenever the Sequencer Memory Data register is read from.

Address: Base + 10_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Sequencer Memory Address															

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Sequencer Memory Data (Read/Write)

Each location in this memory corresponds to one timing cycle. For that cycle, it defines the location of the first subcycle in the timing generator memories, and determines whether or not to arm the trigger, generate a marker, cause a breakpoint or end the sequence. Bits 13, 12, 9 and 8 are "don't-care" when writing and give 1's when read. All other bits give the last values written when read (assuming no AUTO INCR). If bit 5 of the Status/Control Register # 1 (06_h) is set, the MSByte cannot be written to. If bit 4 of the Status/Control Register # 1 (06_h) is set, the LSByte cannot be written to.

Address: Base + 12_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	BKPT	TRIG ARM	X	X	TRIG OUT (& BRA)	EOS	X	X	Timing Cycle Tag							

Bit Definitions

- Bit 15: BRKPT (1 = a breakpoint will occur before this cycle)
- Bit 14: TRIG ARM (1 = the trigger will be armed before this cycle)
- Bit 11: MARKER (1 = a marker pulse will be generated in this cycle)
- Bit 10: EOS (1 = this cycle is the end of the sequence)
- Bits 7-0: TIMING CYCLE TAG (the first subcycle of this cycle is located at the timing generator memory location which has an address equal to four times this value)

High-Speed Memory Address (Read/Write)

This register can be substituted for the normal sequencer output by setting Bit 0 of Status/Control # 1 to 1. It is also used to address the three timing generator memories and the truth table memories when loading or reading them. When accessing these memories, Bits 1 and 0 of Status/Control # 1 must be set to 1. Bits 13 and 12 of this register are "don't-care" when writing; when read, all 16 bits give the last values written to them.

Address: Base + 14_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	BKPT	TRIG ARM	X	X	TRIG OUT	EOS	High-Speed Memory Address									

Bit Definitions

- Bit 15: BRKPT
- Bit 14: TRIG ARM
- Bit 11: MARKER
- Bit 10: EOS
- Bits 9-0: HIGH-SPEED MEMORY ADDRESS (bits 0 and 1 have no effect when using this regster as sequence memory substitute)

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Truth Table Memory Data (Read/Write)

Bits 15-8 of this register are "don't-care" when writing and give 1's when read. Bit 7 is "don't-care" when writing and gives 0 when read. Bits 6-4 are "don't-care" when writing but give the states of Ready and Trigger inputs when read. Bits 3-0 correspond to the four bits of the truth table memory. Each location of this memory corresponds to a state of the Q9-Q0 inputs and gives the states of the four CONDitions for that state of Q9-Q0. When read, these bits give the values last written to that location. This register cannot be written to unless HSMA MODE (bit 1 in the Status/Control Register # 1) is set.

Address: Base + 16_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	0	FRONT PANEL READY (Read Only)	POD READY (Read Only)	TRIG STATE (Read Only Output of Trigger Mux)	TRIG QUAL	COND 2	COND 1	COND 0

Bit Definitions

- Bit 6: FP READY (gives the state of the front-panel Ready input)
- Bit 5: POD READY (gives the state of the pod's Ready input)
- Bit 4: TRIG STATE (gives the state of the trigger selector's output; this bit is valid even when triggers are disabled)
- Bit 3: COND3 (trigger qualifier function)
- Bit 2: COND2
- Bit 1: COND1
- Bit 0: COND0

Control TG Memory Data (Read/Write)

Each location in this memory corresponds to one subcycle in a timing cycle. For that subcycle, this memory gives the states of the eight control output lines. Bits 15-8 are "don't-care" when writing and give 1's when read. Bits 7-0 correspond to Control Outputs 7-0, respectively, and give the values last written to that location when read.

Address: Base + 18_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	CTG 7	CTG 6	CTG 5	CTG 4	CTG 3	CTG 2	CTG 1	CTG 0

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Control Output Direct Access (Read/Write)

This location allows the control timing generator's output register to be directly read and/or altered. Bits 15-8 of this register are "don't-care" when writing and give 1's when read. Bits 7-0 correspond to Control Outputs 7-0, respectively. In order for the contents of the output register to appear at the module or pod connector, Bit 10 of Status/Control # 1 must be set to 1.

Address: Base + $1A_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	CTG 7	CTG 6	CTG 5	CTG 4	CTG 3	CTG 2	CTG 1	CTG 0

External Input Direct Access (Read/Write)

Bits 15-14 of this register are "don't-care" when writing and 0's when read. If this register is enabled (by setting Bit 9 of Status/Control # 1 to 1) then Bits 13-0 will attempt to drive various module inputs with the contents of the register. This register is connected to the inputs through resistors, however, and therefore may not be able to overdrive inputs which are driven from external sources or the pod. Reading this register while it is enabled gives the last value written to it; reading it while disabled gives 0 on Bits 12 and 10 and the states of the inputs on the remaining bits.

Address: Base + $1C_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	FP READY	FORCE FPECL	FORCE FPTTL	FORCE POD	QC 9	QC 8	QC 7	QC 6	QC 5	QC 4	QC 3	QC 2	QC 1	QC 0

Bit Definitions

- Bit 13: FP READY (front-panel Ready input)
- Bit 12: FORCE FP ECL (1 = front-panel ECL Trigger input is driven high)
- Bit 11: FP TTL (front-panel TTL Trigger input)
- Bit 10: FORCE POD (1 = Trigger and Ready inputs from the pod are driven high)
- Bits 9-0: Q9-Q0, respectively

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Trigger Delay (Read/Write)

The amount by which the minimum trigger latency is increased is N*6.25ns, where N is the 16-bit unsigned integer in this register. There is a delay of up to 2µs (see note below) before new values take effect. Reading this location gives the last value written to it.

Address: Base + $1E_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Trigger Delay															

Additional Delay	**Register Value**
0.00ns	0000
6.25ns	0001
12.50ns	0002
. . .	. . .
409.6µs	FFFF

NOTE: The TTL/ECL translators used have a response time of approximately 2µs.

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Status # 2 (Read Only)

Reading this location gives the status of various state machines in the module.

Address: Base + 20_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	0	0	ADDR OVR	EOC/SEQCLK STATE		OSC ACTIVITY	ADDR OVER	WAIT ACTIVITY	WAIT FOR TRIG	WAIT FOR COND2	WAIT FOR COND1	WAIT FOR COND0	BKPT	EOS	RUN/STOP STATEi	

Bit Definitions

- Bits 15-13: 0
- Bits 12-11: EOC/SEQCLK STATE:
  00 = EOC (End of Cycle)
  x1 = BOC1 (Beginning of Cycle)
  10 = NBE (Neither Beginning nor End of cycle)
- Bit 10: OSC ACTIVITY (1 = there has been at least one master oscillator cycle since the last time this location was read; this bit is cleared after being read)
- Bit 9: ADDR OVER (1 = the stimulus timing generator address counter has advanced past the timing generator memory space; this bit is cleared by hard or soft reset and by the INIT command)
- Bit 8: WAIT ACTIVITY (1 = at least one of this register's Bits 7-4 has been set since the last time this location was read; this bit is cleared after being read)
- Bit 7: WFT (1 = Waiting for Trigger)
- Bit 6: WFC2 (1 = Waiting for COND2)
- Bit 5: WFC1 (1 = Waiting for COND1)
- Bit 4: WFC0 (1 = Waiting for COND0)
- Bit 3: BRKPT --Breakpoint--(1 = the sequencer has encountered a Breakpoint)
- Bit 2: EOS --End of sequence--(1 = the sequencer has encountered an End-of-Sequence)
- Bits 1-0: RUN/STOP STATE:
  00 = Stopped (this state results from an INIT command)
  01 = Paused (this state results from a breakpoint, end- of-sequence, or the SET PAUSE command while running)
  1x = Running (this state results from a RUN command issued after proper initialization or from the Paused state)

NOTE: Bits 10 and 8 are cleared when read.

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Command Register (Read/Write)

Bits 15-2 of this register are "don't-care" when writing and give 1's when read. Bits 1-0 specify a command to the module and give the last values written when read.

Address: Base + 22_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	X	X	X	X	X	X	COMMAND BITS	

Bit Definitions

- Bits 1-0: Command:
  00 = INIT (resets various state machines and clocks the sequencer once to make control information from the first step of the sequence available to the timing generators; aborts any sequence which is in progress)
  01 = RUN (takes the timing generators from a properly initialized or Paused state to the Running condition)
  10 = SET PAUSE (sets a flag which causes the timing generators to enter the Paused state at the end of the current cycle; issuing a RUN command while this flag is set causes one cycle to occur)
  11 = CLEAR PAUSE (clears the pause flag; issuing a RUN command while the flag is cleared causes the sequence to continue)

NOTE: Bits 0 and 1 are cleared (an INIT command is issued) by a hard or soft reset.

Stimulus TG Memory Data (Read/Write)

Each location in this memory corresponds to one subcycle in a timing cycle and gives the states of the six stimulus pattern clocks and six control bits for that subcycle. Bits 15-12 are "don't-care" when writing and give 1's when read. Bits 11-0 give the values last written to them when read (assuming address has not changed and HSMA MODE = 1).

Address: Base + 24_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	TC2*	TC1*	TC0*	TRIG PULSE*	NEOCIR	NEOC	OUT TICK5	OUT TICK4	OUT TICK3	OUT TICK2	OUT TICK1	OUT TICK0

Bit Definitions

- Bit 11: TC2* (0 = test COND2 and wait if necessary for it to become true; 1 = ignore COND2)
- Bit 10: TC1* (0 = test COND1 and wait if necessary for it to become true; 1 = ignore COND1)
- Bit 9: TC0* (0 = test COND0 and wait if necessary for it to become true; 1 = ignore COND0)
- Bit 8: TRIG PULSE* (0 = assert the selected backplane ECL trigger bus(es) if the sequencer specifies a marker in this cycle; should be 0 in the first two subcycles of every cycle and 1 in the remaining subcycles)
- Bit 7: NEOCIR --End if ready--(1 = the next subcycle will be the current cycle's last if the Ready input(s) are true).
- Bit 6: NEOC (1 = the next subcycle will be the current cycle's last, unconditionally)

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- Bits 5-0: SPC 5-0, respectively (states of the Stimulus Pattern Clocks; each should be set in exactly one subcycle of any cycle)

Response TG Memory Data (Read/Write)

Each location in this memory corresponds to one subcycle in a timing cycle and gives the states of the six response pattern clocks for that subcycle. Bits 15-7 are "don't-care" when writing and give 1's when read. Bits 5-0 give the values last written to them when read.

Address: Base + 26_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	X	X	IN TICK5	IN TICK4	IN TICK3	IN TICK2	IN TICK1	IN TICK0

Bit Definitions

- Bits 5-0: RPC 5-0, respectively (states of the Response Pattern Clocks; each should be set in exactly one subcycle of any cycle)

Prescaler Divide Ratio (Read/Write)

Each subcycle of every timing cycle will have a duration which is (N+ 1)*6.25ns, where N is the 16-bit unsigned integer in this register. There is a delay of up to 2us before new values take effect. Reading this location gives the last value written.

Address: Base + 28_H																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	Prescaler Divide Ratio															

Value = N - 1 Where: N is the desired ratio. N can range from 1 to 65,536.

Stimulus TG Memory Address (Read Only)

Bits 15-10 give 1's when read; Bits 9-0 give the current state of the stimulus timing generator's address counter. (Readback of the main high-speed address counter.)

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Address: Base + $2A_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	T.G. Memory Address									

Timing Generator Delay (Read/Write)

Bits 15-8 of this register are "don't-care" when writing and give 1's when read. Bits 7-4 set the Control Timing Generator's delay and Bits 3-0 set the Response Timing Generator's delay. Bits 7-0 give the last values written to them when read.

Address: Base + $2C_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	X	X	CONTROL TG DELAY				RESPONSE TG DELAY			

Bit Definitions

- Bits 7-4: CONTROL TG DELAY
  0000 = Minimum
  0001 = Minimum + 1.56ns
  0010 = Minimum + 3.13ns
  .
  .
  1111 = Minimum + 23.44ns

- Bits 3-0: RESPONSE TG DELAY
  0000 = Minimum
  0001 = Minimum + 6.25ns
  0010 = Minimum + 12.5ns ...
  .
  .
  1011 = Minimum + 68.75ns
  11xx = Illegal

Trigger Output Control

Bits 15-10 of this register are "don't-care" when writing and give 1's when read. Bits 9-0 specify which, if any, of the backplane trigger busses are to be driven with the marker pulse, and give the last values written when read.

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Address: Base + $2E_H$																
Bit #	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	X	X	X	X	X	X	ECLTRG n ENABLES		TTLTRGn ENABLES							

Bit Definitions

- Bit 9: ECLTRG1 ENABLE (1 = marker pulse drives ECLTRG1)
- Bit 8: ECLTRG0 ENABLE (1 = marker pulse drives ECLTRG0)
- Bit n: TTLTRGn ENABLE, n = 0-7 (1 = marker pulse drives TTLTRGn)

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Appendix A
Agilent E1450 160 MHz Timing Module Specifications

Sequencer Specifications

Memory Depth: 65,536 (64k) vectors. Multiple test sequences may co-reside in memory.

Functions: Timing Cycle Selection, Stopping Point, Breakpoints, Markers, and Trigger Arming, all programmable on a cycle-by-cycle basis.

Timebase Specifications

Timing Cycle Duration:
Minimum: 50ns or 4 Subcycles, whichever is greater
Maximum: 1024 Subcycles (see NUMBER OF TIMING CYCLES below)
Resolution: One Subcycle

Subcycle Period:
Minimum: 6.25ns
Maximum: 409.6µs
Resolution: 6.25ns
Accuracy: 0.01%

Number Of Timing Cycles: Up to 256. The total length of all Timing Cycles may not exceed 1024 Subcycles.

Stimulus Timing Generator Specifications

Function: Provides six Stimulus Pattern Clock signals which define edge placements for E1451A/52A Pattern I/O Ports configured in Stimulus mode. (Each I/O Port is programmed to use one Pattern Clock as its timing reference.) Pattern Clocks are independent of each other and may have different delays in different Timing Cycles.

Stimulus Pattern Clock Delay (from beginning of Timing Cycle)
Minimum: 0 Subcycles
Maximum: Timing Cycle Duration - 1 Subcycle
Resolution: 1 Subcycle
NOTE: No sequence of Timing Cycles may be allowed to cause Pattern Clocks to occur less than 50ns apart.

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Response Timing Generator Specifications

Function: Provides six Response Pattern Clock signals which define sampling points for E1451/52 Pattern I/O Ports configured in Response mode. (Each I/O Port is programmed to use one Pattern Clock as its timing reference.) Pattern Clocks are independent of each other and may have different delays in different Timing Cycles. The Response Timing Generator is automatically delayed from the Stimulus Timing Generator by an amount equal to the round-trip delay to the DUT. The timing frame-of-reference is thus moved to the location of the DUT, up to 2.1 meters from the mainframe (when using pods).

Response Pattern Clock Delay (from beginning of Timing Cycle)

Minimum: 0 Subcycles
Maximum: Timing Cycle Duration - 1 Subcycle
Resolution: 1 Subcycle
NOTE: Each Timing Cycle must have exactly one Pattern Clock; no sequence of Timing Cycles may cause Pattern Clocks to occur less than 50ns apart.

Control Timing Generator Specifications

Function: Provides 8 general-purpose Control Signals to the DUT via the front-panel pod connector (or E1453 Pod, if present). Control waveforms can have multiple transitions in each cycle, and may differ from cycle to cycle. These outputs can be set directly and enabled or tri-stated programmatically. The Control Timing Generator is automatically delayed relative to the Stimulus Timing Generator to compensate for delays through the backplane and E1451/52 Pattern I/O Ports (and differences in pod delays, if pods are used in the system). This minimizes skew between Pattern and Control outputs.

Control Signal Edge Timing:

Minimum Delay (from beginning of Timing Cycle): 0 Subcycles
Maximum Delay: Timing Cycle Duration - 1 Subcycle
Resolution: 1 Subcycle
Minimum Programmable Pulse Width (high or low): 12.5ns
Skew:
Control to Control or E1451/E1452 output: 6ns, max.*
Control to Control, same E1450: 3ns, typical
Risetime: < 5ns, typical
Falltime: < 5ns, typical

** Specification assumes all Master/Slave cables are the same length.*

Output Levels

E1450A Module Outputs:

Maximum Continuous Output Current: ± 24mA per line
High, Open-Circuit: 4.4V, min.
Low, Open-Circuit: 0.1V, max.
Output Impedance: 50Ω, typical

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Capacitance (outputs disabled): < 20pF, typical

E1453 Pod Outputs:

Maximum Continuous Output Current: ± 24mA per line
High, Open-Circuit: 4.3V, min.
High, Sourcing 24mA: 3.7V, min.
Low, Open-Circuit: 0.1V, max.
Low, Sinking 24mA: 0.44V, max
Capacitance (outputs disabled): < 15pF, typical

Trigger Specifications

Function: The Sequencer can be programmed to Arm the Trigger system at the beginning of any Timing Cycle. When this occurs, the system enters the Waiting-for-Trigger state and all Timing Generators stop. Once a trigger is received from the selected source and delayed by a programmable amount, the Timing Generators resume operation. If the delay for a certain trigger event expires before the system is in the Waiting-for-Trigger state, then that trigger will have no effect. If a second trigger is received before the delay for a previous trigger has expired, the second trigger will have no effect.

Trigger Sources: Eight VXI TTL trigger busses, two VXI ECL trigger busses, TTL- and ECL-compatible front-panel coaxial connectors (SMB-type), and a TTL-compatible input on E1453 Pod (if present). There is also an "Immediate" source which has the effect of triggering the system immediately upon entering the Waiting-for-Trigger state. Finally, the system can be triggered programmatically, regardless of the selected source.

Trigger Slopes: The VXI ECL and TTL inputs are sensitive to rising and falling edges, respectively. Coaxial and Pod inputs can be programmed to be sensitive to rising or falling edges. There is no slope associated with the "Immediate" source.

Trigger Qualification: Triggers from any source but "Immediate" can be qualified by a user-defined Boolean expression ("CONDition3") of the ten "Q" inputs. (Refer to "Wait-For-Condition Specifications", following, for details of how this expression is defined.) When the "Q" inputs are in a state which makes the expression true, triggers are recognized; when the expression is false, triggers have no effect. This function can be programmatically disabled, resulting in unqualified triggering. Triggers from the "Immediate" source are always unqualified.

Programmable Trigger Delay: The latency time of any trigger source but "Immediate" can be programmatically increased by 0 to 409.59375µs in steps of 6.25ns. See "Trigger Timing" (following) for un-delayed latency times.

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Trigger Input Levels And Loading

VXIbus TTL and ECL inputs: meet VXIbus specifications

Front-panel TTL coaxial

High:> 2.0V (internal 50kΩ pull-up)

Low: < 0.8V at < 250mA

Capacitance: < 10pF, typical

Front-panel ECL coaxial

High:> -1.07V at < 150µA

Low: < -1.48V at ≅ 1.5µA (internal 50kΩ pull-down)

Capacitance: < 10pF, typical

Pod TTL input

High:> 2.0V (internal 50kΩ pull-up)

Low: < 0.8V at < 3.35mA

Capacitance: < 10pF, typical

Trigger Timing:

Minimum Pulse Width (High or Low)

VXIbus TTL and ECL inputs: meet VXIbus specifications

Front-panel TTL: 6ns

Front-panel ECL: 4ns

Pod TTL input: 6ns

Minimum Time Between Triggers: 12.5ns + Programmed Trigger Delay.

Latency Time:

Defined as the time which elapses from a (qualified) trigger from the specified source to the specified Control outputs, with Trigger Delay programmed to 0. Latency from the "Immediate" source is 0; others are given by the table below. Latency times in the table consist of fixed delays which vary from unit to unit plus 6.3ns non-cumulative jitter.

	Trigger Source				
	VXI TTL	VXI ECL	Front Panel TTL	Front Panel ECL	Pod TTL
To E1450 Outputs (min) (max)	79ns 93ns	75ns 87ns	76ns 88ns	74ns 86ns	n/a n/a
To E1453 Outputs (min) (max)	99ns 113ns	95ns 107ns	96ns 108ns	94ns 106ns	106ns 119ns

Trigger Qualifier Timing: Setup time is defined as how long the "Q" inputs must be stable before trigger edge from the specified source. Hold time is defined as how long the "Q" inputs must remain stable after a trigger edge from the specified source.

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	Trigger Source				
	VXI TTL	VXI ECL	Front Panel TTL	Front Panel ECL	Pod TTL
E1450 "Q" Inputs (setup) (hold)	3ns 9ns	7ns 3ns	6ns 4ns	8ns 2ns	n/a n/a
E1453 "Q" Inputs (setup) (hold)	20ns -3ns	24ns -9ns	24ns -8ns	25ns -10ns	12ns 2ns

Wait-for-condition Specifications

Function: The E1450 contains four Expression Evaluators which continually evaluate user-defined Boolean expressions whose variables are the states of the ten "Q" input lines. One evaluator, named "CONDition3", produces the trigger qualifier (see TRIGGER SPECIFICATIONS above); the other three, named "CONDition0", "CONDition1 ", and "CONDition2", are available for general synchronization and handshaking. The E1450's Timing Generators can be programmed to test any combination (including none) of CONDition0 through CONDition2 at the end of any Subcycle of any Timing Cycle. If any of the tested Conditions is false, the system enters the Waiting-for-Condition state and the Timing Generators stop. Operation resumes once all tested conditions become true.

Accepted Expression Elements (firmware)

Variables: "Q0", "Q1", ..., and "Q9", corresponding to the ten "Q" inputs
Operators: "AND", "OR", "EXOR", and "NOT"
Constants: "T" (for True) and "F" (for False)
Parentheses: "(" and ")" to bound expressions and indicate evaluation order

"Q" Input Levels And Loading

E1450 Module Inputs
- High:> 2.0V (internal pull-up)
- Low: < 0.8V at < 250µA
- Capacitance: < 10pF, typical

E1453 Pod Inputs
- High:> 2.0V (internal pull-up)
- Low: < 0.8V at < 150µA
- Capacitance: < 10pF, typical

"Q" Input Timing: The following definitions apply to a Condition which is tested in a certain Subcycle: Setup time is how long the "Q" lines (at the specified input) must satisfy the condition before the end of that Subcycle (as observed at the specified control output). Hold time is how long the condition must remain satisfied after that Subcycle. If the system is in the Waiting-for-Condition state, latency time is how long it takes to resume operation once all Conditions are satisfied. Latency time consists of a fixed delay which varies from unit to unit plus 6.3ns non-cumulative jitter.

Without Pod (E1450 "Q" Inputs and Control Outputs)
- Setup: 89ns
- Hold: -71ns
- Latency: 72ns to 88ns

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With Pod (E1453 "Q" Inputs and Control Outputs)
Setup: 126ns
Hold: -103ns
Latency: 104ns to 125ns

End-if-ready Specifications

Function: The End-if-Ready (EIR) flag may be set in any Subcycle of any Timing Cycle (subject to the rules governing Timing Cycle length, Pattern Clock timing and Control Output timing). When this flag is encountered and a Ready condition is indicated via external input(s), then that Timing Cycle will end after that Subcycle. If a Not Ready indication is given, the cycle continues past the EIR flag. With proper programming, this allows a DUT to request "wait states" (up to the maximum defined length for that Timing Cycle) if it is not ready for the next cycle to begin. There is a TTL-compatible Ready coaxial connector (SMB-type) on the E1450 front panel and another on the E1453 Pod. These inputs have internal pull-ups, causing a default Ready indication if left open. Pulling either input low signifies Not Ready. The logic sense of these inputs can be programmatically inverted, and in this case, the unused input must be grounded before the other will be effective. For the front panel coaxial connector, this is done by attaching an SMB-type 50Ω termination or short.

"READY" Input Levels And Loading:
E1450A Front-Panel Coaxial Input
High:> 2.0V (internal pull-up)
Low: < 0.8V at < 250µA
Capacitance: < 10pF, typical
E1453A Pod Input
High:> 2.0V (internal pull-up)
Low: < 0.8V at < 3.35mA
Capacitance: < 10pF, typical

"**READY**" **Input Timing:** The following definitions apply to an EIR flag which is set in a certain Subcycle: Setup time is how long the specified "Ready" input must be stable before the end of that Subcycle (as observed at the specified output) in order to ensure the desired operation. Hold time is how long the input must remain stable after the end of that Subcycle.

E1450 Front-Panel SMB Input/ E1450 "Control" Outputs
Setup: 72ns + 1 Subcycle
Hold: -(58ns + 1 Subcycle)
E1450 Front-Panel SMB Input/ E1453 "Control" Outputs
Setup: 92ns + 1 Subcycle
Hold: -(78ns + 1 Subcycle)
E1453 Input/ E1453A "Control" Outputs
Setup: 104ns + 1 Subcycle
Hold: -(89ns + 1 Subcycle)

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Marker Specifications

Function: The Sequencer can be programmed to produce a Marker signal at any step of the Sequence. This Marker is available as both positive- and negative-going TTL/CMOS-compatible pulses via front-panel coaxial (SMB-type) connectors. It can also be programmatically directed to assert any or all of the VXI trigger busses.

Output Levels:

Front-Panel SMBs

Maximum Continuous Output Current: ± 24 mA

High, Open-Circuit:> 4.4V

Low, Open-Circuit: < 0.1V

Output Impedance: ≅ 50Ω

VXI Trigger Busses: meet VXIbus specifications

Pulse Width:

To Front-Panel SMBs: Duration of Timing Cycle ± 5ns

To VXI TTL Trigger Bus: Duration of Timing Cycle ± 5ns

To VXI ECL Trigger Bus: ≥ 2 Subcycles ± 2ns

(marker asserted for first 2 subcycles only)

Miscellaneous Specifications

Power Requirements:

+ 5V (Excluding Control Output load current): 1.6A peak, 80mA dynamic

-5.2V: 8.9A peak, 150mA dynamic

-2V: 5.9A peak, 150mA dynamic

Cooling:

Average Power/Slot: 32 Watts

Ambient Temperature

Operating: 0 to 55°C

Storage : -40 to 75°C

Humidity: 65% relative from 0 to 40°C

Airflow Required per Slot (for 10°C rise): 2.8 liter/sec at 0.9mm Water

Weight: 3.0 kg

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