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Spartan-6 FPGA Board
XCM-110 Series Rev2
User's Manual

Ver. 2.0



HuMANDATA LTD.

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1. This product uses ordinary off-the-shelf electronic components, and is therefore inappropriate for use in applications that require special quality or reliability and are expected to protect human lives or prevent accidents, such as safety mechanisms in fields including space, aeronautics, medicine, and nuclear power.
2. Do not be used underwater or in high-humidity environments.
3. Do not be used in the presence of corrosive gases, combustible gases, or other flammable gases.
4. Do not turn on power when circuit board surface is in contact with other metal.
5. Do not apply voltage higher than rated voltage.

⚠ Attention

6. This manual may be revised in the future without notice owing to improvements.
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2. HuMANDATA actively publishes, on the Web and in other ways, information considered useful to customers. Examples would be how to use FPGAs and how to use development tools.
3. HuMANDATA makes efforts for the long-term provision of products and for continuing their long-term support.
4. Instead of concealing small product problems and documentation errors, HuMANDATA makes them public.
5. HuMANDATA abides by Japanese law and its spirit. We make no transactions with purchasers who commit illegal acts.

Revision History

Date	Revision	Description
Jul. 3, 2023	v2.0	Revised: Product Revision to Rev2

Introduction

Thank you for purchasing our product XCM-110.
This is an evaluation board equipped with a FPGA Spartan-6, voltage regulators, configuration reset circuit, oscillators and configuration device.
It can provide you with very convenient and easy-to-use development environment.

1. Shared Pins [IMPORTANT]

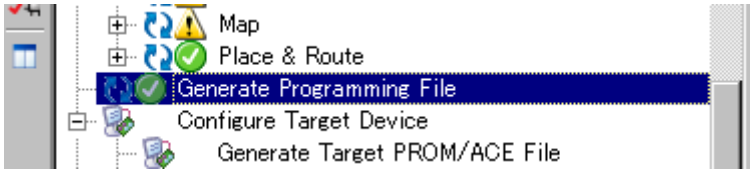
Some Vref pins listed below are connected mutually on this board.

VRFB	V09_REF
A4	K8
A9	Y1
A13	M4
C16	B3

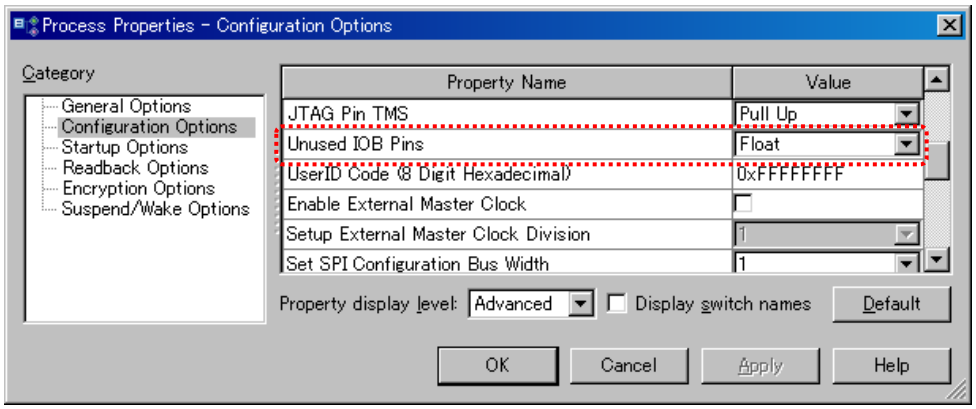
To prevent these pins from being shorted out, it is recommended to set them as "Float" in advance.

Please refer to the following steps and check the "Unused IOB Pins" setting.

1. Right click **[Generate Programming File]** and open **[Process Properties]** window.



2. Confirm **[Unused IOB Pins]** in **[Configuration Options]**.



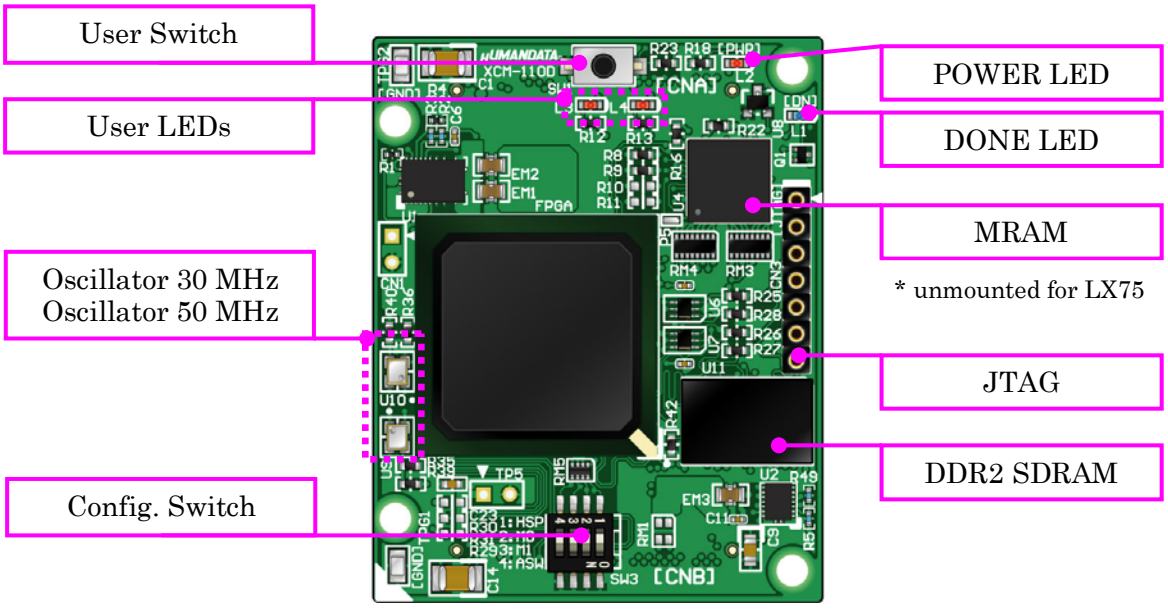
2. Specifications

Model Name	XCM-110-LX75	XCM-110-LX45	XCM-110-LX100	XCM-110-LX150
FPGA	XC6SLX75 -2FGG484C	XC6SLX45 -2FGG484C	XC6SLX100 -2FGG484C	XC6SLX150 -2FGG484C
Config. Device	M25P32-VMF6P (32Mbit)		M25P64-VMF6P (64Mbit)	
DDR2 SDRAM	MT47H32M16NF-25E:H (Micron, 512Mbit: 8Mbit x16 x4 banks)			
MRAM	Unmounted	MR2A16AMA35 (Everspin, 4 Mbit)		
On-Board Clock	50 [MHz], 30 [MHz]			
External Clock Input	User I/Os (CNA-11/12, CNB-11/12)			
Power Input	DC 3.3 [V]			
Dimensions	1.693" x 2.126" (43 x 54 [mm])			
Weight	19 [g] typ.			
User I/Os	128			
User I/O Connectors	FX10A-80P/8-SV1 (Hirose) x 2			
User Switches	2 (Push x 1, Slide x 1)			
User LEDs	2			
PCB	8 Layer FR-4 t1.6 [mm] Immersion gold			
Power-On Reset	240 [ms] typ. (Config. reset signal)			
JTAG Connector	SIL 7-pin socket, 2.54 [mm] pitch			
Status LEDs	Power (red) x1, Done (blue) x1			
Accessories	SIL 7-pin header (Mounted) x1			
	FX10A-80S/8-SV (Hirose) x 2			
RoHS Compliance	YES			

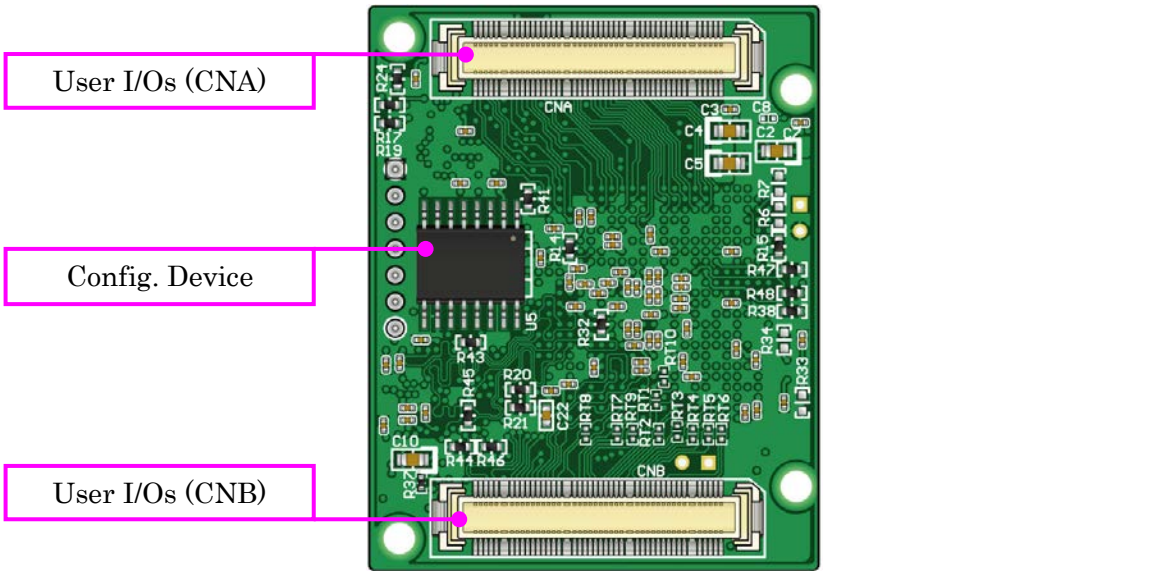
*** There may be cases that these parts and specifications are changed.**

3. Overview

3.1. Name of Parts

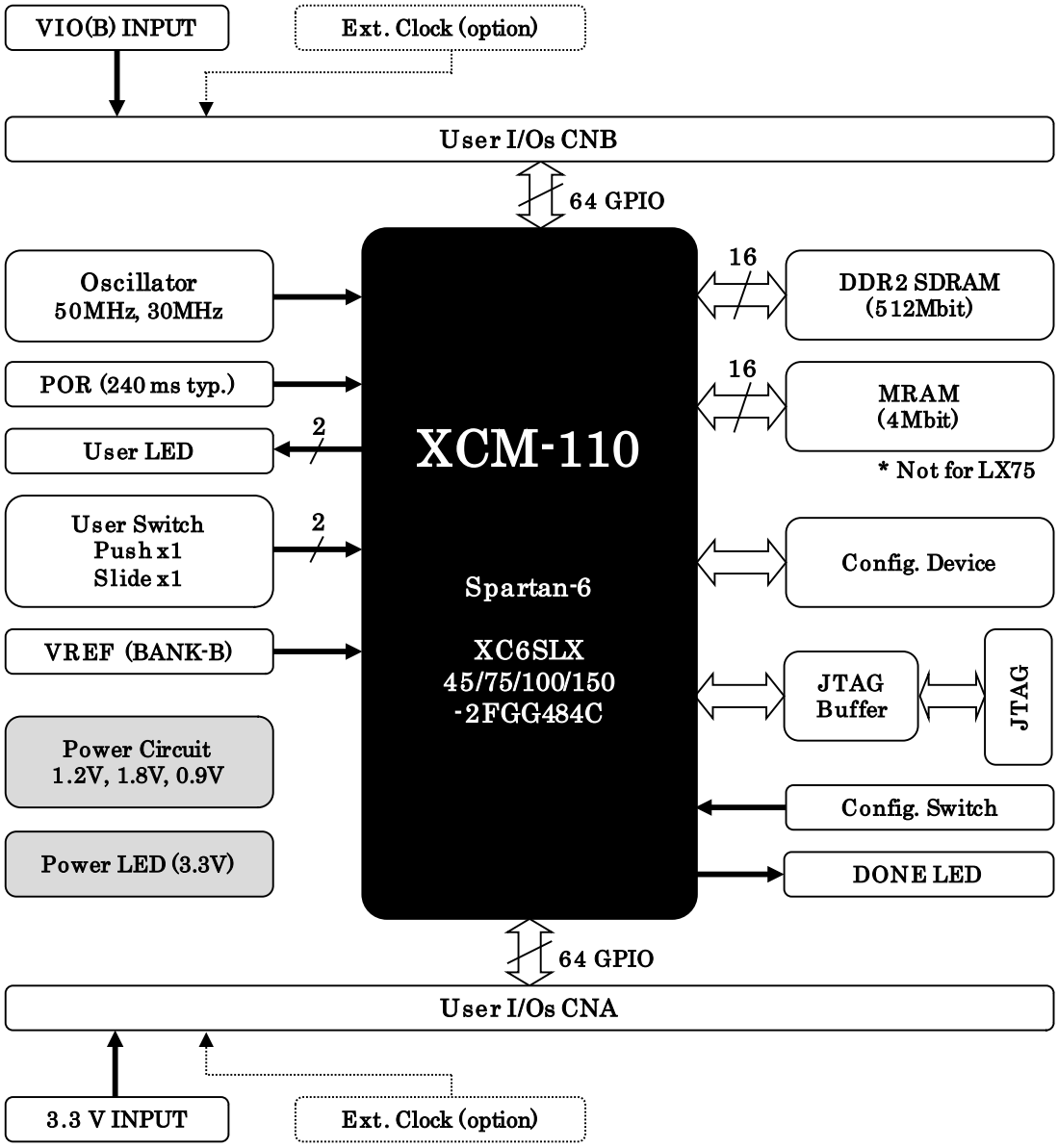


Component Side



Solder Side

3.2. Block Diagram



3.3. Power Supply

This board operates from single DC 3.3 V power supply from CNA and CNB.

Internally required 1.8[V], 1.2[V] and 0.9[V] are generated by on-board voltage regulators.

The external power supply should be sufficient and stabilized. Please do not apply over 3.3V voltage.

VCCIO in BANK B is not connected to 3.3V. Please input given voltage from CNB.

For more details, please refer to circuit schematics and FPGA data sheet.

3.4. Clock

A 50 MHz (U9) and a 30 MHz (U10) oscillator are equipped as on-board clock.
External clock can be input from user I/O connectors (CNA, CNB).
For more details, please refer to a circuit schematic.

3.5. JTAG Connector

JTAG connector is used to configure the FPGA and program the configuration device in-system. Pin assignment is as follows. You can use AMD download cable.

CN3

Pin No.	Signal Name	Direction
1	GND	I/O
2	TCK	IN
3	TDO	OUT
4	TMS	IN
5	VCC	OUT (POW)
6	TDI	IN
7	GND	I/O

Notice

Please pay attention not to attach cables in reverse.

3.6. Configuration Switch (SW3)

The specification of configuration switch is below. “ON” means “Low (Ground)”. For each pins details, please refer to Spartan-6 configuration user guide.

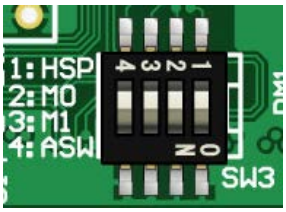
SW3

	4	3	2	1
Net Label	ASW0	X_M1	X_M0	X_HSWAPEN
Function	User	Configuration Mode		HSWAPEN

Configuration Mode

	X_M1	X_M0
Master serial/SPI	ON	OFF
JTAG	OFF	X

ON: Low (0), OFF: High (1), X: Don’t Care



- **ASW0**

  You can use this as a user switch.

- **M1, M0**

  Configuration mode select pins. The modes showed above are a part of all. Generally, users do not need to be attentive to mode setting for JTAG configuration. But for this product, it is recommended to set the mode as shown above.

- **HSWAPEN**

  User I/O pull-up control.
  When low during configuration, enables pull-up resistors in all I/O pins to respective I/O bank VCCO input.

  ON : Pull-ups during configuration
  OFF : No Pull-ups

  For more detail, please refer to Spartan-6 data sheet.

4. FPGA Configuration

To configure the FPGA via JTAG directly, select an FPGA icon detected by Boundary-Scan and assign a bit-stream file.
If configuration is completed successfully, the DONE LED will light up.

5. Configuration Device Programming

An mcs file is required to download an FPGA configuration data to the configuration device via JTAG. To generate an mcs file using iMPACT, please refer to the following steps.

5.1. Generating mcs file

Start iMPACT, and double-click [Create PROM File] and set items as shown below.

Storage Target	: SPI Flash – Configure Single FPGA
Storage Device	: 32M or 64M (set one device)
File Format	: MCS
Others	: any

Select your bit file, and generate MCS file.

5.2. Programming Configuration Device

Assign the mcs file to a Flash icon and choose [SPI PROM – M25P32] or [SPI PROM – M25P64] for device type, then right click and select a command.
Please set FPGA configuration mode to [Master Serial/SPI] mode.

6. Additional Documentation and User Support

The following documents and other supports are available at
https://www.hdl.co.jp/en/spc/XCM/xcm-110/

- Circuit Schematic
- Pin List
- Outline drawing
- Net List

… and more.

Spartan -6 FPGA Board

XCM-110 Series Rev2

User's Manual

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