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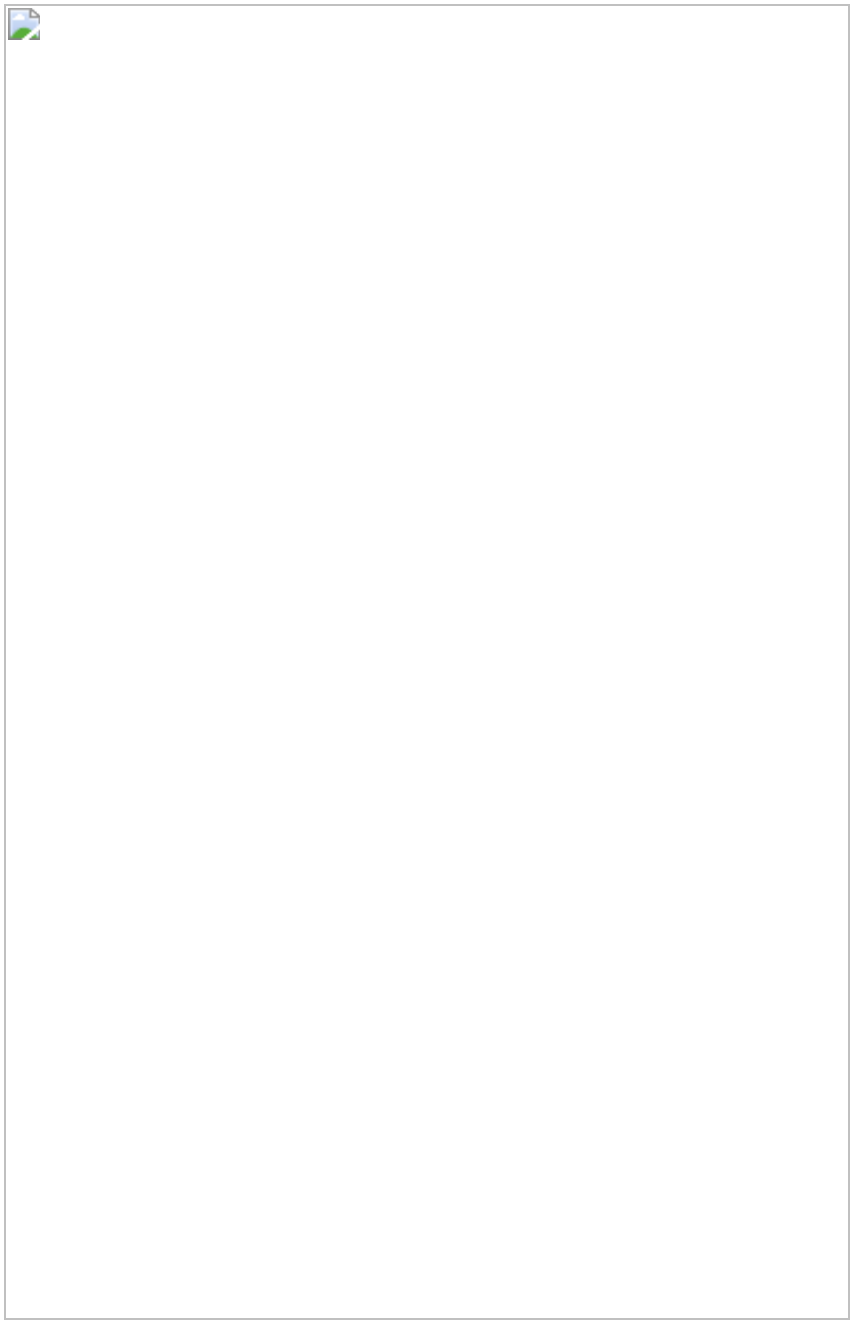
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ICE-DTDM

Digital Tuner Demodulator Module

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The ICE-DTDM is a programmable Digital Tuner Demodulator Module for an ICE processor module site featuring:

- One Xilinx Virtex-II Pro programmed as a data and packet router, sequencer, DDR ram controller, resampler, demodulator and tuner interface
- Eight GC4016 digital tuner chips
- Two 16bit, 32Mby 200MHz DDR SDRAMs for short term memory

The Power-PC core in the Virtex-II Pro runs either a C program or Java Virtual Machine to sequence the processing of data and command packets from the module site as well as specific processing primitives called by the host libraries. The GC4016 tuners are used as hardware accelerators for the software tuner primitives executing in the Power-PC core. This allows a very flexible use of tuner channels to meet a wide variety of processing needs.

Using multi-pass mode through the tuner banks, the module supports

- 4 channels (up to 24MHz BW) at 800MHz input
- 8 channels (up to 12MHz BW) at 400MHz input
- 16 channels (up to 6MHz BW) at 200MHz input
- 32 channels (up to 3MHz BW) at 100MHz input
- 64 channels (up to 1.5MHz BW) at 50MHz input
- 128 channels (up to .75MHz BW) at 25MHz input

Using cascaded multi-pass mode through the tuner banks, the module supports

- 144 channels (up to 400kHz BW) at 100MHz input
- 3000 channels (up to 25kHz BW) at 100MHz input

The Virtex-II Pro fixed point multipliers and look-up tables act as accelerators to demodulator primitives also executing in the Power-PC core. The table driven demodulator algorithms support AM, FM, PM, PSK, QAM and other modulation types. The tight control from the DEMOD primitive helps facilitate burst demod algorithms.

The Virtex-II Pro also supports a 28tap variable rate resampling filter that can process up to 200MSPS. The resampler can be steered by ephemeris calculations, embedded timecode, or an external reference measurement from the host PIC card.



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