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ICS-115 DELTA-SIGMA DAC BOARD

No. 16 Rev. A Interactive Circuits & Systems Ltd.

INTRODUCTION

The ICS-115 is a 32-channel VMEbus DAC board which offers true 16-bit precision and update rates of up to 50 kHz/channel. The use of Delta-Sigma DACs offers a high degree of precision and digital interpolation which moves the aliased image away from the signal band. This significantly relaxes post filtering requirements. A 2-pole reconstruction filter for each DAC output is provided for each channel. The ICS-115 provides differential outputs with high current drives to directly drive large capacitive loads.

To allow fast input of DAC data, the ICS-115 board includes a 64 MBytes/s VME64 interface, a 40 MBytes/s VSB interface and a 32 bit front panel data port (FPDP) capable of sustained data rates up to 80 MBytes/sec. The FPDP protocol is supported by a large number of DSP and Array Processor vendors. The VME64 interface provides both master and slave functions with BLT and MBLT block transfer capabilities. The A32/D32 VSB interface supports block transfer.

The ICS-115 has been designed to simplify complex conversion requirements by offering:

- A large number of channels (4-32 per board);
- 16 bit resolution, with differential outputs;
- Front panel synchronization signals to allow simultaneous sampling over a large number of boards;
- Delta-Sigma DACs which virtually eliminate complex and expensive reconstruction filtering;
- Simultaneous sampling at rates from 4 Hz to 50 kHz;
- 90 dB dynamic range and -90 dB interchannel crosstalk;
- External or programmable internal clock;
- Internal clock resolution of approximately ± 4 Hz;
- 1 MSample on board buffer;
- High speed VMEbus interface with VME64 Master capability;
- High speed VSBbus slave interface;
- High speed 32 bit Front Panel Data Port (FPDP) for direct interface to Mercury, CSPI, SKY, Ariel, and Ixthos array processors as well as other ICS products;
- Ability to bus the FPDP inputs across multiple ICS-115 boards which allows each board to convert any user-selected set of 32 channels from the input data stream.

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SPECIFICATIONS

Analog Specifications

No. of Analog Output Channels:	4, 8, 16, or 32 differential
Analog Connector Type:	Two 44-pin D-Shell Positronix
Output Impedance:	< 1 Ohm
Output Drive:	24 mA max.
Full Scale Output:	5.0 Vpp differential*
Output Conversion Rate:	50 kHz/ch. max.
Output Signal Bandwidth:	22.7 kHz Max.
Dynamic Range (S/N+D):	> 90 dB
Inter-channel Crosstalk:	< -90 dB

Digital Specifications

Sample size:	16 bits		
On Board Storage:	1 MSample		
Programmable decimation factor:	1 to 256		
VMEbus Interface:	A64/A32/A24 D64/D32 MBLT/BLT Master/Slave Full interrupt support		
VSB Interface:	A32/D32 BLT Slave Polled Interrupts		
Front-Panel Interface:	FPDP 32-bit, 20 MHz max, compatible with Mercury, CSPI, SKY, Ariel, and Ixthos FPDP interfaces.		
Environmental:	Operating	Temperature:	0 - 70°C
		Humidity:	0 - 95% RH, non-condensing
	Storage	Temperature:	0 - 70°C
		Humidity:	0 - 95% RH, non-condensing
Power Consumption: (when driving high impedance loads)	+5V @ 4.5 Amps +12V @ 0.1 Amps -12V @ 0.1 Amps		
Board size:	233 x 160 mm VMEbus 6U standard		

* 5.0 Vpp in each differential output leg.

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GENERAL DESCRIPTION

Figure 1 shows a simplified block diagram of the ICS-115 board. The board has up to 32 16-bit Delta-Sigma DACs. A two pole Butterworth filter is applied to the final output of the DACs to further reduce out of band noise. The serial DAC data is supplied by 32 16-bit parallel to serial converters. This converter data is supplied at the sampling rate by a FIFO buffer, which decouples the conversion rate from the input data rate.

Data is supplied to the FIFO buffer from a 1 MSample Swing Buffer; this allows the ICS-115 to be operated in several different modes. In the **continuous** mode of operation, a continuous data stream is fed to the swing buffer. In the **one-shot** mode, the swing buffer is loaded once, and the data is converted once with each application of the trigger. In the **loop mode**, the swing buffer is loaded once, and the data is repeatedly converted after one application of the trigger.

Data is supplied to the ICS-115 in frames. A frame is defined as a set of data in which each data item is to be applied to a DAC, and where each item relates to the same sampling instant. The number of data items in a frame is referred to as the frame length. The frame length may be greater than the number of channels on the ICS-115, since the board has the capability to select a programmable number of channels from the frame for output.

The data input section of the ICS-115 consists of a dual port input buffer, a barrel shifter, and a dual port sequencer. The input buffer is of the swing buffer type; one half is loaded with a frame of data, while the other half is unloaded into the barrel shifter. The sequencer and barrel shifter allow an arbitrary selection of any 32 channels from an input frame whose frame length can be up to 2048 channels. The barrel shifter selects which 16 bits of the 32-bit input stream are to be applied to the DACs, on a channel by channel basis. The data can be supplied from VMEbus, VSB, or from the Front-Panel Data Port (FPDP).

The ICS-115 supports both internal and external clocks. In either case, the clock frequency must be 256 times the desired sampling rate (256 x Fs). The internal clock can be programmed to within approximately 4Hz (relative to the sampling frequency Fs), by writing the appropriate clock frequency program word to the board. The ICS-115 also supports internal and external triggers. The trigger can be configured as edge or level sensitive. An alternate trigger mode is available in which the ICS-115 converts a preset number (user programmable) of frames of data upon application of the trigger.

To synchronize multiple boards, one board is configured as master and all other boards are configured as slaves. The master generates and distributes synchronization signals via the P4 connector on the front panel, which is bussed between boards. These signals ensure simultaneous sampling across all boards and also guarantee that data frames are processed synchronously between all boards in the group.

The ICS-115 has an on-board diagnostic capability which can be used to test both the digital and the analog functioning of the board. In addition, each of the thirty-two channels can be independently muted (set to zero volt output). Figure 2 shows the output section of the ICS-115 board. For the purpose of analog diagnostics, 32 comparators are provided on the board. These are connected between pairs of adjacent channels for each leg of the differential outputs. By comparing the outputs, faults can be localized to one pair of channels.

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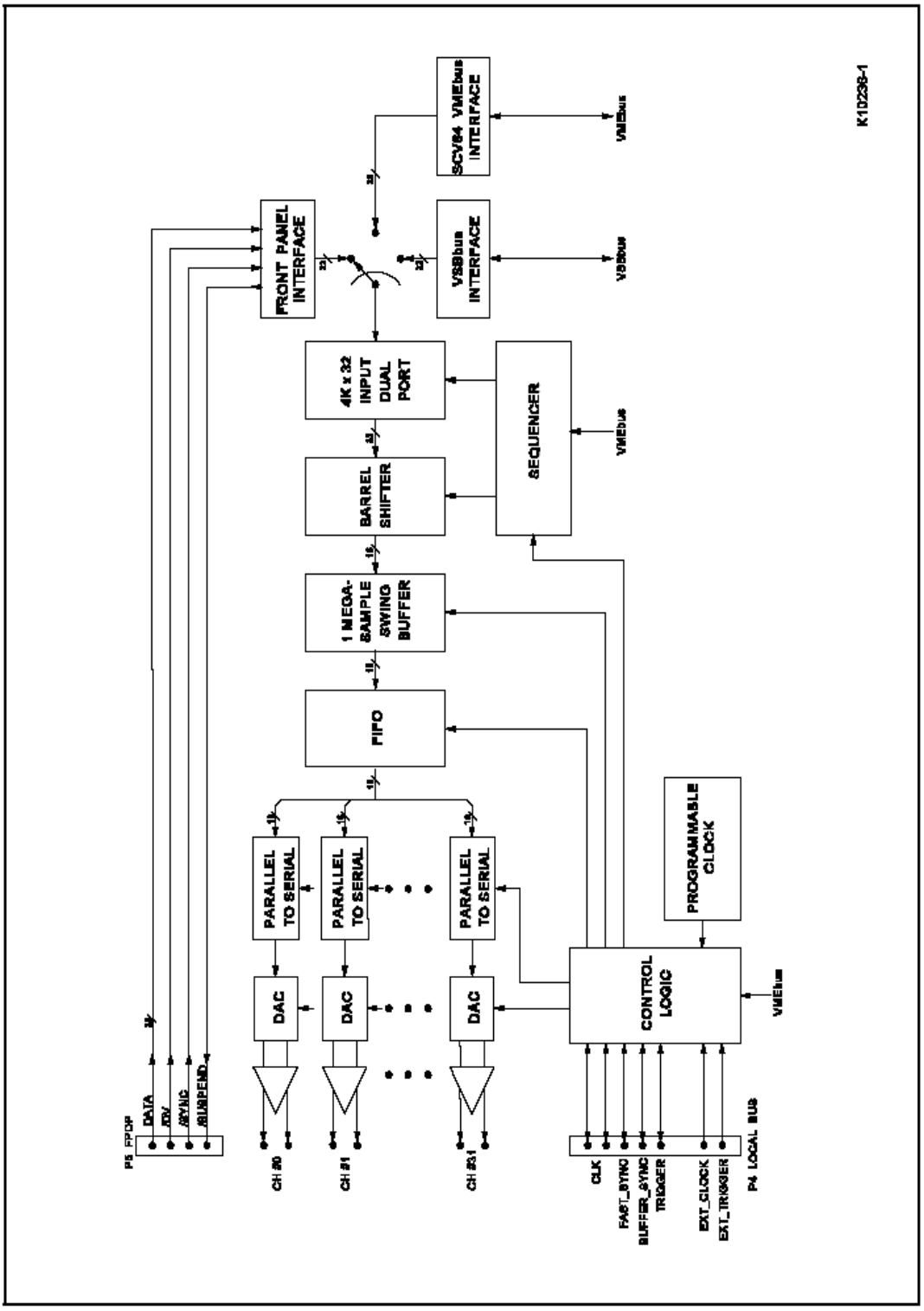


FIGURE 1. ICS-115 Block Diagram

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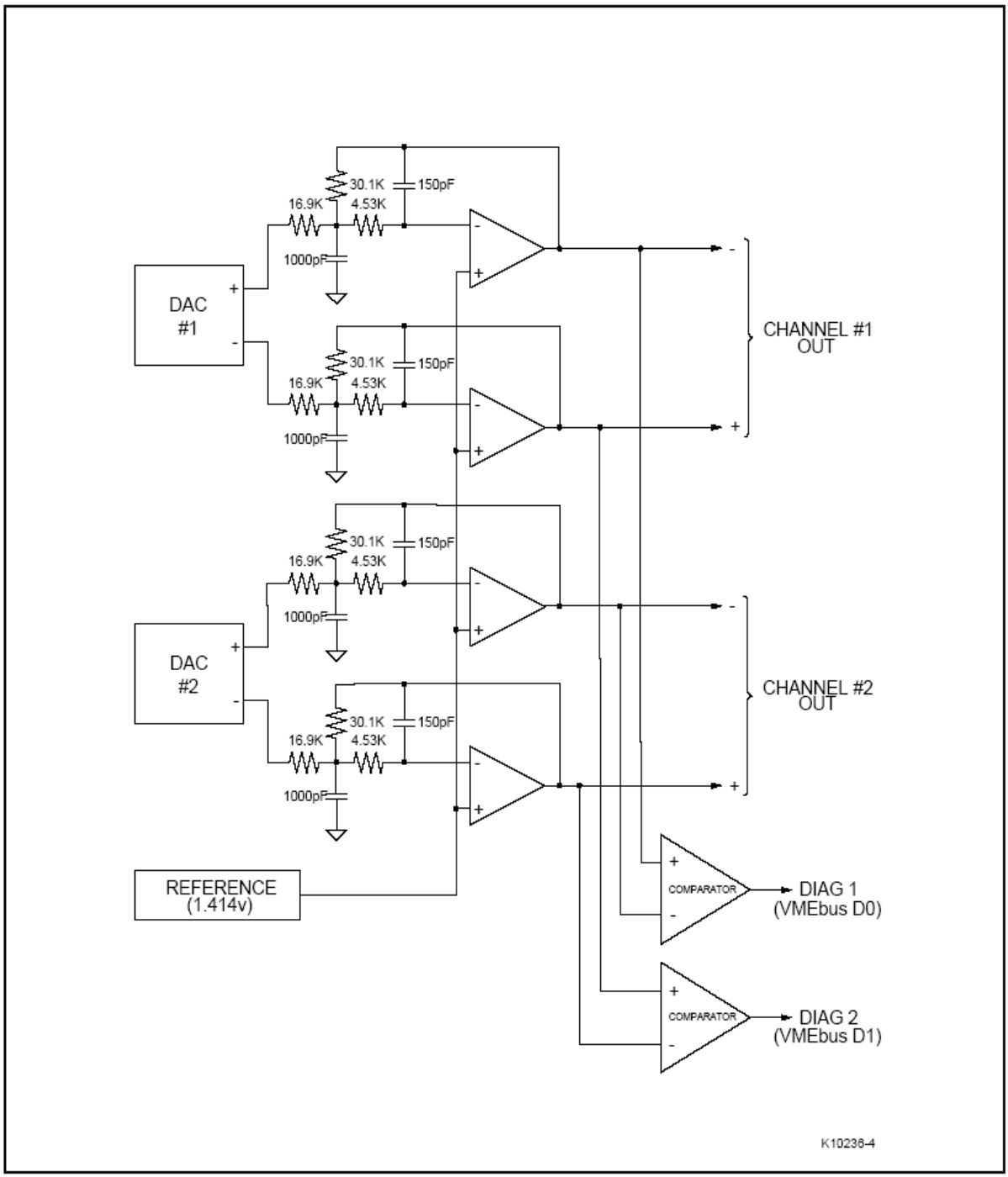


FIGURE 2. ICS-115 Output section (only 2-channels shown) illustrating on-board diagnostic capability

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Figure 3 shows a typical 1024-point FFT which demonstrates ICS-115 performance. For the purpose of this measurement, the ICS-115 was configured in Loop mode and loaded with a synthesized pure sine waveform. It was operated using the internal programmable clock, and its output was connected to an ICS-110A Sigma-Delta ADC board to allow the waveform to be digitized. The ICS-115 input data was scaled to drive the output to about 9dB below full scale, so as not to over drive the ICS-110A input.

ICS-115 APPLICATIONS

The ICS-115 board has been designed for direct application in digital audio, waveform generation, simulation/stimulation, and sonar transmit signal generation. The characteristics that make the ICS-115 an attractive choice in many of these applications are given below:

a) a large number of boards can be operated synchronously;

b) "continuous", "one-shot" and "loop" modes of operation greatly simplify generating any arbitrary, one-shot or periodic waveform;

c) three alternative high speed interfaces are provided for DAC data input, namely VME64, VSB and FPDP;

d) the FPDP interface provides easy data transfer from a Digital Signal Processor or from other ICS boards, thus reducing system integration time by virtually eliminating software development;

e) large swing-buffer memory size allows reduction of VME/VSB interrupt rate when loading DAC data.

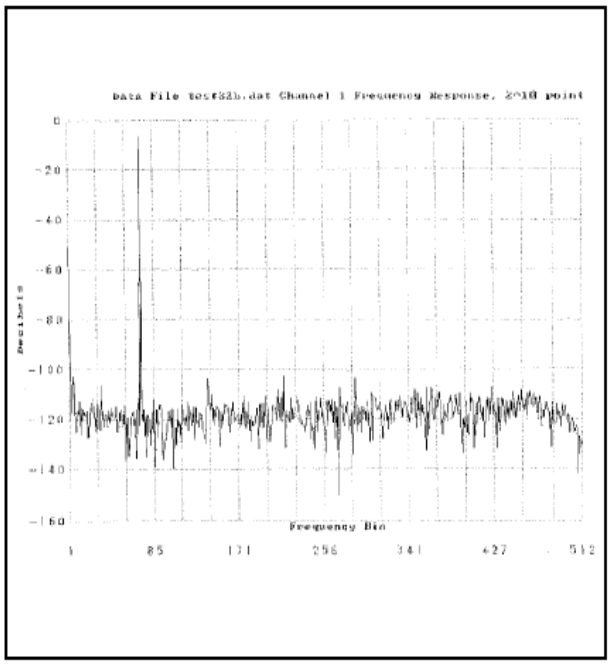


FIGURE 3. 1024-point FFT of synthesized sinewave sampled at 48kHz. An ICS-110A ADC board was used to synchronously digitize the ICS-115 board's output (which is 9 dB below full scale).

Figures 4 and 5 show system configurations for a 32-channel analog I/O workstation and a 224-channel sonar transmit system. The workstation example of Figure 4 can be used for digital audio, control, and test and monitoring applications. The system uses the ICS-110A sigma-delta ADC board for signal digitization and the ICS-2200S DSP board for FIR filtering, demodulation, equalization, etc. The data is transferred from one module to another via FPDP cabling as shown in the diagram. The sonar transmit system example of Figure 5 uses the ICS-7220 board for VME/VSB data buffering and the ICS-2200S board for inverse beamforming (i.e. generating 224 delayed replicas of input signal via interpolation). Here again, data is transferred via FPDP cabling. Note that in either example the number of output channels can be expanded simply by adding more ICS-115 boards.

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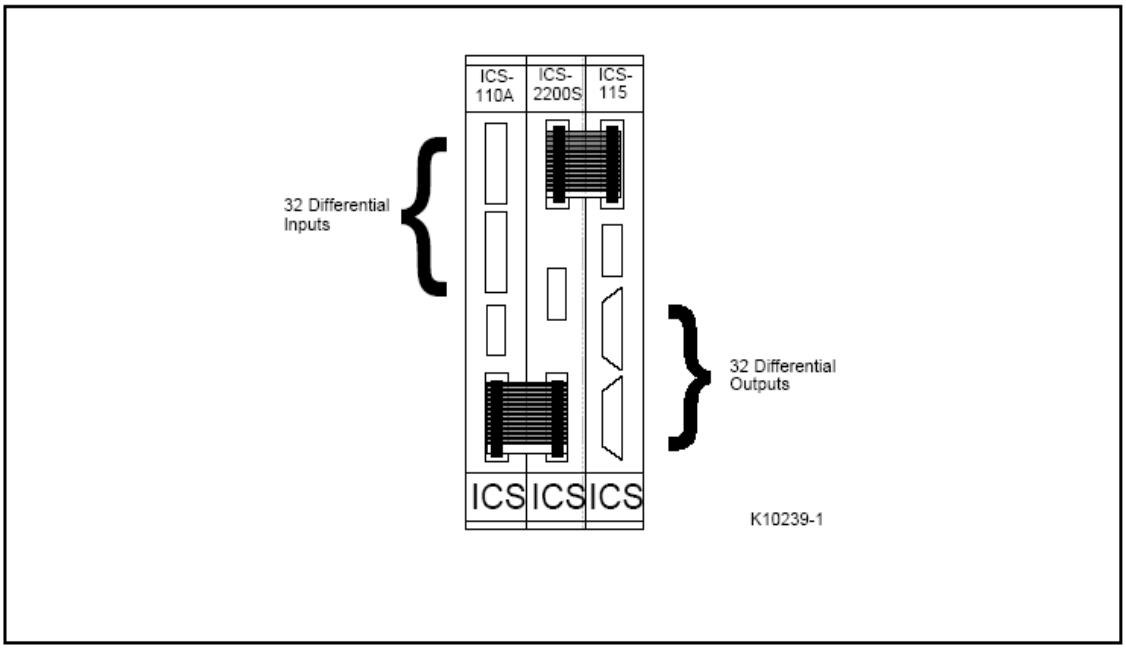


FIGURE 4. An Analog I/O Workstation

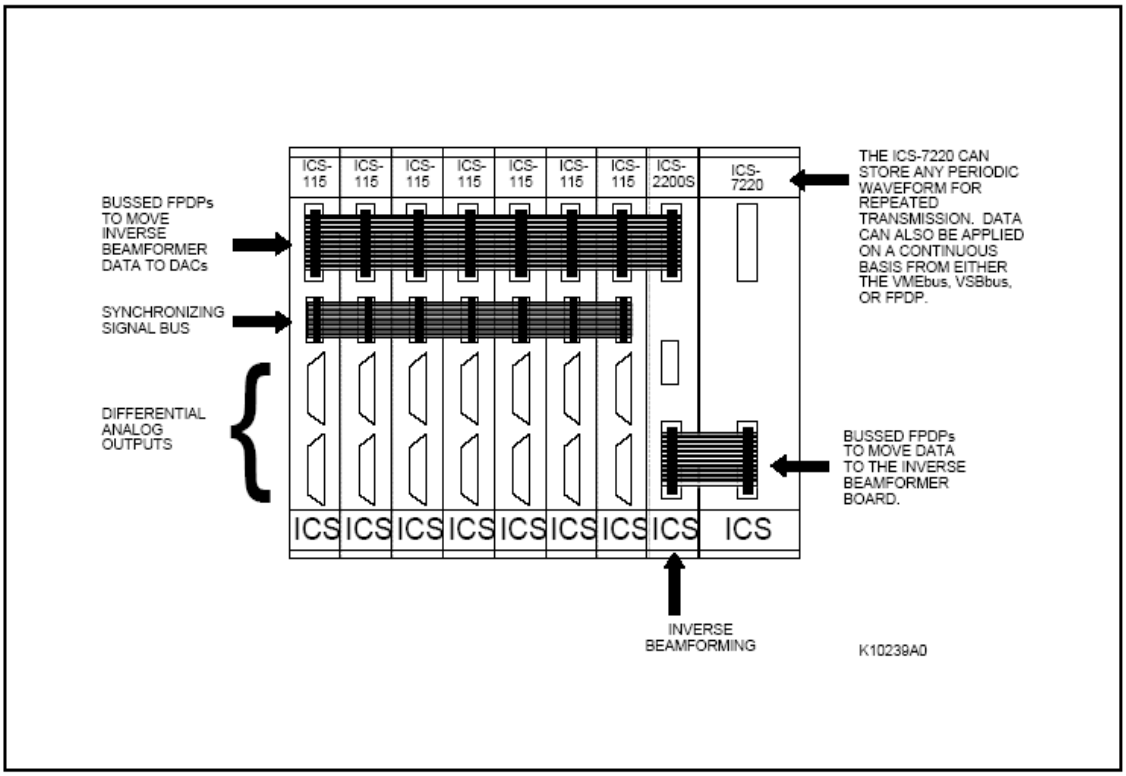


FIGURE 5. A Sonar Transmit System Configuration

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DETAILED DESCRIPTION

Delta-Sigma Analog Conversion

The ICS-115 uses Crystal Semiconductor's CS4329 Delta-Sigma converter. This device is designed to perform one bit conversions at 128 times the required sampling rate. It incorporates a 128x digital interpolation filter, followed by a fourth order Delta-Sigma modulator, a 1-bit DAC, and a single pole switched capacitor filter. As shown in Figure 2, the output of the CS4329 is filtered by a second order Butterworth filter using Linear Technologies LT1355 Op Amps to further reduce out of band noise. No further filtering should be required, as the 1 bit DAC's Nyquist frequency is at least six octaves away from the highest signal frequency. The output circuit also removes the 2.2V DC bias of the differential outputs of the CS4329. The final output of the ICS-115 is 5.0V peak-to-peak differential (i.e. ±2.5 V on each wire of the differential pair). The differential outputs offer excellent noise immunity and common mode rejection.

The ICS-115 offers >90 dB S/N ratio and <-90 dB inter-channel crosstalk. The passband edge of the combined analog and digital filtering is 0.45 x Fs, where Fs is the desired sampling frequency. Note that the actual clock supplied to the DACs must be 256 x Fs, as noted above.

Clock/Trigger Options

The ICS-115 offers both internal and external clocking options. For external clocking, the user must supply a differential clock signal to the External Clock connections of the P4 connector at 256 times the desired sampling rate. In a multiple ICS-115 board configuration, the external clock is used only by the master board, which generates the distribution clock (CLK) and sampling period clock (FAST_SYNC) and drives them on the P4 bus to all slave ICS-115 boards. This guarantees simultaneous sampling across all ICS-115 boards. The maximum clock frequency is 12.8 MHz corresponding to a sampling period of 50 kHz.

The internal clock of the ICS-115 is generated by a Fox F6053 Programmable Crystal Oscillator. This oscillator allows the user to select any desired sampling rate from 1 kHz to 50 kHz with approximately 4 Hz resolution by writing a 22-bit programming word to the Clock Frequency Register of the ICS-115. The sampling clock is made available to the user on the P4 connector.

The ICS-115 offers output decimation to achieve effective sampling rates of less than 1 kHz. The decimation factor (DF) can be from 1 to 256. With decimation the same sample data is applied to the DACs for DF number of sample periods. The input data need only be supplied at the decimated rate.

As with the clock, the ICS-115 can be triggered either internally or externally. The user supplies the trigger only to the master. The master synchronizes the trigger signal to the sampling rate and drives the distribution trigger (TRIGGER) to all slave ICS-115 boards. This again ensures that all boards are simultaneously triggered. The trigger can be programmed to be either level or edge sensitive. With level sensitive triggering, the ICS-115 converts while the trigger is high. For edge sensitive triggering, the ICS-115 initiates conversion following the rising edge of the trigger. The edge sensitive trigger must be at least one sample period in length.

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Operating Modes

The ICS-115 offers a number of operating modes. Note that the Swing Buffer length is programmable in all modes:

In the **Continuous** mode, the user must continuously supply data to the board at a rate sufficient to keep up with the conversion rate. Note that the swing buffer allows large blocks of data to be transferred at very high speed. Once one bank of the swing buffer memory has been filled to the programmed length, further transfers must wait until swing buffer bank swap occurs. This is indicated by an interrupt.

In the **One-shot** mode of operation, the user supplies data to the swing buffer once, and the ICS-115 converts the contents of the swing buffer once for each application of the trigger. This mode is further divided into reloadable and non-reloadable sub-modes. In the former, fresh data must be loaded prior to each conversion. In the latter, the memory need be loaded only once prior to repetitive conversions using the same data.

In the **Loop** mode of operation, the user supplies data to the swing buffer once, and the ICS-115 repeatedly converts the contents of the swing buffer following one application of the trigger. This mode of operation is ideal for generating periodic waveforms.

The ICS-115 offers a **Frame Count** feature. When this feature is selected, the ICS-115 converts a programmable number of frames (from 1 to 65536) of data for each application of the trigger.

Input Data Word (Channel) Selection

The ICS-115 board includes a sequencer circuit which can be programmed to select any 32 data words (channels) from the input data stream. Each frame of data in the data stream is stored in one bank of the dual port input buffer. The frame size may be from 2 to 2048 data elements. When a frame has been stored, the sequencer reads out any arbitrary 32 data elements to the DACs.

The sequencer circuit also includes a barrel shifter which can be programmed to select any 16 adjacent bits, on a channel by channel basis, for analog conversion.

Multiple Boards

In line with ICS product philosophy, the ICS-115 design provides simultaneous sampling not only on all channels on one board, but also on all channels across multiple boards. In order to achieve multiple board synchronization, one board is designated as the master, and all remaining boards are configured as slaves. The master provides clock and trigger signals to the slave boards in the group to ensure both simultaneous start-up and simultaneous sampling of all boards in the group. These signals are bused on the P4 connector on the front panel of the ICS-115.

VMEbus Interface

The ICS-115 implements a VMEbus Master/Slave A64/D64 A32/D64 A24/D32 interface using the Newbridge Microsystems SCV64 integrated circuit. BLT (Block Transfer) and MBLT (Multiplexed Block Transfer) cycles are supported, both when the ICS-115 is VMEbus slave and when it is master. On power-up, default A32 and A24 slave images are loaded by the SCV64 with base addresses determined from on-board switches. The VMEbus host can configure the SCV64 internal registers by accessing the SCV64 register block using either of these slave images. Note that the slave base address of the SCV64 can be reprogrammed by the host by loading appropriate values in the SCV64 VMEbus Base Address Register.

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The SCV64 can be configured to perform VMEbus Master Block Transfers by loading the SCV64 internal registers with the appropriate VMEbus starting address, the local (to the ICS-115) starting address, and the transfer count. After the DMAGO bit in the SCV64 Control Register is set, the SCV64 will acquire the VMEbus and perform the requested transfer, freeing the host for other tasks. Note that the VMEbus specification limits block transfers to a maximum of 256 bytes, however, the ICS-115 design does not prevent transfers of larger blocks. Transfers can be either D64 or D32. D64 transfer rates of at least 50 MB/s can be attained. A programmable VMEbus interrupt is available to indicate that a transfer has been completed. A Programmable interrupt is also available for the DAC Ready condition.

VSB Interface

The ICS-115 implements a VSB Slave A32/D32 BLT interface. On power-up, the VSB slave image is disabled. The VMEbus host loads the ICS-115 with the VSB Respond, Broadcast and Broadcall base addresses, and sets the appropriate slave enable bits in the ICS-115 VSB control register. The ICS-115 can generate a VSB interrupt for the DAC Ready condition. The ICS-115 supports only polled interrupts.

FPDP Interface

Connector P5 on the front panel of the ICS-115 is compatible with the ICS FPDP Interface. The **ICS** **F**ront **P**anel **D**ata **P**ort (**FPDP**) is an industry standard interconnection for board-to-board or system-to-system data transfer. This interface standard has gained acceptance in the industry for use in a broad range of signal processing applications. It is directly compatible to CSPI's SC130/P100, Mercury's RIN-T/ROUT-T, SKY's SKYburst 160, Ixthos' IXI2S32-F, and Ariel's Hydra FPDP interfaces.

The FPDP is a high performance 32-bit parallel interface configured with a ribbon cable to connect boards or systems together. The simple and well-defined physical and electrical interface provides the basis for integrating many different types of boards and sub-systems. The maximum clock rate of the ICS-115 FPDP interface is 20 MHz providing a sustained data rate of up to 80 MBytes/s.

The FPDPs of multiple ICS-115 boards can be bussed to supply DAC data to each boards (See Figure 5). Data may be transmitted onto the FPDP as a large frame (frame length up to 2048 channels). Each ICS-115 board can be programmed to select its own set of 32 channels for analog conversion. Up to 32 ICS-115 boards can be bussed on a single FPDP. More details on the ICS FPDP can be found in INPUT Note #15.

Diagnostics

The ICS-115 offers built-in digital and analog diagnostics. In the diagnostic mode of operation, DAC data can be written to the board via the VMEbus interface. The data that would normally be applied to the DACs can then be read from the DAC FIFO to verify data path integrity. Normal operation is suspended while in diagnostic mode. Analog diagnostics are available by using 32 comparators attached to the outputs of adjacent channels. The comparator outputs are stored in a register for VMEbus access. By setting one channel of the pair of channels to a DC level, and adjusting the other channel to determine its crossover point, faults can be isolated to one pair of channels.

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Channel Mute

The ICS-115 has a thirty-two bit register to control individual channel muting. Each bit corresponds to one channel, and writing a '1' to the bit corresponding to a particular channel mutes that channel. This causes the channel output to immediately swing to zero volts.

PROGRAMMING MODEL

The ICS-115 VMEbus memory map is shown in Figure 6. The individual bit fields of some of the registers are shown in Figure 7. All programming and control of the ICS-115 is accomplished through the VMEbus interface. All register bits that are not defined have no effect on the operation of the ICS-115, and may be read as zero or one.

The ICS-115 VSB interface provides a 32 MByte Respond address space for writing DAC data. In practice, the size of VSB data transfers may be limited by the Swing Buffer length. The ICS-115 also provides a 512 MByte Broadcast and a 512 MByte Broadcall address spaces to allow multiple boards to participate in VSB transfers.

SOFTWARE DEVICE DRIVERS

The ICS-115 board is supported by comprehensive software device drivers for the Solaris 1 and Solaris 2 operating systems and for the VxWorks Real-time Operating System.

The use of these drivers greatly simplifies control and operation of the ICS-115, and is strongly recommended. It will generally save programmers much time since they are relieved of the requirement to understand the complexities of the ICS-115 hardware model and of the Newbridge SCV64 VMEbus interface device.

All drivers include the following elements:

(i) A device driver conforming to the I/O model for the target operating system, including support for open, close, read, write and ioctl functions, as well as device initialization and attachment.

(ii) A comprehensive library containing 25 'C' functions, split in two parts:

(a) Library functions. These provide, in most cases, access to individual device registers, thus providing control of all aspects of the ICS-115.

(b) Utility functions. e.g., to provide control over the frequency of the on-board clock oscillator using engineering units (kHz). The function returns a value to be programmed to the board, and the actual frequency programmed in kHz.

The library functions allow the user to quickly program applications using meaningful function names rather than the low level "ioctl" functions. For users who wish to customize or expand the library routines, and for those who wish to port the driver to other operating systems, complete source code is available. Some descriptions of library functions follow.

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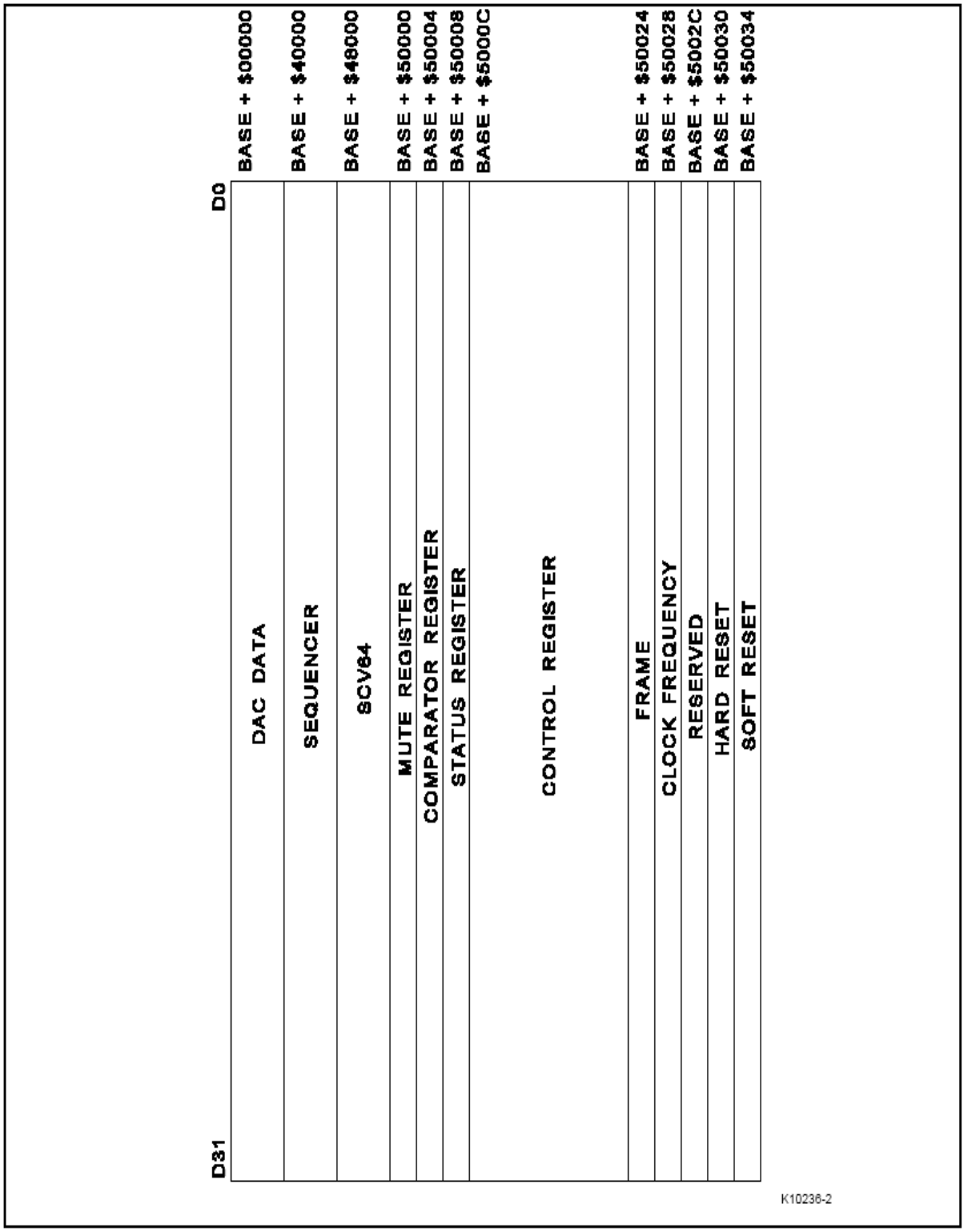


FIGURE 6. ICS-115 Memory Map

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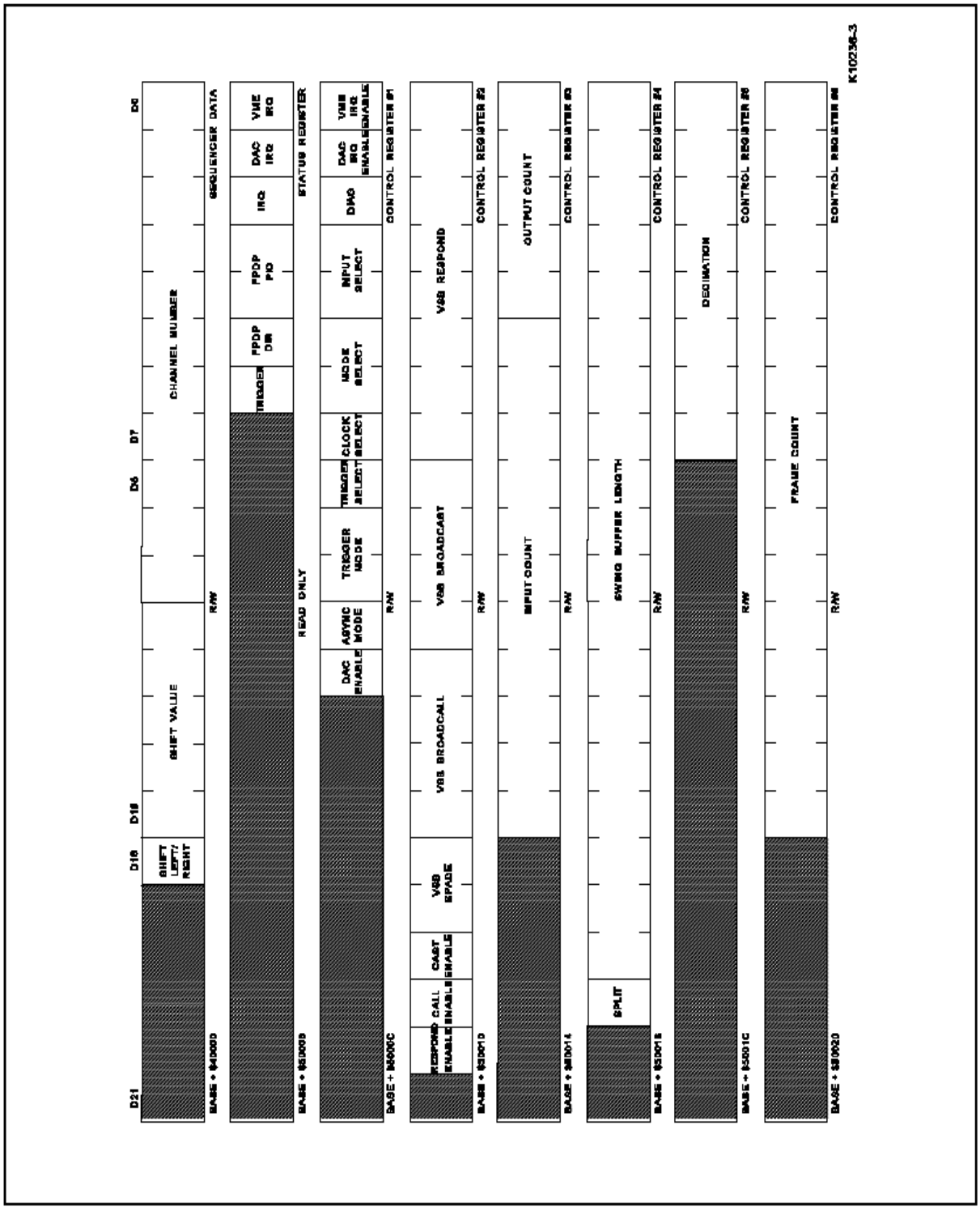


FIGURE 7. ICS-115 Register Definitions

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The following are examples of some of the library routines:

ics115ControlSet() -	Configures board (trigger mode, internal/external clock and trigger, output mode, input path, etc.)
ics115VSBSet() -	Configures VSBbus
ics115ConfigSet() -	Configures DAC (data frame size, no. of channels, swing buffer size, decimation factor, etc.)
ics115ClkSet() -	Sets sampling frequency.
ics115DiagGet() -	Gets the contents of the analog diagnostic register.
ics115Enable() -	Enables DAC conversion
ics115Disable() -	Disables DAC conversion
ics115Write() -	Writes data to the ICS-115 memory for output.
ics115Read() -	Reads data from the ICS-115 memory when in diagnostic mode.
ics115doVMEDMA() -	Initiates a DMA transfer on VMEbus. The ICS-115 is configured as bus master. Transfers may be single word or block (BLT/MBLT).

The following is an example of a fragment of 'C' code which uses the VxWorks driver and library. The ICS-115 is configured for loop mode operation with internal clock. A 32-channel digitized waveform is loaded into on-board memory prior to starting conversion.

```
/* This is a fragment of 'C' code showing how to use ICS-115 library functions for VxWorks */
/* The fragment gives an example of how to program the DAC for loop mode conversion */
/* with frame counting disabled. Internal trigger and clock (frequency = 48kHz) are selected. */
/* The data is loaded from VMEbus. The user may select which channel/s to use for output */


#include <stdio.h>
#include <vxWorks.h>
#include <vme.h>
#include <ioLib.h>
#include <string.h>
#include <errnoLib.h>
#include <math.h>
#include <drv/vme/vmechip2.h>
#include <stdlib.h>
#include <usrLib.h>
#include <taskLib.h>
```


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```
#include "115brd.h"

/* Local Definitions */

#define VMEADDRESS 0x100000
#define VMEMODIFIER 0x3d
#define IVECT 240
#define ILVL 3


/* Global Variables */

char g115Name[]="/ics115/0";
int g115;

int loopModeExample(void)
  {
  ICS115_DACCONFIG config;                /* Structure defining board configuration */
  int i,j;
  double angle;
  int chanSel;
  int value;
  int stopit;
  long *buf;

  if (ics115Drv()==ERROR)                 /* Initialize the driver */
       {
       printf("ICS115 Driver initialization failed\n");
       return(ERROR);
       {

  if(ics115DevCreate(g115Name, VMEMODIFIER, VMEADDRESS, ILVL, IVECT)==ERROR)   /* Add board as a device */
       {
       printf("Unable to attach ICS115\n");
       return(ERROR);
       }

  g115=open(g115Name, O_RDWR);            /* Open the ICS115 for read/write */

  config.enable=ICS115_DISABLE;           /* Make sure board is disabled at start */
  config.async=ICS115_DISABLE;
  config.trigmode=ICS115_LEVEL;
  config.trigsel=ICS115_INTERNAL;         /* Internal trigger */
  config.clksel=ICS115_INTERNAL;          /* Internal clock */
  config.mode=ICS115_LOOP;                /* Loop mode operation */
  config.inputsel=ICS115_VME;             /* Load data from VMEbus */
  config.diag=ICS115_DISABLE;             /* Diagnostic mode disabled */
  config.dacinten=ICS115_DISABLE;         /* Interrupts disabled */
  config.vmeinten=ICS115_DISABLE;         /* VMEbus interrupts disabled */
  config.frame=32;                        /* Frame size equals number of channels */
  config.numchan=32;                      /* Number of channels to use */
  config.split=ICS115_DISABLE;
  config.sblen=32*1024;                   /* 1024 data items to be loaded per channel */
  config.dec=1;                           /* Decimation factor */
  config.fcount=0;                        /* Frame count disabled */
  config.sFreq=48.0;                      /* Internal clock sampling frequency (kHz) */
  config.mute=0;                          /* No muting */
  for (i=0; i<32; i++)
       {
```


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```
        config.seq[i].index=i;
        config.seq[i].shift=0;              /* Select LS 16 bits of 32 for output */
        config.seq[i].dir=ICS115_LEFT;
        }
   ics115DACConfigSet(g115,&config);        /* Load configuration to ICS-115 */

   printf("\nEnter Channel (0=All) :");
   scanf("%d",&chanSel);
   buf=(long*) malloc(32*2048*4);
   for (i=0; i<2048; i++)
        {
        angle=i*2.0*3.1415927*34.0/2048.0;  /* calculate data for a sine signal in bin 34 */
        value=32768*sin(angle);             /* full scale signal */
        for (j=0; j<32; j++)
              if ( (j==(chanSel-1))||(chanSel==0) )
                    buf[i*32+j]=value;
              else
                    buf[i*32+j]=0;
        }
   ics115Write(g115, buf, 32*2048);         /* Write data to ICS-115 */
   ics115Enable(g115);                      /* Start conversion */

   printf("\nPress any key to stop conversion :");
   scanf("%d",&stopit);
   ics115Disable(g115);                     /* Stop conversion */

   close(g115);                             /* Close device */
   }
/* End of code */
```

ICS SENSOR PROCESSING

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