ICS-115A

OPERATING MANUAL

Interactive Circuits And Systems Ltd.
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Extra copies of this manual are available from the factory.

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1 INTRODUCTION

This manual describes the ICS-115A VMEbus analog output board, including the following versions:

ICS-115A-xx	100kHz/channel maximum sampling frequency (xx indicates the number of channels on the board)
ICS-115A-32B	ICS-115A with modified output voltage (10Vpp on each wire)

The ICS-115A is a VMEbus analog output board which is designed to simplify complex conversion requirements by offering:

- Large number of channels (4-32 per board);
- Differential outputs;
- Front-panel synchronization signals to allow simultaneous sampling over a large number of boards;
- Delta-Sigma DACs which virtually eliminate complex and expensive post filtering;
- Simultaneous sampling at rates from 64 Hz to 100 kHz;
- 16 bit resolution;
- 90 dB dynamic range and -90 dB interchannel crosstalk;
- External, programmable internal or FPDP frame clock;
- Internal clock resolution of approximately +/- 4 Hz;
- 1 MSample on board buffer;
- High speed VMEbus interface with VME64 Master Capability;
- High speed VSBbus slave interface;
- High speed 32 bit Front-Panel Data Port (FPDP) for direct interface to Mercury, CSPI, SKY, Ariel, and Ixthos array processors/DSP boards as well as other ICS products;
- Ability to bus the FPDP inputs across multiple ICS-115A boards to accept one composite data stream.

1.1 References

OpenBus Interface Components, SCV64 User Manual, Document No. 891078.MD301.01, Newbridge Microsystems, 1993.

2. VxWorks Device Driver Manual for the ICS-115/ICS-115A, Document No. E10452, Interactive Circuits and Systems Ltd.

3. VMEbus Specification, IEC 821, ANSI/IEEE Std.

4. VSBbus Specification, IEC 821, ANSI/IEEE Std. 1096-1988, VMEbus International Trade Association.

2 GENERAL DESCRIPTION

Figure 1 shows a simplified block diagram of the ICS-115A board. The board has up to 32 16-bit Delta-Sigma DACs which drive differential outputs on two high density D-subminiature connectors on the front panel (see Figure 2). A two pole Butterworth filter is applied to the final output of the DACs to further reduce out of band noise (see Figure 3). The serial DAC data is supplied by 32 16 bit parallel to serial converters. This converter data is supplied at the sampling rate by a FIFO, which decouples the conversion rate from the input data rate.

Because of the digital interpolation included in the Delta-Sigma DAC devices, which provides 8 x oversampling (conversion) of the signal, there is no need for the user to select a conversion rate which is greater than (B/0.45) Hz, where B represents the highest frequency in the signal. Unlike conventional D/A Converters, where a high order filter may be required, a two pole filter is sufficient with the ICS-115A. The product includes a two pole filter with a Butterworth characteristic and a cut-off frequency of 70.0 kHz.

The FIFO data is supplied by a 1 MSample Swing Buffer, which allows the ICS-115 to be operated in several different modes. In the **continuous** mode of operation, a continuous data stream is fed to the swing buffer. In the **one-shot** mode, the swing buffer is loaded once, and the data is converted once with each application of the trigger. In the **loop mode**, the swing buffer is loaded once, and the data is repeatedly converted after one application of the trigger.

The data input section of the ICS-115A consists of a dual port input buffer, a barrel shifter, and a dual port sequencer. The dual port input buffer is organized as a swing buffer, such that while one half of the buffer is being loaded with a frame of data, the other half is emptied into the Barrel Shifter. The sequencer and barrel shifter allow an arbitrary selection of any 32 channels from an input frame, which can be up to 2048 channels in length. The barrel shifter selects which 16 bits of the 32 bit input stream are to be applied to the DACs on a channel-by-channel basis. The data can be supplied from VMEbus, VSBbus, or the P3 Front-Panel Data Port (FPDP).

The ICS-115A supports internal, external and FPDP frame rate clocks. The internal clock can be programmed to within less than 400 ppm by simply writing the appropriate clock frequency program word to the board. The programmed frequency must be 256 times the desired sampling rate (256 x Fs). The ICS-115A also supports internal and external triggers. The trigger can be configured as edge or level sensitive. A trigger mode is available whereby the ICS-115A converts a preset number of frames of data upon application of the trigger.

To synchronize multiple boards, one board is configured as a sampling master and all other boards are configured as slaves. The sampling master generates and distributes synchronization signals via the P4 connector on the front panel, which is bussed between boards. These signals both ensure simultaneous sampling, and guarantees data path integrity, across all boards.

The ICS-115A has on-board diagnostic capability which can be used to test both the digital and the analog functioning of the board. In addition, pairs of channels can be independently muted (set to zero volt output).

2.1 Board Specifications

Analog Specifications:

No. of Analog Output Channels:	4, 8, 16, or 32 Differential
Sample Size:	16 bits
Analog Connector Type:	Two 44-pin D-shell
Output Impedance:	< 1 Ohm
Output Drive	24 mA
Full Scale Output (ICS-115A-xx):	5.0 Vpp differential*
Full Scale Output (ICS-115A-32B):	10.0 Vpp differential
Reconstruction filter characteristic:	Butterworth, two pole
Reconstruction filter cut-off frequency:	70 kHz
Output Signal Bandwidth:	49.0 kHz max.
Maximum Channel Input Data Rate (Fs):	100 kHz
Digital interpolation factor:	8
Group Delay:	30/Fs sec
Maximum Input Data Rate:	20MSample/sec
Maximum no. of channels input:	2048
Programmable Decimation Factor:	1 to 256
Minimum clock frequency:	4 MHz
Maximum clock frequency:	25.6 MHz
Dynamic Range (S/N+D):	> 90 dB
Inter-channel Crosstalk:	< -90 dB
Harmonic Distortion:	< -90 dB

Digital Specifications

On Board Storage	1 MSample
VMEbus Interface:	A64/A32/A24 D64/D32 MBLT Master/Slave Full interrupt support 64 MBytes/s
VSB Interface:	A32/D32 BLT Slave Polled Interrupts 32 MBytes/s
Front-Panel Interface:	32-bit, 20 MHz (80MBytes/s). Compatible with Mercury, CSPI, SKY, Ariel, and Ixthos front-panel interfaces.
Environmental:	Operating Temp. 0 - 50°C Hum. 95% max RH, non-condensing Non-op Temp.-45 - +85°C Hum. 95% max RH, non-condensing
Power consumption (high Z loads):	+5V @ 4 Amps +12V @ 0.2 Amps -12V @ 0.2 Amps
Board size:	VMEbus 6U standard (233 X 160 mm)

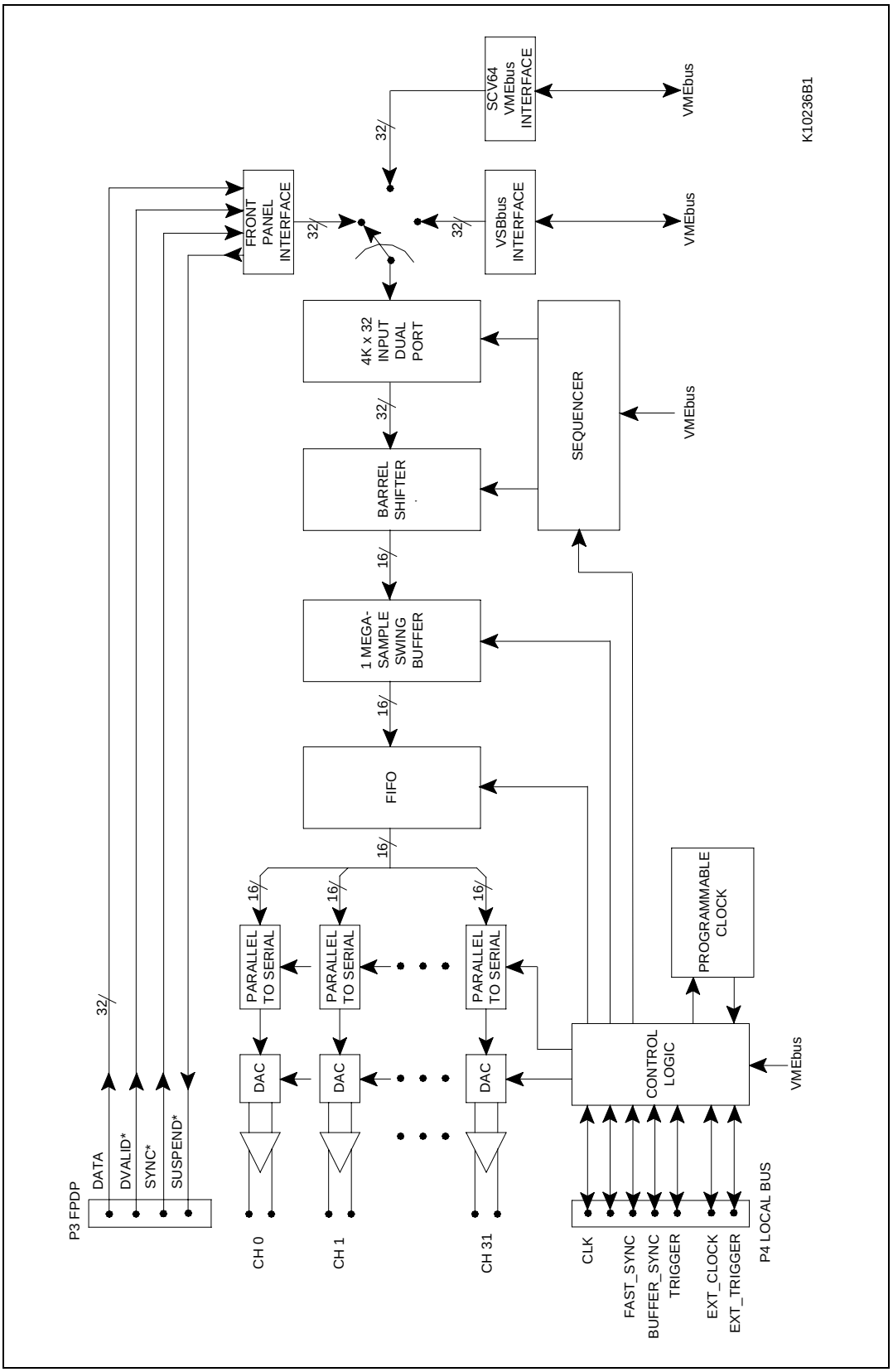


Figure 1 - ICS-115A Block Diagram

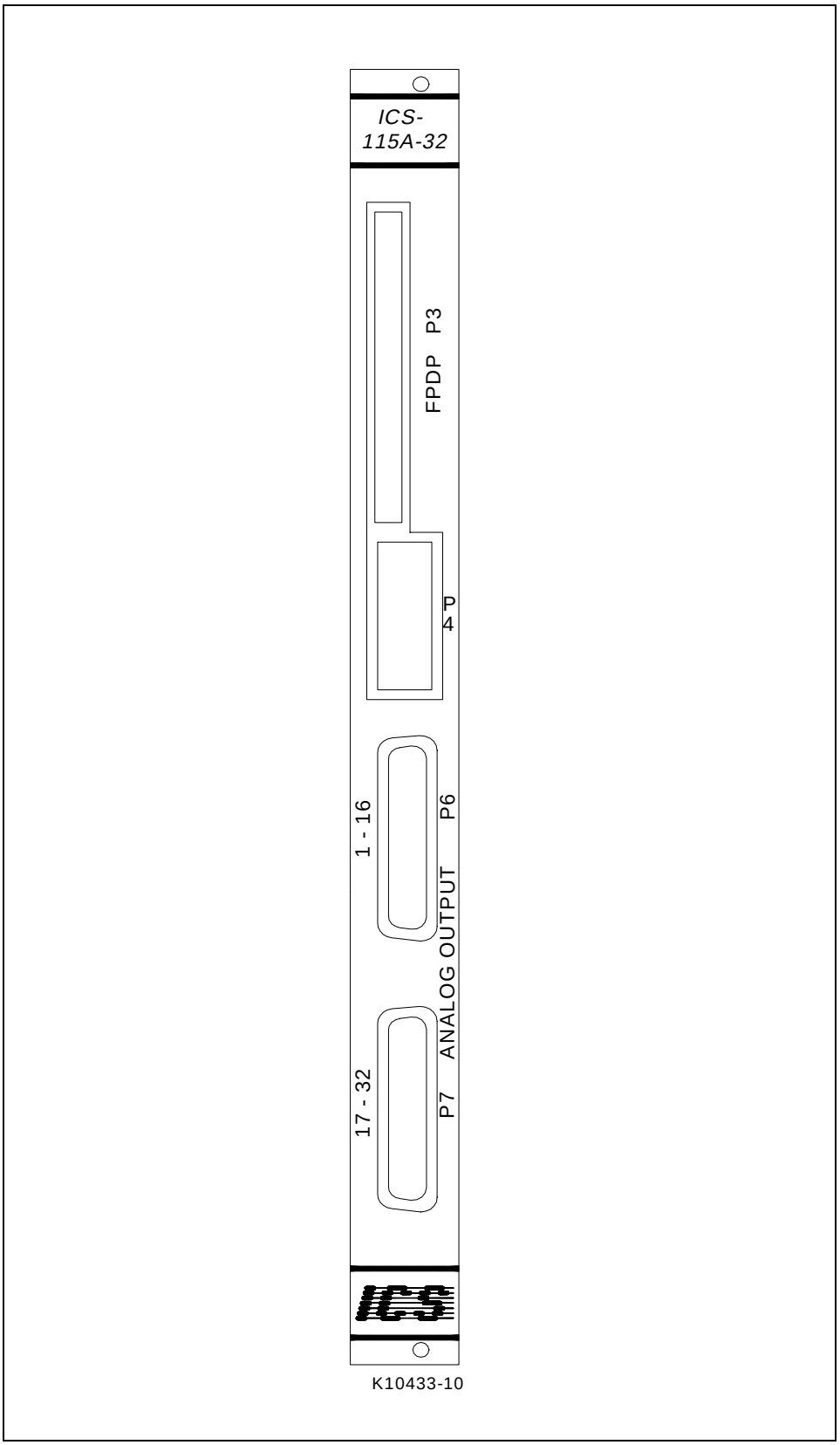


Figure 2 - ICS-115A Front Panel View

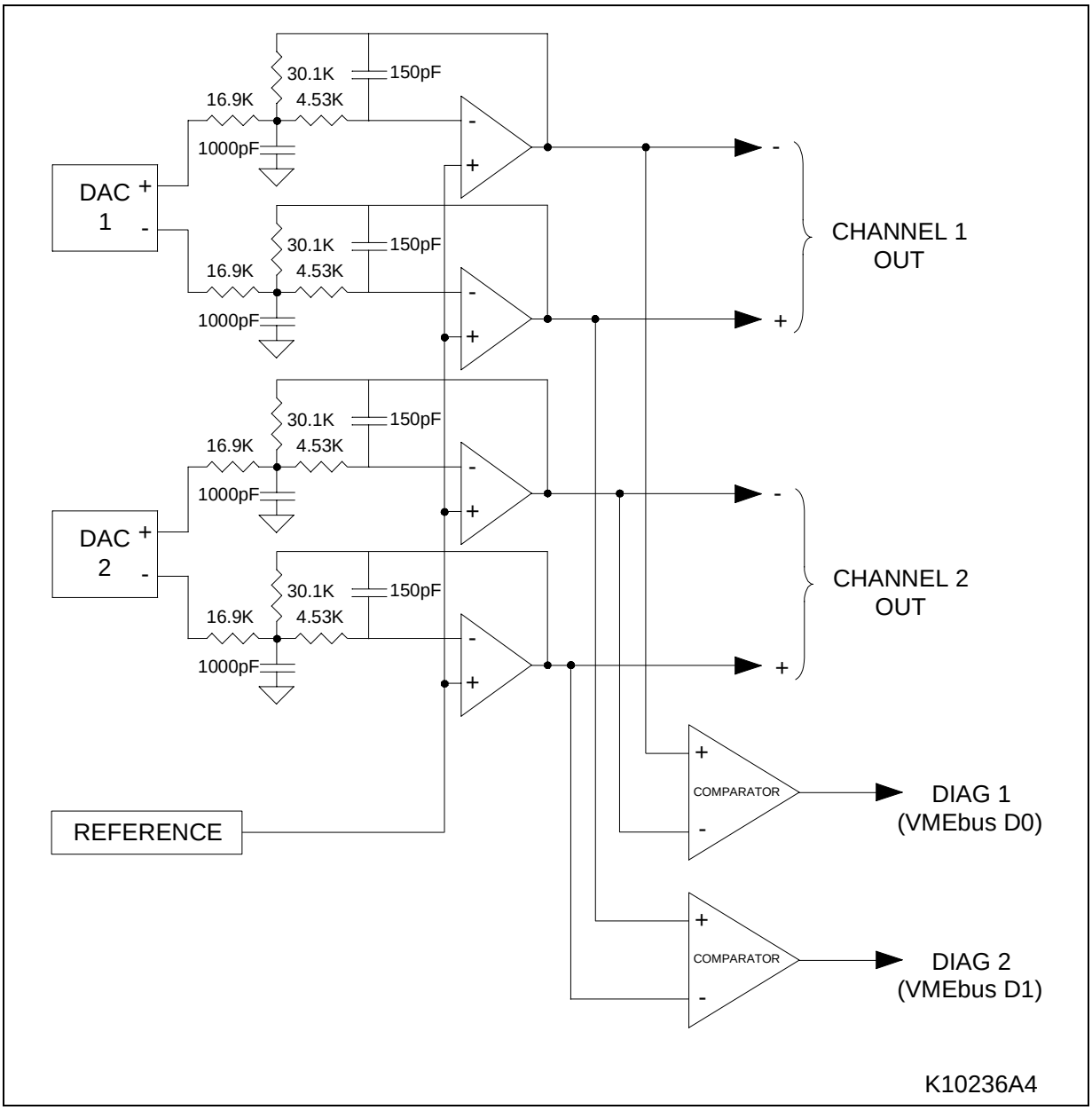


Figure 3 - Output Circuit of the ICS-115A

3 DETAILED DESCRIPTION

3.1 Delta-Sigma Analog Conversion

The operation of a Sigma-Delta DAC differs significantly from traditional DACs. The primary purpose of using a Delta-Sigma architecture is the inherent linearity of a 1-bit DAC. The ICS-115A uses the Burr-Brown PCM1716 Delta-Sigma converter. This device is designed to perform a one bit conversion at 64 times the sampling rate. It incorporates an 8x digital interpolation filter, followed by a fourth order Delta-Sigma modulator, a 1 bit DAC, and a single-pole switched capacitor filter. The final output circuit of the ICS-115A is shown in Figure 3. The output of the PCM1716 is further filtered on the ICS-115A by a second order Butterworth filter with a cut-off frequency of 70 kHz, implemented using Linear technologies LT1355 operational amplifiers, to further reduce out of band noise. No further filtering should be required, as the one bit DAC's Nyquist frequency is at least six octaves away from the highest signal frequency. The output circuit also removes the 2.2V DC bias of the differential outputs of the PCM1716. The final output of the ICS-115A is 5.0Vpp differential (5.0 Vpp on each wire). The differential outputs offer excellent noise immunity as well as common mode rejection.

The ICS-115A provides >90 dB S/N ratio and <-90 dB inter-channel crosstalk. The passband edge of the combined analog and digital filtering is 0.49 x Fs.

NOTE: Since the Delta-Sigma DACs of the ICS-115A operate at 256 Fs, to avoid confusion, the term "DAC clock" or "sampling clock" is used to refer to the actual clock supplied to the DACs (256 x Fs). "Sampling period" or "rate" refers to the update rate of the DACs (Fs).

3.2 Clock/Trigger Options

The ICS-115A offers internal, external and FPDP frame rate clocking options. For external clocking, the user must supply the clock signal to the sampling Master only, on the External Clock wires of the P4 connector. The supplied clock may either be at the conversion rate or at 256 times the desired sampling rate. In the former case, Phase-locked Loop (PLL) circuits on the board are used to derive the 256 X clock required by the DACs. It is recommended that the user provide a 256 X external clock if possible, in order to minimize sampling jitter. The Master generates the distribution clock (XTI) and sampling period (FSYNC) and drives them on the P4 bus to all slaves. This guarantees simultaneous sampling across all boards. The maximum clock frequency is 25.6 MHz corresponding to a sampling frequency of 100 kHz.

The internal clock of the ICS-115A is generated by a Programmable Crystal Oscillator. This oscillator, which is programmed at the oversampling (256 X) frequency, allows the user to select the desired sampling rate with approximately 4 Hz resolution by writing a 22 bit programming word to the Clock Frequency Register of the ICS-115A. Note that, although the frequency range of the converters is from 16 kHz to 100 kHz, the frequency range of the programmable clock, at sampling frequency, is 1.41 kHz to 100 kHz. The internal sampling clock is made available to the user on the P4 connector.

The sampling clock may also be obtained from the P3 FPDP input data stream, if used. In this case, the SYNC* signal, which consists of a pulse at the frame rate frequency is multiplied by 256 with the use of the PLL.

The ICS-115A offers output decimation to achieve effective sampling rates of less than 16 kHz. The decimation factor (DF) can be from 1 to 256. With decimation the same sample data is applied to the DACs for DF sample periods, thus reducing the input sample data rate.

As with the clock, the ICS-115A can be triggered either internally or externally. The user supplies the trigger to the sampling master only. The master synchronizes the trigger signal to the sampling rate and

drives the distribution trigger (TRIG) to all slaves. This again insures that all boards are simultaneously triggered. The trigger can be programmed to be either level or edge sensitive. With level sensitive triggering, the ICS-115A converts while the trigger is high. For edge sensitive triggering, the ICS-115A initiates conversion on the application of the trigger. The edge sensitive trigger must be at least one sample period in length.

3.3 Operating Modes

The ICS-115A offers a number of operating modes. In the **continuous** mode, the user must continuously supply data to the board at a rate which matches the conversion rate, on average. (Note that the swing buffer allows large blocks of data to be transferred at very high speed, but the overall data rate must match the sampling rate.) If data is not supplied to the swing buffer at this rate, the ICS-115A will repeat the last valid buffer data until new data is supplied or the DAC is disabled. In the **one-shot** mode of operation, the user supplies data to the swing buffer once, and the ICS-115A converts the contents of the swing buffer once for each application of the trigger. The one-shot mode has two sub-modes, reload and no reload. When one-shot with reload is selected, fresh data must be supplied to the board before each application of the trigger. With one-shot and no reload, the same data is converted at each application of the trigger. In the **loop** mode of operation, the user supplies data to the swing buffer once, and the ICS-115A repeatedly converts the contents of the swing buffer following a single application of the trigger. This mode of operation is ideal for generating periodic waveforms. Another mode of operation, the **terminate on frame count** mode, which is similar to the one-shot mode, allows the user to convert a fixed number of frames (samples per channel) of data. In this mode, the ICS-115A converts a programmable number of frames (from 1 to 65536) of data for each application of the trigger.

3.4 Conversion Modes

The ICS-115A provides two modes of conversion, synchronous and asynchronous modes. The selection of the conversion mode determines the behavior of the board only when data has been provided at a rate insufficient to keep up with the selected conversion rate. During normal operation, therefore the selection of this option has no effect. In the event that a DAC finds that no data is available for the next conversion, if synchronous mode is selected, the converter will resynchronize when new data becomes available, resulting in a phase shift of the output compared to previous outputs. If asynchronous mode is selected, the converter will continue to use the last received data until fresh data becomes available.

3.5 Sequencer

The ICS-115A sequencer allows the user to accommodate almost any data input format. Each frame of data in the data stream is stored in one half of the dual port input buffer. This data stream can contain from 1 to 2048 data elements (channels). When a frame has been stored, the sequencer can be programmed to read out any arbitrary 32 data elements (channels) to the DACs. The sequencer also determines which 16 of the 32 input bits are to be used on a channel-by-channel basis.

3.6 Channel Mute

The ICS-115A has a thirty-two bit register which provides control of the muting of pairs of channels. Each even bit (0,2...30) corresponds to one pair of channels, and writing a '0' to the bit corresponding to a particular pair of channels mutes that pair of channels, i.e. it immediately sets their outputs to zero volts. The odd-numbered bits of the register are not used.

3.7 Diagnostics

The ICS-115A offers built-in digital and analog diagnostics. Digital diagnostics are provided by the **diagnostic** mode of operation. In this mode, DAC data can be written via the VMEbus interface to the board. The data that would be applied to the DACs in normal operation can then be read from the DAC FIFO to verify data path integrity. Analog diagnostics are available from 32 comparators attached to the outputs of adjacent channels during normal operation (see Figure 3). By setting one channel of the pair of channels to a DC level, and adjusting the other channel to determine its crossover point, faults can be located to one pair of channels.

3.8 Light-Emitting Diodes

The ICS-115A is fitted with a set of light-emitting diodes (LEDs) which indicate board operation and error conditions. The diodes are located on the solder side of the board; this is the left-hand side when the board is installed in vertical orientation. The diodes are located starting approximately one half of an inch from the top of the board.

There are four LEDs installed in a line. Table 3.1 describes the ICS-115A LEDs.

TABLE 3.1 Light Emitting Diodes

	LED Function	Colour	Description
1.	VME Access	Green	Illuminated at each valid VMEbus access to ICS-115A
2.	VSB Access	Green	Illuminated at each valid VSBbus access to ICS-115A
3.	FPDP Access	Green	Illuminated at each FPDP access to ICS-115A
4.	Error	Red	Illuminated when an error condition occurs. For example, this might be when data is not available when required by the DACs.

Note: LED1 is nearest the bottom of the board.

The intensity of illumination of each LED will depend on the frequency of occurrence of the event in question. For example, a single VMEbus access will illuminate the LED for one bus cycle only; this will therefore not be visible to the user. However, multiple accesses over a period of time will be visible. This does not apply to the ERROR indicator, which stays illuminated until either a Hard reset or a Soft reset occurs.

3.9 Cascading Multiple Boards

In line with ICS product philosophy, the ICS-115A design provides simultaneous sampling not only on all channels on one board, but also on all channels across multiple boards. In order to achieve multiple board synchronization, one board is designated as the sampling Master, and all remaining boards are configured as Slaves. The sampling Master provides clock and trigger signals to the Slave boards in the group. These signals are bussed on the P4 connector on the front panel of the ICS-115A, and allow the Master to control the sampling signals and data paths of the Slaves. All boards to be synchronized must be located in the same VMEbus chassis in order not to violate signal timing requirements. Multiple boards may also be bussed on a single FPDP.

3.10 VMEbus Interface

The ICS-115A implements a VMEbus Master/Slave A64/D64 A32/D64 A24/D32 interface using the Newbridge Microsystems SCV64 integrated circuit. Master BLT (Block Transfer) and MBLT (Multiplexed Block Transfer) cycles are supported. On power-up, default A32 and A24 slave images are loaded by the SCV64 with base addresses determined from on-board switches (see section 4 for details of switch settings). The VMEbus host can configure the SCV64 internal registers by accessing the SCV64 register block using either of these slave images. Note that the slave base address of the SCV64 can be reprogrammed by the host by loading appropriate values in the SCV64 VMEbus Base Address Register.

The SCV64 can be configured to perform VMEbus Master Block Transfers by loading the SCV64 internal registers with the appropriate VMEbus start address, the local (to the ICS-115A) start address, and the transfer count. After the DMAGO bit in the SCV64 Control Register is set, the SCV64 will acquire the VMEbus and perform the requested transfer, freeing the host for other tasks. Note that the VMEbus specification limits block transfers to a maximum of 256 Bytes, however, the ICS-115A design does not prevent transfers of larger blocks. Transfers can be either D64 or D32. D64 transfer rates as high as 64 MB/s can be attained. A programmable VMEbus interrupt is available to indicate that a transfer has been completed. A programmable interrupt is also available for the DAC Ready condition.

3.11 VSB Interface

The ICS-115A implements a VSB Slave A32/D32 BLT interface. On power-up, the VSB slave image is disabled. The VMEbus host loads the ICS-115A with the VSB Respond, Broadcast and Broadcall base addresses, and sets the appropriate slave enable bits in the ICS-115A VSB control register. VSB transfer rates as high as 40 MB/s can be attained. The ICS-115A can generate a VSB interrupt for the DAC Ready condition. The ICS-115A supports only polled interrupts.

3.12 FPDP Interface

Connector P3 on the front panel of the ICS-115A is compatible with the ANSI/VITA 17 FPDP Interface. The **F**ront **P**anel **D**ata **P**ort (**FPDP**) is an industry standard interconnection for board to board or system to system data transfer. This interface standard has gained acceptance in the industry for use in a broad range of signal processing applications. It is compatible with CSPI's SC130/P100, Ixthos' IXI2S32-F, Mercury's RIN-T and SKY's SKYburst 160 interfaces, among others. Details of the operation of the interface and the connector pinouts are given in Appendix 6.5.

The FPDP is a high performance synchronous 32-bit parallel interface configured with a ribbon cable to connect boards or systems together. The simple and well-defined physical and electrical interface provides the basis for integrating many different types of boards and sub-systems. The maximum clock rate of the ICS-115A FPDP interface is 20 MHz, providing a sustained data rate of up to 80 MBytes/s, when using the TTL level Strobe signal as the clock. When using the Positive-logic ECL (PECL) Strobe signals, PSTROBE+/-, clock rates up to 40 MHz are supported, for a sustained data rate of up to 160 MB/s. The ICS-115A supports both TTL and PECL-level strobe signals.

Multiple ICS-115A boards may be bussed on a single FPDP cable; this enables each board to select a range of channels for output from the FPDP data stream. Also, since multiple FPDP buses are allowed within a single VMEbus chassis, the total data path bus bandwidth may be scaled to system requirements.

3.13 P4 Local Bus Interface

The ICS-115A P4 Local Bus interface provides has two functions: it allows the user to connect an external clock and/or trigger signal, and it enables multiple boards to be synchronized. The external clock and trigger signals are TTL signals terminated by 220/330 ohm pull-up/pull-down terminations. The P4 connector is a generic shrouded 20-pin dual row header on 0.100 inch centers.

Details of the P4 pinouts are given in Appendix 6.4.

4 HARDWARE CONFIGURATION

Prior to board installation, a number of hardware configuration switches and jumpers on the ICS-115A need to be set. Figure 4 shows the jumper and switch locations with the default factory settings.

In the following description, a reference to "SWx-y" means position y of switch block x.

4.1 Switch Functions

The following table gives a summary of the functions of on-board switches.

SWITCH	FUNCTION (When switch in "ON" or "CLOSED" position)
SW1-1	Drive P4p3 TRIG+
SW1-2	Drive P4p4 TRIG-
SW1-3	Drive P4p1 XTI+
SW1-4	Drive P4p2 XTI-
SW1-5	Terminate P4p3 TRIG+
SW1-6	Terminate P4p4 TRIG-
SW1-7	Terminate P4p1 XTI+
SW1-8	Terminate P4p2 XTI-
SW2-1	Terminate P4p10 EXTCLK
SW2-2	Terminate P4P11 EXTTRIG
SW2-3	Drive P4p13 FSYNC
SW2-4	Terminate P4p13 FSYNC
SW2-5	Drive P4p15 VSYNC
SW2-6	Terminate P4p15 VSYNC
SW2-7	Drive P4p17 DSYNC
SW2-8	Terminate P4p17 DSYNC

SW3-1	Terminate P3p2 STROBE
SW3-2	Terminate P3p9 DIR*
SW3-3	Receive P3p27 PSTROBE-
SW3-4	Receive P3p25 PSTROBE+
SW3-5	Terminate P3p27/25 PSTROBE+/-
SW3-6	Use P3p27/25 PSTROBE (PECL Strobe)
SW3-7	Use P3p2 STROBE (TTL Strobe)
SW3-8	Reserved
SW4 -1 to -5	VMEbus A32 Base Address
SW4 -6 to -8	Jumper Parking
SW5 -1 to -5	VMEbus A24 Base Address
SW5 -6 to -8	Jumper Parking

4.2 VMEbus Base Address Selection

The VMEbus A24 and A32 base addresses are set with jumpers on SW4 and SW5. The settings are loaded to the SCV64 register VMEBAR at power-up. This register may be subsequently reprogrammed by the user (see section 5.2). The ICS-115A address map occupies a 512KB (Hexadecimal 0x80000) space. The VMEbus A64 base address is programmed after power up; details of the procedure for doing this are given in section 5.2. The A24 base address is set as follows:

0= JUMPER IN; 1= NO JUMPER;

A24 BASE ADDRESS	SW5- 12345
0x00.0000	00000
0x08.0000	00001
0x10.0000	00010
0x18.0000	00011
0x20.0000	00100
0x28.0000	00101
0x30.0000	00110
0x38.0000	00111
0x40.0000	01000
0x48.0000	01001
0x50.0000	01010
0x58.0000	01011
0x60.0000	01100
0x68.0000	01101
0x70.0000	01110
0x78.0000	01111
0x80.0000	10000
0x88.0000	10001
0x90.0000	10010
0x98.0000	10011
0xA0.0000	10100
0xA8.0000	10101
0xB0.0000	10110
0xB8.0000	10111
0xC0.0000	11000
0xC8.0000	11001
0xD0.0000	11010
0xD8.0000	11011
0xE0.0000	11100
0xE8.0000	11101
0xF0.0000	11110
0xF8.0000	11111

The A24 default base address is 0x100000 (see Fig. 4).

The A32 base address is set as follows:

0=JUMPER IN; 1= NO JUMPER;

A32 BASE ADDRESS	SW4- 12345
0x0000.0000	00000
0x0800.0000	00001
0x1000.0000	00010
0x1800.0000	00011
0x2000.0000	00100
0x2800.0000	00101
0x3000.0000	00110
0x3800.0000	00111
0x4000.0000	01000
0x4800.0000	01001
0x5000.0000	01010
0x5800.0000	01011
0x6000.0000	01100
0x6800.0000	01101
0x7000.0000	01110
0x7800.0000	01111
0x8000.0000	10000
0x8800.0000	10001
0x9000.0000	10010
0x9800.0000	10011
0xA000.0000	10100
0xA800.0000	10101
0xB000.0000	10110
0xB800.0000	10111
0xC000.0000	11000
0xC800.0000	11001
0xD000.0000	11010
0xD800.0000	11011
0xE000.0000	11100
0xE800.0000	11101
0xF000.0000	11110
0xF800.0000	11111

The A32 default base address is 0x10000000 (see Fig. 4).

4.3 FPDP P3 Clock Select

Switch SW3 selects between the single ended TTL STROB and the PECL differential PSTROBE signals used to acquire FPDP data on the P3 Port (see section 6.5.4 for details). The switch settings are shown in Figures 3 and 5.

CLOCK	SW3 3 4	SW3 6 7
STROBE	OFF OFF	OFF ON
PSTROBE,/PSTROBE	ON ON	ON OFF

4.4 Multiple Board Setup

In order to achieve sampling synchronization, multiple boards are connected using the ICS-115A Local Bus which is wired across the front panel P4 connector. If the FPDP is being used as the source of the DAC data, the FPDP cable may also be bussed across the P3 connectors of multiple boards. In these multiple board configurations, it is important to observe a few rules concerning the switch settings on the boards and the physical ordering of the boards on the two busses.

With regard to the P4 Local Bus signals, there are four types of board configuration which may be used in multiple ICS-115A systems: Stand-Alone Master, Master, Slave, and End Slave. The Stand-Alone Master is the configuration to be used when there is only one ICS-115A. When there are two boards, one must be a Master and the other must be an End Slave. When there are more than two boards, one or more Slave boards must be positioned between the Master and the End Slave. Figures 7 through 10 show the proper switch settings for each configuration. The Master is configured to drive the P4 signals to the Slaves. The End Slave terminates all P4 signals driven by the Master.

When the FPDP is used, the P4 Master is also the FPDP/RM (FPDP Receive Master). All other ICS-115A boards in the group, if any, are FPDP/R boards. In multi-board configurations, the Master must always be at one extreme end of the FPDP bus, i.e. the end opposite to the FPDP/TM (FPDP Transmitter Master) board.

4.5 External Clock Termination

Switch SW2-1 determines the termination of the external clock signal on the P4 connector. When ON, the ICS-115A uses parallel Thevenin (220/330 ohm) termination. When OFF, no termination is used. This allows the external clock signal to be driven by a source series-terminated driver.

4.6 External Trigger Termination

Switch SW2-2 determines the termination of the external trigger signal on the P4 connector. When ON, the ICS-115A uses parallel Thevenin (220/330 ohm) termination. When OFF, no termination is used. This allows the external trigger signal to be driven by a source series-terminated driver.

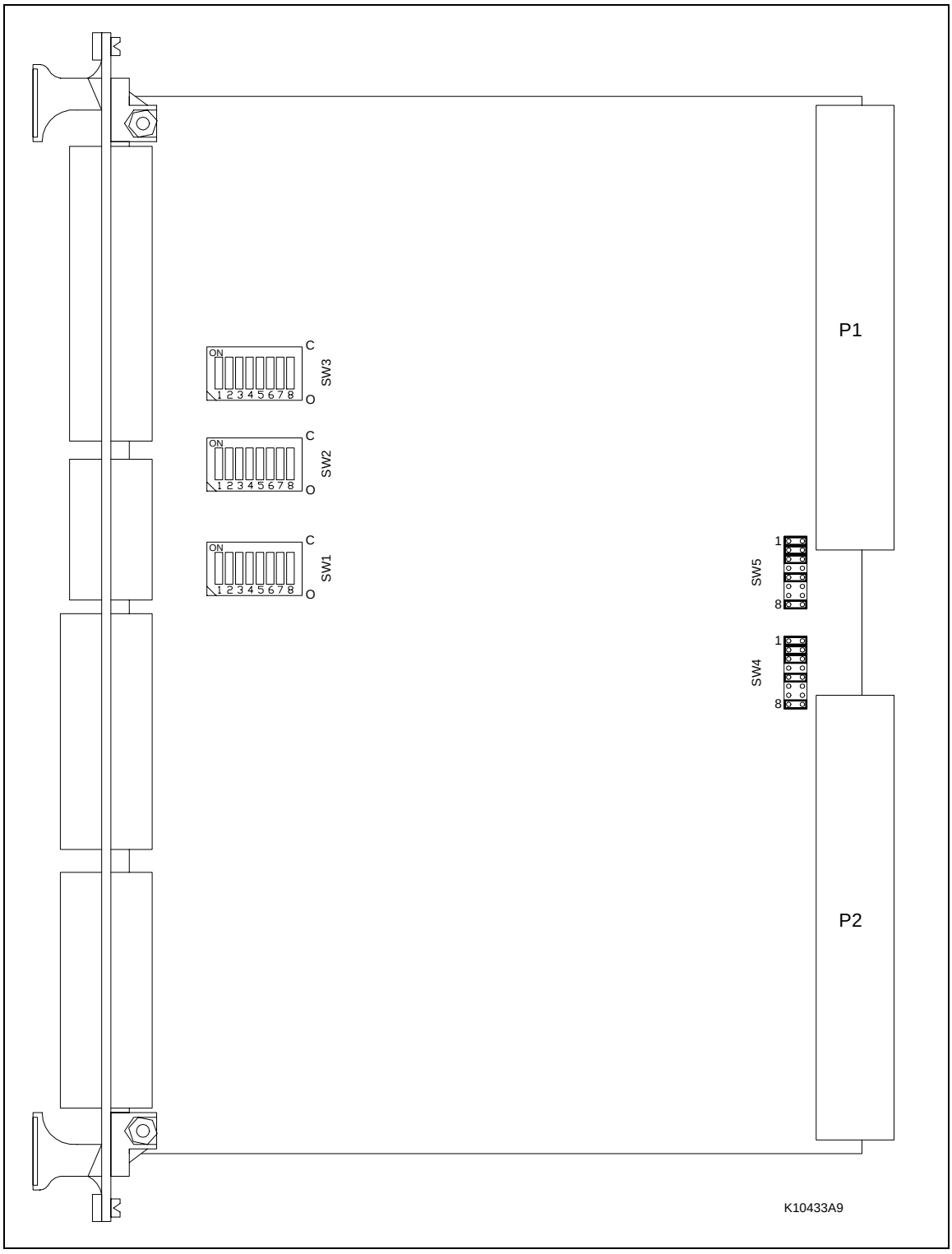


Figure 4 - ICS-115A Jumper and Switch Locations

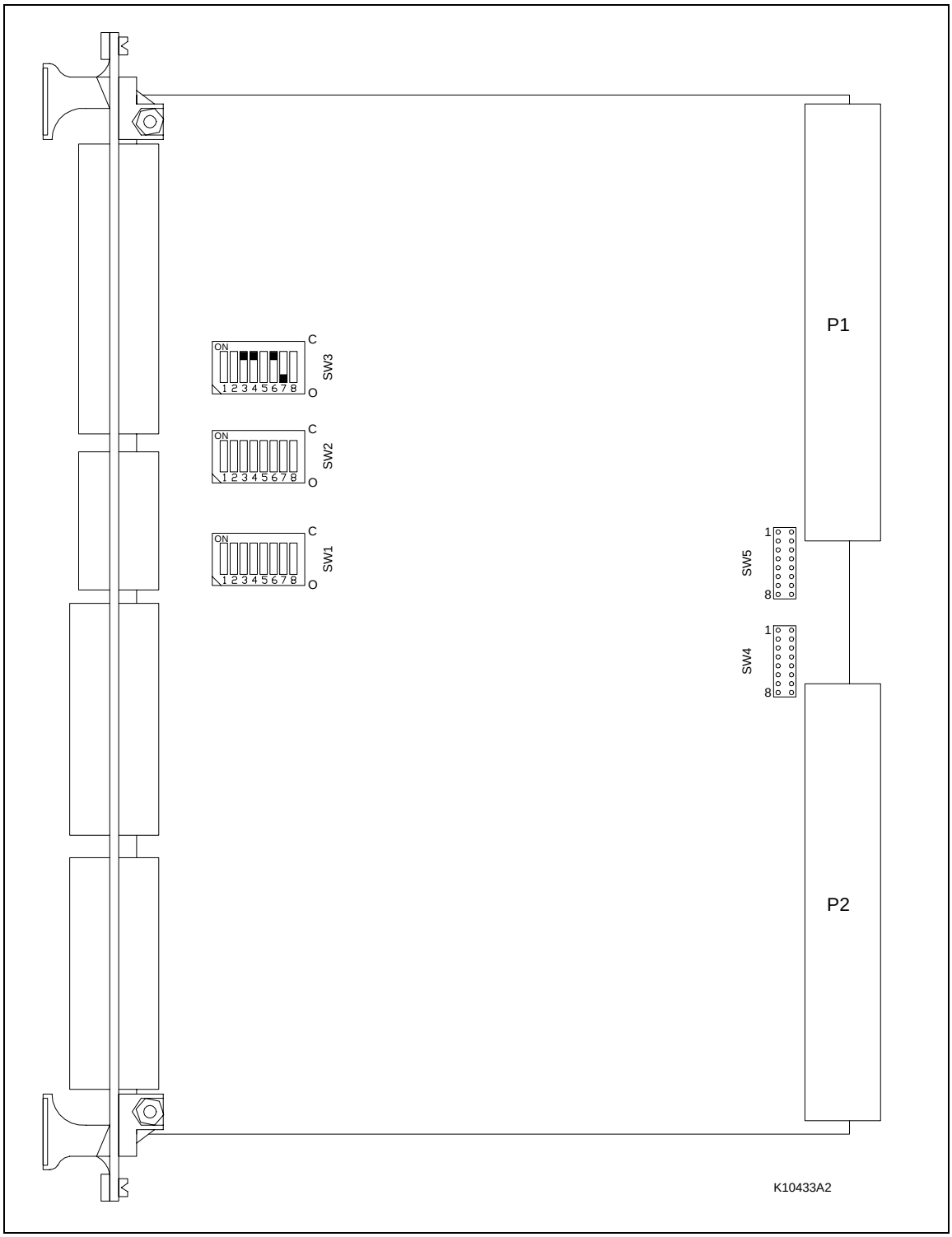


Figure 5 - Switch settings for all boards using FPDP PECL clock

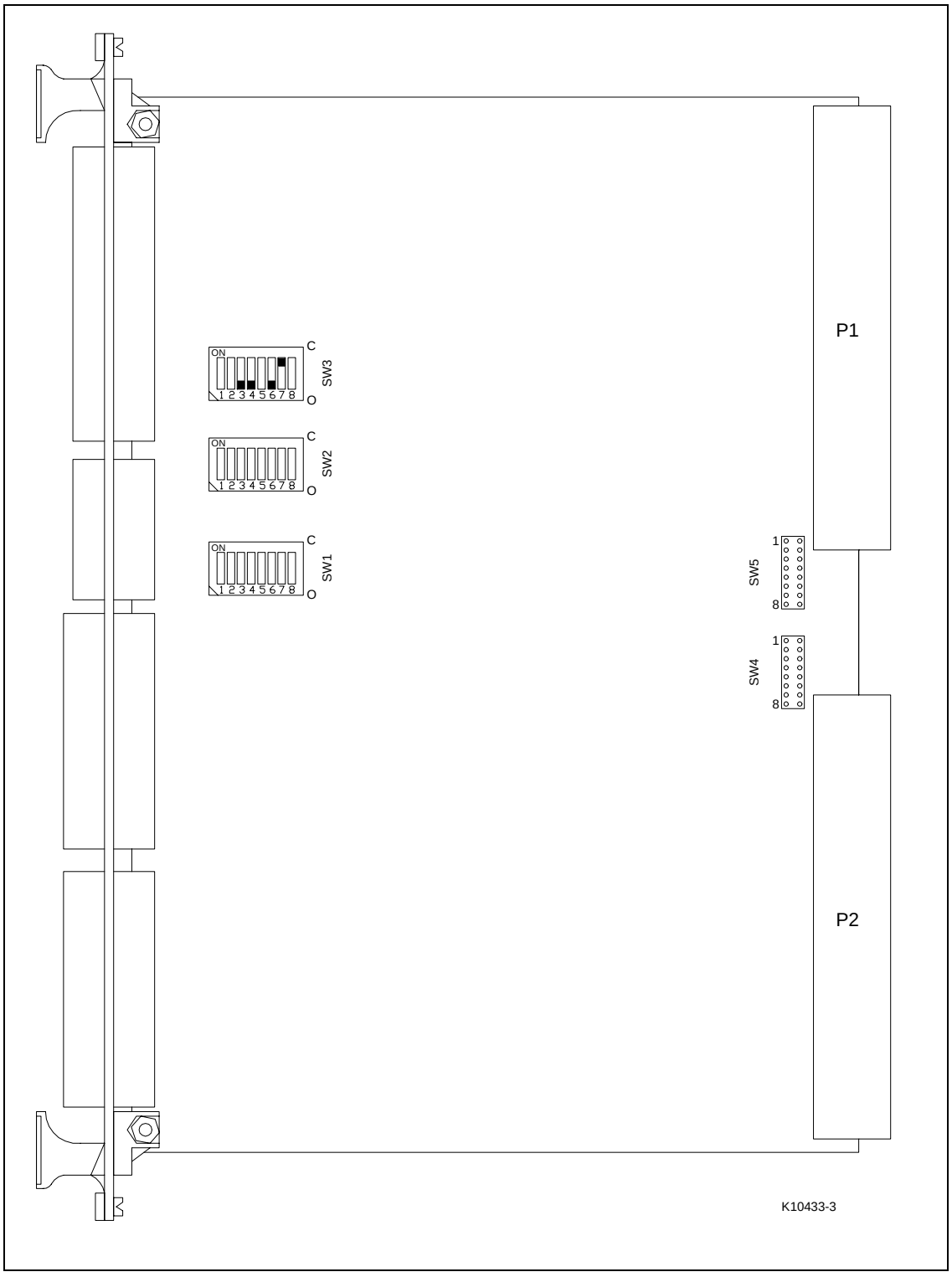


Figure 6 - Switch settings for all boards using FPDP TTL clock

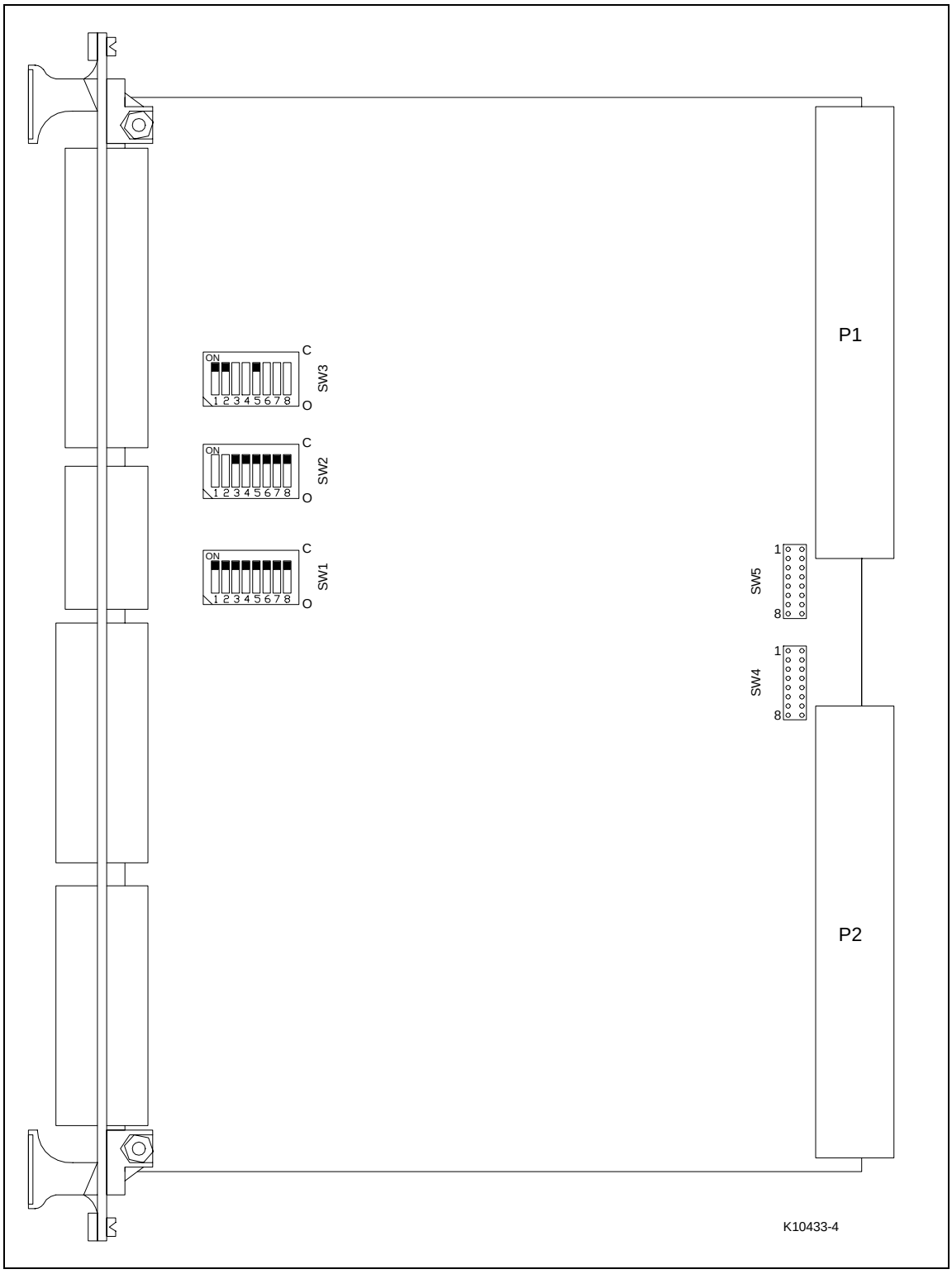


Figure 7 - Switch settings for Stand-Alone Master configuration

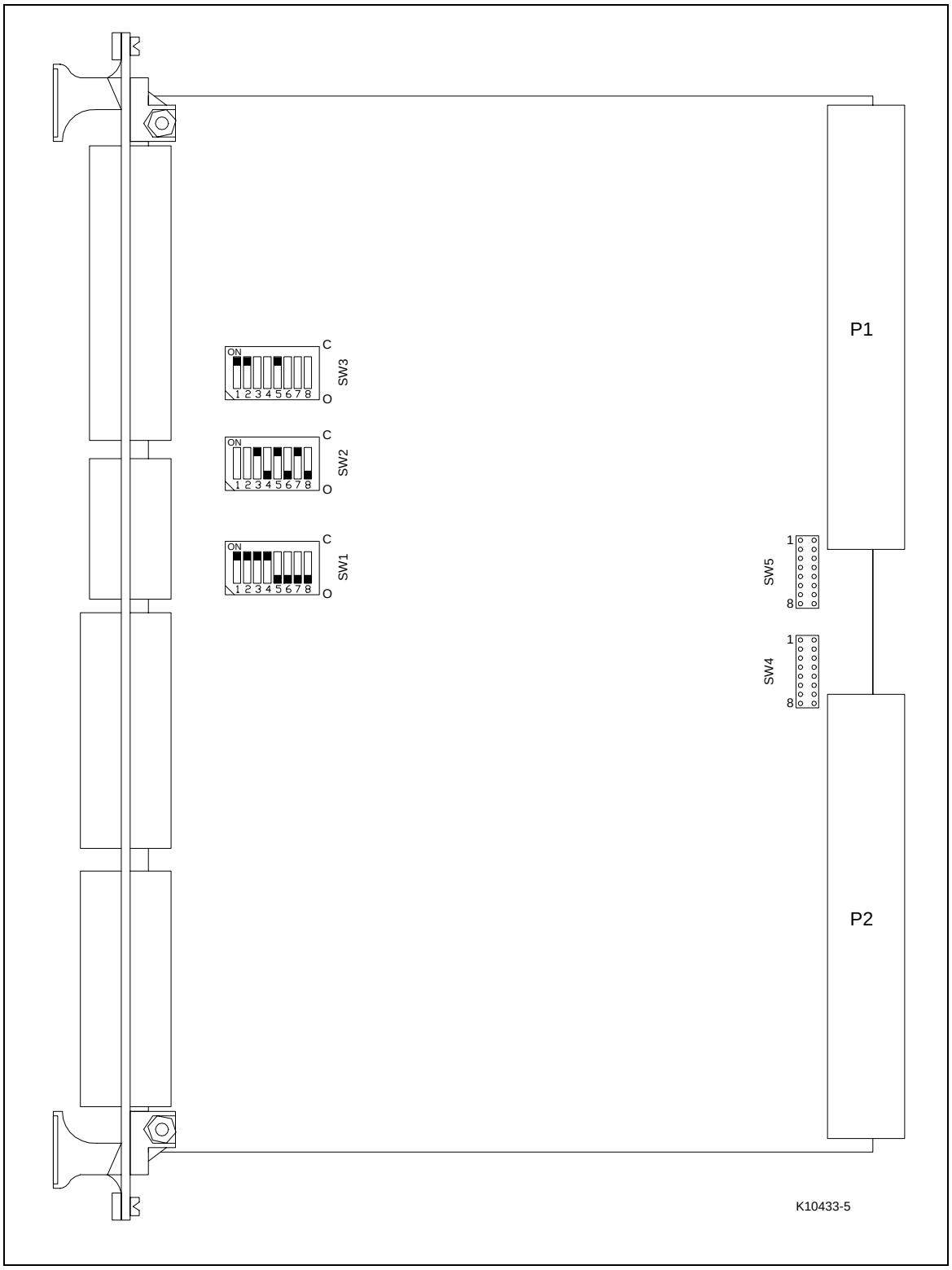


Figure 8 - Switch settings for Master configuration

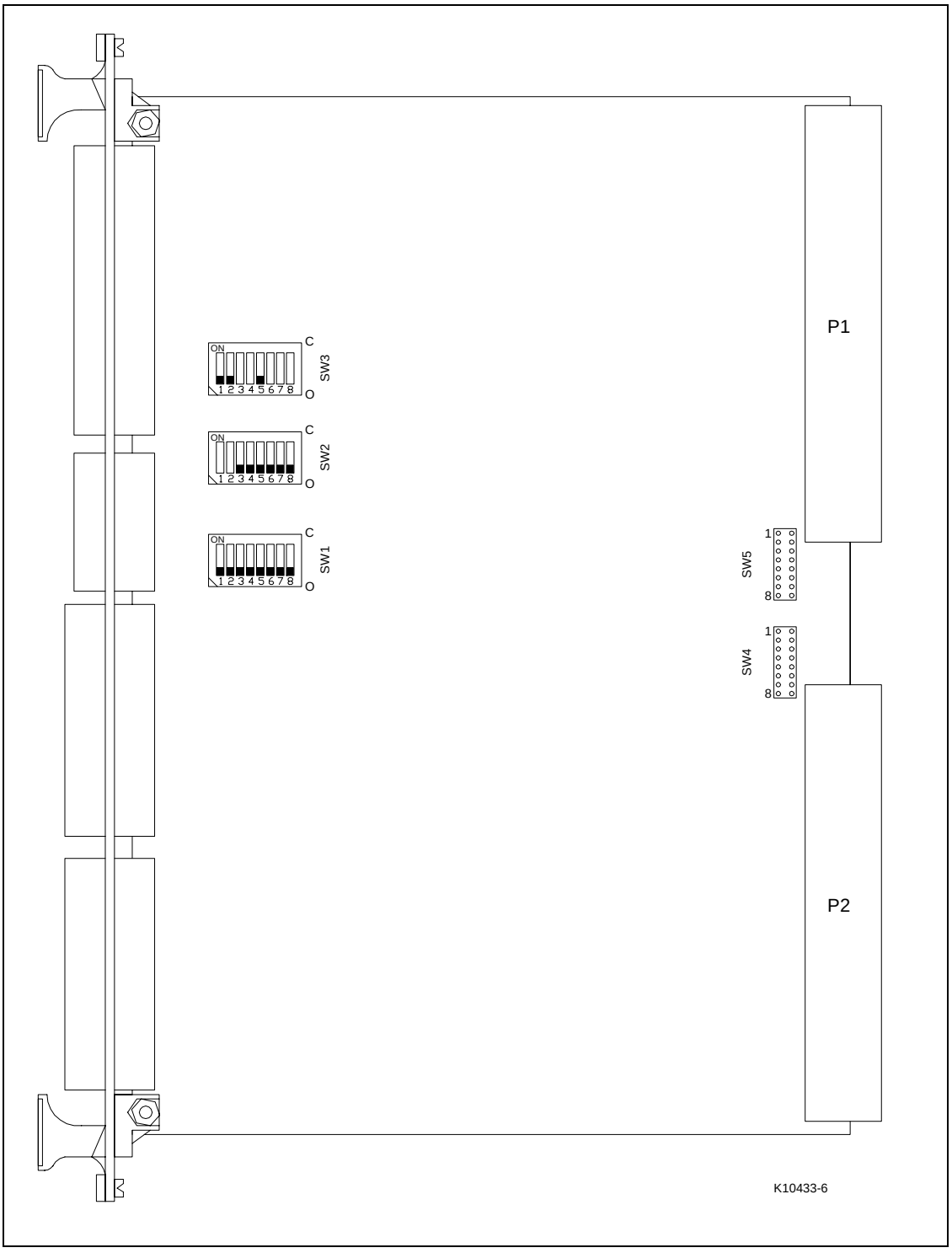


Figure 9 - Switch settings for Slave configuration

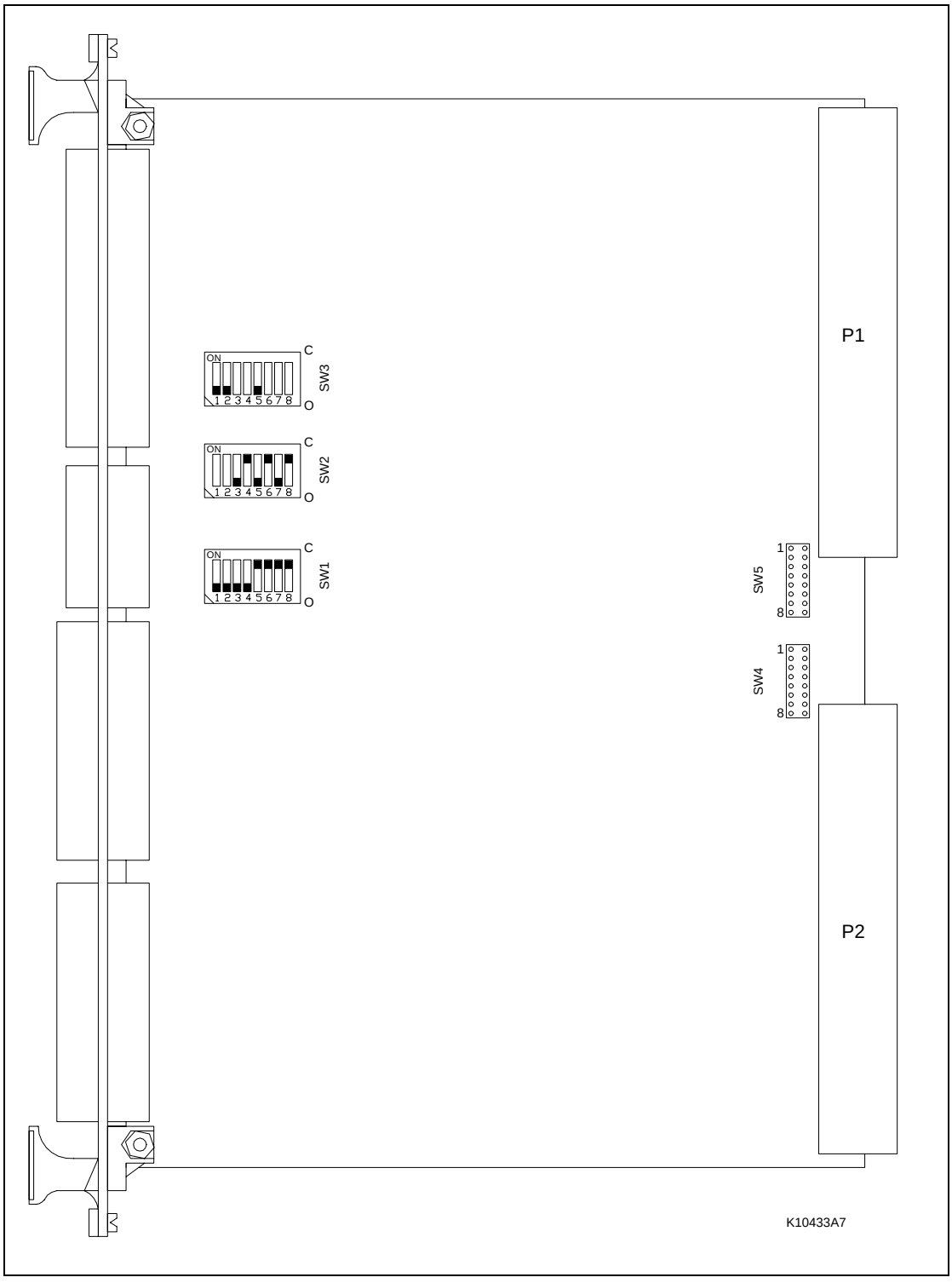


Figure 10 - Switch settings for End Slave configuration

5 PROGRAMMING MODEL

The ICS-115A VMEbus memory map is shown in Figure 11. The individual bit fields of the registers are shown in Figure 12. All programming and control of the ICS-115 is accomplished through the VMEbus interface. All control register bits that are not defined have no effect on the operation of the ICS-115A, but will always be read as zero. All other bits are undefined, and may be read as zero or one.

The ICS-115A VSB Memory Map is shown in Figure 13. The interface provides a 32 MByte Respond address space for writing DAC data. In practice, the size of VSB data transfers will be limited not by this figure, but by the Swing Buffer length. The ICS-115A also provides 512 MByte Broadcast and 512 MByte Broadcall address spaces to allow multiple boards to participate in VSB transfers.

ICS offers software drivers for the ICS-115A for a number of platforms (including VxWorks, SunOS, Solaris). These drivers greatly simplify control and operation of the ICS-115A, and are strongly recommended. Using one of these drivers will generally save programmers much time since they are relieved of the requirement to understand the complexities of the ICS-115A hardware model and of the Newbridge SCV64 VMEbus interface device. Contact ICS for further details.

5.1 General Notes

All transfers to and from the ICS-115A control and status registers should be done using D32 VMEbus cycles. The A24 and A32 VMEbus base addresses are programmed with jumpers as described in section 4. The ICS-115A responds to both SUPERVISORY and NON-PRIVILEGED VMEbus cycles. Individual bits in the 32 bit registers are referred to in braces. e.g. CR1<0> corresponds to Control Register #1 bit 0, and DEC<7:0> corresponds to Decimation Register bits 7 through 0.

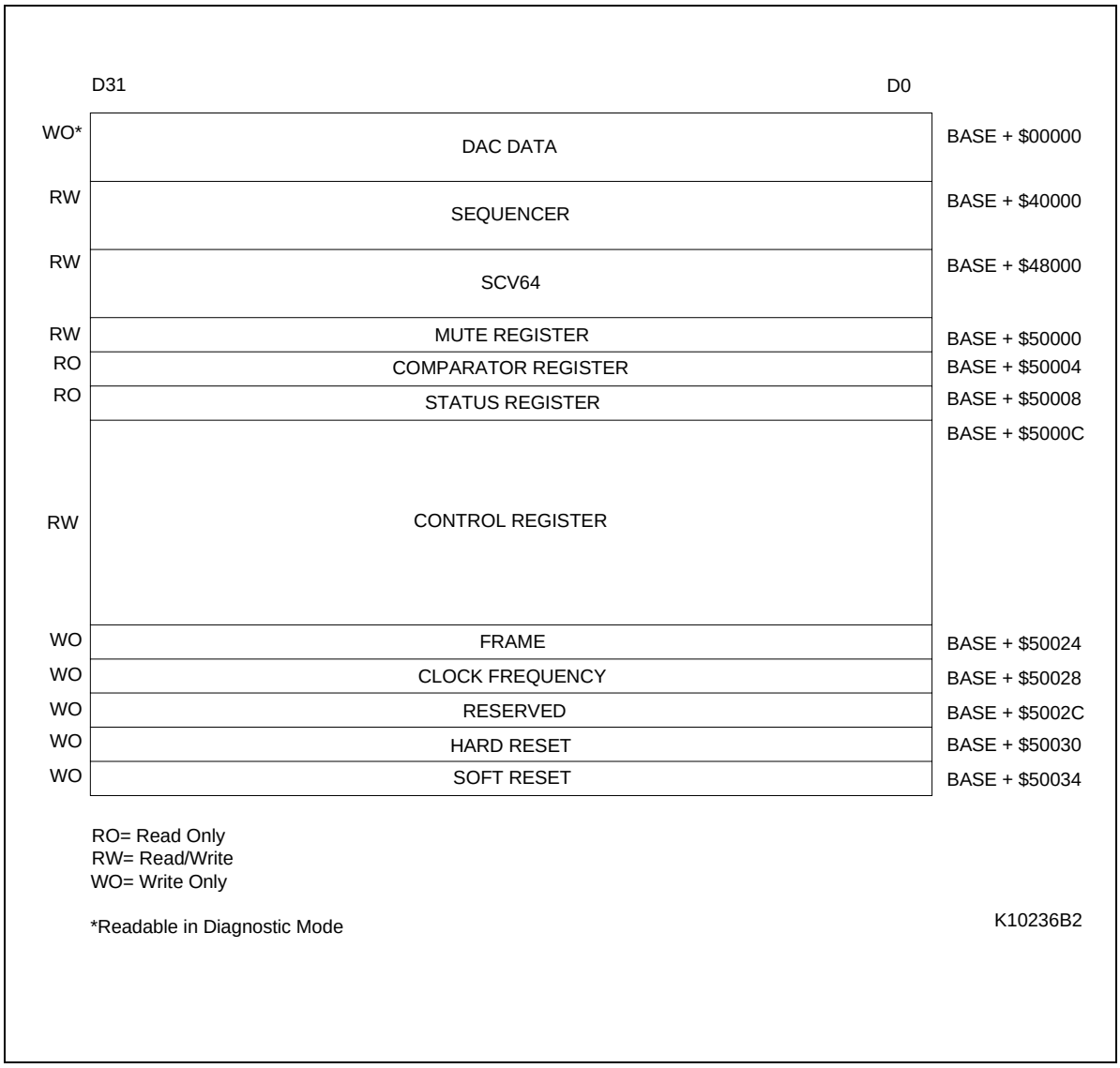


Figure 11 - ICS-115A VMEbus Memory Map

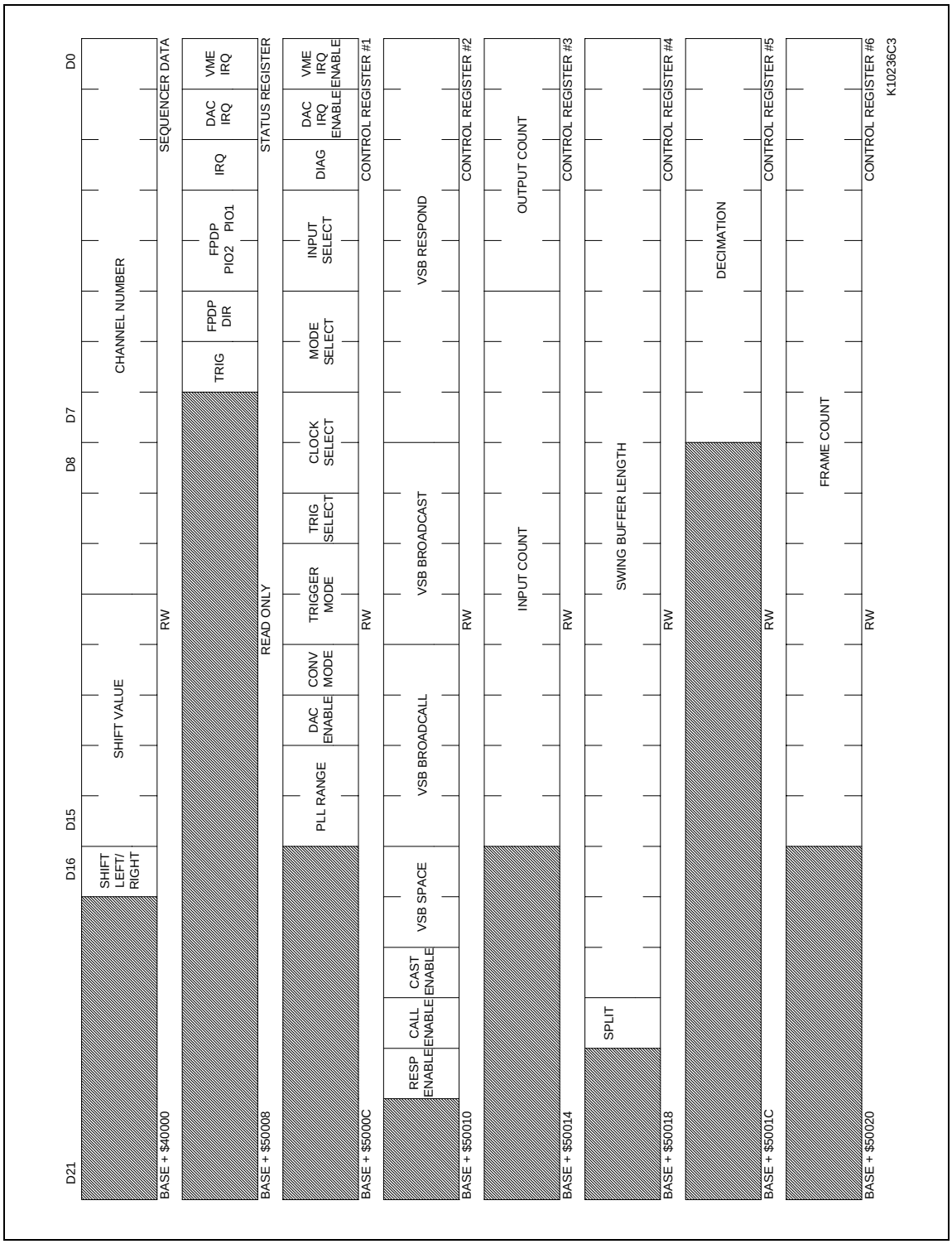


Figure 12 - ICS-115A VMEbus Register Definitions

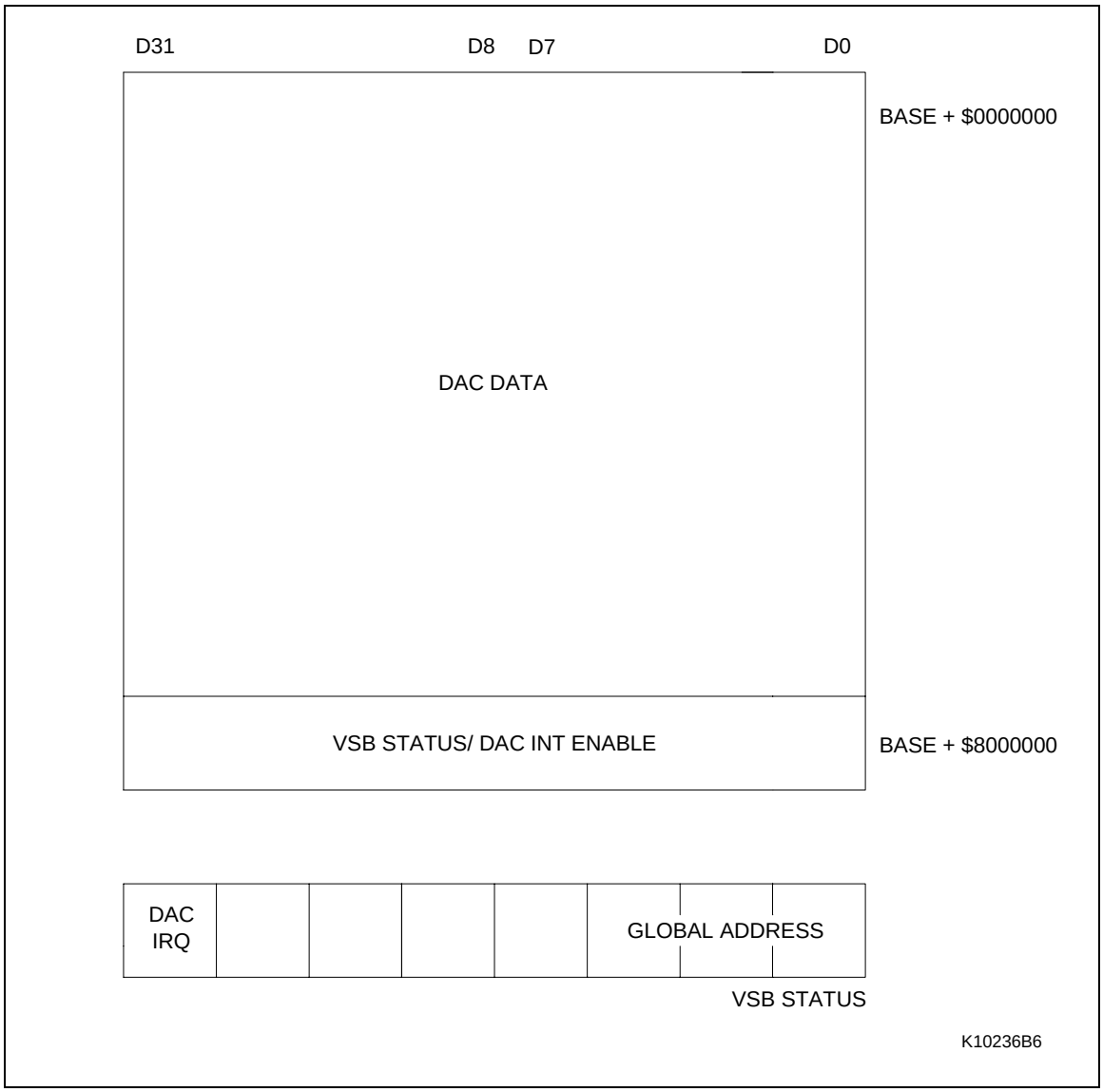


Figure 13 - ICS-115A VSB Memory Map

5.2 SCV64 Registers

The ICS-115A uses the Newbridge SCV64 VMEbus interface chip to handle all VMEbus communications. Full details of the SCV64 may be found in the SCV64 User Manual (See Ref. 1). Table 5.1 gives descriptions for the SCV64 registers which may be needed when programming the ICS-115A. Unless the Master BLT/MBLT or the A64 capability of the SCV64 is to be utilized, the power-up defaults of the register contents are sufficient, with the following exception: the MODE register should be programmed to the hexadecimal value 0x9480e401. This value is chosen to optimize speed of transfer between the ICS-115A and the VMEbus. Descriptions of some of the bits of the MODE register are given in Table 5.1. For a more detailed description, see Ref. 1.

If the user wishes to employ VMEbus 64-bit address cycles (A64 addressing mode) when addressing the ICS-115A, it is necessary to program the most significant 32 bits of the ICS-115A base address to SCV64 register SA64BAR. The procedure for doing this is as follows:

i) Set MODE<12> to '1' (coupled mode).
ii) Write most significant 32 bits of VMEbus address to SA64BAR.
iii) Clear MODE<12>.

The least significant 32 bits of the 64-bit base address are taken from the A32 base address values configured for the board using jumpers SW4 and SW5 (see section 4). These settings are loaded to the SCV64 VMEBAR register at power up, but can be subsequently reprogrammed by the user.

The register map of the SCV64 is complex; only the relevant register assignments are discussed here. For this reason, accesses to the SCV64 memory space other than to documented offsets may have unpredictable consequences and should be avoided. The SCV64 has two sets of address and data busses, one connected to the VMEbus and the other to the ICS-115A local bus. VMEbus accesses are mapped from VMEbus space to local bus according to the programming of the SCV64. When the SCV64 is used to perform VMEbus Master transfers, it simultaneously becomes the local bus Master, and the VMEbus Master. When VMEbus Slave cycles occur, the SCV64 is the VMEbus Slave, but the local bus Master. When performing VMEbus Master transfers, the SCV64 can be configured to use normal cycles (VMEbus address broadcast between each cycle), BLT (D32 block transfer), or MBLT (D64 multiplexed block transfer). All register offsets are given with respect to the beginning of the SCV64 register window (BASE + 0x48000).

When the SCV64 is programmed to operate as the VMEbus Master, some caution must be taken when considering transfer counts. This is discussed in section 5.3.

TABLE 5.1 SCV64 Register Descriptions

Name	Register	Read/Write	Offset	Description
DMALAR	DMA Local Address	R/W	0x0	This register contains the local bus address used by the SCV64 when performing a VMEbus Master. This register must be re-programmed to zero before each Master transfer cycle is initiated.
DMAVAR	DMA VMEbus Address	R/W	0x4	This register contains the VMEbus address accessed by the SCV64 when it is performing a VMEbus Master transfer cycle. If not re-programmed between cycles, it continues from the next consecutive address.
DMATC	DMA Transfer Count	R/W	0x08	This register contains the DMA transfer count (Longwords) used by the SCV64 when it is performing a VMEbus Master transfer cycle. Register width is 20 bits (DMATC<19:00>).
DCSR	Control and Status Register	R/W	0x0C	The following describes the bits of the SCV64 Control and Status Register used by the ICS-115A. All other bits should be set to 0 during a write. The register should always be cleared before starting to set up a DMA transfer.
				DCSR<16> When asserted, this bit indicates an SCV64 configuration error
				DCSR<12> A64 base address ready. Must be programmed to 1 after the SA64BAR and MA64BAR registers have been programmed.
				DCSR<5> If asserted, a bus error has occurred during a DMA transfer. Write a '0' to clear the error.
				DCSR<3:2> If either of these bits are asserted, the previous DMA cycle failed. This can result from transferring too much data (See SCV Registers) or BERR was asserted on the VMEbus during the transfer. Writing '0' to these bits clears them.

				DCSR<1> When asserted, the previous DMA cycle was successfully completed. Writing '0' to this bit clears it.
				DCSR<0> Writing a '1' to this bit starts the DMA cycle. Reading a '1' indicates that a DMA cycle is in progress. A DMA cycle may be aborted while in progress by clearing this bit. In this case, DCSR<1> will be set, and a transfer complete interrupt will be requested.
VMEBAR	VMEbus Slave Base Address Register	R/W	0x10	This register is used to set the VME A24 and A32 Slave Base Address values. The A32 SBA is also used as the LS 32 bits of the A64 Slave Base Address. On power up, the A24 and A32 values are loaded from the on-board jumpers (see section 4).
				VMEBAR<22:21> Size of A24 slave image: 0 - 512K 1 - 1M 2 - 2M 3 - 4M
				VMEBAR<20:16> Base address of A24 slave image. These bits form bits A23-A19 of base address. Address bits A17 and A16 are forced to zero according to setting of VMEBAR<22:21> described above.
				VMEBAR<08:05> A32 slave image size. Selectable in powers of two from 4K to 128M. Program 0 for 4K, 0xF for 4M.
				VMEBAR<04:00> A32 base address. Selects base address in increments of 0x0800.0000 from 0x0000.0000 to 0xF800.0000. Program 0 for A32 address 0x0000.0000.
IVECT	VMEbus Interrupter Vector Register	R/W	0x24	This register contains the interrupt vector the SCV64 responds with during an interrupt acknowledge cycle.

MODE	Mode Control Register	R/W	0x3C	The following describes the bits of the SCV64 Mode Control Register which may need to be accessed when using the ICS-115A. All other bits should be set to '0' during a write.
				MODE<31> This bit controls the maximum transfer size of the SCV64. When set to '0', the maximum programmable transfer size is 4K (12 bit transfer count). When set to '1', the maximum is 2M (20 bit transfer count).
				MODE<28> This bit should always be written as '1'.
				MODE<26> This bit should always be written as '1'.
				MODE<23> When set to '0', the SCV64 uses non-privileged AM codes when doing Master transfers. When set to '1' it uses supervisory AM codes. Must be cleared if MODE<20> is set to '1'.
				MODE<20> When set to '1' SCV64 Master transfer cycles are performed using A64 addressing on the VMEbus. Otherwise A32 or A24 cycles are used, as determined by MODE<9>.
				MODE<19> When set to '1', SCV64 Master transfer cycles are performed using MBLT (D64) cycles on the VMEbus. Must be cleared if MODE<9> is set to '1' or if MODE<18> is set to '1'.
				MODE<18> When set to '1' SCV64 Master transfer cycles are performed using BLT cycles on the VMEbus. Must be cleared if MODE<19> is set to '1'.
				MODE<16> When set to '0' SCV64 Master transfer cycles are performed from ADC memory to the VMEbus, and from the VMEbus to DAC memory when '1'.
				MODE<15:13> These bits should always be written as all '1's.

				MODE<12> When set to '1', the receive FIFOs couple VME and local buses. When '0', busses are uncoupled. Should normally be written as '0', except when accessing SA64BAR and MA64BAR registers (see descriptions below).
				MODE<10> When set to '0' the VMEbus Slave image of the ICS-115A is disabled (will not respond), and enabled when set to '1'.
				MODE<9> When set to '0', the SCV64 Master operates in A32 or A64 mode (as determined by MODE<20>), and in A24 mode when set to '1'.
				MODE<0> If set to '0', all Slave images of the SCV64 are disabled. IN THIS EVENT, THE ICS-115A CANNOT BE ACCESSED UNTIL A VMEBUS RESET OCCURS.
SA64BAR	Slave A64 Base Address Register	R/W	0x40	This register sets bits 63-32 of the VMEbus A64 slave base address. The remaining bits (31-0) are taken from the A32 image. Before accessing this register, MODE<12> must be set to '1'. After accessing this register, MODE<12> should be cleared.
MA64BAR	Master A64 Base Address Register	R/W	0x44	This register sets bits 63-32 of the VMEbus A64 master base address. The remaining bits (31-0) are taken from the A32 image. Before accessing this register, MODE<12> must be set to '1'. After accessing this register, MODE<12> should be cleared.
VINT	VMEbus Interrupter Request Register	R/W	0x8C	The least significant three bits (D2:0) set the interrupt level of generated by the SCV64. Programming D3 high enables the interrupt. This bit is reset when the interrupt is acknowledged. Caution: Changing the interrupt level while D3 is in the enable state may cause improper operation.
VREQ	VMEbus Requester Register	R/W	0x90	The following describes the contents of VREQ:
				VREQ<7> VMEbus Ownership Timer Enable. Condition 1 after reset. 0 = Disable Timer, 1 = Enable Timer.

				VREQ<6>	Bus Clear Recognition Control. Condition 0 after reset. 0 = Ignore BCLR* signal. 1 = Release bus if BCLR* asserted.
				VREQ<5>	VMEbus Release Mode Control. Condition 1 after reset. 0 = Release on Request (ROR), 1 = Release when Done (RWD).
				VREQ<4>	VMEbus Request Mode Control. Condition 1 after reset. 0 = Fair, 1 = Demand.
				VREQ<3:2>	VMEbus Ownership Timer (Time-out Period). Condition 3 after reset. 0=Zero, 1=2microsec, 2=4microsec, 3=8microsec.
				VREQ<1:0>	VMEbus Request Level. Condition 3 after reset. 0 = Level Zero.

5.3 Performing Block Transfers

When performing block (DMA) transfers, it is important that the transfer count is correctly programmed. If not, data loss may occur. The maximum size of the transfer is determined by one of three factors: the size of the data block currently available, the size of the ICS-115A data area (VMEbus or VSB), or the Swing Buffer length which has been programmed in CR4, whichever is smaller. When considering Swing Buffer size, it is important to take into account cases where the input frame size is larger than the output frame size (i.e. some channels are discarded by the Sequencer).

The size of the VMEbus data area is 64K long (32-bit) words. The size of the VSB data area is 8M longwords; the latter, therefore, is never a determining factor.

The maximum Swing Buffer block size may be determined using the following expression:

$$B = S \times M \times \frac{I}{O}$$

Where, B = Maximum block size (longwords)
S = Swing buffer programmed size (samples)
M = 1 for Continuous mode
= 2 for all other modes
I = Input frame size (longwords)
O = Output frame size (samples)
S must always be an integral multiple of O

The expression takes into account the fact that input data may be packed as either one or two samples per longword. A factor of two is included for mode of operation; this is because only half of the swing buffer is filled at each transfer for continuous mode operation. When programming the SCV64 for VME Master transfers, the transfer count must be specified in longwords. Note that the VMEbus specification limits block transfers to a maximum of 256 Bytes, however, the ICS-115A design does not prevent transfers of larger blocks as described above.

Details of the procedures required to perform block transfers are given in the following sections.

5.3.1 VMEbus DMA Master

The SCV64 device is capable of acting as bus master and can generate VMEbus block transfers when doing so. Block transfers are also known as Direct Memory Access (DMA) transfers. The SCV64, when acting as bus master, is capable of generating either BLT (D32) standard block transfer cycles or MBLT (D64) multiplexed block transfer cycles in all three address modes.

The order of programming for Master BLT and MBLT transfers is as follows. All register references are to SCV64 registers. For register details, please refer to Table 5.1 above.

1. Clear the DCSR register.
2. Set up the addressing and data transfer modes by writing to the MODE register. The default to be used for setting this register should be 0x9480e401. The following bits of the register may need to be changed - refer to the descriptions in Table 5.1:

   MODE<23>
   MODE<20>
   MODE<19>
   MODE<18>
   MODE<17>
   MODE<16>
   MODE<15:13>
   MODE<12>
   MODE<9>

3. Clear the DMALAR (local bus address) register.
4. Write the VMEbus address (least significant 32 bits for A64 address) to DMAVAR. This is the source address for a read operation for the VMEbus master interface.
5. For A64 address cycles only, write the most significant 32 bits of the VMEbus source address to MA64BAR, using the following procedure:

i) Set MODE<12> to '1' (coupled mode).
ii) Write most significant 32 bits of VMEbus address to MA64BAR.
iii) Clear MODE<12>.

6. Write the transfer count (number of 32 bit longwords) to DMATC.
7. Set DCSR<0>. This is the 'DMAGO' bit. The transfer will start at this point.
8. At the completion of the transfer DMAGO will be read as clear. The DONE bit, DCSR<1>, should be read as set, and a VME interrupt will be asserted. The user should clear DCSR<1> in order to clear the interrupt. If a completion interrupt occurs but the DONE bit is not read as set, an error has occurred. The type of error is indicated by bits DCSR<3:2> and DCSR<5>.

5.3.2 VMEbus DMA Slave

The SCV64 is also capable of acting as slave when performing a VMEbus BLT or MBLT block transfers. In this case, no set-up activity is necessary unless the programmer wishes to use A64 address cycles. The set-up procedure for doing this is given in section 5.3 above. The VMEbus DAC Data area is 0x40000 in size; thus the maximum possible block transfer is 256KB.

5.3.3 VSB DMA Slave

When performing a VSB block transfer with the ICS-115A as the slave device, it is only necessary to ensure that Control Register 2 has been programmed appropriately. The most significant 8 bits (or 4 bits for Broadcast and Broadcall address spaces) of the VSB slave base address must be written; the Slave Enable bit (Respond, Broadcast or Broadcall) must be set; and the VSB Space Code must be set to agree with that of the VSB master device. The VSB DAC Data area is 0x2000000 in size; thus the maximum possible block transfer is 32MB.

5.4 Using Diagnostic Mode

In diagnostic mode, digital data written to the board may be read back. This mode, unlike using the analog comparator feature, does not test the DACs. When using diagnostic mode, a valid clock must be provided. Data may be sourced from VMEbus, VSB or FPDP. Reading of data read may only be from VMEbus. The sequence of programming required to use diagnostic mode is as follows:

1. Configure control registers
2. Program Mute register if required (See Note 2)
3. Write Swing buffer up to programmed length
4. Enable diagnostic mode in CR1<2>
5. Enable DACs
6. Perform a dummy read of one 32-bit word and discard it
7. Read data for comparison

Note 1: Steps 4 and 5 above may be done in the same register access.

Note 2: Analog channel outputs will be unpredictable during diagnostic mode operation. If this is undesirable, the Mute register should be programmed to zero the outputs prior to start of diagnostic mode operation.

5.5 DAC Data

Write Only (Normal Operation)
Read Only (Diagnostic Mode Operation)

This section of the ICS-115A's VMEbus memory map is used to move data to the DAC memory from VMEbus, and to read back DAC data when using **diagnostic** mode (see section 5.10, Control Register description). The data is written to the data area in a FIFO (First In First Out) fashion, hence successive addresses used for access to the data area may be either incremental or repetitive, provided that they fall within the data area.

The significant data may be presented in any adjacent sixteen bits of the 32-bit data path width, and subsequently shifted using the ICS-115A's barrel shifter. Since all 32 bits are used, the user can increase VMEbus data transfer rates by packing two channels per longword with the sequencer programmed to unpack them when transferring to the Swing Buffer, thus doubling the input data rate.

5.6 Sequencer Data (SD)

Read/Write

The Sequencer Data area programs the channel source and shift for each output channel during transfer from the dual port input buffer to the swing buffer. The 32-bit longwords of this area are indexed by board channel number (i.e. output channel number - BASE+0x40000 contains output channel N configuration, BASE+0x40004 contains output channel N-1 configuration, ..., BASE+0x4007C contains output channel 1 configuration if all 32 channels are selected). N, the number of output channels in use is programmed to Control Register 3 (CR3) Output Channel Count field. Each longword must be programmed with the input data frame source channel number, shift amount and shift direction of the data to be applied to that output channel.

Thus, for example, the user may program the sequencer to select the same input data frame channel number for output on two different channels, but with different shifts, thus allowing for packing of two samples per input word.

5.6.1 SD<10:0> - Channel Number

These bits select which channel of the input data frame is to be selected for conversion (valid values are 0 to 2047 or frame size, inclusive). The numbering of the channels in the input data frame is in reverse order. For example, if CR3<4:0> were programmed with the value 9 (i.e. 10 output channels) and CR3<15:5> were programmed with 127 (i.e. 128 input channels), and it is required that the first input channel arriving at the board be output on channel 1, the value 127 should be written to BASE+0x40024<10:0>, i.e. the tenth long word of the Sequencer Data area.

5.6.2 SD<15:11> - Shift Value

These bits determine the number of bits of shift to be applied by the barrel shifter. When shifting left, the barrel shifter fills from the right with zeros. When shifting right, the barrel shifter sign extends. The output of the barrel shifter is taken from the least significant 16 bits, so the sequencer must be programmed to shift the desired sixteen bits of the input into the least significant sixteen bit positions. The five-bit shift value is equal to the number of bits shifted, when performing a left shift. When performing a right shift, the number of bits shifted is equal to (32 – shift value). For example, a right shift value of 31 gives a shift equal to 32- 31 = 1 bit. The most commonly used right shift value will be 10000_2 (16), which produces a right shift of 16 bits.

The following tables show the mapping of the 32 input data bits (I0-I31) to the DAC data bits (D0-D15) for each shift direction.

Right Shift								
Shift Code (binary)	Shift Code (decimal)	D15	D14	D13	...	D2	D1	D0
00000	0	I31	I31	I31	...	I31	I31	I31
00001	1	I31	I31	I31	...	I31	I31	I31
00010	2	I31	I31	I31	...	I31	I31	I30
00011	3	I31	I31	I31	...	I31	I30	I29
...		...	...	...	...	...	...	...
10000	16	I31	I30	I29	...	I18	I17	I16
...		...	...	...	...	...	...	...
11100	28	I19	I18	I17	...	I6	I5	I4
11101	29	I18	I17	I16	...	I5	I4	I3
11110	30	I17	I16	I15	...	I4	I3	I2
11111	31	I16	I15	I14	...	I3	I2	I1

Left Shift								
Shift Code (binary)	Shift Code (decimal)	D15	D14	D13	...	D2	D1	D0
00000	0	I15	I14	I13	...	I2	I1	I0
00001	1	I14	I13	I12	...	I1	I0	0
00010	2	I13	I12	I11	...	I0	0	0
00011	3	I12	I11	I10	...	0	0	0
...		...	...	...	...	...	...	...
11100	28	0	0	0	...	0	0	0
11101	29	0	0	0	...	0	0	0
11110	30	0	0	0	...	0	0	0
11111	31	0	0	0	...	0	0	0

5.6.3 SD<16> - Shift Direction

This bit reflects the direction the barrel shifter will shift the selected input.

SD<16>	Shift Direction
READ/WRITE	
0	Input data is shifted left
1	Input data is shifted right

5.7 Mute Register (MR)

Read/Write

The 32-bit Mute Register allows muting of pairs of DAC outputs. MR<0> corresponds to channel no. 1 & 2 mute control, and MR<30> corresponds to channel no. 31 & 32 mute control. Writing a '0' to the bit corresponding to the desired pair of channels causes those outputs to be muted (i.e. immediately set to zero volts). The odd-numbered bits of this register are not used.

Note: At power-up, the state of the Mute register bits is undefined, and therefore some channels may be enabled while others are muted.

5.8 Comparator Status (CS)

Read Only

The 32-bit Comparator Status register reflects the output state of the thirty-two analog diagnostic comparators on the outputs of adjacent channels. CS<00> corresponds to the output of the comparator connected between the negative legs of channels 1 & 2. CS<01> corresponds to the output of the comparator connected between the positive legs of channels 1 & 2. CS<02> corresponds to the output of the comparator connected between the negative legs of channels 3 & 4. etc. A bit will be set if the lower numbered channel has a more positive voltage than the higher numbered channel of the pair. Therefore, unless the outputs of two adjacent channels are very similar, the two comparators connected to those channels will display opposite bit settings.

5.9 Status Register (SR)

Read Only

5.9.1 SR<0> - VMEbus Master IRQ

This bit indicates the interrupt status of the SCV64 VMEbus Master interface; it will be asserted when the interface is ready to perform a transfer. If VMEbus interrupts are enabled, an interrupt request will occur when this bit toggles from the zero state to the one state.

SR<0>	VMEbus Master Interrupt Request Status
READ ONLY	
0	SCV64 interrupt is not asserted
1	SCV64 interrupt is asserted

5.9.2 SR<1> - DAC IRQ

This bit reflects the status of the DAC control unit. It is asserted when the DAC memory is ready to accept data. If DAC interrupts are enabled, an interrupt request will occur when the bit is in the one state. Note that if interrupts are enabled when the board is first programmed and before data is loaded, an interrupt will occur immediately. In one-shot modes, the bit will be asserted when the swing buffer has been completely emptied. In continuous mode, it will be asserted when the swing buffer swap occurs, i.e. when the swing buffer is half empty. In loop mode, the DAC interrupt should not be used, since it is meaningless.

SR<1>	DAC Interrupt Request
READ ONLY	
0	DAC control unit is not generating an IRQ
1	DAC control unit is generating an IRQ

5.9.3 SR<2> - VMEbus IRQ

This bit indicates that the ICS-115A is asserting a VMEbus interrupt (Master or DAC). It is therefore an OR of the state of bits 0 and 1 of this register.

VMESR<2>	VMEbus Interrupt Request
READ ONLY	
0	VMEbus interrupt is not asserted
1	VMEbus interrupt is asserted

5.9.4 SR<4:3> - FPDP PIO

These bits indicate the state of the user-defined Front Panel Data Port signals PIO2 and PIO1. SR<4> corresponds to PIO2, while SR<3> corresponds to PIO1. The values read will only be meaningful if driven by a device connected to the ICS-115 P3 connector by an FPDP cable.

5.9.5 SR<5> - FPDP DIR

This bit indicates the state of the Front Panel Data Port signal DIR*. DIR* is asserted low (0) by the data source when ready to initiate data transfers. The value read will only be meaningful if driven by a device connected to the ICS-115 P3 connector by an FPDP cable.

SR<5>	Front Panel Data Port Status
READ ONLY	
0	The FPDP data source has been initialized
1	The FPDP data source is not ready

5.9.6 SR<6> - Trigger Status

This bit is asserted while DAC conversion is in progress.

SR<6>	DAC Status
READ ONLY	
0	Conversion not in progress
1	Conversion in progress

5.10 Control Registers (CR)

Read/Write

The Control Registers are used to control the operation of the ICS-115A. They occupy six consecutive addresses.

5.10.1 Control Register #1 (CR1)

Read/Write

5.10.1.1 CR1<0> - VMEbus SCV64 IRQ Mask

This bit enables the SCV64 interrupt. When set, the SCV64 generates a VMEbus interrupt upon completion of each master transfer.

CR1<0>	VMEbus SCV64 Interrupt Mask
READ/WRITE	
0	SCV64 interrupts are disabled
1	SCV64 interrupts are enabled

5.10.1.2 CR1<1> - VMEbus DAC IRQ Mask

This bit enables the DAC interrupt. When set, the DAC controller generates a VMEbus interrupt whenever ready to accept a block of data. The conditions under which this occurs are described in section 5.9.2.

CR1<0>	VMEbus DAC Interrupt Mask
READ/WRITE	
0	DAC interrupts are disabled
1	DAC interrupts are enabled

5.10.1.3 CR1<2> - Diagnostics Control

This bit enables the **Diagnostic** mode of the ICS-115A. When enabled, data can be read from the FIFO that normally feeds the parallel to serial converters by reading from the DAC Data area (BASE + 0x00000). The data appears in the most significant 16 bits. Data cannot be read from the VSBbus data area in diagnostic mode.

CR1<2>	Diagnostic Mode
READ/WRITE	
0	**Diagnostic** mode disabled
1	**Diagnostic** mode enabled

5.10.1.4 CR1<4:3> - Input Select

These bits determine the source for the DAC data. For FPDP data, the control signal SUSPEND can be either used or ignored.

CR1<4:3>	Source for DAC Data
READ/WRITE	
00	VMEbus
01	VSB
10	FPDP with SUSPEND disabled.
11	FPDP with SUSPEND enabled.

5.10.1.5 CR1<6:5> - Mode Select

These bits determine the mode of operation of the ICS-115A.

CR1<6:5>	DAC Mode
READ/WRITE	
00	**Continuous** Mode
01	**Loop** Mode
10	**One-Shot** Mode with reload
11	**One-Shot** Mode with no reload

5.10.1.6 CR1<8:7> - Clock Select

These bits select between the internal and external clocks. Their setting is not important for slave and end-slave boards.

CR1<8:7>	Clock Select
READ/WRITE	
0	Internal Clock (f = 256 X Conversion Rate)
1	External Clock (f = 256 X Conversion Rate)
2	PLL FPDP Clock (f = FPDP frame rate = Conversion rate)
3	PLL External Clock (f = Conversion Rate)

5.10.1.7 CR1<9> - Trigger Select

This bit selects between the internal and external trigger. Its setting is not important for slave and end-slave boards.

CR1<9>	Trigger Select
READ/WRITE	
0	Internal Trigger
1	External Trigger

5.10.1.8 CR1<11:10> - Trigger Mode

These bits select the triggering mode of the ICS-115A. Their setting is not important for slave and end-slave boards.

CR1<11:10>	Trigger Mode
READ/WRITE	
00	Convert when level high. Cease conversion when level low
01	Initiate conversion on rising edge
11	Initiate conversion on rising edge. Stop conversion on frame count programmed to CR6

5.10.1.9 CR1<12> - Conversion Mode

This bit selects between the synchronous conversion mode (data rate is locked to the conversion rate) and the asynchronous conversion mode (data rate is not locked to the conversion rate). Under normal operating conditions, the synchronous mode should always be used. See also section 3.4.

CR1<12>	Conversion Mode
READ/WRITE	
0	Synchronous conversion mode
1	Asynchronous conversion mode

5.10.1.10 CR1<13> - DAC Enable

This bit is used to start the DAC conversion. If internal triggering is selected, the converion process is started immediately. If external triggering is selected, conversion starts when the trigger is applied, in accordance with the trigger mode selected in CR1<11:10>.

CR1<13>	DAC Enable
READ/WRITE	
0	DAC conversion disabled
1	DAC conversion enabled

5.10.1.11 CR1<15:14> - PLL Range

These bits select the frequency range for the Phase Locked Loop (PLL) circuits. They are used only when an external frame rate (i.e. sampling frequency, not 256X) clock is used. This clock may be provided either externally through P4p10 (CR1<8:7> set = 3) or via the FPDP frame, when using FPDP input (CR1<8:7> set = 2, and CR1<4:3> set = 2 or 3).

CR1<15:14>	External Sampling Clock or FPDP Frame Rate Frequency
READ/WRITE	
00	20 - 50 kHz
01	8.0 - 20 kHz
10	3.2 - 8.0 kHz
11	50-100kHz

5.10.2 Control Register #2 (CR2)

Read/Write

5.10.2.1 CR2<7:0> - VSBbus Respond Base Address

These bits are compared to the most significant eight address lines (A31:A24) during VSBbus cycles. If a match occurs and the respond image is enabled in CR2<20>, the ICS-115A responds to the cycle.

5.10.2.2 CR2<11:8> - VSBbus Broadcast Base Address

These bits are compared to the most significant four address lines (A31:A24) during VSBbus cycles. If a match occurs and the broadcast image is enabled in CR2<18>, the ICS-115 participates in the cycle.

5.10.2.3 CR2<15:12> - VSBbus Broadcall Base Address

These bits are compared to the most significant four address lines (A31:A24) during VSBbus cycles. If a match occurs and the broadcall image is enabled in CR2<19>, the ICS-115 participates in the cycle.

5.10.2.4 CR2<17:16> - VSBbus Space Code

These bits set the VSB Space Code for the slave image to respond or participate in data transfers. The space code must match with that presented by the VSB master in order for an access to succeed.

CR2<17:16>	VSB Space Code for Slave Image
READ/WRITE	
01	Alternate Address Space
10	I/O Address Space
11	System Address Space

5.10.2.5 CR2<18> - VSBbus Broadcast Enable

This bit enables VSBbus Broadcast image. See also VSBbus Broadcast Base Address, CR2<11:8>.

CR2<18>	VSBbus Broadcast Enable
READ/WRITE	
0	Broadcast image is disabled
1	Broadcast image is enabled

5.10.2.6 CR2<19> - VSBbus Broadcall Enable

This bit enables VSBbus Broadcall image. See also VSBbus Broadcall Base Address, CR2<15:12>.

CR2<19>	VSBbus Broadcall Enable
READ/WRITE	
0	Broadcall image is disabled
1	Broadcall image is enabled

5.10.2.7 CR2<20> - VSBbus Respond Enable

This bit enables VSBbus Respond image. See also VSBbus Respond Base Address, CR2<7:0>.

CR2<20>	VSBbus Respond Enable
READ/WRITE	
0	Respond image is disabled
1	Respond image is enabled

5.10.3 Control Register #3 (CR3)

Read/Write

5.10.3.1 CR3<4:0> - Output Channel Count

This register determines the number of channels read by the sequencer from the dual port input buffer for each frame, and hence the number of DAC outputs to be updated each sampling period. This register must be correctly programmed to one less ($N_{outputs}$-1) than the desired count for all operating modes and all sources of data (i.e. VMEbus, VSBbus or FPDP). In multiple board configurations, this count applies to the current ICS-115A only; the maximum value which may be programmed is therefore 31. Note that the minimum number of channels which may be configured for output is two.

5.10.3.2 CR3<15:5> - Input Channel Count

This register must be programmed to the number of input data elements per frame of data. This includes any non-DAC data which may be interleaved with the DAC data. This register must be correctly programmed to one less (N_{inputs}-1) than the desired count for all operating modes and sources of data. Since the maximum allowed frame size is 2048 elements, the maximum value which may be programmed is 2047.

5.10.4 Control Register #4 (CR4)

Read/Write

5.10.4.1 CR4<18:0> - Swing Buffer length

This register determines the length of each half of the Swing Buffer. The length must be an integral multiple of the Output Channel Count, and is programmed as one less (($N_{outputs}$ * $N_{samples}$) -1) than the desired value.

5.10.4.2 CR4<19> - Swing Buffer Split Control

When set, this bit causes the swing buffer to split into four separate buffers of equal length. In this mode of operation the values of the two most significant bits of the Swing Buffer length must be written to determine which of the four buffer segments are to be used for current operation (either for writing to, or during conversion). Note that the remaining size of the swing buffer is still controlled by the least significant 17 bits of the Swing Buffer length.

Data may be written to the entire swing buffer prior to setting the split control. Alternatively, the split control bit may be set and the data subsequently written to each of the four buffer segments by changing the most significant two bits of the swing buffer length register. It is also permissible to reprogram the MS two bits of the swing buffer length register on the fly during normal operation in order to change the portion of the buffer in use.

5.10.5 Control Register #5 (CR5)

Read/Write

5.10.5.1 CR4<7:0> - Decimation Value

This register determine the decimation count. During conversion, the DACs are supplied with new data every decimation count sampling periods (e.g. when the decimation count is 1, data is updated every sample period, when 2, data is updated every two sampling periods). At intervening sampling intervals, the values output by the DACs remain the same as during the previous sampling interval. This mode of operation effectively reduces the sampling rate by the decimation count. However, users are cautioned that decimation reduces the performance advantages of the Delta-Sigma DAC. This register is programmed as one less ($N_{decimate}$-1) than the desired value.

5.10.6 Control Register #6 (CR6)

Read/Write

5.10.6.1 CR6<15:0> - Frame Count

This register determines the number of frames to be converted on each application of the trigger when the trigger mode is set to the **terminate on frame count** mode. This register is programmed as one less (N_{frames}-1) than the desired value.

5.11 Frame Register (FR)

Write Only

A write to this location forces data alignment of the ICS-115A dual port input buffer to a frame boundary. In theory this is not necessary providing that the correct number of words are always written to the ICS-115A (i.e. a number of words corresponding to the input channel count programmed to CR3<15:5>). However, should a fault condition occur, it is possible that misalignment could occur. When VMEbus or VSBbus data paths are used, periodic writes to this register (e.g. at the end of a block transfer) will cause fault recovery.

5.12 Clock Frequency Register (CLK)

Write Only

This register allows the user to program the internal sampling (conversion) frequency. This is done by writing a 22-bit programming word representing the oversampling (256 X) frequency to the on-board programmable oscillator. Data is written serially to the oscillator; i.e. one write must occur for each bit of data to be written, with the desired data in D0. See section 6 for details of programming the oscillator. Note that the minimum sampling frequency which may be programmed is 1.41 kHz.

5.13 Hard Reset Register (HRR)

Write Only

A write to this register resets the board to its power-up state. All registers, memories, and counters on board the ICS-115A are immediately reset.

5.14 Soft Reset Register (SRR)

Write Only

A write to this register resets all on board memory and counters. It does not clear board configuration. A Soft Reset should be performed after all configuration is complete, and before data is written to the board or the DAC Enable bit (CR1<13>) is set. This guarantees that the ICS-115A is properly loaded with all configuration information, and all internal logic is in a known state.

5.15 VSB Memory Map

The layout of the VSB Memory Map of the ICS-115A is shown in Fig. 13. Most aspects of VSB configuration, such as enabling of the VSB slave image, are programmed from the VMEbus. See the descriptions of Control Register #2 in section 5.10.2 above. Data transfer, interrupt enabling and interrupt request status are available on the VSB. These are described below.

5.15.1 DAC Data

This section of the ICS-115A's VSB memory map is used to move data to the DAC memory from the VSB. The organization of data when written to this space is the same as for the VMEbus DAC data area (see section 5.5 above).
The data area appears to the user as FIFO type memory. In other words, data access is always sequential; random access to samples in the memory is not available. Addresses presented by the bus master when writing data may be either incremental or repetitive (i.e. always the same address). Provided that addresses fall within the DAC Data area, consecutive data will be written to the board regardless of the addressing mode. This allows for standard addressing and block transfers with devices which either increment addresses or repetitively present the same address.

5.15.2 VSB Status/Interrupt Enable Register (VSBSI)

Read/Write

When written to, this register enables VSB DAC interrupts. The data written is unimportant. Interrupts must be reenabled after every occurrence. The criteria for an interrupt to occur are the same as for the VMEbus DAC interrupt.

When read from, the register provides information on the VSB Global Address of the board and the interrupt request status. A read clears any existing interrupt request. Details of the register fields are given below.

5.15.2.1 VSBSI<26:24> - VSB Global Address

These bits reflect the VSB Backplane Global Address GA0-2 of the ICS-115A in accordance with the VSB Bus Specification.

VSBSI<26:24>	VSB Backplane Global Address
READ ONLY	
000	VSB Slot 1
001	VSB Slot 2
010	VSB Slot 3
011	VSB Slot 4
100	VSB Slot 5
101	VSB Slot 6

5.15.2.2 VSBSI<31> - Interrupt Request

This bit indicates that the ICS-115A is asserting a DAC interrupt.

VSBSI<31>	Interrupt Request
READ ONLY	
0	Interrupt is not asserted
1	Interrupt is asserted

6 APPENDICES

6.1 Programming the Internal Clock Generator

6.1.1 Introduction

The frequency of the ICS-115A internal sampling clock is controlled by programming the programmable oscillator through the Clock Frequency register of the VMEbus memory map (see Fig. 10 above). The device is programmed not in engineering units, but by means of a complex programming word whose construction is described below; a series of control words must also be written to the device. Data is transferred to the device serially; it is necessary to write the data to the ICS-115A Clock Frequency register one bit at a time; bit 0 of the register is the relevant bit. Thus the programming sequence should normally be done by repeatedly writing each control or programming word to the Clock Frequency register, shifting the data right by one bit after each write, until every bit of the word has been written.

Automatic calculation of the programming word is provided by the ics115calcFoxWord() function and other functions in the 'C' language function library supplied with the optional ICS-115A software drivers, available for SunOS, Solaris 2 or VxWorks environments. These routines generate a 22-bit formatted programming word equivalent to the nearest possible frequency to that supplied as input by the user (in MHz), and also supply the actual frequency represented by the programming word, as an output.

6.1.2 Programming Summary

The oscillator device contains two registers, the Control Register and the Programming Word Register. The programming sequence is as follows:

1. Write to Control Register to configure device and prepare the device to receive the Programming Word.

2. Write Programming Word.

3. Write to Control Register to load Programming Word data into device.

4. Wait at least 10ms for device Voltage Controlled Oscillator (VCO) frequency to stabilize.

5. Write to Control Register to enable device output of new frequency.

6.1.3 Control Register

When writing data to the Control Register, it is necessary to include a Protocol Field to identify the data as Control Register data.

Protocol Field (6 bits) = 0 1 1 1 1 0

It is important that the sequence of four ones contained in the protocol field never be sent except as part of the Protocol Field. Thus, when writing programming word data to the device, it is necessary to use a technique of inserting an extra zero after a run of three ones; this technique is called "bit stuffing", and is described in more detail in section 6.1.4.

The control register contains eight bits, which are defined as shown in Table 6.1.

Table 6.1

Bit No.	Description	Function	Power-up Default
0	Enable Programming Word register to be written by next data	0 = Program Register Disabled 1 = Program Register Enabled to Receive Data	0
1	Internal Output Disable	0 = Output is VCO or f_{REF} 1 = Output is tri-stated	0
2	Internal Multiplexer	0 = Output is VCO frequency 1 = Output is f_{REF}	1
3	Device pin 7 usage	Set to zero only	0
4 - 7	Reserved	Set to 0	0000

Control register data is written to the device starting with bit 0 of the control word, continuing to bit 7 of the control word, and followed by the 6 bits of the Protocol field, for a total of 14 bits.

Note that the default configuration of the device following power-up results in the output being at the frequency of the reference oscillator which is 14.31818 MHz.

6.1.4 Programming Register

The Programming register is written with a 22-bit word describing the required frequency of the output. However, it is essential that programming words do not mimic the Control word Protocol field (see section 6.1.3 above) by containing runs of four consecutive ones. Thus, the device specification requires that a zero must be inserted in the word after each occasion when three one's have been transmitted to the device, regardless of whether the next bit is a 0 or a 1. This procedure is known as "bit stuffing". For this reason, the actual length of a programming word may vary between 22 and 29 bits.
For example, to send this programming data:

Last Bit				**First Bit**
1111	**0101**	**0111**	**1110**	**111111**

Transmit this serial bit stream:

Last Bit				**First Bit**
10111	**0101**	**00111**	**01110**	**01110111**

The fields of the programming word are described in Table 6.2.

Table 6.2

Field	Bits	# of Bits	Notes
P Counter value (P)	<21:15>	7	MSB (Most Significant Bits)
Duty Cycle Adjust Up (D)	<14>	1	Set to logic 0
Mux (M)	<13:11>	3	
Q Counter Value (Q)	<10:4>	7	
Index (I)	<3:0>	4	LSB (Least Significant Bits)

The frequency of the programmable oscillator f_{VCO}, and the output frequency f_{OUT} are determined by these fields as follows:

$$f_{VCO} = 2 * f_{REF} * (P+3)/(Q+2)$$

where, f_{REF} = Reference frequency (i.e. 14.31818 MHz)

$$f_{OUT} = f_{VCO} / 2^{M}$$

The values of the P and Q parameters must be selected so that f_{VCO} remains between 50 MHz and 150 MHz, inclusive. The value programmed to the M field programs a division register to allow sub-multiples of the VCO frequency to be obtained at the output; the maximum divisor possible is 128.

The **Index field (I)** is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to f_{VCO} rather than to the desired output frequency.)

I	f_{vco} (MHz)
0000	50 – 80
1000	80 - 150

If the desired VCO frequency is exactly 80 MHz, then either index value may be used (since both limits are tested). However, the manufacturer recommends using the setting corresponding to the higher frequency range.

6.1.5 VCO Programming Constraints

There are three primary programming constraints the user must be aware of:

1: 50MHz <= Fvco <= 150MHz
2: 1 <= P <= 127
3: 1 <= Q <= 127

The constraints have to do with the trade-offs between optimum speed with lowest noise, VCO stability and factors affecting the loop equation.

6.1.6 Program Register Example

The following is an example of how to calculate a clock programming word:

Derive the proper programming word for 12.8 MHz clock frequency.

Since 12.8 MHz < 50 MHz, quadruple it to 51.2 MHz
Set M to 010_2
Set I to 0000_2

The result:

Fout = 12.8 = $(2*14.31818*(P+3)/(Q+2))/2^M$

where M = 0, 1, 2, 3, 4, 5, 6, 7
since M = 2: (P+3)/(Q+2) = 1.787936735

The two choices of P and Q giving the nearest to the required frequency are:

P	Q	f_{vco}	Error (PPM)
56	31	51.19834	32
115	64	51.19834	32
90	50	51.21503	293

Taking the first set of values, i.e. (P,Q) = (56,31):

P = 56 decimal = 0111000 binary = 0(0)111000

Q = 31 decimal = 0011111 binary = 0011(0)111

NOTE: The presence of three ones in a row in both P and Q values causes zero bit-stuff values to be inserted in each. However, it is necessary to examine the values in the previous (I) field before inserting a zero in the least significant bits of the Q value. If the I field had contained a 1 in the most significant position the inserted zero would have been in a different position.

The full programming word, W is therefore:

W = P, D, M, Q, I = 00111000, 0, 010, 00110111, 0000 = 001110000010001101110000 (382370 Hex)

6.1.7 Oscillator Programming Example

The oscillator requires three control words plus the programming word in order to program a new output frequency (see programming sequence given in section 6.1.2 above). The following paragraphs provide an overview of how the control words are build along side the programming word.

All data is written to the oscillator serially through the ICS-115A ADC Clock register bit 0. The data is written least significant bit first. An example of programming the oscillator to an initial or new frequency is as follows:

1. Load Control register to enable loading of the Programming word register, enable the output and select the reference frequency for output from the Internal Multiplexer. The Protocol word follows the control word. All data is shifted in LSB (Least Significant Bit) first.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 0 1 0 1
	Protocol Word Control Reg. Data

2. Shift in the desired output frequency value via a programming word that is 22 bits in length, plus any required bit stuffs. (Up to 29 bits can be obtained with bit-stuffing). The example programming word for 12.8 MHz, calculated in section 6.1.6 above, is shown below.

	Last Bit First Bit
Programming word for 12.8 MHz (0x382370)	0 0 1 1 1 0 0 0 0 0 1 0 0 0 1 1 0 1 1 1 0 0 0 0

3. Load the Control register to disable further loading of the Programming word register. This causes the required output frequency value to be programmed while keeping the output set to the reference frequency for the time being.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 0 1 0 0
	Protocol Word Control Reg. Data

4. Wait at least 10ms for the VCO to settle to the new frequency. The value will be accurate to within 0.1% within this time.

5. Load the Control register to disable the Internal Multiplexer. This will cause the output to immediately swing to the new frequency.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 0 0 0 0
	Protocol Word Control Reg. Data

6.2 Analog 1-16 Connector Details

Connector on board: ODD44F4R7NTX
Mating connector: ODD44M..... (consult Manufacturer's data for details)
Manufacturer: Positronics Industries Inc., (417)866-2322

PIN	DESCRIPTION	PIN	DESCRIPTION
32	CHANNEL 1-	33	CHANNEL 1+
18	CHANNEL 2-	19	CHANNEL 2+
3	CHANNEL 3-	4	CHANNEL 3+
34	CHANNEL 4-	35	CHANNEL 4+
20	CHANNEL 5-	21	CHANNEL 5+
5	CHANNEL 6-	6	CHANNEL 6+
36	CHANNEL 7-	37	CHANNEL 7+
22	CHANNEL 8-	23	CHANNEL 8+
7	CHANNEL 9-	8	CHANNEL 9+
38	CHANNEL 10-	39	CHANNEL 10+
24	CHANNEL 11-	25	CHANNEL 11+
9	CHANNEL 12-	10	CHANNEL 12+
40	CHANNEL 13-	41	CHANNEL 13+
26	CHANNEL 14-	27	CHANNEL 14+
11	CHANNEL 15-	12	CHANNEL 15+
42	CHANNEL 16-	43	CHANNEL 16+

* all other pins are connected to analog ground on the board

6.3 Analog 17-32 Connector Details

Connector on board: Positronics ODD44F4R7NTX (see above)

PIN	DESCRIPTION	PIN	DESCRIPTION
32	CHANNEL 17-	33	CHANNEL 17+
18	CHANNEL 18-	19	CHANNEL 18+
3	CHANNEL 19-	4	CHANNEL 19+
34	CHANNEL 20-	35	CHANNEL 20+
20	CHANNEL 21-	21	CHANNEL 21+
5	CHANNEL 22-	6	CHANNEL 22+
36	CHANNEL 23-	37	CHANNEL 23+
22	CHANNEL 24-	23	CHANNEL 24+
7	CHANNEL 25-	8	CHANNEL 25+
38	CHANNEL 26-	39	CHANNEL 26+
24	CHANNEL 27-	25	CHANNEL 27+
9	CHANNEL 28-	10	CHANNEL 28+
40	CHANNEL 29-	41	CHANNEL 29+
26	CHANNEL 30-	27	CHANNEL 30+
11	CHANNEL 31-	12	CHANNEL 31+
42	CHANNEL 32-	43	CHANNEL 32+

* all other pins are connected to analog ground on the board

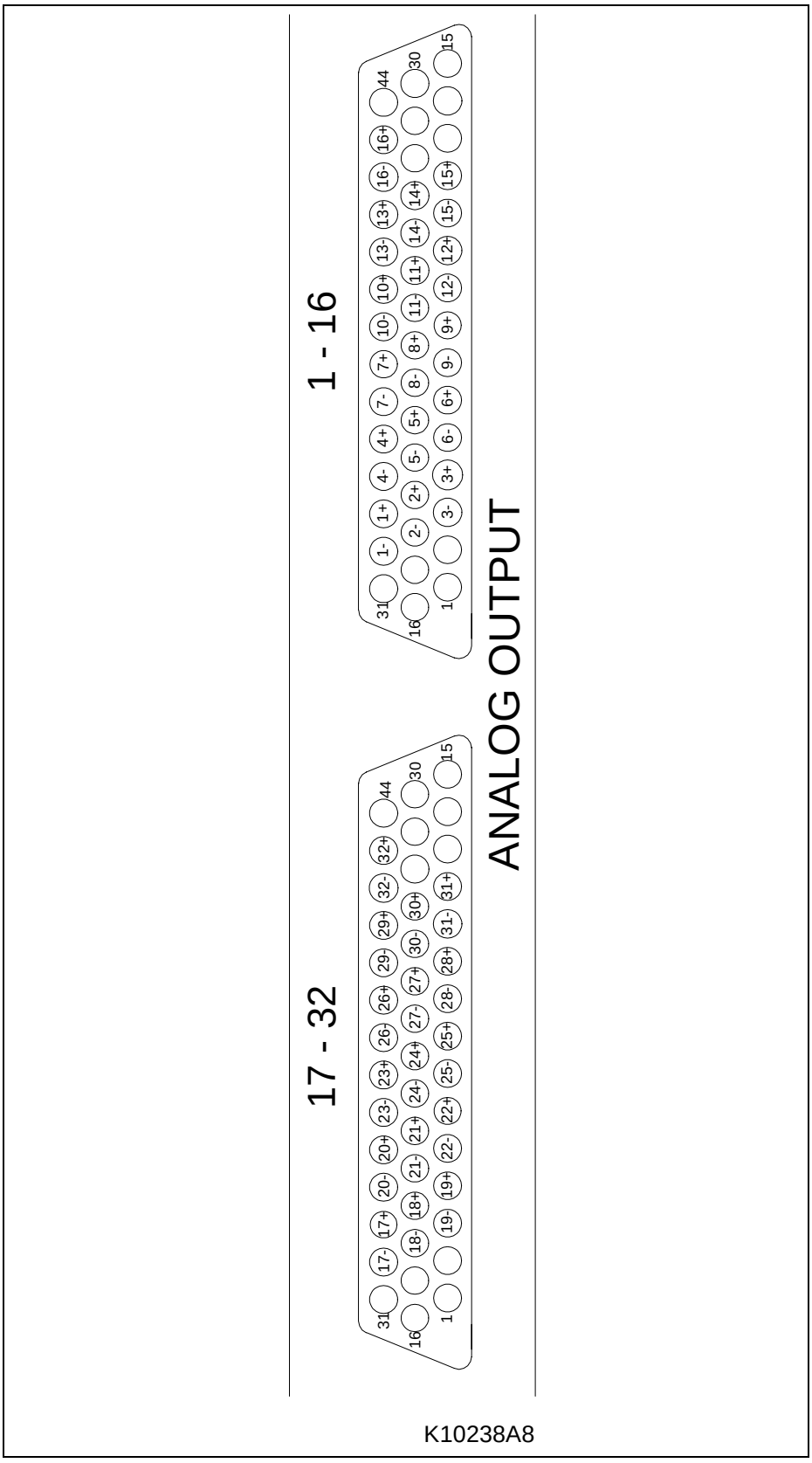


Figure 14 - Analog Connector Pinout

6.4 P4 Local Bus Connector Details

Suitable mating connectors are available from a number of manufacturers. The one listed is an example only.

Connector on board: 501-2007ES
Mating connector: 622-2001 (Non-polarized)
622-2041 (Polarized)
Manufacturer: Thomas & Betts, (803)676-2900

Pin No.	Signal Name	Description
1	XTI+	Positive signal of the differential 256xFs clock. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
2	XTI-	Negative signal of the differential 256xFs clock. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
3	TRIG+	Positive signal of the differential trigger. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
4	TRIG-	Negative signal of the differential trigger. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
5	n/c	Reserved
6	GND	Digital Ground
7	n/c	Reserved
8	n/c	Reserved
9	GND	Digital Ground
10	EXTCLK	External Clock - The user drives this TTL signal to supply an external sampling rate or 256x oversampling clock. In multiple board systems, only the sampling master receives the external clock signal.
11	EXTTRIG	External Trigger - The user drives this TTL signal to supply an external trigger. In multiple board systems, only the sampling master receives the external trigger signal.
12	GND	Digital Ground
13	FSYNC	Fast Sync - This signal is used by the ICS-115 to keep all slaves in phase with respect to the 256x oversampling clock and decimation. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
14	GND	Digital Ground
15	VSYNC	VME/VSB Sync - This signal is used to distribute the VME/VSB Frame signal to the slaves. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
16	GND	Digital Ground
17	DSYNC	Swing Buffer Sync - This signal is used by the ICS-115 to keep the swing buffers on all slaves in sync. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
18	GND	Digital Ground
19	n/c	Reserved
20	GND	Digital Ground

6.5 P3 FPDP Details

Connector on board:	8831E-080-170L (KEL Corporation) P50E-080P1-SR1-TG (Robinson-Nugent)
Mating connector:	8825E-080-175 KEL (with strain relief) 8825R-080-175 KEL (without strain relief) P25E-080S-TG Robinson-Nugent
Manufacturers:	KEL Corporation, (408)720-9044 Robinson-Nugent, (812)945-0211

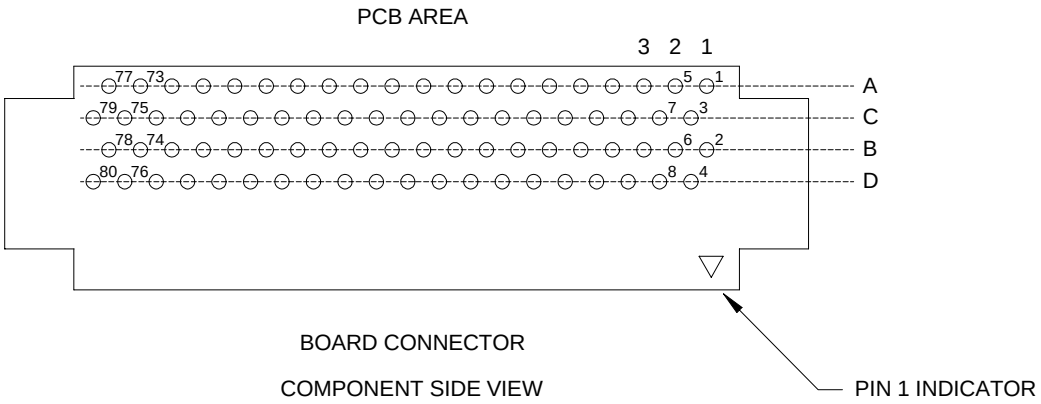
Note 1: The pinout list given in Table 6.3 below corresponds to the wire numbers on the ribbon cable, starting from the connector pin 1 index mark (see Figure 14). Previous ICS documentation referred to the board connector row and column numbers. These are also shown in the Figure to allow cross-reference.

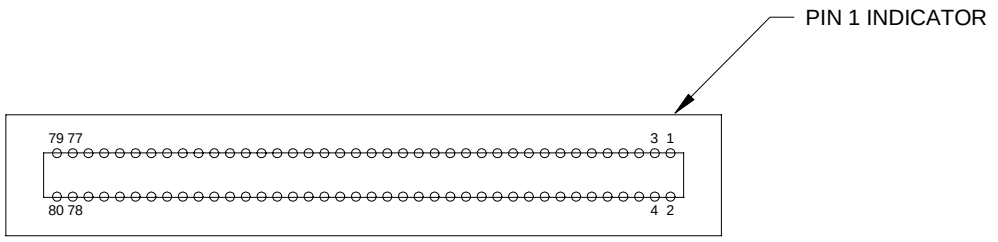
Note 2: When connecting one or more ICS-115A boards to a DSP board, the user should be aware that some DSP implementations have the FPDP connector inverted. For the ICS-115A, the connector index mark appears at the bottom right hand side of the connector when the board is mounted vertically in a chassis. In order to prevent the need to fold the FPDP ribbon cable when connecting to the DSP board, the cable is supplied with the connector at one end inverted. The pinouts at the DSP FPDP connector are therefore reversed, compared to the ones given below. In other words, at the DSP connector pin 1 connects to pin 80 at the ICS-115A, while pin 2 connects to pin 79 at the ICS-115A.

The FPDP is a high performance 32 bit parallel interface configured with a ribbon cable to connect boards or systems together. The simple and well-defined physical and electrical interface provides the basis for integrating many different types of boards and sub-systems. The maximum clock rate of the ICS-115A FPDP interface is 20 MHz, providing a sustained data rate of up to 80 MBytes/s. Since multiple FPDP buses are possible, the total data path bus bandwidth may be scaled to system requirements.

6.5.1 FPDP Connector Pin Assignments

The FPDP interface connector is an 80-pin high-density connector available from KEL and Robinson-Nugent. The connector on the board is a KEL 8831E-080-170L or R-N P50E-080P1-SR1-TG and is shown in Figure 14. The mating cable connector is a KEL 8825E-080-175S or R-N P25E-080S-TG, and takes a single ribbon cable of 80 conductors on 0.025 inch pitch. Table 6.3 defines the connector pin assignments.





Connector row and column designations are shown outside connector outline.

Cable numbers are shown inside connector outline.

FPDP BOARD-MOUNTED CONNECTOR
KEL 8831E-080-170L
or
Robinson-Nugent P50E-080P1-SR1-TG

K10128B2

Figure 15 - FPDP Board Connector

TABLE 6.3 ICS-115 FPDP P3 connector pin assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	2	STROBE	3	GND	4	GND
5	GND	6	GND	7	NRDY*	8	GND
9	DIR*	10	GND	11	RESERVED	12	GND
13	SUSPEND*	14	GND	15	GND	16	GND
17	PIO2	18	GND	19	PIO1	20	GND
21	RESERVED	22	GND	23	RESERVED	24	GND
25	PSTROBE	26	GND	27	PSTROBE*	28	GND
29	SYNC*	30	GND	31	DVALID*	32	GND
33	D31	34	D30	35	GND	36	D29
37	D28	38	GND	39	D27	40	D26
41	GND	42	D25	43	D24	44	GND
45	D23	46	D22	47	GND	48	D21
49	D20	50	GND	51	D19	52	D18
53	GND	54	D17	55	D16	56	GND
57	D15	58	D14	59	GND	60	D13
61	D12	62	GND	63	D11	64	D10
65	GND	66	D09	67	D08	68	GND
69	D07	70	D06	71	GND	72	D05
73	D04	74	GND	75	D03	76	D02
77	GND	78	D01	79	D00	80	GND

6.5.2 FPDP Signals

A description of FPDP signals is given in Table 6.4.

TABLE 6.4 ICS-115 FPDP Signal Descriptions

Signal/s	Signal Name	Description
D31:00	Data Bus	32 bit data bus driven by the data source.
DIR*	Data Direction	The data source asserts DIR* low.
DVALID*	Data Valid	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each data sample.
STROB	Data Strobe	STROB is a free running clock supplied by the data source. The receiving end should clock the data with the rising edge of STROB.
NRDY*	Not Ready	NRDY* is asserted by the receiver when it is not ready to receive data. The data source must sample this signal until the receiver brings it high, at which time the transfer can commence. Since NRDY* is asynchronous to STROB, the data source should double-synchronize to it before sampling its state; this avoid metastability problems.
PIO1,PIO2	Prog. I/O	The PIO signals are programmable I/O lines for user-defined functions. They can be configured as inputs or outputs.
PSTROBE	+ PECL Data Strobe	This signal along with PSTROBE* are generated by the data source as an optional differential PECL (Positive Emitter-Coupled Logic) data strobe. PSTROBE is the positive version of the differential clock and has the same polarity as STROB. For high data rate applications, the differential PECL data strobe should be used instead of STROB. The user must configure the board appropriately; see section 4.2.
PSTROBE*	- PECL Data Strobe	This signal is the negative version of the differential PECL data strobe.
RESERVED		Do not connect to reserved signals.
SUSPEND*	Suspend Data	SUSPEND* is generated by the receiver to inform the data source of a pending FIFO overflow condition. The data source is allowed as many as 16 cycles before suspending the transfer. Since SUSPEND* is asynchronous to STROB, the data source should be double-synchronized to it before sampling its state; this avoids metastability problems.
SYNC*	Sync Pulse	The data source can provide a sync pulse to the receiver to synchronize data transfers. The receiver waits for the sync pulse before accepting data. The receiver starts accepting data on the first Data Valid period following the sync pulse.

6.5.3 FPDP Electrical Characteristics

Table 6.5 lists the recommended driver, receiver and termination components for each signal.

TABLE 6.5 FPDP Driver, Receiver and Termination Components

SIGNAL	TRANSMITTER	RECEIVER	TERMINATION
All data	IDT 74FCT16952	IDT 74FCT16952	27 Ohm series
STROB	IDT 49FCT806A	IDT 49FCT806A	220/330 Ohm Thevenin
DVALID*, SYNC*	IDT 74FCT16245	IDT 74FCT16952	27 Ohm series
PSTROBE, PSTROBE*	Motorola MC10ELT28D	Motorola MC10ELT28D	Driver: 390 Ohm to ground on both connections. Receiver: 110 Ohm across + and -.
PIO1, PIO2	IDT 74FCT16245	IDT 74FCT16245	27 Ohm series
SUSPEND*, DIR*, NRDY*	Signetics 74F3038 Open collector	Signetics 74F3038	220/330 Ohm Thevenin

6.5.4 FPDP Timing

Figures 15 & 16 show timing diagrams for the FPDP interface. Either STROB or [PSTROBE, PSTROBE*] can be used to clock in the data. STROB is a free running clock conforming to TTL specifications and [PSTROBE, PSTROBE*] is a differential PECL (Positive Emitter-Coupled Logic) version of the same clock. Users are advised that it is preferable to use the PECL clock, particularly when operating at higher clock speeds, since it provides improved noise margins compared with the TTL clock. However, the user should confirm that the FPDP Transmitter device supports the PECL Strobe signals before deciding to use it. The user must configure the board so that the DAC uses either STROB or the PSTROBE pair; this is done using an on board switch (see section 4 of this manual). The DVALID* signal is asserted low when valid data is transmitted. The SYNC* signal is used to synchronize the data. This signal is asserted by the data source coincident with the last channel of every frame.

Table 6.6 lists the FPDP timing specifications. Any device using the FPDP must meet these requirements in order to guarantee correct operation.

TABLE 6.6 FPDP Timing Specifications

	Description	FPDP Specification
1	STROB period	50 ns min.
2	STROB low	22 ns min.
3	STROB high	22 ns min.
4	DATA, DVALID* & SYNC* setup to STROB	10 ns min.
5	DATA, DVALID* & SYNC* hold from STROB	10 ns min.
6	SUSPEND* to DVALID* deasserted	16 STROB max.
7	SUSPEND* deasserted to DVALID* re-asserted	1 STROB min.

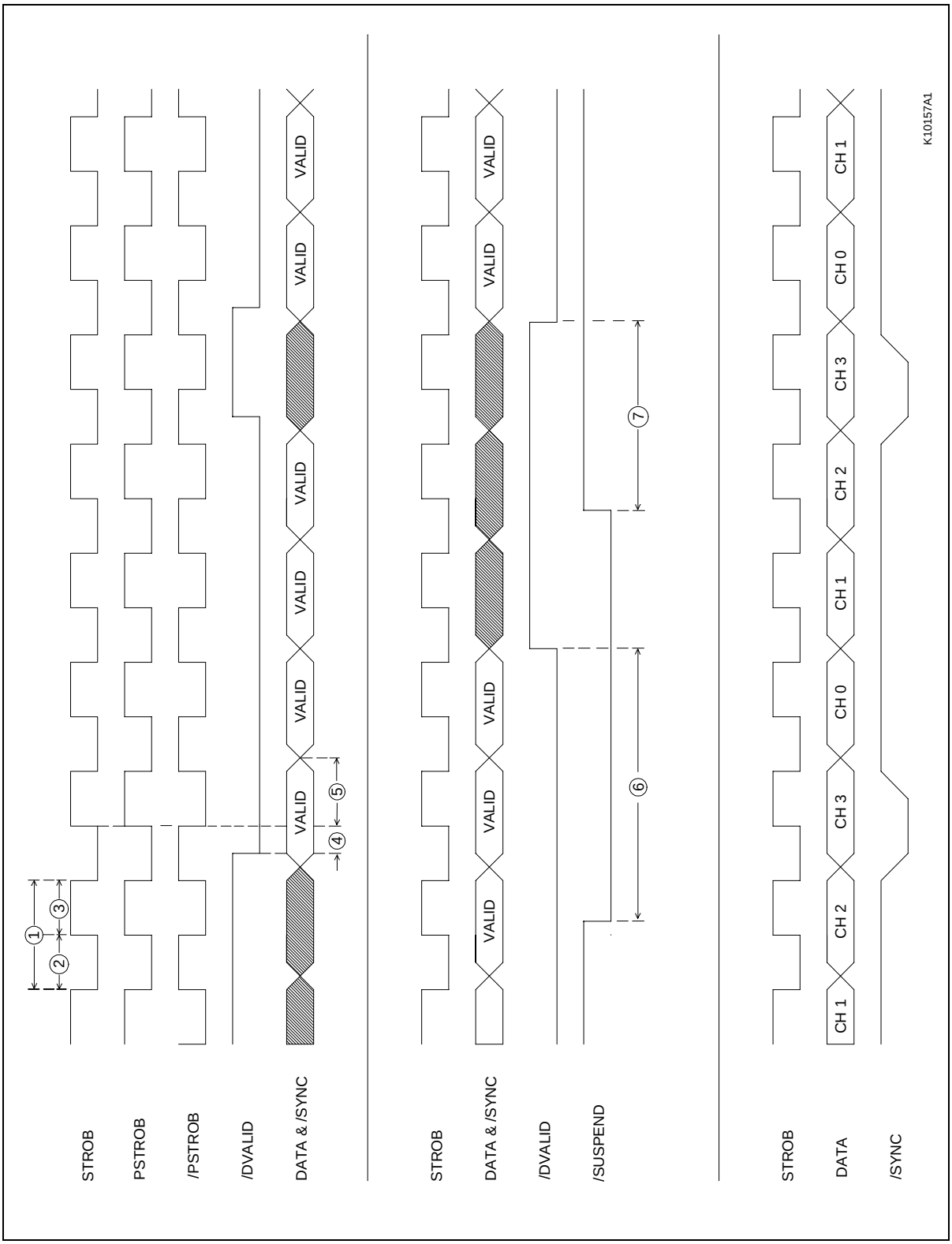


Figure 16 - FPDP Interface Timing

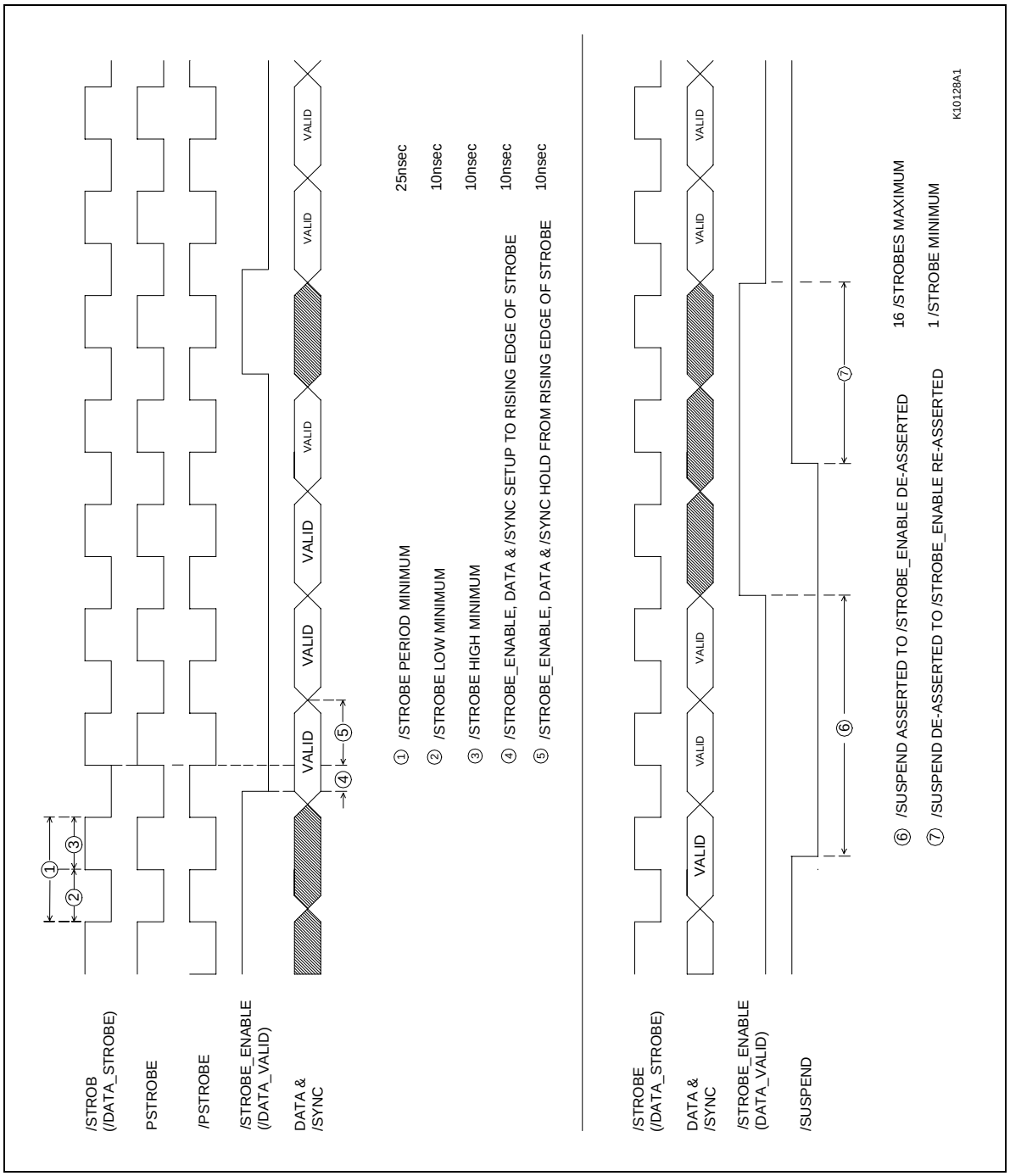


Figure 17 - FPDP I/O Timing

