ICS-110BL

OPERATING MANUAL

Interactive Circuits And Systems Ltd.
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Extra copies of this manual are available from the factory.

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1. INTRODUCTION

The ICS-110BL VMEbus analog input board is functionally similar to the earlier ICS-110B product, but has reduced power consumption. Note that the ICS-110B and ICS-110BL products should not be mixed in a single acquisition cluster, since there may be minor differences in the timing of the sampling instant between the two board types. The ICS-110BL is designed to simplify complex data acquisition requirements by offering:

- a large number of channels (4 to 32);
- Sigma-Delta ADCs which virtually eliminate complex and expensive anti-alias filtering;
- optional signal conditioning daughter card with programmable gain of up to 31.5dB, fixed frequency 2-pole anti-alias filters and calibration/test signal generation;
- simultaneous sampling at rates from 125 Hz/channel to 108 kHz/channel;
- 24-bit and 16-bit resolution output options;
- 110 dB dynamic range and -105 dB interchannel crosstalk;
- front panel signals for synchronizing up to 32 ICS-110BL boards;
- external or programmable internal clock;
- 128 KByte on-board storage;
- 32-bit VMEbus and VSB interfaces which support block transfers;
- a 32-bit Front-Panel Data Port (ANSI/VITA 17 FPDP) for direct input to Mercury, SKY, Ixthos, Spectrum, Transtech DSP, and other array processors and DSP boards, as well as other ICS products;
- the ability to bus the FPDP outputs from multiple ICS-110BL boards into one composite data stream.

1.1 References

1. VMEbus Specification, ANSI/IEEE 1014-1987.

2. ICS-110B VxWorks Device Driver Manual, Document No. E10535, Interactive Circuits and Systems Ltd.

3. AK5393 Product Information, M0038-E-01/00, Asahi Kasei Microsystems Co. Ltd., www.akm.com.

2. GENERAL DESCRIPTION

Figure 1 shows a simplified block diagram of the ICS-110BL motherboard. The board includes up to 32 separate 24-bit Sigma-Delta ADCs to simultaneously digitize all channels at rates up to 108 kHz per channel. All inputs are differential in order to suppress common-mode noise. Full scale input voltage is ±1.0V on each wire of the differential pair for the standard product, and ±5.0V on each wire for the ICS-110BL-32B version. The latter version is not available with the optional signal conditioning daughter card. The serial output from each ADC is converted to a 24-bit parallel word before being stored in a FIFO for subsequent read-out. A separate FIFO is included for odd and even channels. Data is acquired in frames, where a frame contains one sample from each selected channel at a single sampling instant. Any number of channels (multiples of 2 only) up to the maximum for the board may be selected for operation, but the channels are always allocated in ascending order starting at channel one.

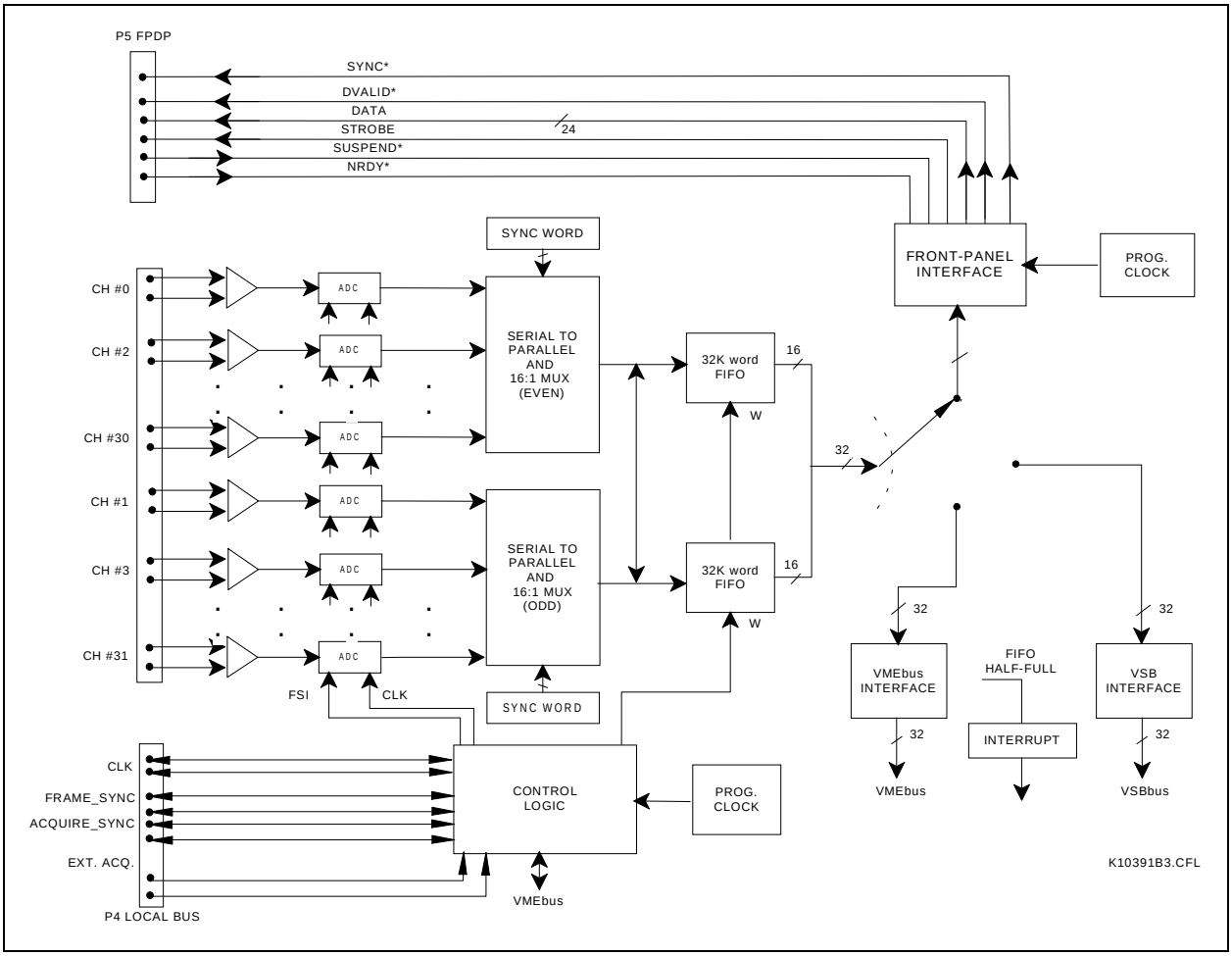


Figure 1 - ICS-110BL Motherboard Block Diagram

At the output, 24-bit samples are presented in the most significant 24 bits of each 32-bit data word. If preferred, the 24-bit data may be truncated to 16-bits for output over the VMEbus or VSB (not FPDP). In this case, data from consecutive odd and even channels is combined to form a 32-bit word in order to make the most efficient use of bus bandwidth. Both the VMEbus and VSB interfaces support block transfers. A VMEbus or VSB interrupt at FIFO Half-Full can be generated to facilitate real-time operation.

The sampling clock for the ICS-110BL board can be either an external clock or the board's programmable frequency internal clock. The clock frequency must be 256 times the output data rate for each channel when using 64x oversampling, and 512 times the output data rate when using 128x oversampling. The output data rate is equivalent to the sampling rate in conventional ADCs. The input signal is sampled at one quarter the clock rate, which is typically more than 128 times the input signal bandwidth. This high sampling rate virtually eliminates the need for anti-aliasing. Each Sigma-Delta ADC uses internal digital filtering and decimation to produce an output at the desired sampling rate. The output data rate can be further reduced using a programmable on-board decimation register. However, care must be taken to ensure that the input signal is properly anti-aliased before decimating the ADC output.

The internal sampling clock of the ICS-110BL can produce a user-specified sampling rate to within 20Hz at the output rate. The clock is programmed by writing the appropriate clock frequency program word to the board's PROGRAM_CLOCK register. Software is included with the software device driver for the board to simplify computation of this programming word.

Data acquisition can be triggered using either an external signal or by software control. The trigger functions as a gate, allowing acquisition to be repetitively enabled and disabled using the selected trigger source. When using the external trigger, the signal is applied to the differential EXT_ACQ input and must conform to differential TTL signal levels. Acquisition starts when the signal changes from the low state to the high state, and stops when it returns to the low state. Acquisition is automatically synchronized so that a full frame of data is always written to the FIFO memory at the beginning and end of an acquisition cycle.

Up to 32 ICS-110BL boards may be configured as a cluster to provide simultaneous sampling with excellent synchronization. When operating in this configuration, one board must be configured as Sampling Master, while the remainder are configured as Slaves. This board generates the sampling clock and trigger (external or internal) and feeds them to all other boards in the cluster. The signals required to provide this functionality are routed on the front panel P4 Local Bus connector. When using multiple board configurations, the P5 Front Panel Data Port (FPDP) can operate in a multiplexed fashion so that a composite data frame is generated on FPDP containing data from all channels in the cluster. The control signals required to generate composite FPDP frames with the correct timing are also included on the front panel P4 Local Bus interface.

The optional daughter card included with the ICS-110B1L product provides up to 32 channels of signal conditioning with test and calibration capability. Figure 2 gives a block diagram showing a single channel of the daughter card. When the daughter card is installed, the differential signals at the front panel analog input connectors are routed to the daughter card; the motherboard must be modified to allow this. Here they are buffered and converted to single ended signals. After passing through a relay that selects either analog input or the test/calibration signal, the signals pass through a two-pole anti-alias filter with a Butterworth characteristic. The cut-off frequency of this filter is fixed and must be specified at time of ordering. The filter outputs are applied to a programmable gain stage which provides between -95.0dB to +31.5dB of gain; separate values may be programmed to each channel. After the gain stage, the signals connect to the motherboard, where they are applied to the input buffers as when no daughter board is present.

The test/calibration relays allow one of two signal sources to be applied to all input channels. The first is an external calibration signal taken from one of the front panel analog input connectors; the second is a single waveform from one of eight which may be stored in a one-time programmable Programmable Read-Only Memory (PROM) which is located on the daughter card. The selection of which stored waveform is to be used is programmable.

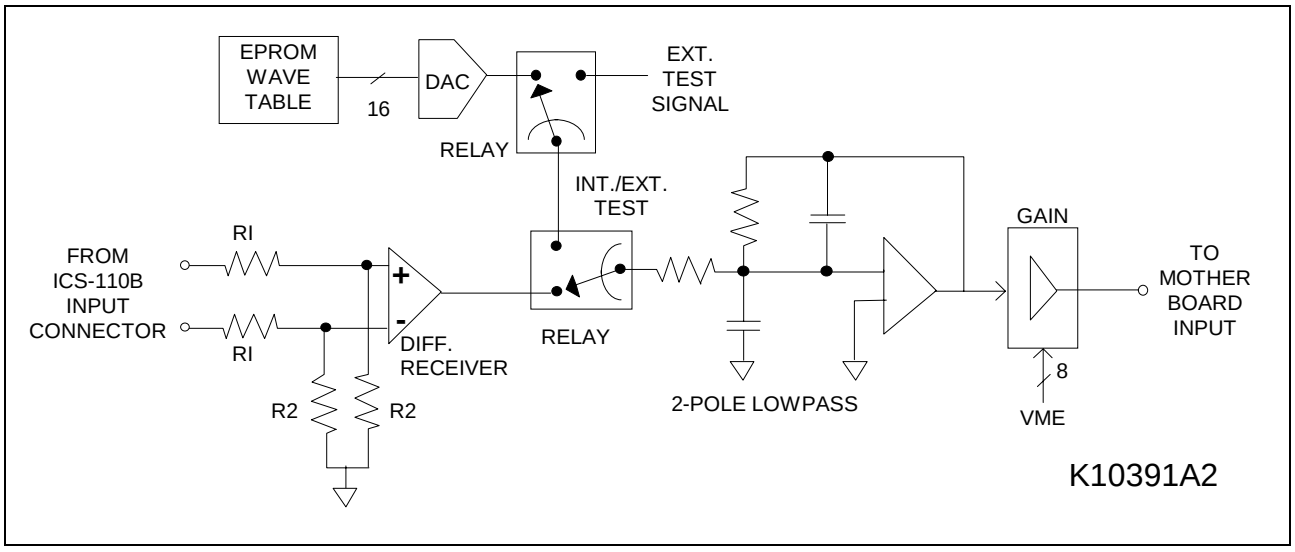


Figure 2 - ICS-110BL Daughter Board Block Diagram (One Channel)

2.1 Specifications

ICS-110BL Motherboard

Number Of Differential Analog Inputs :	4, 8, 16 or 32
Input Impedance :	10 kOhm
Full Scale Input :	±1.0 V differential* (standard product) ±5.0 V differential* (ICS-110BL-32B product)
Maximum Input Signal Bandwidth (-0.003dB):	45.35 kHz
Input Sampling Rate:	128 x Output rate for BW < 22kHz 64 x Output rate for BW > 22kHz
Output Rate (effective sampling rate) :	Max. 108 kHz/ch. Min. 1 kHz/ch.
Programmable Decimation Factor :	1 to 16
Internal Sample Clock :	Programmable in steps of 20Hz (at output freq.)
Dynamic Range:	> 110dB in 128x sampling mode > 105dB in 64x sampling mode
Total Harmonic Distortion:	< -105dB
Crosstalk:	< -105dB
On-board Storage:	64 Kwords
Output Word Length:	32 bits packed (2 samples per word) (VME and VSB only) 24 bits (1 sample per word) (VME,VSB and FPDP)
VMEbus Interface:	A32/24/16 D32 BLT Slave, Vectored Interrupts 32 MBytes/sec
VSBbus Interface :	A32 D32 BLT Slave, Polled Interrupts 40 MBytes/sec
FPDP Support :	ANSI/VITA 17 Front Panel Data Port Repeating Frame Data mode Up to 20 MWords/sec burst
Power :	+5 volts 4.05 Amps maximum +12 volts 0.5 Amps maximum -12 volts 0.24 Amps maximum
Operating Temperature :	0 to +50 Deg. C
Storage Temperature :	-40 to +85 Deg. C
Humidity :	95% RH, non-condensing
Board Size :	233 x 160 mm, VMEbus 6U standard

ICS-110BL Daughter Board (Optional)

Number Of Differential Analog Inputs :	4, 8, 16 or 32
Input Impedance :	>1 Mohm (±5V max. input) >100 kohm (±25V max. input)
Maximum Input Level :	±1.87 V differential* standard Contact factory for other options
Lowpass filter :	2-pole Butterworth, Fc=75kHz, giving a flat response up to 45kHz
Gain :	-95.0 dB to +31.5 dB in steps of 0.5 dB
Internal Test Signal :	Eight 16-bit preprogrammed waveforms in a 256K x 16-bit PROM
Dynamic Range :	> 85 dB @ 0 dB gain and ±1.0 V diff. input
Power :	+5 volts 0.5 Amps maximum +12 volts 0.26 Amps maximum -12 volts 0.17 Amps maximum

* i.e. voltage in each differential input leg.

Specifications subject to change without notice

3. DETAILED DESCRIPTION

3.1 Sigma-Delta Analog Conversion

The operation of a Sigma-Delta ADC differs significantly from traditional ADCs. A 1-bit analog-to-digital conversion is performed at a very high rate. The total quantization noise energy remains constant, but by spreading it over a wider spectrum, the amount in the frequency band of interest is reduced. The noise in the passband is further reduced by filtering (noise shaping). The oversampled signal is then lowpass filtered to remove the out-of-band quantization noise. This is achieved using a decimation comb filter and an FIR low-pass filter/decimator. The resultant output spectrum is equivalent to a traditional ADC.

For more information on Sigma-Delta analog-to-digital conversion techniques, refer to IEEE press publication "Oversampling Sigma-Delta Data Converters" edited by James C. Candy and Gabor C. Temes.

3.2 Anti-Alias Filtering

The ICS-110BL board uses the Asahi Kasei Microsystems (AKM) AK5393 Sigma-Delta converter. This device is designed to sample the input signal at a rate which is greater than 128 times the signal bandwidth, when an output rate of up to 54kHz is required. A 64x oversampling mode is also provided for output rates up to 108kHz. For 24-bit conversion accuracy, the anti-alias prefilter must provide 110 dB attenuation at the Nyquist frequency.

Since the Nyquist frequency is at least six (6) octaves away from the highest signal frequency, no more than a 3-pole filter is required for anti-aliasing. The input differential amplifiers buffering the analog inputs on the ICS-110BL board, however, have a finite bandwidth. Further, the input signal strength reduces naturally beyond the passband of interest in many applications. A simple single or double pole filter may therefore be sufficient for anti-aliasing. Note that no anti-aliasing is provided on the ICS-110BL motherboard, but a two-pole Butterworth filter is provided on the optional signal conditioning daughter card (see section 3.15).

The Sigma-Delta ADC limits the signal bandwidth to approximately 40% of the output data rate by digital filtering. The minimum output rate is 1 kHz. However, lower output rates can be achieved by using the on-board decimation feature. In this case, care must be taken to ensure that the input signal is bandlimited to less than half the final output rate in order to avoid aliasing.

3.3 Input Section

The ICS-110BL board accepts true differential input signals with peak amplitudes of ±1.0V differential, as shown in Figure 3. The input impedance is 10 kOhm. The maximum input signal bandwidth is approximately 45 kHz.

For best performance, differential input signals are recommended. If, however, a single-ended input must be used, the -ve input terminals can be tied together to a common analog ground, preferably the ground of the source. The input signal is applied to the +ve terminal. The full-scale swing of the input signal should not exceed ±1.0V. Thus, for single-ended inputs, there is a 6dB loss in dynamic range.

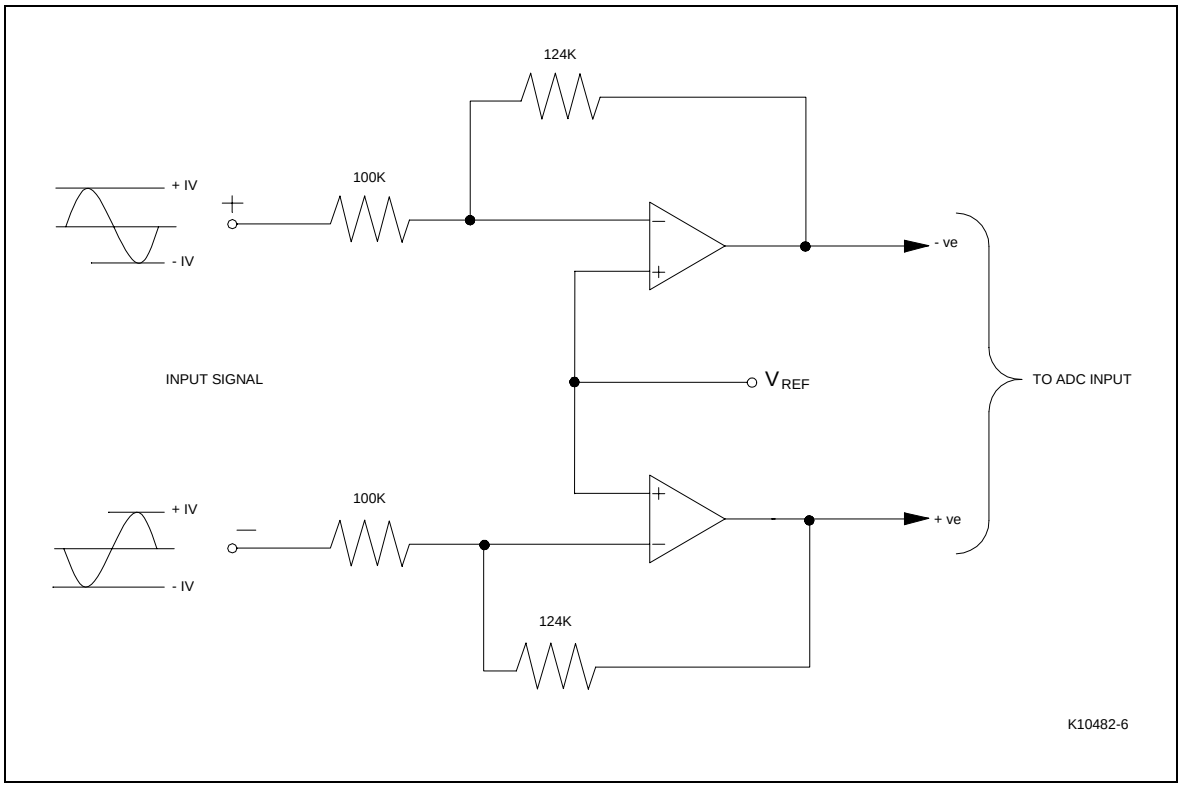


Figure 3 - ICS-110BL (Motherboard) Analog Input Configuration

3.4 Dynamic Range

The ICS-110BL offers over 110 dB dynamic range in the 128x oversampling mode of operation, which provides a maximum input signal bandwidth of approximately 22kHz. The dynamic range is over 105 dB in the 64x oversampling mode of operation, which provides a maximum input signal bandwidth of approximately 45kHz.

The ICS-110BL offers excellent gain and phase matching across channels. Since the Sigma-Delta converters employ minimal analog technologies, such performance is expected. In the design of the ICS-110BL board, extreme care has been taken in the generation of sampling clocks in order to assure precise simultaneous sampling on every card, and across cards in a multiple board system.

The frequency response is flat over the entire signal bandwidth (approximately 45% of the output rate) to within ±0.003 dB.

3.5 Sampling Clock

The ICS-110BL board can be configured (by programming the control register) to use either the internal programmable-frequency sampling clock or an external clock. If used, the external sampling clock signal should conform to differential TTL signal levels and applied to the EXT_CLK pins on the front panel P4 connector. A single-ended TTL clock signal can also be applied provided that the high level of the signal is above 3.5 volts. The frequency of the external clock signal must be 256 times the desired output rate when operating in 64x oversampling mode, or 512 times the desired output rate when operating in 128x oversampling mode.

The internal clock (after conversion to differential TTL signals) is available at the P4 Local Bus connector pins in order to supply clock signals to other ICS-110BL boards for synchronous operation. The board generating the clock signal (the Sampling Master) requires appropriate jumper settings in order to route the clock signals back from the P4 connector pins. All Sampling Slave ICS-110BL boards must be configured for external clock. Thus all boards including the master see identical propagation delays for the clock signal, regardless of whether it is generated by a ICS-110BL board or applied from an external source.

The maximum clock frequency is approxaimtely 27.65 MHz and the minimum clock frequency is 391 kHz.

3.6 Output Decimation

The output rate can be reduced using the on-board decimation feature. At the output, samples are automatically discarded, which has the effect of lowering the effective sampling rate. The maximum decimation factor that may be programmed is 16.

The user is cautioned that decimating the output requires anti-aliasing (similar to using a conventional ADC) in order to bandlimit the input signal to Nyquist frequency that is equal to half the final output rate. Thus, output decimation is only recommended for reducing the output rate below 1 kHz.

3.7 Clock vs Channel Output Rate Relationship

The channel output rate is directly related to the frequency of the internal programmable or external clock signal frequency as follows:

Channel Output Rate = Fs / (R x DF)

where Fs is the clock frequency and DF is the decimation factor (see section 3.6). R is a ratio equal to 512 when the oversampling ratio is 128, and equal to 256 when the oversampling ratio is 64.

Thus, for a 25.6 MHz clock, using 64x oversampling and assuming no output decimation, the channel output rate is:

Channel Output Rate = 25,600,000 / (256 x 1)
= 100 kHz.

For a 25.6 MHz clock, using 128x oversampling and assuming no output decimation, the channel output rate is:

Channel Output Rate = 25,600,000 / (512 x 1)
= 50 kHz.

For a minimum clock frequency of approximately 512kHz, using 128x oversampling and assuming no output decimation, the channel output rate is:

Channel Output rate = 512,000 / (512 x 1)
= 1.0 kHz.

3.8 External Trigger

Triggering of acquisition can be either internally controlled from the VMEbus by writing to the Control register, or externally controlled via the P4 EXT_ACQ input. In either case, the effect is to start and stop acquisition by enabling and inhibiting writes to the board's FIFO memory. The trigger acts as a gate. Acquisition occurs only when the signal or enable bit is high, and it may be repetitively started and stopped using this mechanism. The operation is data-frame oriented; acquisition can only be started at the beginning of a frame or stopped at the end of a frame. A frame includes all channel data corresponding to a given sample period. Note that the ADCs are never stopped - they are always operating.

The differential P4 EXT_ACQ input is used to start and stop acquisition externally. A TTL high level enables acquisition. A single-ended TTL signal can be used provided the high level is not less than 3.5 volts.

3.9 Front Panel Interface

The ANSI/VITA 17 Front Panel Data Port (FPDP) is a synchronous parallel data transfer bus which uses ribbon cable. It is ideally suited to the requirements of high speed real-time data transfer. Since only one bus master is allowed and there is no addressing on the bus, the maximum possible bandwidth is available for data transfer. FPDP provides a simple and inexpensive mechanism for off-loading data from VMEbus.

The FPDP protocol for data transfer is supported by all ICS current products. An 80-pin ribbon cable connector is provided for the FPDP (see Appendix section 7.6).

The ICS-110BL, since it provides 24-bit resolution, drives data only on data lines D31 (Most Significant bit) through D08 (Least Significant bit), inclusive. The undriven least significant 8 bits of the 32-bit bus are tied to ground.

The FPDP burst rate (Data Strobe frequency) is software programmable to up to 20 MHz. In addition to the Data Strobe signal, positive-logic ECL differential clocks (+PECL Strobe & -PECL Strobe) are also supplied in order to support longer cable lengths, high speed operation, and greater immunity from clock-related problems.

The Front Panel Data Port interface operates using two FIFO memories in a swing buffer configuration, as shown in Figure 1. During one frame, data is converted and written to one FIFO memory, while the FPDP interface reads data from the other and transmits it over the FPDP cable. At the end of the frame, the two banks switch. Before any new ADC data is written to the swapped FIFO memory, it is automatically reset to ensure channel synchronization. If the synchronization is somehow lost, this scheme ensures that the synchronization is recovered in the next frame.

By programming the FPDP_BLOCK_COUNT register, the user can set the bank switch to occur after storing a specified number of frames.

3.10 FPDP Timing Limits

When using the FPDP in a multiple board configuration, it must be noted that the maximum FPDP data rate is 20 MHz. The value programmed for the FPDP Data Strobe frequency using the CLOCK_FREQUENCY register should not exceed this value (see sections 5.16 and 7.1). The user must ensure that whatever FPDP Data Strobe frequency is programmed is sufficient to provide the data throughput required by the selected sampling frequency. The minimum required data strobe rate is simply the sample output frequency multiplied by the number of channels programmed for the system (example, for all ICS-110BL boards connected on the same FPDP). This channel count is programmed in the NUM_CHANNELS_FPDP register.

At a channel output rate of 100 kHz, approximately 200 channels can be used (100 kHz x 200 = 20 MHz). Note that the decimation factor must be taken into account, if decimation is used. Approximately 800 channels can be used when the channel output rate is 25 kHz or less (25 kHz x 800 = 20MHz).

Where the user's requirement would exceed the maximum transfer rate of FPDP, it is possible to set up multiple board configurations with multiple FPDP outputs. This is possible because the Sampling Master and FPDP Master functions of the ICS-110BL are separate. By configuring a system with a single Sampling Master and multiple FPDP masters, the cluster of ICS-110BL boards will all sample synchronously, but will output data on two or more FPDP cables. Details of board configuration are given in section 4.

3.11 VMEbus Interface

The ICS-110BL contains a Slave A32/D32 VMEbus interface. The VMEbus interface supports block transfers and vectored interrupts. Data transfer rates in excess of 32 MBytes/sec can be achieved. D16 path width must be used for access to most control registers, while D32 path width must be used for access to the ADC data and to some control registers.

Although data is always accessed using 32-bit data transfers, channel data can be organized as one channel per transfer (unpacked mode) or two channels per transfer (packed mode). In unpacked mode, the channel data is located in the upper 24 bits of the 32-bit data word (the lower 8 bits are forced to zero). In packed mode, the 24-bit samples are truncated to 16 bits and packed into 32-bits such that channel N is in the upper 16 bits, and channel N+1 is in the lower 16 bits of the 32-bit data word.

3.12 VSB Interface

The ICS-110BL also contains a Slave A32/D32 VSB interface. The VSB interface supports block transfers and polled interrupts. Data rates up to 40 MBytes/sec can be achieved. Data organization is as discussed in the VMEbus Interface section above.

At power up, the VSB interface is disabled and cannot be used until the VSB base address is programmed to the VSB Base Address register (see section 5.13).

3.13 Interrupts

When enabled, the ICS-110BL will generate interrupts when the data FIFO reaches the half-full state, thus relieving the user of the need to poll the status bit for this condition. The interrupt may be generated on VMEbus or VSB. Prior to using the interrupt mechanism on VMEbus, the interrupt vector must be loaded to the board's INTERRUPT_VECTOR register. To enable the interrupt, the appropriate enable bit in the VMEbus CONTROL register (CR:15 or CR:14) must be set. In the case of VSB interrupts, the VSB INTERRUPT_ENABLE location must be read, in addition to setting the enable bit in the Control register.

When an interrupt occurs, the user may transfer data using either conventional or block transfer cycles. To avoid the possibility of the data FIFO ever reaching the full state, the user should read as much data as possible when the interrupt occurs, but should be careful not to cause a FIFO empty state. If using conventional cycles, the FIFO_EMPTY bit of the STATUS register (SR:00) should be polled before each read to ensure that FIFO underflow does not occur.

If either the FIFO empty or FIFO full states occur, data has been lost and the board should be stopped, reset by writing to the BOARD_RESET register, and reconfigured before continuing.

3.14 Block Transfers

The ICS-110BL can act as a slave device for block transfers (D32 BLT cycles) on either VMEbus or VSB. If using block transfer cycles, the user should program the master device with a block size not exceeding half the FIFO length to ensure that FIFO underflow does not occur. The FIFO length is 64 KSamples. Because of the limit imposed by address map size, the maximum block size allowed for VMEbus transfers is 16,256 long words (0xFE00 = approx. 63KBytes). The maximum VSB block size is 8,192 long words (0x8000 = 32KBytes).

When addressing the ADC_DATA areas on either VMEbus or VSB memory maps, successive reads need not be to sequential addresses. Any access within the valid address range from the base address (see above) will read the next data value from the FIFO. It is valid to use the same address on every access, if desired.

3.15 Converter Programmable Features

The AK5393 converters used on the ICS-110BL provide several features which may be programmed by the user. Programming is done using the ADC Configuration register (see section 5.8). The most important of these are chip calibration and selection of the on-chip high pass filter.

3.15.1 Chip Calibration

Calibration of the converters should be done following power-up, and may be done at other times when it is acceptable to interrupt normal converter operation. It should not

be done until thermal equilibrium of the converter chips has occurred, at least 10 seconds after application of power.

Calibration may be done either using an internally-generated reference voltage (i.e. internal to the converter chips) or with the voltage present on the converter inputs. The selection of these alternatives may be made under software control (see below). If the user is concerned with the level of DC offset measured by the converter, it may be important to consider which of these options to use. If the analog inputs are held at zero volts when performing calibration with the external reference, the calibration procedure will effectively remove almost all of the offset due to the input buffers as well as that produced by the converters. However, if the user is not able to control the signal present at the board's analog inputs when doing calibration, it will be necessary to select the internal calibration reference. In this case, some residual DC offset due to the input buffers or signal conditioning circuits (ICS-110B1L product) will be seen.

The procedure for calibration of the ICS-110BL has been designed to be compatible with that used for the ICS-110B. Not all aspects of the ICS-110B calibration procedure are required for the ICS-110BL, but the ICS-110B procedure may be used unchanged on the ICS-110BL. The procedure for converter calibration on the ICS-110BL is as follows:

1. Write 0xC0 (internal calibration reference), or 0x80 (external calibration reference), to converter register 1.
2. Write 0x44 (64x OS) or 0xC4 (128x OS) to converter register 2.
3. Delay for a minimum of 1.275 seconds to allow calibration to complete.
4. Write 0x00 to register 1.

Follow the procedure given in section 5.8 for writing data to the converter registers. Following calibration, the on-chip high pass filters are enabled, but the user may disable them by using the procedure given in the next section.

3.15.2 Converter High Pass Filter

The AK5393 converter includes a first order high pass digital filter at the output, which may be used to remove DC offset. The filter is enabled following application of power, and following converter calibration (see section 3.15.1), but it may be disabled by the user, by programming the ADC Configuration register. The filter 3dB cut-off frequency is equal to fo/48000 Hz. In other words, it is 1.0 Hz when the output rate is 48kHz. The filter characteristics scale linearly with frequency.

The procedure for disabling the on-chip high pass filters is as follows:

1. Write 0x0C (64x OS) or 0x8C (128x OS) to converter register 2

The procedure for enabling the on-chip high pass filters is as follows:

1. Write 0x04 (64x OS) or 0x84 (128x OS) to converter register 2

Follow the procedure given in section 5.8 for writing data to the converter registers.

3.16 Signal Conditioning Daughter Card

The optional signal conditioning daughter board provides up to 32 channels of programmable gain, anti-alias filtering and test/calibration signal injection. Gain is individually programmable for each channel in the range -95.0 to +31.5 dB in steps of 0.5 dB. Gain changes may take up to 18 ms to be effected. The anti-alias filters are 2-pole filters with a Butterworth characteristic. The cut-off frequency of these filters is fixed, and must be specified at time of ordering. The standard frequency is 75kHz. Cut-off frequencies of 3.5kHz and 35kHz are also available on request at time of ordering.

When the daughter board is installed, signals connect to it from the front panel Analog Input connectors. Jumpers (wire links) must be correctly positioned on the motherboard to allow use of the daughter card. This may be done by the user (see section 4.8).

Test/calibration signal injection is available from a single external signal or from a digital generator on the daughter board. In either case, the same calibration signal is applied to all channels. The calibration function is enabled and the signal source selected by means of relays under program control. The external signal is a single-ended signal which must be connected to pin 16 or the Analog 1-16 connector. The full scale signal level is ±1V when the gain is set to be 0dB; however, since the daughter board drives the motherboard with a single-ended signal, this will achieve an output which is -6dB compared to full scale. This is the maximum signal level which may be applied to the converter.

The on-board signal generator consists of a one-time-programmable PROM memory located in a socket on the daughter card. The memory is divided into eight waveforms of 32K samples each; the waveform to be used can be selected under program control. When enabled, the samples of the selected waveform are repetitively output to a 16-bit Digital-to-Analog converter on the daughter card, providing a continuous periodic waveform. As shipped, the PROM contains 4 pre-stored waveforms; the user may remove the PROM from the board and program the remaining positions, if suitable tools and equipment are available. The PROM part number is HN27C4096CC-10 in a 44-pin PLCC package, available from Hitachi, Mitsubishi, AMD and others. Each waveform contains 32,768 16-bit samples. The waveform details are as follows - waveforms are numbered such that waveform 1 occupies the lowest address range:

Waveform No.	Description	No. of Cycles	Amplitude (peak)
1	Sine	544	±0x4026
2	Negative DC level	-	0xFBF4
3	Positive DC level	-	0x040C
4	Ramp (sawtooth)	50	±0x7FFF
5-8	Unused		

When using a 10kHz output rate in 64x oversampling mode, the measured output frequency of waveform 1 is approximately 166 Hz. When used in 128x oversampling mode, the output frequency will be twice this figure.

A full scale 16-bit digital input to the DAC corresponds to a full scale 24-bit digital output from the ADCs. Since the signal generator produces 16-bit samples, the dynamic range of the ICS-110BL output when using the signal generator will correspond to 16-bit performance, about 87 dB.

4. HARDWARE PREPARATION

This section provides information necessary for hardware preparation of both single board and multiple board ICS-110BL systems. Figure 4 shows the position of jumper (wire link) blocks on the ICS-110BL motherboard. There are no switches or jumpers on the daughter board.

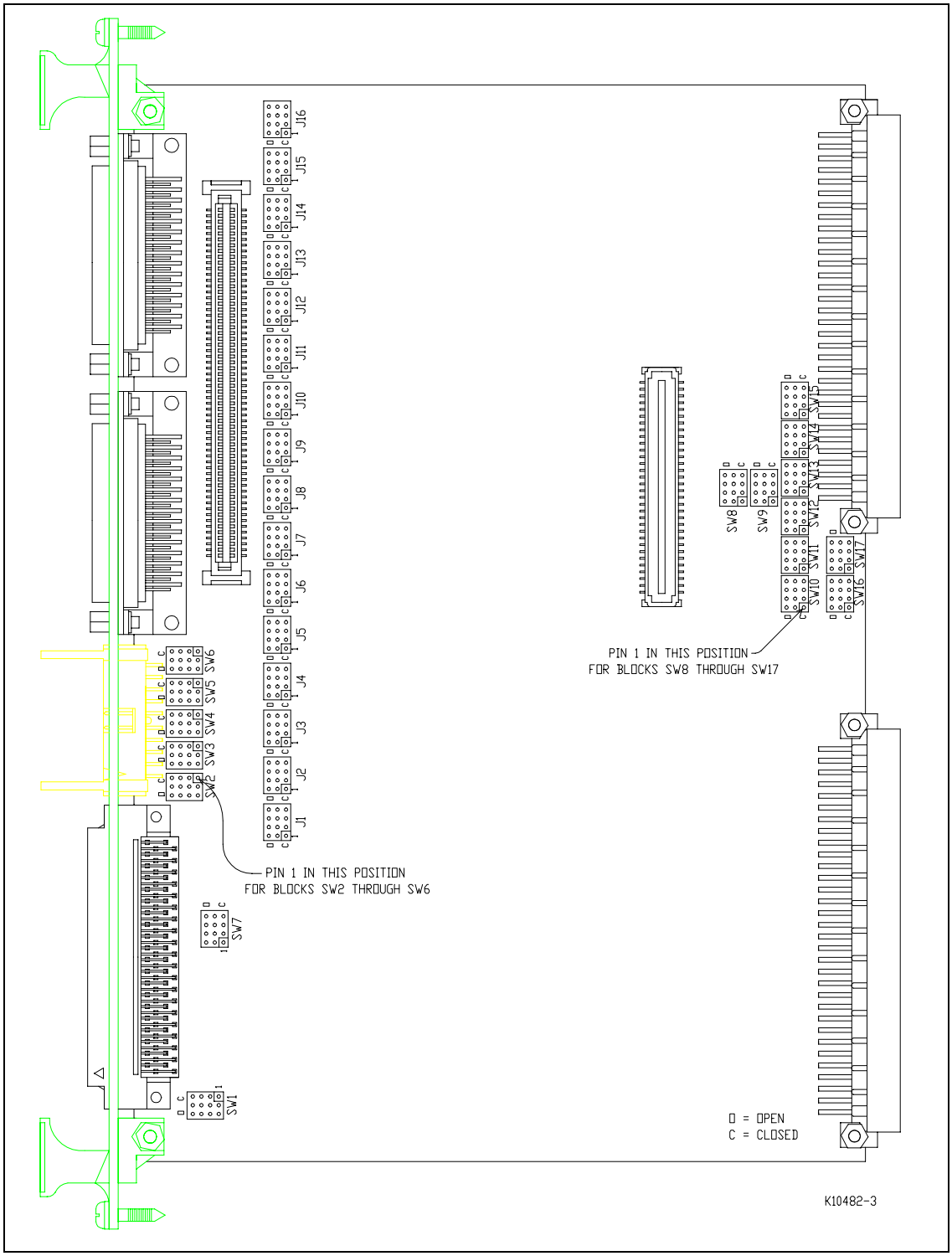


Figure 4 - ICS110BL Jumper Locations

4.1 System Configuration

The ICS-110BL is designed to allow simultaneous sampling across all channels on a board, and also across all channels on multiple boards. To facilitate multiple board clusters, timing and external clock/trigger signals are bussed on the front panel P4 Local Bus cable. In addition, if the Front Panel Data Port (FPDP) is used for data output, multiple ICS-110BL boards may be bussed on the same FPDP cable. The user is advised not to mix ICS-110B and ICS-110BL boards in the same cluster, since sample timing may vary somewhat between board types.

Two multiple board cluster configurations are possible:

- All ICS-110BL boards on one Local Bus cable and on one FPDP cable
- All ICS-110BL boards on one Local Bus cable, but on two or more FPDP cables

The latter case addresses the situation where a single FPDP cable would not have sufficient throughput, or where the FPDP/R- (receiver) board has insufficent throughtput and multiple receiving boards must be used.

For the purposes of correctly driving and terminating bussed front panel signals, there are four possible hardware switch configurations for an ICS-110BL board. These are:

- Master - the board drives timing signals and terminates received signals
- Mid-Slave - the board does not terminate or drive signals except data lines
- End-Slave - the board terminates timing signals and drives data lines
- Stand-alone Master - the board drives and terminates all signals

These classifications are applicable to both Local Bus and FPDP operation. It is possible therefore, for a board to be a Local Bus Mid-Slave but an FPDP Master, FPDP End-Slave or FPDP Stand-alone Master. The Master board must be located at one end of the cable. The End-Slave is located at the opposite end of the cable to the Master. The Mid-Slaves are located in between the Master and End-Slave boards. In a two board system, only Master and End-Slave configurations apply. Finally, the Stand-Alone Master refers to a one board system. The required switch settings are determined by which of these four cases applies to the board in question. Also, switch settings are affected by whether a configuration uses internal or external clock (EXT_CLK+/-) and trigger (EXT_ACQ+/-) signals.

If the ICS-110BL board/s is/are connected to one or more Digital Signal Processor (DSP) or Array Processor boards using the FPDP, the DSP board/s should be installed in the chassis at the End-Slave end of the FPDP cable (for example, the ordering should be Master, Mid-slaves, End-Slave, DSP). If FPDP is not being used, the position of the DSP board/s in the chassis with respect to the ICS-110BL boards is not important, however it is recommended that the ICS-110BL boards are installed in adjacent slots.

4.2 Functions Of Board Jumpers

The ICS-110BL has seventeen jumper blocks, designated SW1 through SW17 which must be configured by the user according to the required operating configuration. Other jumpers are used to configure the board for daughter board use, these are designated J1 through J16. Figure 4 shows the location of these jumper blocks on the ICS-110BL motherboard. A summary of the functions of the jumpers is given in the following table. Jumpers shown in the open position may be absent. Jumpers shown in the closed position must be present.

JUMPER	FUNCTION	NOTES
SW1, SW7	FPDP (P5) Terminations and PECL Strobe Enable	See Section 4.3
SW2	Internal/External sample clock configuration	See Section 4.3/4.6
SW3, SW4, SW6	Local Bus (P4) Terminations	See Section 4.3
SW5	External Clock Terminations	See Section 4.7
SW8	VMEbus Address Mode	See Section 4.4
SW9	VMEbus Interrupt Level	See Section 4.5
SW10	Not Used	
SW11, SW12, SW13, SW14, SW15	VMEbus Address	See Section 4.4
SW16, SW17	VMEbus Interrupt Level	See Section 4.5

4.3 Local Bus, FPDP and External Clock/Trigger Terminations

Jumper blocks SW2, SW3, SW4, SW5, SW6 and SW7 allow resistive terminations to be connected to the Local Bus and External Clock and Trigger signals which appear on the front panel P4 connector. The purpose of two SW2 jumper positions (SW2-1 and SW2-2) is to allow the internal clock of the Master board to drive the Master and Slave boards (if any). Details of the Local Bus P4 connector are given in Appendix B. The resistive terminations are 220 Ohm pull-up to +5VDC and 330 Ohm pull-down to ground on each signal.

SW6 connects the Local Bus PECL strobe signal drivers and terminations. The terminations are 390 Ohm to ground on each wire at the transmitter, and 100 Ohm connected between the two differential strobe signals at the receiver.

The drivers for the Local Bus clock and strobe signals must be enabled on Stand-Alone Master boards and on the Master board of a multi-board configuration. The terminations must be enabled on Stand-Alone Master boards and on End-Slave boards of multi-board configurations. On Mid-Slave boards of multi-board configurations, neither drivers nor terminations are enabled.

For the EXT_ACQ± signals, the terminations must be enabled on Stand-Alone Master and End-Slave boards only.

SW1 and SW7 connect the FPDP PECL Strobe signals and terminate some FPDP signals that are sourced by the receiving DSP board rather than the ICS-110BL. These jumpers should be inserted if the FPDP is being used, only on Master and Stand-Alone Master boards. The resistive terminations are 220 Ohm pull-up to +5VDC and 220 Ohm pull-down to ground on each signal.

The following table shows the correspondence between signals on the Local Bus connector, P4, and jumper positions in SW8, SW9 and SW10. In all cases, the closed position of the jumper (see Fig. 4) connects the termination or enables the specified function.

P4 Pin	Jumper	Signal	Function
1	SW2-1	CLOCK+	Connect Sample Clock to Master and Slave Boards
2	SW2-2	CLOCK-	Connect Sample Clock to Master and Slave Boards
1	SW3-1	CLOCK+	Terminate
2	SW3-2	CLOCK-	Terminate
3		Ground	
4		FRAME_TC	
5	SW3-3	ACQUIRE_SYNC	Terminate
6	SW3-4	BLOCK_SYNC	Terminate
7	SW2-3	EXT_CLOCK+	Terminate
8	SW2-4	EXT_CLOCK-	Terminate
9	SW5-1	EXT_ACQ+	Terminate
10	SW5-2	EXT_ACQ-	Terminate
11		Ground	
12	SW6-1	DATA_CLOCK+	Connect Driver
13	SW6-2	DATA_CLOCK-	Connect Driver
12,13	SW6-3	DATA_CLOCK+/-	Terminate
14	SW4-1	BOARD_ADDR0	Terminate
15	SW4-2	BOARD_ADDR1	Terminate
16	SW4-3	BOARD_ADDR2	Terminate
17	SW4-4	BOARD_ADDR3	Terminate
18	SW7-1	BOARD_ADDR4	Terminate
19	SW7-2	DATA_CLOCK_EN	Terminate
20		NC	

The following table shows the correspondence between signals on the FPDP connector, P5, and SW1, SW7 jumper positions. In all cases, the closed position of the jumper (see Fig. 4) connects the termination or enables the specified function.

P5 Pin (Cable wire)	Jumper	Signal	Function
13	SW1-1	SUSPEND*	220 Ohm Pull-Up
13	SW1-2	SUSPEND*	220 Ohm Pull-Down
7	SW1-3	NRDY*	220 Ohm Pull-Up
7	SW1-4	NRDY*	220 Ohm Pull-Down
25	SW7-3	PSTROBE	Connect Driver to FPDP
27	SW7-4	PSTROBE*	Connect Driver to FPDP

The following table lists the normal jumper positions for most of the Local Bus and FPDP jumpers depending on the board function. Other jumper positions are discussed in the following sections.

Board Configuration	SW2-3,4, SW3-1,2,3,4, SW4-1,2,3,4, SW5-1,2 SW6-3 SW7-1,2	SW2-1,2, SW6-1,2, SW1-1,2,3,4, SW7-3,4
Master	Open	Closed
Middle-Slave	Open	Open
End-Slave	Closed	Open
Stand-Alone Master	Closed	Closed

Examples of jumper settings for various board configurations are given in section 4.8.

4.4 VMEbus Board Address

The ICS-110BL VMEbus base address can be set at any 0x10000 (64 KByte) address interval in A24 or A32 address space using jumpers SW11 through SW15, as given in the following table. An closed jumper selects a zero for that address bit, while an open jumper selects a one. Consult Figure 4 for jumper polarities. Examples are discussed in section 4.8.

Jumper	VME Address Bit	Jumper	VME Address Bit	Jumper	VME Address Bit
SW15-3	A31	SW13-3	A23		
SW15-2	A30	SW13-2	A22	SW11-3	NC
SW15-1	A29	SW13-1	A21	SW11-2	NC
SW14-4	A28	SW12-4	A20	SW11-1	NC
SW14-3	A27	SW12-3	A19	SW10-4	NC
SW14-2	A26	SW12-2	A18	SW10-3	NC
SW14-1	A25	SW12-1	A17	SW10-2	NC
SW13-4	A24	SW11-4	A16	SW10-1	NC

The ICS-110BL can be configured, by means of jumper block SW8, to reply only to certain AM codes or to ignore AM codes when decoding short, standard, or extended addresses during VMEbus accesses. The configurable addressing modes of the ICS-110BL are:

Jumper	Address Decoding Scheme
SW8-1: C	A32 Addressing, AM Codes 09, 0B, 0D, 0F
SW8-2: C	A24 Addressing, AM codes 39, 3B, 3D, 3F
SW8-3: C	A32 Addressing, Ignore AM Codes
SW8-4	Unused

Under the Jumper column, SW8-X: C implies that jumper SW8 bit X is closed and all jumpers other than bit "X" of SW8 are open. The above AM codes refer to the following address decoding schemes:

AM Code	Function
39	Standard Non-Privileged Data Access
3B	Standard Non-Privileged Block Transfer
3D	Standard Supervisory Data Access
3F	Standard Supervisory Block Transfer
09	Extended Non-Privileged Data Access
0B	Extended Non-Privileged Block Transfer
0D	Extended Supervisory Data Access
0F	Extended Supervisory Block Transfer

The default factory settings are as follows:

VMEbus Base Address = 0xD00000
A24 Addressing, AM codes 39, 3B, 3D, 3F

4.5 VMEbus Interrupt Level

The VMEbus interrupt level is set using SW9, SW16 and SW17 as shown in the following table:

Jumper	SW9-1	SW9-2	SW9-3	IRQ Level
SW16-1: C	O	C	C	1
SW16-2: C	C	O	C	2
SW16-3: C	O	O	C	3
SW16-4: C	C	C	O	4
SW17-1: C	O	C	O	5
SW17-2: C	C	O	O	6
SW17-3: C	O	O	O	7

Under the Jumper column, SW16-X: C implies that all jumpers listed in that column other than bit "X" of SW16 are set open. Jumper SW9 position 4 is unused.

The default factory setting is:

VMEbus IRQ Level = 3.

4.6 Master/Slave Clock Selection

Jumpers SW2-1 and SW2-2 are used to connect the clock signal regenerated by the Sampling Master ICS-110BL to the slave boards, in multiple board configurations:

Master/Slave Clock Selection	SW2-1	SW2-2
Sampling Master board	Closed	Closed
Sampling mid-slave, end-slave boards	Open	Open

The default factory setting is:

Sampling Master

The clock termination resistors must also be correctly configured, regardless of whether the clock source is internal or external. The correct settings are shown in the following table. The definition of terms in the table is given in section 4.1.

Board Configuration	SW3-1	SW3-2
Master	Open	Open
Mid-Slave	Open	Open
End-Slave	Closed	Closed
Stand-Alone Master	Closed	Closed

4.7 EXT_ACQ Input

The EXT_ACQ input, P4 pins 9 and 10, is the external trigger signal used to start and stop ICS-110BL sampling when the Control Register bit CR<02> (ACQUIRE SOURCE) is set for external acquisition control. The board responds to the level of the signal. Acquisition will occur while the signal is at a high logic level, and will stop while the signal level is low. In multiple board configurations, the EXT_ACQ signal is used by the Master ICS-110BL only.

The board is designed to accept a signal which conforms to differential TTL levels. As with the External Clock, a single- ended TTL compatible level may be used instead of a differential signal. In this case, the signal should be connected to P4 pin 9. P4 pin 10 should be left unconnected. The high logic level on the signal must be at least 3.5 volts.

In a multiple board configuration, the EXT_ACQ signal is connected to the Master board, which synchronizes the signal to the sampling clock, and then transmits the reclocked signal as the ACQUIRE_SYNC signal on P4 pin 5. Termination of EXT_ACQ is achieved by setting jumpers SW5-1 & SW5-2 to the closed position as shown in the following table.

Board Configuration	SW5-1	SW5-2
Master	Open	Open
Middle-Slave	Open	Open
End-Slave	Closed	Closed
Stand-Alone Master	Closed	Closed

4.8 Daughter Board Configuration

The ICS-110BL can accept an optional signal conditioning daughter board (ICS-110B1L version). Jumpers J1 through J16 on the ICS-110BL motherboard provide connections for the analog input signals, either directly to the A/D converters, or to the daughter board, if installed. These jumpers must be correctly configured in either case. If the user installs or removes a daughter card, it will be necessary to move the positions of these jumpers. Jumper SW9-4 also needs to be changed when the daughter board is installed. Figures 5 through 8 show the appropriate settings for all these jumpers.

There are no switches or jumpers on the daughter board that require to be set.

4.9 Example Configurations

Figures 5 to 8 are provided as an aid to the installation procedure. They show jumper settings for all the common ICS-110BL configurations.

Figure 5 specifies the settings for a Master ICS-110BL in a multi-board system. This figure also reflects the following settings:

VMEbus base address = 0xD00000
A24 addressing, AM codes 39, 3B, 3D, 3F
VMEbus IRQ level = 3

Figure 6 specifies the settings for a Mid-Slave ICS-110BL in a multi-board system. This figure also reflects the following settings:

VMEbus base address = 0xD10000
A24 addressing, AM codes 39, 3B, 3D, 3F

Figure 7 specifies the settings for an End-Slave ICS-110BL in a multi-board system. This figure also reflects the following settings:

VMEbus base address = 0xD20000
A24 addressing, AM codes 39, 3B, 3D, 3F

Figure 8 specifies the settings for a Stand-Alone Master ICS-110BL in a single-board system. This figure also reflects the following settings:

VMEbus base address = 0xD00000
A24 addressing, AM codes 39, 3B, 3D, 3F
VMEbus IRQ level = 3

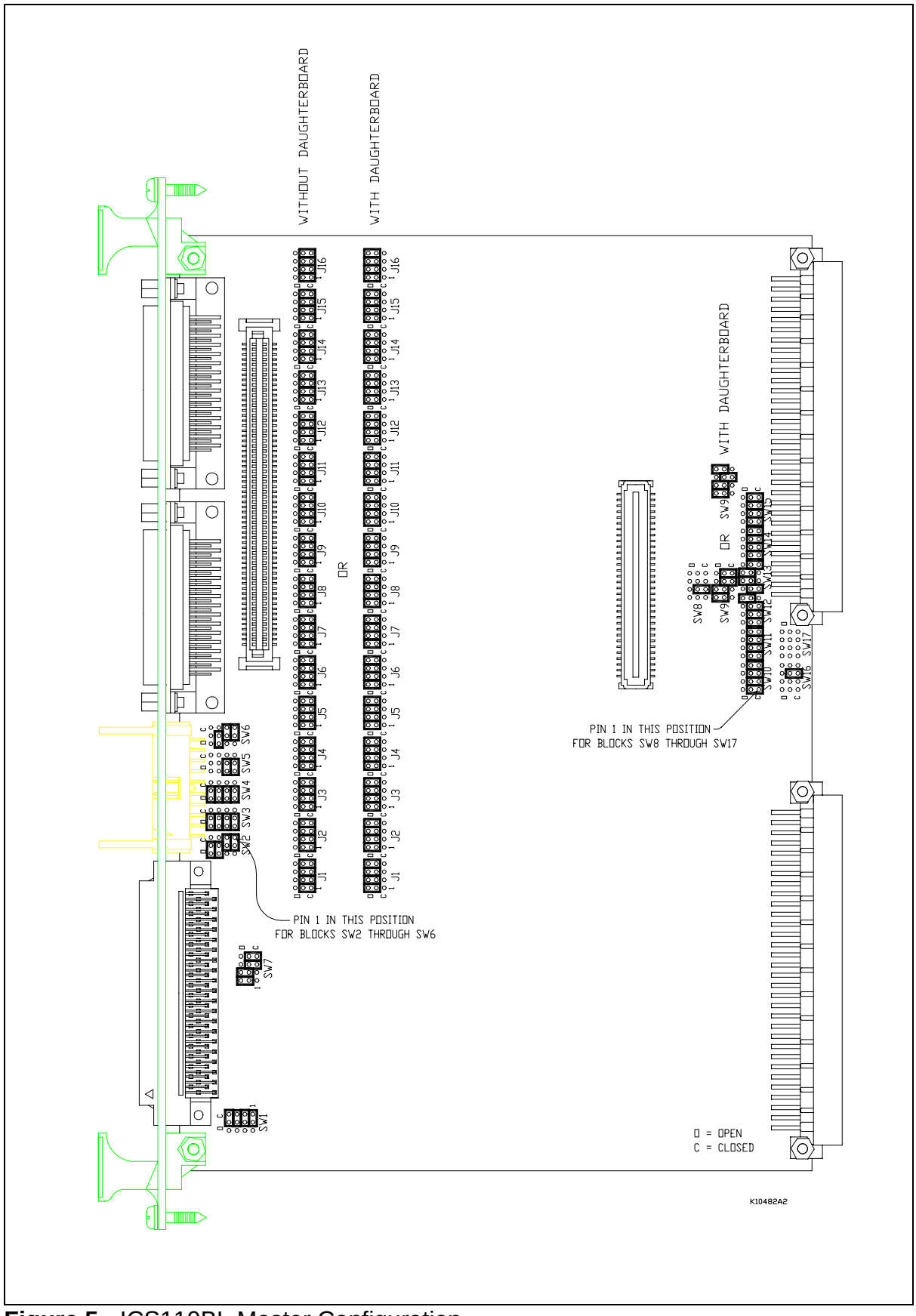


Figure 5 - ICS110BL Master Configuration

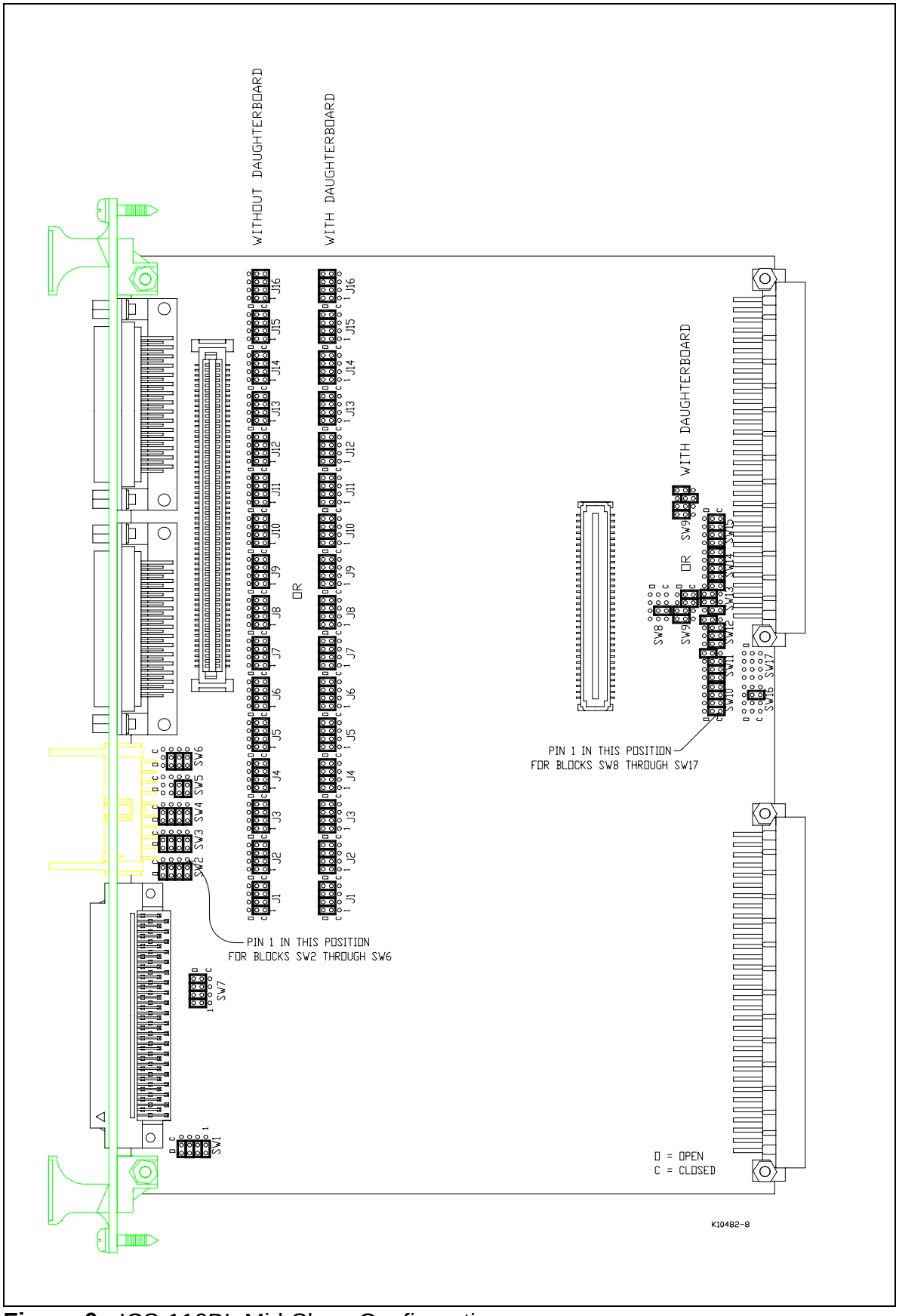


Figure 6 - ICS-110BL Mid-Slave Configuration

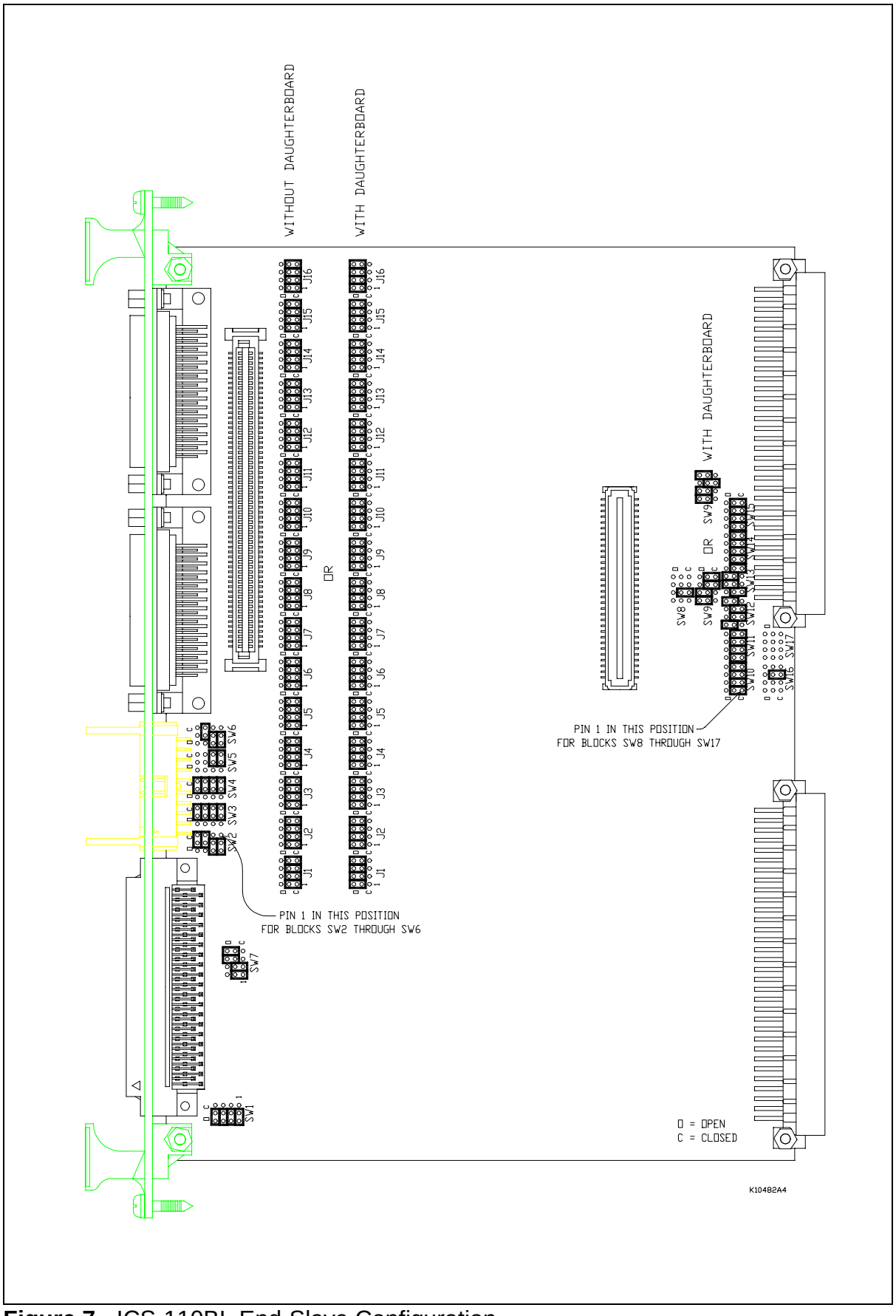


Figure 7 - ICS-110BL End-Slave Configuration

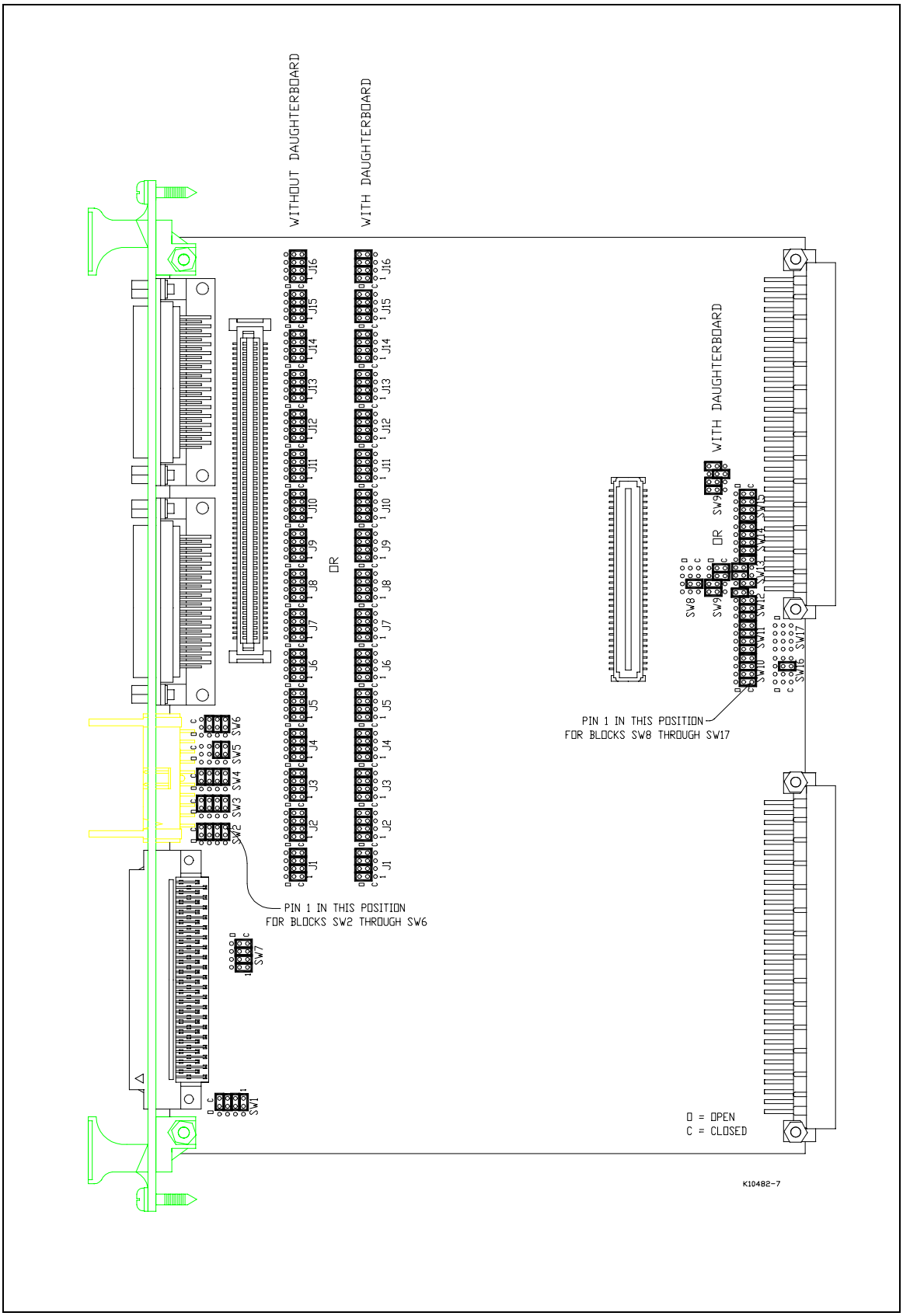


Figure 8 - ICS-110BL Stand-Alone Master Configuration

4.10 Front Panel Data Port (FPDP) Connections

The FPDP provides a bus style interface between multiple ICS-110BL boards and one or more Digital Signal Processor (Array Processor) boards. Up to 32 ICS-110BL boards may be linked on a single FPDP connection. Figure 9 shows, as an example, how four ICS-110BL boards can be bussed together. The 80-pin ribbon cable busses the four FPDP outputs, while the 20-pin Local Bus ribbon cable busses EXT_CLK+/-, EXT_ACQ+/-, and synchronization signals.

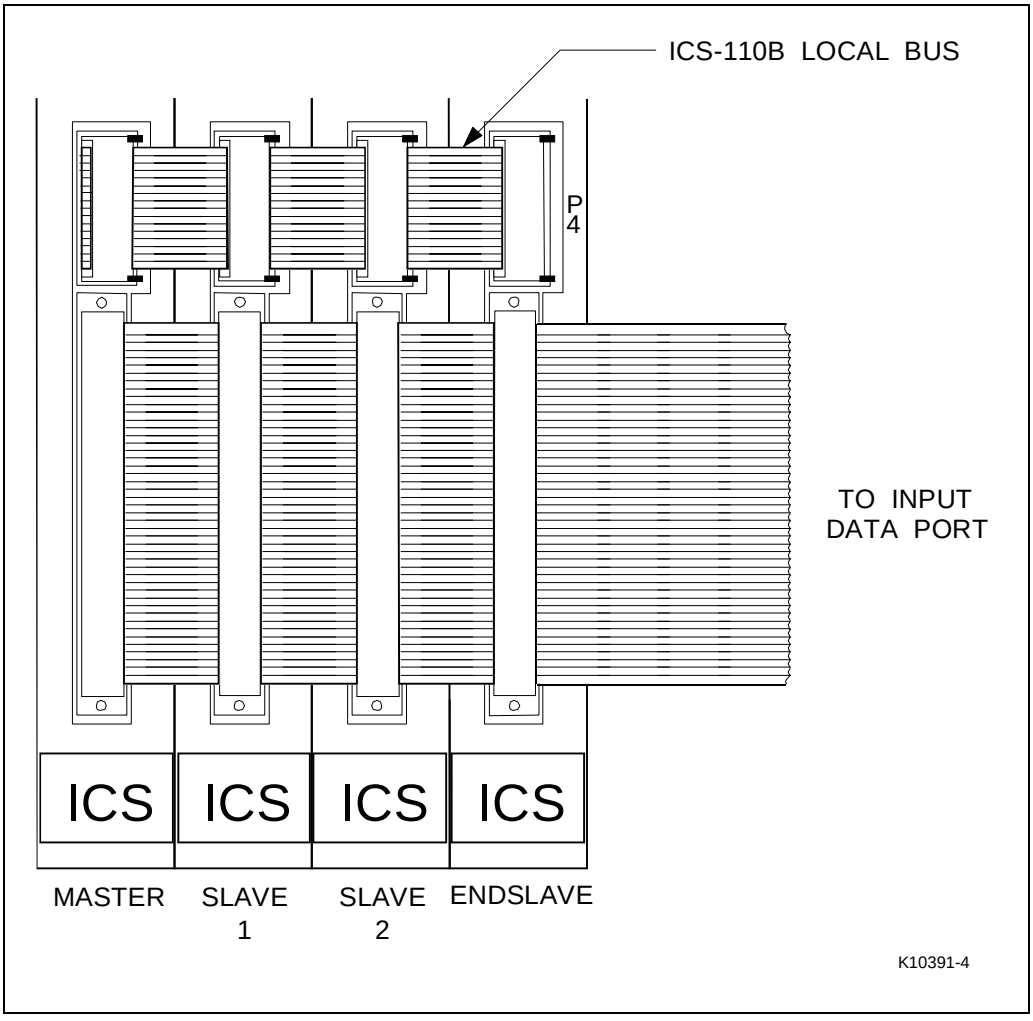


Figure 9 - ICS-110BL FPDP Connections

5. PROGRAMMING MODEL

The ICS-110BL memory map is shown in Fig. 10. The individual bit fields of the registers are given in Fig. 11 and Fig. 12. Detailed register descriptions are given in the following sections. All programming and control of the ICS-110BL is done through the VMEbus interface. All undefined control register bits may be written as 0 or 1 without affecting board operation. When read, they may also be in either state.

There are two 32-bit wide ADC Data areas, one in the VMEbus map and one in the VSB map. The VMEbus ADC Data area is 16,256 32-bit words (0xFE00 bytes) in length, while the VSB ADC_DATA area is 8,192 32-bit words (0x8000 bytes) in length.

5.1 General Notes

All transfers to and from ICS-110BL 32-bit registers should be done using D32 VMEbus cycles. In the case of 16-bit registers, D16 VMEbus cycles must be used. The A24 or A32 VMEbus base address is configured using jumpers on the board as described in section 4 above.

In the following register descriptions, register bits are referred to in the following way:

CR<0>	Bit 0 (least significant bit) of Control register.
VSBS<26:24>	Bits 24 to 26 inclusive of VSB Status register.

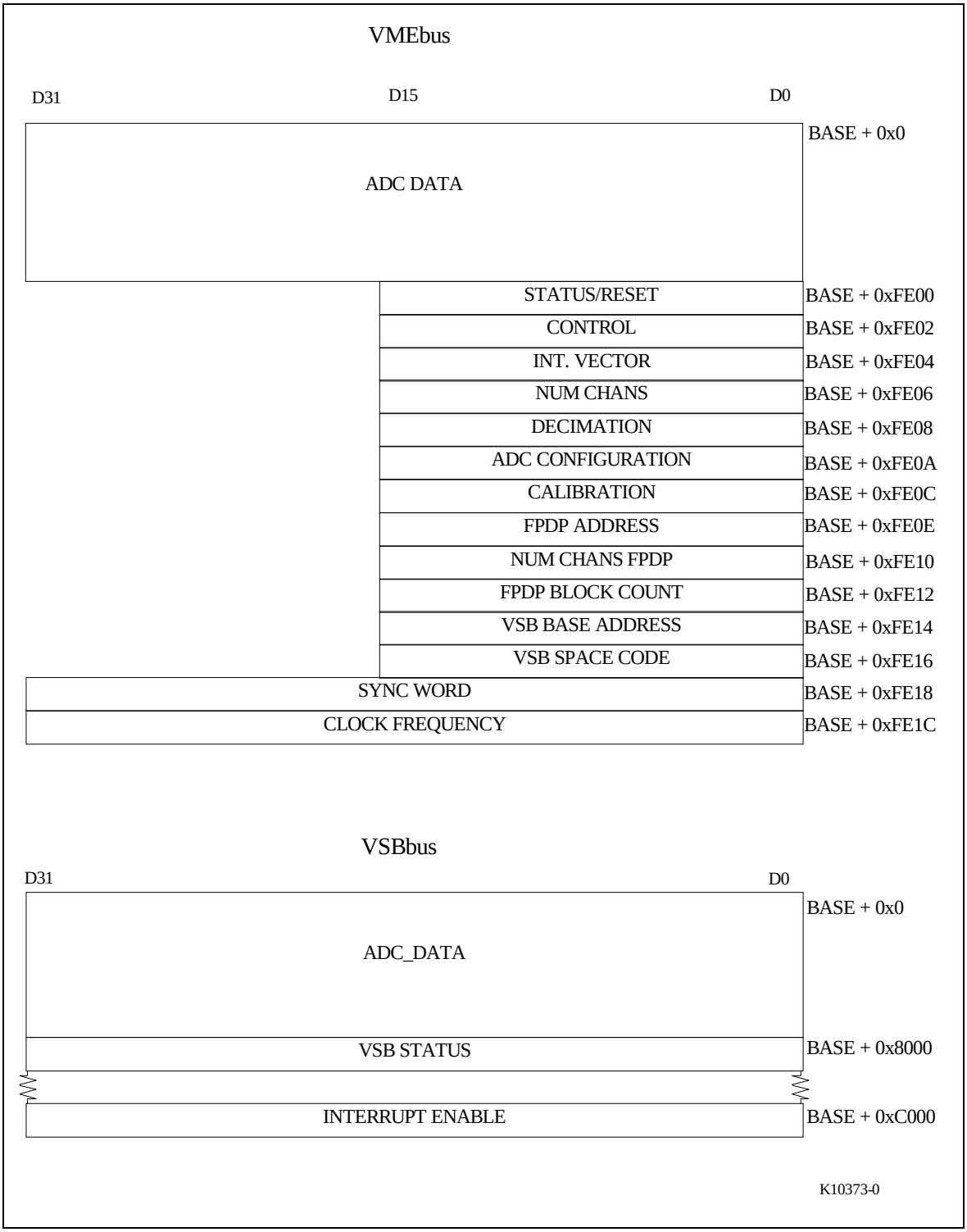


Figure 10 - ICS110BL VMEbus/VSB Address Map

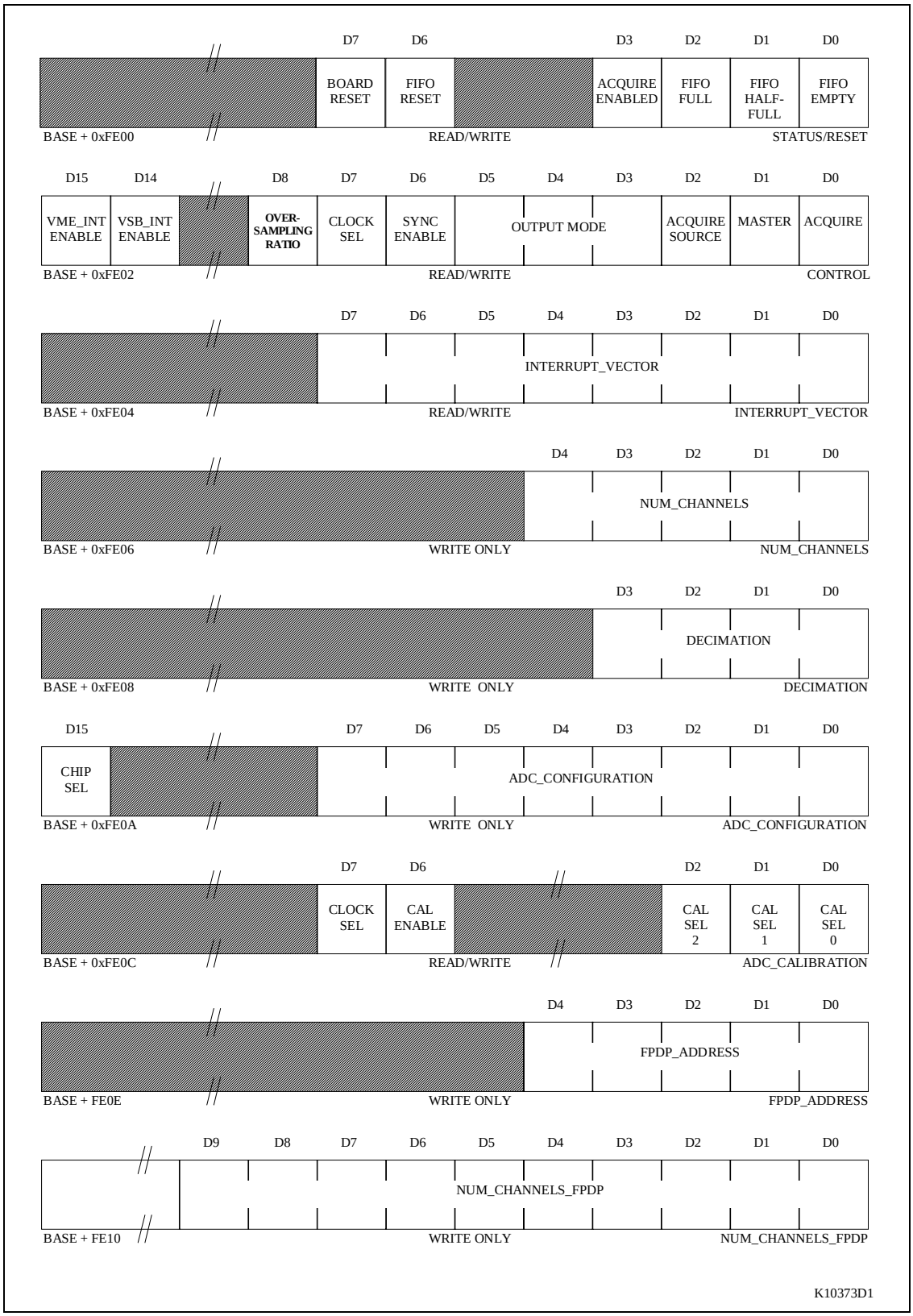


Figure 11 – ICS-110BL Register Descriptions

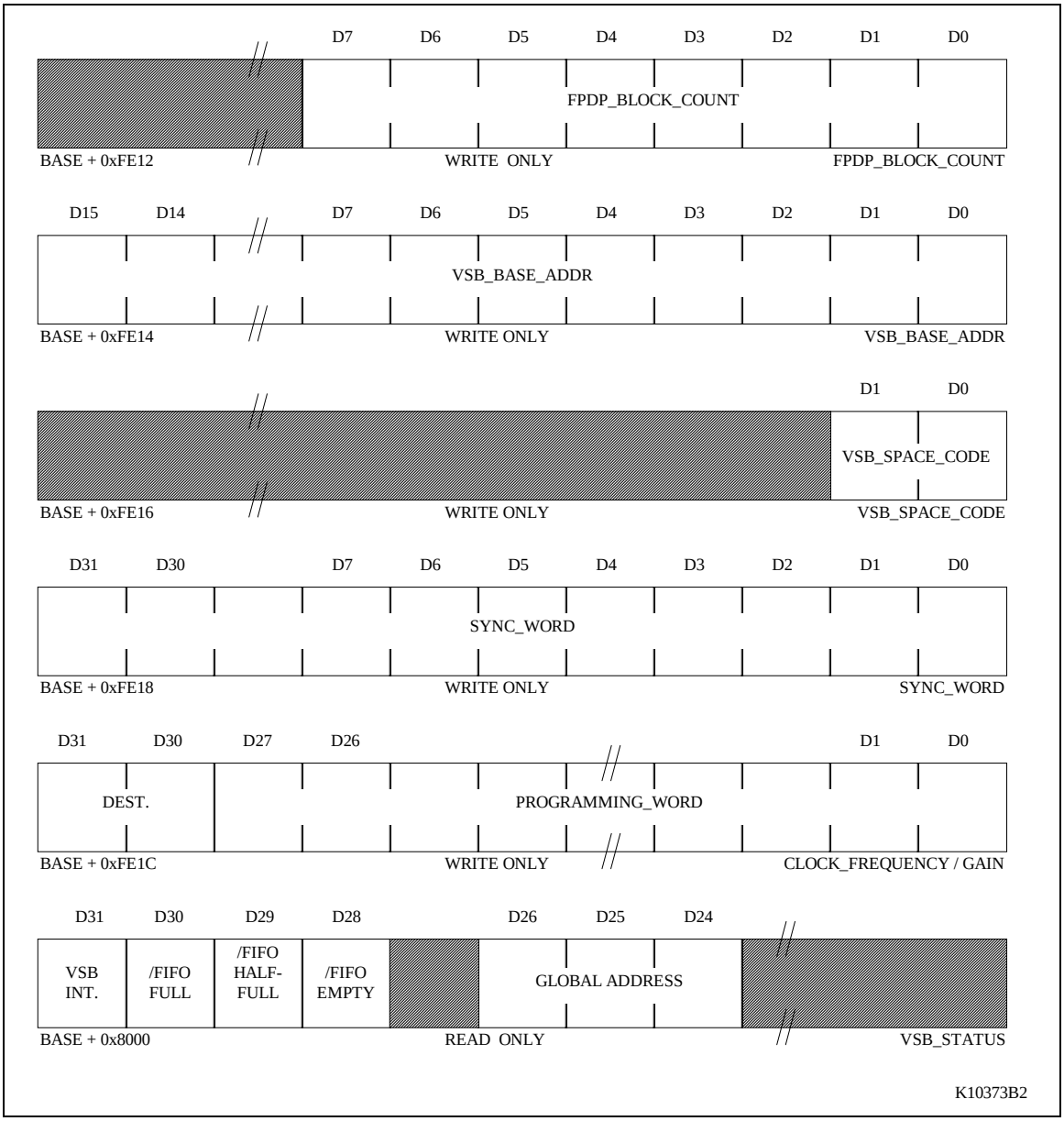


Figure 12 - ICS-110BL Register Descriptions (cont'd)

5.2 ADC Data Area (VMEbus)

Read Only

This area of the memory map provides the user with access to the ADC Data FIFO when VMEbus has been selected as the output path (CR<05:03> = 0 or 2). The VMEbus ADC Data area is 16,256 long words in length (0xFE00 = 65,024Bytes).

When addressing the ADC Data area, successive reads need not be to sequential addresses. Any access within the valid address range from the base address (see above) will read the next data value from the FIFO. It is valid to use the same address on every access, if desired. Random access to ADC data is not available.

For more information on ADC Data FIFO organization, consult section 6.1.

5.3 Status/Reset Register

Read/Write

The Status/Reset register allows the user to monitor the ADC Data FIFO for full, half-full, and empty conditions, as well as inform the user as to the current acquisition status. The status bits are read only. The register also allows the user to perform a Board reset or a ADC Data FIFO reset; these bits are write only.

5.3.1 SR<00> - FIFO Empty

Read Only

This bit informs the user as to whether or not the ADC Data FIFO is empty. When reading data from the ADC Data FIFO, the user should check the state of this flag before each read, in order to ensure that valid data remains in the FIFO.

SR<00>	FIFO Status
0	Not Empty
1	Empty

5.3.2 SR<01> - FIFO Half Full

Read Only

This bit informs the user as to whether or not the ADC Data FIFO is at least half-full. If VMEbus interrupts were enabled by means of CR<15>, a VMEbus interrupt will occur when the FIFO is at least half full. If VSB interrupts were enabled (CR<14>), a VSB interrupt will occur when the FIFO is at least half full. Note that the half full state occurs when the FIFO contains 16K samples (total from all selected channels) in unpacked mode, or 32K samples in packed mode.

SR<01>	**FIFO Half Full**
0	Less than Half Full
1	More than Half Full

5.3.3 SR<02> - FIFO Full

Read Only

This bit informs the user as to whether or not the ADC Data FIFO is full. This indicates an error condition, since data may have been lost. In this event, the user should stop acquisition, do a Board Reset (see section 5.3.6) and program the required configuration to the board before continuing. Note that the full state occurs when the FIFO contains 32K samples (total from all selected channels) in unpacked mode, or 64K samples in packed mode.

SR<02>	**FIFO Full**
0	Not Full
1	Full

5.3.4 SR<03> - Acquire Enabled

Read Only

This bit reflects the current acquisition status. When acquisition is enabled either internally or externally, the ICS-110BL waits until the beginning of the next frame before beginning to store data to the ADC Data FIFO. This ensures channel 0 is the first valid channel read from the ADC Data FIFO.

Similarly, when acquisition is disabled, the ICS-110BL waits until the end of the current frame before ending the acquisition cycle. This ensures that the complete current frame of data is written to the ADC Data FIFO before the acquisition cycle is stopped.

SR<03>	Acquire Enabled
0	Not running
1	Running

5.3.5 SR<07> - FIFO Reset

Write Only

Setting this bit resets the ADC Data FIFO to an empty condition. All data stored in the FIFO prior to the FIFO Reset operation is lost.

This operation should always be done after configuring the board and before enabling acquisition, to make sure that the ADC FIFO memory is empty prior to starting acquisition.

SR<07>	FIFO Reset
0	No action
1	Reset FIFO Memory

5.3.6 SR<08> - Board Reset

Write Only

When this bit is set, the ICS-110BL board is reset. Acquisition is halted and the board is reset to default (power up) conditions. In general, this should not be done unless a fault condition (for example, FIFO Full) has occurred. The effect of doing this, in detail, is as follows:

1. Control Register set to default values.
2. ADC Data FIFO reset to empty condition.
3. Any acquisition is immediately terminated.
4. The VSB interface is disabled (see section 3.12).

The above conditions also apply after a hardware VMEbus reset. All data already acquired to the ADC Data FIFO prior to the board reset operation is lost.

SR<08>	Board Reset
0	No action
1	Reset ICS-110BL

5.4 Control Register

Read/Write

The control register allows the user to configure the following operating parameters:

- acquisition start and stop control through software
- sampling master/slave selection
- internal/external acquisition control selection
- output mode (VMEbus packed/unpacked, VSB packed/unpacked, FPDP)
- internal/external clock selection
- oversampling ratio
- enable/disable VMEbus or VSB interrupts

The control register bits are discussed in detail below. The reset default for each CR bit reflects the bit's state after a hardware VMEbus reset or a software reset via SR<08>. Note that all undefined CR bits must be set to zero.

5.4.1 CR<00> - Acquire

This bit allows the user to start and stop acquisition under software control when internal triggering has been selected by setting CR<02> (Acquire Source) = 0. When Acquire=0, data acquisition is disabled and data is not written to the ICS-110BL FIFO memories. When Acquire=1, data acquisition is enabled and data is written to the ICS-110BL ADC Data FIFO memories.

CR<00>	**Acquire**
0	Stop Acquisition
1	Start Acquisition

Reset Default: Acquire=0.

5.4.2 CR<01> - Master

This bit allows the user to specify whether the board is configured as a Sampling Master or a Sampling Slave. When CR<01> = 1, the board is configured as a Sampling Master. When CR<01> = 0, the board is configured as a Sampling Slave. This bit must be set on Stand-alone Master boards.

CR<01>	**Master**
0	Sampling Slave
1	Sampling Master

Reset Default: Master=0.

5.4.3 CR<02> - Acquire Source

This bit allows the user to specify the triggering source for the Sampling Master (or Stand-alone Master), which can be either under software control using CR<00> (when Acquire Source=0), or under hardware control using the differential EXT_ACQ signal applied to P4 pins 9 and 10 (when Acquire Source =1). Note that a Slave's Acquire Source must always be set to Internal.

CR<02>	Acquire Source
0	Internal Trigger
1	External Trigger

Reset Default: Acquire Source=0 (Internal Trigger).

5.4.4 CR<05:03> - Output_Mode

These bits allow the user to specify the output path of the converted data. All output paths use 32-bit (D32) data path width. For all three output paths, the signed 24-bit samples from each channel may be output as one sample per 32-bit word, justified to the most significant 24 bits of each word. Alternatively, for VMEbus and VSB output (but not FPDP output), the data may be truncated to 16 bits and output as two samples per 32-bit word. The two output formats are referred to in the following table as unpacked data and packed data, respectively. Tables showing the format of packed and unpacked data are given in section 6.

Output Mode			Output Path
CR<05>	CR<04>	CR<03>	
0	0	0	VMEbus (Packed)
0	0	1	VSB (Packed)
0	1	0	VMEbus (Unpacked)
0	1	1	VSB (Unpacked)
1	0	0	FPDP Master
1	0	1	FPDP Slave

Reset Default: Output Mode=0 (VMEbus Packed).

5.4.5 CR<06> - Sync Enable

This bit is reserved for future use. It must be set to zero when programming the board.

Reset Default: Sync Enable=0.

5.4.6 CR<07> - Clock Select

This bit allows the user to select either internal or external clock. When using an external clock in multiple board systems, external clock should be selected on the Sampling Master board only. All Sampling slaves should have internal clock selected.

CR<07>	Clock Select
0	Internal
1	External

Reset Default: Clock Select=0 (Internal).

5.4.7 CR<08> - Oversampling Ratio

This bit sets the oversampling ratio of the converter. 128 times oversampling provides superior signal-to-noise ratio performance but is available only for output rates up to 54kHz. 64 times oversampling is available for output rates up to 108kHz.

CR<08>	Oversampling ratio
0	Oversampling ratio = 64 x
1	Oversampling ratio = 128 x

Reset Default: Oversampling ratio = 0 (64 x).

5.4.8 CR<14> - VSB Int Enable

Setting this bit enables VSB interrupts when the ADC Data FIFO becomes half-full.

CR<14>	VSB Int Enable
0	VSB Interrupt disabled
1	VSB Interrupt enabled

Reset Default: VSB Interrupt disabled.

5.4.9 CR<15> - VME Int Enable

Setting this bit enables VMEbus interrupts when the ADC Data FIFO becomes half-full.

CR<15>	VME Int Enable
0	VMEbus Interrupt disabled
1	VMEbus Interrupt enabled

Reset Default: VMEbus Interrupt disabled.

5.5 Interrupt Vector Register

Read/Write

This register allows the user to specify the VMEbus interrupt vector for the board, and must be written before enabling VMEbus interrupts. When using an ICS-supplied software device driver, it is not necessary for the user to program this register, since the driver does so.

5.6 Num Channels Register

Write Only

This register allows the user to set the number of channels to be acquired in each frame. Unused channels are simply discarded prior to storage in the ADC Data FIFO. The number of channels selected for acquisition must be an even number, and not greater than the channel capacity of the board. The register must be set to the actual number of channels required less one. Thus, valid numbers written to this register are 1 (2 channels) to 31 (32 channels), in steps of 2.

In multiple board synchronous sampling configurations, when the P4 local bus connector is bussed, it is mandatory to allocate the full 32 channels on all boards except the End Slave.

Reset Default: None

5.7 Decimation Register

Write Only

This register is used to set the decimation factor. Decimation is done by periodically discarding a specified number of samples from each channel at the output of the converters, before the samples are written to the ADC Data FIFO. The decimation is applied equally to all channels.

The register allows the user to specify the decimation factor in the range 1 to 16. The number programmed to the register must be the required decimation factor minus one. The decimator behaviour is given by the following equations:

$$f_{OP_{DEC}} = \frac{f_{OP}}{DF}$$

$$DF = (N + 1)$$

where :

$f_{OP_{DEC}}$ = Decimated output rate (Hz)

f_{OP} = Output Rate before decimation (Hz)

DF = Decimation factor

N = Programmed decimation value (0 - 15)

For example, when Decimation=0, no decimation of the output takes place. When Decimation=1, every second output frame of data is decimated.

5.8 ADC Configuration

Write Only

This register is used for setting the configuration of the Analog-to-Digital converters. This is done by controlling several signal pins of the converters. All converters are accessed simultaneously and are configured in the same way.

Features of the converters are described in detail in the AK5393 data sheet available from AKM (ref. 3).

The features controlled are:

- Converter calibration - this should always be done following power-up.
- Enabling and disabling of on-chip high-pass filter

These features are described in detail in section 3.15. For compatibility with the earlier ICS-110B product, the programming of these features is done by accessing two notional registers on the converters themselves.

The converter registers are programmed by writing the address of the notional on-chip register followed by the data for each register to be programmed. Registers are programmed sequentially starting with the address specified; only two registers are available. Each value written to this register must have bit 15 (chip select) set, and a zero value must be written first in order to prepare the interface for programming. The procedure is as follows:

1. Write value 0x8000 to this register (i.e. zero data with chip select bit set).

2. Write address of first register to be programmed.
3. Write successive bytes of data to this register, in order of ascending register address.
4. Write zero to disable interface.

The default ADC configuration following power up is as follows:

- High pass filter enabled.

5.9 ADC Calibration

Read/Write

This register is used to configure the calibration circuit on the signal conditioning daughter board. It is not available if the daughter card is not present. This feature should not be confused with converter chip calibration which is always available.

5.9.1 ADC Calibration<02:00> - Cal/Test Waveform Select

When using the on-board calibration signal generator, these bits select which waveform is to be used. The on-board PROM stores eight waveforms, numbered 0 through 7.

5.9.2 ADC Calibration<06> - Cal/Test Enable

This bit, when set, selects the calibration/test signal (either from the PROM or from the external calibration/test signal input), for input to all ADC channels. When clear, the front panel analog signal inputs are selected.

5.9.3 ADC Calibration<07> - Clock Sel

This bit, when set, selects the on-board PROM as the source of the calibration/test signal. When clear, the external calibration/test signal is selected. For this selection to be active, ADC Calibration<06> must be set.

5.10 FPDP Address Register

Write Only

This register is used to set the FPDP board address in a multiple board system when using the Front Panel Data Port. The board address is used to control the reading of data over the FPDP in a multi-board system.

The FPDP board address must be set, even if only one ICS-110BL board is in use. In this case the board address must be set to zero.

The FPDP Address should be programmed as zero on the first board (FPDP Master), and should then be allocated in ascending order to each board in turn. For a 3-board system the FPDP Addresses should be allocated as follows:

Master :	BOARD_ADDRESS=0.
Mid-Slave :	BOARD_ADDRESS=1.
End-Slave :	BOARD_ADDRESS=2.

The highest FPDP Address allowed in a multi-board system is 31 (for a 32-board system).

5.11 Num Channels FPDP Register

Write Only

This register allows the user to select the total number of channels when using the Front Panel Data Port. The number of channels in a single or multi-board system must be an even number. Num Channels FPDP must be set to the actual number of channels less one. This register only needs to be set on the FPDP Master. When configuring multiple board systems with more than one FPDP, this register must be programmed on each FPDP Master, and must indicate the number of channels assigned to that FPDP bus only (not the total number of channels for all FPDP busses).

As an example, an 80-channel system would consist of three boards defined as follows:

Master :	Num Channels=31 (32 channels), Num Channels FPDP=79 (80 channels in system).
Middle-Slave :	Num Channels =31 (32 channels).
End-Slave :	Num Channels =15 (16 channels).

The maximum number of channels in a multi-board system when using the Front Panel Data Port is limited to 1024 (32 boards) (Num Channels FPDP = 1023). Note that in bussed configurations, it is mandatory for all boards, except for the End Slave, to have 32 channels allocated.

5.12 FPDP Block Count Register

Write Only

This register defines, when configured for FPDP output, how many frames are stored in a block before a bank jumper occurs.

The number programmed into this register, specifying the number of frames per block, must be the actual number of frames minus one (FPDP Block Count = 0 to 255).

In general, users should use a larger FPDP Block Count value unless latency is a critical issue, in which case a value of zero may be programmed to this register to provide the lowest possible latency. In this case, the user should ensure that the receiving FPDP interface is capable of keeping up with the data rate without asserting the FPDP Suspend (SUSPEND*) signal, otherwise data may be lost.

5.13 VSB Base Address Register

Write Only

This register specifies A16-A31 of the board's VSB Base Address. A write operation to this register enables the VSB interface.

5.14 VSB Space Code Register

Write Only

This register specifies the board's VSB Space Code. Generally all boards in the system should be configured with the same space code, otherwise they will not be able to communicate.

5.15 Sync Word Register

Write Only

This register is reserved for future use.

5.16 CLOCK Frequency/Gain Register

Write Only

This register is used for programming the sampling frequency, the FPDP Strobe frequency and the daughter board channel gain (if the daughter board is installed). The selection of which of these parameters is to be programmed is made using bits 30 and 31. The programming value is written to the least significant 30 bits of the register.

Clock Freq/Gain<31>	Clock Freq/Gain<30>	Parameter Programmed
0	0	Sampling Clock
1	0	FPDP Strobe Frequency
x	1	Daughter Board Gain

5.16.1 Clock Frequency

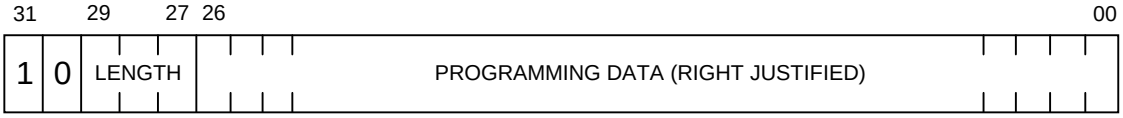
When programming either the sampling or FPDP Strobe frequency, the register is programmed with a variable length programming word which represents the frequency required. The programming word may be calculated using the information given in section 7.1.

Note that when programming the sampling frequency, the actual frequency programmed to the clock must be a multiple (either 256x or 512x) of the required output rate, as described in section 3.5.

To program a clock frequency to either the ADC sampling clock or to the FPDP Strobe clock oscillators, a series of programming words must be written to the register, with the same bits set in bits 30 and 31 of the register each time, as appropriate for the specific clock to be programmed. Appendix 7.1 describes how to calculate these programming words. Each word should include a length parameter in bits 29-27, inclusive, to indicate the length of the programming word in excess of 22 bits. If the programming word length is less than 23 bits, the parameter should be set to zero. A delay of approximately 170 ms should be observed after the programming of each word.

The sampling clock programming words are therefore structured as follows:

The FPDP Strobe programming words are therefore structured as follows:



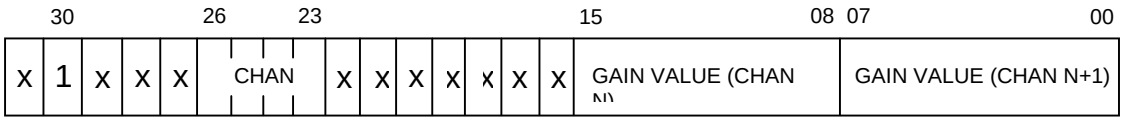
After programming the required sequence of words, it takes up to 10ms for the clock frequency to achieve its final value.

5.16.2 Gain Programming

The optional signal conditioning daughter board must be installed in order for gain programming to operate. Programmed gain changes occur on the second zero crossing of the input waveform after programming, unless no zero crossing occurs, in which case the gain change occurs after approximately 18 milliseconds. A delay of at least 100 microseconds should be observed between each write of a gain word of this register.

The programming word consists of channel pair identifier (bits 23-26) and gain word (bits 00-22). Bit 30 must be set to identify the programming word as a gain setting. Gains are programmed for a pair of channels at a time. The register must be written repetitively in order to program gain values for all channels on a board.

In the diagram below, channel numbering 0-31 is assumed, with the channel number N being an even number.



For a required gain of Gain dB, calculate the programmed value, G, for each channel as follows:

1. G1 = ((Gain (dB) + 95.5) x 2) + 1
2. G1 must be taken as an integer and truncated to an eight bit value.
3. G = (G1, with bit order reversed). This is now the gain value for one channel.

A second gain value must be calculated for the second channel of the pair to be programmed, using the same method as in steps 1-3 above. Note that the even numbered channel is programmed in bits 8-15, while the odd numbered channel is programmed in bits 0-7.

To select the channel pair to be programmed, the number of the even numbered channel, divided by two, is programmed in bits 23-26.

The composite value programming word should then be written to the Clock Frequency/ Gain register with bit 30 set high.

5.17 ADC Data Area (VSB)

Read Only

This area of the memory map provides the user with access to the ADC Data FIFO when VSB has been selected as the output path (CR<05:03> = 1 or 7). Each access to this area will read successive samples from the ADC Data FIFO, regardless of the actual address used. Random access to the FIFO is not available. The VSB ADC Data area is 8,192 long words in length (32 KBytes, = 0x8000).

When addressing the ADC_DATA area, successive reads need not be to sequential addresses. Any access within the valid address range from the base address (see above) will read the next data value from the FIFO. It is valid to use the same address on every access, if desired.

For more information on ADC Data FIFO organization, consult section 6.1.

5.18 VSB Status Register

Read Only

The ICS-110BL VSB interface includes a 32-bit VSB Status register. This register provides information regarding FIFO status (the same as that provided by the VMEbus Status register), as well the status of the VSB interrupt generator on the ICS-110BL. Because the ICS-110BL supports polled interrupts, this STATUS register must be read after a VSB interrupt to verify the origin of the interrupt. When this register is read, VSB interrupts are automatically disabled.

5.18.1 VSB Status<26:24> - Global Address

These three bits reflect the VSB Global Address of the ICS-110BL. The Global Address of the ICS-110BL is slot dependant with regard to the VSBbus backplane. The leftmost board in the VSBbus backplane has a Global Address = 0. The next board to the right has a Global Address = 1, and so on. The VSB Global Address is defined and hardwired on the VSB backplane, and does not need to be set by the user.

5.18.2 VSB Status<28> - FIFO Empty

This bit informs the user as to whether or not the ADC Data FIFO is empty. When reading data from the ADC Data FIFO, the user should check the state of this flag before each read, in order to ensure that valid data remains in the FIFO.

VSB Status <28>	FIFO Status
1	Not Empty
0	Empty

5.18.3 VSB Status<29> - FIFO Half Full

This bit informs the user as to whether or not the ADC Data FIFO is at least half-full. If VMEbus interrupts were enabled by means of CR<15>, a VMEbus interrupt will occur when the FIFO is at least half full. If VSB interrupts are enabled (CR<14>), a VSB interrupt will occur when the FIFO is at least half full.

VSB Status <29>	FIFO Half Full
1	Less than Half Full
0	More than Half Full

5.18.4 VSB Status<30> - FIFO Full

This bit informs the user as to whether or not the ADC Data FIFO is full. This indicates an error condition, since data may have been lost. In this event, the user should stop acquisition, perform a Board Reset (see section 5.3.6) and program the required configuration to the board before continuing.

VSB Status <30>	FIFO Full
1	Not Full
0	Full

5.18.5 VSB Status<31> - VSB Int

When this bit = 1, a VSB interrupt is pending for this board. When VSB Int = 0, no interrupt has been generated.

5.19 VSB Interrupt Enable Register

Read Only

Performing a read operation at this register enables VSB interrupts. For the ICS-110BL to source a VSBbus interrupt, this register must be read and the VSB Int Enable bit (CR<14>) must be set.

See section 6.3 for an example of how to set up an ICS-110BL VSB interrupt mechanism.

6. USING THE ICS-110BL

This section provides an overview of the board operation through the use of examples.

6.1 ADC Data FIFO Organization

This section discusses ADC Data FIFO organization with respect to the different output modes.

6.1.1 VMEbus Data Organization

Data from the ADC Data FIFO may be read over the VMEbus as 32-bit (longword) read operations from the ICS-110BL VMEbus ADC Data area at VMEbus address BASE+0x0 (BASE refers to the base address of the ICS-110BL). Table 6.1 shows the organization of the ADC Data FIFO for Packed Output Mode transfers.

Table 6.2 shows the organization of the ADC Data FIFO for Unpacked Output Mode transfers.

To access data over the VMEbus, CR<05:03> (Output Mode) should be set to 0 or 2.

6.1.2 VSBbus Data Organization

Data from the ADC Data FIFO is accessible over the VSBbus as 32-bit longword read operations from the ICS-110BL VSBbus ADC Data area at VSB address BASE (BASE refers to the VSBbus base address of the ICS-110BL). The organization of the ADC Data FIFO as seen by the VSB is the same as that for the VMEbus.

To access data over the VSBbus, CR<05:03> (Output Mode) should be set to 1 or 7.

6.1.3 FPDP Data Organization

The ICS-110BL FPDP interface allows the user to move data at rates of up to 20 MSample/s. This standard supports a 32-bit data bus, however the ICS-110BL drives only 24 bits of the data bus (bits D31 through D08). Bits D07:D00 are held in the low state. Table 6.2 summarizes the data organization on the FPDP.

TABLE 6.1 - Packed Data Output Format (Eight Channels Selected)

	D31 D16	D15 D00
FIRST READ	CHANNEL 0 (T)	CHANNEL 1 (T)
SECOND READ	CHANNEL 2 (T)	CHANNEL 3 (T)
THIRD READ	CHANNEL 4 (T)	CHANNEL 5 (T)
•	CHANNEL 6 (T)	CHANNEL 7 (T)
•	CHANNEL 0 (T+1)	CHANNEL 1 (T+1)
•	CHANNEL 2 (T+1)	CHANNEL 3 (T+1)
•	CHANNEL 4 (T+1)	CHANNEL 5 (T+1)
•	CHANNEL 6 (T+1)	CHANNEL 7 (T+1)
•	CHANNEL 0 (T+2)	CHANNEL 1 (T+2)
•	CHANNEL 2 (T+2)	CHANNEL 3 (T+2)
•	CHANNEL 4 (T+2)	CHANNEL 5 (T+2)
•	CHANNEL 6 (T+2)	CHANNEL 7 (T+2)
•	CHANNEL 0 (T+3)	CHANNEL 1 (T+3)
•		

TABLE 6.2 - Unpacked Data Output Format (Eight Channels Selected)

	D31 D08	D07 D00
FIRST READ	CHANNEL 0 (T)	0
SECOND READ	CHANNEL 1 (T)	0
THIRD READ	CHANNEL 2 (T)	0
•	CHANNEL 3 (T)	0
•	CHANNEL 4 (T)	0
•	CHANNEL 5 (T)	0
•	CHANNEL 6 (T)	0
•	CHANNEL 7 (T)	0
•	CHANNEL 0 (T+1)	0
•	CHANNEL 1 (T+1)	0
•	CHANNEL 2 (T+1)	0
•	CHANNEL 3 (T+1)	0
•	CHANNEL 4 (T+1)	0
•		

6.2 Single-Board Real-Time VMEbus Operating Example

In this configuration, data is converted and accessed over the VMEbus using 32-bit read operations. The following example explains how to initialize the ICS-110BL, and how to access the data in real-time using the VMEbus interrupt mechanism. A twenty channel configuration is assumed, operating at a 108 kHz output rate using the internal sampling clock in 64x oversampling mode. Acquisition control is internal using the ACQUIRE Control Register bit (CR<00>). The board jumper settings must be configured for Stand-Alone Master operation with internal clock and trigger, as in Figure 8.

1. Perform a board reset by writing to the Status/Reset register with SR<08> set.

2. Program the Clock Frequency register with a value calculated using the procedure of section 7.1 to set the sampling clock frequency to 100,000 x 256 = 25.6 MHz. Note that because the required oversampling ratio is 64x, the clock frequency must be set to 256x the required output rate.

3. Configure the ICS-110BL CR as follows:

   CR<00> ACQUIRE=0.
   CR<01> MASTER=1.
   CR<02> ACQUIRE SOURCE=0.
   CR<05:03> OUTPUT MODE=0.
   CR<06> SYNC ENABLE=0.
   CR<07> CLOCK SELECT=0.
   CR<08> OVERSAMPLING RATIO=0.
   CR<14> VSB_INT_ENABLE=0.
   CR<15> VME_INT_ENABLE=1.

4. Set NUM CHANNELS=19.

5. Write to the Status/Reset register FIFO RESET bit (SR<07>) to reset the ADC Data FIFO.

6. To begin acquisition, set CR<00> ACQUIRE=1.

7. Wait for a VMEbus interrupt.

8. When an interrupt occurs:

   A. Disable interrupts by setting VME_INT_ENABLE=0.
   B. Check for data loss by reading FIFO_FULL in the VMEbus Status/Reset register.
   C. Perform up to 32,768 data transfers via the VMEbus ADC Data FIFO register.
   D. Enable VMEbus interrupts by setting VME_INT_ENABLE=1.

For real-time operation, repeat steps 7. and 8.

6.3 Three-Board Real-Time VSB Operating Example

In this configuration, data is converted and accessed over the VSB using 32-bit read operations. The example explains how to initialize all three ICS-110BL boards, and how to access the data in real-time using the VSB interrupt mechanism. A 96-channel configuration is assumed operating at a 20 kHz output rate in 128x oversampling mode using an external clock. Acquisition control is external using the P4 EXT_ACQ input. The board jumpers must be correctly set as explained in section 4 of this manual in order to achieve this.

A VSB base address of 0x10000000 is given to the Master board, with each slave spaced 0x10000 above the adjacent board.

The external trigger signal must be fed to EXT_ACQ+/- (pins 9 and 10) of the P4 Local Bus. The differential external clock signal must be fed to EXT_CLK+/- (pins 7 and 8) of the P4 Local Bus. The clock frequency must be 20 kHz x 512 = 10.24 MHz. Note that the ratio is 512 because the converter oversampling ratio is 128x.

Jumper settings for this 3-board system should be as shown in Figures 5 to 7.

1. Perform a board reset by writing to the Status/Reset register with SR<08> set.

2. Configure the ICS-110BL Master CR as follows:

   CR<00> ACQUIRE=0.
   CR<01> MASTER=1.
   CR<02> ACQUIRE SOURCE=1.
   CR<05:03> OUTPUT MODE=1.
   CR<06> SYNC ENABLE=0.
   CR<07> CLOCK SELECT=1.
   CR<08> OVERSAMPLING RATIO=1.
   CR<14> VSB_INT_ENABLE=1. (Master produces VSB interrupt)
   CR<15> VME_INT_ENABLE=0.

   VSB_BASE_ADDRESS = 0x1000.
   VSB_SPACE_CODE = 3.

   Configure the ICS-110BL Middle-Slave CR as follows:

   CR<00> ACQUIRE=1.
   CR<01> MASTER=0.
   CR<02> ACQUIRE SOURCE=0.
   CR<05:03> OUTPUT MODE=1.
   CR<06> SYNC ENABLE=0.
   CR<07> CLOCK SELECT=0.
   CR<08> OVERSAMPLING RATIO=1.
   CR<14> VSB_INT_ENABLE=0.
   CR<15> VME_INT_ENABLE=0.

   VSB_BASE_ADDRESS = 0x1001.

VSB_SPACE_CODE = 3.

Configure the ICS-110BL End-Slave CR as follows:

CR<00> ACQUIRE=1.
CR<01> MASTER=0.
CR<02> ACQUIRE SOURCE=0.
CR<05:03> OUTPUT MODE=1.
CR<06> SYNC ENABLE=0.
CR<07> CLOCK SELECT=0.
CR<08> OVERSAMPLING RATIO=1.
CR<14> VSB_INT_ENABLE=0.
CR<15> VME_INT_ENABLE=0.

VSB_BASE_ADDRESS = 0x1002.
VSB_SPACE_CODE = 3.

3. On all three boards, set NUM_CHANNELS=31.

4. Write to the Status/Reset register FIFO RESET bit (SR<07>) on all three cards to reset the ADC Data FIFOs.

5. To start acquisition, assert the EXT_ACQ input signal.

6. Read the VSB INTERRUPT_ENABLE register of the Master ICS-110BL to enable VSB interrupts.

7. Wait for a VSB interrupt.

8. When an interrupt occurs:

   A. Check for data loss by reading FIFO Full bit in the VSB STATUS register of the Master.
   B. Check that the Master ICS-110BL was the source of the interrupt by verifying that the VSB Int bit in the VSB STATUS register of the Master is set. If the Master ICS-110BL is NOT the interrupt source, skip step C.
   C. Perform up to 32,768 data transfers via the VSB ADC Data FIFO register of each board.

For real-time operation, repeat steps 6. through 8.

6.4 Two-Board Real-Time FPDP Operating Example

In this configuration, data is converted by two ICS-110BL boards and transmitted over the FPDP interface to a receiving board, which might be an ICS-2200, ICS-7220 or a Digital Signal Processor. The following example explains how to initialize both ICS-110BL boards, as well as prepare the FPDP interface. A 40-channel configuration is assumed using the internal clock and operating at an output rate of approximately 1.2 kHz in 128x oversampling mode. Acquisition control is external using the P4 EXT_ACQ+/- input.

The differential external trigger is applied to the EXT_ACQ+/- signal (pins 9 and 10) of the front panel P4 expansion connector. The FPDP bus must be connected between the two ICS-110BL boards and the FPDP receiver. The FPDP receiver provides the necessary signals to read data from the ICS-110BL FPDP.

With a two ICS-110BL board configuration, the left-hand board should be configured as a Master, and the right-hand ICS-110BL should be configured as an End-Slave. Jumper settings for both these configurations should be as shown in Figures 5 and 7.

1. Perform a board reset by writing to the Status/Reset register with SR<08> set.

2. Program the Clock Frequency register with a value calculated using the procedure of section 7.1 to set the sampling clock frequency to 1,200 x 512 = 614.4 kHz. Note that because the oversampling ratio is 128x, the clock frequency must be set to 512x the required output rate.

3. Configure the ICS-110BL Master CR as follows:

   CR<00> ACQUIRE=0.
   CR<01> MASTER=1.
   CR<02> ACQUIRE SOURCE=1.
   CR<05:03> OUTPUT MODE=4. (FPDP Master)
   CR<06> SYNC ENABLE=0.
   CR<07> CLOCK SELECT=0.
   CR<08> OVERSAMPLING RATIO=1.
   CR<14> VSB_INT_ENABLE=0.
   CR<15> VME_INT_ENABLE=0.

   Configure the ICS-110BL Slave CR as follows:

   CR<00> ACQUIRE=0.
   CR<01> MASTER=0.
   CR<02> ACQUIRE SOURCE=0.
   CR<05:03> OUTPUT MODE=5. (FPDP Slave)
   CR<06> SYNC ENABLE=0.
   CR<07> CLOCK SELECT=0.
   CR<08> OVERSAMPLING RATIO=1.
   CR<14> VSB_INT_ENABLE=0.
   CR<15> VME_INT_ENABLE=0.

4. On the ICS-110BL Master board, set NUM_CHANNELS=31.
   On the ICS-110BL Slave board, set NUM_CHANNELS=7.

5. On the ICS-110BL Master, set NUM_CHANNELS_FPDP=39.

6. On the ICS-110BL Master, set BOARD_ADDRESS=0.
   On the ICS-110BL Slave, set BOARD_ADDRESS=1.

7. Write to the Status/Reset register FIFO RESET bit (SR<07>) on both cards to reset the ADC Data FIFOs.

8. On the ICS-110BL Master, set FPDP_BLOCK_COUNT=0.

9. To start acquisition, change the level of the EXT_ACQ input signal from low to high logic level.

After step 9, the ICS-110BL FPDP mechanism will begin to feed data over the FPDP bus to the FPDP receiver. The ICS-110BL Master will handshake with the receiver in order to ensure that the receiver's buffer does not overflow. This handshake is mediated by means of the SUSPEND* and DVALID* FPDP signals. However, it is the responsibility of the FPDP receiver to keep up with the output data rate of the ICS-110BL two-board system. Descriptions of FPDP signals are given in section 7.5 of this manual.

APPENDICES

7. APPENDICES

7.1 Programming the Internal Clock Generator

7.1.1 Introduction

The frequency of the ICS-110BL internal sampling clock is controlled by programming the Fox F6053A programmable oscillator through the Clock Frequency / Gain register of the VMEbus memory map (see Fig.10 and Fig. 12 above). The device is programmed not in engineering units, but by means of a complex programming word whose construction is described below; a series of control words must also be written to the device. Data is transferred to the device serially from the least significant bit of the ICS-110BL Clock Frequency / Gain register after the user has written the programming word to this register. The word to be programmed to the register includes the following fields.

1. Data to be loaded to programmable oscillator (bits 0 to 26).
2. Length of data in excess of 22 bits (bits 27 to 29). Note that these bits are also all set for control words, even though their length is less than 22 bits.
3. Destination bits (bits 30, 31) - see section 5.16 above.

Automatic calculation of the programming word is provided by the ics110bcalcFoxWord() function and other functions in the 'C' language function library supplied with the optional ICS-110B/ICS-110BL software drivers, available for VxWorks and Solaris 2 environments. These routines generate a 22-bit formatted programming word for the oscillator equivalent to the nearest possible frequency to that supplied as input by the user (in MHz), and also supply the actual frequency represented by the programming word, as an output.

7.1.2 Programming Summary

The oscillator device contains two registers, the Control Register and the Programming Word Register. The programming sequence is as follows:

1. Write to Control Register to configure device and prepare the device to receive the Programming Word.

2. Write Programming Word.

3. Write to Control Register to load Programming Word data into device.

4. Wait at least 10ms for device Voltage Controlled Oscillator (VCO) frequency to stabilize.

5. Write to Control Register to enable device output of new frequency.

7.1.3 Control Register

When writing data to the Control Register, it is necessary to include a Protocol Field to identify the data as Control Register data.

Protocol Field (6 bits) = 0 1 1 1 1 0

It is important that the sequence of four ones contained in the protocol field never be sent except as part of the Protocol Field. Thus, when writing programming word data to the device, it is necessary to use a technique of inserting an extra zero after a run of three ones; this technique is called "bit stuffing", and is described in more detail in section 7.1.4.

The control register contains eight bits, which are defined as shown in Table 7.1.

Table 7.1

Bit No.	Description	Function	Power-up Default
0	Enable Programming Word register to be written by next data	0 = Program Register Disabled 1 = Program Register Enabled to Receive Data	0
1	Internal Output Disable	0 = Output is VCO or f_{REF} 1 = Output is tri-stated	0
2	Internal Multiplexer	0 = Output is VCO frequency 1 = Output is f_{REF}	1
3	Device pin 7 usage	Set to zero only	0
4 - 7	Reserved	Set to 0	0000

Control register data is written to the device starting with bit 0 of the control word, continuing to bit 7 of the control word, and followed by the 6 bits of the Protocol field, for a total of 14 bits.

Note that the default configuration of the device following power-up results in the output being at the frequency of the reference oscillator which is 14.31818 MHz.

7.1.4 Programming Register

The Programming register is written with a 22-bit word describing the required frequency of the output. However, it is essential that programming words do not mimic the Control word Protocol field (see section 7.3.3 above) by containing runs of four consecutive ones. Thus, the device specification requires that a zero must be inserted in the word after each occasion when three one's have been transmitted to the device, regardless of whether the next bit is a 0 or a 1. This procedure is known as "bit stuffing". For this reason, the actual length of a programming word may vary between 22 and 29 bits.
For example, to send this programming data:

Last Bit				First Bit
1111	0101	0111	1110	111111

Transmit this serial bit stream:

Last Bit				First Bit
10111	0101	00111	01110	01110111

The fields of the programming word are described in Table 7.2.

Table 7.2

Field	Bits	# of Bits	Notes
P Counter value (P)	<21:15>	7	MSB (Most Significant Bits)
Duty Cycle Adjust Up (D)	<14>	1	Set to logic 0
Mux (M)	<13:11>	3	
Q Counter Value (Q)	<10:4>	7	
Index (I)	<3:0>	4	LSB (Least Significant Bits)

The frequency of the programmable oscillator f_{VCO}, and the output frequency f_{OUT} are determined by these fields as follows:

$$f_{VCO} = 2 * f_{REF} * (P+3)/(Q+2)$$

where, f_{REF} = Reference frequency (i.e. 14.31818 MHz)

$$f_{OUT} = f_{VCO} / 2^{M}$$

The values of the P and Q parameters must be selected so that f_{VCO} remains between 50 MHz and 150 MHz, inclusive. The value programmed to the M field programs a division register to allow sub-multiples of the VCO frequency to be obtained at the output; the maximum divisor possible is 128.

The **Index field (I)** is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to f_{VCO} rather than to the desired output frequency.)

I	f_{vco} (MHz)
0000	50 – 80
1000	80 - 150

If the desired VCO frequency is exactly 80 MHz, then either index value may be used (since both limits are tested). However, the manufacturer recommends using the setting corresponding to the higher frequency range.

7.1.5 VCO Programming Constraints

There are three primary programming constraints the user must be aware of:

1: 50MHz <= Fvco <= 150MHz
2: 1 <= P <= 127
3: 1 <= Q <= 127

The constraints have to do with the trade-offs between optimum speed with lowest noise, VCO stability and factors affecting the loop equation.

7.1.6 Program Register Example

The following is an example of how to calculate a clock programming word:

Derive the proper programming word for 12.8 MHz clock frequency.

Since 12.8 MHz < 50 MHz, quadruple it to 51.2 MHz
Set M to 010_2
Set I to 0000_2

The result:

Fout = 12.8 = $(2*14.31818*(P+3)/(Q+2))/2^M$

where M = 0, 1, 2, 3, 4, 5, 6, 7
since M = 2: (P+3)/(Q+2) = 1.787936735

The two choices of P and Q giving the nearest to the required frequency are:

P	Q	f_{VCO}	Error (PPM)
56	31	51.19834	32
115	64	51.19834	32
90	50	51.21503	293

Taking the first set of values, i.e. (P,Q) = (56,31):

P = 56 decimal = 0111000 binary = 0(0)111000

Q = 31 decimal = 0011111 binary = 0011(0)111

NOTE: The presence of three ones in a row in both P and Q values causes zero bit-stuff values to be inserted in each. However, it is necessary to examine the values in the previous (I) field before inserting a zero in the least significant bits of the Q value. If the I field had contained a 1 in the most significant position the inserted zero would have been in a different position.

The full programming word, W is therefore:

W = P, D, M, Q, I = 00111000, 0, 010, 00110111, 0000 = 001110000010001101110000 (382370 Hex)

7.1.7 Oscillator Programming Example

The oscillator requires three control words plus the programming word in order to program a new output frequency (see programming sequence given in section 7.1.2 above). The following paragraphs provide an overview of how the control words are build along side the programming word.

All data is written to the oscillator through the Clock Frequency/Gain register. Bits 30 and 31 of the register must be appropriately set to program the required oscillator (sampling clock or FPDP Strobe); these bits are not included in the example given here. An example of programming the oscillator to an initial or new frequency is as follows:

1. Load Control register to enable loading of the Programming word register, enable the output and select the reference frequency for output from the Internal Multiplexer. The Protocol word follows the control word.

	MS Bit	**LS Bit**

Control word	0 1 1 1 1 0 0 0 0 0 0 0 1 0 1
	Protocol Word Control Reg. Data

2. Program the desired output frequency value via a programming word that is 22 bits in length, plus any required bit stuffs. (Up to 27 bits can be obtained with bit-stuffing). The example programming word for 12.8 MHz, calculated in section 7.1.6 above, is shown below.

	MS Bit **LS Bit**
Programming word for 12.8 MHz (0x382370)	0 0 1 1 1 0 0 0 0 0 1 0 0 0 1 1 0 1 1 1 0 0 0 0

3. Load the Control register to disable further loading of the Programming word register. This causes the required output frequency value to be programmed while keeping the output set to the reference frequency for the time being.

	MS Bit **LS Bit**
Control word	0 1 1 1 1 0 0 0 0 0 0 1 0 0
	Protocol Word Control Reg. Data

4. Wait at least 10ms for the VCO to settle to the new frequency. The value will be accurate to within 0.1% within this time.

5. Load the Control register to disable the Internal Multiplexer. This will cause the output to immediately swing to the new frequency.

	MS Bit **LS Bit**
Control word	0 1 1 1 1 0 0 0 0 0 0 0 0 0
	Protocol Word Control Reg. Data

7.2 Analog 1-16 Connector Details

Connector on board: ODD44F4R7NTX
Mating connector: ODD44M..... (consult Manufacturer's data for details)
Manufacturer: Positronics Industries Inc., (417)866-2322

PIN	SIGNAL	PIN	SIGNAL
32	CHANNEL 1-	33	CHANNEL 1+
18	CHANNEL 2-	19	CHANNEL 2+
3	CHANNEL 3-	4	CHANNEL 3+
34	CHANNEL 4-	35	CHANNEL 4+
20	CHANNEL 5-	21	CHANNEL 5+
5	CHANNEL 6-	6	CHANNEL 6+
36	CHANNEL 7-	37	CHANNEL 7+
22	CHANNEL 8-	23	CHANNEL 8+
7	CHANNEL 9-	8	CHANNEL 9+
38	CHANNEL 10-	39	CHANNEL 10+
24	CHANNEL 11-	25	CHANNEL 11+
9	CHANNEL 12-	10	CHANNEL 12+
40	CHANNEL 13-	41	CHANNEL 13+
26	CHANNEL 14-	27	CHANNEL 14+
11	CHANNEL 15-	12	CHANNEL 15+
42	CHANNEL 16-	43	CHANNEL 16+
16	EXTERNAL CALIBRATION INPUT		

Note 1: All other pins are connected to analog ground on the board.
Note 2: External Calibration signal used only when Daughter Board installed.

7.3 Analog 17-32 Connector Details

Connector on board: Positronics ODD44F4R7NTX (see above)

PIN	SIGNAL	PIN	SIGNAL
32	CHANNEL 17-	33	CHANNEL 17+
18	CHANNEL 18-	19	CHANNEL 18+
3	CHANNEL 19-	4	CHANNEL 19+
34	CHANNEL 20-	35	CHANNEL 20+
20	CHANNEL 21-	21	CHANNEL 21+
5	CHANNEL 22-	6	CHANNEL 22+
36	CHANNEL 23-	37	CHANNEL 23+
22	CHANNEL 24-	23	CHANNEL 24+
7	CHANNEL 25-	8	CHANNEL 25+
38	CHANNEL 26-	39	CHANNEL 26+
24	CHANNEL 27-	25	CHANNEL 27+
9	CHANNEL 28-	10	CHANNEL 28+
40	CHANNEL 29-	41	CHANNEL 29+
26	CHANNEL 30-	27	CHANNEL 30+
11	CHANNEL 31-	12	CHANNEL 31+
42	CHANNEL 32-	43	CHANNEL 32+

Note 1: All other pins are connected to analog ground on the board.

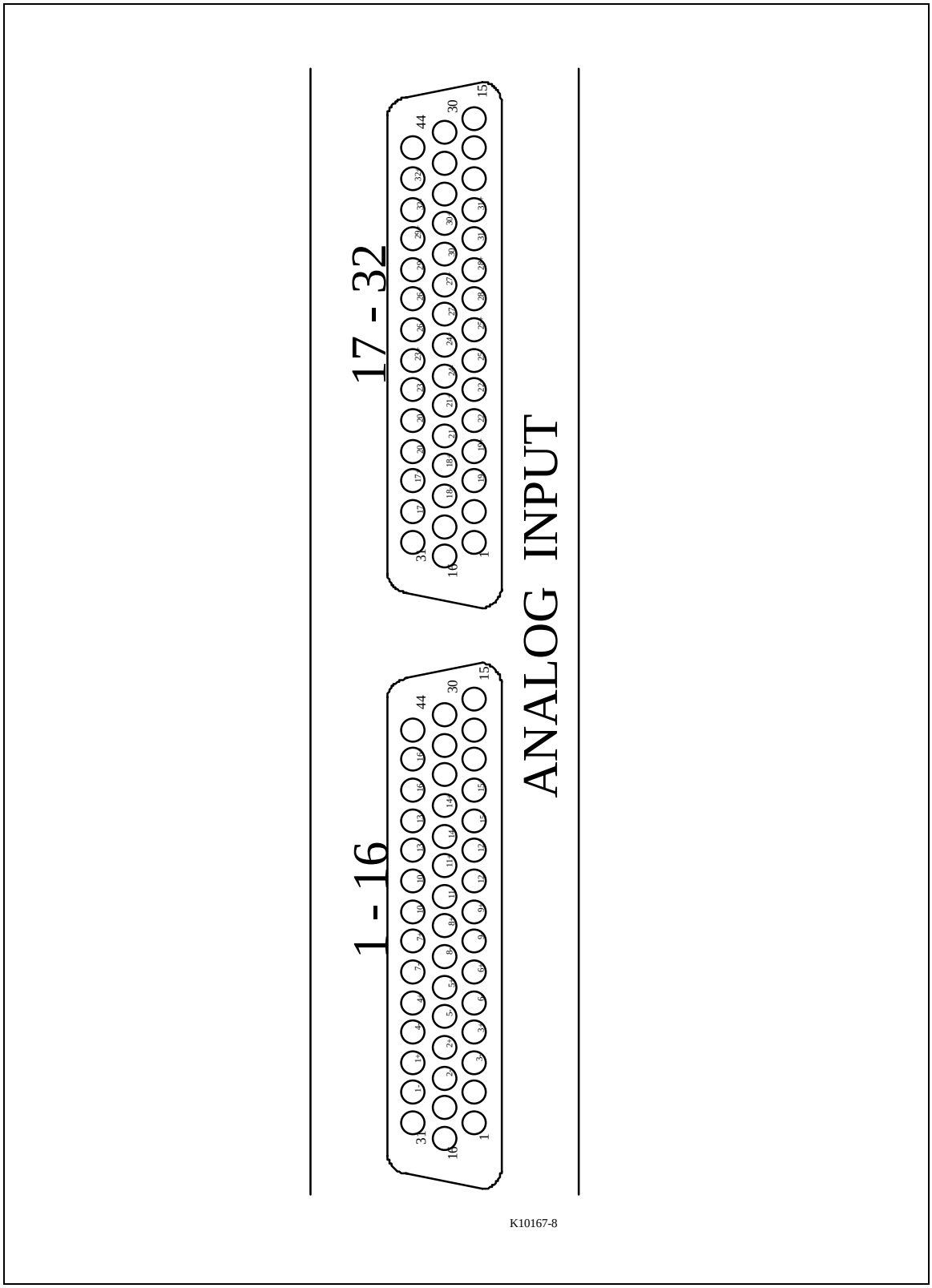


Figure 13 - ICS-110BL Analog Connector Pinout

7.4 P4 Local Bus Connector Details

Connector on board: 501-2007ES
Mating connector: 622-2001 (Non-polarized)
622-2041 (Polarized)
Manufacturer: Thomas & Betts, (803)676-2900

PIN	DESCRIPTION
1	CLOCK+ (TTL+)
2	CLOCK- (TTL-)
3	GND
4	FRAME_TC
5	ACQUIRE_SYNC
6	BLOCK_SYNC
7	EXT_CLK+ (TTL+)
8	EXT_CLK- (TTL-)
9	EXT_ACQ+ (TTL+)
10	EXT_ACQ- (TTL-)
11	GND
12	DATA_CLOCK+ (PECL+)
13	DATA_CLOCK- (PECL-)
14	BOARD_ADDR0
15	BOARD_ADDR1
16	BOARD_ADDR2
17	BOARD_ADDR3
18	BOARD_ADDR4
19	DATA_CLOCK_EN
20	NC

7.5 P5 FPDP Details

Connector on board:	8831E-080-170L (KEL Corporation)
	P50E-080P1-SR1-TG (Robinson-Nugent)
Mating connector:	8825E-080-175 (with strain relief)
	8825R-080-175 (without strain relief)
	P25E-080S-TG (Robinson-Nugent)
Manufacturer:	KEL Corporation, (408) 720-9044
	Robinson-Nugent (812) 945-0211

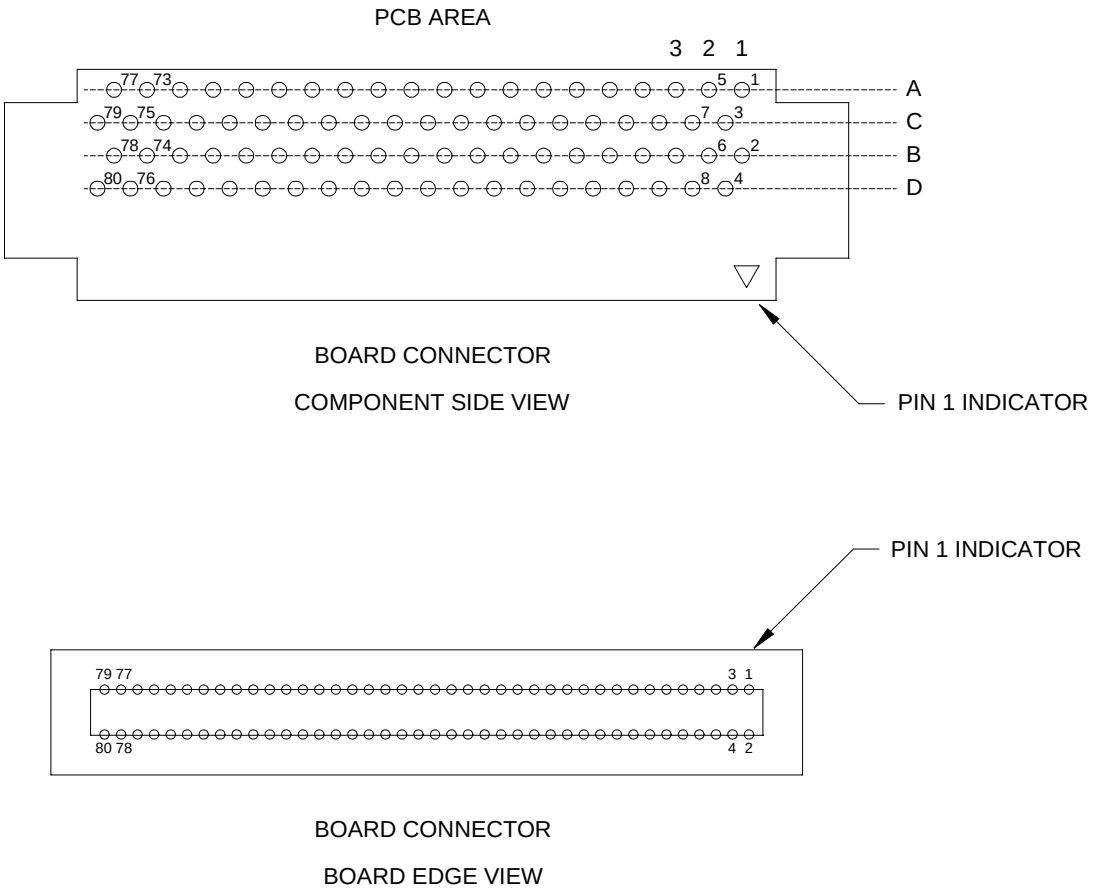
Note 1: The ICS-110BL uses 24 bits of the 32 bit data bus width available on the FPDP (D31:D00). The bits used are D31:D08. The ICS-110BL data assignments are shown in brackets (d23:d00) in the pinout list. The unused pins are driven low.

Note 2: When connecting one or more ICS-110BL boards to a DSP board, the user should be aware that some DSP implementations have the FPDP connector inverted. For the ICS-110BL, the connector index mark appears at bottom right hand side of the connector when the board is mounted vertically in a chassis; cable conductor #1 is adjacent to this mark. In order to prevent the need to fold the FPDP ribbon cable, the cable is supplied with the DSP connector inverted. The pinouts at the DSP FPDP connector are therefore reversed, compared to the ones given below. In other words, at the DSP connector pin 1 connects to pin 80 at the ICS-110BL, while pin 79 connects to pin 2 at the ICS-110BL.

The FPDP is a high performance 32 bit parallel interface configured with a ribbon cable to connect boards or systems together. The simple and well-defined physical and electrical interface provides the basis for integrating many different types of boards and sub-systems. The maximum clock rate of the ICS-115 FPDP interface is 20 MHz, providing a sustained data rate of up to 80 MBytes/s. Since multiple FPDP buses are possible, the total data path bus bandwidth may be scaled to system requirements.

7.5.1 FPDP Connector Pin Assigments

The FPDP interface connector is an 80-pin high density connector available from KEL and Robinson-Nugent. The connector on the board is a KEL 8831E-080-170L or R-N P50E-080P1-SR1-TG and is shown in Figure 14. The mating cable connector is a KEL 8825E-080-175S or R-N P25E-080S-TG, and takes a single ribbon cable of 80 conductors on 0.025 inch pitch. Table 7.3 defines the connector pin assignments.



Connector row and column designations are shown outside connector outline.

Cable numbers are shown inside connector outline.

FPDP BOARD-MOUNTED CONNECTOR
KEL 8831E-080-170L
or
Robinson-Nugent P50E-080P1-SR1-TG

K10128B2

Figure 14 - FPDP Interface Connector

TABLE 7.3 ICS-110BL FPDP P5 Connector Pin Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	2	STROBE	3	GND	4	GND
5	GND	6	GND	7	NRDY*	8	GND
9	DIR*	10	GND	11	RESERVED	12	GND
13	SUSPEND*	14	GND	15	GND	16	GND
17	PIO2	18	GND	19	PIO1	20	GND
21	RESERVED	22	GND	23	RESERVED	24	GND
25	PSTROBE	26	GND	27	PSTROBE*	28	GND
29	SYNC*	30	GND	31	DVALID*	32	GND
33	D31(d15)	34	D30(d14)	35	GND	36	D29(d13)
37	D28(d12)	38	GND	39	D27(d11)	40	D26(d10)
41	GND	42	D25(d09)	43	D24(d08)	44	GND
45	D23(d07)	46	D22(d06)	47	GND	48	D21(d05)
49	D20(d04)	50	GND	51	D19(d03)	52	D18(d02)
53	GND	54	D17(d01)	55	D16(d00)	56	GND
57	D15	58	D14	59	GND	60	D13
61	D12	62	GND	63	D11	64	D10
65	GND	66	D09	67	D08	68	GND
69	D07	70	D06	71	GND	72	D05
73	D04	74	GND	75	D03	76	D02
77	GND	78	D01	79	D00	80	GND

7.5.2 FPDP Signals

A description of FPDP signals is given in Table 7.4.

Further details concerning the FPDP design are given in ICS INPUT Technical Note No.16 and the VITA 17 draft standard Rev.1.7, which is available from the factory or from the ICS Web site at:

www.ics-ltd.com/technotes_white_papers.html

TABLE 7.4 ICS-110BL FPDP Signal Descriptions

Signal/s	Signal Name	Description
D31:00	Data Bus	32 bit data bus driven by the data source.
DIR*	Data Direction	The data source asserts DIR* low.
DVALID*	Data Valid	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each data sample.
STROB	Data Strobe	STROB is a free running clock supplied by the data source. The receiving end should clock the data with the rising edge of STROB.
NRDY*	Not Ready	NRDY* is asserted by the receiver when it is not ready to receive data. The data source must sample this signal until the receiver brings it high, at which time the transfer can commence. Since NRDY* is asynchronous to STROB, the data source should double-synchronize to it before sampling its state; this avoid metastability problems.
PIO1,PIO2	Prog. I/O	The PIO signals are programmable I/O lines for user-defined functions. They can be configured as inputs or outputs.
PSTROBE	+ PECL Data Strobe	This signal along with PSTROBE* are generated by the data source as an optional differential PECL (Positive Emitter-Coupled Logic) data strobe. PSTROBE is the positive version of the differential clock and has the same polarity as STROB. For high data rate applications, the differential PECL data strobe should be used instead of STROB. The user must configure the board appropriately; see section 4.2.
PSTROBE*	- PECL Data Strobe	This signal is the negative version of the differential PECL data strobe.
RESERVED		Do not connect to reserved signals.
SUSPEND*	Suspend Data	SUSPEND* is generated by the receiver to inform the data source of a pending FIFO overflow condition. The data source is allowed as many as 16 cycles before suspending the transfer. Since SUSPEND* is asynchronous to STROB, the data source should be double-synchronized to it before sampling its state; this avoids metastability problems.
SYNC*	Sync Pulse	The data source can provide a sync pulse to the receiver to synchronize data transfers. The receiver waits for the sync pulse before accepting data. The receiver starts accepting data on the first Data Valid period following the sync pulse.