ICS-150B

OPERATING MANUAL

Interactive Circuits And Systems Ltd.
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1 INTRODUCTION

The ICS-150B is a 4-channel 40 MHz 12-bit VMEbus analog input and output board which offers multiple options for moving data at high speeds to and from the board. It replaces the earlier ICS-150 product which had to be redesigned due to obsolescence of some components. The ICS-150B is designed to be fully software-compatible with the ICS-150, so that ICS-150 software drivers may be used with the ICS-150B. However, some performance parameters of the ICS-150B differ from those of the ICS-150; these are described in detail in section 2.3 of this manual.

The ICS-150B board has been optimized to solve high-speed data acquisition problems which also demand high precision and ease of system integration. The ICS-150B is ideal for applications in:

- Radar
- Communications & EW
- Ultrasound
- Imaging, and
- Test and Measurement

The ICS-150B board significantly advances the state-of-the-art by combining the ultimate in analog and digital technologies in a single 6U size VMEbus board. The ICS-150B offers not only high speed and high performance, but also provides the ultimate in user convenience. A list of the major features of the board are listed below:

- 4 separate 12-bit Analog to Digital Converters (ADCs)
- 4 separate 12-bit Digital to Analog Converters (DACs)
- The ADCs and DACs can operate at sampling rates up to 40 MHz/channel for 2 channels or 20 MHz/channel for 4 channels
- Continuous or one-shot modes of operation
- Large dual-ported sample memories (2 MSample for ADC and 2 MSample for DAC)
- Internal/External clock and trigger
- Internal ADC or DAC clocks are independently programmable in steps of better than 8000 Hz
- VME64 Master/Slave DMA interface
- VSB32 Master/Slave interface
- Programmable length VMEbus and VSB interrupts
- Simultaneous VMEbus and VSB operations
- Two separate ANSI/VITA 17 Front Panel Data Ports (FPDPs) for ADC and DAC data.
- The FPDPs are compatible with the front-panel ports of Mercury, SKY, CSPI and many other array processor boards as well as other ICS boards.

1.1 References

1. OpenBus Interface Components, SCV64 User Manual, Document No. 891078.MD301.01, Tundra Semiconductor (formerly Newbridge Microsystems), 1993.

2. VxWorks Device Driver Manual for the ICS-150B, Document No. E10433, Interactive Circuits and Systems Ltd.

3. SunOS Device Driver Manual for the ICS-150B, Document No. E10430, Interactive Circuits and Systems Ltd.

4. ANSI/VITA 17 Front Panel Data Port Standard, American National Standards Institute, 1997.

2 GENERAL DESCRIPTION

Figure 1 shows a simplified block diagram of the ICS-150B board. The board uses 4 12-bit 20 MHz ADCs (Analog Devices AD6640) and 4 12-bit 40 MHz DACs (Analog Devices AD9713B) to provide simultaneous sampling and generation at rates up to 20 MHz/channel for four channels. The large bandwidth and low aperture jitter of the ADCs support time-multiplexed operation which can be used to double the sampling rate to 40 MHz/channel for two channels.

ADC data is buffered in the dual-ported memories for subsequent read-out via the FPDP, VMEbus or VSB. The sampling clock and the trigger can be either internal or external. The internal ADC clock is user programmable in steps of better than 8000 Hz. The ADCs can be operated either in one-shot or in continuous mode. In the one-shot mode (also called capture mode), 2N number of samples are acquired for each channel following the application of a trigger. In continuous mode, the swing buffer swaps every N samples. In both cases, N is fully programmable. An additional acquisition mode, the PRF mode, is available with the swing buffer option. In the PRF mode, a fixed number of samples (selectable by number of 32-bit words in buffer: 256, 512, 1024, 2048, 4096, 8192, or 16384 - see section 5.22) is converted for each application of the trigger. This feature is supported in both the one-shot and continuous modes of operation, and is intended for use when individual data captures are of short duration, and multiple acquisitions are performed before the data is read.

The DAC data can also be supplied either from the VMEbus, VSB or FPDP. The DAC clock can be either internal or external. Here again, the internal clock is programmable (independent of the ADC clock) in steps of better than 8000 Hz. The DACs can also be operated in either continuous, one-shot and loop modes (latter mode only available with swing buffer option). In the loop mode of operation, N data samples for each channel are repeatedly applied to the DAC from the DAC memories, where N is fully programmable. Unlike continuous mode operation, fresh data is not loaded by the user at each cycle of the swing buffer.

To allow fast transfer of ADC and DAC data, the ICS-150B board includes a VME64 interface capable of in excess of 70 MByte/s (i.e. A64/D64 bus cycles), a 40 MByte/s VSB32 interface, and two separate 40 MHz, 32-bit front-panel interfaces which are compatible with the ANSI/VITA 17 Front Panel Data Port (FPDP) standard. The VME64 interface circuitry uses the Tundra Semiconductor SCV64 chip to support a BLT / MBLT (Multiplexed BLock Transfer) master/slave interface. The A32, A24 and D32 address modes are supported. The A32/D32 VSB interface supports block transfer. The ICS-150B board can generate separate VMEbus and VSB interrupts in order to support simultaneous VMEbus and VSB operations. An interrupt can be generated at any user programmed interval (number of samples). All power requirements of the ICS-150B are satisfied with standard VMEbus voltages.

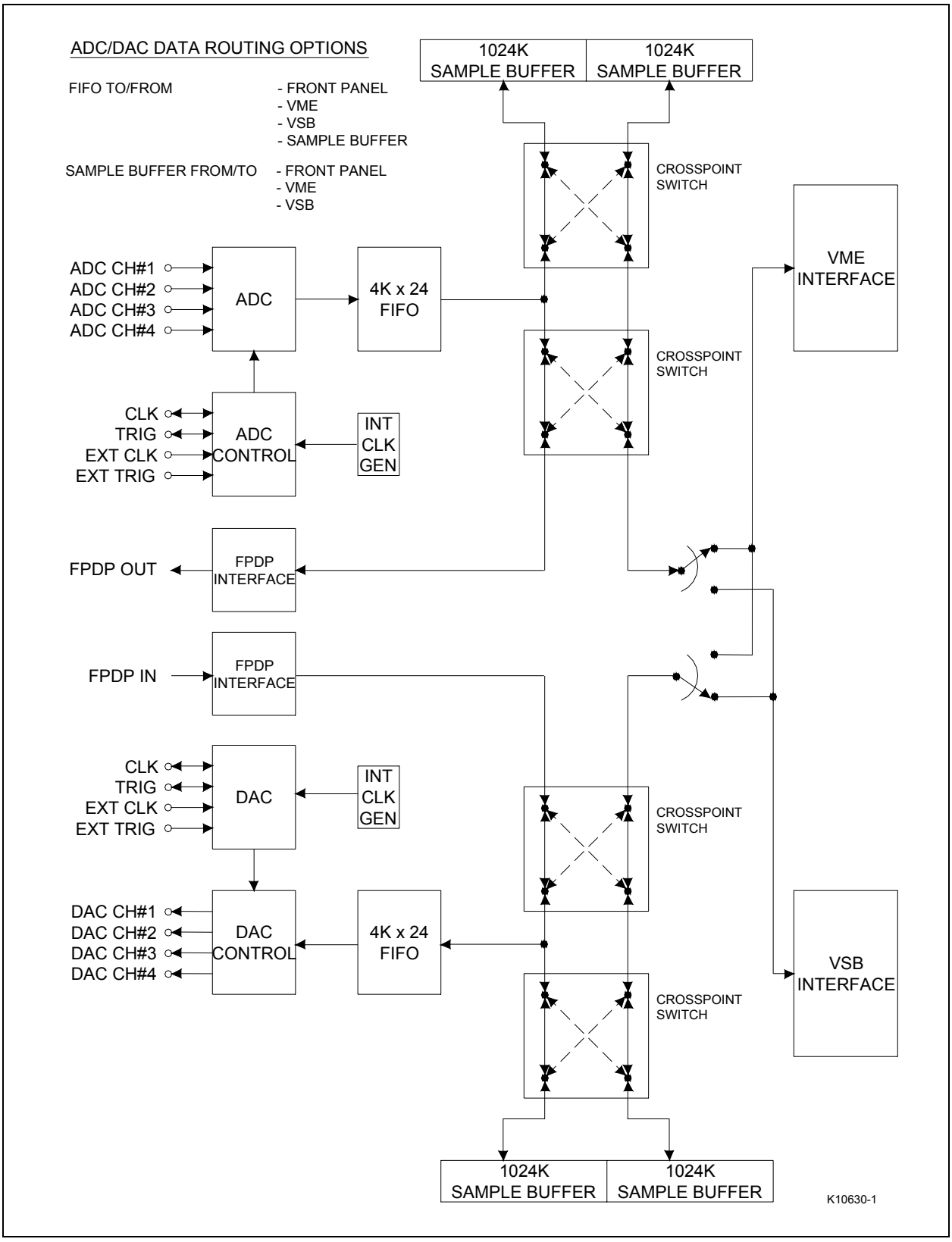


Figure 1 - ICS-150B Block Diagram

2.1 Ordering Options

The ICS-150B board is available in 3 different versions . Software device drivers are also available:

Model No.	Description
ICS-150B-AM	Provides 4 ADCs only, and 2MSamples (3Mbytes) of swing buffer memory in addition to FIFO memory.
ICS-150B-DM	Provides 4 DACs only, and 2MSamples (3Mbytes) of swing buffer memory in addition to FIFO memory.
ICS-150B-ADM	Includes both ADCs and DACs and 2MSamples (3Mbytes) of swing buffer memory for each.
DRV-150-SoS	SunOs software device driver for ICS-150 / ICS-150B.
DRV-150-VxW	VxWorks software device driver for ICS-150 / ICS-150B.
DRV-150-SSS	Solaris 2.x software device driver for ICS-150 / ICS-150B.

2.2 Board Specifications

Analog to Digital Converter Section

No. of Analog Input Channels:	4
Analog Connector Type:	SMB Coaxial
Input Impedance:	50 Ohm
Full Scale Input:	± 1.024 Volts
Input Signal Bandwidth:	>70 MHz
Max. Sampling Rate:	40 MHz/ch. for 2 channels 20 MHz/ch. for 4 channels
Sampling:	Rising edge of sample clock
External trigger:	Sampling occurs on first rising clock edge following rising edge of external trigger
Sample Conversion Time:	3 cycles of sample clock (4 channel mode), 6 cycles of sample clock (2 channel mode), plus FIFO and bus access times.
Dynamic Range (S/N+D):	>65dB @ 20 MHz >62dB @ 40 MHz
Inter-channel Cross-talk:	<-65dB
On-board Storage:	2Msamples (3 Mbytes)

Digital to Analog Converter Section

No. of Analog Outputs:	4
Analog Connector Type:	SMB Coaxial
Output Impedance:	50 Ohm
Full Scale Output:	± 0.920 Volts
Max. Output Conversion Rate:	40 MHz/ch. for 2 channels 20 MHz/ch. for 4 channels
Conversion:	Rising edge of sample clock
External trigger:	Conversion occurs on first rising clock edge following rising edge of external trigger
Sample Conversion Time:	1 cycle of sample clock, plus FIFO and bus access times.
Dynamic Range (S/N+D):	>63dB @ 20 MHz >60dB @ 40 MHz
Inter-channel Crosstalk:	<-65dB
On-board Storage:	2MSamples (3Mbytes)

General

VMEbus Interface:	A64/A32/A24 D64/D32 MBLT Master/Slave
VSB Interface:	A32/D32 BLT Master/Slave
Front-Panel Interface:	ANSI / VITA 17 Front Panel Data Port (FPDP) Repeating Frame Data mode only. Independent ports for ADC and DAC sections.
Environmental:	Temp: -0º- 50ºC operating (at entry point of forced air, approximately 490 LFM) -40º - +85ºC Storage Humidity 90% non-condensing
Power:	+5V @ 2.5 Amps for ICS-150B-AM @ 2.5 Amps for ICS-150B-DM @ 3.5 Amps for ICS-150B-ADM +12V @ 0.25 AMPS for ICS-150B-AM @ 0.25 AMPS for ICS-150B-ADM -12V @ 0.1 AMPS for ICS-150B-AM @ 0.1 AMPS for ICS-150B-ADM

*Specifications are subject to change without notice

2.3 ICS-150 / ICS-150B Differences

The ICS-150B is designed to be as closely compatible as possible with the earlier ICS-150 product. In many cases it will be possible to replace ICS-150 boards by ICS-150B boards and achieve similar or improved performance with no changes required in software.

The following changes were made to the design because of obsolescence of components, but do not affect how the board is used:

1. The ADC converter part was changed from AD9022B to AD6640.
2. The DAC converter part was changed from AD9713B to AD9754.
3. All versions of the ICS-150B include the extended memory size, i.e. 2Msamples for ADC and 2Msamples for DAC.

The following changes were made, and do affect how the board is used:

1. The switch layout has changed. This is described in detail in section 4 of this manual.
2. There are no longer any switches that select between ADC 2-channel and 4-channel modes. This is now done entirely under software control.
3.
4. The LED indicators have been moved to a new location on the board, and the ordering sequence has been inverted (see section 3.9).
5. The functions of the ADC Running and DAC Running LEDs have been exchanged in the sequence of 8 LEDs (see section 3.9).

3 DETAILED DESCRIPTION

3.1 ADC Section

The ICS-150B board uses 4 12-bit ADCs (Analog Devices's AD6640) each of which is capable of operating at up to 40 MHz sampling rate. Two channel mode of operation must be selected when operating with sample rates above 20MHz. This is done by means of the Channel Mode bit in the ADC Control register. The full scale input signal level is ± 1.024v, with an input impedance of 50Ω. Four separate SMB coaxial connectors (marked A1, B1, A2, and B2) are provided on the front-panel for applying the single-ended analog input signals (see Figure 2).

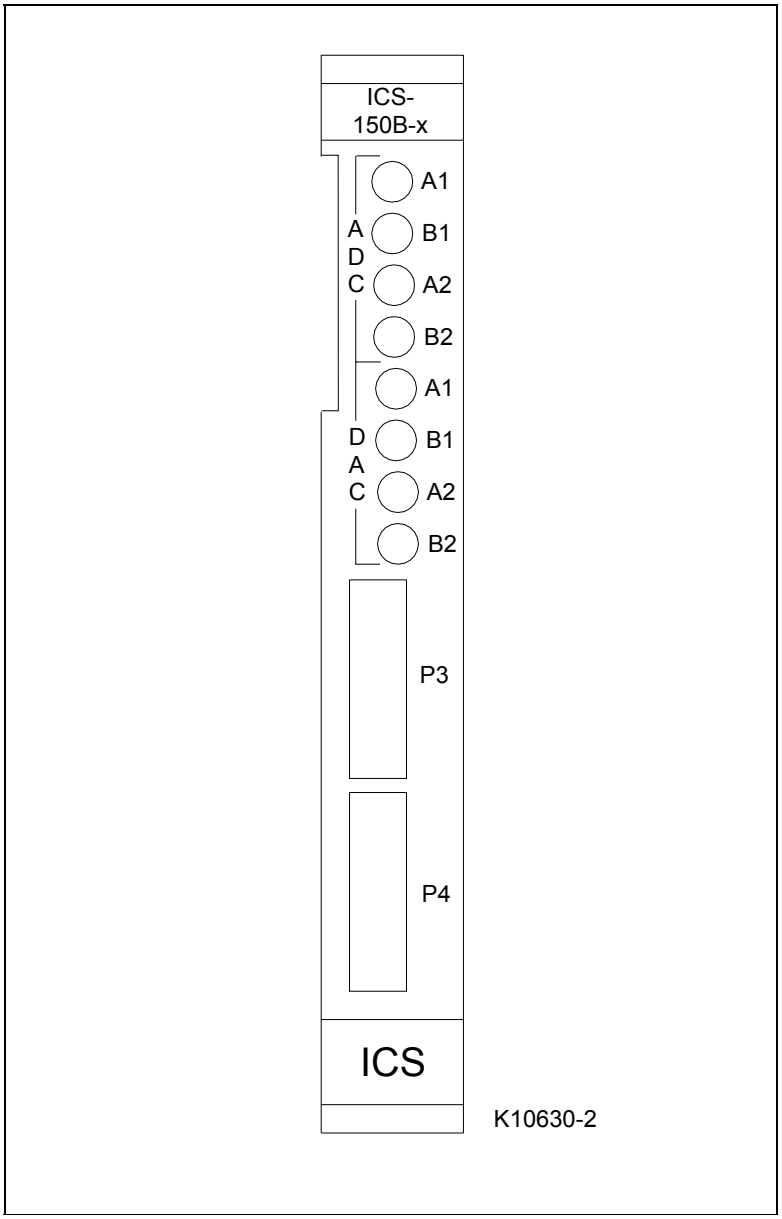


Figure 2 - ICS-150B Front Panel Layout

In the 4-channel 20 MHz mode of operation the 4 ADC outputs are combined in two successive 24-bit words for storing into the ADC FIFO. The ICS-150B board also supports 40 MHz 2-channel operation. The two analog inputs are connected to the SMB connectors marked A1 and A2. The ICS-150B board has been optimized to support 40 MHz operation by using state-of-the-art devices and design techniques. In particular:

(i) the analog front-ends, including the track-and-hold circuitry contained in the ADCs, have large bandwidth (the large signal bandwidth is over 70 MHz);

(ii) closely matched ADCs are used to the extent possible;

(iii) the jitter and skew of the sampling clocks are kept to less than 100 ps.

In the 40MHz 2-channel mode of operation, the outputs of two ADCs (A1 and A2) are combined to produce a 24-bit word which is stored in the ADC FIFO.

In both 2-channel and 4-channel modes, multiplexed data from the ADCs is written to the 8kSample ADC FIFO. Data from this FIFO can then be directed to the swing buffer, the VMEbus interface, the VSB interface, the FPDP, or the daughter board. A programmable interrupt is generated on the FIFO half full condition for continuous operation, and on the FIFO full condition for the one-shot mode. This interrupt can be configured to generate either a VMEbus interrupt or a VSB interrupt.

If the swing buffer is used, the data from the swing buffer can be sent to the VMEbus interface, VSB interface, or the FPDP. In both one-shot and continuous modes of operation, the size of both banks (i.e. number of samples) is programmable by means of a parameter which the programmer writes to the ADC Buffer Length register. For continuous mode operation, the value of this parameter determines when the banks of the swing buffer swap. An interrupt is generated at this point, if enabled. For one-shot operation, the interrupt is generated when both banks have been filled with a number of samples equal to the programmed buffer length parameter.

If the swing buffer is used, an additional ADC feature called PRF mode is available in conjunction with both one-shot and continuous modes of operation. The user must program the ADC PRF Length Register with a number representing the number of samples to be captured at each assertion of the trigger (either internal of external). However, this value is expressed in terms of the number of 32-bit words captured in the swing buffer; this value may be any integer power of 2 between 256 and 16384. This value is independent of the buffer length parameter which is programmed in the ADC Buffer Length register. Since an interrupt is generated when the buffer length parameter equals the number of samples captured, an interrupt may be generated after a single PRF mode capture, or after multiple PRF capture sequences, thereby reducing bus loading. The user must allow a minimum of 3.2 microseconds between the end of one PRF acquisition cycle and the next assertion of the trigger signal to allow the ICS-150B to be internally primed.

3.2 DAC Section

The ICS-150B board uses 4 12-bit DACs (Analog Devices's AD9754) each of which is capable of operating at an update rate up to 40 MHz. The full scale output signal level is ± 0.920v, with an output impedance of 50Ω. Four separate SMB coaxial connectors (marked A1, B1, A2, and B2) are provided on the front-panel with the single-ended analog output signals.

In the 4-channel 20 MHz mode of operation two successive 24-bit words from the DAC FIFO are applied as four 12 bit words to the DACs. Since the ICS-150B input/output circuitry is limited to providing a 24 bit data stream at 40 MHz, only two channels of data are available in this mode. In the 2-channel 40MHz mode of operation, the DACs driving outputs A1 and B1 are supplied with the same data, as are the DACs driving A2 and B2. The selection of 2-channel or 4-channel mode is made by means of the Channel Mode bit in the DAC Control register. As with the ADC section, the timing relationship between channels is precisely maintained using high-precision phase-lock loop circuitry.

The DAC data is supplied by the 8kSample DAC FIFO. Data to this FIFO can be supplied by the swing buffer, the VMEbus interface, the VSB interface, or the FPDP. A programmable interrupt is generated on the FIFO half empty condition for continuous mode and loop mode operation, and on the FIFO empty condition for the one-shot mode. This interrupt can be configured to generate a VMEbus interrupt or a VSB interrupt.

If the swing buffer is used, the data for the swing buffer can be supplied from the VMEbus interface, VSB interface, or the FPDP. In both one-shot and continuous modes of operation, the size of both banks (i.e. number of samples) is programmable by means of a parameter which the programmer writes to the DAC Buffer Length register. For continuous mode operation, the value of this parameter determines when the banks of the swing buffer swap. An interrupt is generated at this point, if enabled. For one-shot operation, the interrupt is generated when both banks have been emptied by a number of samples equal to the programmed buffer length parameter.

3.3 Clock/Trigger Options

The ICS-150B offers a number of clock and trigger options. Both the ADC and DAC have internal clock generators that offer independent clock generation with a programming resolution of about +/-4kHz over the 3.75 MHz to 40 MHz range. The ADC and DAC can also be clocked from the same internal source by setting a switch option. The clock can be independently selected between internal and external for the DAC and ADC sections. The user-supplied external clocks are connected via the front panel connector. If an external clock is supplied, the user must supply a continuous clock of the desired clock frequency in order to maintain frequency lock of the ICS-150B's PLL (Phase-Locked Loop) clock circuitry.

The ADC and DAC sections have independent triggers, which can be programmed to be internal or external. The external trigger is a rising-edge TTL signal supplied by the user on the front panel connector, and must be at least one clock cycle long. The trigger is internally synchronized to the sampling clock by the ICS-150B and acquisition/conversion is initiated on the next rising edge of the sampling clock after the application of the trigger.

Both external clock and trigger signals must conform to standard TTL levels and drive capability. The relevant signals are listed in section 4.6.

The ICS-150B provides the ability to synchronize multiple boards in a system. This is done by bussing the front panel local bus. Details of this are given in section 3.7 below.

Since the on-board PLLs for both the ADC and DAC sections require a minimum sampling rate of 3.75 MHz, the ICS-150B allows the user to decimate either data stream in order to achieve data sampling and conversion rates below this figure. On the ADC side, data is only written to storage every N samples, where N is a value programmed into the ADC Decimation register. Similarly, On the DAC side, data is only read from storage every N samples, where N is a value programmed into the DAC Decimation register. Both ADC and DAC decimation values are independently programmable between 1 and 256. This provides a minimum effective sampling and conversion rate of 14.6 kHz.

3.4 Modes of Operation

The ICS-150B provides many options with regard to operating modes, data buffering and data paths to and from the board. The destination for the ADC data can be VMEbus, VSB or the FPDP. Independent of the data destination, data buffering can be chosen from the ADC FIFO, the Swing Buffer, or the optional Daughter Board. The Swing Buffer and FIFO memories support both Capture and Continuous modes, but the daughter board option supports only the Capture mode of operation. PRF mode is supported only with the Swing Buffer memory option for both the Capture and Continuous modes.

3.5 VMEbus Interface

The ICS-150B implements a VMEbus Master/Slave A64/D64 A32/D64 A24/D32 interface using the Tundra Semiconductor SCV64 integrated circuit. Master BLT (Block Transfer) and MBLT (Multiplexed Block Transfer) cycles are also supported. On power-up, default A32 and A24 slave images are loaded by the SCV64 with base addresses determined from on-board switches (see section 4 for details of switch settings). The VMEbus Host can configure the SCV64 internal registers by accessing the SCV64 register block using either of these slave images. Note that the slave base address of the SCV64 can be reprogrammed by the host by loading appropriate values in the SCV64 VMEbus Base Address Register.

The SCV64 can be configured to perform VMEbus Master Block Transfers by loading the SCV64 internal registers with the appropriate VMEbus Start Address, the local (to the ICS-150B) start address, and the transfer count. After the DMAGO bit in the SCV64 Control Register is set, the SCV64 will acquire the VMEbus and perform the requested transfer, freeing the host for other tasks. Note that the VMEbus specification limits block transfers to a maximum of 256 bytes, however, the ICS-150B design does not prevent transfers of larger blocks. Transfers can be either D64 or D32. D64 transfer rates as high as 70 MB/s can be attained. A programmable VMEbus interrupt is available to indicate that a transfer has been completed. Programmable interrupts are also available for the VSB Transfer Complete, ADC Ready and DAC Ready conditions.

3.6 VSB Interface

The ICS-150B implements a VSB Master/Slave A32/D32 BLT interface. On Power-Up, the ICS-150B's VSB slave image is disabled. The VMEbus host loads the ICS-150B with the VSB base address, and sets the Slave Enable bit in the ICS-150B VSB control register. For VSB Master BLT operation, the VMEbus Host loads the ICS-150B VSB Start Address register and the VSB Count register, and then sets the VSB GO bit in the VSB control register. The ICS-150B then arbitrates for the VSB, and performs the requested transfer. Note that very long transfers can be achieved on the VSB. A programmable VMEbus interrupt is available to indicate that a transfer has been completed. The ICS-150B can also generate VSB interrupts for the ADC Ready and DAC Ready conditions. Note that the ICS-150B VSB interface is a "Respond" type device. It has no Broadcast or Broadcall facility.

3.7 Cascading Multiple Boards

In common with other ICS products, the ICS-150B design provides simultaneous sampling not only on all channels on one board, but also on all channels across multiple boards. In order to achieve multiple board synchronization, one board is designated as the "FPDP Master" and provides clock and trigger signals to the other (slave) boards in the group. These signals are wired on the P3 FPDP connector on the front panel of the ICS-150B. All boards to be synchronized must be located in the same VMEbus chassis in order not to violate signal timing requirements. Programming of master/slave status is done using register VMECR (see section 5.7).

As with single boards, either internal or external clock and trigger signals may be used with multiple board configurations. In the case of external clock and/or trigger, the user supplies the external signal/s only to the master, which in turn distributes the clock and trigger to the slaves. The ICS-150B's PLL clock circuitry allows multiple board systems to have simultaneous triggering (+/- 0 samples) and less than 1.5 ns board to board sampling skew. See also section 3.8.2 below.

The signals that must be bussed for multiple board operation are listed in section 4.9.

3.8 FPDP Interface

Two connectors on the front panel of the ICS-150B, designated P3 and P4, are compatible with the ANSI/VITA 17 Front Panel Data Port (FPDP) Interface. Tables 3.1 and 3.2 list the pin assignments for these connectors. FPDP is an industry standard interconnection for high speed board to board or system to system data transfer, using ribbon cable to connect between front panel connectors. This interface standard has gained acceptance in the industry for use in a broad range of signal processing applications. It is directly compatible to CSPI's SC130/P100, Mercury's RINJ-T/ROUTJ-T, SKY's SKYburst 160 and Ixthos' IXI2S32-F interfaces and is also supported by a wide range of products from other manufacturers.

The maximum FPDP strobe (clock) frequency that may be used is 40 MHz, providing a sustained data rate of up to 160 MBytes/s. Note that ICS-150B FPDP ports do not support the connection of more than one ICS-150B on each FPDP cable for transmission of data to or from a DSP device.

3.8.1 FPDP Connector Pin Assignments

The FPDP interface connector is an 80-pin high density connector manufactured by KEL. Figure 3 shows the connector appearance and part numbers. The mating cable connector is a KEL 8825E-080-175S, and takes a single ribbon cable of 80 conductors on 0.025 inch pitch. Tables 3.2 and 3.3 define the connector pin assignments. The corresponding pin assignments on the ribbon cable are A1,B1,C1,D1,..., starting from the connector index mark.

Please note that the FPDP specification defines 32 bits of data, and the listing of data bit connections in the tables reflects this. However, since the ICS-150B is a 12-bit system, the mapping of ICS-150B data bits to FPDP pins is shown thus:

D31(d23),

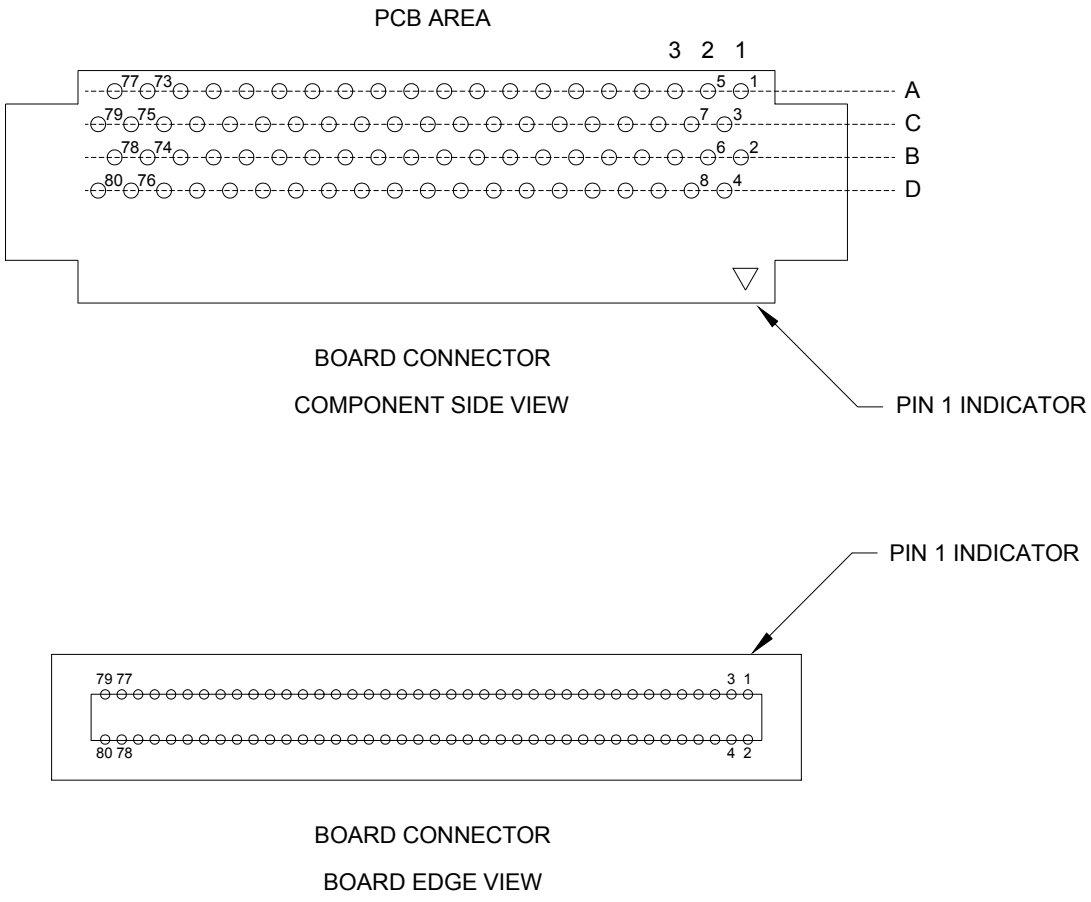
where D31 is the FPDP description for the most significant bit of data, and d23 is the most significant bit of ICS-150B data when two 12-bit words are driven onto the FPDP in parallel. In some cases, unused data bit connections are used to carry clock and trigger signals, and the names of these signals are shown in brackets as for the above example.

The connectors used are given in Table 3.1 below.

TABLE 3.1 – FPDP Connector Part Numbers

Connector on board	KEL 8831E-080-170L
Mating connector	KEL 8825E-080-175 (with strain relief)
	KEL 8825R-080-175 (without strain relief)
	R-N P25E-080S-TG
Manufacturers	KEL Corporation, (408) 720-9044
	Robinson-Nugent, (812) 945-0211

Note: When connecting the ICS-150B to a DSP board, the user should be aware that some DSP implementations have the FPDP connector and pinouts inverted. For the ICS-150B, the connector index mark appears at the bottom right hand side when the board is installed in the normal vertical orientation; cable conductor #1 is adjacent to this mark. In order to prevent the need to fold the FPDP ribbon cable when connecting to a DSP board with an inverted FPDP configuration, the cable must have connectors that are inverted with respect to one another. The pinouts at the DSP FPDP connector are therefore reversed, compared to the ones given below. In other words, at the DSP, connector pin 1 connects to pin 80 at the ICS-150B, while pin 79 connects to pin 2 at the ICS-150B.



Connector row and column designations are shown outside connector outline.

Cable numbers are shown inside connector outline.

FPDP BOARD-MOUNTED CONNECTOR
KEL 8831E-080-170L
or
Robinson-Nugent P50E-080P1-SR1-TG

K10128B2

Figure 3 – FPDP Interface Connector

TABLE 3.2 - ICS-150B FPDP P4 ADC Data connector pin assignments

PIN		PIN		PIN		PIN	
1	GND	2	STROBE	3	GND	4	GND
5	GND	6	GND	7	NRDY*	8	GND
9	DIR*	10	GND	11	RESERVED	12	GND
13	SUSPEND*	14	GND	15	GND	16	GND
19	PIO2	20	GND	19	PIO1	20	GND
23	RESERVED	24	GND	23	RESERVED	24	GND
27	PSTROBE+	28	GND	27	PSTROBE-	28	GND
31	SYNC*	32	GND	31	DVALID*	32	GND
33	D31(d23)	34	D30(d22)	35	GND	36	D29(d21)
37	D28(d20)	38	GND	39	D27(d19)	40	D26(d18)
41	GND	42	D25(d17)	43	D24(d16)	44	GND
45	D23(d15)	46	D22(d14)	47	GND	48	D21(d13)
49	D20(d12)	50	GND	51	D19(NC)	52	D18(NC)
53	GND	54	D17(NC)	55	D16(NC)	56	GND
57	D15(d11)	58	D14(d10)	59	GND	60	D13(d09)
61	D12(d08)	62	GND	63	D11(d07)	64	D10(d06)
65	GND	66	D09(d05)	67	D08(d04)	68	GND
69	D07(d03)	70	D06(d02)	71	GND	72	D05(d01)
73	D04(d00)	74	GND	75	D03(NC)	76	D02(NC)
77	GND	78	D01(NC)	79	D00(NC)	80	GND

TABLE 3.3 - ICS-150B FPDP P3 DAC Data connector pin assignments

PIN		PIN		PIN		PIN	
1	GND	2	STROBE	3	GND	4	GND
5	GND	6	GND	7	NRDY*	8	GND
9	DIR*	10	GND	11	RESERVED	12	GND
13	SUSPEND*	14	GND	15	GND	16	GND
17	PIO2	18	GND	19	PIO1	20	GND
21	RESERVED	22	GND	23	RESERVED	24	GND
25	PSTROBE+	26	GND	27	PSTROBE-	28	GND
29	SYNC*	30	GND	31	DVALID*	32	GND
33	D31(d23)	34	D30(d22)	35	GND	36	D29(d21)
37	D28(d20)	38	GND	39	D27(d19)	40	D26(d18)
41	GND	42	D25(d17)	43	D24(d16)	44	GND
45	D23(d15)	46	D22(d14)	47	GND	48	D21(d13)
49	D20(d12)	50	GND	51	D19 (ADCECLK)	52	D18 (ADCETRIG)
53	GND	54	D17 (DACECLK)	55	D16 (DACETRIG)	56	GND
57	D15(d11)	58	D14(d10)	59	GND	60	D13(d09)
61	D12(d08)	62	GND	63	D11(d07)	64	D10(d06)
65	GND	66	D09(d05)	67	D08(d04)	68	GND
69	D07(d03)	70	D06(d02)	71	GND	72	D05(d01)
73	D04(d00)	74	GND	75	D03 (ADCSCLK)	76	D02 (ADCSTRIG)
77	GND	78	D01 (DACSCLK)	79	D00 (DACSTRIG)	80	GND

3.8.2 FPDP Signals

A description of FPDP signals is given in Table 3.4. In addition to the standard FPDP signals, the DAC FPDP connector P3 also carries the External Clock (ADCECLK and DACECLK) and External Trigger (ADCETRIG and DACETRIG) as well as the Multiple Board Synchronization signals (ADCSCLK, ADCSTRIG, DACSCLK and DACSTRIG) (See Table 3.3 above). In multiple board systems, one board is configured as the MASTER and the other/s as SLAVES. The External Clock and External Trigger signals must be connected to the P3 connector on the Master board, but not to the Slave boards. The Master distributes the Clock and Trigger signals to the slaves over the SCLK and STRIG connections.

TABLE 3.4 - ICS-150B FPDP Signal Descriptions

Signal/s	Signal Name	Description
d23:00	Data Bus	24 bit data bus driven by the data source. Channels A1 and A2 are presented simultaneously, with Channel A1 in the most significant word (MSW - d23:d12) and Channel A2 in the least significant word (LSW - d11:d00). In four channel mode, the next data sample contains Channels B1 and B2 with Channel B1 in the MSW and Channel B2 in the LSW. In 12 bit FPDP mode, only bits d23:12 are driven (see section 5.31).
DIR*	Data Direction	The data source asserts /DIR low.
DVALID*	Data Valid	When asserted, /DVALID indicates that the data bus has valid data. This signal is generated by the data source with each data sample.
STROB	Data Strobe	STROB is a free running clock supplied by the data source. The receiving end should clock the data with the rising edge of STROB.
NRDY*	Not Ready	/NRDY is asserted by the receiver when it is not ready to receive data. The data source must sample this signal until the receiver brings it high, at which time the transfer can commence. Since /NRDY is asynchronous to STROB, the data source should double-synchronize to it before sampling its state; this avoid metastability problems.
PIO1,PIO2	Prog. I/O	The PIO signals are programmable I/O lines for user-defined functions. They can be configured as inputs or outputs.
PSTROBE+	+ PECL Data Strobe	This signal along with /PSTROBE are generated by the data source as an optional differential PECL (Positive Emitter-Coupled Logic) data strobe. PSTROBE is the positive version of the differential clock and has the same polarity as STROB. For high data rate applications, the differential PECL data strobe should be used instead of STROB. The user must configure the board appropriately; see section 3.8.4.
PSTROBE-	- PECL Data Strobe	This signal is the negative version of the differential PECL data strobe.
Reserved		Do not connect to reserved signals.
SUSPEND*	Suspend Data	/SUSPEND is generated by the receiver to inform the data source of a pending FIFO overflow condition. The data source is allowed as many as 16 cycles before suspending the transfer. Since /SUSPEND is asynchronous to STROB, the data source should be double-synchronized to it before sampling its state; this avoids metastability problems.
SYNC*	Sync Pulse	The data source can provide a sync pulse to the receiver to synchronize data transfers. The receiver waits for the sync pulse before accepting data. The receiver starts accepting data on the first Data Valid period following the sync pulse.

3.8.3 FPDP Electrical Characteristics

Please refer to the ANSI/VITA 17 standard for details concerning FPDP electrical characteristics.

3.8.4 FPDP Timing

Please refer to the ANSI/VITA 17 standard for details concerning FPDP timing characteristics.

3.9 Light-Emitting Diodes

The ICS-150B is fitted with a set of light-emitting diodes (LEDs) which indicate board operation and error conditions. The diodes are located on the component side of the board; this is the right hand side when the board is installed in vertical orientation. The diodes are located starting approximately one half of an inch from the bottom of the board.

There are eight LEDs installed in a line. On the ICS-150B-ADM product, all LEDs are installed. On other boards (ICS-150B-AM and ICS-150B-DM), only the LEDs relating to the function of the board are installed. e.g. on ICS-150B-AM boards, the LEDs relating to DAC operation are omitted.

Table 3.6 describes the ICS-150B LEDs.

TABLE 3.6 Light Emitting Diodes

	LED Function	Colour	Description
1.	VME Access	Green	Illuminated at each valid VMEbus access to ICS-150B
2.	VSB Access	Green	Illuminated at each valid VSBbus access to ICS-150B
3.	FPDP In	Green	Illuminated at each FPDP Input access to ICS-150B
4.	FPDP Out	Green	Illuminated at each FPDP Output access to ICS-150B
5.	DAC Running	Green	Illuminated when DAC running.
6.	ADC Running	Green	Illuminated when ADC running.
7.	ADC Error	Red	Illuminated when ADC error condition occurs. Caused by user reading incorrect amount of data from swing buffer, or FIFO overflow or underflow.
8.	DAC Error	Red	Illuminated when DAC error condition occurs. Caused by user writing incorrect amount of data to swing buffer, or FIFO overflow or underflow.

Note: LED1 is nearest the bottom of the board.

The intensity of illumination of each LED will depend on the frequency of occurrence of the event in question. For example, a single VMEbus access will illuminate the LED for one bus cycle only; this will therefore not be visible to the user. However, multiple accesses over a period of time will be visible. Similarly, although ADC and DAC Running LEDs will be visible when operating in continuous modes, the intensity of illumination will reduce proportionally with the degree of decimation selected.

4 HARDWARE CONFIGURATION

Prior to board installation, the user should examine the VMEbus chassis where the ICS-150B board is to be installed. Some VMEbus signals are of the "daisy chain" type, i.e. they are routed through each board in turn using one connector pin for input to a board, and another pin for output; the signals in question are BG0IN/OUT, BG1IN/OUT, BG2IN/OUT, BG3IN/OUT and IACKIN/IACKOUT. For slots where boards will not be installed, one of two mechanisms is normally employed to ensure continuity for these signals. Either the user must install a set of jumpers on the VMEbus backplane, or the connectors are of a type which can sense the presence of a board and make or break the connection accordingly. If the backplane in use is a jumpered type, the user should remove all jumpers for the slot where an ICS-150B will be installed. All unused slots between slot 1 and the slot where the ICS-150B is installed must be jumpered to ensure correct operation.

A number of hardware configuration switches on the ICS-150B need to be configured. Figure 4 shows the switch locations.

Note that on some switches the on/off indication is shown by means of an arrow. In these cases, the arrow points in the "ON" or "CLOSED" direction of the switch.

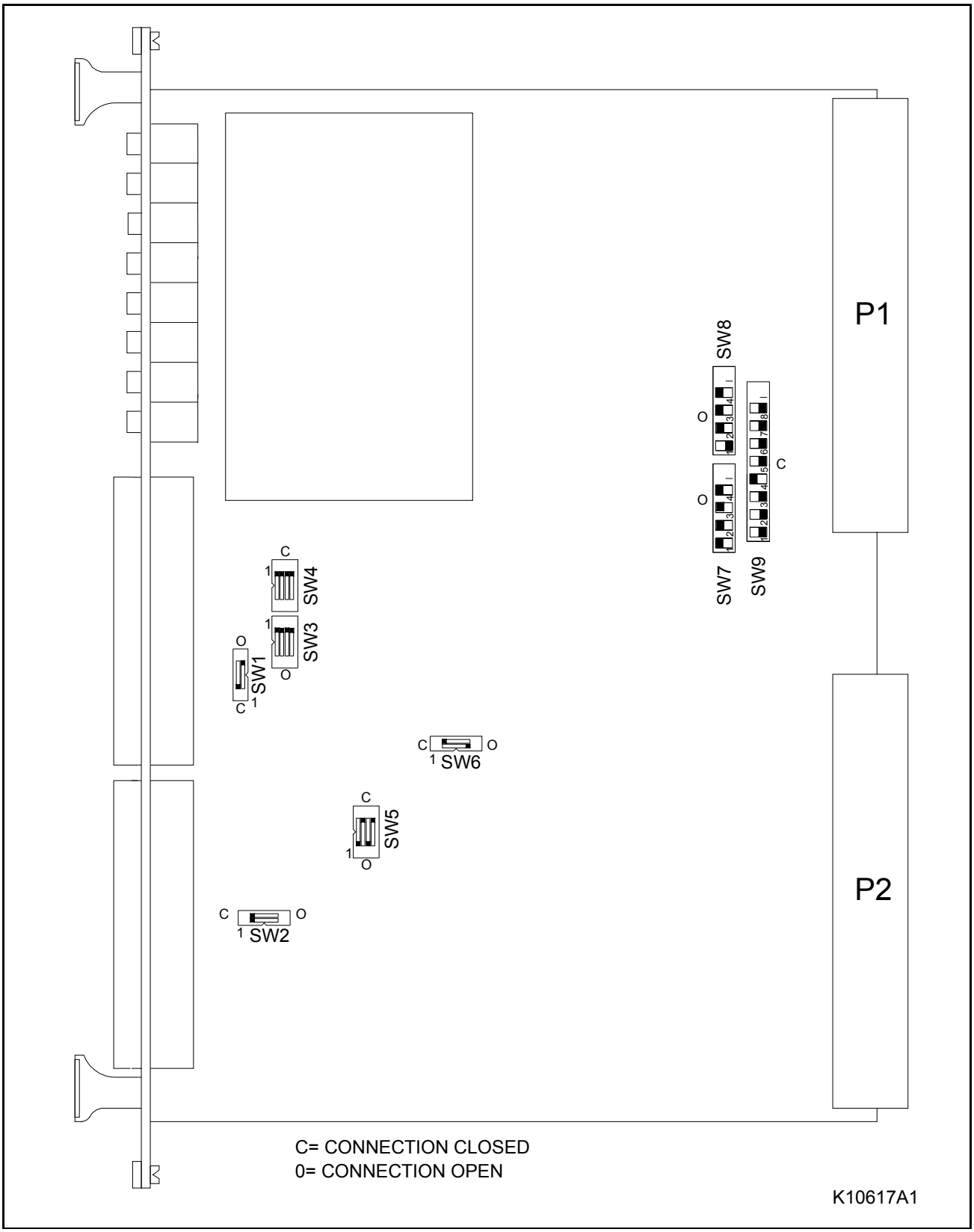


Figure 4 - ICS-150B Switch Placement and Default Settings

4.1 VMEbus Base Address Selection

The VMEbus A24 and A32 Base Address is set with switches SW8 and SW9. The values of these switches are loaded to SCV64 register VMEBAR at power-up. This register may be subsequently reprogrammed by the user (see section 5.3). The ICS-150B address map occupies a 512kB (Hexadecimal 0x80000) space. The VMEbus A64 base address is programmed after power up; details of the procedure for doing this are given in section 5.3. The A24 base address is set as given below. The factory default A24 address is 0x100000.

0=CLOSED (ON) 1=OPEN (OFF)

A24 BASE ADDRESS	SW9 12345	A24 BASE ADDRESS	SW9 12345
0x00.0000	00000	0x80.0000	10000
0x08.0000	00001	0x88.0000	10001
0x10.0000	00010	0x90.0000	10010
0x18.0000	00011	0x98.0000	10011
0x20.0000	00100	0xA0.0000	10100
0x28.0000	00101	0xA8.0000	10101
0x30.0000	00110	0xB0.0000	10110
0x38.0000	00111	0xB8.0000	10111
0x40.0000	01000	0xC0.0000	11000
0x48.0000	01001	0xC8.0000	11001
0x50.0000	01010	0xD0.0000	11010
0x58.0000	01011	0xD8.0000	11011
0x60.0000	01100	0xE0.0000	11100
0x68.0000	01101	0xE8.0000	11101
0x70.0000	01110	0xF0.0000	11110
0x78.0000	01111	0xF8.0000	11111

The A32 base address is set as given below. The factory default A32 address is 0x08000000.

0=CLOSED (ON) 1=OPEN (OFF)

A32 BASE ADDRESS	SW9 678	SW8 12
0x0000.0000	000	00
0x0800.0000	000	01
0x1000.0000	000	10
0x1800.0000	000	11
0x2000.0000	001	00
0x2800.0000	001	01
0x3000.0000	001	10
0x3800.0000	001	11
0x4000.0000	010	00
0x4800.0000	010	01
0x5000.0000	010	10
0x5800.0000	010	11
0x6000.0000	011	00
0x6800.0000	011	01
0x7000.0000	011	10
0x7800.0000	011	11
0x8000.0000	100	00
0x8800.0000	100	01
0x9000.0000	100	10
0x9800.0000	100	11
0xA000.0000	101	00
0xA800.0000	101	01
0xB000.0000	101	10
0xB800.0000	101	11
0xC000.0000	110	00
0xC800.0000	110	01
0xD000.0000	110	10
0xD800.0000	110	11
0xE000.0000	111	00
0xE800.0000	111	01
0xF000.0000	111	10
0xF800.0000	111	11

4.2 VSB Arbitration ID

Switch SW7 sets the VSB Arbitration ID for both INTV Interrupters during interrupt acknowledge cycles, and PAR requesters during VSB Arbitration. SW10 1 corresponds to the ID bit presented on VSB bit AD30, and SW10 4 corresponds to the ID bit presented on VSB bit AD27. VSB Bits corresponding to switches set CLOSED (ON) are driven low.

4.3 ADC Operating Mode

For the previous ICS-150 product, SW5 and SW6 set the 2-channel or 4-channel ADC operating mode. This mode is not required to be set for the ICS-150B, and SW5 and SW6 have different functions in the this product.

4.4 FPDP P3 Clock Select

Switch SW1 selects between the single ended TTL STROB and the PECL differential PSTROBE signals used to acquire FPDP data on the P3 Port (see section 3.8.4 for details):

CLOCK	SW1 1 2
STROB	ON OFF
PSTROBE,/PSTROBE	OFF ON

4.5 FPDP P4 Clock Select

Switch SW2 is used to connect the differential PECL PSTROBE clock signal to the FPDP P4 connector. If the PSTROBE signal is not required, both switches should be set to OFF (see section 3.8.4 for details):

PSTROBE OUTPUT TO P4	SW2 1 2
DISABLED	OFF OFF
ENABLED	ON ON

4.6 ADC Frequency Range

Switch SW5 1,2 set the ADC frequency range. These settings determine phase-locked loop parameters and must be correctly set when using an external clock as well as for internal clock. When using a frequency corresponding to an overlap between ranges, either setting may be used. When using the internal clock, the ADC Clock Frequency Select register must be used to program the precise sampling frequency.

FREQUENCY RANGE		SW5 1 2
4 CHANNEL MODE	2 CHANNEL MODE	
3.75 to 8.75MHz	7.5 to 17.5MHz	OFF ON
6.25 to 15MHz	12.5 to 30MHz	OFF OFF
10 to 20MHz	20 to 40MHz	ON OFF

4.7 DAC Frequency Range

Switch SW5 3,4 set the DAC frequency range. These settings determine phase-locked loop parameters and must be correctly set when using an external clock as well as for internal clock. When using a frequency corresponding to an overlap between ranges, either setting may be used. When using the internal clock, the DAC Clock Frequency Select register must be used to program the precise frequency.

FREQUENCY RANGE		SW5 3 4
4 CHANNEL MODE	2 CHANNEL MODE	
3.75 to 8.75MHz	7.5 to 17.5MHz	OFF ON
6.25 to 15MHz	12.5 to 30MHz	OFF OFF
10 to 20MHz	20 to 40MHz	ON OFF

4.8 DAC Internal Clock Source

Switch SW6 sets the DAC internal clock source. The DAC internal clock may be sourced either from the second programmable oscillator, or from the first programmable oscillator, which is also used by the ADC. This latter option ensures that the DAC clocks synchronously with the ADC, when this is required.

DAC INTERNAL CLOCK SOURCE	SW6 1 2
DAC Internal Clock Independent	OFF ON
DAC Internal Clock sourced from ADC Internal Clock	ON OFF
Not legal	OFF OFF
Not legal	ON ON

4.9 FPDP P3 Auxiliary Signals

Switches SW3 and SW4 are used to connect the external clock and trigger as well as the clock and trigger signals for multiple board synchronization to the FPDP P3 connector as described in the Table below.

NO	SIGNAL	SWITCH BIT	DESCRIPTION
1	ADCECLK	SW3 1	ADC External Clock Input
2	ADCETRIG	SW3 2	ADC External Trigger Input
3	DACECLK	SW3 3	DAC External Clock Input
4	DACETRIG	SW3 4	DAC External Trigger Input
5	ADCSTRIG	SW4 1	ADC Multiple Board (Slave) Trigger
6	DACSTRIG	SW4 2	DAC Multiple Board (Slave) Trigger
7	ADCSCLK	SW4 3	ADC Multiple Board (Slave) Clock
8	DACSCLK	SW4 4	DAC Multiple Board (Slave) Clock

If an external clock or trigger is to be used, the corresponding switch/es, numbers 1 through 4 in the table, should be set in the closed position on the board receiving the external signal/s. For multiple board configurations, only the master board should have these switches closed. If internal clock or trigger is used, the corresponding switch must be in the open state.

To achieve sampling synchronization and/or trigger synchronization between boards in multiple board configurations, the slave clock and/or trigger switches should be closed on all boards, including the master, but only for those signals used.

5 PROGRAMMING MODEL

The ICS-150B VMEbus Memory Map is shown in Figure 5. The individual bit fields of the registers are shown in Figure 6 through Figure 8. All programming and control of the ICS-150B is accomplished through the VMEbus interface. All control register bits that are not defined have no effect on the operation of the ICS-150B, but will always be read as zero. All other bits are undefined, and may be read as zero or one.

The ICS-150B VSB Memory Map is shown in Figure 9. The interface provides a 32MByte address space for reading and writing ADC and DAC data. In practice, the size of VSB data transfers will be limited not by this figure, but by the FIFO or Swing Buffer size.

ICS offers software drivers for the ICS-150B for a number of platforms (including VxWorks, SunOs, Solaris). These drivers greatly simplify control and operation of the ICS-150B, and are strongly recommended. Using one of these drivers will generally save the programmer much time since he/she is relieved of the requirement to understand the complexities of the ICS-150B hardware model and of the Tundra Semiconductor SCV64 VMEbus interface device. Contact ICS for further details.

5.1 General Notes

All transfers to and from the ICS-150B control and status registers should be done using D32 VMEbus cycles. The A24 and A32 VMEbus base address is programmed with on board switches as described in section 4. The ICS-150B responds to both SUPERVISORY and NON-PRIVILEGED VMEbus cycles. Individual bits in the 32 bit registers are referred to in braces. e.g. ADCCR<0> corresponds to ADC Control Register bit 0, and ADCDEC<7:0> corresponds to ADC Decimation Register bits 7 through 0.

IMPORTANT NOTE - ICS-150B Clock Frequency Stability

Due to the nature of the PLL (Phase-Locked Loop) clock generation circuitry of the ICS-150B, care should be taken to ensure that the PLL is locked before performing either ADC or DAC operations. The user should allow a 1 millisecond delay after a stable clock signal has been supplied to the PLL. When using the internal clock, this is when the programming word has been written to the internal clock and internal clock has been enabled in bit ADCCR1<0> or DACCR1<0>. When using an external clock, it is when the signal from the external clock source is known to be stable. If the required delay is not observed, the ADC or DAC sampling frequency may be grossly in error.

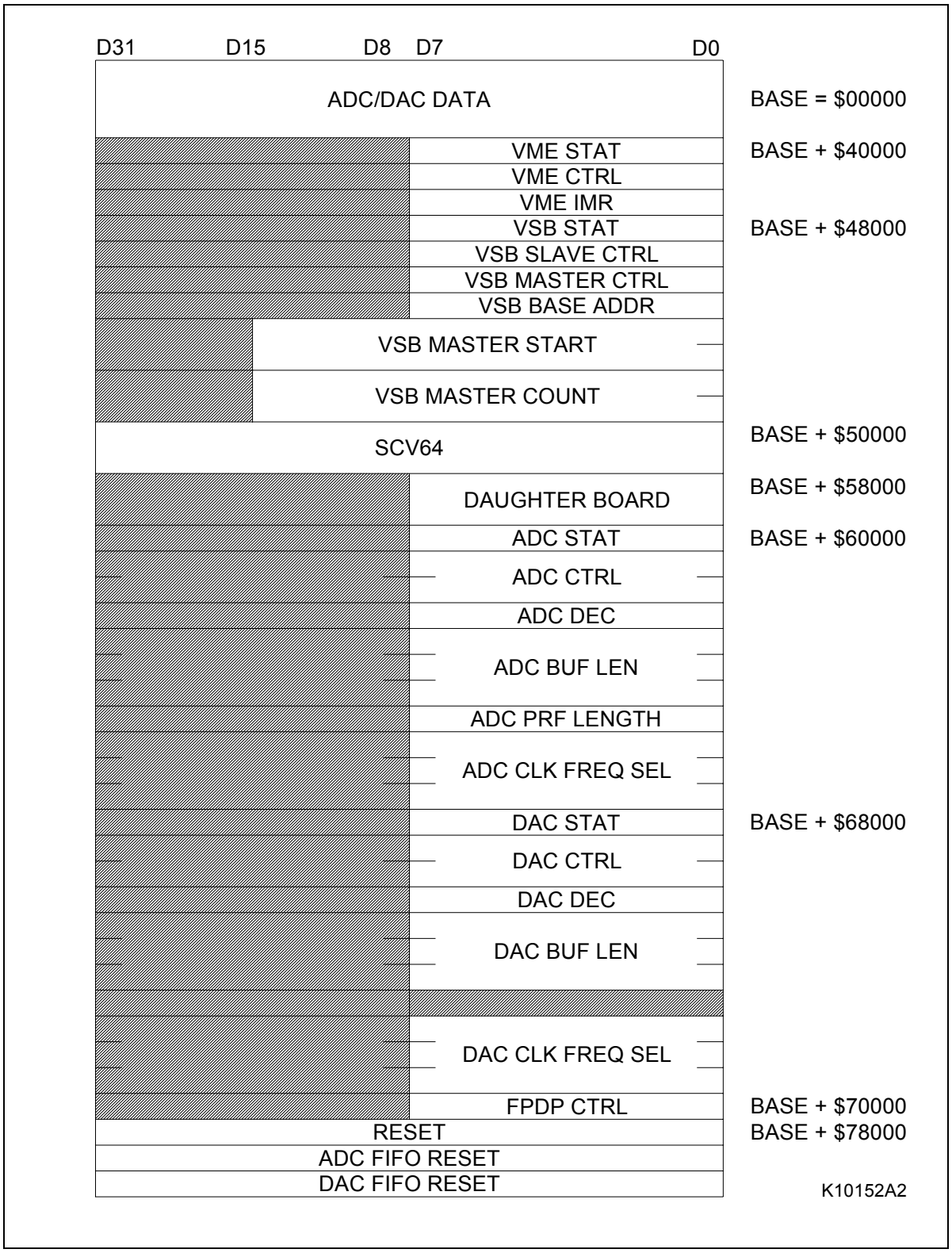


Figure 5 - ICS-150 VMEbus Memory Map

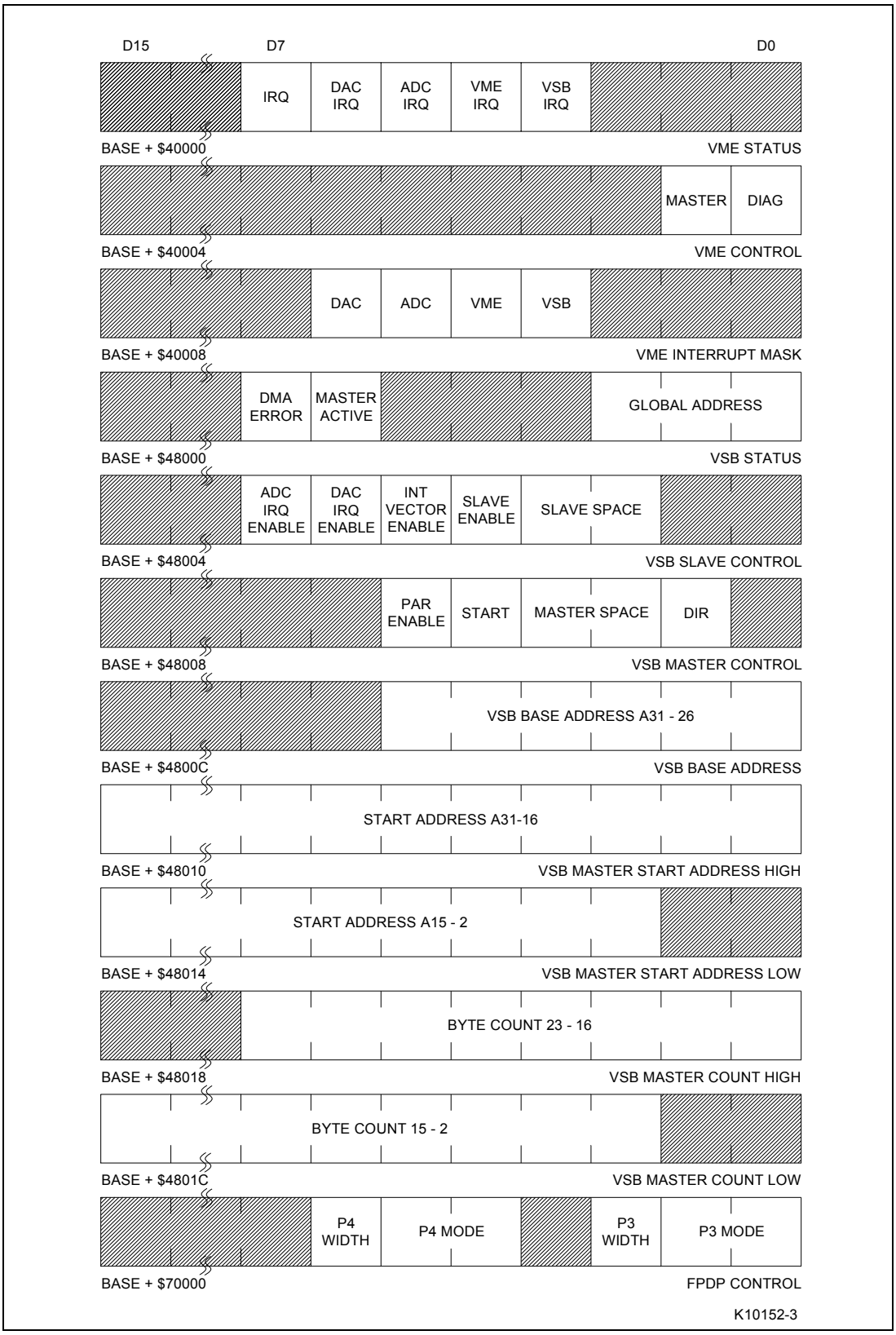


Figure 6 - ICS-150B VMEbus VME / VSB Control Registers

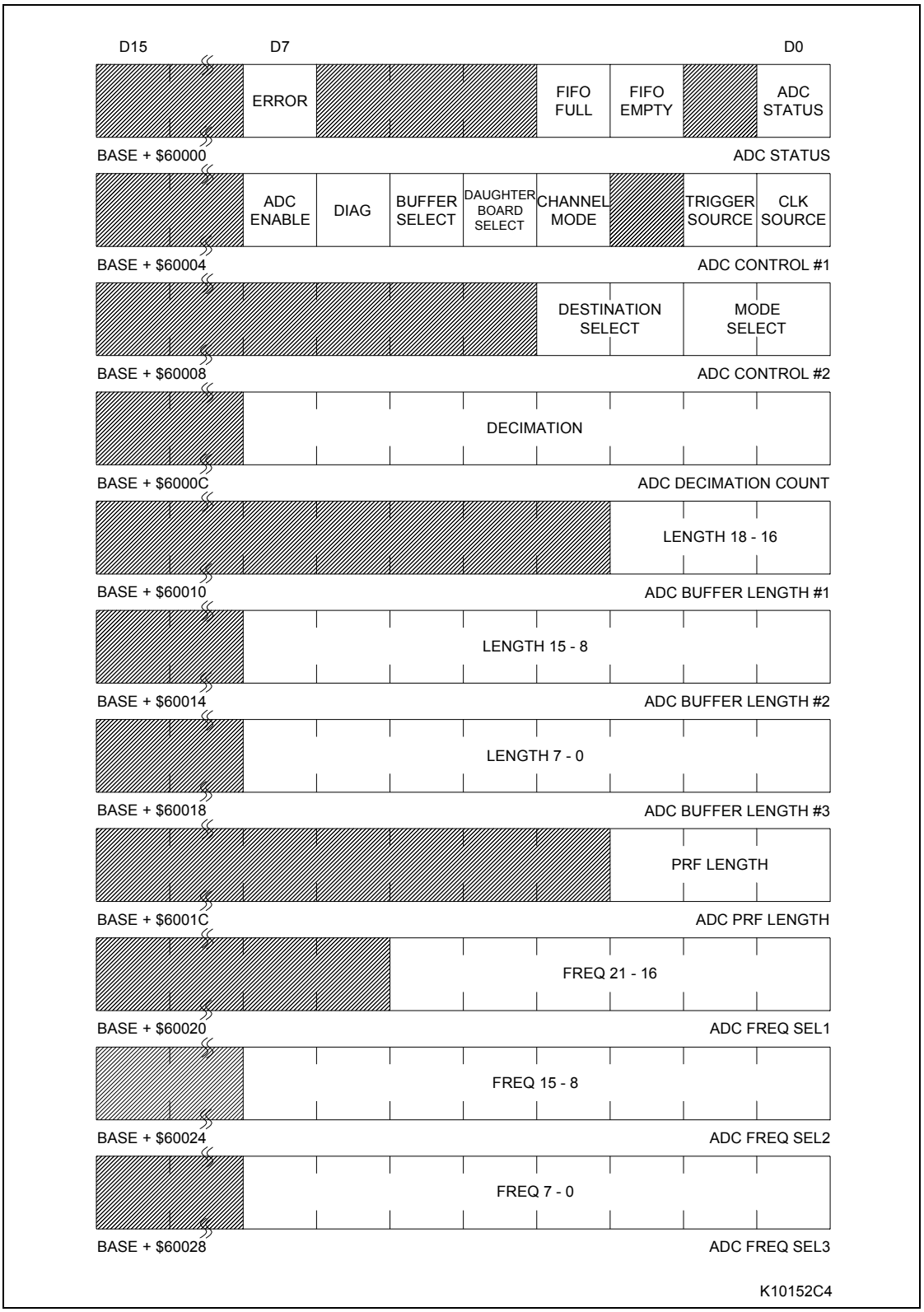


Figure 7 - VMEbus ADC Control Registers

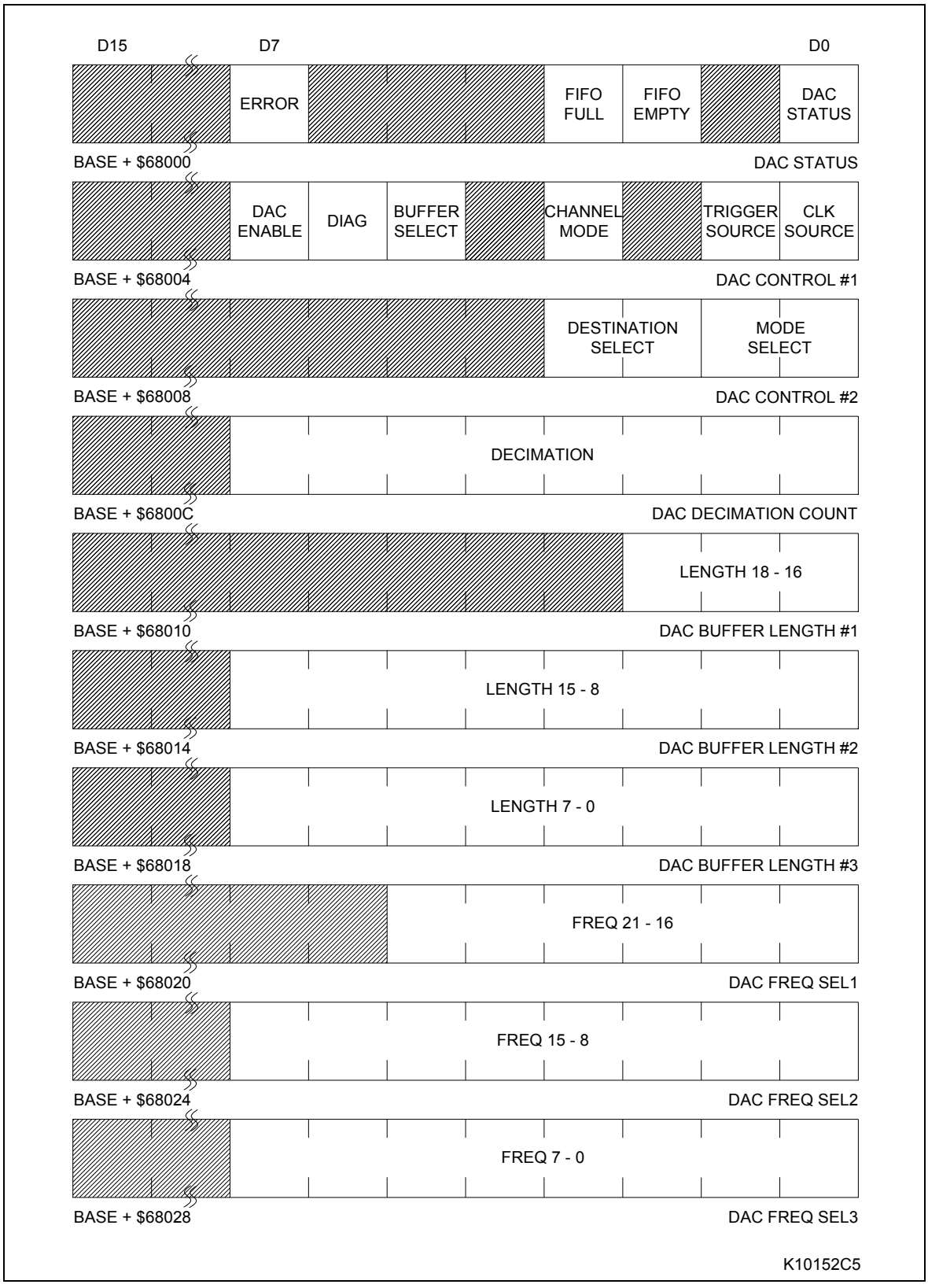


Figure 8 - VMEbus DAC Control Registers

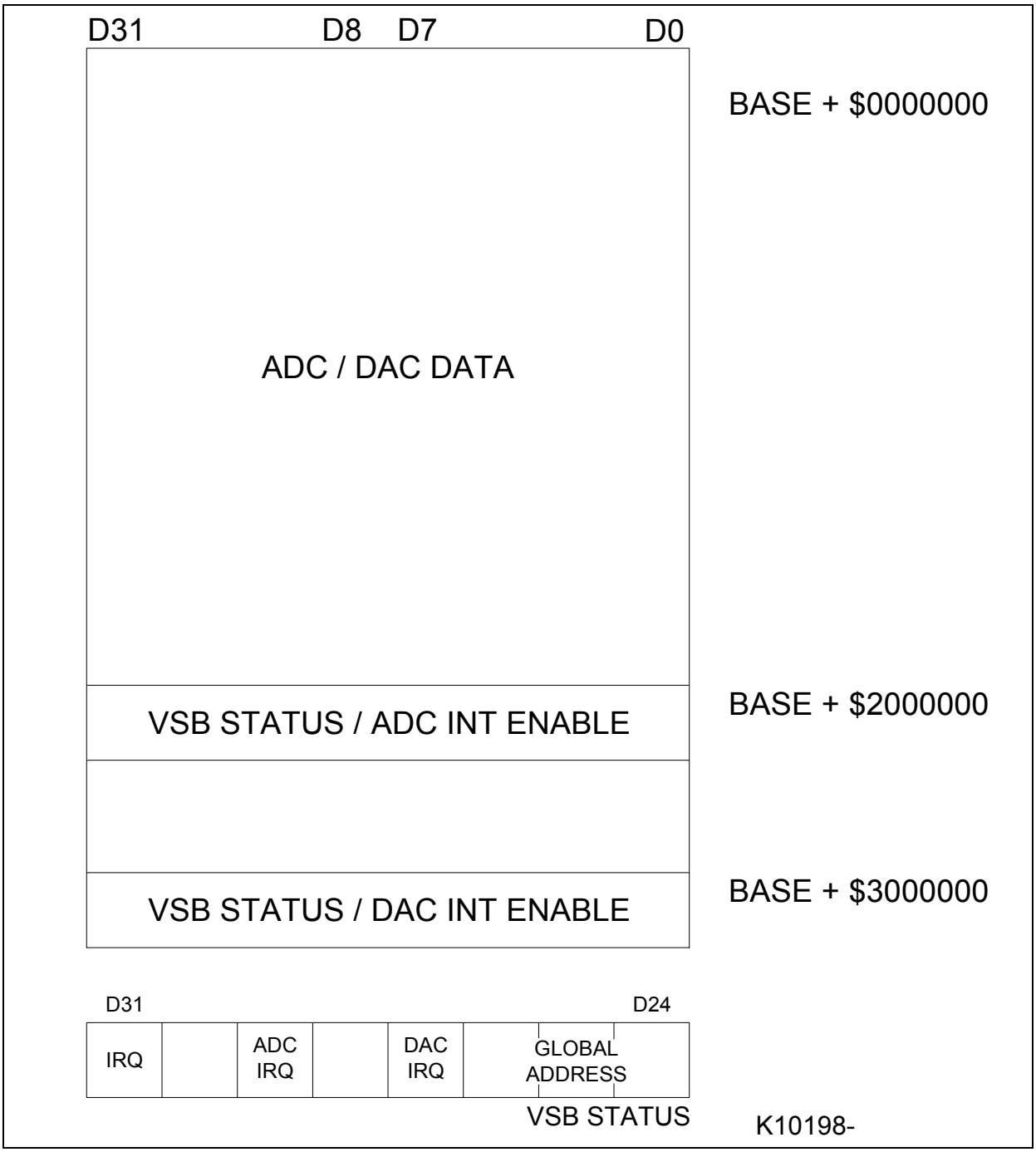


Figure 9 - ICS-150 VSB Memory Map

5.2 Using Diagnostic Mode

In order to test for correct functioning of either ADC or DAC channels, two approaches may be used. A full loop-round test may be conducted by externally connecting one or more of the DAC analog outputs to an ADC input. The DAC clock should also be connected to the ADC clock. The board may then be programmed to operate in its various modes, and comprehensive tests can be carried out using any data patterns which the user wishes to use. Alternatively, the built-in diagnostic features can be used. These are only available when one of the Swing Buffer options is installed on the board, and can only be exercised using the VMEbus. Diagnostic mode allows digital portions of the board to be checked by enabling write operations into the ADC Swing Buffer memory, and read operations from the DAC Swing Buffer. The ADC and DAC components themselves are not tested by this procedure, however the VME and VSB interfaces and large portions of the digital circuitry on the board are tested.

Both ADC and DAC sections of the ICS-150B are provided with a diagnostic mode. The mode is enabled using bit 6 of the ADCCR1 register and bit 6 of the DACCR1 register, respectively. Bit 0 of the VMR Control Register (VMECR) must also be set in either case.

Two peculiarities of diagnostic mode operation should be noted: Following the writing of data to both halves of the ADC Swing Buffer memory in diagnostic mode, when the data is read back, the order of reading the buffer halves is reversed. i.e. the half buffer written last is read first, and vice versa. Similarly when reading data from the DAC Swing Buffer following a write operation. Secondly, for both ADC and DAC, a "read" of one 32 bit longword must be done immediately before reading valid data from the buffers in order to correctly initialize the address logic. The data thus read is unimportant and may be discarded. The subsequent read operations must read the full length of each half buffer, as programmed in the buffer length register.

When using Diagnostic mode, it is important to carry out the various programming steps in the right order. The following fragments of pseudocode illustrate these steps:

/* ADC Memory Diagnostic Test */

1. Set Diag Mode bit. The FPDP master bit in VME Control Register should be set for Master boards only.
2. Set the following ADC configuration in ADCCR1 and ADCCR2:

   Diagnostic mode,
   Swing Buffer memory enabled,
   Internal Trigger,
   Internal Clock,
   Data routing = VME
   ADC Mode = One-shot

3. Set ADC Buffer Length to number of 32-bit words less 1 (maximum is 0x1FFFF or 0x7FFFFdepending on memory option installed)
4. Write to ADC Reset Register to initialize buffer
5. Write chosen data pattern to Swing buffer memory, observing buffer data organization described in section 5.5. The number of sample pairs written to memory must agree with buffer length parameter written previously
6. Clear diagnostic mode bit in ADCCR1. Other bits should remain unchanged
7. Clear diagnostic bit in VMECR. Other bit should remain unchanged
8. Perform dummy read of one 32 bit word from Swing Buffer memory
9. Read second half of Swing Buffer memory

10. Read first half of Swing Buffer memory
11. Compare data read with original data to check for correct operation

/* End of ADC Memory Diagnostic Test */

/* DAC Memory Diagnostic Test */

1. Clear Diagnostic Mode bit, set FPDP Master bit in VME Control Register (if Master board, otherwise clear it)
2. Set the following DAC configuration in DACCR1 and DACCR2:

    Diagnostic mode disabled,
    Swing Buffer memory enabled,
    Internal Trigger,
    Internal Clock,
    Data routing = VME
    DAC Mode = One-shot

3. Set DAC Buffer Length to number of 32-bit words less 1 (maximum is 0x1FFFF or 0x7FFFF, depending on memory option installed)
4. Write to DAC Reset Register to initialize buffer
5. Write chosen data pattern to Swing buffer memory, observing buffer data organization described in section 5.5. The number of sample pairs written to memory must agree with buffer length parameter written previously
6. Set diagnostic mode bit in DACCR1. Other bits should remain unchanged
7. Set diagnostic bit in VMECR. Other bit should remain unchanged
8. Perform dummy read of one 32 bit word from Swing Buffer memory
9. Read second half of Swing Buffer memory
10. Read first half of Swing Buffer memory
11. Compare data read with original data to check for correct operation
12. Clear DAC Diagnostic mode bit in DACCR1
13. Clear Diagnostic bit in VMECR

/* End of DAC Memory Diagnostic Test */

5.3 SCV64 Registers

The ICS-150B uses the Tundra Semiconductor SCV64 VMEbus interface chip to handle all VMEbus communications. Full details of the SCV64 may be found in the SCV64 User Manual (See Ref. 1). Table 5.1 gives descriptions for the SCV64 registers which may be needed when programming the ICS-150B. Unless the Master BLT/MBLT or the A64 capability of the SCV64 is to be utilized, the power-up defaults of the register contents are sufficient, with the following exception: the MODE register should be programmed to the hexadecimal value 0x9480e401. This value is chosen to optimize speed of transfer between the ICS-150B and the VMEbus. Descriptions of some of the bits of the MODE register are given in Table 5.1. For a more detailed description, see Ref. 1.

If the user wishes to employ VMEbus 64-bit address cycles (A64 addressing mode) when addressing the ICS-150B, it is necessary to program the most significant 32 bits of the ICS-150B base address (i.e. bits A<63:32>) to SCV64 register SA64BAR. The procedure for doing this is as follows:

i) Set MODE<12> to '1' (coupled mode).
ii) Write most significant 32 bits of VMEbus address to SA64BAR.
iii) Clear MODE<12>.

The least significant 32 bits of the 64-bit base address are taken from the A32 base address values configured for the board using switches SW11 and SW12 (see section 4). These switch settings are loaded to the SCV64 VMEBAR register at power up, but can be subsequently reprogrammed by the user.

The register map of the SCV64 is complex; only the relevant register assignments are discussed here. For this reason, accesses to the SCV64 memory space other than to documented offsets may have unpredictable consequences and should be avoided. The SCV64 has two sets of address and data busses, one connected to the VMEbus and the other to the ICS-150B local bus. VMEbus accesses are mapped from VMEbus space to local bus according to the programming of the SCV64. When the SCV64 is used to perform VMEbus Master transfers, it simultaneously becomes the local bus Master, and the VMEbus Master. When VMEbus Slave cycles occur, the SCV64 is the VMEbus Slave, but the local bus Master. When performing VMEbus Master transfers, the SCV64 can be configured to use normal cycles (VMEbus address broadcast between each cycle), BLT (D32 block transfer), or MBLT (D64 multiplexed block transfer). All register offsets are given with respect to the beginning of the SCV64 register window (BASE + 0x50000).

When the SCV64 is programmed to operate as the VMEbus Master, some caution must be taken when considering transfer counts. This is discussed in section 5.4.

TABLE 5.1 SCV64 Register Descriptions

Name	Register	Read/Write	Offset	Description
DMALAR	DMA Local Address	R/W	0x0	This register contains the local bus address used by the SCV64 when performing a VMEbus Master. This register must be re-programmed to zero before each Master transfer cycle is initiated.
DMAVAR	DMA VMEbus Address	R/W	0x4	This register contains the VMEbus address accessed by the SCV64 when it is performing a VMEbus Master transfer cycle. If not re-programmed between cycles, it continues from the next consecutive address.
DMATC	DMA Transfer Count	R/W	0x08	This register contains the DMA transfer count (Longwords) used by the SCV64 when it is performing a VMEbus Master transfer cycle. Register width is 20 bits (DMATC<19:00>).
DCSR	Control and Status Register	R/W	0x0C	The following describes the bits of the SCV64 Control and Status Register used by the ICS-150B. All other bits should be set to 0 during a write. The register should always be cleared before starting to set up a DMA transfer.
				DCSR<16> When asserted, this bit indicates an SCV64 configuration error
				DCSR<12> A64 base address ready. Must be programmed to 1 after the SA64BAR and MA64BAR registers have been programmed.
				DCSR<5> If asserted, a bus error has occurred during a DMA transfer. Write a '0' to clear the error.
				DCSR<3:2> If either of these bits are asserted, the previous DMA cycle failed. This can result from transferring too much data (See SCV Registers) or BERR was asserted on the VMEbus during the transfer. Writing '0' to these bits clears them.
				DCSR<1> When asserted, the previous DMA cycle was successfully completed. Writing '0' to this bit clears it.
				DCSR<0> Writing a '1' to this bit starts the DMA cycle. Reading a '1' indicates that a DMA cycle is in progress. A DMA cycle may be aborted while in progress by clearing this bit. In

				this case, DCSR<1> will be set, and a transfer complete interrupt will be requested.
VMEBAR	VMEbus Slave Base Address Register	R/W	0x10	This register is used to set the VME A24 and A32 Slave Base Address values. The A32 SBA is also used as the LS 32 bits of the A64 Slave Base Address. On power up, the A24 and A32 values are loaded from the on-board switches (see section 4).
				VMEBAR<22:21> Size of A24 slave image: 0 - 512K 1 - 1M 2 - 2M 3 - 4M
				VMEBAR<20:16> Base address of A24 slave image. These bits form bits A23-A19 of base address. Address bits A17 and A16 are forced to zero according to setting of VMEBAR<22:21> described above.
				VMEBAR<08:05> A32 slave image size. Selectable in powers of two from 4K to 128M. Program 0 for 4K, 0xF for 4M.
				VMEBAR<04:00> A32 base address. Selects base address in increments of 0x0800.0000 from 0x0000.0000 to 0xF800.0000. Program 0 for A32 address 0x0000.0000.
IVECT	VMEbus Interrupter Vector Register	R/W	0x24	This register contains the interrupt vector the SCV64 responds with during an interrupt acknowledge cycle.
MODE	Mode Control Register	R/W	0x3C	The following describes the bits of the SCV64 Mode Control Register which may need to be accessed when using the ICS-150B. All other bits should be set to '0' during a write.
				MODE<31> This bit controls the maximum transfer size of the SCV64. When set to '0', the maximum programmable transfer size is 4K (12 bit transfer count). When set to '1', the maximum is 2M (20 bit transfer count).
				MODE<28> This bit should always be written as '1'.
				MODE<26> This bit should always be written as '1'.

				MODE<23> When set to '0', the SCV64 uses non-privileged AM codes when doing Master transfers. When set to '1' it uses supervisory AM codes. Must be cleared if MODE<20> is set to '1'.
				MODE<20> When set to '1' SCV64 Master transfer cycles are performed using A64 addressing on the VMEbus. Otherwise A32 or A24 cycles are used, as determined by MODE<9>.
				MODE<19> When set to '1', SCV64 Master transfer cycles are performed using MBLT (D64) cycles on the VMEbus. Must be cleared if MODE<9> is set to '1' or if MODE<18> is set to '1'.
				MODE<18> When set to '1' SCV64 Master transfer cycles are performed using BLT cycles on the VMEbus. Must be cleared if MODE<19> is set to '1'.
				MODE<16> When set to '0' SCV64 Master transfer cycles are performed from ADC memory to the VMEbus, and from the VMEbus to DAC memory when '1'.
				MODE<15:13> These bits should always be written as all '1's.
				MODE<12> When set to '1', the receive FIFOs couple VME and local buses. When '0', busses are uncoupled. Should normally be written as '0', except when accessing SA64BAR and MA64BAR registers (see decriptions below).
				MODE<10> When set to '0' the VMEbus Slave image of the ICS-150B is disabled (will not respond), and enabled when set to '1'.
				MODE<9> When set to '0', the SCV64 Master operates in A32 or A64 mode (as determined by MODE<20>), and in A24 mode when set to '1'.
				MODE<0> If set to '0', all Slave images of the SCV64 are disabled. IN THIS EVENT, THE ICS-150B CANNOT BE ACCESSED UNTIL A VMEBUS RESET OCCURS.
SA64BAR	Slave A64 Base Address Register	R/W	0x40	This register sets bits 63-32 of the VMEbus A64 slave base address. The remaining bits (31-0) are taken from the A32 image. Before accessing this register, MODE<12> must be set to '1'. After accessing

				this register, MODE<12> should be cleared.
MA64BAR	Master A64 Base Address Register	R/W	0x44	This register sets bits 63-32 of the VMEbus A64 master base address. The remaining bits (31-0) are taken from the A32 image. Before accessing this register, MODE<12> must be set to '1'. After accessing this register, MODE<12> should be cleared.
GENCTL	General Control Register	R/W	0x88	GENCTL <0> (VI1BI) should be cleared in order to prevent the ICS-150B VMEbus interface from entering bus isolation (BI) mode in the event that the IRQ1 interrupt request signal is asserted.
VINT	VMEbus Interrupter Request Register	R/W	0x8C	The least significant three bits (D2:0) set the interrupt level of generated by the SCV64. Programming D3 high enables the interrupt. This bit is reset when the interrupt is acknowledged. Caution: Changing the interrupt level while D3 is in the enable state may cause improper operation.
VREQ	VMEbus Requester Register	R/W	0x90	The following describes the contents of VREQ:
				VREQ<7> VMEbus Ownership Timer Enable. Condition 1 after reset. 0 = Disable Timer, 1 = Enable Timer.
				VREQ<6> Bus Clear Recognition Control. Condition 0 after reset. 0 = Ignore BCLR* signal. 1 = Release bus if BCLR* asserted.
				VREQ<5> VMEbus Release Mode Control. Condition 1 after reset. 0 = Release on Request (ROR), 1 = Release when Done (RWD).
				VREQ<4> VMEbus Request Mode Control. Condition 1 after reset. 0 = Fair, 1 = Demand.
				VREQ<3:2> VMEbus Ownership Timer (Time-out Period). Condition 3 after reset. 0=Zero, 1=2microsec, 2=4microsec, 3=8microsec.
				VREQ<1:0> VMEbus Request Level. Condition 3 after reset. 0 = Level Zero.

5.4 Performing Block Transfers

When performing block transfers, it is important that the transfer count is correctly programmed. If not, memory buffer overflow may occur, or the ADC/DAC data window size may be exceeded. The size of the transfer should be the size of the data block currently available or the size of the ADC/DAC data window, whichever is smaller. For VME Master transfers, the count is specified in (32 bit) longwords, while for VSB Master transfers, the count is in bytes. Note that the VMEbus specification limits block transfers to a maximum of 256 Bytes, however, the ICS-150B design does not prevent transfers of larger blocks as described above. The parameters for maximum transfer count sizes are as follows for single-shot ADC/DAC operation, since the entire buffer is used:

Memory Type/Parameter	Longword count *	Byte Count	Sample Count
FIFO memory	4kLongwords	16kB	8kS
Swing Buffer, ICS-150BAM, DM and ADM versions	1MLongwords	4MB	2MS
VMEbus ADC/DAC Window	64kLongwords	256kB	128kS
VSB ADC/DAC Window	8MLongwords	32MB	16MS

* k = 1024
  M = 1024 X 1024

For continuous ADC/DAC operation, where half of the buffer length is filled at a time, the transfer counts are half of the above values.

Details of the procedures required to perform block transfers are given in the following sections.

5.4.1 VMEbus DMA Master

The SCV64 device controls all VMEbus Block transfers. These are also known as Direct Memory Access (DMA) transfers. With A24 or A32 addressing, standard VMEbus Block transfer (BLT) cycles may be used. With A32 or A64 addressing, Multiplexed Block transfer (MBLT) cycles may be used.

The order of programming for Master BLT and MBLT transfers is as follows. All register references are to SCV64 registers. For register details, please refer to Table 5.1 above.

1. Clear the DCSR register.
2. Set up the addressing and data transfer modes by writing to the MODE register. The default to be used for setting this register should be 0x9480e401. The following bits of the register may need to be changed - please refer to the descriptions in Table 5.1:

   MODE<23>
   MODE<20>
   MODE<19>
   MODE<18>
   MODE<17>
   MODE<16>
   MODE<15:13>
   MODE<12>
   MODE<9>

3. Clear the DMALAR (local bus address) register.
4. Write the VMEbus address (least significant 32 bits for A64 address) to DMAVAR. This is the destination address for a (write) operation from the ADC, or the source address for a (read) operation to the DAC.
5. For A64 address cycles only, write the most significant 32 bits of the VMEbus (source or destination) address to MA64BAR, using the following procedure:

   i) Set MODE<12> to '1' (coupled mode).
   ii) Write most significant 32 bits of VMEbus address to MA64BAR.
   iii) Clear MODE<12>.

6. Write the transfer count (number of 32 bit longwords) to DMATC.
7. Set DCSR<0>. This is the 'DMAGO' bit. The transfer will start at this point.
8. At the completion of the transfer DMAGO will be read as clear. The DONE bit, DCSR<1>, should be read as set, and a VME interrupt will be asserted. The user should clear DCSR<1> in order to clear the interrupt. If a completion interrupt occurs but the DONE bit is not read as set, an error has occurred. The type of error is indicated by bits DCSR<3:2> and DCSR<5>.

5.4.2 VMEbus DMA Slave

When performing a VMEbus BLT or MBLT block transfer with the ICS-150B as the slave device, no set-up activity is necessary unless the programmer wishes to use A64 address cycles. The set-up procedure for doing this is given in section 5.3 above.

The VMEbus ADC/DAC Data area is 0x40000 in size. Thus the maximum possible block transfer is 256kB. When initiating a transfer, the programmer should ensure that there are sufficient samples available in the buffer, and that the buffer is of sufficient size for the size of transfer contemplated (buffer sizes are given in section 5.4 above).

5.4.3 VSB DMA Master

Set-up and control for VSB Master transfers is done by programming various VMEbus registers as follows. Please note that there is a VSB Status register in the VMEbus memory map as well as the VSB map. The two registers contain different status information. The VMEbus VSB Status register is referred to here. The start address and count for the transfer must be chosen so that the VSB address presented by the master never crosses a 24 bit block boundary (i.e. bits A<31:24> do not change during the transfer):

1. Set all required parameters in the ICS-150B VSB Master Control register, with the START bit clear.
2. Write the Start address for the transfer to the VSB Master Start Address High and VSB Master Start Address Low registers.
3. Write the byte count for the transfer to the VSB Master Count High and VSB Master Count Low registers (24 bit width, LS 2 bits forced to zero - i.e. longword transfers).
4. If a completion interrupt is required, set the VSB bit in the VME Interrupt mask.
4. Set the START bit in the VSB Master Control register to initiate the transfer.
5. The MASTER ACTIVE bit in the VSB Status register will remain high until the transfer completes. If the VSB interrupt bit of the VME Interrupt mask was set, a VMEbus interrupt will occur upon completion of the transfer.

5.4.4 VSB DMA Slave

When performing a VSB block transfer with the ICS-150B as the slave device, it is only necessary to ensure that the most significant 6 bits of the VSB slave address have been written to the VSB Base Address register and the Slave Enable bit in the VSB Slave Control register has been set.

The VSB ADC/DAC Data area is 0x2000000 in size. Thus the maximum possible block transfer is 32MB, however, this exceeds the maximum buffer size of the ICS-150B. When initiating a transfer, the programmer should ensure that there are sufficient samples available in the buffer, and that the buffer is of sufficient size for the size of transfer contemplated. The maximum block transfer sizes are given in section 5.4 above.

5.5 ADC/DAC Data

This section of the ICS-150B's VMEbus memory map is used to move data from the ADC memory to VMEbus, and to move data to the DAC memory from VMEbus. The directions are reversed when using the built-in diagnostics capability (see section 5.2). This area of the map is used for access to data regardless of which memory buffer is being used, i.e. FIFO, Swing Buffer or Daughter Card Memory Buffer.

The data is organized as one sample in each 16-bit word, justified to the most significant 12 bits of the word. When two channel mode is selected, memory contains only data for these two channels. In four channel mode, memory contains data for all four channels. Successive channels occupy successive words, with "big endian" ordering. i.e. in two channel mode, channel A1 occupies the most significant 16 bits and channel A2 occupies the least significant 16 bits of a 32 bit longword. In four channel mode, the ordering, starting with the MS 16 bits of the first longword and ending with the LS 16 bits of the second longword is A1, A2, B1, B2.

Regardless of the type of memory in use, the data area appears to the user as FIFO type memory. In other words, random access to samples in the memory is not available. Data access is always sequential regardless of the address used for read or write, as long as the address used falls within the ADC/DAC Data area.

Each time a data word is read from the buffer (ADC operation), the data is removed from memory and buffer pointers are modified. DAC operation is similar. When using the optional swing buffer, the buffer length must be programmed. In this case, the user must be careful to read the exact number of 32-bit words corresponding to the programmed buffer length, otherwise buffer overflow or underflow will occur.

The user should perform a reset of the memory (ADCRST or DACRST register) after programming the ADC or DAC configuration and before loading data (DAC only) and enabling acquisition or generation. This is necessary to ensure that the buffer pointers are correctly aligned prior to buffer access by the ADC or DAC circuits.

Addresses presented by the bus master when reading or writing data may be either incremental or repetitive (i.e. always the same address). Provided that addresses fall within the ADC/DAC Data area, consecutive data will be read from or written to the board regardless of the addressing mode. This allows for standard addressing and block transfers with devices which either increment addresses or repetitively present the same address.

5.6 VMEbus Status Register (VMESR)

Read only

The VMEbus Status Register contains information about the state of the ICS-150B VMEbus Interface. It is used to determine the interrupt status of the ICS-150B, and the source of the interrupt.

5.6.1 VMESR<3> - VSB Master IRQ

This bit reflects the status of the VSB master interface.

VMESR<3>	VSB Master Interrupt Request Status
READ ONLY	
0	VSB Master is not generating an IRQ
1	VSB Master is generating an IRQ

5.6.2 VMESR<4> - VMEbus Master IRQ

This bit reflects the interrupt status of the SCV64 VMEbus master interface.

VMESR<4>	VMEbus Master Interrupt Request Status
READ ONLY	
0	SCV64 is not generating an IRQ
1	SCV64 is generating an IRQ

5.6.3 VMESR<5> - ADC IRQ

This bit reflects the status of the ADC control unit. When the FIFO reaches half full or the Swing Buffer swaps (whichever is selected), the ADC control unit will assert this flag. If ADC interrupts are enabled, an interrupt request will occur.

VMESR<5>	ADC Interrupt Request
READ ONLY	
0	ADC control unit is not asserting IRQ
1	ADC control unit is asserting IRQ

5.6.4 VMESR<6> - DAC IRQ

This bit reflects the status of the DAC control unit. When the FIFO reaches half empty or the Swing Buffer swaps (whichever is selected), the DAC control unit will assert this flag. If DAC interrupts are enabled, an interrupt request will occur.

VMESR<6>	DAC Interrupt Request
READ ONLY	
0	DAC control unit is not generating an IRQ
1	DAC control unit is generating an IRQ

5.6.5 VMESR<7> - IRQ

This bit indicates that the ICS-150B is asserting a VMEbus interrupt from any source (i.e. Master transfer completion, ADC, or DAC). It is therefore an OR of the state of bits 4, 5 and 6 of this register.

VMESR<7>	VMEbus Interrupt Request
READ ONLY	
0	VMEbus interrupt is not asserted
1	VMEbus interrupt is asserted

5.7 VMEbus Control Register (VMECR)

Read/Write

The VMEbus Control Register configures the following operating parameters of the ICS-150B.

- diagnostic mode selection
- master or slave selection

5.7.1 VMECR<0> - Diagnostics control

This bit is used to enable the Diagnostic mode for the DAC and ADC Swing Buffer memories. To perform ADC diagnostics, both this bit and the diagnostics bit in the ADC Control Register must be used. Similarly, to perform diagnostics of the DAC memory, both this bit and the DAC Control Register diagnostics bit must be used.

VMECR<0>	Diagnostics control
READ/WRITE	
0	Diagnostic mode disabled
1	Diagnostic mode enabled

5.7.2 VMECR<1> - FPDP Master Enable

This bit determines which board is the master or a slave when using multiple board synchronization. In single board configurations, this bit must always be set.

VMECR<1>	FPDP Master Enable
READ/WRITE	
0	Board is a Slave
1	Board is a Master

5.8 VMEbus Interrupt Mask Register (VMEIMR)

Read/Write

The Interrupt Mask Register controls the possible sources of VMEbus interrupts. Masked interrupts are still seen in the corresponding bits of the status register, but do not affect the VMEbus IRQ signal.

5.8.1 VMEIMR<3> - VSB IRQ Mask

This bit enables the VSB Master controller to generate VMEbus interrupts upon completion of a transfer.

VMEIMR<3>	VSB Master VMEbus Interrupt Enable Mask
READ/WRITE	
0	VSB Master Interrupts are disabled
1	VSB Master Interrupts are enabled

5.8.2 VMEIMR<4> - VMEbus IRQ Mask

This bit enables the SCV64 VMEbus Master controller to generate VMEbus interrupts upon completion of a transfer.

VMEIMR<4>	VMEbus Master Interrupt Enable Mask
READ/WRITE	
0	SCV64 Interrupts are disabled
1	SCV64 Interrupts are enabled

5.8.3 VMEIMR<5> - VME ADC IRQ Mask

This bit enables the ADC control unit controller to generate VMEbus interrupts.

VMEIMR<5>	ADC Interrupt Enable Mask
READ/WRITE	
0	ADC Interrupts are disabled
1	ADC Interrupts are enabled

5.8.4 VMEIMR<6> - VME DAC IRQ Mask

This bit enables the DAC control unit controller to generate VMEbus interrupts.

VMEIMR<6>	DAC Interrupt Enable Mask
READ/WRITE	
0	DAC Interrupts are disabled
1	DAC Interrupts are enabled

5.9 VSB Status Register (VSBSR)

Read only

The VSB Status register contains information about the status of the ICS-150B's VSB interface. It contains the board's VSB Global Address, whether the VSB Master is performing a transfer, and the error status of the last (or current) VSB transfer.

5.9.1 VSBSR:<2:0> - VSB Global Address

These bits reflect the VSB Backplane Global Address GA0-2 of the ICS-150B in accordance with the VMEbus Specification. This information is also available from the VSB Bus Status Register (see section 5.32.1).

VSBSR<2:0>	VSB Backplane Global Address
READ ONLY	
000	VSB Slot 1
001	VSB Slot 2
010	VSB Slot 3
011	VSB Slot 4
100	VSB Slot 5
101	VSB Slot 6

5.9.2 VSBSR<6> - VSB Master Active

This bit reflects the activity of the VSB Master Interface.

VSBSR<6>	VSB Master Status
READ ONLY	
0	VSB Master Idle
1	VSB Master Active

5.9.3 VSBSR<7> - VSB Error

This bit indicates when a VSB Master transfer error occurs. Errors result when a slave responds with the VSB ERR signal, at which point the master terminates the transfer.

VSBSR<7>	VSB Master Transfer Error
READ ONLY	
0	No Error
1	Error occurred during transfer.

5.10 VSB Slave Control Register (VSBSCR)

Read/Write (bits 2 to 5), Read Only (bits 6 and 7)

The VSB Slave Control Register determines the behavior of the ICS-150B VSB Slave Interface.

5.10.1 VSBSCR<3:2> - VSB Slave Space

These bits set the VSB Space Code for the slave image to respond and participate in data transfers.

VSBSCR<3:2>	VSB Space Code for Slave Image
READ/WRITE	
01	Alternate Address Space
10	I/O Address Space
11	System Address Space

5.10.2 VSBSCR<4> - VSB Slave Image Enable

This bit enables the slave image of the ICS-150B on the VSB. The ICS-150B will not respond to VSB accesses until this bit has been set.

VSBSCR<4>	VSB Slave Image Enable
READ/WRITE	
0	Slave image disabled
1	Slave image enabled

5.10.3 VSBSCR<5> - VSB INTV Enable.

This bit enables Vectored Interrupts on the VSB. Vectored interrupts allow the VSB to arbitrate prioritized interrupts. If vectored interrupts are not enabled, the VSB master must poll the VSB Status register of each VSB board to determine the source of the interrupt.

VSBSCR<5>	VSB Vectored Interrupt Enable
READ/WRITE	
0	INTP (Polled) Interrupts enabled only
1	INTP (Polled) and INTV (Vectored) Interrupts enabled

5.10.4 VSBSCR<6> - VSB DAC Interrupt Enable Status

This read-only bit shows the status of the DAC interrupt enable on the VSB.

VSBSCR<6>	VSB DAC Interrupt Enable Status
READ ONLY	
0	VSB DAC Interrupt disabled
1	VSB DAC Interrupt enabled

5.10.5 VSBSCR<7> - VSB ADC Interrupt Enable Status

This read-only bit shows the status of the ADC interrupt enable on the VSB.

VSBSCR<7>	VSB ADC Interrupt Enable Status
READ ONLY	
0	VSB ADC Interrupt disabled
1	VSB ADC Interrupt enabled

5.11 VSB Master Control Register (VSBMCR)

Read/Write

The VSB Master Control Register determines the behavior of the ICS-150B VSB Master Interface.

5.11.1 VSBMCR<1> - VSB Direction Control

This bit determines direction of the transfer to be performed by the master interface.

VSBMCR<1>	VSB Transfer Direction Control
READ/WRITE	
0	Read Data Transfer (i.e. input of data to ICS-150B)
1	Write Data Transfer (i.e. output of data from ICS-150B)

5.11.2 VSBMCR<3:2> - VSB Master Space

These bits set the VSB Space Code used by the Master when performing transfers.

VSBMCR<3:2>	VSB Space Code for Master Image
READ/WRITE	
01	Alternate Address Space
10	I/O Address Space
11	System Address Space

5.11.3 VSBMSCR<4> - VSB Master Enable

This bit is used to start a DMA transfer on VSB with the ICS-150B as master.

VSBMSCR<4>	VSB Master Interface Enable
READ/WRITE	
0	VSB Master interface disabled
1	VSB Master interface enabled

5.11.4 VSBSCR<5> - VSB PAR Enable

This bit enables parallel arbitration for VSB mastership. Note that if SER arbitration is used, a VSB Arbiter must be in VSB slot 1.

VSBSCR<5>	VSB Parallel Arbitration Enable
READ/WRITE	
0	SER Arbitration only
1	SER and PAR Arbitration

5.12 VSBBAR - VSB Slave Base Address

Read/Write

During VSB address cycles, the most significant bits (A31-26) of the address presented on the bus are compared with the value of this register. If the Slave image is enabled, a match will result in an ICS-150B response. The value of bit A25 is decoded to provide access either to ADC/DAC data (if A25 is zero) or to the VSB status register (if A25 is one) (see Figure 11, ICS-150B VSB Memory Map).

5.13 VSBMSAH<15:0> - VSB Master Start Address (high)

Write only

The value of this register is used as address bits A31-A16 of the starting address of the slave device during a master transfer.

5.14 VSBMSAL<15:0> - VSB Master Start Address (low)

Write only

The value of this register is used as address bits A15-A00 of the starting address of the slave device during a master transfer.

5.15 VSBMCH<7:0> - VSB Master Count (high)

Write only

The value of this register is loaded as the most significant bits (23-16) of the byte counter for a master transfer.

5.16 VSBMCL<15:0> - VSB Master Count (low)

Write only

The value of this register is loaded as the least significant bits (15-0) of the byte counter for a master transfer. Note that the least significant two bits (1 and 0) are always zero, since the master interface always performs longword transfers (four bytes).

5.17 ADCSR - ADC Status Register

Read Only

5.17.1 ADCSR<0> - ADC Internal Trigger

This bit reflects the status of the ADC control unit. It will be set when the ADCCR1<7> has been set (for internal triggering) or when an external trigger rising edge has been received (for external triggering). For an indication of completion of single-shot acquisition or buffer swap, the user should examine the ADC IRQ bit (VMESR<5>).

ADCSR<0>	ADC Internal Trigger Status
READ ONLY	
0	ADC acquisition halted
1	ADC acquisition in progress

5.17.2 ADCSR<2> - ADC FIFO Empty Flag

This bit indicates that the ADC FIFO is empty.

ADCSR<2>	ADC FIFO Empty Flag
READ ONLY	
0	FIFO is not empty
1	FIFO is empty

5.17.3 ADCSR<3> - ADC FIFO Full Flag

This bit indicates that the ADC FIFO is full.

ADCSR<3>	ADC FIFO Full Flag
READ ONLY	
0	FIFO is not full
1	FIFO is full

5.17.4 ADCSR<7> - ADC Acquisition Error

This bit indicates if an error occurred during acquisition. Acquisition errors include:

1. FIFO Full when not in FIFO capture mode.
   This may occur if the clock frequency is greater than the specified range for the board.
2. Bank Swap before completion of readout.
   This may occur if the user fails to allow for data read/write rates which keep pace with the selected sampling/data generation frequency.
3. SYNC bit misalignment.
   This may occur on the DAC FPDP link if the data source device does not correctly generate the SYNC bit.

ADCSR<7>	ADC Acquisition Error
READ ONLY	
0	No error
1	An Acquisition Error occurred

5.18 ADCCR1 - ADC Control register #1

Read/Write

5.18.1 ADCCR1<0> - ADC Sampling Clock Source

This bit selects between the internal and external sampling clocks for the ADC. When the board is a slave (i.e. takes its sampling clock from a ICS-150B configured as a master), this bit is a "don't care". Refer to section 4.9 for details of external clock and multiple board configurations.

ADCCR1<0>	ADC Sampling Clock Source
READ/WRITE	
0	Internal Sampling Clock
1	External Sampling Clock

5.18.2 ADCCR1<1> - ADC Trigger Enable

This bit determines if the external ADC Trigger is used to start an acquisition. When using an external trigger, triggering occurs following the rising edge of the trigger signal. The signal must remain high for at least two complete clock cycles. This bit is a "don't care" for slave boards.

ADCCR1<1>	ADC Trigger Enable
READ/WRITE	
0	Use internal enable (bit ADCCR1<7>)
1	Use External Trigger input

5.18.3 ADCCR1<3> - ADC Channel Mode

This bit must be set to reflect the operating mode of the ADC, either two channel or four channel. Hardware switches SW5 and SW6 must also be set (see section 4.3 above).

ADCCR1<3>	ADC Channel Mode
READ/WRITE	
0	4 Channel mode
1	2 Channel mode

5.18.4 ADCCR1<4> - Daughter Board Select

This bit switches between the on-board sample buffers and the daughter board sample buffer. In order to use the daughter board, the Swing Buffer memory must also be selected (bit ADCCR1<5>). Daughter board data is accessed at the ADC/DAC data area of the memory map, as for the on-board buffers.

ADCCR1<4>	Daughter Board Select
READ/WRITE	
0	On-Board FIFO and Swing Buffer sample memory selected
1	Daughter Board sample memory selected

5.18.5 ADCCR1<5> - ADC FIFO Select

This bit is used to select either the on-board swing buffer and the daughter board memory (when installed), or the ADC FIFO sample buffer. When using either of the on-board sample buffers, ADCCR1<4> (Daughter Board Select) must be set to zero, otherwise it must be set to 1. When using either of the on-board sample buffers, data is read from the ADC/DAC Data area of the memory map.

ADCCR1<5>	ADC FIFO Select
READ/WRITE	
0	ADC FIFO selected
1	ADC Swing Buffer and Daughter board memory selected

5.18.6 ADCCR1<6> - ADC Diagnostics enable

This bit is used to enable the ADC Diagnostic mode. In this mode, VMEbus Data can be written to the swing buffer. Once cleared, the data can be read back from the swing buffer.

ADCCR1<6>	ADC Diagnostics enable
READ/WRITE	
0	Diagnostic Mode disabled
1	Diagnostic Mode enabled

5.18.7 ADCCR1<7> - ADC Enable

This bit is used to start an acquisition. If external triggering is selected, the acquisition begins following the next rising edge of the trigger, otherwise it starts on the next rising clock edge. In multiple board configurations with synchronized trigger, this bit should be set on all slave boards before setting it on the master, in order to arm the slaves. This guarantees that all boards will start sampling simultaneously.

ADCCR1<7>	ADC Enable
READ/WRITE	
0	ADC acquisition disabled
1	ADC acquisition enabled

5.19 ADCCR2 - ADC Control Register #2

Read/Write

5.19.1 ADCCR2<1:0> - ADC Mode

These bits select between the continuous, one-shot and PRF modes of operation. PRF mode requires the Swing Buffer option to be installed. In PRF mode, the number of 32-bit words specified by the value programmed to the PRF length register (ADCPRFLEN - see section 5.22) is captured at each application of the trigger (rising edge of signal if external trigger selected). Following completion of each PRF acquisition sequence, the user must ensure that a dwell period of at least 3.2 microseconds is allowed before the next trigger.

ADCCR2<1:0>	ADC Mode
READ/WRITE	
00	Continuous Mode
01	One-Shot Mode
10	Continuous Mode with PRF
11	One-Shot Mode with PRF

5.19.2 ADCCR2<3:2> - Destination Select

These bits control the flow of the ADC data.

ADCCR2<3:2>	Destination for ADC Data
READ/WRITE	
00	VMEbus
01	VSB
10	FPDP

5.20 ADCDEC<7:0> - ADC Decimation Count

Write Only

This register determines the eight bit decimation count. Setting this register to zero disables decimation. Any other value determines the number of sample clock cycles between ADC FIFO writes. This effectively reduces the sampling rate, allowing operation of the ICS-150B with an effective sampling rate below 3.75 MHz (4 channel mode) or 7.5 MHz (2 channel mode).

5.21 ADCBL - ADC Buffer Length Register

Write only

The ADC Buffer Length Register is used only when the Swing Buffer option is installed on the ICS-150B. The number programmed must always be one less than the buffer length value required. The 19 bit buffer length (+1) determines the number of 32-bit words written to the swing buffer by the ADCs before the buffer banks are swapped (i.e. half of the total swing buffer length). In continuous mode, this number of words will be stored prior to each interrupt. In one-shot mode, twice this number of 32-bit words will be acquired before acquisition halts. Note that each 32-bit word contains two samples.

The number of samples per channel contained in the swing buffer depends on whether two or four channel mode is operative. In two channel mode, the number of samples per channel is equal to the programmed swing buffer length (+1). In four channel mode, the swing buffer length (+1) must be divided by two to yield the number of samples per channel. Details of data packing are given in section 5.5.

The number of 32-bit words (not samples) which must be unloaded is as follows:

M x(BL+1)

where M = 2 for ADC capture mode.
M = 1 for ADC continuous mode.
BL = value programmed to the buffer length register

The user must perform an ADC Reset (see ADCRST register) after loading ADCBL in order for the new buffer length to take effect.

5.21.1 ADCBL1<2:0> - ADC Buffer Length Register 1

These bits are bits 18-16 of the 19 bit ADC Swing Buffer Length register.

5.21.2 ADCBL2<7:0> - ADC Buffer Length Register 2

These bits are bits 15-8 of the 19 bit ADC Swing Buffer Length register.

5.21.3 ADCBL3<7:0> - ADC Buffer Length Register 3

These bits are bits 7-0 of the 19 bit ADC Swing Buffer Length register.

5.22 ADCPRFLEN<2:0> - ADC PRF Length Register

When PRF mode is enabled, these bits determine the PRF length. At each application of the trigger, the specified number of 32-bit words will be acquired and stored in the buffer. Bank swap and interrupt (if enabled) will not occur until the total number of 32-bit words in the buffer equals the value specified by the buffer length register (ADCBL). The Swing Buffer option must be installed on the ICS-150B when using PRF mode. Note that the correspondence between 32-bit words in the swing buffer and samples per channel depends on the channel mode. In 2-channel mode, samples per channel equals 32-bit words. In 4-channel mode, samples per channel equals 32-bit words divided by two. The buffer length registers, ADCBL1, ADCBL2 and ADCBL3 (see section 5.21), must be programmed with a value which is an exact multiple (less one) of the PRF length so as to avoid buffer overflow.

ADCPRFLEN<2:0>	ADC PRF Length Register
WRITE ONLY	
000	256 32-bit words
001	512 32-bit words
010	1024 32-bit words
011	2048 32-bit words
100	4096 32-bit words
101	8192 32-bit words
110	16384 32-bit words

5.23 ADCFS - ADC Clock Frequency Select register

Write only

The ADC Clock Frequency Select register is used to program the frequency of the internal ADC clock. The clock is programmable to a resolution of approximately 200Hz. The program word is not in engineering units, and must be calculated by the user, or obtained using a utility function (subroutine) included with the ICS-150B software drivers. Details of the algorithm for computing this programming word are given in section 6.

These registers need not be programmed if an external sampling clock is used. In multiple board configurations, only the Master board's sample clock need be programmed.

ADCFS1<5-0> - ADC Clock Frequency Select Register #1

These bits are bits 21-16 of the 22 bit clock programming word.

ADCFS2<7-0> - ADC Clock Frequency Select Register #2

These bits are bits 15-8 of the 22 bit clock programming word.

ADCFS3<7-0> - ADC Clock Frequency Select Register #3

These bits are bits 7-0 of the 22 bit clock programming word. When programming a new frequency value, this register should be written last, since upon completion of a write to this register the entire 22 bit clock programming word is shifted out to the Clock Generator. The valid programming range for the ICS-150B is 3.75 MHz to 40 MHz.

5.24 DACSR - DAC Status Register

Read Only

5.24.1 DACSR<0> - DAC Internal Trigger

This bit reflects the status of the DAC control unit. It will be set when the DACCR1<7> has been set (for internal triggering) or when an external trigger rising edge has been received (for external triggering). For an indication of completion of single-shot generation or buffer swap, the user should examine the DAC IRQ bit (VMESR<6>). This bit will reset when the DAC Enable bit is cleared.

DACSR<0>	DAC Internal Trigger Status
READ ONLY	
0	DAC idle
1	DAC running

5.24.2 DACSR<2> - DAC FIFO Empty Flag

This bit indicates that the DAC FIFO is empty.

DACSR<2>	DAC FIFO Empty Flag
READ ONLY	
0	FIFO is not empty
1	FIFO is empty

5.24.3 DACSR<3> - DAC FIFO Full Flag

This bit indicates that the DAC FIFO is full.

DACSR<3>	DAC FIFO Full Flag
READ ONLY	
0	FIFO is not full
1	FIFO is full

5.24.4 DACSR<7> - DAC Error

This bit indicates if an error occurred while running. Error conditions include:

1. FIFO Full (Overflow condition)
2. FIFO Empty (Underflow condition)
3. Bank Swap before completion of readout
4. SYNC bit misalignment

DACSR<7>	DAC Acquisition Error
READ ONLY	
0	No error
1	A DAC error occurred

5.25 DACCR1 - DAC Control register #1

Read/Write

5.25.1 DACCR1<0> - DAC Sampling Clock Source

This bit selects between the internal and external sampling clocks for the DAC. When the board is a slave (i.e. takes its sampling clock from a ICS-150B configured as a master), this bit is a "don't care". Refer to section 4.9 for details of external clock and multiple board configurations.

DACCR1<0>	DAC Sampling Clock Source
READ/WRITE	
0	Internal Sampling Clock
1	External Sampling Clock

5.25.2 DACCR1<1> - DAC Trigger Enable

This bit determines if the external DAC Trigger is used to start data generation. When using an external trigger, triggering occurs following the rising edge of the trigger signal. The signal must remain high for at least two complete clock cycles. This bit is a "don't care" for slave boards.

DACCR1<1>	DAC Trigger Enable
READ/WRITE	
0	Use internal enable (bit DACCR1<7>)
1	Use External Trigger input

5.25.3 DACCR1<3> - DAC Channel Mode

This bit must be set to reflect the operating mode of the DAC, either two channel or four channel. Hardware switches SW5 and SW6 must also be set (see section 4.3 above).

DACCR1<3>	DAC Channel Mode
READ/WRITE	
0	4 Channel mode
1	2 Channel mode

5.25.4 DACCR1<5> - DAC FIFO Select

This bit is used to select either the on-board swing buffer (when installed) or the DAC FIFO sample buffer. In either case, data is read from the ADC/DAC Data area of the memory map.

DACCR1<5>	DAC FIFO Select
READ/WRITE	
0	DAC FIFO selected
1	DAC Swing Buffer selected

5.25.5 DACCR1<6> - DAC Diagnostics enable

This bit is used to enable the DAC Diagnostic mode. In this mode, VMEbus data can be read back from the swing buffer. When cleared, data is written into the swing buffer. When set, data can be read back.

DACCR1<6>	DAC Diagnostics enable
READ/WRITE	
0	Diagnostic Mode disabled
1	Diagnostic Mode enabled

5.25.6 DACCR1<7> - DAC Enable

This bit is used to start the DAC conversion. If external triggering is selected, the conversion begins following the next rising edge of the trigger, otherwise it starts on the next rising clock edge. In multiple board configurations with synchronized trigger, this bit should be set on all slave boards before setting it on the master, in order to arm the slaves. This guarantees that all boards will start conversion simultaneously.

DACCR1<7>	DAC Enable
READ/WRITE	
0	DAC conversion disabled
1	DAC conversion enabled

5.26 DACCR2 - DAC Control Register #2

Read/Write

5.26.1 DACCR2<1:0> - DAC Mode

These bits select between the continuous, loop and one-shot modes of operation. Loop mode requires the Swing Buffer option to be installed.

DACCR2<1:0>	DAC Mode
READ/WRITE	
00	Continuous Mode
01	Loop Mode
10	One-Shot Mode

5.26.2 DACCR2<3:2> - Source Select

These bits control the flow of the DAC data.

DACCR2<3:2>	Source of the DAC Data
READ/WRITE	
00	VMEbus
01	VSB
10	FPDP

5.27 DACDEC<7:0> - DAC Decimation Count

Write Only

This register determines the eight bit decimation count. Setting this register to zero disables decimation. Any other value determines the number of sample clocks between DAC FIFO reads. This effectively reduces the sampling rate, allowing operation of the ICS-150B with an effective sampling rate below 3.75 MHz (4 channel mode) or 7.5 MHz (2 channel mode).

5.28 DACBL - DAC Buffer Length Register

Write only

The DAC Buffer Length Register is used only when the Swing Buffer option is installed on the ICS-150B. The number programmed must always be one less than the buffer length value required. The 19 bit buffer length (+1) determines the number of 32-bit words which may be written to the swing buffer before the buffer banks swap (i.e. half of the total swing buffer length). In continuous mode, following each interrupt, the user should write this number of words to the board. In one-shot mode, the user should write twice this number of words in order to fill the buffer to the correct length prior to starting conversion.

The number of samples per channel contained in the swing buffer depends on whether two or four channel mode is operative. In two channel mode, the number of samples per channel is equal to the programmed swing buffer length (+1). In four channel mode, the swing buffer length (+1) must be divided by two to yield the number of samples per channel. Details of data packing are given in section 5.5.

The number of 32-bit words (not samples) which must be loaded is as follows:

M x(BL+1)

where M = 2 for DAC loop and one-shot modes, and for the first memory load before starting conversion.
M = 1 for DAC continuous mode during normal operation (after first loading of DAC).
BL = value programmed to the buffer length register.

The user must perform a DAC Reset (see DACRST register) after loading DACBL in order for the new buffer length to take effect.

DACBL1<2:0> - DAC Buffer Length Register 1

These bits are bits 18-16 of the 19 bit DAC Swing Buffer Length register.

DACBL2<7:0> - DAC Buffer Length Register 2

These bits are bits 15-8 of the 19 bit DAC Swing Buffer Length register.

DACBL3<7:0> - DAC Buffer Length Register 3

These bits are bits 7-0 of the 19 bit DAC Swing Buffer Length register.

5.29 DACFS - DAC Clock Frequency Select register

Write only

The DAC Clock Frequency Select register is used to program the frequency of the internal DAC clock. The clock is programmable to a resolution of approximately 200Hz. The program word is not in engineering units, and must be calculated by the user, or obtained using a utility function (subroutine) included with the ICS-150B software drivers. Details of the algorithm for computing this programming word are given in section 6.

In multiple board configurations, the clock frequency need only be programmed on the master board.

DACFS1<5:0> - DAC Clock Frequency Select Register #1

These bits are bits 21-16 of the 22 bit clock programming word.

DACFS2<7:0> - DAC Clock Frequency Select Register #2

These bits are bits 15-8 of the 22 bit clock programming word.

DACFS3<7:0> - DAC Clock Frequency Select Register #3

These bits are bits 7-0 of the 22 bit clock programming word. When programming a new frequency value, this register should be written last, since upon completion of a write to this register the entire 22 bit clock programming word is shifted out to the clock generator. The valid programming range for the ICS-150B is 3.75 MHz to 40 MHz.

5.30 MRESET - Master Reset

Write only

A write to this register masks all interrupts, resets all control register bits to their power-up defaults (zero) and resets all on-board memory. SCV64 registers and status are unaffected. The data written to the register is unimportant.

5.31 ADCRST - ADC Reset

Write only

A write to this register resets the ADC FIFO and the ADC swing buffer (if installed) memory pointers. It does not alter memory contents. The value written to the register is unimportant. This register must be written to after configuring the ADC section and before enabling acquisition in order for the FIFO and Swing Buffer memory to be correctly initialized.

5.32 DACRST - DAC Reset

Write only

A write to this register resets the DAC FIFO and the DAC swing buffer (if installed) memory pointers. It does not alter memory contents. The data written to the register is unimportant. This register must be written to after configuring the DAC section and before writing data to the FIFO or Swing Buffer memories and enabling the DAC section, in order for the memory to be correctly initialized.

5.33 FPDPCTRL - FPDP Control Register

Write only

The FPDP Control register determines the operating modes of the two Front Panel Data Port (FPDP) connectors P3 and P4. The FPDP is a synchronous multiplexed parallel data port which may be used to connect one or more ICS-150B boards with an array processor (Digital Signal Processor) by means of a simple ribbon cable connection. P3 is used to provide data to the ICS-150B DAC, while P4 is used to output data from the ICS-150B ADC. Since the FPDP specification requires the data source to generate the FPDP clock, the P4 (ADC) control includes clock frequency selection, while the P3 (DAC) control does not. The FPDP clock not synchronous with sampling operations on the ICS-150B and therefore the FPDP clock frequency should be selected so that it is high enough to handle the peak data rate provided by the ADC. A full description of the FPDP interface and operation is given in section 3.8 above.

5.33.1 FPDPCTRL<6> - P4 Bus Width

This bit selects the width of the P4 port. In 24 bit mode, channels A1 (d23:12) and A2 (d11:00) are clocked out simultaneously, followed by B1 (d23:12) and B2 (d11:00). In 12 bit mode, only bits d23:12 are used, and each channel is clocked out separately. (i.e. A1 followed by A2 followed by B1 followed by B2). See Table 3.1 above for a full list of P4 connections.

FPDPCTRL<6>	P4 Bus Width
WRITE ONLY	
0	Port is 24 bits wide (d23:d00)
1	Port is 12 bits wide (d23:d12)

5.33.2 FPDPCTRL<5:4> - P4 mode

These bits control the output data rate of the P4 FPDP.

FPDPCTRL<5:4>	P4 Mode
WRITE ONLY	
00	Port is disabled
01	10 MHz Output Data Rate
10	20 MHz Output Data Rate
11	40 MHz Output Data Rate

5.33.3 FPDPCTRL<2> - P3 Bus Width

This bit selects the width of the P3 port. In 24 bit mode, channels A1 (d23:12) and A2 (d11:00) are clocked in simultaneously, followed by B1 (d23:12) and B2 (d11:00). In 12 bit mode, only bits d23:12 are used, and each channel is clocked in separately. (i.e. A1 followed by A2 followed by B1 followed by B2).

FPDPCTRL<2>	P3 Bus Width
WRITE ONLY	
0	Port is 24 bits wide
1	Port is 12 bits wide

5.33.4 FPDPCTRL<1:0> - P3 mode

These bits are used to enable the P3 FPDP.

FPDPCTRL<1:0>	P3 mode
WRITE ONLY	
00	Port is disabled
01	Port is enabled

5.34 VSB Memory Map

The layout of the VSB Memory Map is shown in Fig. 11. Most aspects of VSB configuration, such as selection of whether interrupts are polled or vectored and enabling of the VSB slave image, are programmed from the VMEbus. See the descriptions of registers VSBSCR, VSBMCR, and VSBBAR in sections 5.10-5.12 above. Data transfer, interrupt enabling and interrupt request status are available on the VSB. These are described below.

5.34.1 ADC/DAC Data

This section of the ICS-150B's VSB memory map is used to move data from the ADC memory to the VSB, and to move data to the DAC memory from the VSB. This area of the map is used for access to data regardless of which memory buffer is being used, i.e. FIFO, Swing Buffer or Daughter Card Memory Buffer.

The organization of data when read from or written to this space is the same as for the VMEbus ADC/DAC Data area. Please refer to section 5.5 above for details concerning data access.

5.34.2 VSBBSAI - VSB Bus Status Register/ADC Interrupt Enable

Read/Write

When written to, this register enables VSB ADC interrupts. The data written is unimportant. Interrupts must be reenabled after every occurrence. The criteria for an ADC interrupt to occur are the same as for the VMEbus ADC interrupt.

When read from, the register provides information on the VSB Global Address of the board and the interrupt request status. Details are given below.

5.34.3 VSBBSAI<26:24> - VSB Global Address

These bits reflect the VSB Backplane Global Address GA0-2 of the ICS-150B in accordance with the VSB Bus Specification. This information is also available from VMEbus register VSBSR (see section 5.9.1 above).

VSBBSAI<26:24> VSBBSDI<26:24>	VSB Backplane Global Address
READ ONLY	
000	VSB Slot 1
001	VSB Slot 2
010	VSB Slot 3
011	VSB Slot 4
100	VSB Slot 5
101	VSB Slot 6

5.34.4 VSBBSAI<27> - DAC Interrupt Request

This bit indicates that the ICS-150B is asserting a DAC interrupt.

VSBBSAI<27> VSBBSDI<27>	DAC Interrupt Request
READ ONLY	
0	DAC interrupt is not asserted
1	DAC interrupt is asserted

5.34.5 VSBBSAI<29> - ADC Interrupt Request

This bit indicates that the ICS-150B is asserting an ADC interrupt.

VSBBSAI<29> VSBBSDI<29>	ADC Interrupt Request
READ ONLY	
0	ADC interrupt is not asserted
1	ADC interrupt is asserted

5.34.6 VSBBSAI<31> - VSB Interrupt Request

This bit indicates that the ICS-150B is generating a VSB ADC or DAC interrupt.

VSBBSAI<31> VSBBSDI<31>	VSB Interrupt Request
READ ONLY	
0	VSB interrupt is not asserted
1	VSB interrupt is asserted

5.34.7 VSBBSDI - VSB Bus Status Register/DAC Interrupt Enable

Read/Write

When written to, this register enables VSB DAC interrupts. The data written is unimportant. Interrupts must be reenabled after every occurrence. The criteria for an ADC interrupt to occur are the same as for the VMEbus ADC interrupt.

When read from, the register provides the same information on the VSB Global Address of the board and the interrupt request status as is given by register VSBBSAI described above. Please refer to that description for details.

6 PROGRAMMING THE INTERNAL ADC AND DAC CLOCK GENERATORS

The internal ADC and DAC clock generators must be programmed to produce the desired frequency/s when the internal sampling clock/s have been selected in the ADC or DAC Control registers. The frequency for each oscillator is programmed by means of a 22-bit programming word which is programmed to the ADC Frequency Select and/or DAC Frequency Select register sets.

Automatic calculation of the programming word is provided by the calcFoxWord() function and other functions in the 'C' language function library supplied with the optional ICS-150 software drivers, available for SunOS or VxWorks environments. These routines generate a 22-bit formatted programming word equivalent to the nearest possible frequency to that supplied as input by the user (in MHz), and also supply the actual frequency represented by the programming word.

Following programming, it takes up to 10ms for the oscillator to reach the final frequency.

The programming word contains 5 fields:

FIELD	BITS	# OF BITS	NOTES
Index (I)	<21:18>	4	MSB (Most Significant Bits)
P Counter value (P)	<17:11>	7	
Reserved (R)	<10>	1	normally set to logic 1
Mux (M)	<9:7>	3	
Q Counter Value (Q)	<6:0>	7	LSB (Least Significant Bits)

The output is derived from a reference clock (14.31818MHz), and the output frequency, f_{VCO}, is a function of the parameters listed above, as follows:

$$f_{VCO} = 2 \times f_{REF} \times \frac{(P+3)}{(Q+2)}$$

where, f_{REF} = Reference frequency (i.e. 14.31818 MHz)

The values of the parameters must be selected so that f_{VCO} remains between 40MHz and 120MHz, inclusive. However, a division register is also provided on board the oscillator to allow sub-multiples of the frequency to be obtained. The value of the divisor is selected by programming the Mux field (M) as follows:

M	Divisor	M	Divisor
000	1	100	16
001	2	101	32
010	4	110	64
011	8	111	128

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to the VCO frequency f_{VCO} rather than to the desired output frequency.)

I	f_{vco} (MHz)	I	f_{vco} (MHz)	I	f_{vco} (MHz)
0000	40.0 - 42.5	0110	68.5 - 69.0	1011	92.1 - 105.0
0001	42.5 - 47.5	0111	69.0 – 82.0	1100	105.0 - 115.0
0010	47.5 - 53.5	1000	82.0 - 87.0	1101	115.0 - 115.0
0011	53.5 - 58.5	1001	87.0 - 92.0	1110	115.0 – 120.0
0100	58.5 - 62.5	1010	92.0 - 92.1	1111	115.0 - 120.0
0101	62.5 - 68.5				

If the desired VCO frequency lies on a boundary in the table -- in other words, if it is exactly the upper limit of one entry and the lower limit of the next -- then either index value may be used (since both limits are tested), but the manufacturer recommends using value corresponding to the higher frequency range.

Programming Constraints

There are four primary programming constraints the user must be aware of. The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation.

1. $200\ kHz \leq \frac{14.31818\ MHz}{Q} \leq 1\ MHz$

2. $40\ MHz \leq f_{vco} \leq 120\ MHz$

3. $1 \leq P \leq 127$

4. $1 \leq Q \leq 127$

Programming Example

Derive the proper programming word for a 39.5 MHz output frequency:

Since 39.5 MHz < 40 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0111. The result:

$$f_{out} = 39.5 = (2 \times 14.31818 \times (P+3)/(Q+2))/2^{M}$$

$$m = 1$$

Since m=1, $\frac{(P+3)}{(Q+2)} = 2.7587$

Several choices of P and Q are available:

P	Q	f_{vco}	Error (PPM)
66	23	79.0363	460
77	27	78.9969	40
88	31	78.9669	419

Choose (P,Q) = (77,27) for best accuracy (40 PPM).

Therefore:

P = 77 = 1001101
Q = 27 = 0011011

and the full programming word, W, is:

W = I, P, R, M, Q = 0111,1001101,1,001,0011011
= 011110011011001011011

or (in hexadecimal) 0x01e6c9b

