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CHAPTER 5
REGISTERS

The PCVISION*plus* Frame Grabber contains twelve 8–bit registers that you can access through the IBM PC bus to control the operation of the PCVISION*plus* Frame Grabber. These are illustrated in Figure 5–1 with their offsets. Sixteen contiguous locations are reserved by the PCVISION*plus* Frame Grabber.

These registers are located starting at the Register Base Address. This address is selected using jumpers on the PCVISION*plus* Frame Grabber (as discussed in Chapter 2).

This chapter describes each of the registers and individual bit functions in detail. The [R/W] notation after a bit name indicates that the bit is a read/write bit. The [R–O] notation indicates that the bit is read–only (status bits). The [W–O] notation indicates that a bit or register is write–only. Numbers followed by the letter H are in hexadecimal notation. Numbers followed by the letter B are in binary notation.

NOTE

The PCVISION*plus* Frame Grabber performs a power–up reset on the Control, LUT Control, Pan, and Scroll registers. Your application program must initialize all other registers; otherwise, results are unpredictable.

Base Address +		*Refer to Page #*
0H	CONTROL	5-3
1H	LUT CONTROL	5-7
2H	LUT ADDRESS	5-9
3H	LUT DATA PORT	5-9
4H	GAIN/OFFSET	5-10
5H	ACQUIRE/STATUS	5-12
6H	PAN	5-15
7H	SCROLL	5-15
8H	MEM ACCESS CONTROL	5-16
9H	HOST MASK	5-18
AH	VIDEO ACQ MASK	5-18
BH	PIXEL BUFFER	5-19
CH	*RESERVED*	
DH	*RESERVED*	
EH	*RESERVED*	
FH	*RESERVED*	

Figure 5-1. PCVISION*plus* Control Registers

5.1 CONTROL REGISTER [R/W]

Base Address + 0H

7							0
BLOCK2	BLOCK1	BLOCK0	BDSEL	DIR	OFFEN	GAINEN	ZOOM

The Control register specifies various board functions dealing with both host access and video acquisition and display.

BIT	MNEMONIC	FUNCTION
0	ZOOM	Zoom Enable
1	GAINEN	Gain Adjust Enable
2	OFFEN	Offset Adjust Enable
3	DIR	Adjust Direction Control
4	BDSEL	Board Select
5	BLOCK0	Memory Block Select, Bit 0
6	BLOCK1	Memory Block Select, Bit 1
7	BLOCK2	Memory Block Select, Bit 2

5.1.1 Zoom Enable (ZOOM) [R/W]

The zoom enable bit enables and disables the zoom display factor. Refer to Chapters 1 and 4 for an explanation of the zoom process. This bit affects how frame memory is addressed during scan cycles. When zoom is enabled, the entire frame memory is addressed in a zoom mode. All video access (display and acquire) has the same zoom factor. During a continuous acquisition, only change the zoom bit during the vertical blanking period.

State	Function
0	Zoom factor 1; normal scan
1	Zoom factor 2; pixel replication

5.1.2 Gain Adjust Enable (GAINEN) [R/W]

The gain adjust enable bit assigns the Gain/Offset Counter to adjust the programmable gain. When set (1), the gain value is fixed in nonvolatile memory. The gain is adjustable from .67 to 1.33, in 100 counts or steps as described later in this chapter, under "Gain and Offset Counter."

State	Function
0	Counter adjusts gain
1	Gain is fixed

5.1.3 Offset Adjust Enable (OFFEN) [R/W]

The offset adjust enable bit assigns the Gain/Offset Counter to adjust the programmable offset voltage level. When this bit is set (1), the offset value is fixed in nonvolatile memory. The offset is adjustable from −0.1V to +1V, in 100 steps or counts as described later in this chapter, under "Gain and Offset Counter."

State	Function
0	Counter adjusts offset
1	Offset is fixed

5.1.4 Adjust Direction Control (DIR) [R/W]

The DIR bit causes the gain or offset circuitry to either increment or decrement with the Gain/Offset Counter. GAINEN or OFFEN or both must be 0 to enable adjustment.

State	Function
0	Decrement
1	Increment

5.1.5 Board Select (BDSEL) [R/W]

The Board Select bit (BDSEL) enables the frame memory onto the PC bus. This bit must be set (1) for the host PC to access pixel data. BDSEL is useful in multiple–board systems where the frame memory of each board is mapped to the same Memory Base Address in the PC. Do not enable more than one board onto the PC bus at any one time. This bit is zero at power–up reset.

State	Function
0	Board disabled
1	Board enabled

5.1.6 Memory Block Select (BLOCK) [R/W]

The frame memory is mapped into the PC memory address space in 64K byte blocks. The frame memory is divided into eight 64K blocks according to one of the two patterns shown in Figures 5–2 and 5–3. The Memory Block Select bits select the block that is mapped into memory at a given time.

BLOCK2	BLOCK1	BLOCK0	Block Selected
0	0	0	Block 0
0	0	1	Block 1
0	1	0	Block 2
0	1	1	Block 3
1	0	0	Block 4
1	0	1	Block 5
1	1	0	Block 6
1	1	1	Block 7

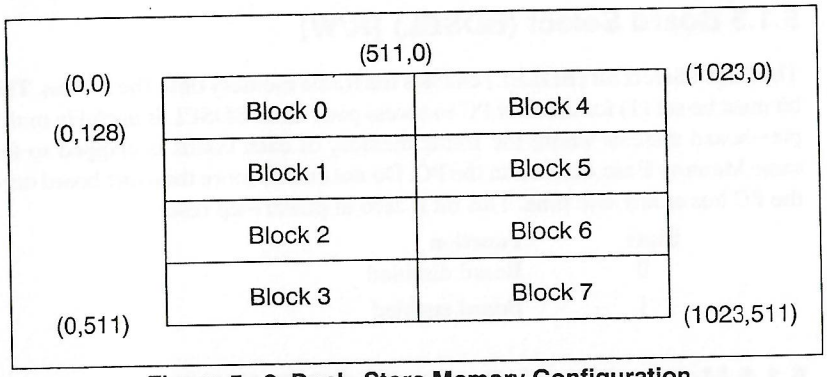


Figure 5-2. Dual-Store Memory Configuration

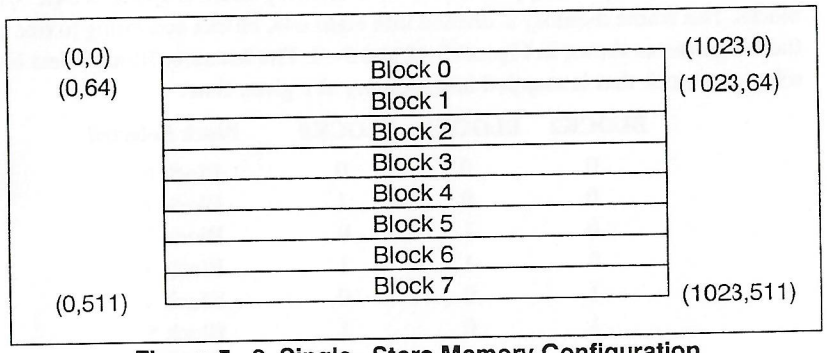


Figure 5-3. Single-Store Memory Configuration

5.2 LUT CONTROL REGISTER [R/W]

Base Address + 1H

7							0
OLUT2	OLUT1	OLUT0	ILUT2	ILUT1	ILUT0	LUTMOD1	LUTMOD0

The Look–Up Table Control register controls the selection of the various LUTs on the PCVISION*plus* for display and host access.

BIT	MNEMONIC	DESCRIPTION
0	LUTMOD0	Look–Up Table Mode, Bit 0
1	LUTMOD1	Look–Up Table Mode, Bit 1
2	ILUT0	Input LUT Select, Bit 0
3	ILUT1	Input LUT Select, Bit 1
4	ILUT2	Input LUT Select, Bit 2
5	OLUT0	Output LUT Select, Bit 0
6	OLUT1	Output LUT Select, Bit 1
7	OLUT2	Output LUT Select, Bit 2

5.2.1 Look–Up Table Mode (LUTMOD) [R/W]

The LUTMOD bits select one of four sets (channels) of LUTs for host access. These bits have no effect on video display.

LUTMOD1	LUTMOD0	LUT Set Selected
0	0	Red
0	1	Green
1	0	Blue
1	1	Input

5.2.2 Input LUT Select (ILUT) [R/W]

The Input Look-Up Table Select bits (ILUT2-0) activate one of eight input LUTs for host access or transformation of the video input. These bits affect both host access and video processing.

ILUT2	ILUT1	ILUT0	LUT Selected
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.2.3 Output LUT Select (OLUT) [R/W]

The Output Look-Up Table Select bits (OLUT2-0) select an output bank, in other words three LUTs are defined, one within each channel of output LUTs for transformation of the video output data. The same numbered LUT from each color channel is used simultaneously. For host access only one LUT from one color set or group is used as defined by the LUTMOD bits. Bank is a display operation only.

OLUT2	OLUT1	OLUT0	LUTs Selected
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.3 LUT ADDRESS REGISTER [R/W]

Base Address + 2H

LUTADR

7							0
ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0

The Look–Up Table Address register specifies an eight–bit address in the selected LUT. Data written to the LUT Data Port is stored at this address, in the LUT selected by the LUT Control register.

5.4 LUT DATA PORT [R/W]

Base Address + 3H

LUTDAT

7							0
DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

The Look–Up Table Data Port is used with the LUT Address and LUT Control register to program or read the Look–Up Tables. When you write to the LUT Data Port, the data is transferred to the LUT specified by the OLUT or ILUT bits in the LUT Control register, at the address specified by the LUT Address register.

5.5 GAIN AND OFFSET COUNTER [W-O]

Base Address + 4H

7							0
COUNT7	COUNT6	COUNT5	COUNT4	COUNT3	COUNT2	COUNT1	COUNT0

This register is used to increment or decrement the gain or offset of the input signal as determined by the GAINEN, OFFEN, and DIR bits in the Control register. Each time you write to this register, the counter is increased or decreased by one step. The actual data value written to this counter is ignored. You cannot program a specific value in this counter. There are 100 positions or steps in the adjustment range (0 to 99). Disabling the gain adjust (GAINEN) or offset adjust (OFFEN) saves the current adjustment in non-volatile memory.

NOTE

The circuit controlling offset and gain has a time-out of 7 microseconds. Some personal computers can write data faster than this. Your program must include a delay of at least 10 microseconds between each write to the gain and offset counter.

As shipped from the factory, Gain is 1 (at a possible count of 49 to 51), and offset is zero (at a possible count of 74 to 76). At these settings, a full-scale RS-170 or CCIR input of 0.714 Volts gives an ADC value of 255 decimal or FFH.

The Gain is adjustable from 0.67 to 1.33, in 100 steps (.0066 per step). The maximum gain of 1.33 corresponds to a counter setting of 0. The minimum gain of 0.67 corresponds to a counter setting of 99. The output of the ADC decreases when you increase the counter (decrease the gain).

The offset is adjustable from −0.854 to +0.266 Volts in 100 steps (1.12 mV per step). The maximum negative offset corresponds to a counter setting of 0. The maximum positive offset corresponds to a counter setting of 99. The output of the ADC increases when you increase the counter (decrease negative offset).

To program the counter to a repeatable setting: program DIR = 1 (increase), adjust to full-scale (position 99) by writing to the counter 101 times, program DIR = 0 (decrease), and adjust by writing to the counter the number of counts needed.

Always adjust the offset first, to make the video black level yield an ADC output of 0, and then adjust the gain to make the video white level yield an ADC output of 255 (FFH).

Figure 5–4 illustrates the internal operation of the gain and offset circuits. The gain counter adjusts the ADC full–scale voltage from 3 to 6 Volts. The minimum gain of 0.67 corresponds to counter position 99 or ADC full–scale 6 Volts. The maximum gain of 1.33 corresponds to counter position 0 or ADC full–scale 3 Volts. The resolution of full–scale adjustment is 30 mV/count.

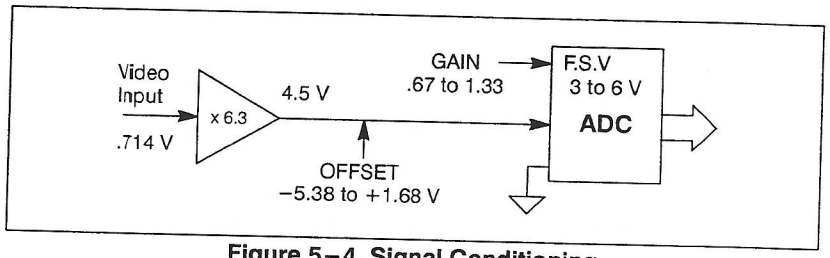


Figure 5–4. Signal Conditioning

The offset counter adjusts the added offset after the 6.3 gain amplifier from −5.38 to +1.68 Volts. The offset is −5.38 Volts at counter position 0. The offset is +1.68 at counter position 99. The resolution is 70.6 mV/step at the ADC input. Dividing these voltage values by 6.3 gives the offset adjustment the video input −0.854 to +0.266 Volts, and 1.12 mV/count.

The relative weight of the offset increases as gain is reduced. At a gain of 1.33, the resolution of the ADC is: 3 VFS/256 ADC steps = 11.71 mV/ADC step; and the resolution of the offset counter is: 70.6 mV/11.71 mV/step = 6.02 ADC steps/offset count. At a gain of 1, the resolution of the ADC is: 4.5 VFS/256=17.58 mV/ADC step; and the resolution of the offset is: 70.6 mV/17.57 mV/step = 4.0 ADC steps/offset count. At a gain of 0.67, the resolution of the ADC is: 6 VFS/256=23.4mV/step; and the resolution of the offset is: 70.6 mV/step / 23.4 mV/step = 2.17 ADC steps/offset count.

5.6 ACQUIRE AND STATUS REGISTER [R/W]

Base Address + 5H

7							0
ACQMD1	ACQMD0	HBS	VBS	LFS	OES	CLOCK	VIDSEL

The Acquire and Status register controls the video input select and the acquisition modes. The four status bits for the PCVISION*plus* Frame Grabber are also contained in this register.

BIT	MNEMONIC	DESCRIPTION
0	VIDSEL	Video Input Select
1	CLOCK	Clock Source Select
2	OES	Odd/Even Status
3	LFS	Last Field Status
4	VBS	Vertical Blank Status
5	HBS	Horizontal Blank Status
6	ACQMD0	Acquire Mode, Bit 0
7	ACQMD1	Acquire Mode, Bit 1

5.6.1 Video Input Select (VIDSEL) [R/W]

The PCVISION*plus* has two video input channels. The VIDSEL bit controls the channel selected.

State	Function
0	Channel 0
1	Channel 1

5.6.2 Clock Source Select (CLOCK) [R/W]

This bit controls the selection of either the phase-locked loop (PLL) or the crystal oscillator as the system clock source, as described in Chapter 4 of this manual, "Timing and Synchronization."

State	Function
0	Crystal Oscillator
1	Phase-Locked Loop

5.6.3 Odd/Even Field Status (OES) [R–O]

This bit indicates when the currently displayed field is the odd or even field of an interlaced image. This bit changes at the leading edge of the vertical synchronization pulse.

State	Function
0	Even Field Displayed
1	Odd Field Displayed

5.6.4 Last Field Status (LFS) [R–O]

This bit indicates when the PCVISION*plus* is acquiring the second field of a snap, or the last field of a grab, signaling the end of an acquire operation. In continuous acquire mode, this bit is set before the second field is acquired and remains set until another command is issued. This bit changes at the trailing edge of the vertical synchronization pulse.

State	Function
0	Acquiring Last Field
1	Not Acquiring Last Field

5.6.5 Vertical Blank Status (VBS) [R–O]

This bit indicates a vertical blanking interval, and remains active for 1.4 ms.

State	Function
0	Vertical Blanking
1	Not Blanking

5.6.6 Horizontal Blank Status (HBS) [R–O]

This bit indicates a horizontal blanking interval, and is active for 12.7 ms.

State	Function
0	Horizontal Blanking
1	Not Blanking

5.6.7 Acquire Mode (ACQMD) [R/W]

These two bits are used for both control and status. The control function appears in italics. The status operation is explained immediately after.

ACQMD1	ACQMD0	Write	Read
0	0	Freeze	No operation in progress
0	1	Clear	N/A
1	0	Snap	N/A
1	1	Grab	Acquire or Clear in progress

Freeze — Terminate a clear or acquire operation. When read, this value indicates that no operation is in progress.

Clear — Initiate a clear frame memory operation. At the trailing edge of the next vertical synchronization pulse of the even field, the contents of these bits change to 1,1 indicating the clear operation has begun. All pixels in frame memory are set to the value currently held in the Pixel Buffer register. Bit-planes protected in the Host Mask register are not affected. ACQMD0 and ACQMD1 remain as 1 for one frame time, then change to 0 indicating completion of the clear operation.

Snap — Acquire a single frame only. At the trailing edge of the next vertical synchronization pulse of the even field, ACQMD0 changes to 1 indicating the acquire operation has begun. Bit-planes protected in the Video Acquisition Mask register are not affected. After one frame time, both bits change to 0, indicating completion of the snap operation.

Grab — Acquire images continuously. These bits remain set until some other command is issued. Bit-planes protected in the Video Mask Acquisition register are not affected.

5.7 PAN REGISTER [R/W]

Base Address + 6H

7							0
Reserved	PAN6	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0

The Pan register holds the 7–bit starting horizontal offset of the frame memory scan circuit. Pan resolution is on eight pixel boundaries. Every increment of this register moves the active video window (AVW) eight pixel positions to the right across the frame memory.

This register can be updated at any time. The new pan value is accepted during the next horizontal blanking period.

5.8 SCROLL REGISTER [R/W]

Base Address + 7H

7							0
Reserved	SCROL6	SCROL5	SCROL4	SCROL3	SCROL2	SCROL1	SCROL0

This register holds the 8–bit starting vertical offset of the frame memory scan circuit. Scroll resolution is on two–line boundaries. Every increment of this register moves the AVW down two lines in the frame memory.

This register can be updated at any time. The new scroll value is accepted during the next vertical blanking period.

5.9 MEMORY ACCESS CONTROL REGISTER [R/W]

Base Address + 8H

7							0
Reserved	PBEN	Reserved	TMODE	Reserved	PS2	PS1	PS0

The Memory Access Control register controls host computer access to the frame memory.

BIT	MNEMONIC	DESCRIPTION
0	PS0	Plane Select, Bit 0
1	PS1	Plane Select, Bit 1
2	PS2	Plane Select, Bit 2
3	Reserved	"Don't Care"
4	TMODE	Transfer Mode
5	Reserved	"Don't Care"
6	PBEN	Pixel Buffer Enable
7	Reserved	Must be 0

5.9.1 Plane Select (PS) [R/W]

The Plane Select bits select one frame memory plane for access by the PC using X-Mode. Three plane select bits, (PS2-0) select one bit-plane from 0 through 7. These bits have no effect in Z-mode.

PS2	PS1	PS0	Bit Plane
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

5.9.2 Transfer Mode (TMODE) [R/W]

This bit specifies the transfer mode (X– or Z–Mode) for accessing frame memory data from the host computer.

State	Function
0	Z–Mode: One pixel is transferred during frame memory read or write from the host bus.
1	X–Mode: From 1 to 8 horizontally–adjacent pixels are transferred from one memory plane during frame memory read or write from the host bus.

5.9.3 Pixel Buffer Enable (PBEN) [R/W]

This bit applies only during Z–Mode memory write. PBEN enables the Pixel Counter, and allows the Pixel Buffer to accept data from the PC during a frame memory write cycle. The Pixel Counter is used in Z–Mode when loading the Pixel Buffer from the host, and when writing to frame memory. In all other read and write modes this bit and the Pixel Counter are ignored. When PBEN is cleared, the Pixel Buffer contents and the Pixel Counter are protected from the host computer during write operations. This function is useful in screen clear and block move operations.

State	Function
0	Pixel Buffer PROTECTED: Pixel Buffer contents are protected from the host during frame memory writes. The contents are used repeatedly in later memory write cycles.
1	Pixel Buffer ENABLED: Data from the host is strobed into the Pixel Buffer during a frame memory write, and Pixel Counter is reset.

5.10 HOST MASK REGISTER [R/W]

Base Address + 9H

7							0
PLANE7	PLANE6	PLANE5	PLANE4	PLANE3	PLANE2	PLANE1	PLANE0

This register is used to individually write-protect entire bit-planes in frame memory during host access and frame memory clear operations. A protected plane is not changed or written to. The eight bits of this register correspond directly to the eight bit-planes in frame memory. Bit zero is used to write protect plane zero (the LSB of all pixel data), and bit seven protects plane seven.

State	Function
0	Bit-plane NOT PROTECTED: The corresponding bit-plane is modified by host write accesses and clear operations.
1	Bit-plane PROTECTED: The corresponding bit-plane is protected during host accesses and clear operations.

5.11 VIDEO MASK REGISTER [R/W]

Base Address + AH

7							0
PLANE7	PLANE6	PLANE5	PLANE4	PLANE3	PLANE2	PLANE1	PLANE0

This register is used to individually write-protect entire bit-planes in frame memory during image acquisition. The bits in this register correspond to the eight bit-planes in the frame memory. Bit zero is the least significant bit-plane.

State	Function
0	Bit-plane NOT PROTECTED: The corresponding bit-plane is modified during image acquisition operations.
1	Bit-plane PROTECTED: The corresponding bit-plane is protected during image acquisition operations

5.12 PIXEL BUFFER REGISTER [R/W]

Base Address + BH

7							0
BUFF7	BUFF6	BUFF5	BUFF4	BUFF3	BUFF2	BUFF1	BUFF0

This register is a data port that provides access to the Pixel Buffer. Data is loaded into the Pixel Buffer from the host computer and then transferred to frame memory in one host computer frame memory write access. Alternatively, eight pixels are loaded into the Pixel Buffer from the frame memory by a host frame memory read access, and then accessed by the host computer through this register or transferred back into frame memory by a write cycle. Refer to Chapter 4 for details on the Pixel Buffer operation.

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