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MVC 150/40

IMS Hardware

Reference Manual

47-H54002-01

iMAGING Technology

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IMS Hardware Reference Manual

Document Number **47-H54002-01**

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PREFACE

The IMS (Standard Image Manager) is a single VME board with up to three plug-in modules for camera, display, and computation. The IMS provides configurable frame memory, multiple data paths, and local pipelined processing. The IMS can operate as a video bus master only.

- Chapter 1, “Overview” introduces the IMS and provides a list of specifications.
- Chapter 2, “Theory of Operation” describes the operation of the IMS.
- Chapter 3, “Registers” provides register and bit definitions for all control and status registers.
- Chapter 4, “Configuration” describes the IMS factory default configuration and how to change each reconfigurable option. Use the board diagram at the end of this chapter to document any changes made to the factory configuration.
- Appendix A, “IMS Connectors” details the pin-out of the connectors on the IMS-150 front plate.
- Appendix B, “Video Cables and Connectors” describes the video input cables available for the IMA.

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DOCUMENTATION CONVENTIONS

The following conventions are used throughout this manual:

Example	Description
CAUTION	A caution calls attention to a hazard to the equipment or software; a condition, practice, or procedure that must be observed to avoid damage to or destruction of equipment.
NOTE	A note calls attention to essential information of special importance, interest, or assistance in operation.
0110B	Binary numbers are followed by a B.
0x3F0, 03F0H	Hexadecimal numbers are preceded by 0x or followed by an H.
AM	Acquisition Module; a plug-in camera interface.
AM-CLR	The color acquisition module.
AM-VS	The variable-scan acquistion module.
AM-DIG	The digital acquisition module.
AM-FA	The fast analog acquistion module.
CPS	Cross-Port Switch, a video data multiplexer.
IMS	The MVC 150/40 standard image manager.
R/W	The bit or register supports both read and write access.
R-O	The bit or register supports read access only.
W-O	The bit or register supports write access only.
X	When used within a table, this notation indicates an irrelevant bit value, also called a “don’t care”.

This manual documents registers using the Motorola “big-endian” convention. The high order register byte is on an even byte address (2H) and the low order register byte is on an odd byte address (3H). Word access is defined to be a VMEbus I/O cycle during which both DS0 (Data Strobe 0) and DS1 (Data Strobe 1) are asserted.

The Intel™ 80286 and most personal computer processors use the opposite convention. Intel addresses words at even addresses (for example, 2H). The low order register byte is on an even byte address (2H) and the high order register byte is on an odd byte address (3H).

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CHAPTER 1
OVERVIEW

The IMS (standard image manager) is a single VME board containing image memory, Cross–Port Switches for data routing, an AOI (area–of–interest) timing generator, video bus interface, and support for three plug–in modules: AM (acquisition module), CM (computation module, and DM (display module). The modules provide flexible camera and display interfaces as well as local processing capabilities. The IMS controls the time base for the MVC 150/40™ subsystem. The IMS is available with 3MB (megabytes) or 1.5MB of image memory.

1.1 VIDEO DATA STORAGE

The IMS image memory stores digitized images at. The image memory is organized as three frames; A0, A1, and B1. The 1.5MB IMS has three 1024 pixel by 512 line by 8–bit frames. The 3MB IMS has three 1024 pixel by 1024 line by 8–bit frames. Multiple asynchronous data paths have access to the frame stores. The IMS memory architecture supports pan, scroll, and zoom in hardware. This hardware reduces the software overhead usually needed for these functions.

A single IMS contains sufficient image memory needed in an image processing subsystem; however, up to three IMA boards can be connected to the IMS through the 150/40 video bus for increased on–line image storage. The IMS supports a single CM (computation module). Up to three CMC (computation module controller) boards can be connected to the IMS through the 150/40 video bus for increased computation capacity. Each CMC supports three CMs.

1.2 HOST ACCESS

The IMS control and status registers occupy 128 words in the VME short word address space. An 8–pin switch selects the 16–bit I/O base address. Registers respond to VME bus privileged (supervisory) and non–privileged data access, short word addressing.

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The IMS allows the host CPU direct access to frame memory data. The frame memory is mapped into the host memory address space as a software–selectable block of size 1MB, 2MB, or 4MB. The IMS supports both standard (A24) and extended (A32) addressing.

The image memory and modules (AM, DM, CM) share the same memory address space. The IMS manages access between memory and modules through paging. The IMS is software enabled (or disabled) onto the memory address space. Multiple MVC 150/40 boards may share the same block of memory address space, but each board must have a unique I/O address.

1.3 VIDEO BUS

The 150/40 video bus interconnects MVC 150/40 boards and runs at a 40 MHz pixel rate. The video bus has a 24–bit global bus driven by the IMS and a 24–bit pipeline bus. Figure 1–1 shows how boards are interconnected. The IMS controls the timebase for the whole MVC 150/40 subsystem. Only one IMS is allowed in a subsystem. The slaves may be IMA (advanced image manager) or CMC (computation module controller) boards.

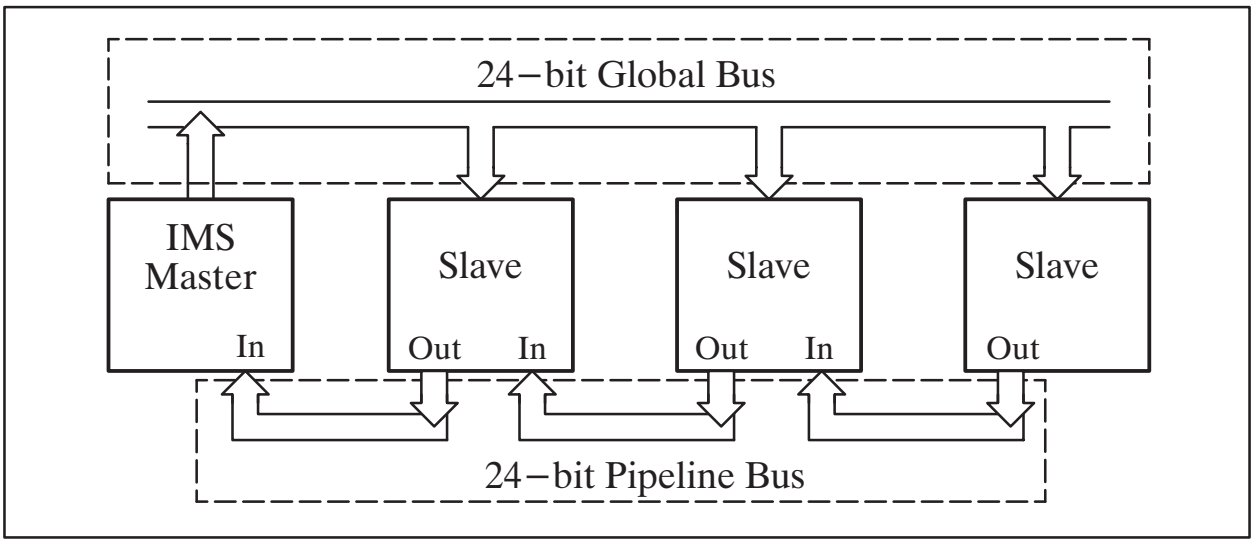


Figure 1−1. 150/40 Video Bus

The global bus connects to all MVC 150/40 boards on the video bus. The global bus is driven with camera or AOI timing. An IMS can drive data from any of its three image stores onto any byte of this bus. The IMS can only output data onto the Global bus. The IMS cannot receive data on the global bus.

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CAUTION *Every IMA must have a different processor number! If two boards have the same number, damage can result when you select that number to drive the Global Video Bus. The processor number is selected by hardware switches on the IMA.*

The pipeline bus connects between two adjacent boards. The pipeline bus transmits 24–bit resultant images back to the IMS. Some MVC 150/40 boards have a pipeline input and a pipeline output. The IMS has a pipeline input only.

1.4 IMS SPECIFICATIONS

This section gives the detailed operating specifications for the IMS.

1.4.1 Image Memory

- Frame Memory Size —
  3MB version; 1024 by 1024 pixels by 24 bits
  1.5MB version; 1024 by 512 by 24–bits
- Organized as 3 separate frame stores: A0, A1, B1; each frame 8–bits per pixel
- Supports AOI processing of images up to 1024 pixels by 1024 lines
- Individual bit–planes protected from host access.
- Independent read pan and scroll, and write pan and scroll, for each frame store
- Hardware pan on single pixel boundaries (display pan on 2 pixel boundaries)
- Hardware scroll on single line boundaries
- Sub–sample acquire (÷2). Allows 50% image reduction into any frame
- Display zoom — in frame B1 only, 1X, 2X, 4X by pixel replication.

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1.4.2 Host Interface

- Standard VME P1 and P2 connectors.
- IMS control and status registers occupy 64 words in the VME short word (A16) address space.
- Image memory and modules are mapped into host memory address space, as 1MB, 2MB, or 4MB block. Map enable, block size, and memory base address are software controlled.
- Page register moves 1MB block through 3MB memory, and selects between the three modules (AM, CM, DM)
- Physical addresses (for memory base address A00000H) —
  frame A0: A00000H to AFFFFFH (starts at base address +0H);
  frame A1: B00000H to BFFFFFH (starts at base address +100000H);
  Reserved area: C00000H to CFFFFFH (starts at base address +200000H);
  frame B1: D00000H to DFFFFFH (starts at base address +300000H)

1.4.3 Physical Parameters

- Board Size — 9.375 inches by 6.375 inches; 239 mm by 163 mm.
- Operating Temperature — 10–60 degrees Celsius.
- Relative Humidity — 0–90% non–condensing.
- Power Requirements — does not include modules
  4 Amperes at +5 Volts (typical)

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CHAPTER 2
THEORY OF OPERATION

This chapter discusses the basic functional areas of the IMS. The information provided describes how the frame memory operates and interfaces to the video bus to provide image data to the other Series 150/40 modules. Figure 2–1 shows the functional blocks of the IMS:

- Frame Memory
- Host Interface
- Input Cross–Port Switch
- Output Cross–Port Switch
- System Timing
- Video Bus Interface
- Analog Module Interface
- Computation Module Interface
- Display Module Interface

2.1 FRAME MEMORY

The IMS contains image memory organized into three frame stores: A0, A1, and B1. All three frames are the same size: 1024 by 512 by 8–bits on the 1.5MB version IMS, and 1024 by 1024 by 8–bits on the 3MB version IMS. All three frame stores receive 8–bit video data from the input cross–port switch. All three frame stores supply data to the output cross–port switch and have a feedback to the input cross–port switch. Frame B1 can supply data to the display interface. The IMS frame memory allows simultaneous host and video (scan) access.

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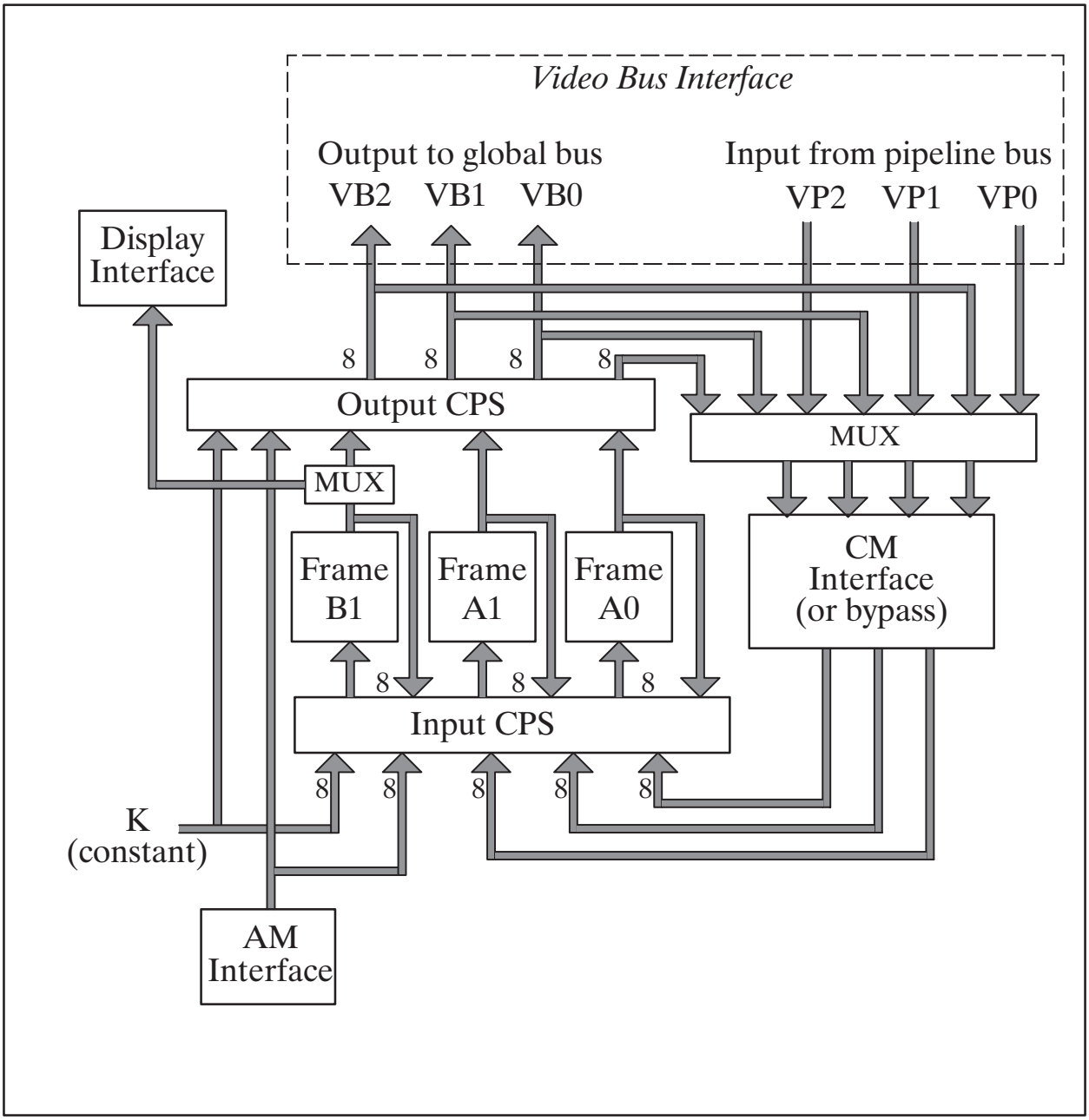


Figure 2–1. IMS Block Diagram

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2.1.1 Video Access

Each frame has two associated video address generators, separate for read and write access, as illustrated in Figure 2–2. The IMS supports pan and scroll on single pixel boundaries (except display pan: 2 pixel boundaries). Each 8–bit frame contains two 10–bit pan registers (read pan and write pan) and two 10–bit scroll registers (read scroll and write scroll).

As shown in Figure 2–2, three 8–bit images can be written simultaneously at independent addresses. Frame A0 may acquire an interlaced image from the camera, while frame A1 acquires the result from a non–interlaced AOI process and frame B1 acquires from the video bus. Each frame store has independent selection for write timing. The IMS can be storing three asynchronous images in the three frames at three different pan and scroll values. Video input can occur at pixel rates up to 40 MHz. The video input can be driven by camera (AM timing), CM timing, or 150/40 video bus timing, based on video input source selection. Individual bit–planes can be write–protected from both video and host write access by the Mask A and Mask B registers.

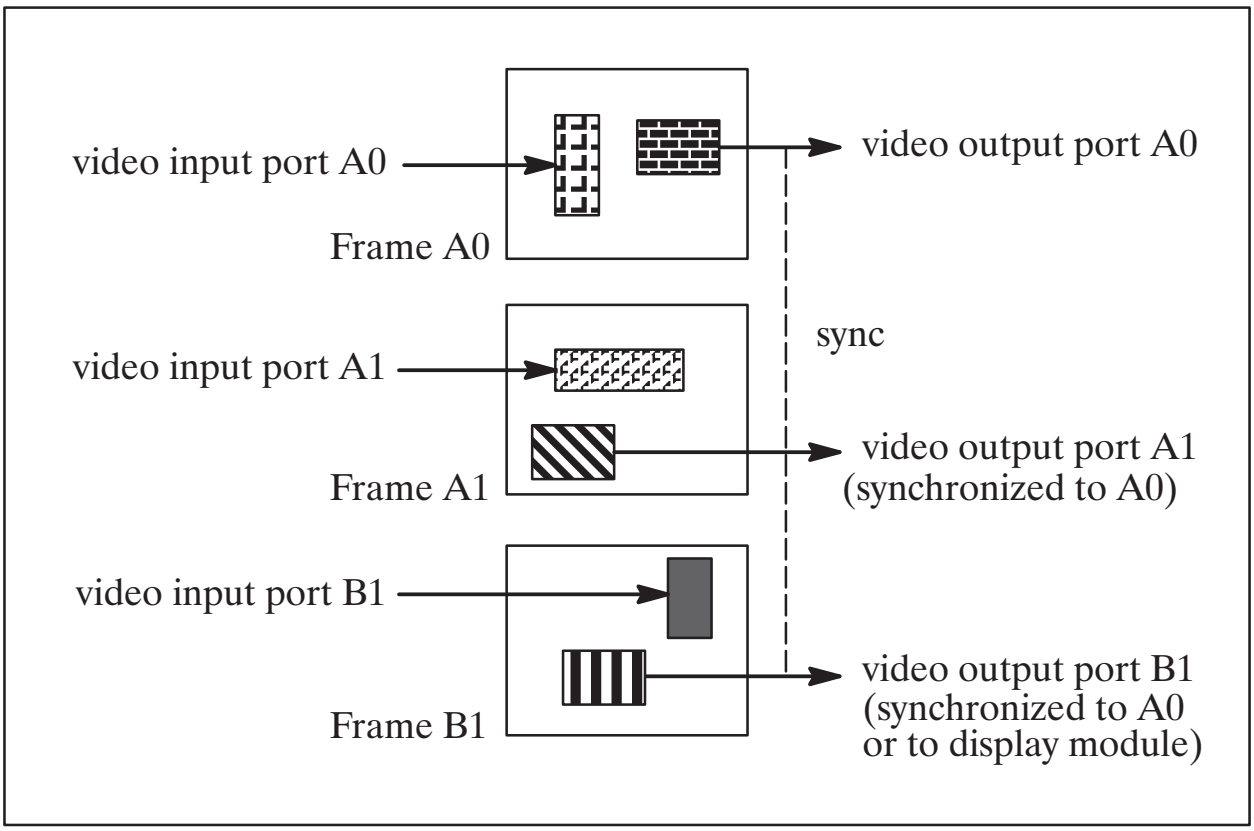


Figure 2–2. Scan Access Ports

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Figure 2–2 also shows that images can be read from unrelated addresses. One important restriction applies. The three frame stores do not have independent selection for read timing. The outputs of A0 and A1 are synchronized and have the same timing. The pan and scroll may be different, but the frame sizes and formats are the same. If the display interface is not active, frame B1 output is also synchronized to frame A0 and A1 output, and has the same size and format. If the display interface is active, frame B1 output is synchronized to the display module.

Frame B1 is the display frame buffer. The output of frame B1 can be software switched to output according to the display interface timing. The 8–bit video output can occur at rates up to 65 MHz or 65MB/second. This speed can support display resolutions to 1024 by 768 non–interlaced. All video data displayed by the DM–PC plug–in display module must must be stored in frame B1.

2.1.2 Zoom Display

Frame B1 supports zoom factors of 2x and 4x for display. If the display is disabled, zoom is no longer available. Figure 2–3 illustrates display zoom by 2. A 256 by 256 area in frame B1 is expanded to fill a 512 by 512 display area in zoom by 2. Display zoom is controlled independently in the horizontal and vertical directions, by the DISPXZ and DISPYZ bits in the Frame B Control register (CTLB).

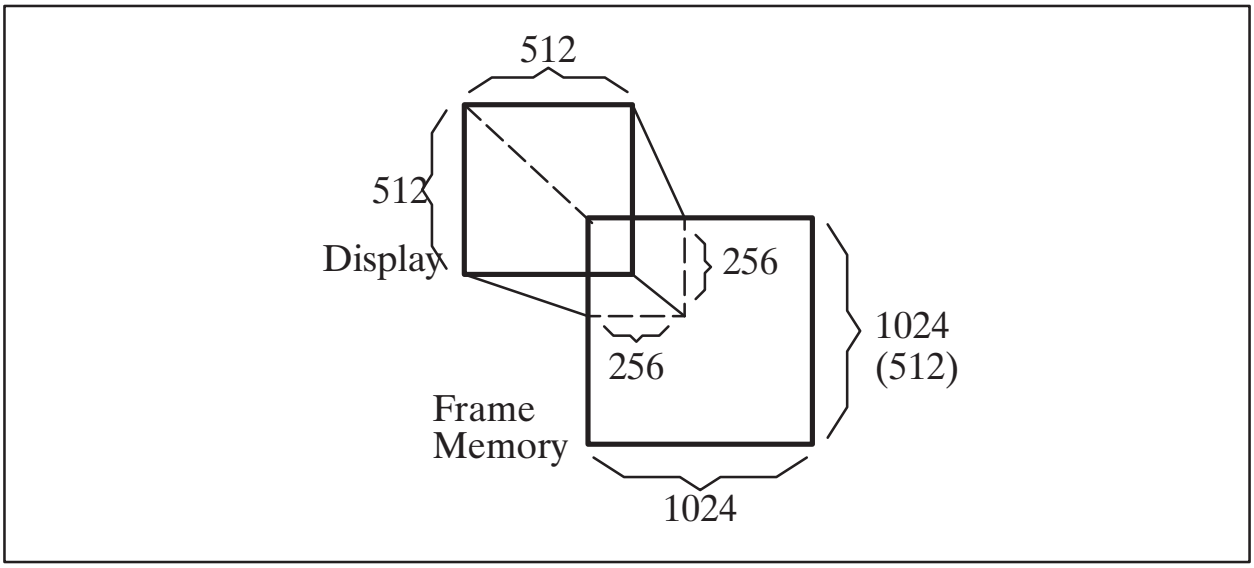


Figure 2–3. Display Zoom by 2

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2.1.3 Zoom Acquire

The IMS supports pixel decimation (sub–sampling) by 2 on each frame input. The IMS has independent zoom controls for X and Y direction (horizontal and vertical). Figure 2–4 illustrates decimation or sub–sampling. Acquire zoom is controlled by the WYZ***F*** and WXZ***F*** bits, where ***F*** is the frame.

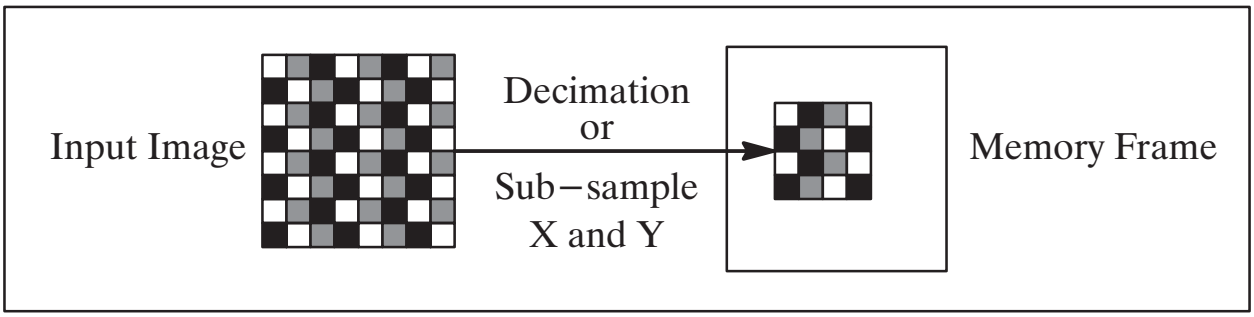


Figure 2−4. Sub−Sample and Zoom

2.1.4 Acquisition Control

Each 8–bit frame has an associated acquisition register. An image is acquired relative to the frame timing selected. The acquire operation begins at the trailing edge of vertical blank and ends at the leading edge, as illustrated in Figure 2–5. Alternatively, the operation will begin and end upon receiving a trigger pulse from the analog module. Any frame can generate an interrupt at the end of the acquisition period, if so programmed.

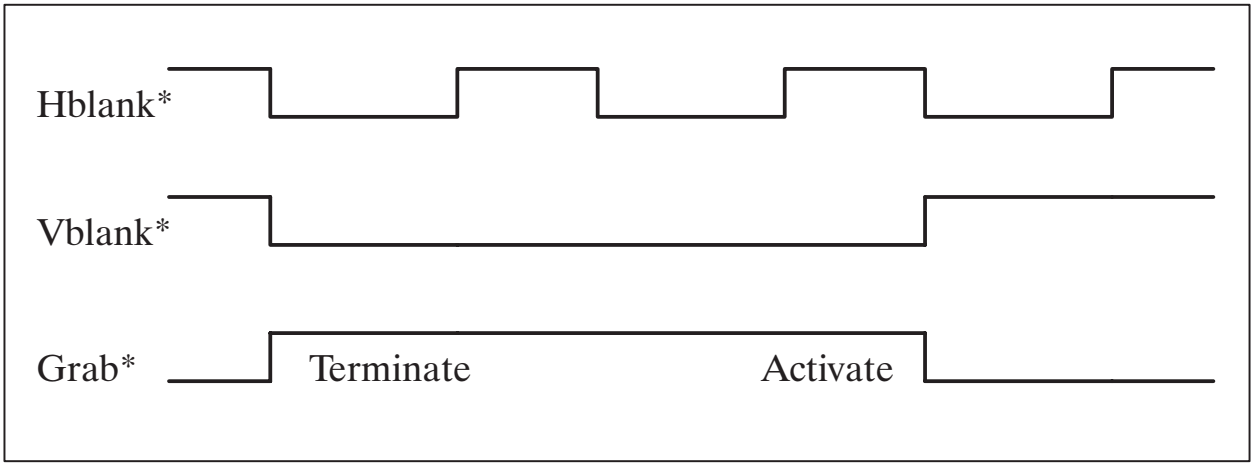


Figure 2−5. Acquisition Control

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2.2 HOST INTERFACE

The IMS responds to both supervisory and non–privileged data access. The IMS supports both standard (A24) and extended (A32) VME memory access. The IMS supports short (A16) access for local registers.

2.2.1 Registers

The IMS registers are mapped into VME short word (A16) address space occupying 64 words. An 8–pin switch configures the register base address, as described in Chapter 4. Chapter 3 describes all registers and bits in detail. Registers support address modifiers 0x29 and 0x2D. Figure 2–6 illustrates register access as supported on the VME bus.

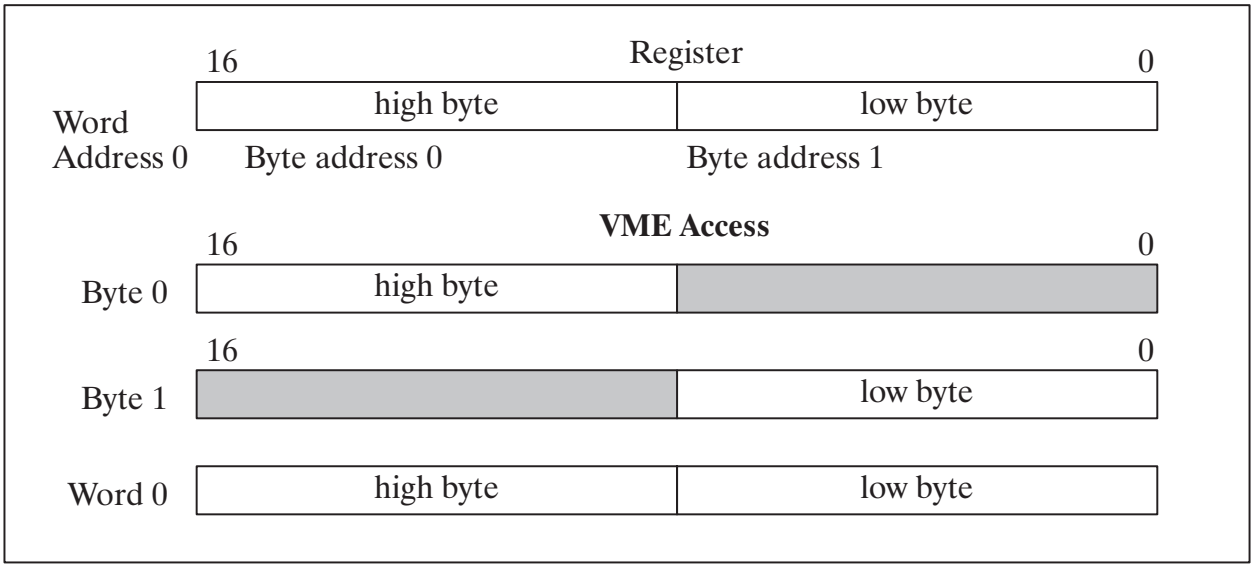


Figure 2–6. Register Access

2.2.2 Memory

The IMS image memory is directly mapped into VME address space. The IMS memory responds to standard (A24) and extended (A32) addressing, as selected by software. Image memory supports address modifiers 0x39, 0x3D, 0x09, and 0x0D. Access is through user–defined pages ranging from 1MB to 4MB. The page size and base address are software programmable. The Configuration register selects the memory addressing mode (standard or extended), map size, and memory base address.

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The Page register enables memory access. The IMS memory supports byte, word, and long–word access.

Each 8–bit frame has an associated write mask for bit–plane protection from host access or video scan access. The mask is always enabled. A logic 1 enables writing the bit–plane and a 0 masks it. Each byte masks an 8–bit segment of the corresponding 16–bit frame. The mask registers are undefined at power–up. Figure 2–7 illustrates VME memory access modes.

The host has byte,word and long word access to the 8–bit B1 frame. Byte access will access one pixel. Word access will access two adjacent pixels. Long word access will access four adjacent pixels. On a host write, individual bit–planes can be write–protected using the Mask B register. This register applies to both host and video write cycles.

The host has byte, word and long word access to frame A0 and frame A1. When each frame is configured as separate 8–bit frames, byte access will access one pixel, word access will access two adjacent pixels, and long word access will access four adjacent pixels.

Frame A can be read as a 16–bit frame (programmed in the Page register). In this mode, the high byte of a 16–bit word accesses frame A1 and the low byte accesses frame A0. Two 16–bit pixels are accessed in a single 32–bit cycle.

When frames A0 and A1 are configured as one 16–bit frame (Frame A), word access will access one 16–bit pixel. Long word access will access two adjacent 16–bit pixels. On a host write, individual bit–planes can be write–protected using the Mask A register. This register also applies to both host and video write cycles.

The IMS Frame Memory consists of three 1024 by 1024 by 8–bit frames mapped into host address space at the following addresses:

Frame A0	Memory offset 0
Frame A1	Memory offset 100000H
Reserved	Memory offset 200000H
Frame B1	Memory offset 300000H

When less than 4MB of memory are mapped into host address space access to this memory is done using the IMS Page register.

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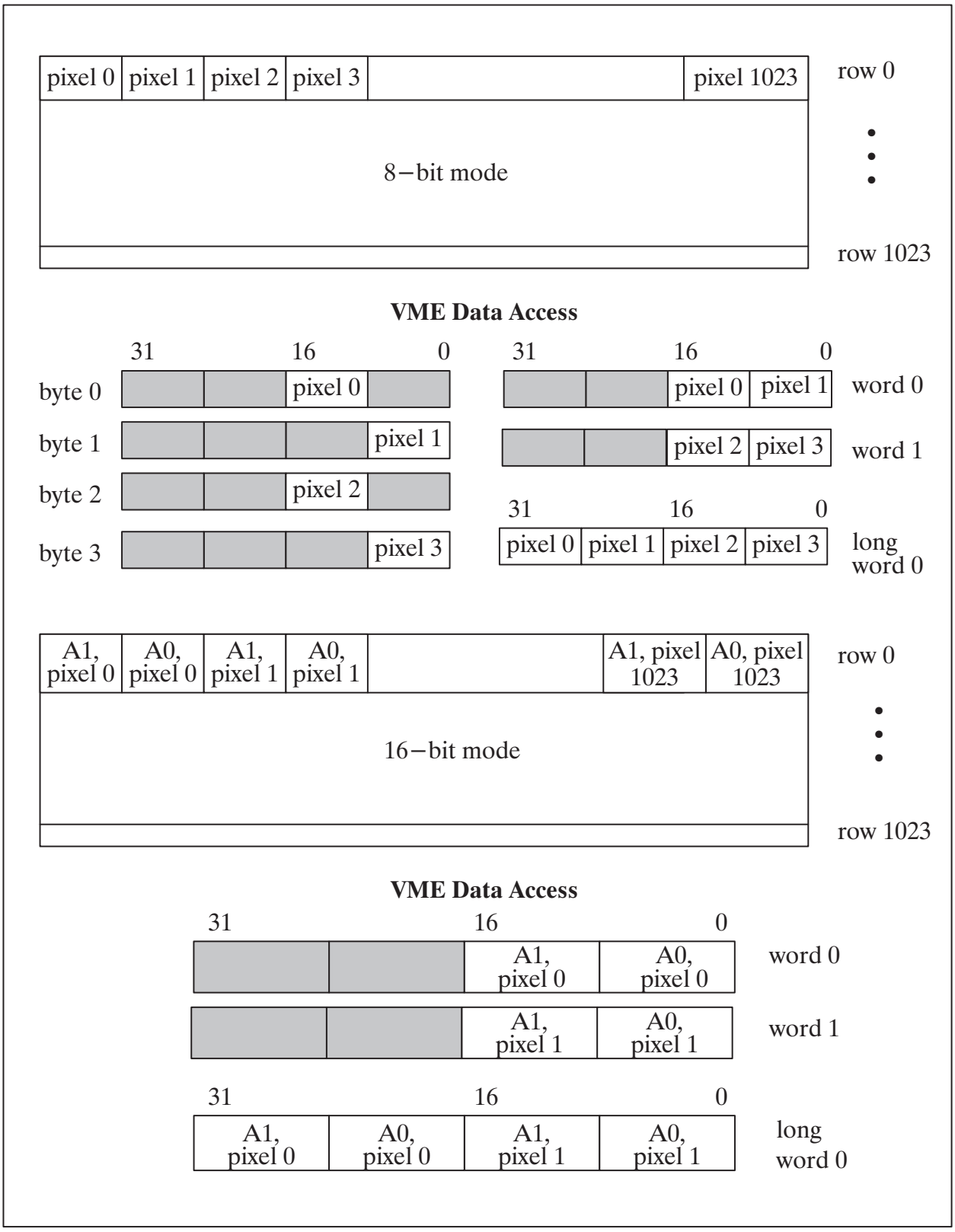


Figure 2−7. Memory Access

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2.2.3 Modules

All modules are directly mapped into VME memory address space at the same software selected address as the image memory. Modules support byte and word accesses only. The Page register selects between modules and memory for access. The IMS allocates 256K for the CM, 4K for the AM, and 8 words for the DM. The IMS supports the CM master mode. The IMS also supports CMs operating slower than the IMS clock speed.

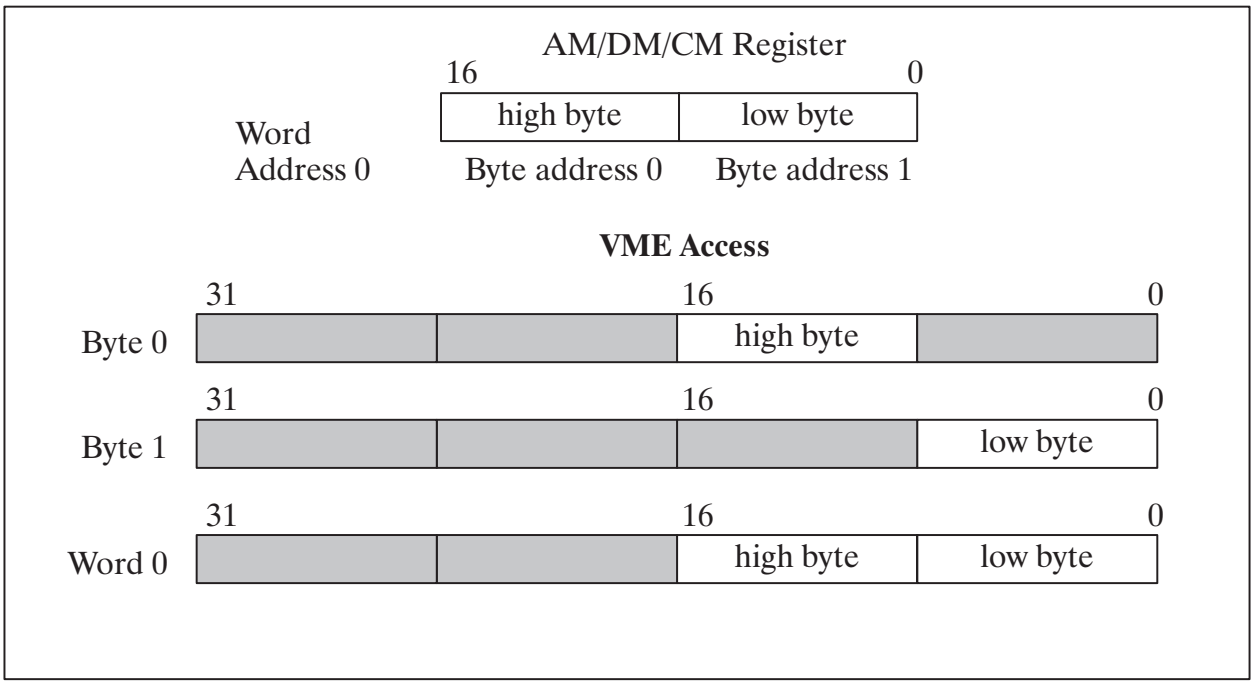


Figure 2–8. Module Access

2.2.4 Interrupts

The IMS interrupts the host on one of seven request lines, as selected by hardware switch SW2. The IMS supports vectored interrupts. The Reset On Register Access (RORA) protocol is supported. An interrupt can occur upon detection of one of the following events:

a. Start of vertical blank (frame programmable)

b. End of acquisition (frame programmable)

c. External trigger

d. Module interrupts

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2.3 INPUT CROSS–PORT SWITCH

The IMS contains an input cross–port switch for video data input path control. The input cross–port switch has eight 8–bit data inputs and three 8–bit data outputs which allow data to be routed in a variety of ways to any of the IMS frames. The cross–port switch has three timing inputs and three timing outputs.

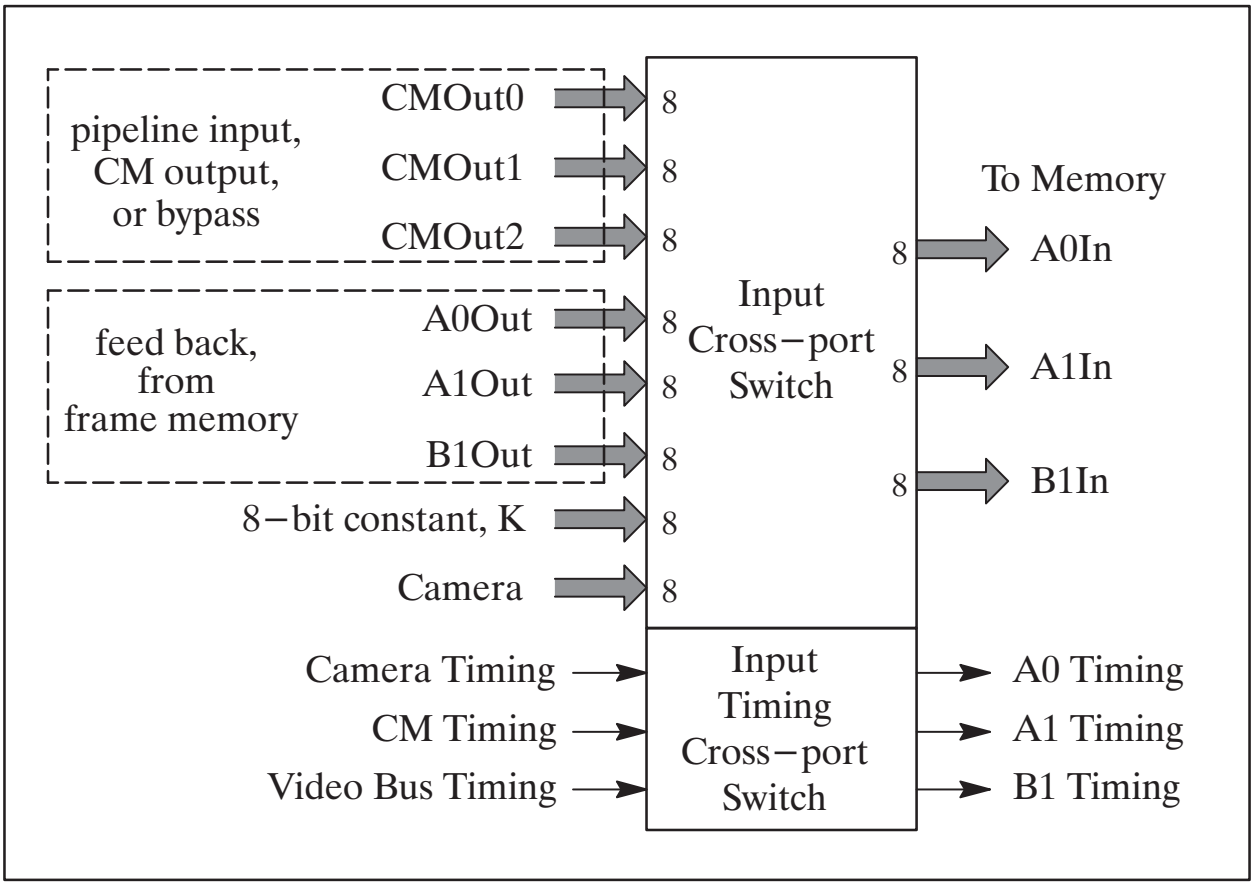


Figure 2–9. Input Cross Port Switch

The path control registers (FA0SEL, FA1SEL, FB1SEL) define which input drives a particular frame input. The format of each of these registers is described in Chapter 3. When acquiring into a frame from a computation module (CMOut0, CMOut1, CMOut2 in Figure 2–9) the input timing cross–port switch should be programmed to pass the CM frame timing to that frame. When acquiring into a frame from any of the memory feedback busses (A0Out, A1Out or B1Out) the input timing cross–port switch should be programmed to pass the 150/40 video bus timing to that frame. When acquiring into a frame directly from a camera the input timing cross–port switch should be programmed to pass the Camera timing to that frame.

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2.4 OUTPUT CROSS–PORT SWITCH

The IMS contains an output cross–port switch for data path control. The output cross–port switch has five 8–bit inputs and four 8–bit outputs which allow data to be routed from the IMS frame stores, the CM, or the output to the video bus.

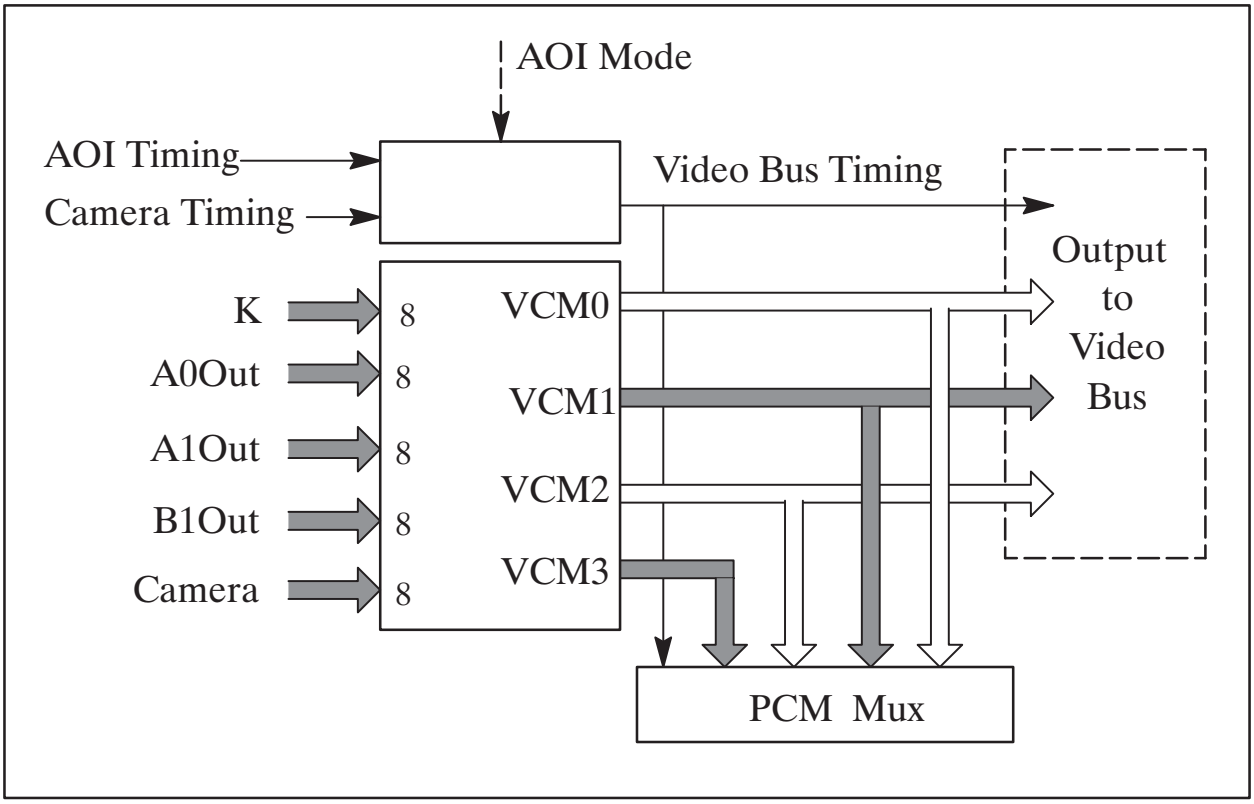


Figure 2–10. Output Cross–Port Switch

The output cross–port switch Control registers define which input drives a particular output. The format of each of these registers is described in the Chapter 3. The AOI Mode bit in the AOI Control register determines the time base for the 150/40 video bus. All frames are unloaded to the output cross–port switch according to this time base selection. When passing camera data directly to the 150/40 bus or to the CM MUX, the AOI Mode should disabled.

2.5 PCM MUX

The PCM MUX will pass either the pipeline input (PI0, PI1 or PI2) or the output of the output cross–port switch to the PCM buses (PCM0, PCM1, or PCM2). The VCM3 bus from the output cross–port switch goes directly to the PCM3 bus. Enabling the VCM

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or PI busses onto the PCM busses is done on a bus by bus basis. Whenever at least one of the 150/40 pipeline busses is enabled onto a PCM bus, the 150/40 pipeline timing is also enabled onto the PCM bus timing. Multiplexing onto the VCM bus is controlled by the output cross–port switch control registers. The format of these registers is described in the software interface. **Notice that VCM3/PCM3 connect to CMIn1, and PI1/VCM1/PCM1 connect to CMIn3.**

The CM Bypass allows PCM bus data to bypass the CM module and go directly to the CM output buses and input cross–port switch. Enabling the CM Bypass will disable all three CM module outputs and enable all three CM Bypass outputs. Disabling the CM Bypass will enable all three CM Module outputs and disable all three CM Bypass outputs.

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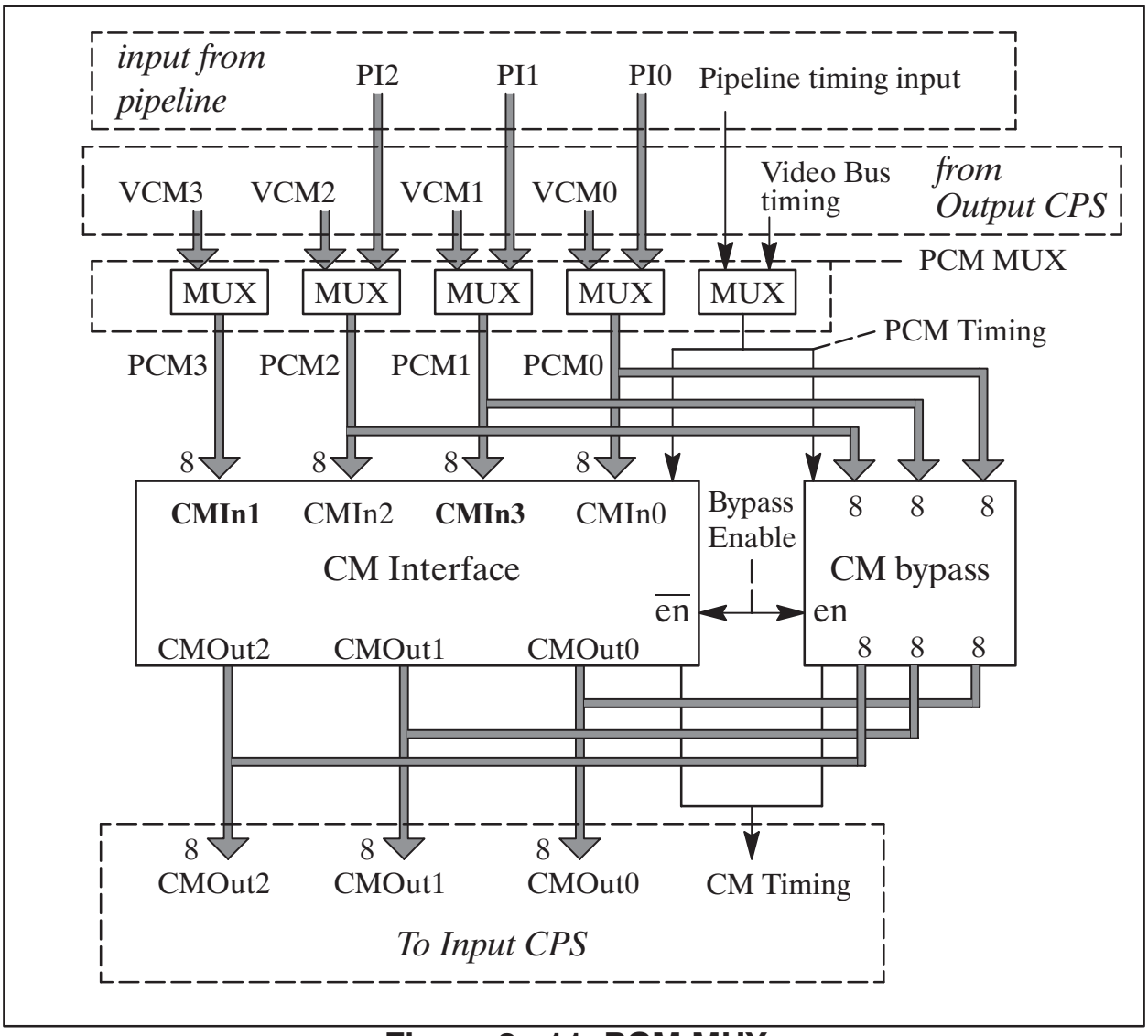


Figure 2–11. PCM MUX

2.6 SYSTEM TIMING

The IMS operates only as a video bus master. Timing is derived from an on–board oscillator. As a master, the IMS drives the video bus. The video bus pixel clock speed may be changed under software control, to maintain compatibility with the slowest processing device in the system. Options for 40 MHz, 20 MHz, and 10 MHz are provided.

The IMS must internally set up the frame memories to receive and transmit data during each horizontal blanking period. This “set–up time” dictates the minimum horizontal blank time of 40 us (40 microseconds) during an AOI transfer.

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2.7 VIDEO BUS INTERFACE

The video bus has a 24–bit “global bus” driven by the IMS, and a 24–bit “pipeline bus” illustrated in Figure 2–12. The global bus connects to all Series 150/40 boards on the video bus front–plane. The pipeline bus connects the input of one board to the output of an adjacent board.

The Global bus is driven with camera or AOI timing. The IMS can drive data from any frame onto any byte of this bus. The IMS can select a slave to drive data on the Global bus at any one time. Only one IMS is allowed in a Series 150/40 subsystem. The IMS can only output data onto the global bus. The IMS cannot receive data from the global bus. The IMS can only receive data from the pipeline bus.

The pipeline typically transmits resultant images back to the IMS in a multiple board system. The IMS receives pipeline data and stores it according to the pipeline timing. The pipeline timing can be a delayed version of the global bus timing or a different time base that adheres to the 150/40 bus timing.

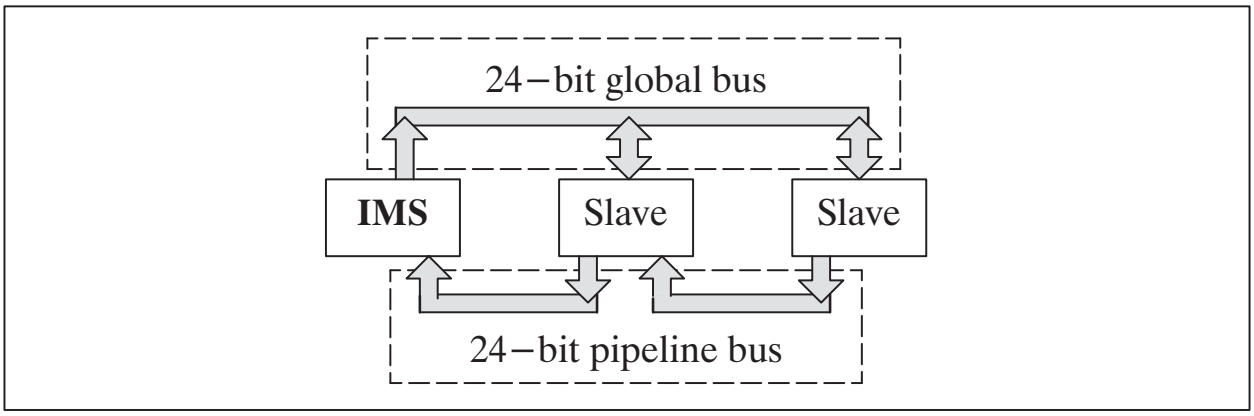


Figure 2−12. 150/40 Video Bus

2.8 MODULE INTERFACES

The IMS provides an interface to each of the Series 150/40 modular board types. The modules are the same physical size; but the connectors for each are of different sizes and locations to prevent incorrect installation. The modules are directly mapped into the host VME memory address space, at the same base address as the image memory. The Page register selects between memory and modules for access. For example, with the PAGE register programmed to 0x15, memory word location 0 points to register 0 on the DM.

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PGSEL	PGADR1	PGADR0	Operation
0	0	0	Access memory page 0
0	0	1	Access memory page 1
0	1	0	Access memory page 2
0	1	1	Access memory page 3
1	0	0	Access AM, 4K
1	0	1	Access DM, 8 words
1	1	0	Access CM, 256K
1	1	1	*Undefined*

2.8.1 Analog Module Interface

The IMS provides a Camera interface compatible with the AM family. The AM contains line FIFOs which are loaded at the camera rate and unloaded at the operating rate of the IMS (40 MHz, 20 MHz, or 10 MHz). The interface supports 8 bits of data, external triggering and interrupts. The IMS and AM interface uses an asynchronous request/acknowledge handshake. Each time the AM finishes loading a line in the FIFO, the AM requests the mother board to unload the buffer (FIFO). The mother board can sample this request as true, perform any necessary setup, and start reading data. The mother board unloads the buffer, and enters horizontal blank at the end–of–line. The mother board waits in horizontal blank until the AM makes a new unload request, at the end of loading a line. A new request can occur before the mother board enters horizontal blank (at the end of the current line unload) but the request is only sampled during the horizontal blank.

The capabilities of each AM are different. The IMS provides a 44–pin, High–Density connector for camera interfacing. The AM in use defines the pin–out of this connector. Appendix A shows the standard pin–out. Refer to the AM Hardware Reference Manual for specific signal functions.

The AM supplies scanning information to the IMS (interlaced/non–interlaced and field) together with blanking status and valid data status. The IMS only has to know when a frame or field begins and when a valid line has been captured. For external triggering, the AM supplies a trigger pulse which activates the SNAP. If trigger on line is supported, the AM has to track the line address at which the trigger occurred, so that the frame may be terminated correctly.

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2.8.2 Computation Module Interface

The IMS supports one computational module. The IMS provides the CM with 32–bits of video input and receives 24–bits of video output from the CM. The interface supports all of the Series 150/40 CM modules, and supports CM master mode. Registers and memory on the CM are directly mapped in host address space. The addressability of each CM module is 256K words, four 64K pages.

2.8.3 Display Module Interface

The IMS display interface allows for one Display Module to be installed on the IMS. The Display Module will provide the IMS with a divide by two Pixel Clock & frame timing signals. The IMS can unload 16–bit serial data (two 8–bit pixels in parallel) to the display module at clock rates up to 33 MHz. This allows the IMS to support display rates up to 1024 by 768 non–interlaced (65M pixels/second).

All data for the Display Module comes from B1 memory. The resolution of frame B1 read pan is two pixels when displaying and one pixel when not displaying. Frame B1 read scroll resolution is one line. Zoom of B1 for display is accomplished by pixel and line replication. No zoom is allowed on the B1 read port when not displaying.

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CHAPTER 3
REGISTERS

This chapter provides a detailed description of all IMS registers and bits. The IMS occupies 64 words in the VME short word (A16) address space. Figure 3–1 shows the mapping of the IMS registers and their offsets relative to the register base address. The figure also gives page number references for the register definitions.

The IMS responds to VMEbus short word supervisory and non–supervisory access. IMS registers support byte and word access. The R/W notation following a register or bit name indicates the register or bit supports both read and write access. The R–O notation following a register or bit name indicates the register or bit supports read access only. The W–O notation following a register or bit name indicates the register or bit supports write access only.

This manual documents registers using the same convention as the Motorola 68000. Motorola reads the odd byte (address 3H) called the low byte first, and reads the even byte (address 2H), called the high byte, second. Word access is defined to be a VMEbus I/O cycle during which both DS0 (Data Strobe 0) and DS1 (Data Strobe 1) are asserted.

NOTE *Upon power–up most of the IMS registers are in an unknown state. The host CPU must initialize these registers for proper operation. A system reset does not affect the contents of these registers.*

NOTE ***Program all reserved bits and registers to zero unless otherwise indicated.***

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I/O Base Address +	*address n*	*address n+1*	*Refer to Page #*
0H	**Configuration (CONF)**		3–4
2H	*Reserved*		—
4H	**STATUS**		3–6
6H	*Reserved*		—
8H	**MASK A**		3–8
AH	*Reserved*		—
CH	**MASK B**	**Constant (CONST)**	3–9
EH	*Reserved*		—
10H	**AOI0 Horizontal Size (AOIXS0)**		3–9
12H	**AOI0 Horizontal Blank (AOIXB0)**		3–10
14H	**AOI0 Vertical Size (AOIYS0)**		3–10
16H	**AOIYB0**	**AOICTL**	3–10, 3–11
18H–1FH	*Reserved*		—
20H	**PAGE**		3–13
22H	*Reserved*		—
24H	**Control (CTL)**		3–14
26H	*Reserved*		—
28H	**Interrupt Vector (IVEC)**		3–16
2AH	**Interrupts Enable (IEN)**		3–16
2CH	**INTACK/ISTAT**		3–18, 3–20
2EH	**Interrupt Priority (IPRI)**		3–21
30H	**A0 Acquisition Control (ACQA0)**		3–21
32H	**A1 Acquisition Control (ACQA1)**		3–25
34H	**Acquisition Enable (ACQEN)**		3–28
36H	**B1 Acquisition Control (ACQB1)**		3–28

(continued)

Figure 3–1. IMS Register Map

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I/O Base Address +	*address n* / *address n+1*	*Refer to Page #*
38H–3FH	*Reserved*	—
40H	**A0 Read Pan (RPANA0)**	3–31
42H	**A0 Read Scroll (RSCRA0)**	3–32
44H	**A0 Write Pan (WPANA0)**	3–32
46H	**A0 Write Scroll (WSCRA0)**	3–32
48H	**A1 Read Pan (RPANA1)**	3–33
4AH	**A1 Read Scroll (RSCRA1)**	3–33
4CH	**A1 Write Pan (WPANA1)**	3–33
4EH	**A1 Write Scroll (WSCRA1)**	3–34
50H	**Frame A Control (CTLA)**	3–34
52H	**B1 Read Pan (RPANB1)**	3–36
54H	**B1 Read Scroll (RSCRB1)**	3–36
56H	**B1 Write Pan (WPANB1)**	3–37
58H	**B1 Write Scroll (WSCRB1)**	3–37
5AH	**Frame B Control (CTLB)**	3–38
5CH–5FH	*Reserved*	—
60H	**CM2In Select (PVB2)**	3–40
62H	**CMIn1 Select (PVB1)**	3–41
64H	**CMIn0 Select (PVB0)**	3–42
66H	**Pipeline Inputs Select (PIPECON)**	3–43
68H	**CMIn3 Select (PVB3)**	3–45
6AH	**Frame A0 Input Select (FA0SEL)**	3–46
6CH	**Frame A1 Input Select (FA1SEL)**	3–48
6EH	**Frame B1 Input Select (FB1SEL)**	3–50
70H–7FH	**CPS Format Control (CPSCTL)**	3–51

Figure 3–1. (continued) IMS Register Map

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3.1 CONFIGURATION (CONF) [R/W]

I/O Base Address + 0H *word only*

CONF

7							0
STDADR3	STDADR2	STDADR1	STDADR0	EXTSEL	STDSEL	MAPSEL1	MAPSEL0

Extended addressing only

15							8
EXTADR7	EXTADR6	EXTADR5	EXTADR4	EXTADR3	EXTADR2	EXTADR1	EXTADR0

This register configures the memory base address, addressing mode, and the amount of image memory mapped into the VME memory address space.

BIT	MNEMONIC	FUNCTION
0	MAPSEL0	Map Size Select Bit 0
1	MAPSEL1	Map Size Select Bit 1
2	STDSEL	Standard Addressing Mode Select
3	EXTSEL	Extended Addressing Mode Select
4	STDADR0	Standard Address Bit 0 (A20)
5	STDADR1	Standard Address Bit 1 (A21)
6	STDADR2	Standard Address Bit 2 (A22)
7	STDADR3	Standard Address Bit 3 (A23)
8	EXTADR0	Extended Address Bit 0 (A24)
9	EXTADR1	Extended Address Bit 1 (A25)
10	EXTADR2	Extended Address Bit 2 (A26)
11	EXTADR3	Extended Address Bit 3 (A27)
12	EXTADR4	Extended Address Bit 4 (A28)
13	EXTADR5	Extended Address Bit 5 (A29)
14	EXTADR6	Extended Address Bit 6 (A30)
15	EXTADR7	Extended Address Bit 7 (A31)

This register is undefined at power–up. This register must be properly initialized before setting the MEMEN bit in the Page register.

3.1.1 Map Size Select (MAPSEL) [R/W]

These two bits define the size of the block mapped into VME memory address space. The minimum map size supported is 1MB. If a page size less than 4MB is selected, memory can be accessed by using the Page register. This mechanism moves the

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memory–mapped window through the IMS address space. The Page register PGADR1–0 bits substitute for upper memory addresses when the map size is less than 4MB. The appropriate translator (AT to VME) provides additional mapping control down to 64K segments.

MAPSEL1	MAPSEL0	Function
0	0	1MB mapped into VME memory space
0	1	2MB mapped into VME memory space
1	0	3MB mapped into VME memory space
1	1	4MB mapped into VME memory space

The IMS contains 3MB of image memory and 3 memory–mapped modules. A page select bit PGSEL selects between memory and modules for access.

NOTE *Module access is not affected by map size. Modules are accessed via the Page register.*

3.1.2 VME Addressing Format (STDSEL, EXTSEL) [R/W]

These two bits select either standard (A24) or extended (A32) addressing for the IMS. In standard A24 addressing mode, the board responds to address modifiers 3DH and 39H. In extended A32 addressing mode, the board responds to address modifiers 0DH and 09H. These bits are qualified with the MEMEN bit in the Page register.

EXTSEL	STDSEL	Function
0	0	*Undefined*
0	1	Standard A24 addressing mode
1	0	Extended A32 addressing mode
1	1	*Undefined*

Bits STDADR(3–0), in conjunction with the programmed map size, are compared with address bits A23–20 at the start of each host access.

In extended (A32) VME addressing mode, the high byte of the Configuration register configures the upper 8–bits of the memory base address. Bits EXTADR(7–0) are compared with address bits A31–24 at the start of each host access.

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3.2 STATUS (STATUS) [R–O]

I/O Base Address + 4H *word only*

STATUS

7							0
Reserved	AOIVB1	Reserved	EN1SH0	VBUSFLD	VBUSVB	CAMFLD	CAMVB

15							8
Reserved	Reserved	Reserved	Reserved	CMMOD	DMMOD	AMMOD	Reserved

This register provides general status regarding the current state of the camera and video bus, module configuration, and IMS revision. Additional frame timing status is provided in the appropriate acquisition registers.

BIT	MNEMONIC	FUNCTION
0	CAMVB	Camera Vertical Blank Status
1	CAMFLD	Camera Field Status
2	VBUSVB	Video Bus Vertical Blank Status
3	VBUSFLD	Video Bus Field Status
4	EN1SH0	AOI One–Shot Ready
5	*Reserved*	*Read as zero*
6	AOIVB1	AOI Vertical Blank
7	*Reserved*	*Read as zero*
8	*Reserved*	*Read as zero*
9	AMMOD	Acquisition Module Present
10	DMMOD	Display Module Present
11	CMMOD	Computation Module Present
12	*Reserved*	*Read as zero*
13	*Reserved*	*Read as zero*
14	*Reserved*	*Read as zero*
15	*Reserved*	*Read as zero*

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3.2.1 Camera Vertical Blank Status (CAMVB) [R−O]

This signal low indicates that the sensor is in vertical blank. The acquisition (snap, grab, freeze) bits, and the pan and scroll registers are reprogrammed during vertical blank.

SCAMVB	Function
0	Camera/sensor in vertical blank
1	Not in vertical blank (active video or horizontal blank)

3.2.2 Camera Field Status (CAMFLD) [R−O]

This signal indicates which field is currently being unloaded from the acquisition module (AM).

CAMFLD	Function
0	Even field
1	Odd field

3.2.3 Video Bus Vertical Blank Status (VBUSVB) [R−O]

This signal low indicates that the 150/40 video bus is in vertical blank. The acquisition (snap, grab, freeze) bits, and the pan and scroll registers are reprogrammed during vertical blank.

VBUSVB	Function
0	Vertical blank on 150/40 video bus
1	Not in vertical blank (active video or horizontal blank)

3.2.4 Video Bus Field Status (VBUSFLD) [R−O]

This signal indicates which field is currently being unloaded to the 150/40 video bus.

VBUSFLD	Function
0	Even field
1	Odd field

3.2.5 AOI One−Shot Ready (EN1SH0) [R−O]

This signal shows the status of the AOI one shot–circuit.

EN1OS0	Function
0	AOI one–shot ready
1	Not ready

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3.2.6 AOI Vertical Blank Status (AOIVB1) [R−O]

This signal low indicates that AOI generator is in vertical blank.

AOIVB1	Function
0	AOI vertical blank
1	Active video or horizontal blank

3.2.7 Acquisition Module Present (AMMOD) [R−O]

This signal indicates that an acquisition module (AM) is present (installed).

AMMOD	Function
0	AM installed
1	No AM installed

3.2.8 Display Module Present (DMMOD) [R−O]

This signal indicates that a display module (DM) is present (installed).

DMMOD	Function
0	DM installed
1	No DM installed

3.2.9 Computational Module Present (CMMOD) [R−O]

This signal indicates that a computation module (CM) is present (installed).

CMMOD	Function
0	CM installed
1	No CM installed

3.3 FRAME A MASK (MASKA) [R/W]

Base Address + 8H *word only*

MASKA0

7							0
MA07	MA06	MA05	MA04	MA03	MA02	MA01	MA00

MASKA1

15							8
MA17	MA16	MA15	MA14	MA13	MA12	MA11	MA10

Each frame has an associated write mask for bit–plane protection. The write masks are used for both scan (video) and host access (see note). The mask is always enabled. A

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logic 1 enables writing the bit plane and a 0 masks it. The low byte protects Frame A0 bit–planes 7–0. The high byte protects Frame A1 bit–planes 7–0. If the host is accessing in 16 bit/pixel mode, the entire mask is used. **Mask registers are undefined at power–up.**

3.4 CONSTANT/FRAME B MASK (MASKB) [R/W]

Base Address + CH *word only*

MASKB1

7							0
MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0

CONSTANT

15							8
K7	K6	K5	K4	K3	K2	K1	K0

Each frame has an associated write mask for bit–plane protection. The write masks are used for both scan (video) and host access (see previous note). The mask is always enabled. A logic 1 enables writing the bit plane and a 0 masks it. The low byte protects Frame B1 bit–planes 7–0. **Mask registers are undefined at power–up.**

The constant register is input to the IMS input cross–port switch, providing a constant value on any of the IMS video buses.

3.5 AOI HORIZONTAL SIZE (AOIXS0) [R/W]

Base Address + 10H *word only*

AOIXS0

7							0
XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	XA9	XA8

The AOI timing generator provides AOI timing for the 150/40 video bus. The video bus timing switches from camera timing to AOI timing when the MODE bit in the AOICON register is 1.

The horizontal active size is programmable on 4–pixel boundaries. The actual size is XSIZE=((AOIXS0 + 1) x 4). This 10–bit register supports a horizontal size up to and including 4K.

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3.6 AOI HORIZONTAL BLANK (AOIXB0) [R/W]

I/O Base Address + 12H *word only*

AOIXB0

7							0
Reserved	Reserved	Reserved	XB4	XB3	XB2	XB1	XB0

The horizontal blank size is programmable on 8–pixel boundaries. This 5–bit register supports blank sizes up to and including 256 pixels. The actual size is XBLANK=((AOIXB+ 1) x 8). **The Series IMS requires a minimum blank size of 64 pixels at 40 MHz, 32 pixels at 20 MHz and 10 MHz.**

The blank size register allows software to adjust the blanking interval according to the way the IMS memory is utilized.

3.7 AOI VERTICAL SIZE (AOIYS0) [R/W]

Base Address + 14H *word only*

AOIYS0

7							0
YA7	YA6	YA5	YA4	YA3	YA2	YA1	YA0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	YA9	YA8

The AOI vertical size is programmable on boundaries of 1 line. This 10–bit register provides an AOI frame to 1024 lines. The actual size is:

$$YSIZE = (AOIYS0 + 1)$$

3.8 AOI VERTICAL BLANK (AOIYB0) [R/W]

I/O Base Address + 16H *word or byte*

AOIYB0

7							0
Reserved	Reserved	Reserved	YB4	YB3	YB2	YB1	YB0

The AOI vertical blank register is programmable on boundaries of 2. This 5–bit register provides 64 lines of blank. The actual size is:

$$YBLANK = 2(AOIYB0 + 1)$$

resulting in a minimum blank period of two lines.

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3.9 AOI CONTROL (AOICTL0) [R/W]

I/O Base Address + 17H *word or byte*

AOICTL0

8							0
Reserved	Reserved	Reserved	Reserved	AOIMODE	OSHOT0	AOILK0	AOIHLT0

This register controls the operation of the AOI timing generator. This register is the upper byte of AOIYB. The AOI timing generator is continuously running according to the bits described below. Switching to AOI mode on the video bus is asynchronous, minimizing the dead–time between operations.

BIT	MNEMONIC	FUNCTION
0	AOIHLT0	AOI Halt
1	AOILK0	AOI Lock
2	OSHOT0	AOI One–Shot
3	AOIMODE	AOI Mode Enable
4–7	*Reserved*	“Don’t Care” or program to zero

3.9.1 AOI Halt (AOIHLT0) [R/W]

This bit, when programmed to 1, will stall the AOI generator in vertical blank. When AOIHLT0 is zero, the AOI generator is continuously running. The AOI generator samples this bit at the end of vertical blank. If AOIHLT0 is sampled true, the IMS reloads the AOIYB0 register and starts counting down again. This cycle continues until AOIHLT0 is sampled false. The latency between resetting this bit and starting an active frame is dependent on the value programmed in the AOIYB0 register. **This bit is ignored if AOI Lock mode is active.**

AOIHLT0	Function
0	AOI generator free running (continuous)
1	Halt AOI timing generator in vertical blank

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3.9.2 AOI Lock (AOILK0) [R/W]

This bit, when programmed to 1, will cause the AOI generator to stall at the end of the next vertical blank period. At this point, the camera vertical blank is sampled to determine if the next AOI frame can begin. If sampled false, the AOIYB0 register is reloaded and the vertical blank interval repeats. This mode is like a frame one shot which is triggered by the camera vertical blank.

AOILK0	Function
0	Normal AOI vertical blank
1	Lock AOI generator at end of vertical blank

NOTE *If the AOI size is greater than the camera size, the AOI generator will effectively sample every other frame. If the AOIYB0 register value is greater than the camera frame time, it is possible that the AOI generator could stall forever.*

3.9.3 AOI One−Shot (OSHOT0) [R/W]

This bit is used in conjunction with the AOIHLT0 bit. When AOIHLT0 is set to 1, the AOI generator is stalled and the status bit EN1SH0 is generated (Status register). If the status bit is true (logic 0), set OSHOT0 to 1 to generate a single AOI frame. Following this frame, the AOI generator will be stalled again in vertical blank.

OSHOT0	Function
0	Normal operation, or halted if HALT=1
1	Begin single AOI0 frame (one–shot AOI0)

3.9.4 AOI Mode Enable (AOIMODE) [R/W]

This bit switches the video bus into and out of AOI mode. This bit is sampled on 4–pixel boundaries. If sampled true, timing will immediately switch to AOI mode.

AOIMODE	Function
0	AOI mode disabled
1	AOI mode enabled

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3.10 PAGE [R/W]

I/O Base Address + 20H *word or byte*

PAGE

7							0
Reserved	Reserved	Reserved	MEMEN	PIXSZ	PGSEL	PGADR1	PGADR0

The Page register allows direct access to memory and modules. It also defines the pixel size of the frame being accessed. **This register is reset to zero at power–up**.

3.10.1 Page Select (PGSEL, PG) [R/W]

The PGSEL bit selects between memory and modules for access. The PG bits provide upper memory addresses when the page segment is less than 4MB. The page segment is defined by the map size bits in the configuration register.

PGSEL	PGADR1	PGADR0	Operation
0	0	0	Access memory page 0
0	0	1	Access memory page 1
0	1	0	Reserved
0	1	1	Access memory page 3
1	0	0	Access AM
1	0	1	Access DM
1	1	0	Access CM
1	1	1	Undefined

NOTE *If the map size is 1MB, page 0 is Frame A0, page 1 is Frame A1, and page 3 is Frame B1.*

3.10.2 Pixel Size (PIXSZ) [R/W]

This bit defines the size of pixel that the host expects to access. A long–word host cycle can access four 8–bit or two 16–bit pixels.

PIXSZ	Function
0	8 bits per pixel
1	16 bits per pixel

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3.10.3 Memory Enable (MEMEN) [R/W]

This bit enables VME access to the IMS image memory or modules. The Configuration register (CONFIG) must be initialized before memory access is enabled.

State	Function
0	VME memory access disabled
1	VME memory access enabled

3.11 CONTROL (CTL) [R/W]

I/O Base Address + 24H *word or byte*

CTL

7							0
DISPOE	EXTRIG	DMEN	CLRBM	CLKSPD1	CLKSPD0	SLAVSEL1	SLAVSEL0

BIT	MNEMONIC	FUNCTION
0	SLAVSEL0	Frame Processor Select Bit 0
1	SLAVSEL1	Frame Processor Select Bit 1
2	CLKSPD0	System Clock Speed Bit 0
3	CLKSPD1	System Clock Speed Bit 1
4	CLRBM	Clear Bit Mask Registers
5	DMEN	Display Module Enable
6	EXTRIG	AM Module External Trigger Mode
7	DISPOE	Digital Display Output Enable

3.11.1 Frame Processor Select (SLAVSEL) [R/W]

These bits are used by the IMS to select slave boards for supplying data onto the video bus. The IMS master always drives video bus timing.

SLAVSEL1	SLAVSEL0	Function
0	0	Master (IMS) drives video bus
0	1	Slave 0 (IMA) drives video bus
1	0	Slave 1(IMA) drives video bus
1	1	Slave 2 (IMA) drives video bus

CAUTION *Every IMA must have a different processor number! If two boards have the same number, damage can result when you select that number to drive the Global Video Bus. The processor number is defined by hardware switches on the IMA.*

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3.11.2 System Clock Speed (CLKSPD) [R/W]

This bits are used by the master to select the video rate within the system. Only the master can change the system clock speed. Slave boards can not affect the clock.

CLKSPD1	CLKSPD0	Function
0	0	40 MHz (normal oscillator frequency)
0	1	20 MHz
1	0	10 MHz
1	1	*Reserved*

3.11.3 Clear Bit Mask Registers (CLRBM) [R/W]

The serial write ports of each memory must be properly initialized to prevent unintentional overwriting during snap operations. This bit must be toggled during the initialization sequence. To clear the mask registers, first program CLRBM to one, then program CLRBM to zero. This clears all 16 bits in the Frame A Mask and Frame B Mask registers, protecting all bit–planes of all frames in memory. There is no timing requirement associated with this bit.

3.11.4 Display Module Enable (DMEN) [R/W]

This bit allows the display module, if present, to be disabled under software control. Resetting this bit prevents image data from being displayed, it has no affect on overlays. Disabling the display module allows frame B1 to be used for processing.

State	Function
0	Disable image display
1	Display image

3.11.5 External Trigger Mode (EXTRIG) [R/W]

This bit is used to put define the AM module external trigger mode. Refer to the AM module manual for details on Trigger Modes.

EXTRIG	Function
0	Trigger on frame mode
1	Trigger on line mode

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3.11.6 Digital Display Output Enable (DISPOE) [R/W]

This bit is used to enable the IMS digital display output. When there is no DM Module present this bit must be programmed to a one to output digital data on the 26 pin D–Sub display connector. When a DM module is present on the IMS this bit is ignored.

DISPOE	Function
0	Tri–state IMS digital display output.
1	Enable IMS digital display output.

3.12 INTERRUPT VECTOR (IVEC) [R/W]

I/O Base Address + 28H *word or byte*

IVEC

7							0
IVEC7	IVEC6	IVEC5	IVEC4	IVEC3	IVEC2	IVEC1	IVEC0

This register contains the vector that is read during a valid interrupt acknowledge cycle. The host must write the correct priority code on address lines A3–A0 to match the IPRI register to cause the contents of this register to appear on the data bus.

3.13 INTERRUPTS ENABLE (IEN) [R/W]

I/O Base Address + 2AH *word or byte*

IEN

7							0
CMIEN	DMIEN	AMIEN	ETIEN	FMIEN	FMIMOD	FMSEL1	FMSEL0

This register enables interrupt requesters. The IMS provides 6 sources of interrupt, defined as follows:

BIT	MNEMONIC	FUNCTION
0	FMSEL0	Frame Select Bit 0
1	FMSEL1	Frame Select Bit 1
2	FMIMOD	Frame Interrupt Mode
3	FMIEN	Frame Interrupt Enable
4	ETIEN	External Trigger Interrupt Enable
5	AMIEN	Analog Module Interrupt Enable
6	DMIEN	Display Module Interrupt Enable
7	CMIEN	Computation Module Interrupt Enable

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3.13.1 Frame Interrupts (FMIEN, FMIMOD, FMSEL) [R/W]

The two FMSEL bits select which write port is selected for interrupt generation. The FMIMOD bit determines which event associated with the selected write port generates an interrupt, end of acquisition or start of vertical blank. The FMIEN bit enables frame interrupts to occur.

FMIEN	FMIMOD	FMSEL1	FMSEL0	Operation
0	X	X	X	Frame interrupts disabled
1	0	0	0	Frame A0 interrupts at end of acquisiton
1	0	0	1	Frame A1 interrupts at end of acquisition
1	0	1	0	Undefined
1	0	1	1	Frame B1 interrupts at end of acquisition
1	1	0	0	Frame A0 interrupts at start of vertical blank
1	1	0	1	Frame A1 interrupts at start of vertical blank
1	1	1	0	Undefined
1	1	1	1	Frame B1 interrupts at start of vertical blank

3.13.2 External Trigger Interrupt Enable (ETIEN) [R/W]

If this bit is set, an interrupt will be generated upon the detection of an external trigger pulse from the analog module. If an acquisition command is pending and external trigger mode is selected, acquisition commences after a delay specified by Trigger Mode.

ETIEN	Function
0	Disable interrupt on trigger ETINT
1	Enable interrupt on trigger ETINT

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3.13.3 Analog Module Interrupt Enable (AMIEN) [R/W]

If this bit is set, an interrupt will be generated if the AM is requesting one. Not all AMs have this capability.

AMIEN	Function
0	Disable interrupt by analog module AMINT
1	Enable interrupt by analog module AMINT

3.13.4 Display Module Interrupt Enable (DMIEN) [R/W]

If this bit is set, an interrupt will be generated if the DM is requesting one.

DMIEN	Function
0	Disable interrupt by display module DMINT
1	Enable interrupt by display module DMINT

3.13.5 Computation Module Interrupt Enable (CMIEN) [R/W]

If this bit is set, an interrupt will be generated if the CM is requesting one. Not all CMs have this capability.

CMIEN	Function
0	Disable interrupt by computation module CMINT
1	Enable interrupt by computation module CMINT

3.14 INTERRUPT STATUS (ISTAT) [R–O]

I/O Base Address + 2CH *word or byte*

ISTAT

7							0
CMINT	DMINT	AMINT	ETINT	FINT	Reserved	Reserved	Reserved

This interrupt status port relays which interrupts are currently requesting service.

BIT	MNEMONIC	FUNCTION
0–2	*Reserved*	*Program to zero, read "don't care*
3	FINT	Frame Interrupt
4	ETINT	External Trigger Interrput
5	AMINT	Analog Module Interrupt
6	DMINT	Display Module Interrupt
7	CMINT	Computation Module Interrupt

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3.14.1 Frame Interrupt (FINT) [R–O]

A frame interrupt occurs if enabled by FIEN in the interrupts enable register (IEN). The FMIMOD and FMSEL(1–0) bits select the frame and condition that causes an interrupt.

FINT	Function
0	No interrupt
1	Interrupt requesting service

3.14.2 External Trigger Interrupt (ETINT) [R–O]

A trigger interrupt occurs if enabled by ETIEN in the interrupts enable register (IEN) upon the detection of an external trigger pulse from the analog module.

ETINT	Function
0	No interrupt
1	Interrupt requesting service

3.14.3 Analog Module Interrupt (AMINT) [R–O]

An analog module interrupt occurs if enabled by AMIEN in the interrupts enable register (IEN) and if the analog module is requesting an interrupt.

AMINT	Function
0	No interrupt
1	Interrupt requesting service

3.14.4 Display Module Interrupt (DMINT) [R–O]

A display module interrupt occurs if enabled by DMIEN in the interrupts enable register (IEN) and if the display module is requesting an interrupt.

DMINT	Function
0	No interrupt
1	Interrupt requesting service

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3.14.5 Computation Module Interrupt (CMINT) [R−O]

A computation module interrupt occurs if enabled by CMIEN in the interrupts enable register (IEN) and if the computational module is requesting an interrupt.

CMINT	Function
0	No interrupt
1	Interrupt requesting service

3.15 INTERRUPT ACKNOWLEDGE (INTACK) [W−O]

I/O Base Address + 2CH *word or byte*

INTACK (7 … 0)

CMACK	DMACK	AMACK	ETACK	FMACK	Reserved	Reserved	Reserved

This register is used to clear pending interrupts. The IMS uses the Reset On Register Access (RORA) implementation of the VME priority interrupt protocol. The interrupt handler is required to reset the interrupt by writing the appropriate bit in this register.

NOTE *While writing to the bits in this register negates the interrupt to the bus, it may not necessarily satisfy the requesting device. For example, a DM module using the 34010 will require a second write (to the 34010 host control port) to fully acknowledge the event.*

BIT	MNEMONIC	FUNCTION
0–2	*Reserved*	*Program to zero*
3	FMACK	Frame Interrupt Acknowledge
4	ETACK	External Trigger Interrput Acknowledge
5	AMACK	Analog Module Interrupt Acknowledge
6	DMACK	Display Module Interrupt Acknowledge
7	CMACK	Computation Module Interrupt

Acknowledge

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3.16 INTERRUPT PRIORITY LEVEL (IPRI) [R/W]

I/O Base Address + 2EH *word or byte*

IPRI

7							0
Reserved	Reserved	Reserved	Reserved	Reserved	IPRI2	IPRI1	IPRI0

During an interrupt acknowledge cycle, the host broadcasts a 3–bit priority code on address lines A03–A01 which are compared with the IPRI(3–0) bits. Only if a valid comparison is detected does the board respond by driving the interrupt vector onto the bus.

3.17 FRAME A0 ACQUISITION (ACQA0) [R/W]

I/O Base Address + 30H *word or byte*

ACQA0

7							0
ABTSA01	ABTSA00	SMA0	VBA0	Reserved	NEWAQA0	WTAQA0	TMODA0

This register controls acquisition to frame A0. The Input Cross–Port–Switch allows acquiring from many sources. Program the correct paths and frame timing prior to issuing an acquisition command.

BIT	MNEMONIC	FUNCTION
0	TMODA0	Trigger Mode
1	WTAQA0	Start Acquisition Disable
2	NEWAQA0	Acquisition Pending
3	*Reserved*	*Program to zero, read "don't care"*
4	VBA0	Vertical Blank
5	SMA0	Scan Mode
6	ABTSA00	Acquisition Mode Bit 0
7	ABTSA01	Acquisition Mode Bit 1

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3.17.1 Trigger Mode (TMODA0) [R/W]

This bit selects frame A0 acquisition on external event. If this bit is set high, the acquire begins and ends upon detection of the external trigger pulse. The external trigger is supplied by the AM and supports trigger on line or frame. The signal is synchronized locally to prevent false writes.

TMODA0	Function
0	Trigger disabled
1	Acquisition begins and ends on trigger

3.17.2 Wait Acquistion Start (WTAQA0) [R/W]

Setting this bit to a 1 will prevent an acquisition from occurring until the ACQEN register is written. This bit is used to synchronize camera acquisitions into multiple frame stores. To synchronize multiple frame acquisitions set this bit to 1 along with writing the ABTSA0 bits. After setting up all other frame store acquisition registers, with each WTAQA0 bit set to 1, a write to the ACQEN register will enable all frame acquisitions simultaneously. A write to the ACQEN register will reset this bit to 0. When this bit is not set to 1 acquisition will begin at the end of the next vertical blank after the ABTSA0 bits have been set.

WTAQA0	Function
0	Acquisition enabled
1	Acquisition disabled

3.17.3 New Acquire (NEWAQA0) [RO]

This bit is set to a 1 whenever a snap or grab command is written to this register. It will be reset to 0 when the acquisition begins.

NEWAQA0	Function
0	No acquisition pending
1	Acquisition pending

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3.17.4 Vertical Blank (VBA0) [R−O]

This bit provides vertical blanking status for frame A0. It is used to determine when to write the acquisition bits.

VBA0	Function
0	Vertical blank, (safe to write to ABTSA0)
1	Frame active or horizontal blank

3.17.5 Scan Mode (SMA0) [R−O]

This bit specifies the format of the incoming video for frame A0.

SMA0	Function
0	Interlaced video
1	Non–Interlaced video

3.17.6 Acquisition Mode (ABTSA0) [R/W]

These bits are dual–purpose in that they start an acquisition in frame A0 while providing status of the operation.

ABTSA01	ABTSA00	Function
0	0	Freeze (idle)
0	1	*Undefined*
1	0	Snap
1	1	Grab

On the IMS, these bits change state immediately when they are written. An operation begins at the leading edge of vertical blank and ends at the trailing edge (refer to Figure 3–2). Commands are not double buffered. Successive operations are accomplished by writing the ABTSA0 bits within the vertical blanking interval between frames. Clear operations are snaps with the data set to a constant value by the Cross–Port Switch.

Acquisition is controlled by a Scan Mode bit (SMA0) associated with the incoming frame. This bit represents interlaced/non–interlaced addressing. The IMS acquires one or two frames (fields) based upon the scan mode. Selective field acquiring is accomplished by polling the Status register, waiting for the opposite field from which to start acquisition and then setting the ABTSA0 bits.

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The frame (event) counter is associated with frame A0. When a snap command is issued, X frames are acquired as determined by the counter. Full frames are counted as defined by Scan Mode.

The IMS supports independent X and Y zoom on the write port. Zoom factors are 1X and 1/2X. If the Y zoom is set to 1 and the incoming frame is interlaced, the acquisition circuit will snap one field and the SAC will count non–interlaced.

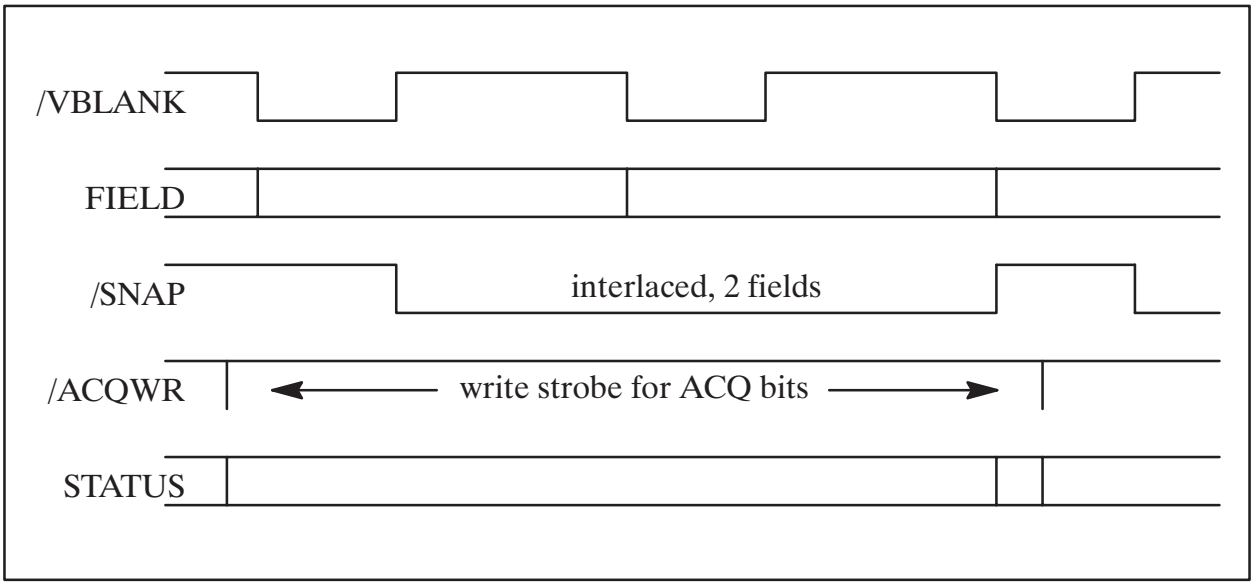


Figure 3−2. Acquisition Timing

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3.18 FRAME A1 ACQUISITION (ACQA1) [R/W]

I/O Base Address + 32H *word or byte*

ACQA1

7							0
ABTSA11	ABTSA10	SMA1	VBA1	Reserved	NEWAQA1	WTAQA1	TMODA1

This register controls acquisition to frame A1. Program the correct paths and frame timing prior to issuing an acquisition command.

BIT	MNEMONIC	FUNCTION
0	TMODA1	Trigger Mode
1	WTAQA1	Start Acquistion Disable
2	NEWAQA1	Acquisition Pending
3	*Reserved*	*Program to zero, read "don't care"*
4	VBA1	Vertical Blank
5	SMA1	Scan Mode
6	ABTSA10	Acquisition Mode Bit 0
7	ABTSA11	Acquisition Mode Bit 1

3.18.1 Trigger Mode (TMODA1) [R/W]

This bit selects frame A1 acquisition on external event. If this bit is set high, the acquire begins and ends upon detection of the external trigger pulse. The external trigger is supplied by the AM and supports trigger on line or frame. The signal is synchronized locally to prevent false writes.

TMODA1	Function
0	Trigger disabled
1	Acquisition begins and ends on trigger

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3.18.2 Wait Acquistion Start (WTAQA1) [R/W]

Setting this bit to a 1 will prevent an acquisition from occurring until the ACQEN register is written. This bit is used to synchronize camera acquisitions into multiple frame stores. To synchronize multiple frame acquisitions set this bit to 1 along with writing the ABTSA1 bits. After setting up all other frame store acquisition registers, with each WTAQA1 bit set to 1, a write to the ACQEN register will enable all frame acquisitions simultaneously. A write to the ACQEN register will reset this bit to 0. When this bit is not set to 1 acquisition will begin at the end of the next vertical blank after the ABTSA1 bits have been set.

WTAQA1	Function
0	Acquisition enabled
1	Acquisition disabled

3.18.3 New Acquire (NEWAQA1) [RO]

This bit is set to a 1 whenever a snap or grab command is written to this register. It will be reset to 0 when the acquisition begins.

NEWAQA1	Function
0	No acquisition pending
1	Acquisition pending

3.18.4 Vertical Blank (VBA1) [R−O]

This bit provides vertical blanking status for frame A1. It is used to determine when to write the acquisition bits.

VBA1	Function
0	Vertical blank (safe to write to ABTSA1)
1	Frame active or horizontal blank

3.18.5 Scan Mode (SM)A1 [R−O]

This bit specifies the format of the incoming video for frame A1.

State	Function
0	Interlaced video
1	Non–Interlaced video

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3.18.6 Acquisition Mode (ABTSA1) [R/W]

These bits are dual–purpose in that they start an acquisition in frame A1 while providing status of the operation.

ABTSA11	ABTSA10	Function
0	0	Freeze (idle)
0	1	*Undefined*
1	0	Snap
1	1	Grab

On the IMS, these bits change state immediately when they are written. An operation begins at the leading edge of vertical blank and ends at the trailing edge (refer to Figure 3–2, page 3–31). Commands are not double buffered. Successive operations are accomplished by writing the ABTSA1 bits within the vertical blanking interval between frames. Clear operations are snaps with the data set to a constant value by the Cross–Port Switch.

Acquisition is controlled by a Scan Mode bit (SMA1) associated with the incoming frame. This bit represents interlaced/non–interlaced addressing. The IMS acquires one or two frames (fields) based upon the scan mode. Selective field acquiring is accomplished by polling the Status register, waiting for the opposite field from which to start acquisition and then setting the ABTSA1 bits.

The frame (event) counter is associated with frame A0. When a snap command is issued, X frames are acquired as determined by the counter. Full frames are counted as defined by the scan mode.

The IMS supports independent X and Y zoom on the write port. Zoom factors are 1X and 1/2X. If the Y zoom is set to 1 and the incoming frame is interlaced, the acquisition circuit will snap one field and the SAC will count non–interlaced.

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3.19 ACQUISITION ENABLE (ACQEN) [WO]

I/O Base Address + 34H *word or byte*

ACQEN

7							0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

This register controls synchronous acquisition into the IMS frame stores. When an acquire is pending in any of the IMS acquisition registers, along with that register's WTAQ*xx* bit being set, a write to this register will clear any WTAQ*xx* bits and enable acquisition into the frame store.

3.20 FRAME B1 ACQUISITION (ACQB1) [R/W]

I/O Base Address + 36H *word or byte*

ACQB1

7							0
ABTSB11	ABTSB10	SMB1	VBB1	Reserved	NEWAQB1	WTAQB1	TMODB1

This register controls acquisition to frame B1. Program the correct paths and frame timing prior to issuing an acquisition command.

BIT	MNEMONIC	FUNCTION
0	TMODB1	Trigger Mode
1	WTAQB1	Start Acquisition Disable
2	NEWAQB1	Acquisition Pending
3	*Reserved*	*Program to zero, read "don't care"*
4	VBB1	Vertical Blank
5	SMB1	Scan Mode
6	ABTSB10	Acquisition Mode Bit 0
7	ABTSB11	Acquisition Mode Bit 1

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3.20.1 Trigger Mode (TMODB1) [R/W]

This bit selects frame B1 acquisition on external event. If this bit is set high, the acquire begins and ends upon detection of the external trigger pulse. The external trigger is supplied by the AM and supports trigger on line or frame. The signal is synchronized locally to prevent false writes.

TMODB1	Function
0	Trigger disabled
1	Acquisition begins and ends on trigger

3.20.2 Wait Acquistion Start (WTAQB1) [R/W]

Setting this bit to a 1 will prevent an acquisition from occurring until the ACQEN register is written. This bit is used to synchronize camera acquisitions into multiple frame stores. To synchronize multiple frame acquisitions set this bit to 1 along with writing the ABTSB1 bits. After setting up all other frame store acquisition registers, with each WTAB1Q bit set to 1, a write to the ACQEN register will enable all frame acquisitions simultaneously. A write to the ACQEN register will reset this bit to 0. When this bit is not set to 1 acquisition will begin at the end of the next vertical blank after the ABTSB1 bits have been set.

WTAQB1	Function
0	Acquisition enabled
1	Acquisition disabled

3.20.3 New Acquire (NEWAQB1) [RO]

This bit is set to a 1 whenever a snap or grab command is written to this register. It will be reset to 0 when the acquisition begins.

NEWAQB1	Function
0	No acquisition pending
1	Acquisition pending

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3.20.4 Vertical Blank (VBB1) [R−O]

This bit provides vertical blanking status for frame B1. It is used to determine when to write the acquisition bits.

VBB1	Function
0	Vertical blank (safe to write to ABTSB1)
1	Frame active or horizontal blank

3.20.5 Scan Mode (SMB1) [R−O]

This bit specifies the format of the incoming video for frame B1.

SMB1	Function
0	Interlaced video
1	Non–Interlaced video

3.20.6 Acquisition Mode (ABTSB1) [R/W]

These bits are dual–purpose in that they start an acquisition in frame B1 while providing status of the operation.

ABTSB11	ABTSB10	Function
0	0	Freeze (idle)
0	1	*Undefined*
1	0	Snap
1	1	Grab

On the IMS, these bits change state immediately when they are written. An operation begins at the leading edge of vertical blank and ends at the trailing edge (refer to Figure 3–2, page 3–31). Commands are not double buffered. Successive operations are accomplished by writing the ABTSB1 bits within the vertical blanking interval between frames. Clear operations are snaps with the data set to a constant value by the Cross–Port Switch.

Acquisition is controlled by a Scan Mode bit (SMB1) associated with the incoming frame. This bit represents interlaced/non–interlaced addressing. The IMS acquires one or two frames (fields) based upon the scan mode. Selective field acquiring is accomplished by polling the Status register, waiting for the opposite field from which to start acquisition and then setting the ABTSB1 bits.

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The frame (event) counter is associated with frame A0. When a snap command is issued, X frames are acquired as determined by the counter. Full frames are counted as defined by the scan mode.

The IMS supports independent X and Y zoom on the write port. Zoom factors are 1X and 1/2X. If the Y zoom is set to 1 and the incoming frame is interlaced, the acquisition circuit will snap one field and the SAC will count non–interlaced.

3.21 FRAME A0 READ PAN (RPANA0) [R/W]

Base Address + 40H *word only*

RPANA0

7							0
PAN7	PAN6	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PAN9	PAN8

This 10–bits register allows panning across a 1K horizontal line.

NOTE *Frame A0 and frame A1 read ports are synchronized. These registers are not double buffered and must be changed during vertical blank to avoid output jitter. Refer to Figure 3–3.*

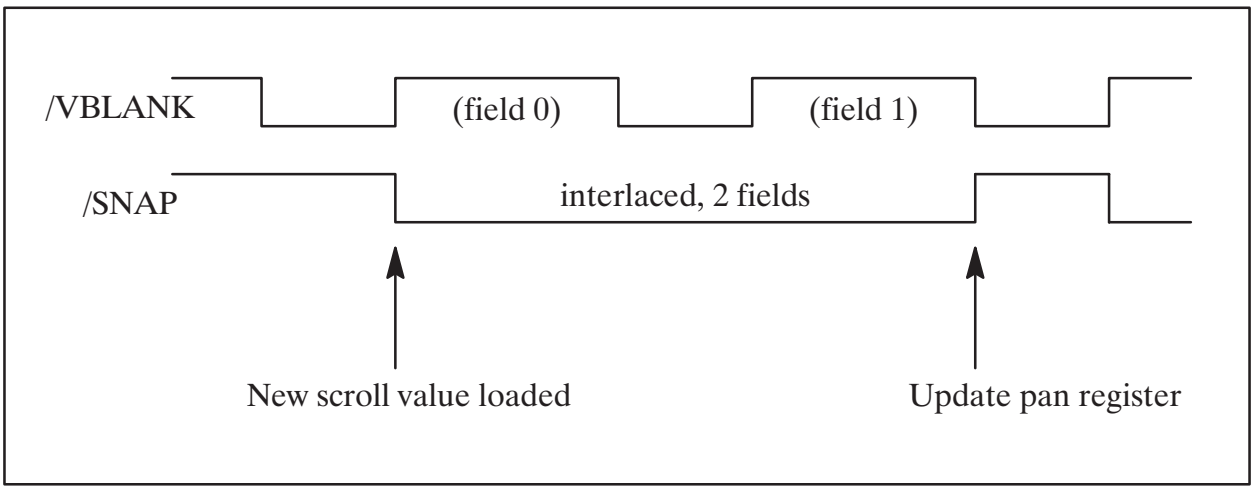


Figure 3–3. Pan and Scroll Update

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3.22 FRAME A0 READ SCROLL (RSCRA0) [R/W]

I/O Base Address + 42H *word only*

RSCRA0

7							0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCR9	SCR8

This 11–bit register allows scrolling through 1K lines.

3.23 FRAME A0 WRITE PAN (WPANA0) [R/W]

Base Address + 44H *word only*

WPANA0

7							0
PAN7	PAN6	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PAN9	PAN8

This 10–bits register allows panning across a 1K horizontal line.

NOTE *Frame A0 and frame A1 write ports are asynchronous. These registers are NOT double buffered and must be changed during vertical blank to avoid output jitter. Refer to Figure 3–3, page 3–41.*

3.24 FRAME A0 WRITE SCROLL (WSCRA0) [R/W]

I/O Base Address + 46H *word only*

WSCRA0

7							0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCR9	SCR8

This 11–bit register allows scrolling through 1K lines.

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3.25 FRAME A1 READ PAN (RPANA1) [R/W]

Base Address + 48H *word only*

RPANA1

7							0
PAN7	PAN6	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PAN9	PAN8

This 10–bits register allows panning across a 1K horizontal line.

NOTE *Frame A0 and frame A1 read ports are synchronized. These registers are NOT double buffered and must be changed during vertical blank to avoid output jitter. Refer to Figure 3–3, page 3–41*

3.26 FRAME A1 READ SCROLL (RSCRA1) [R/W]

I/O Base Address + 4AH *word only*

RSCRA1

7							0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCR9	SCR8

This 10–bit register allows scrolling through 1K lines.

3.27 FRAME A1 WRITE PAN (WPANA1) [R/W]

Base Address + 4CH *word only*

WPANA1

7							0
PAN7	PAN6	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PAN9	PAN8

This 10–bits register allows panning across a 1K horizontal line.

NOTE *Frame A0 and frame A1 write ports are asynchronous. These registers are NOT double buffered and must be changed during vertical blank to avoid output jitter. Refer to Figure 3–3, page 3–41*

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3.28 FRAME A1 WRITE SCROLL (WSCRA1) [R/W]

I/O Base Address + 4EH *word only*

WSCRA1

7							0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCR9	SCR8

This 10–bit register allows scrolling through 1K lines.

3.29 FRAME A CONTROL (CTLA) [R/W]

I/O Base Address + 50H *word or byte*

CTLA

7							0
WXZA1	WXZA0	WYZA1	WYZA0	A1BP	A0BP	Reserved	Reserved

This register controls the horizontal pitch, tiling and write zoom on frames A0 and A1. It should be updated during vertical blank. Frame 0 does not support read zoom. **This register is undefined at power–up.**

BIT	MNEMONIC	FUNCTION
0–1	*Reserved*	*Program to zero, read "don't care"*
2	A0BP	Bit–Pack Mode A0
3	A1BP	Bit–Pack Mode A1
4	WYZA0	Write Vertical Zoom Control A0
5	WYZA1	Write Vertical Zoom Control A1
6	WXZA0	Write Horizontal Zoom Control A0
7	WXZA1	Write Horizontal Zoom Control A1

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3.29.1 Binary Bit–Pack Mode (A0BP/A1BP) [R/W]

These two bits force frame A0 or A1 to sub–sample acquire by 8. In this mode, binary images are packed into bytes on a computational module and stored for fast host access.

A0BP	Function
0	Normal operation
1	Binary bit–pack frame A0

A1BP	Function
0	Normal operation
1	Binary bit–pack frame A1

3.29.2 Write Vertical Zoom Control Frame A0 (WYZA0) [R/W]

Frame A0 supports normal and sub–sampled acquisition. Zoom is controlled independently in X and Y. If this bit is set, the IMS captures every other line within a frame. Addressing is always non–interlaced in zoom mode. Thus, if this bit is set and WXZA0 is not during an interlaced acquisition, only one field will be acquired. This field will be correctly positioned in memory.

WYZA0	Function
0	Normal
1	Sub–sample Y direction, Frame A0

3.29.3 Write Vertical Zoom Control Frame A1 (WYZA1) [R/W]

Frame A1 supports normal and sub–sampled acquisition. Zoom is controlled independently in X and Y. If this bit is set, the IMS captures every other line within a frame. Addressing is always non–interlaced in zoom mode. Thus, if this bit is set and WXZA1 is not set during an interlaced acquisition, only one field will be acquired. This field will be correctly positioned in memory.

WYZA1	Function
0	Normal
1	Sub–sample Y direction, Frame A1

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3.29.4 Write Horizontal Zoom Control Frame A0 (WXZA0) [R/W]

This bit set causes every other pixel to be acquired into frame A0.

WXZA0	Function
0	Normal
1	Sub–sample X direction, Frame A0

3.29.5 Write Horizontal Zoom Control Frame A1 (WXZA1) [R/W]

This bit set causes every other pixel to be acquired into frame A1.

WXZA1	Function
0	Normal
1	Sub–sample X direction, Frame A1

3.30 FRAME B1 READ PAN (RPANB1) [R/W]

Base Address + 52H *word only*

RPANB1

7							0
PAN7	PAN6	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PAN9	PAN8

This 10–bit register allows panning across a 1K horizontal line.

3.31 FRAME B1 READ SCROLL (RSCRB1) [R/W]

I/O Base Address + 54H *word only*

RSCRB1

7							0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCR9	SCR8

This 10–bit register allows scrolling through 1K lines.

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3.32 FRAME B1 WRITE PAN (WPANB1) [R/W]

Base Address + 56H *word only*

WPANB1

7							0
PAN7	PAN6	PAN5	PAN4	PAN3	PAN2	PAN1	PAN0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	PAN9	PAN8

This 10–bit register allows panning across a 1K horizontal line.

3.33 FRAME B1 WRITE SCROLL (WSCRB1) [R/W]

I/O Base Address + 58H *word only*

WSCRB1

7							0
SCR7	SCR6	SCR5	SCR4	SCR3	SCR2	SCR1	SCR0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	SCR9	SCR8

This 10–bit register allows scrolling through 1K lines.

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3.34 FRAME B CONTROL (CTLB) [R/W]

I/O Base Address + 5AH *word or byte*

CTLB

7							0
WXZB1	B1BP	WYZB1	Reserved	DISPYZ1	DISPYZ0	DISPXZ1	DISPXZ0

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register controls the horizontal pitch, tiling and zoom on frames B0 and B1. It should be updated during vertical blank. Frame B1 supports zoom on the read port for display. **This register is undefined at power–up.**

BIT	MNEMONIC	FUNCTION
0	DISPXZ0	Display Horizontal Zoom Bit 0
1	DISPXZ1	Display Horizontal Zoom Bit 1
2	DISPYZ0	Display Vertical Zoom Bit 0
3	DISPYZ1	Display Vertical Zoom Bit 1
4	*Reserved*	*Program to zero, read "don't care"*
5	WYZB1	Write Vertical Zoom B1
6	B1BP	Frame B1 Bit–Pack Mode
7	WXZB1	Write Horizontal Zoom B1

3.34.1 Display Horizontal Zoom (DISPXZ) [R/W]

These two bits define the display horizontal zoom factor on frame B1. This frame is optionally used for display and hence needs to support zooming. Horizontal zooming is by pixel replication and the amount of zoom is defined as follows:

DISPXZ1	DISPXZ0	Function
0	0	Zoom by 1 horizontal (default) No zoom
0	1	Zoom by 2 horizontal
1	0	Zoom by 4 horizontal
1	1	*Reserved/undefined*

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3.34.2 Display Vertical Zoom (DISPYZ) [R/W]

These two bits define the display vertical zoom factor on frame B1. This frame is optionally used for display and hence needs to support zooming. Vertical zooming is by line replication and the amount of zoom is defined as follows:

DISPYZ1	DISPYZ0	Function
0	0	Zoom by 1 vertical (default) No zoom
0	1	Zoom by 2 vertical
1	0	Zoom by 4 vertical
1	1	*Reserved/undefined*

3.34.3 Write Vertical Zoom Frame B1 (WYZB1) [R/W]

Frame B supports normal and sub–sampled acquisition. Zoom is controlled independently in X and Y. If this bit is set, the IMS captures every other line within a frame. Addressing is always non–interlaced in zoom mode. Thus, if this bit is set and WXZ1 is not set during an interlaced acquisition, only one field will be acquired. This field will be correctly positioned in memory.

WYZB1	Function
0	Normal
1	Sub–sample in Y direction, Frame B1

3.34.4 Binary Bit–Pack Mode (B1BP) [R/W]

This bit forces frame B1 to sub–sample acquire by 8. In this mode, binary images are packed into bytes on a computational module and stored for fast host access.

B1BP	Function
0	Normal operation
1	Binary bit–pack frame B1

3.34.5 Write Horizontal Zoom Frame B1 (WXZB1) [R/W]

This bit causes every other pixel to be acquired into frame B1.

WXZB1	Function
0	Normal
1	Sub–sample in X direction, Frame B1

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3.35 CM INPUT TWO PATH (PCM2) [R/W]

Base Address + 60H *word or byte*

PVB2

7							0
1	PVB2F	PVB2S2	PVB2S1	PVB2S0	Reserved	Reserved	Reserved

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register selects one of five input ports to drive the VCM2 bus. Video bus timing is derived from the camera (AM) or AOI timing, as selected by the AOIMODE bit in the AOI Control register.

3.35.1 Input Bus Select (PVB2S) [R/W]

These three bits control the CPS to select the data output onto the VCM2 bus (when PVB2F is zero).

PVB2S2	PVB2S1	PVB2S0	Input Data Path
0	0	1	Frame A0
0	1	0	Constant
0	1	1	Frame A1
1	1	0	Frame B1
1	1	1	Camera

All other combinations are undefined

3.35.2 Output Function Select (PVB2F) [R/W]

This bit defines special operations for PVB2S2 and PVB2S1. PVB2S1 forces the output port into three–state (tri–state). This mode should not be used. If PVB2F is set, the output port is set to the value programmed in PVB2S2. This mode can be used for frame clears.

PVB2F	PVB2S2	PVB2S1	Operation
0	X	X	Normal operation of PVB2S
1	X	0	Enable video bus 2 output
1	X	1	Disable (tri–state) video bus 2 outputs
1	0	0	Set video bus 2 output to all zeros
1	1	0	Set video bus 2 output to all ones

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3.36 CM INPUT ONE PATH (PVB1) [R/W]

Base Address + 62H *word or byte*

PVB1

7							0
1	PVB1F	PVB1S2	PVB1S1	PVB1S0	Reserved	Reserved	Reserved

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register selects one of five input ports to drive the VCM1 bus. Video bus timing is derived from the camera (AM) or AOI timing, as selected by the AOIMODE bit in the AOI Control register.

3.36.1 Input Bus Select (PVB1S) [R/W]

These three bits control the CPS to select the data output onto the VCM1 bus (when PVB2F is zero).

PVB1S2	PVB1S1	PVB1S0	Input Data Path
0	0	1	Frame A0
0	1	0	Constant
0	1	1	Frame A1
1	1	0	Frame B1
1	1	1	Camera

All other combinations are undefined

3.36.2 Output Function Select (PVB1F) [R/W]

This bit defines special operations for PVB1S2 and PVB1S1. PVB1S1 forces the output port into three–state (tri–state). This mode should not be used. If PVB1F is set, the output port is set to the value programmed in PVB1S2. This mode can be used for frame clears.

PVB1F	PVB1S2	PVB1S1	Operation
0	X	X	Normal operation of PVB1S
1	X	0	Enable video bus 1 output
1	X	1	Disable (tri–state) video bus 1 outputs
1	0	0	Set video bus 1 output to all zeros
1	1	0	Set video bus 1 output to all ones

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3.37 CM INPUT ZERO PATH (PVB0) [R/W]

Base Address + 64H *word or byte*

PVB0

7							0
1	PVB0F	PVB0S2	PVB0S1	PVB0S0	Reserved	Reserved	Reserved

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register selects one of five input ports to drive the VCM0 bus. Video bus timing is derived from the camera (AM) or AOI timing, as selected by the AOIMODE bit in the AOI Control register.

3.37.1 Input Bus Select (PVB0S) [R/W]

These three bits control the CPS to select the data output onto the VCM0 bus (when PVB2F is zero).

PVB0S2	PVB0S1	PVB0S0	Input Data Path
0	0	1	Frame A0
0	1	0	Constant
0	1	1	Frame A1
1	1	0	Frame B1
1	1	1	Camera

All other combinations are undefined

3.37.2 Output Function Select (PVB0F) [R/W]

This bit defines special operations for PVB0S2 and PVB0S1. PVB0S1 forces the output port into three–state (tri–state). This mode should not be used. If PVB0F is set, the output port is set to the value programmed in PVB0S2. This mode can be used for frame clears.

PVB0F	PVB0S2	PVB0S1	Operation
0	X	X	Normal operation of PVB0S
1	X	0	Enable video bus 0 outputs
1	X	1	Disable (tri–state) video bus 0 outputs
1	0	0	Set video bus 0 output to all zeros
1	1	0	Set video bus 0 output to all ones

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3.38 PIPELINE CONTROL (PIPECON) [R/W]

Base Address + 66H *word or byte*

PIPECON

7							0
1	**1**	**0**	**0**	CMBYP	PCM2S	PCM1S	PCM0S

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register controls the computation module input MUX. Bits 7–4 must be programmed to 1100B.

3.38.1 PCM0 Bus Select (PCM0S) [R/W]

This bit defines which bus (VCM0 or PI0) will drive the PCM0 bus

PCM0S	Function
0	Pass the VCM0 bus to the PCM0 bus
1	Pass the PI0 bus to the PCM0 bus

NOTE *When any one of the PI (150/40 Pipeline Buses 0,1 or 2) busses are selected to drive the PCM (CM Module Input Busses 0,1 or 2) busses the 150/40 PI bus Frame timing will drive the PCM frame timing.*

NOTE *When none of the PI (150/40 Pipeline Buses 0,1 or 2) busses are selected to drive the PCM (CM Module Input Busses 0,1 or 2) busses the VCM bus Frame timing will drive the PCM frame timing.*

3.38.2 PCM1 Bus Select (PCM1S) [R/W]

This bit defines which bus (VCM1 or PI1) will drive the PCM1 bus

PCM1S	Function
0	Pass the VCM1 bus to the PCM1 bus
1	Pass the PI1 bus to the PCM1 bus

NOTE *When any one of the PI (150/40 Pipeline Buses 0,1 or 2) busses are selected to drive the PCM (CM Module Input Busses 0,1 or 2) busses the 150/40 PI bus Frame timing will drive the PCM frame timing.*

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NOTE *When none of the PI (150/40 Pipeline Buses 0,1 or 2) busses are selected to drive the PCM (CM Module Input Busses 0,1 or 2) busses the VCM bus Frame timing will drive the PCM frame timing.*

3.38.3 PCM2 Bus Select (PCM2S) [R/W]

This bit defines which bus (VCM2 or PI2) will drive the PCM2 bus

PCM2S	Function
0	Pass the VCM2 bus to the PCM2 bus
1	Pass the PI2 bus to the PCM2 bus

NOTE *When any one of the PI (150/40 Pipeline Buses 0,1 or 2) busses are selected to drive the PCM (CM Module Input Busses 0,1 or 2) busses the 150/40 PI bus Frame timing will drive the PCM frame timing.*

NOTE *When none of the PI (150/40 Pipeline Buses 0,1 or 2) busses are selected to drive the PCM (CM Module Input Busses 0,1 or 2) busses the VCM bus Frame timing will drive the PCM frame timing.*

3.38.4 CM Bypass (CMBYP) [R/W]

This bit defines which bus group (24 bits) is passed to the CM buses.

CMBPY	Function
0	Pass the CM Module output to the CM busses (CM0,1 & 2)
1	Pass the CM Module input (PCM0,1 & 2) to the CM bus (CM0,1 & 2)

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3.39 CM INPUT THREE PATH (PVB3) [R/W]

Base Address + 68H *word or byte*

PVB3

7							0
1	PVB3F	PVB3S2	PVB3S1	PVB3S0	Reserved	Reserved	Reserved

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

This register selects one of five input ports to drive the VCM3 bus. Video bus timing is derived from the camera (AM) or AOI timing, as selected by the AOIMODE bit in the AOI Control register.

3.39.1 Input Bus Select (PVB3S) [R/W]

These three bits control the CPS to select the data output onto the VCM3 bus (when PVB3F is zero).

PVB3S2	PVB3S1	PVB3S0	Input Data Path
0	0	1	Frame A0
0	1	0	Constant
0	1	1	Frame A1
1	1	0	Frame B1
1	1	1	Camera

All other combinations are undefined

3.39.2 Output Function Select (PVB3F) [R/W]

This bit defines special operations for PVB3S2 and PVB3S1. PVB3S1 forces the output port into three–state (tri–state). This mode should not be used. If PVB3F is set, the output port is set to the value programmed in PVB3S2. This mode can be used for frame clears.

PVB3F	PVB3S2	PVB3S1	Operation
0	X	X	Normal operation of PVB3S
1	X	0	Enable video bus 3 output
1	X	1	Disable (tri–state) video bus 3 outputs
1	0	0	Set video bus 3 output to all zeros

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1	1	0	Set video bus 3 output to all ones

3.40 FRAME A0 INPUT PATH (FA0SEL) [R/W]

Base Address + 6AH *word only*

FA0SEL

7							0
1	FA0F	FA0S2	FA0S1	FA0S0	Reserved	Reserved	Reserved

15						8	
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FA0FTS1	FA0FTS0

This register selects one of eight input ports to drive the FA0I bus. Video bus timing is derived from FA0S bits in this register.

3.40.1 Input Bus Select (FA0S) [R/W]

These three bits control the CPS to select the data input for frame A0 (when FA0F is zero).

FA0S2	FA0S1	FA0S0	Input Data Path
0	0	0	CM Output 2
0	0	1	Frame A0
0	1	0	Constant
0	1	1	Frame A1
1	0	0	CM Output 0
1	0	1	CM Output 1
1	1	0	Frame B1
1	1	1	Camera

3.40.2 Output Function Select (FA0F) [R/W]

This bit defines special operations for FA0S2 and FA0S1. FA0S2 forces the FA0 input port into three–state (tri–state). This mode should not be used. If FA0F is set, the input port is set to the value programmed in FA0S1. This mode can be used for frame clears.

FA0F	FA0S2	FA0S1	Operation
0	X	X	Normal operation of SEL(03–00)
1	0	X	Enable frame A0 input
1	1	X	Disable (tri–state) frame A0 input
1	0	0	Set frame A0 input to all zeros
1	0	1	Set frame A0 input to all ones

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3.40.3 A0 Frame Timing Select (FA0FTS) [R/W]

These two bits select the frame timing to drive the A0 write ports. The value programmed in these bits should correspond with the data FA0 data path selected by the A0 input data select bits (FA0S)

FA0FTS1	FA0FTS0	Frame Timing
0	0	Camera timing
0	1	CM timing
1	0	Video bus timing
1	1	Undefined

The relationship of these bits to the data path select bits is listed below.

FA0FTS1	FA0FTS0	FA0S2	FA0S1	FA0S0	Input Path
0	1	0	0	0	CM Output 2
1	0	0	0	1	Frame A0
X	X	0	1	0	Constant
1	0	0	1	1	Frame A1
0	1	1	0	0	CM Output 0
0	1	1	0	1	CM Output 1
1	0	1	1	0	Frame B1
0	0	1	1	1	Camera

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3.41 FRAME A1 INPUT PATH (FA1SEL) [R/W]

Base Address + 6CH *word only*

FA1SEL

7							0
1	FA1F	FA1S2	FA1S1	FA1S0	Reserved	Reserved	Reserved

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FA1FTS1	FA1FTS0

This register selects one of eight input ports to drive the FA1I bus. Video bus timing is derived from FA1S bits in this register.

3.41.1 Input Bus Select (FA1S) [R/W]

These three bits control the CPS to select the data input to frame A1 (when OFS is zero).

FA1S2	FA1S1	FA1S0	Input Data Path
0	0	0	CM output 2
0	0	1	Frame A0
0	1	0	Constant
0	1	1	Frame A1
1	0	0	CM output 0
1	0	1	CM output 1
1	1	0	Frame B1
1	1	1	Camera

3.41.2 Output Function Select (FA1F) [R/W]

This bit defines special operations for FA1S2 and FA1S1. FA1S2 forces the output port into three–state (tri–state). This mode should not be used. If FA1F is set, the output port is set to the value programmed in FA1S1. This mode can be used for frame clears.

OFS	FA1S2	FA1S1	Operation
0	X	X	Normal operation of FA1S
1	0	X	Enable frame A1 input
1	1	X	Disable (tri–state) frame A1 input
1	0	0	Set frame A1 input to all zeros
1	0	1	Set frame A1 input to all ones

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3.41.3 A1 Frame Timing Select (FA1FTS) [R/W]

These two bits select the frame timing to drive the A1 write ports. The value programmed in these bits should correspond with the data A1 data path selected by the A1 input data select bits FA1S

FA1FTS1	FA1FTS0	Frame Timing
0	0	Camera timing
0	1	CM Timing
1	0	Video Bus Timing
1	1	Undefined

The relationship of these bits to the data path select bits is listed below.

FA1FTS1	FA1FTS0	FA1S2	FA1S1	FA1S0	Input Path
0	1	0	0	0	CM Output 2
1	0	0	0	1	Frame A0
X	X	0	1	0	Constant
1	0	0	1	1	Frame A1
0	1	1	0	0	CM Output 0
0	1	1	0	1	CM Output 1
1	0	1	1	0	Frame B1
0	0	1	1	1	Camera

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3.42 FRAME B1 INPUT PATH (FB1SEL) [R/W]

Base Address + 6EH *word only*

FB1SEL

7							0
1	FB1F	FB1S2	FB1S1	FB1S0	Reserved	Reserved	Reserved

15							8
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	FB1FTS1	FB1FTS0

This register selects one of eight input ports to drive the FB1I bus. Video bus timing is derived from FB1S bits in this register.

3.42.1 Input Bus Select (FB1S) [R/W]

These three bits control the CPS to select the data input to frame B1 (when FB1F is zero).

FB1S2	FB1S1	FB1S0	Input Data Path
0	0	0	CM output 2
0	0	1	Frame A0
0	1	0	Constant
0	1	1	Frame A1
1	0	0	CM output 0
1	0	1	CM output 1
1	1	0	Frame B1
1	1	1	Camera

3.42.2 Output Function Select (OFS) [R/W]

This bit defines special operations for FB1S2 and FB1S1. FB1S2 forces the input port into three–state (tri–state). This mode should not be used. If FB1F is set, the input port is set to the value programmed in FB1S1. This mode can be used for frame clears.

FB1F	FB1S2	FB1S1	Operation
0	X	X	Normal operation of FB1S
1	0	X	Enable frame B1 input
1	1	X	Disable (tri–state) frame B1 input
1	0	0	Set frame B1 input to all zeros
1	0	1	Set frame B1 input to all ones

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3.42.3 B1 Frame Timing Select (FB1FTS) [R/W]

These two bits select the frame timing to drive the B1 write ports. The value programmed in these bits should correspond with the data B1 data path selected by the B1 input data select bits FB1S

FB1FTS1	FB1FTS0	Frame Timing
0	0	Camera timing
0	1	CM timing
1	0	Video bus timing
1	1	Undefined

The relationship of these bits to the data path select bits is listed below.

FB1FTS1	FB1FTS0	FB1S2	FB1S1	FB1S0	Input Path
0	1	0	0	0	CM output 2
1	0	0	0	1	Frame A0
X	X	0	1	0	Constant
1	0	0	1	1	Frame A1
0	1	1	0	0	CM output 0
0	1	1	0	1	CM output 1
1	0	1	1	0	Frame B1
0	0	1	1	1	Camera

3.43 CROSS–PORT SWITCH CONTROL (CPSCTL) [R/W]

I/O Base Address + 70H (through 7FH) *word only*

CPSCTL

7							0
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**

This register (70H) configures the switch for the application bus width and direction. This register must be programmed as indicated. Addresses 71H through 7FH reflect the data at 70H. Program this register before programming any of the path registers.

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CHAPTER 4
CONFIGURATION

This chapter describes the factory configuration of the IMS and altering the switch settings for each option. Read this chapter to make sure the IMS configuration suits the application. The configurable options are:

- Register Base Address
- Interrupt Level

4.1 FACTORY DEFAULT CONFIGURATION

The factory configures the IMS as follows:

- Register base address 0600H
- Interrupts disabled

Table 4–1 summarizes the switch settings for this configuration. Figure 4–1 shows switch locations on the board, for register base address 0600H. The black dots indicate the position or direction a switch is “thrown”. Use the board diagram at the end of this chapter to document changes to the factory default configuration.

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Table 4−1. Factory Default Configuration

Jumper	Position	Function
SW1,1	A	*Not Used*
SW1,2	A	*Not used*
SW1,3	B	Trigger input C31 and strobe output A31
SW1,4	B	Register Base Address, Bit A7
SW2,1	A	*Not used*
SW2,2	A	Interrupt Level, IRQ1
SW2,3	A	Interrupt Level, IRQ2
SW2,4	A	Interrupt Level, IRQ3
SW2,5	A	Interrupt Level, IRQ4
SW2,6	A	Interrupt Level, IRQ5
SW2,7	A	Interrupt Level, IRQ6
SW2,8	A	Interrupt Level, IRQ7
SW3,1	B	Register Base Address, Bit A15
SW3,2	B	Register Base Address, Bit A14
SW3,3	B	Register Base Address, Bit A13
SW3,4	B	Register Base Address, Bit A12
SW3,5	B	Register Base Address, Bit A11
SW3,6	A	Register Base Address, Bit A10
SW3,7	A	Register Base Address, Bit A9
SW3,8	B	Register Base Address, Bit A8

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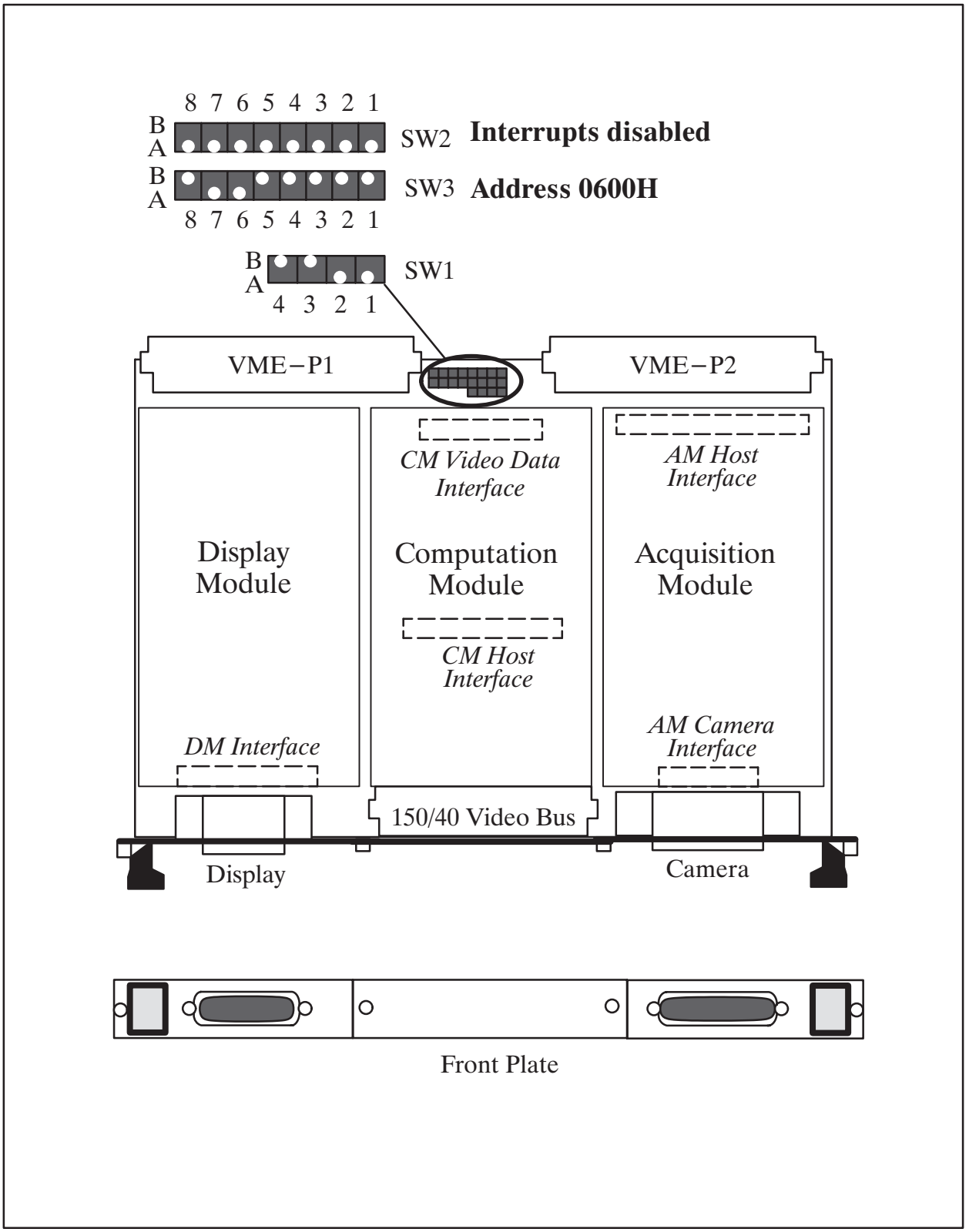


Figure 4−1. IMS Factory Default

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4.2 REGISTER BASE ADDRESS

The IMS registers occupy 128 words in I/O address space. The registers are I/O mapped beginning at the I/O base address. Each register appears at an offset from this address. The IMS compares VMEbus address lines A15–A7 to the switch selected register base address. Address lines A6–A1 select individual IMS registers. Table 4–2 shows the hexadecimal and binary coding for the register base address 0600H. The switches correspond directly to address lines, and form binary and hexadecimal numbers. Other addresses can be deduced from Table 4–2.

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Table 4–2. Default Register Base Address

VMEbus Address Line	Hex Address	Binary Address	Switch	State
msb A15	0	0	SW3,1	B
A14		0	SW3,2	B
A13		0	SW3,3	B
A12		0	SW3,4	B
A11	6	0	SW3,5	B
A10		1	SW3,6	A
A9		1	SW3,7	A
A8		0	SW3,8	B
A7	0	0	SW1,4	B
A6		*	N/A	
A5		*	N/A	
A4		*	N/A	
A3	0	*	N/A	
A2		*	N/A	
A1		*	N/A	
lsb A0		*	N/A	

N/A Not applicable: no switch associated with this address line

* Address lines A7–A1 decode offset to specific registers

Only one IMS is allowed on the 150/40 video bus, multiple IMA and CMC boards may be combined with the IMS. Table 4–3 and Figure 4–2 show some alternative addresses for the IMS. Other addresses and combinations are possible.

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Table 4−3. Alternative Register Base Addresses

Switch	0200H	0400H	0800H	1600H	2600H	3600H
SW3,1	B	B	B	B	B	B
SW3,2	B	B	B	B	B	B
SW3,3	B	B	B	B	A	A
SW3,4	B	B	B	A	B	A
SW3,5	B	B	A	B	B	B
SW3,6	B	A	B	A	A	A
SW3,7	A	B	B	A	A	A
SW3,8	B	B	B	B	B	B

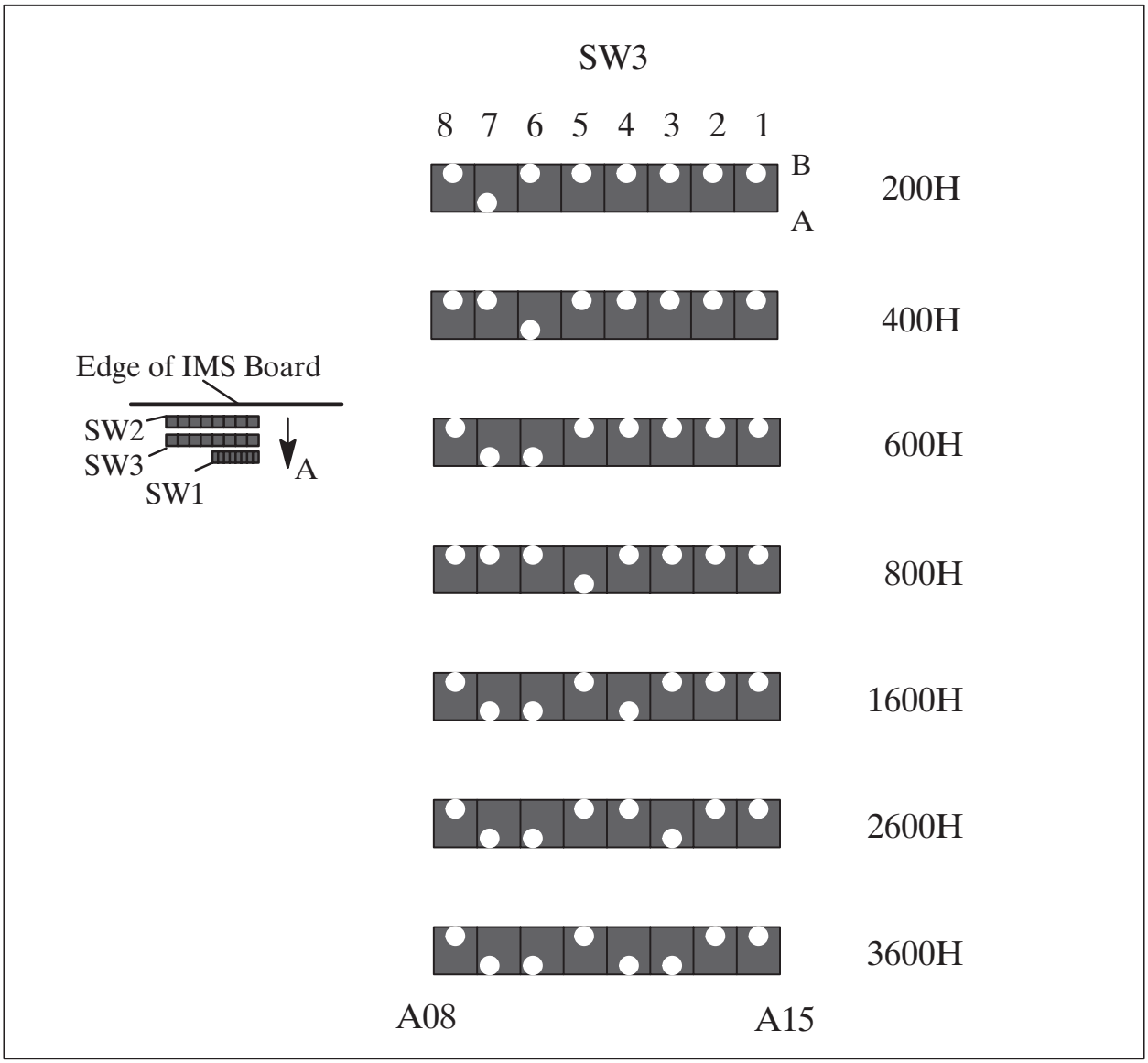


Figure 4−2. Address Settings

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4.3 INTERRUPT LEVEL

The IMS can interrupt the host computer using one of the seven request lines on the host bus. The conditions causing an interrupt are under software control. Switches SW2,2 through SW2,8 select the interrupt line, as shown in Table 4–4. **Select only one interrupt line.** Computers that do not support vectored interrupts recognize the requesting device by the interrupt request line asserted. There is no connection to IRQ0. All interrupt lines are disabled in the factory configuration.

Table 4–4. Interrupt Levels

Switch	Interrupt	Enabled	Disabled
SW2,2	IRQ1	B	A
SW2,3	IRQ2	B	A
SW2,4	IRQ3	B	A
SW2,5	IRQ4	B	A
SW2,6	IRQ5	B	A
SW2,7	IRQ6	B	A
SW2,8	IRQ7	B	A

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Document Changes to the Factory Configuration

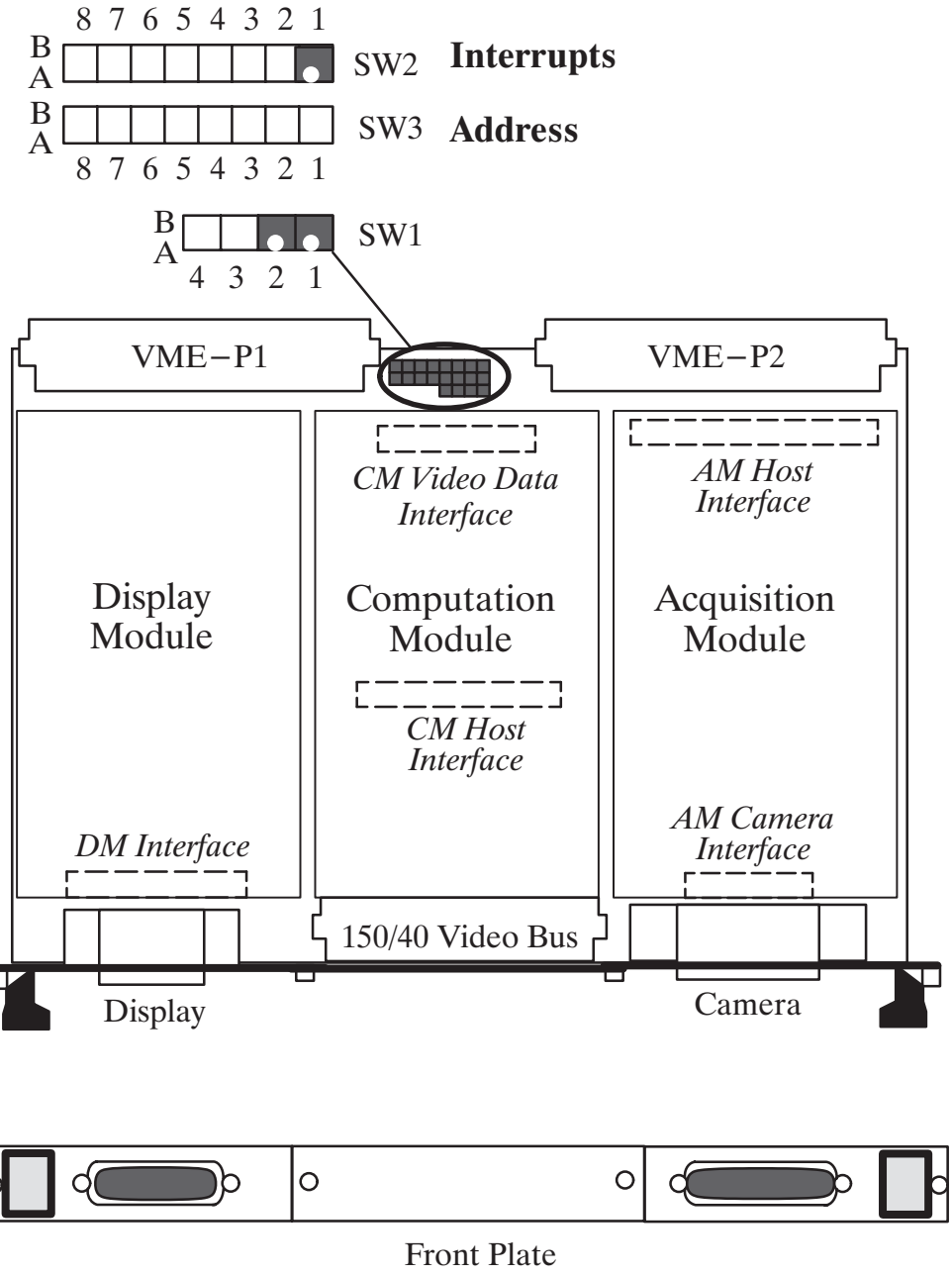


Figure 4−3. IMS Board Diagram

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4.4 STROBE/TRIGGER LOCATION

This switch determines the origin of the external trigger input and the destination of the strobe output.

Switch	Position	Function
SW1,3	B	Trigger input on VME–P2 connector, pin C3; Strobe output on VME–P2 pin C4
	A	Trigger input on VME–P2 connector, pin C2; Strobe output on VME–P2 pin C1

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APPENDIX A
IMS CONNECTORS

DISPLAY CONNECTOR

The IMS provides a 25–pin D–Subminature connector providing connections for the display module video output and the CM–PA serial I/O.

The display connector on the IMS is not plug–compatible with VGA display cables. There are two different display adaptor cables for the IMS, one for VGA compatibility, and one for BNC connections. Refer to Appendix B.

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Table A−1. Display Connector

Pin	Name	Function
1	—	Not Used
2	—	Not Used
3	—	Not Used
4	—	Not Used
5	—	Not Used
6	—	Not Used
7	—	Not Used
8	GND	Ground connection
9	RED	Red video output
10	—	Not Used
11	—	Not Used
12	—	Not Used
13	—	Not Used
14	SIND1	Serial port data input
15	—	Not Used
16	CSYNC	Composite synchronization
17	GND	Ground connection
18	GREEN	Green video output
19	SOUD1	Serial port data output
20	SOUF1	Serial port data output framing signal
21	SINF1	Serial port data input framing signal
22	HSYNC	Horizontal synchronization
23	VSYNC	Vertical synchronization
24	DMLEN	
25	GND	Ground connection
26	BLUE	Blue video output

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VIDEO INPUT CONNECTOR

The video input connector is a high–density 44–pin D–Sub connector with camera inputs for the AM.

Table A–2. Video Input Connector

Pin #	Name	Function	Break Out Connector & Pin #
1	+ 12 Volt – CAM3	Camera 3 + 12V	CAM3_p15
2	+ 12 Volt GND – CAM3	Camera 3 + 12V return	CAM3_p10
3	+ 12 Volt – CAM2	Camera 2 + 12V	CAM2_p15
4	+ 12 Volt GND – CAM2	Camera 2 + 12V return	CAM2_p10
5	+ 12 Volt – CAM1	Camera 1 + 12V	CAM1_p15
6	+ 12 Volt GND – CAM1	Camera 1 + 12V return	CAM1_p10
7	+ 12 Volt – CAM0	Camera 0 + 12V	CAM0_p15
8	+ 12 Volt GND – CAM0	Camera 0 + 12V return	CAM0_p10
9	+ 12 Volt – input	External + 12 Volt input	MISC_p1
10	+ 12 Volt GND – input	External + 12 Volt Supply return	MISC_p6
11	Dgnd	Digital GND	MISC_p8
12	Camera 0 GND	Camera 0 Analog Gnd	CAM0_p7,6,8
13	Camera 1–B	Camera 1–B Analog Video	CAM1_p1
14	Camera 2–A GND	Camera 2 Analog Gnd	CAM2_p7
15	Camera 3–A	Camera 3 Analog Video	CAM3_p2
16	CAM3 – C/HSYNC I/O	Camera 3 C or Hsyncs	CAM3_p13
17	CAM3 – DGND	Camera 3 Digital GND	CAM3_p5
18	CAM2 – VSYNC I/O	Camera 2 Vsync or Vdrive	CAM2_p14
19	CAM1 – VSYNC I/O	Camera 1 Vsync,Vdrive or FEN	CAM1_p14
20	CAM1 – CLK I/O	Camera 1 Pixel CLK I/O	CAM1_p4
21	CAM1 – Misc.	Camera 1 Frame Rst, Line Xfer, etc.	CAM1_p9
22	CAM0 – CLK I/O	Camera 0 Pixel CLK I/O	CAM0_p4

(continued)

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Table A−2 Continued. (Video Input Connector)

Pin #	Name	Function	Break Out Connector & Pin #
23	CAM0 – Misc.	Camera 0 Frame Rst, Line Xfer, etc.	CAM0_p9
24	+12 Volt – input	External + 12 Volt input	MISC_p1
25	+12 Volt GND – input	External + 12 Volt Supply return	MISC_p6
26	Misc. 1	Misc. signal 1– Strobe, Trigger, etc.	MISC_p3
27	Camera 0–B	Camera 0–B Analog Video	CAM0_p1
28	Camera 1–C	Camera 1–C Analog Video	CAM1_p3
29	Camera 1–A	Camera 1–A Analog Video	CAM1_p2
30	Camera 3–A Gnd	Camera 3 Analog Gnd	CAM3_p7
31	CAM3 – Vsync I/O	Camera 3 Vsync or Vdrive	CAM3_p14
32	CAM2 – C/HSYNC I/O	Camera 2 C or Hsyncs	CAM2_p13
33	CAM2 – DGND	Camera 2 Digital GND	CAM2_p5
34	CAM1 – C/HSYNC I/O	Camera 1 C,Hsyncs or LEN	CAM1_p13
35	CAM1 – DGND	Camera 1 Digital GND	CAM1_p5
36	CAM0 – C/HSYNC I/O	Camera 0 C,Hsyncs or LEN	CAM0_p13
37	CAM0 – VSYNC I/O	Camera 0 Vsync,Vdrive or FEN	CAM0_p14
38	CAM0 – DGND	Camera 0 Digital GND	CAM0_p5
39	Misc. 2	Misc. signal 2– Strobe, Trigger, etc.	MISC_p4
40	Misc. 3	Misc. signal 3– Strobe, Trigger, etc.	MISC_p5
41	Camera 0–C	Camera 0–C Analog Vide	CAM0_p3
42	Camera 0–A	Camera 0–A Analog Video	CAM0_p2
43	Camera 1 GND	Camera 1 Analog Gnd	CAM1_p7,6,8
44	Camera 2–A	Camera 2 Analog Video	CAM2_p2

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APPENDIX B
VIDEO CABLES and CONNECTORS

VIDEO OUTPUT CABLES

There are two video output cables for the IMS. The Display Adapter Cable (labeled 4625) adapts the 25–pin connector on the IMS to be compatible with standard VGA 15–pin cables and connectors. The Display Coax Cable (labeled 4626) adapts the 25–pin connector on the IMS to six BNC connectors.

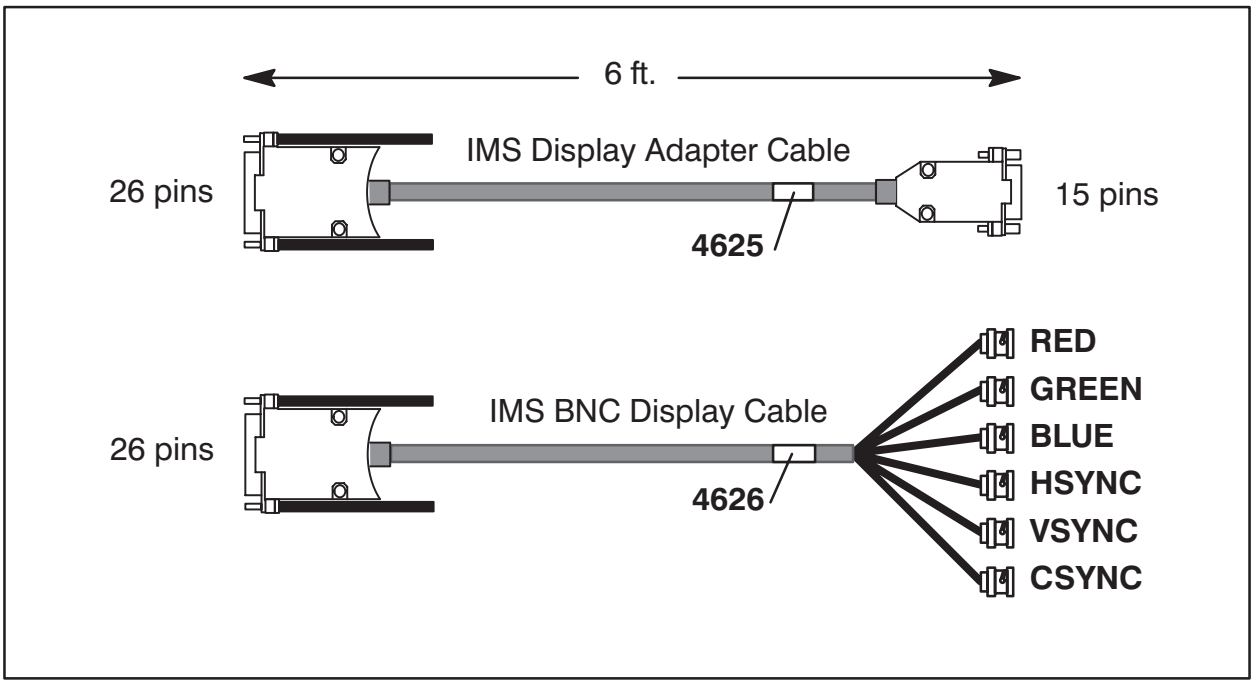


Figure B–1. Display Adapter Cables

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VIDEO INPUT CABLES

Video input cables for the IMS are divided into two catagories: Break–out cables and Adapter cables. The break–out cables connect to the IMS board, and split the 44–pin connector into separate connectors for one, two, or four cameras.The adapter cables connect the break–out cable to a camera.

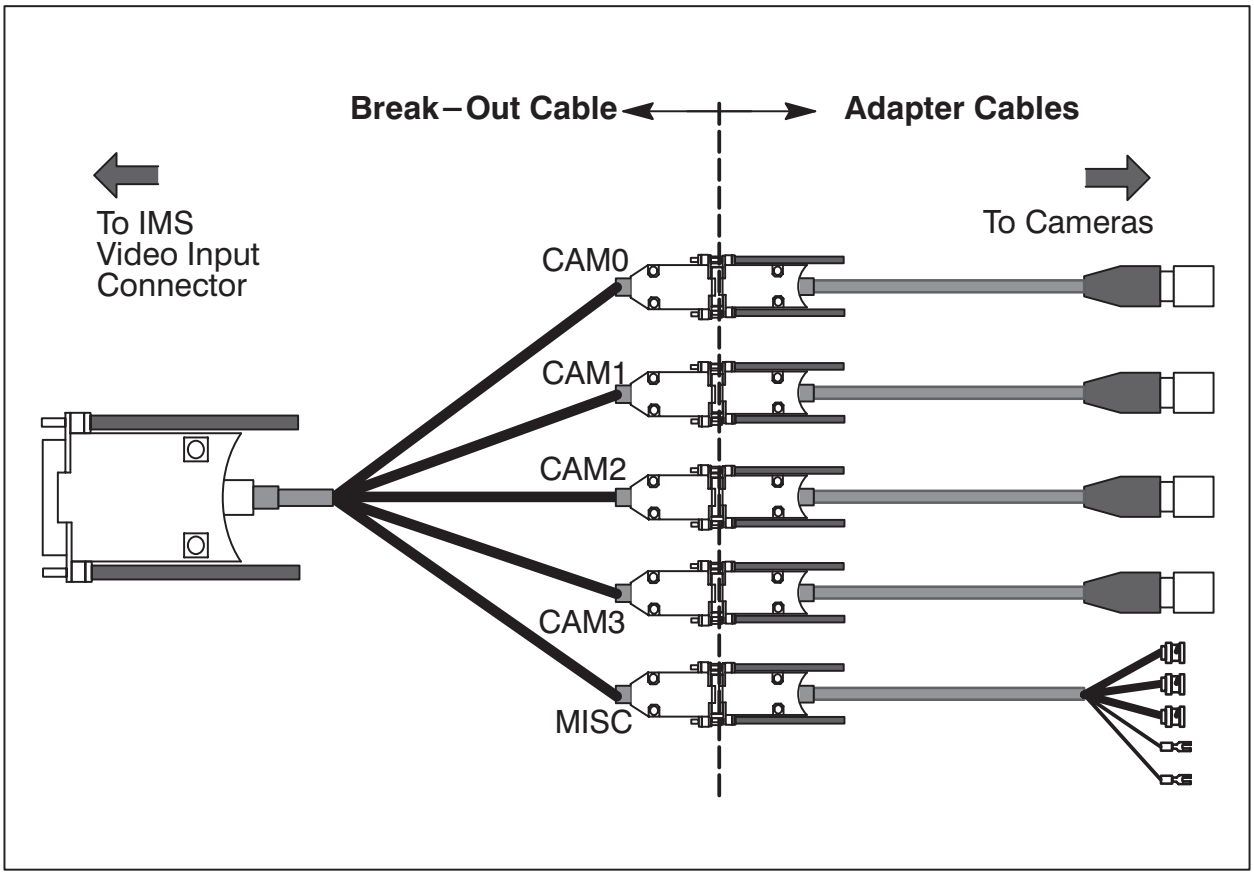


Figure B–2. Video Input Cables

Break–out Cables

Three different break–out cables separate the connections on the 44–pin connector into two, three, or five separate connectors: 15–pin D–Sub connectors for each camera, and a 9–pin D–Sub for miscellaneous connections.

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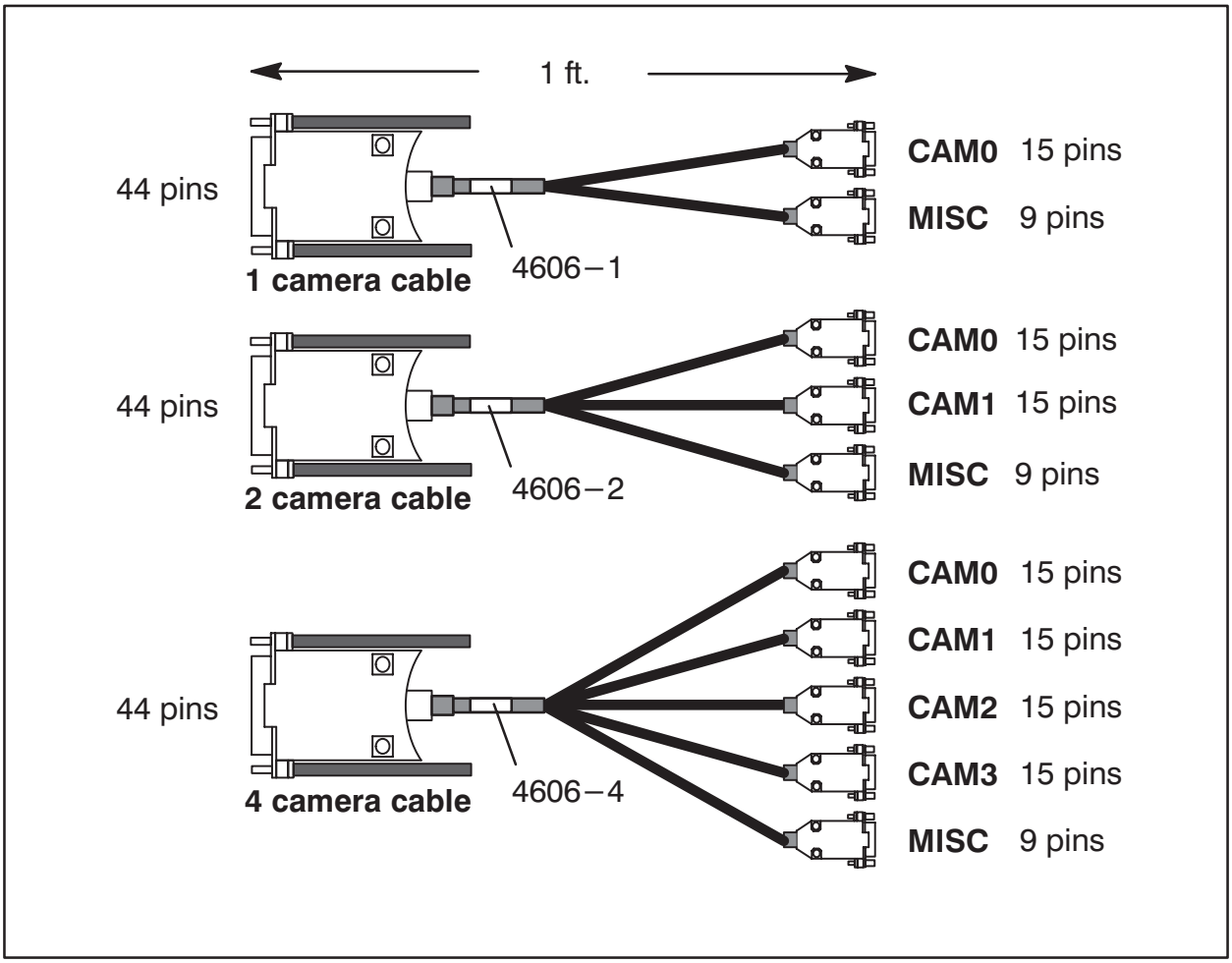


Figure B–3. Break–Out Cable s

Camera Connectors

The specific functions of each camera connector change with each AM. For example; with the AM–VS, CAM0 can be a single–ended or differential analog video input, RS–170, CCIR, or Variable–scan. With the AM–CLR, CAM0 is an RGB RS–170 or CCIR video input. Tables B–1 through B–5 give the general signal pin–outs for the five connectors. Refer to the reference manual for your Acquisition Module for the specific pin–out and function.

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Table B−1. CAM0 Connector

Pin	Signal	Purpose
1	Analog Video−B	Camera 0 Analog Video
2	Analog Video	Camera 0 Analog Video
3	Analog Video−C	Camera 0 Analog Video
4	CLK	Camera 0 Pixel Clock I/O
5	DGND	Camera 0 Digital Gnd
6	Analog Ground−B	Camera 0 Analog Gnd
7	Analog Ground	Camera 0 Analog Gnd
8	Analog Ground−C	Camera 0 Analog Gnd
9	MISC	Camera 0 Misc.
10	+12 Volts GND	Camera 0 +12V return
13	C/HSYNC	Camera 0 C/Hsync I/O
14	VSYNC/VDRIVE	Camera 0 Vdrive I/O
15	+12 Volts	Camera 0 Power

Table B−2. CAM1 Connector

Pin	Signal	Camera Input
1	Analog Video−B	Camera 1 Analog Video
2	Analog Video	Camera 1 Analog Video
3	Analog Video−C	Camera 1 Analog Video
4	CLK	Camera 1 Pixel Clock I/O
5	DGND	Camera 1 Digital GND
6	Analog Ground−B	Camera 1 Analog Gnd
7	Analog Ground	Camera 1 Analog Gnd
8	Analog Ground−C	Camera 1 Analog Gnd
9	MISC	Camera 1 Misc.
10	+12 Volts GND	Camera 1 +12V return
13	C/HSYNC	Camera 1 C/Hsync I/O
14	VSYNC/VDRIVE	Camera 1 Vdrive I/O
15	+12 Volts	Camera 1 Power

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Table B–3. CAM2 Connector

Pin	Signal	Purpose
2	Analog Video	Camera 2 Analog Video
5	DGND	Camera 2 Digital GND
7	Analog Ground	Camera 2 Analog GND
10	+12 Volts GND	Camera 2 +12v Return
13	C/HSYNC	Camera 2 C/Hsync I/O
14	VSYNC/VDRIVE	Camera 2 Vdrive I/O
15	+12 Volts	Camera 2 Power

Table B–4. CAM3 Connector

Pin	Signal	Purpose
2	Analog Video	Camera 3 Analog Video
5	DGND	Camera 3 Digital GND
7	Analog Ground	Camera 3 Analog Gnd
10	+12 Volts GND	Camera 3 +12V return
13	C/HSYNC	Camera 3 C/Hsync I/O
14	VSYNC/VDRIVE	Camera 3 Vdrive I/O
15	+12 Volts	Camera 3 Power

Table B–5. MISC Connector

Pin	Signal	Purpose
1	+12 Volts Input	Camera Power Input
3	MISC 1	Misc.
4	MISC 2	Misc.
5	MISC 3	Misc.
6	+12 Volts GND Input	Camera Power GND input
8	DGND	Misc. Digital Gnd

Adapter Cables

The Misc. Cable plugs into the 9–pin connector on the break–out cables. The other adapter cables plug into the 15–pin D–Sub connectors on the break–out cables, and

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have camera connectors at the other end. Figure B–4 illustrates some of the adapter cables available. **Other adapter cables may be available;** consult your sales office or Imaging Technology.

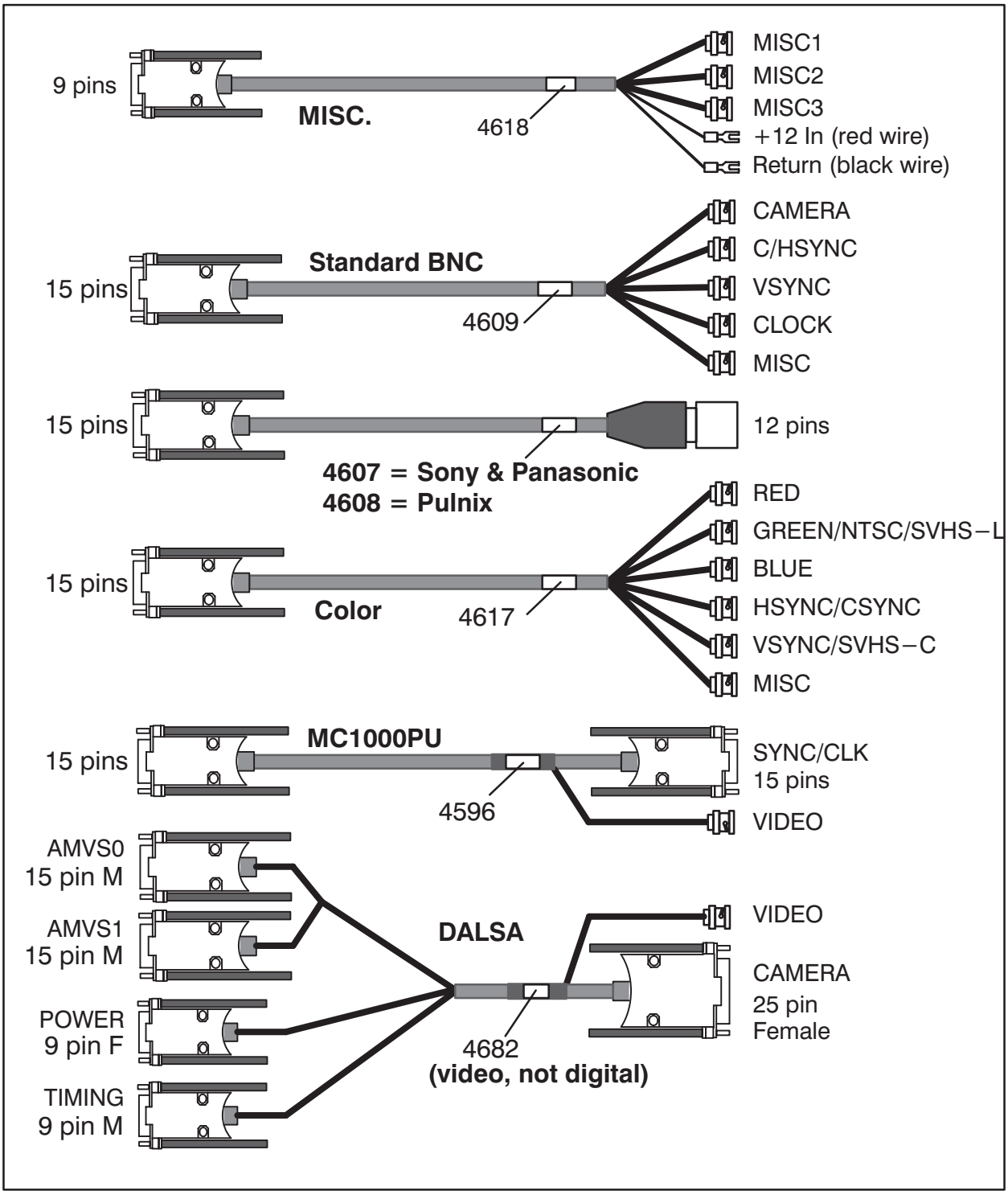


Figure B–4. Camera Adapter Cables

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