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Find the *Molex / Innovative Integration DR PMC* at our website: *Click HERE*

DR PMC/XMC

16-Channel Wide Band Receiver
125 MSPS Sampling
GC5016 Digital Down Converters
Large FPGA for User Code

Features

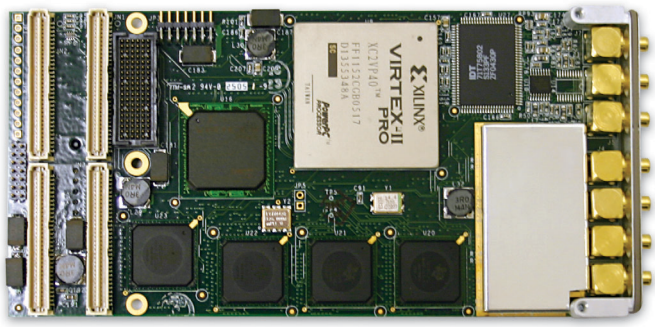
- Four LTC2255, 14-bit, 125 MSPS converters
- Virtex-II Pro FPGA, 4 Million gates
- PCI 64/66 with P4 port to host card
- 64MB SDRAM plus 2MB RAM for FPGA
- Low-jitter PLL clock source
- Advanced SW and firmware demo programs
- XMC - 10 Gbps full duplex

Applications

- Software Defined Radio (SDR)
- Signal Identification
- Electronic Warfare
- Advanced RADAR
- Hardware Testing
- Telecom IP development

Ordering Information

DR PMC Module w/4 GC5016	80123-0
DR PMC Module	80123-1



Overview

The DR Digital Receiver PMC card features 16 receiver channels on one card using the most advanced architecture for ultra-fast signal capture and real-time processing. It integrates the latest analog chips with a 4M Virtex-II Pro FPGA for user-code, ample memory and flexible clocks/triggers on a 64/66 PCI mezzanine format.

High speed digital signal processing algorithms in the FPGA are developed using MATLAB and VHDL code. The FPGA Framework logic allows quick integration of custom signal processing into the data flow of the module through use of component-based modular design. DSP algorithms are rapidly designed using high-level MATLAB simulations that can be integrated into the FPGA hardware with minimal VHDL coding.

Novel features include on-board low jitter PLL clock, Sync Burst RAM dedicated to FPGA for fast, block-oriented processing and a direct PMC J4 DIO connection to the host card. The J4 and XMC interfaces offer a very high-rate, low latency connection to Innovative Integration's Velocia series of DSP and FPGA compact PCI boards and this port protocol can be reconfigured in logic to communicate with third party host cards.

Description

The front-end features four analog input channels consisting of 350 MHz input bandwidth, 50-ohm single-ended input followed by a 125 MSPS, 14-bit Linear Technology LTC2255 A/D converter. The converter clock can be either the highly accurate PLL device ranging from 31MHz to 200MHz with a 3 pico-second RMS jitter, or the user can provide external clocks for conversion or PLL reference.

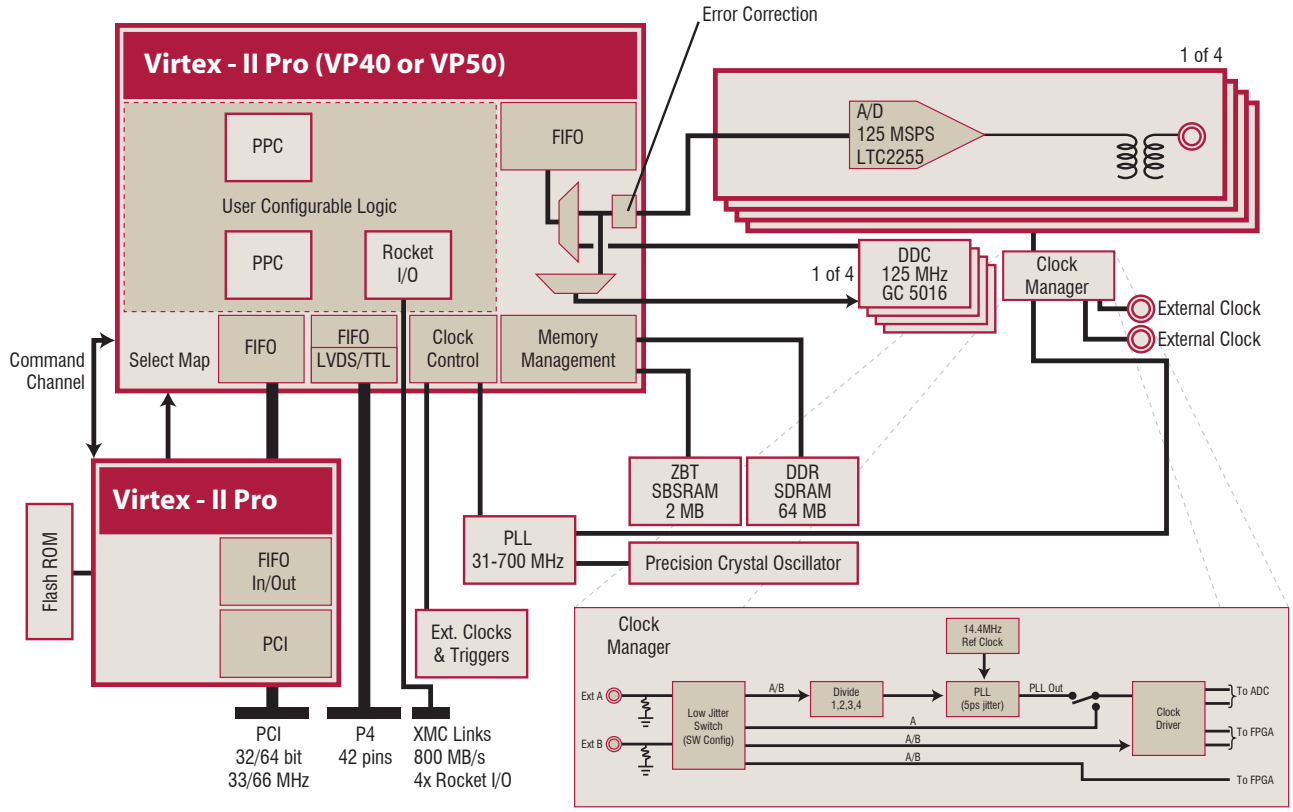
Four TI/GrayChip GC5016 Digital Down Converters have their input and output connected to the user-FPGA. This allows for the most flexible signal path, as each individual signal chain can be defined in logic. The GC5016 is a flexible wideband 4-channel digital up-converter and down-converter. In down-conversion mode, the channel accepts real or complex signals, demodulates them from selected carrier frequencies, decimates them by programmable amounts ranging from 1 to 4096, applies a gain from a user defined automatic gain control, and produces 12 to 20-bit outputs. The frequencies and phase offsets of the four sine/cosine sequence generators can be independently specified, as can the interpolation and filtering of each circuit. Channels can be synchronized to support beam forming or frequency hopped systems. The output from the down-conversion channel is formatted and output in up to four output ports as either real or complex data.

The DR Digital Receiver PMC card shares a common architecture with numerous other VelociaPMC cards including PCI interface, XMC support, clocking and memory.

The "application-FPGA" is a 4-million (XC2VP40) gate device of Xilinx Virtex-II Pro family and is virtually 100% available for user-code. Ample resources allow for flexible integration of the most demanding signal processing blocks such as down/up conversion, complex filtering, resampling, spreading/despreading and signal analysis. For example, the Xilinx DDC logic core for GSM consumes only 1373 slices (< 10K gates) and 1 multiplier.

The application-FPGA controls the I/O, the PLL time base, triggers, 64MB of DDR SDRAM for large data buffering, and a dedicated 2MB SBSRAM. The SDRAM memory is available to the FPGA as a data buffer or for use by the PowerPC processors. The Framework Logic shows an example of using the memory as a very large FIFO for the data channels.
The application FPGA also provides a direct interface to host cards using the PMC J4 or XMC for a private data/control path that can provide a data pipe bandwidth of up to 800MB/s between logic, host and external hardware with Innovative Integration's Velocia DSP and FPGA cPCI boards and other off-the-shelf host cards.

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The application FPGA is tied to the PCI interface chip using 2 Rocket IO links, for a 5 Gbps full duplex maximum data rate. The 64/66 PCI interface supports 528MB/s burst transfers and automatically down-selects to 32 bit and/or 33MHz to permit integration on the widest range of cPCI and PCI carriers. An efficient packet protocol with credit-based flow control allows the PMC to support both high sustained rates of data and a flexible communication path to the host.

Firmware for the application FPGA can be configured dynamically via SelectMap, controlled over the PCI bus with the turnkey utilities with software source code provided.

Software and Logic Framework – Custom Logic Support

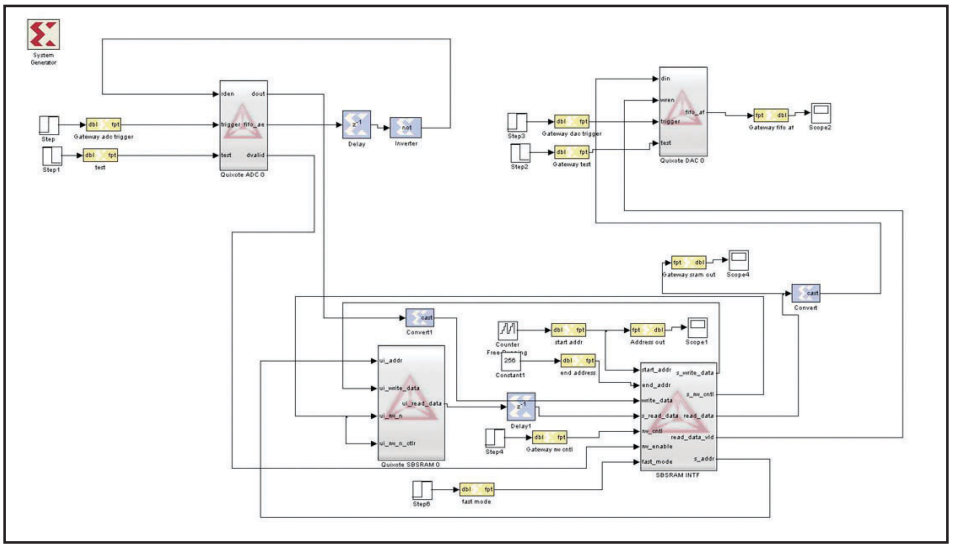
The DR Digital Receiver PMC offers a 4M gate FPGA for custom code implementation. Innovative Integration provides source code of the logic blocks implemented on the card as delivered and demonstrating hardware functionality: Front-end A/D and receiving FIFOs, as well as the DDC converters, PLL time base control, DDR SDRAM control, SBSRAM controller, J4 interface and interface to the PCI-FPGA.

Logic development is supported using either VHDL and/or MATLAB. VHDL source files as well as test bench files for ModelSim are provided to customers. Examples also demonstrate use of Xilinx System Generator for MATLAB into the Framework logic. Control files are also provided for pin use and timing constraints. Development is supported using Xilinx ISE, XST VHDL, with simulation under Mentor Graphics ModelSim.

MATLAB Simulink, in conjunction with Xilinx System Generator may be used for logic development. This powerful graphical tool set allows the signal processing designer to develop algorithms using all the power and grace of MATLAB and then implement them directly in logic. The DR Board Support Package (BSP) provides blocks for the hardware interface ready to use in the Simulink graphical design environment. Gateways to MATLAB allow the developer to quickly test the system by using Simulink to generate, analyze and display the actual data on the hardware during design. Nothing could be easier for advanced signal processing development!

Go directly from MATLAB into the GC5016 using our application software and MATLAB models for the downconversion and filtering design. Once the design is modelled in MATLAB, the design can be put into the GC5016 without any additional coding.

Example MATLAB Simulink applications include data logging to disk, using the SRAM for real-time data collection under MATLAB, and hardware-in-the-loop integration of MATLAB Simulink environment with the UWB PMC. These example



A typical block diagram design using MATLAB

MATLAB Simulink projects are readily modified to add signal processing using the UWB BSP and Xilinx System Generator under MATLAB Simulink.

The PCI-FPGA is not intended for end-user logic development and source code is usually not provided. Contact Innovative Integration if your application might require changes to these specific interfaces.

Software Support

Innovative Integration's software tool kit for the VelociaPMC series is a powerful collection of software libraries, utilities, examples projects and interactive help file that allow developers to be very productive from the start. Numerous program examples - with source code- demonstrate the usage or every peripheral on the board and provide a framework for further custom development.

An application allowing the DR to collect data is provided as an out-of-the-box application for evaluation and as a software example.

OEM Configurations

The DR VelociaPMC board can be configured or modified to fit your specific requirements and provide an optimal mix of performance, cost and features. Contact Innovative Integration with your specific OEM requirements.

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Input

- 4 Independent Analog Input
- 50 Ohm Impedance
- Single-ended
- AC coupled
- 350 MHz input bandwidth
- Range 2.3Vpp
- 14-bit A/D Converter Linear Technology LTC2255
- Sampling Rate: 15-125MSPS (decimation supported for lower rates)
- Digital gain/offset correction in logic

Digital Down-Converters

- 16 channels of digital receiver
- Four Texas Instruments GC5016 chips
- Accepts real or complex signals
- Decimate by 1 to 4096
- User-selectable Gain
- Up to 20-bit output
- Adjustable Freq/Phase Offset on mixer
- Adjustable interpolation and filter
- Supports Channel Synchronization
- Output on 1 to 4 output as real or complex

Time Base and Triggers

- Software selectable timebase:
  - PLL, external input A or B
- PLL using 14.4 MHz precision crystal or external timebase divided by 1,2,4,8, or 16.
- (4) timebases may be used:
  - PLL reference clock range: 10 to 25 MHz
  - (2) external on 50 ohm SMBs
  - PLL capable of 30-700MHz
- Triggering using external input or software (may be modified in custom logic)
- External clock requirements
  - 800 mV p-p minimum, 0.6 to 1.4V
  - maximum input -0.1V to 3.4V
- (2) External clock inputs on 50 Ohm SMB external sync signal

Application-Configurable Logic

- Xilinx Virtex2 Pro XC2VP40
- XC2VP40-5FF1152C (standard, faster speed grades and larger VP50 may be custom ordered.)
- FPGA Fabric :
  - 4 Mgate (approx.)
  - 192 hardware multipliers
  - 3456 Kb embedded FPGA RAM
  - Two PowerPC
  - (4) Rocket IO links using XMC, 10 Gbps full duplex, 2.5 Gbps full duplex each
- SelectMAP loading from PCI bus
- Direct connect to XMC-4 lanes 2Gbps full duplex
- VHDL source code with ModelSim test benches
- JTAG port for download and ChipScope
- J4 connector 42 pins connect to PMC host (RACE++ pinout) to PMC host

PCI-FPGA

- Xilinx Virtex2 Pro VP4
- Supports PCI interface
- Loads from field reprogrammable FLASH memory

Memory

- 16 MB DDR SDRAM (call for larger options)
  - 2 devices configured as 16M x 32 bits, clocked at up to 133 MHz
  - 80 MHz minimum clock rate
- 2 MB ZBT SBSRAM
  - Organized as 1Mx16
  - Clock at up to 167 MHz
- Usable either as FPGA memory or PowerPC memory
- FrameWork Logic provides firmware for DRAM use as FIFO buffer

XMC

- VITA 42.0 compatible
- 4 lanes of Rocket IO
- 2 Gbps per lane standard, full duplex
- Directly attached to application FPGA
- 800 MB/s aggregate rate, full duplex

PCI Interface

- 64-bit, 66 MHz, 3V
- Down-selects to 32 bit and 33MHz if needed
- Packet protocol
- Supports 32 data channels
- 4kB FIFO in each direction

Debug Ports

- JTAG for FPGA:
  - Xilinx standard 14-pin, 2mm header compatible with Xilinx cables
- 38 pin MICTOR compatible with many logic analyzers from application logic

Connectors

- SMB 50ohm for analog I/O, Ext Clocks and Sync

Power

- 10W typical

Operating Conditions

- 10-55 degrees C
- Forced air: minimum 1 cubic ft/min forced air required

Development Languages

- Logic : VHDL with Xilinx ISE, Mentor Graphics ModelSim, MATLAB and System Generator
- VelociaPMC Toolset includes libraries, projects, utilities, help files
- Host PC: MS Visual C++, .NET, Borland C++ Builder,
- Optional DSP: C++ for DSP under TI's Code Composer Studio

Application Software

- Data logging and demonstration application (WinXP/2000)

Physicals

- IEEE 1386 compliant
- Single Width PMC/XMC card
- 74 x 149 mm
- Weight : 0.13kg (0.06 lb)
- 10mm spacing to host card

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