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Innovative Integration

PC32 Hardware Manual

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1. Installation

Installation of a PC32 system involves both hardware and software procedures. This document describes the hardware configuration and installation process. Refer to the associated software supplements for a description of the software installation procedure.

1.1 Host Hardware Requirements

The PC32 is a 16-bit ISA/EISA-compatible expansion card which must be installed into an IBM (or 100% compatible) AT, 386 or 486 machine for proper operation. Rated bus speed for proper is 8.33 MHz.

1.1.1 PC32 Configuration

The PC32 PC board as delivered from Innovative Integration has been configured with the memory and hardware options specified by your order. However, it is sometimes necessary to further configure the PC32 as described below to tailor it to your specific hardware environment.

The factory default settings map the board into the PC's I/O space at address $280, and map the PC32's dual port memory into RAM at address $D000:0000 to $D000:07FF. If the system into which the PC32 is being installed already has devices mapped into these areas, refer to the following pages for directions on how to remap the PC32 to an alternate I/O space and/or RAM region. If these areas are already free on your system, proceed to section 1.3, "PC32 Installation," for instructions on how to install and test the PC32 in your system.

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1.1.2 I/O Configuration

The PC32 must be configured to be addressed within an unused, contiguous, 16-byte I/O region on the host AT. This I/O address should be assigned during the software installation phase by Windows. Select the assigned I/O address from the following table and configure the PC32 to be addressed in that region by setting DIP switch S2 as shown.

I/O Address (hex)	S2 DIP Switch Setting					
	Switch#6	Switch#5	Switch#4	Switch#3	Switch#2	Switch#1
0x100	ON	OFF	ON	ON	ON	ON
0x110	ON	OFF	ON	ON	ON	OFF
0x120	ON	OFF	ON	ON	OFF	ON
0x130	ON	OFF	ON	ON	OFF	OFF
0x140	ON	OFF	ON	OFF	ON	ON
0x150	ON	OFF	ON	OFF	ON	OFF
0x160	ON	OFF	ON	OFF	OFF	ON
0x170	ON	OFF	ON	OFF	OFF	OFF
0x180	ON	OFF	OFF	ON	ON	ON
0x190	ON	OFF	OFF	ON	ON	OFF
0x1A0	ON	OFF	OFF	ON	OFF	ON
0x1B0	ON	OFF	OFF	ON	OFF	OFF
0x1C0	ON	OFF	OFF	OFF	ON	ON
0x1D0	ON	OFF	OFF	OFF	ON	OFF
0x1E0	ON	OFF	OFF	OFF	OFF	ON
0x1F0	ON	OFF	OFF	OFF	OFF	OFF
0x200	OFF	ON	ON	ON	ON	ON
0x210	OFF	ON	ON	ON	ON	OFF
0x220	OFF	ON	ON	ON	OFF	ON
0x230	OFF	ON	ON	ON	OFF	OFF
0x240	OFF	ON	ON	OFF	ON	ON
0x250	OFF	ON	ON	OFF	ON	OFF
0x260	OFF	ON	ON	OFF	OFF	ON
0x270	OFF	ON	ON	OFF	OFF	OFF
0x280	OFF	ON	OFF	ON	ON	ON
0x290	OFF	ON	OFF	ON	ON	OFF
0x2A0	OFF	ON	OFF	ON	OFF	ON
0x2B0	OFF	ON	OFF	ON	OFF	OFF
0x2C0	OFF	ON	OFF	OFF	ON	ON
0x2D0	OFF	ON	OFF	OFF	ON	OFF
0x2E0	OFF	ON	OFF	OFF	OFF	ON
0x2F0	OFF	ON	OFF	OFF	OFF	OFF
0x300	OFF	OFF	ON	ON	ON	ON
0x310	OFF	OFF	ON	ON	ON	OFF
0x320	OFF	OFF	ON	ON	OFF	ON
0x330	OFF	OFF	ON	ON	OFF	OFF
0x340	OFF	OFF	ON	OFF	ON	ON
0x350	OFF	OFF	ON	OFF	ON	OFF
0x360	OFF	OFF	ON	OFF	OFF	ON
0x370	OFF	OFF	ON	OFF	OFF	OFF
0x380	OFF	OFF	OFF	ON	ON	ON
0x390	OFF	OFF	OFF	ON	ON	OFF
0x3A0	OFF	OFF	OFF	ON	OFF	ON
0x3B0	OFF	OFF	OFF	ON	OFF	OFF
0x3C0	OFF	OFF	OFF	OFF	ON	ON
0x3D0	OFF	OFF	OFF	OFF	ON	OFF
0x3E0	OFF	OFF	OFF	OFF	OFF	ON
0x3F0	OFF	OFF	OFF	OFF	OFF	OFF

Figure 1: I/O Address selection DIP switch settings

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1.1.3 Dual Port RAM Configuration

PC32 boards are equipped with dual port memory and must be configured to map the dual port ram into an unused region of the Host AT memory map. The I/O address is assigned by Windows during software installation. Select the assigned memory address from the following table and configure the dual port memory to be addressed in that region by setting DIP switch S1 as shown.

Dual Port Memory Address (hex)	S1 DIP Switch Setting							
	Switch#8	Switch#7	Switch#6	Switch#5	Switch#4	Switch#3	Switch#2	Switch#1
0xC8000	OFF	OFF	ON	ON	OFF	ON	ON	ON
0xC9000	OFF	OFF	ON	ON	OFF	ON	ON	OFF
0xCA000	OFF	OFF	ON	ON	OFF	ON	OFF	ON
0xCB000	OFF	OFF	ON	ON	OFF	ON	OFF	OFF
0xCC000	OFF	OFF	ON	ON	OFF	OFF	ON	ON
0xCD000	OFF	OFF	ON	ON	OFF	OFF	ON	OFF
0xCE000	OFF	OFF	ON	ON	OFF	OFF	OFF	ON
0xCF000	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
0xD0000	OFF	OFF	ON	OFF	ON	ON	ON	ON
0xD1000	OFF	OFF	ON	OFF	ON	ON	ON	OFF
0xD2000	OFF	OFF	ON	OFF	ON	ON	OFF	ON
0xD3000	OFF	OFF	ON	OFF	ON	ON	OFF	OFF
0xD4000	OFF	OFF	ON	OFF	ON	OFF	ON	ON
0xD5000	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
0xD6000	OFF	OFF	ON	OFF	ON	OFF	OFF	ON
0xD7000	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF
0xD8000	OFF	OFF	ON	OFF	OFF	ON	ON	ON
0xD9000	OFF	OFF	ON	OFF	OFF	ON	ON	OFF
0xDA000	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
0xDB000	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF
0xDC000	OFF	OFF	ON	OFF	OFF	OFF	ON	ON
0xDD000	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
0xDE000	OFF	OFF	ON	OFF	OFF	OFF	OFF	ON
0xDF000	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF
0xE0000	OFF	OFF	OFF	ON	ON	ON	ON	ON
0xE1000	OFF	OFF	OFF	ON	ON	ON	ON	OFF
0xE2000	OFF	OFF	OFF	ON	ON	ON	OFF	ON
0xE3000	OFF	OFF	OFF	ON	ON	ON	OFF	OFF
0xE4000	OFF	OFF	OFF	ON	ON	OFF	ON	ON
0xE5000	OFF	OFF	OFF	ON	ON	OFF	ON	OFF
0xE6000	OFF	OFF	OFF	ON	ON	OFF	OFF	ON
0xE7000	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF
0xE8000	OFF	OFF	OFF	ON	OFF	ON	ON	ON

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0xE9000	OFF	OFF	OFF	ON	OFF	ON	ON	OFF
0xEA000	OFF	OFF	OFF	ON	OFF	ON	OFF	ON
0xEB000	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF
0xEC000	OFF	OFF	OFF	ON	OFF	OFF	ON	ON
0xED000	OFF	OFF	OFF	ON	OFF	OFF	ON	OFF
0xEE000	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
0xEF000	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF

Figure 2: Host dual port address DIP switch settings

NOTE: The dual port memory on the PC32 is *disabled* by onboard decoding circuitry whenever the PC is reset or is power-cycled. This feature minimizes the possibility of conflict between other memory-mapped peripheral devices or memory managers and the PC32 dual port memory during PC boot-up. Bit 1 in the PC32 control register must be set low before dual port memory will become active. The PC32 DLL automatically perform this function when the monitor function `DUAL-PORT` is executed as part of the normal start-up behavior of any of the Development System Applets.

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1.1.4 Interrupt Configuration

The PC32 may be configured to interrupt the AT host whenever the PC32 writes data into the hosts communications mailbox. (Note that the terminal emulator provided with the *Development System* is not interrupt-driven). If your application requires PC interrupts, select an unused hardware interrupt from the following table and configure the PC32 to use that interrupt by setting header JP7 as shown. Be sure to use the interrupt number assigned to the PC32 by Windows during the software installation.

Interrupt #	JP7 Setting	Possible Conflict
5	1-2	LPT2:
7	3-4	LPT1:
11	5-6	Network adapter
15	7-8	

Figure 3: PC32 host interrupt jumper settings

Although interrupts 5 and 7 are listed as potentially used by LPT1: and LPT2:, printers rarely implement interrupt driven output in practice. These interrupts are available in many instances.

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1.2 PC32 Installation

Note: *The PC32 employs electronic components which are sensitive to electrostatic discharge. Employ proper electronics handling techniques when installing the PC32 in your IBM-AT.*

Turn off the host IBM computer. Remove the (usually five) screws which secure the cover of the CPU system unit then remove the cover to allow access to the bus expansion slots in the AT.

Isolate an empty 16-bit slot on your motherboard. Remove and store the dummy retainer bracket associated with that slot. Plug the PC32 into the empty 16-bit slot. Be sure to properly seat the PC32 into the card edge connector into the motherboard. Insure that the PC32 is not inadvertently contacting another PC board in an adjacent slot. Use the retainer bracket screw which held the dummy bracket in place to secure the PC32's retainer bracket to the PC chassis.

Install the cover of the CPU system unit and secure it using the cover screws removed earlier.

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1.3 Testing the PC32

Reboot your PC and invoke the terminal emulator from the PC32 program group. Use the File | COFF Download function to download and run the HELLO.OUT file. If the installation was successful, the PC32 should run the classic hello world example program and display output in the terminal console window.

If you experience difficulties:

1. Check that the PC32 is properly configured and that there are no devices bus-contending with it at the configured addresses.
2. Verify that the PC32 card edge connector is clean. A standard pencil eraser can be used to clean dirty card edge connector contacts, if necessary.
3. Reseat the board in its slot.
4. Rerun the test program. If problems persist, call Innovative Integration technical support.

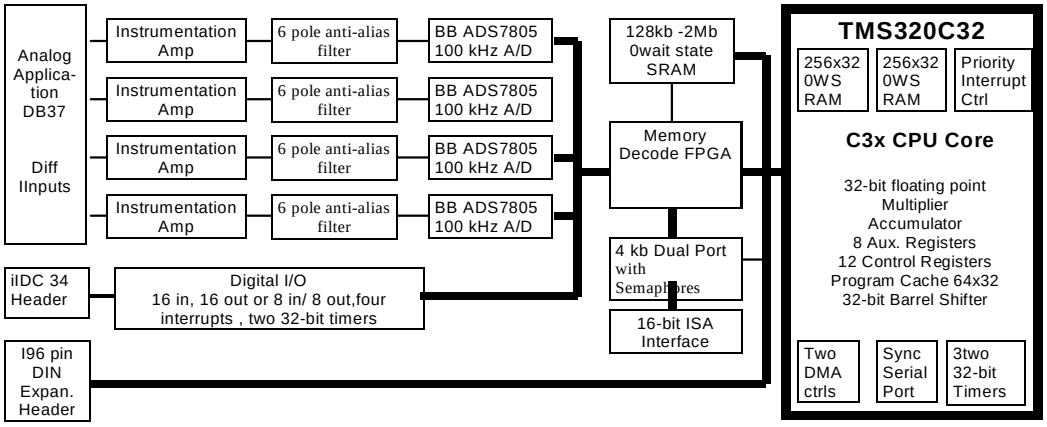
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2. PC32 Hardware Functions

2.1 PC32 Hardware

The PC32 is a complete DSP system on a single half-length ISA bus card. The PC32 offers a very high performance computing engine with determinant timing for fast data acquisition and control to complement the PC. Applications for the card include data acquisition and analysis, intelligent digital control systems, acoustic processing, and coprocessing for the PC. Using the PC32, the PC is freed up from time-critical events and can operate under Windows and other operating systems where real-time performance is an afterthought.

Figure 4: PC32 block diagram.



2.2 PC32 Bus Interface

The TMS320C32 is a 32-bit digital signal processor supporting a 24-bit address bus and 32-bit data paths. The PC32 has been designed as a device which is mapped into the I/O and memory spaces of the IBM AT. Note that the AT bus supports 8 and 16-bit and 32-bit, I/O and memory accesses (32-bit access in protected mode only).

The purpose of the PC32 bus interface is to provide a mechanism for convenient access to all PC32 peripherals and memory resources via the 'C32 processor from the PC-AT and to provide control of the card operation.

When the PC32 is mapped into the I/O space of the IBM-AT, it consumes 16 contiguous bytes located on an even 16-byte boundary within the I/O map. Within this I/O region lie seven, 16-bit registers which are used to communicate with the PC32. The I/O register map is described in the following table. References to *BASE* below refer to the I/O address into which you mapped the PC32 in your system during installation (default 0x280).

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I/O Address	Direction	Function
Control Register		
Base + 0	Write	Latch 16-bit bus control register. Bit 0: PC32 reset, active high. Bit 1: Dual port enable, active low.
	Read	Unsupported. Latch is write only.
Host Interrupt 0 Register		
Base + 2	Write	Send interrupt signal to JP17 pin 2. The PC32 may be configured via JP17 to allow this interrupt to propagate to EI3 or EI1.
	Read	Same as Write to this address.
Host Interrupt 1 Register		
Base + 4	Write	Send interrupt signal to JP17 pin 11. The PC32 may be configured via JP17 to allow this interrupt to propagate to EI3 or EI2.
	Read	Same as Write to this address.
Semaphore 0 Register		
Base + 6	Write	Setting bit zero in this register requests ownership of general-purpose hardware semaphore 0. Resetting bit zero relinquishes ownership of semaphore 0.
	Read	If bit zero is set, PC has obtained ownership of semaphore 0. Otherwise, semaphore 0 is uncommitted.
Semaphore 1 Register		
Base + 8	Write	Setting bit zero in this register requests ownership of general-purpose hardware semaphore 1. Resetting bit zero relinquishes ownership of semaphore 1.
	Read	If bit zero is set, PC has obtained ownership of semaphore 1. Otherwise, semaphore 1 is uncommitted.
Semaphore 2 Register		
Base + 10	Write	Setting bit zero in this register requests ownership of general-purpose hardware semaphore 2. Resetting bit zero relinquishes ownership of semaphore 2.
	Read	If bit zero is set, PC has obtained ownership of semaphore 2. Otherwise, semaphore 2 is uncommitted.
Semaphore 3 Register		
Base + 12	Write	Setting bit zero in this register requests ownership of general-purpose hardware semaphore 3. Resetting bit zero relinquishes ownership of semaphore 3.
	Read	If bit zero is set, PC has obtained ownership of semaphore 3. Otherwise, semaphore 3 is uncommitted.

Figure 5: PC32 I/O port register functions

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16-bit PC bus cycles to any of the above registers take three PC bus cycles (375 nS) to execute. Notably, there are no wait states imposed on dual-port accesses from either the Host PC or the ‘C32.

Note that this bus arrangement does not allow the host PC to *directly* access any of the memory-mapped resources on the PC32. This would appear to indicate that the PC32's digital I/O parallel port, analog I/O, etc. and all onboard RAM memory cannot be accessed by the host PC. However, by using software tools such as the *Talker* provided in the PC32 Development Package, all peripherals and memory addressable by the 'C32 microprocessor may be *indirectly* accessed by the PC via dual-port memory.

2.2.1 Data Transfers via Dual Port and a Talker

To transfer data to or from PC32 memory, software must be running on the PC32 which causes the data transfer through dual port SRAM to or from ‘C32 memory. This piece of code is known as a software monitor or *talker*.

There are many possible implementations of talker programs, supporting a wide variety of application requirements. In general, talkers are small, command driven assembly language programs residing in target memory which implement a means of writing to target memory, reading from target memory and launching application code at a specified address.

One of the main functions of the talker is to download application programs to the PC32 and begin execution. To download application programs, you must first enable the dual port memory usage by the PC while holding the PC32 in reset. This is accomplished by writing a 0x1 to the control register at Base + 0x0. Then the talker may be placed into the dual port to boot the PC32. The talker must be placed starting at address zero of the dual port (0x1000 to the PC32). Once the talker has been written into dual port, the PC32 is released from reset by writing a 0x0 to the control register.

At this point, the talker should be running and will allow downloading of the application program to the main memory of the PC32 for execution. The talker by Innovative allows simple passing of data into memory by using a mailbox structure and semaphores to coordinate the data transfers. The application program is typically a COFF or TOFF file from the C compiler which is then downloaded to the ‘C32 memory for execution. See the PC32 Software supplement for more details.

2.2.2 Hardware Semaphores

In many PC32 applications, there are resources which both the ‘C32 and the PC need to share. An example of such a resource is dual port memory. A common problem with sharing a resource is that it is difficult to keep track of which processor is currently using the device. It is usually imperative for each processor in a multiprocessor system to know when it can access the shared resource without risk of corrupting the data in the resource.

The PC32 dual port has four semaphores which may be used by software to control the data flow through the dual port memory. The semaphores assist software by providing an arbitration method when accessing the dual port memory. Software can pass access control over regions of the dual port memory by passing ownership of one of the semaphores such that bi-directional communications are always handshaken between the two processors. Also, semaphore driven dual port accesses are typically faster since no hardware arbitration contests will occur between the processors for each dual port memory access. This method is particularly useful for block transfers, since one side can prepare a block to be transferred by

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filling a section of dual port with data completely unhindered by the byte-by-byte arbitration contests typical of a hardware arbitration system. Once the buffer is filled, the originating side relinquishes dual port access to the receiver, which then empties the dual port contents (again unhindered by arbitration contests). Before using the shared resource, an application program posts a request for "ownership" of the resource by setting bit zero in a semaphore register (BASE + 6 through BASE + 0C). The program must then poll bit zero of the semaphore control register until it is set. When bit zero becomes set, the program can continue and use the resource as desired. When use of the resource is complete, the resource should be relinquished so that the other processor can have an opportunity to use the resource if needed. This is accomplished by writing clearing bit zero in the semaphore control register. Please note that dual port semaphore accesses only return results on the lower 16 bits of the 32 bit location: the upper 16 bits of any semaphore read by either processor should be masked.

In order for this mechanism to work, the application programs running on both the IBM PC and the PC32 must be coded with an agreed upon convention as to the meaning of each of the hardware semaphores. For example, semaphore 2 could be used to arbitrate accesses to dual port memory region 0x00-0xff and semaphore 3 could be used to arbitrate accesses to dual port memory region 0x100-0x300. Under this "agreement", the PC and the 'C32 must each perform the semaphore acquisition sequence above prior to accessing either of these dual port memory regions. Once arbitration is complete, the owner may randomly accesses the memory region as needed (with no wait-states).

The dual port semaphores reside at 0x81b000 - 0x81c800 on the 'C32 side. These semaphores are fully arbitrated with the PC side semaphores so that only one processor may own the semaphore at any time.

The handshaking steps in using the semaphores are as follows :

1. A processor attempts to write a 0 to the semaphore.
2. A read is performed by the processor and if a 0xXXXX0000 is returned, the semaphore was successfully seized. If a 0xXXXXFFFF is returned the resource is busy.
3. Relinquish the semaphore by writing a 1 to the semaphore when the dual port is no longer needed.

The dual port semaphores are fully arbitrated by the on-chip hardware. Access to the semaphores is always first-come, first-served. Truly simultaneous accesses by both busses will result in an arbitrary winner. Note that failed requests for a semaphore are latched by the semaphore control logic. This means that the request will eventually be granted when the owner relinquishes control of the semaphore. The following example illustrates this behavior:

1. 'C32 requests semaphore #0 and it is granted.
2. Some time later, PC host software requests semaphore #0 and is denied access since the 'C32 already owns the bit.
3. Some time later, the 'C32 releases semaphore #0, and since the PC host never released the original request, the semaphore is immediately granted to the host. If the host software has not been dwelling on the semaphore, it is possible that it is not expecting access to be granted and so may not release the semaphore. For this execution session, the semaphore has been effectively lost since the host software does not release it and the 'C32 can no longer gain access.

This example illustrates that it is good form to release a failed request for a semaphore if the software intends to proceed to other tasks. Doing so avoids the possible deadlock which might result from a granted semaphore which is never released

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2.2.3 PC32 Memory

Memory addresses generated by the 'C32 microprocessor are twenty-four bits wide resulting in 16 MWord total address range.

The PC32 directly supports up to 512 kWords of onboard zero-wait-state “program” SRAM (Static Random Access Memory). Additionally, up to 256 kWords of onboard one-wait-state “data” memory is supported. The PC32 also supports a 1k x 32-bit dual port memory block which may be accessed non-simultaneously by either the PC32 or the IBM PC.

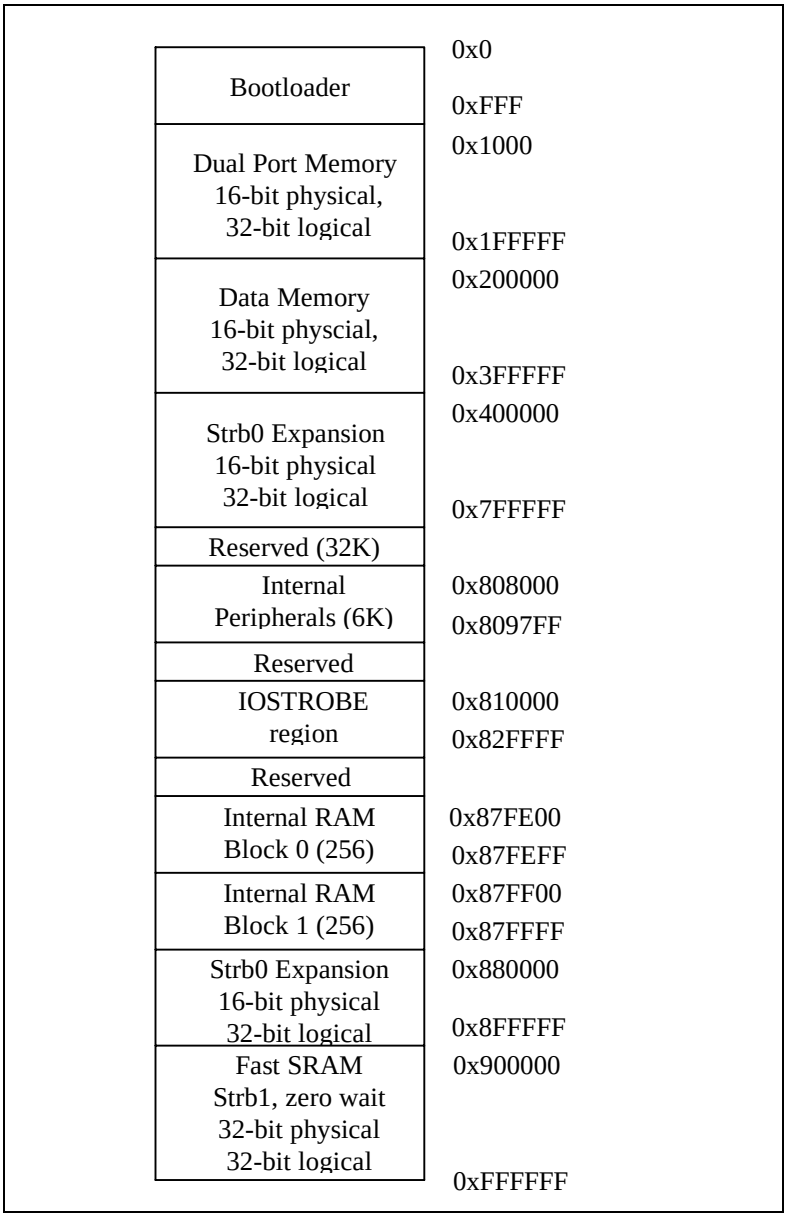


Figure 6: PC32 Memory Map

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From the programmer's perspective, program and data memory and dual port are all addressed as 32-bit words. Physically, only program memory (in the strobe 1 memory region) is truly 32-bits wide; data memory and dual port memory are 16-bit devices mapped into the 'C32 strobe 0 region which require two consecutive bus cycles to perform 32-bit transactions. Further, accesses to the strobe zero region require one wait-state for proper operation. Thus, accesses to the strobe 0 memory region require four processor clocks while accesses to the strobe one region require only a single processor clock..

Each of the three memory regions, strobe zero and one, and the I/O memory region feature independent software-configurable wait states. The talker, provided with the II developers kit for the PC32, initializes each of these registers for proper operation of the board in the default configuration: zero wait states for strobe 1, one wait-state for strobe 0 and one wait state for I/O. However, the PC32 may be optionally be configured with slow SRAM in both the strobe zero and one regions if desired to reduce code in volume applications.

Use of the internal 'C32 cache allows slower memories to perform nearly as well as fast, zero wait state memories in some cases. If the application can be structured to run entirely on-chip and make use of the in the 'C32 cache, performance will be optimal. Most applications benefit substantially from the cache so that one wait state memories do not run at half the rate of zero wait state memories. However, cache use usually renders program timing less deterministic.

Memory expansion beyond the capability of the onboard 756 kWords can be supported by a custom daughter card. Contact Innovative Integration for details.

2.2.4 Wait States

The TMS320C32 features three very flexible, programmable wait-state generators onchip (Chapter 7 of the *TMS320C32 Users Guide*). These wait-state generators are programmed in the default configuration to abbreviate the programmed number of software wait-states through use of offboard 'C32 READY* signal, if implemented by auxiliary hardware.

Memory Region	Recommended Wait States
STRB 0	1
STRB 1	0
IOSTROBE	1

Figure 7: Wait States

2.2.5 Memory Options

The PC32 supports up to 512 kWords of program SRAM plus another 256 kWords of data SRAM on the board without additional off-board hardware. The standard memory configuration shipped is 32 KWords of zero wait state program memory in surface mount packages, with each memory device containing 32k bytes. Other memories may be installed onto the board at the factory to expand the memory provided they follow the JEDEC standard pinout for memories. This allows for easy memory expansion with larger denomination memories. Additionally, cost sensitive applications may work with memories as small as 8k bytes. The two sizes of surface mount packages are supported by the triple row JEDEC footprints are 300

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mil wide, 28 pin SOJ and 400 mil wide 32 pin SOJ. An additional memory footprint on the solder side of the card supports the zero wait state 512Kx8 memory chips with center power and ground pins. Use of the 512Kx8 footprints is exclusive of the triple row JEDEC footprints. Users may purchase memories from Innovative Integration at any time either as original equipment or as upgrades.

The STRB 0 memory region may be populated with either two 128Kx8, 1 wait state memoriesor tw 512Kx8, 1 wait state SRAMS. When reconfiguring data (strobe 0) memory, modify jumper JP19 as follows:

JP19	Function
1-2	64 kW data SRAM installed.
2-3	256 kW data SRAM installed.

Figure 8: Onboard data SRAM size selection jumper

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2.2.6 Dual Port Memory

The PC32 is configured with one IDT 7133 2k x 16-bit dual port memory device to address the most demanding data communications requirements. The dual port is addressable by the PC32 as a contiguous 0x0400 x 32-bit memory block at address 0x1000. The dual port is addressed from the IBM-PC side at the conventional memory address specified via DIP switch S2 (default D000:0000).

Inter-processor data transfers via the dual port RAM yield much higher performance than what is achievable using a conventional PC I/O bus interface. The reason for this is that PC memory bus cycles are shorter and faster than I/O bus cycles (one PC bus cycle versus three bus cycles). Dual port accesses are one-wait-state from the 'C32; Dual port accesses are not wait-stated from the PC.

Like the data memory bank, dual port memory is mapped into the strobe 0 memory region. Thus accesses to dual port require four 'C32 processor clocks to complete - one wait state for both 16-bit accesses.

2.2.6.1 32-Bit-Wide Dual Port

The dual-port implementation on the PC32 takes advantage of the dynamic bus sizing capability of the 'C32 processor to transparently synthesize 32-bit accesses to the 16-bit dual-port RAM on the board. This mechanism is superior to systems configured with simple 16-bit dual-port for several reasons. First, 32-bit addressable dual port eliminates the need to "slice and dice" 32-bit integer of floating point data prior to transferring between processors. Secondly, 8, 16 or 32-bit data can be moved between peripherals or core SRAM and the dual port using the DMA controller on 32-bit dual port PC32 systems.

In summary:

1. Dual port is mapped at 'C32 address 0x001000 on strobe 0.
2. C32 accesses to dual port memory are four-cycle, one-wait-state. PC accesses to dual port are not wait stated. This means that, except from possible overhead associated with arbitrating for use of dual port via the semaphore or mailboxes, data may be transferred through dual port at the maximum rate supported by the ISA bus in your PC. Typically, this is from 2.5 to 3.5 Mbytes/second.
3. Accesses to dual port memory ***are not*** arbitrated in hardware. This means that simultaneous access by *both processors* to the *same memory cell* will be unreliable (all other types of access are OK). If this is an issue in your application program, each processor must arbitrate for use of the dual port using either interrupts or the hardware mailboxes described above. Effective use of interrupts can often eliminate dual-port arbitration altogether.

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2.3 Memory Mapped Peripherals

All PC32 peripherals are memory mapped. The peripheral region is defined as the memory region from 0x810000-0x820000 which is the IOSTROBE region of memory. In this memory region the IOSTROBE signal from the ‘C32 is active.

The peripheral region of memory is decoded on the PC32 to simplify prototyping peripheral boards. Each of the onboard PC32 peripherals is directly addressable within the peripheral region and consumes 0x800 for each peripheral block.

The access cycle length within the I/O peripheral region is controlled by the number of software wait states defined by the WTCNT bits in the I/O Bus Control Register at address 0x806060 Default at reset is seven wait states, but the talker modifies this during startup initialization code within application programs to the appropriate number and physical description. The recommended number of wait states in the IOSTROBE region of memory is one. Access cycles can be abbreviated by asserting the external READY signal during the access cycle provided the wait state control register has been modified to monitor the external signal.

If you are attempting to map a non-zero wait state device into PC32 memory, you must map it into either the strobe zero region or the I/O region. Due to the high speed of the memory required for the ‘C32 DSP, it is not possible to successfully map offboard zero wait-state devices into the strobe 1 memory region. Also, be advised that control of the READY pin in strobe 1 can be difficult. Devices which have a non-determinant wait state requirement, or a mixture of devices with assorted wait state requirements, would usually use STRB0 to reset the wait state counter in external logic between accesses. This will not work because STRB0 will not go inactive for consecutive reads mixed with internal memory cycles which will confuse the external wait state counter. The best option for these devices is to map them to the IOSTROBE region where IOSTROBE is designed to go inactive on internal accesses or use the internal wait state counter ONLY.

Two decoded 0x800 location regions of the IOSTROBE space are provided for custom peripheral interfaces on daughter cards referred to as DECODES 0 and DECODES 1. These two application memory regions are physically and logically 16 bits wide and will be wait stated according the setting of the IOSTROBE wait state control register (normally 1). The number of wait states would typically be 1 wait states on the standard PC32.

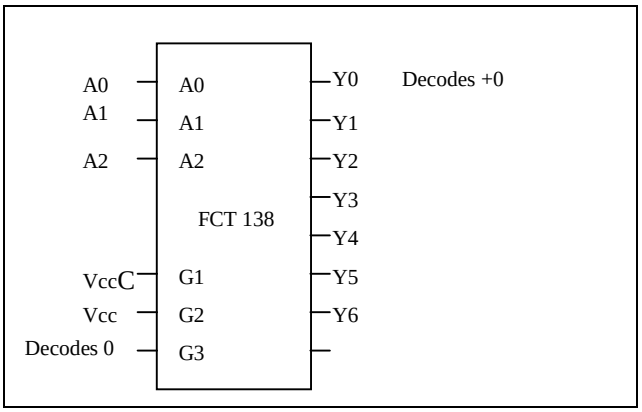


Figure 9: Sample peripheral decoding circuit.

Consult with Innovative Integration for more information on custom device interfacing.

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The following table gives the complete IOSTROBE memory region map, showing the addressing of IOSTROBE mapped peripherals on the PC32.

Address (hex)	Device
810000	ADC 0
810800	ADC 1
811000	ADC 2
811800	ADC 3
812000	PC REFRESH indicator bit used for time interval reference
812800... 813FFF	Reserved
814000	DAC 0
814800	DAC 1
815000	DAC 2
815800	DAC 3
816000	Update DAC 0 output voltage
816800	Update DAC 1 output voltage
817000	Update DAC 2 output voltage
817800	Update DAC 3 output voltage
818000	Digital I/O
818800	Boot Indication Override to PC
819000	Interrupt to PC
819800	Reserved
819800	Decodes 0
81a000	Decodes 1
81b000	Dual port semaphore #0
81b800	Dual port semaphore #1
81c000	Dual port semaphore #2
81c800	Dual port semaphore #3

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Address	Device
808000	DMA Global Control
808004	DMA Source Address
808006	DMA Dest Address
808008	DMA Count
808010	DMA Global Control
808014	DMA Source Address
808016	DMA Dest Address
808018	DMA Count
808020	Timer 0 Global Control
808024	Timer 0 Period
808028	Timer 0 Counter
808030	Timer 1 Global Control
808034	Timer 1 Period
808038	Timer 1 Counter
808040	Serial port Global Control
808042	Serial XMT sync control
808043	Serial RCV sync control
808044	Serial XCV control
808045	Serial XCV clock counter
808046	Serial XCV period register
808048	Serial XMT data
80804c	Serial RCV data
808060	IO bus control register
808064	Strobe 0 bus control register
808064	Strobe 1 bus control register

Figure 10: PC32 peripheral memory map.

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2.3.1 The DIGITAL Parallel I/O Ports

The PC32 has a 16-bit digital I/O port which can be configured as 16 outputs with readback, 16 inputs, or a mixture of 8 inputs/8 outputs. The port is TTL compatible and capable of speeds up to 15 MHz input or output for custom interfaces. The outputs are capable of 64 mA sink and 48 mA drive, making them capable of directly driving LEDs and Opto-isolators. The inputs can be used as general purpose inputs to the 'C32 to sense relay closure, external TTL events, buttons etc.

Inputs to the digital port should be TTL compatible, and readback clock pulses should be at least 3 nS wide, with data set up at least 2.5 nS ahead of the leading edge of the clock pulse (see IDT74FCT16952 transceiver data sheet for complete timings).

Outputs are capable of sourcing 48 mA and sinking 64 mA. This allows the outputs to directly drive LEDs with current limiting resistors and opto-isolator modules.

Two jumper blocks configure the digital I/O bits. Jumper JP13 describes the I/O port configuration as inputs or outputs, and jumper JP14 provides readback on output bits if desired.

Digital Bits	Jumper JP14		Jumper JP13	
	Readback enable	External digital clock	Output	Input
DX0..7	1-2	none	1-3	none
DX6..15	1-2	none	2-4	none

Figure 11: Digital I/O Configuration Jumpers

Readback on output bits is not possible if using an external clock.

Digital readback is the state of the digital I/O pins at the inception of the DSP cycle in which they were read.

IMPORTANT NOTE

Please note that two reads of the digital I/O port are required to latch and recover current input values. The first read serves to latch the data on the I/O port pins, while the second read recovers the data from the port. This applies only to pins setup for input: latched output data may be readback at any time.

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2.3.2 Analog I/O

The analog input section features four channels of 16-bit, 100 or 200 kHz input which are configured with high input impedance instrumentation amplifiers to permit direct connection to sensors and signal sources. The A/D channels are instrumentation grade and have full calibration capability for accurate DC results. Input range is normally +10V to -10V , but may adjusted as required with a simple resistor change.

2.3.2.1 Analog to Digital Converter

The analog to digital converters (U18, U10, U15, U16) are 16-bit devices with a 10 us conversion time (Burr-Brown ADS7805) capable of digitizing CD quality music, sensor outputs like thermocouples and accelerometers, and other demanding acquisition applications. Each A/D channel is an independent conversion path with independent filltering and gain. The default bipolar input range is +/- 10V. Custom input ranges may be achieved as described below.

The ADS7805 A/D converter is internally sampled prior to conversion and requires no external sample and hold circuitry. The ADC is self-timed and will typically convert in less than 10 us, which is the specified maximum conversion time for all conditions. The ADC also has its own internal precision voltage reference for accurate conversions. Do not use the reference output for any other device unless proper signal buffering is provided as this may adversely affect conversion accuracy.

The ADS7805 ADCs are memory mapped read-only peripherals in the C32 IOSTROBE space. A/D samples are read directly from the associated memory address as a 16-bit number. The device may be read by a CPU read or by the DMA controllers.

A/D Channel	Device Designator	Memory Address
0	U8	0x810000
1	U10	0x810800
2	U15	0x811000
3	U16	0x811800

Figure 12: A/D Memory Mapping

Note that on PC32 boards depopulated to just two analog channels, only A/D channels zero and two are available.

The A/D converters may be triggered for conversion by writes to the memory-mapped A/D, externally triggered by a TTL signal, or clocked by one of the two timers in the DSP. For the memory mapped conversion trigger, use a write to the A/D address. Only a write to the memory-mapped address will cause a conversion; reads are used for reading back the data. Generally, it is preferred to trigger the conversion using a timer as this will result in the least jitter and timing ambiguity. This is especially important for audio applications where this is a source of distortion and degrades AC performance. For servo applications, the memory mapped access may be more useful where timing may be less critical.

The triggers source selection for the A/D converters is done using JP5 and JP6. This selection is logically ORed with the memory-mapped address for DSP writes internally in the control logic FPGA. This allows timer driven conversions to be intermixed with memory-mapped triggered conversions if necessary. These jumpers select the trigger sources for A/D pairs, i.e. JP5 selects the trigger source for A/D 0 and 1 (U8 and

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U10 and JP6 selects the trigger source for A/D 2 and 3 (U15 and U16). The A/Ds are separate devices, only the triggers source is common.

External triggering is selected by connecting the trigger source to connector P1 (DB37 at card end) using pin 21 for A/Ds 0/1 or pin 2 for A/Ds 2/3. The external triggering pulse must TTL compatible, be active low, and have a minimum pulse width of 40 nS.

For applications with a mix of channel conversion rates, it may be possible to trigger at the higher rates and only read the lower sample rate channels when required. For example , if an application has one channel which must be read at 50 kHz and another at 100 Hz, it is easy to read the 100 Hz channel one time out of 500 conversions even though it was converted at a much higher rate. The other 499 conversions were ignored.

JP5 and JP6	Conversion Trigger Source
1-2	DSP timer 0 (TCLK0) or memory mapped
2-3	DSP timer 1 (TCLK1) or memory-mapped
None	External clock or memory-mapped

Figure 13: A/D converter trigger sources.

The ADC offsets and gain are set at the factory. If you find that they need recalibration, or need to change to the bipolar input range, here is the adjustment procedure. Both gain and offset errors for the ADC are trimmable by the user on the PC32.

A/D Channel	A/D Reference Designator	Offset Trim Pot	Linearity Trim Pot
0	U8	R47	R48
1	U10	R52	R53
2	U15	R57	R58
3	U16	R62	R63

Figure 14: A/D Offset and Linearity Adjust Pots

Errors should be trimmed with the following methodology at the expected operating temperature:

1. Short the differential inputs for each channel to each other. You may want to do this out at your sensor to include any error sources present in the application circuitry. Trim offset pots R47..R62 such that a zero code is observed when continuously sampling the converters.
2. Connect one input to a voltage reference and check gain for proper codes. Full scale inputs, at a gain of 1, are +/-10V and should read raw ADC codes of 32767 and -32767 respectively for the bipolar range. Unipolar full scale inputs are 0-10 V. Trim R48 ... R63 as necessary to achieve the proper code.

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The analog input range of each A/D channel is configurable using jumpers JP54A1 through JP54A4 for channels 0 through 3 respectively in conjunction with the input resistor selection R17, R23, R29, R35.

A/D Channel	Input Span	Jumper	Setting	Input Resistor
0	+/-10V	JP54A 1	None	R17 = 10K
0	0-10V	JP54A1	2-3	R17=4.99K
0	-10-0V	JP54A1	1-2	R17=4.99K
1	+/-10V	JP54A2	None	R23= 10K
1	0-10V	JP54A2	2-3	R23=4.99K
1	-10-0V	JP54A2	1-2	R23=4.99K
2	+/-10V	JP54A3	None	R29= 10K
2	0-10V	JP54A3	2-3	R29=4.99K
2	-10-0V	JP54A3	1-2	R29=4.99K
3	+/-10V	JP54A4	None	R35= 10K
3	0-10V	JP54A4	2-3	R35=4.99K
3	-10-0V	JP54A4	1-2	R35=4.99K

Figure 15: Standard A/D input range selection.

Custom bipolar input ranges may be achieved by modifying resistor R38 (CH 0), R39 (CH 1), R40 (CH 2), R41 (CH 3). The gain amps used to adjust input signal levels have an inverting topology with the following resistor arrangement:

A/D Channel	Gain Expression	Offset Expression
0	R38/R17 = 10K/10K	Vin + (R17/R42) Vref
1	R39/R23 = 10K/10K	Vin + (R23/R43) Vref
2	R40/R29 = 10K/10K	Vin + (R29/R44) Vref
3	R41/R35 = 10K/10K	Vin + (R35/R45) Vref

Figure 16: Custom A/D input span adjustment.

Vref is the selected offset from JP54A1..4 and is either +5v or -5V. Innovative recommends the use of tight tolerance (1%), low temperature coefficient resistors with low noise characteristics (such as metal film types) for these resistors.

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2.3.2.2 Anti-alias Filtering

The PC32 provides independent 6-pole anti-alias filtering with offset adjustment on each A/D channel. The anti-alias filters come preconfigured from the factory with a 50 kHz passband, but by substituting a commonly available DIP-packaged resistor network these filters can be tuned to virtually any required passband frequency. The schematic for the four filter banks is given on the next page.

The following schematics show the filter structure for each input channel and give the reference designators for each filter component, allowing users to modify the filter networks to suit their applications.

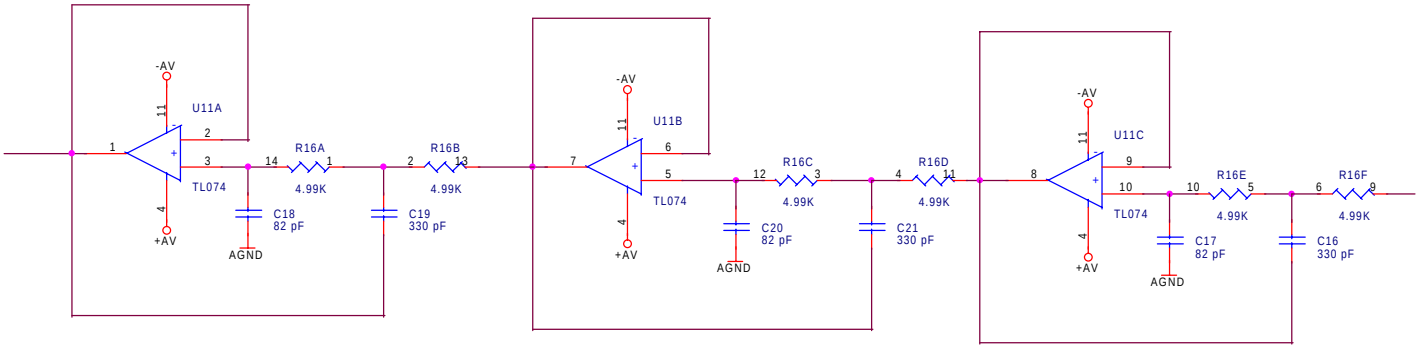


Figure 17: A/D Channel 0 Anti-alias Filter Schematic

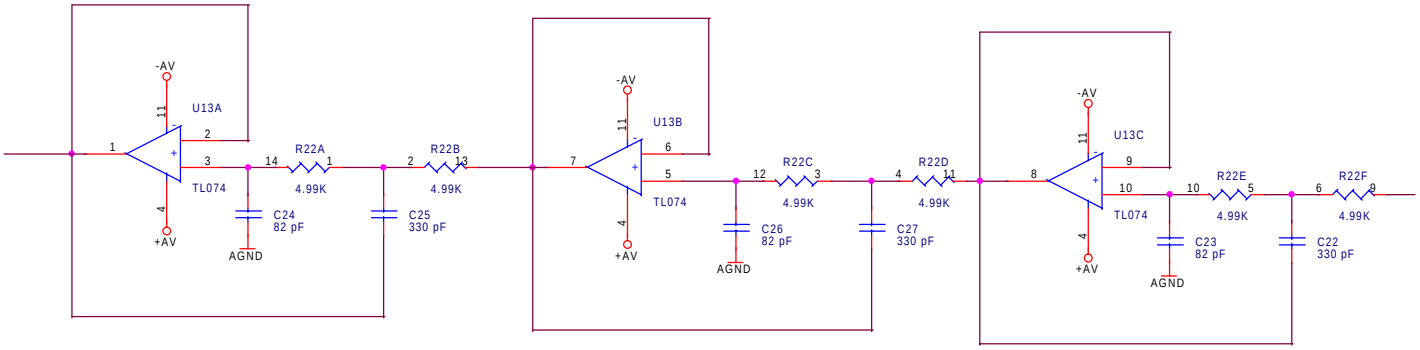


Figure 18: A/D Channel 1 Anti-alias Filter Schematic

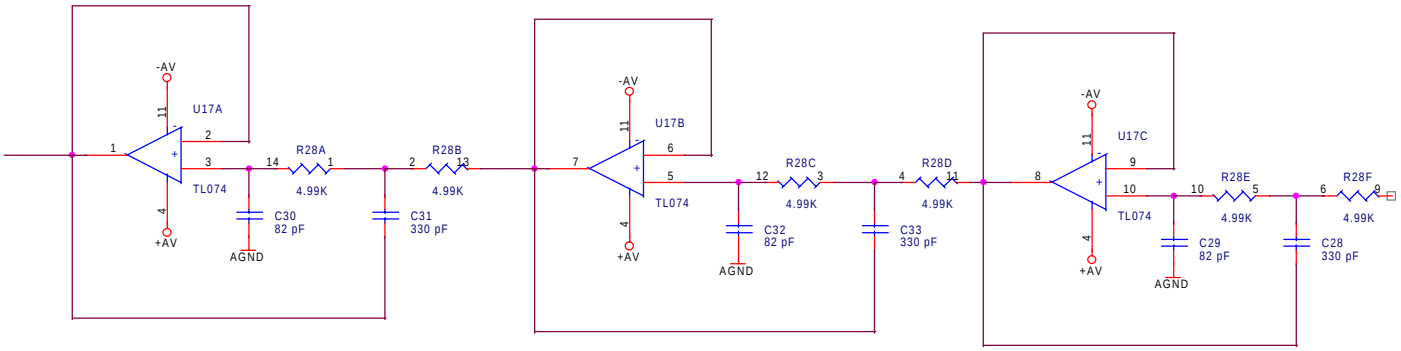


Figure 19: A/D Channel 2 Anti-alias Filter Schematic

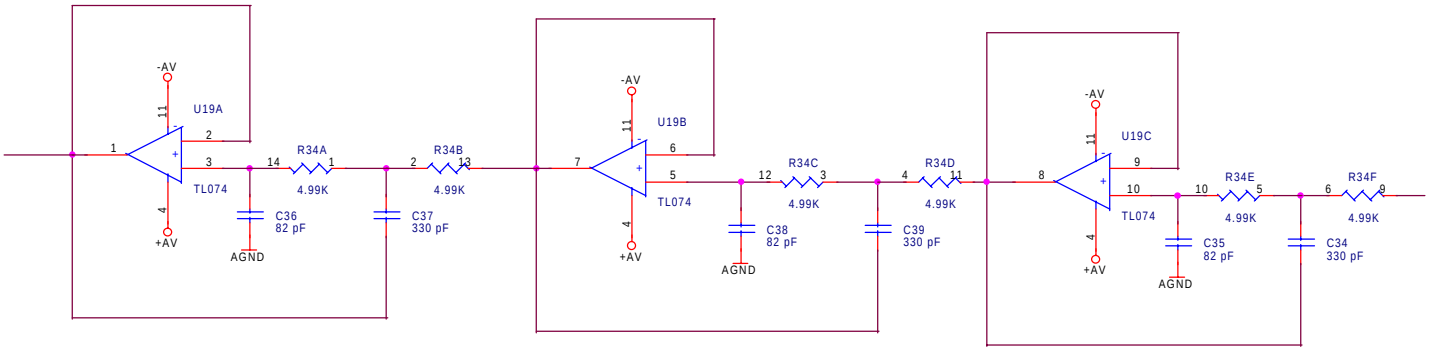


Figure 20: A/D Channel 3 Anti-alias Filter Schematic

By replacing resistor networks R16, R22, R28, or R34 for A/D channels 0 through 3 respectively, the A/D filters can be individually tuned for a user-desired passband. The plot below shows frequency responses for several typical resistor values.

Innovative Integration recommends limiting the size of the network resistor, as op-amp input bias current will cause increasing offset errors with increasing network resistor values.

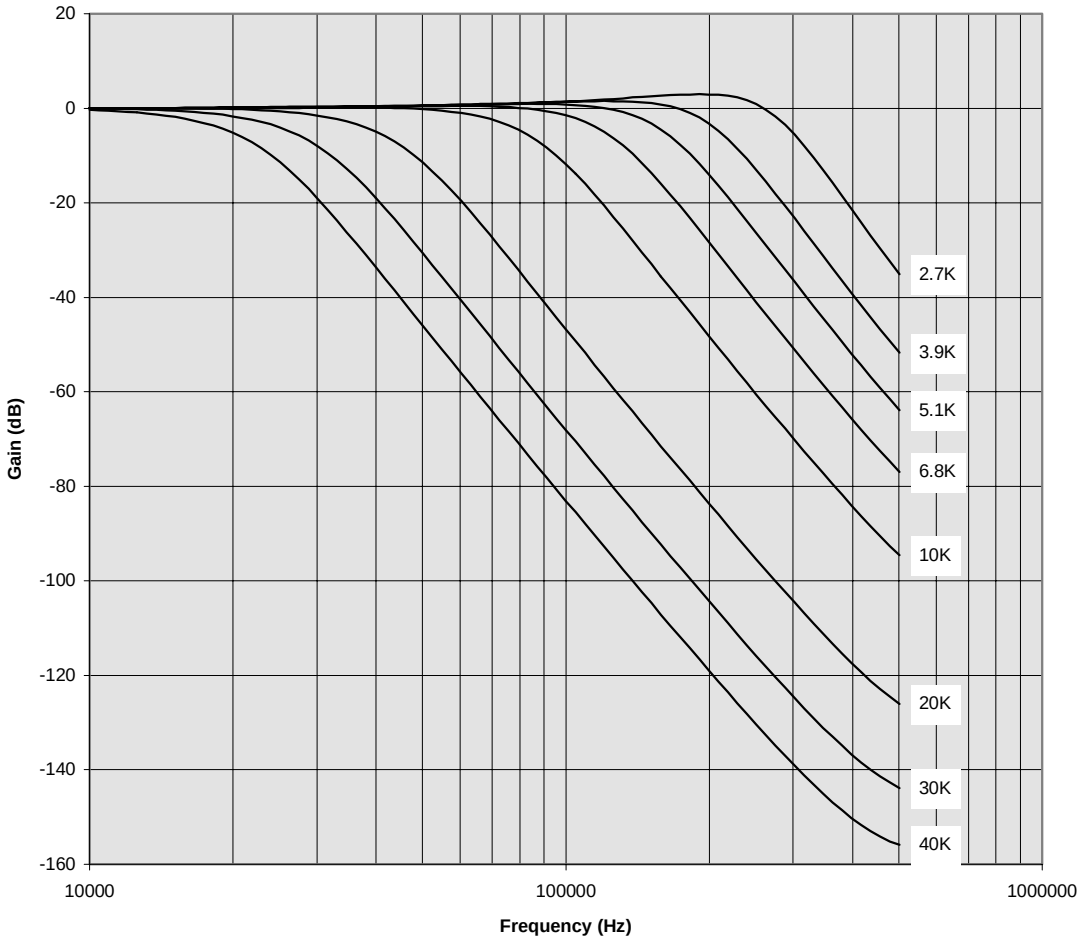


Figure 21: Anti-alias Filter Frequency Response

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2.3.2.3 Analog Output

Four independent channels of 200 kHz, 16-bit instrumentation-grade digital-to-analog converters (D/A) are provided on the PC32. The D/A used is Analog Devices AD669.The data sheet for this part is included in the data sheets in the appendix of this manual. The D/As are useful for analog signal outputs for both control and signal generation.

The D/A converters are double-buffered and the PC32 implements several update methods to accommodate various applications. All of the D/A's may be updated individually, or as pairs by either the TIMER0 or TIMER 1 DSP clock running as a timebase.

The D/As are capable of full scale output swings in 5 µS. Voltages appear on the output pins of each D/A channel within 5 µS (for a full scale change in output) after having completed an analog update operation. Small signal response is significantly faster.

2.3.2.4 D/A Converter Output Ranges

The D/As have a factory default output range of +10V to -10V, which is set via an output amplifier stage on each D/A channel. In addition, each stage has a jumper selectable offset reference voltage which can be used to make unipolar output ranges. The following diagrams give schematics for each of the D/A output amplifier stages.

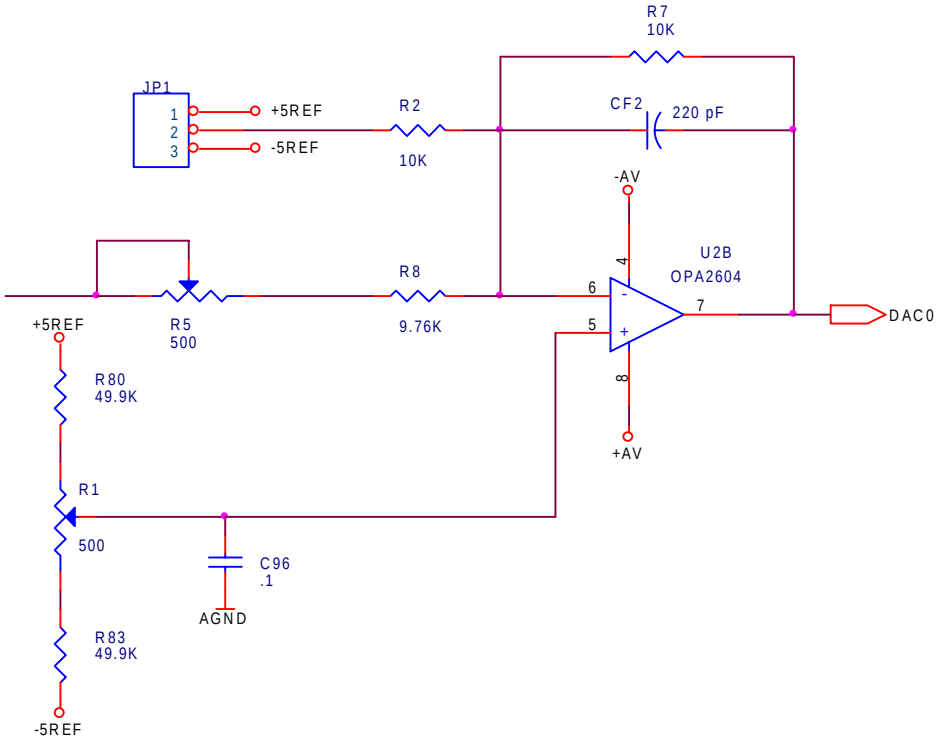


Figure 22: D/A Channel 0 Output Amplifier

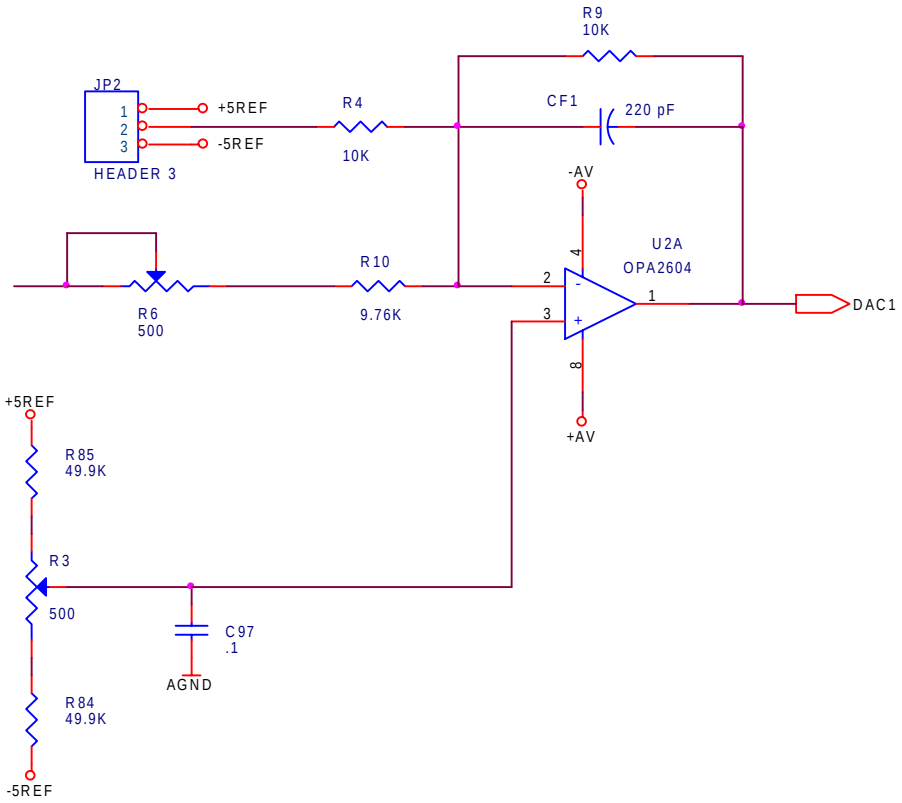


Figure 23: D/A Channel 1 Output Amplifier

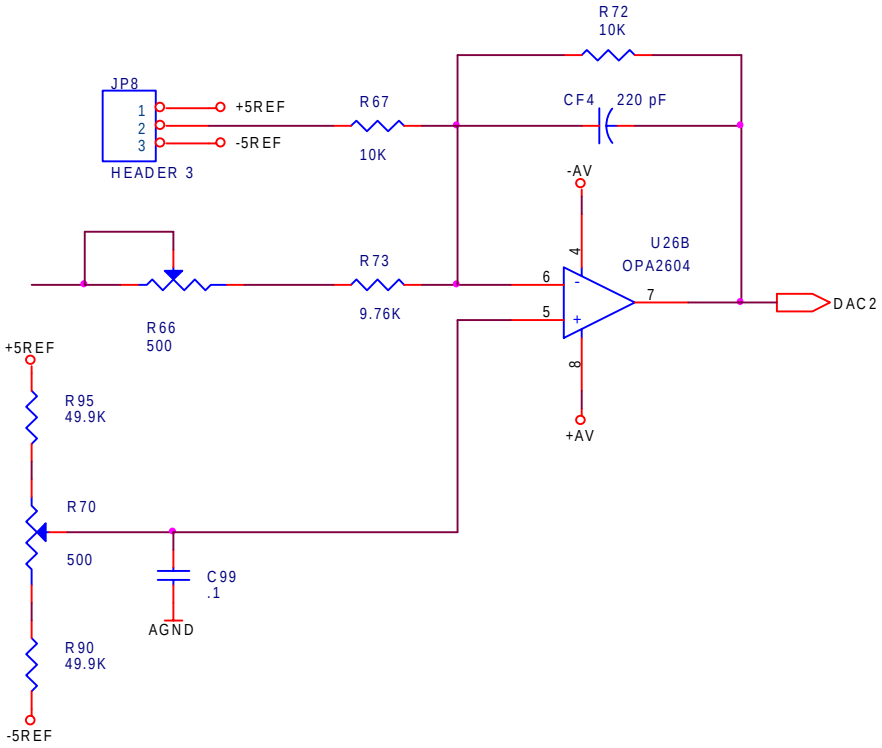


Figure 24: D/A Channel 2 Output Amplifier

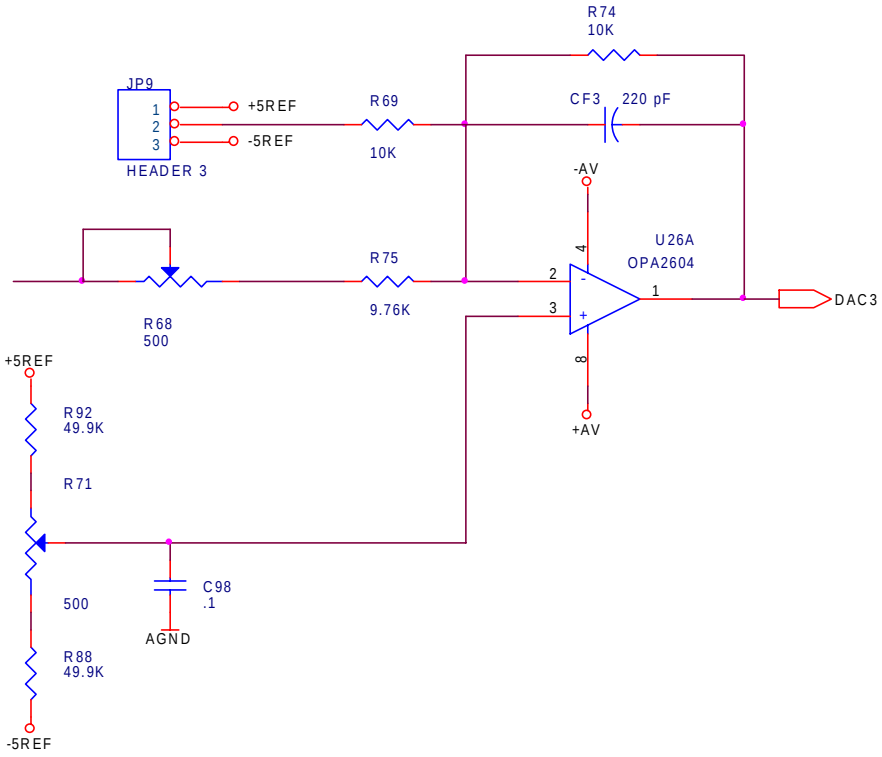


Figure 25: D/A Channel 3 Output Amplifier

The following table gives gain expressions with reference designators for each D/A output channel, where Vout is the amplifier output, Vi is the ampifier input (output from the D/A device), and Voff is the optional offset voltage set using the appropriate jumper (see schematics above). This information can be used to set custom output ranges for each channel. The D/A device output range is always +-10V, so gain and offset calculations are made for the output amplifier to convert this nominal output range to the required range.

For example, to change channel 0 to a +-5V input range the required amplifier function would be Vout = -0.5Vi. Substituting in the table functions, we get

Vout = (-Vi * (R7/R8)) + (-Voff * (R7/R2))
Vout = (-Vi * (0.5)) + (-Voff * 0)
=> R7/R8 = 0.5
=> R7 unmodified, R8 = 19.6 Kohm, jumper JP1 is left unconnected.

To make a unipolar output range (for example, 0 to 10V), the offset capability is used to achieve an amplifier function of Vout = -0.5Vi + 5:

Vout = (-Vi * (R7/R8)) + (-Voff * (R7/R2))
Vout = (-Vi * (0.5)) + (-Voff * 1)
Vout = -0.5Vi -Voff
=> R7/R8 = 0.5, R7/R2 = 1
⇨ R7 unmodified, R8 = 19.6 Kohms, R2 unmodified, JP1 with jumper shunting pins 2 and 3 to connect the offset voltage (-5 volts).

DAC Channel	Gain Expression
0	Vout = (-Vi * (R7/R8)) + (-Voff * (R7/R2))
1	Vout = (-Vi * (R9/R10)) + (-Voff * (R9/R4))
2	Vout = (-Vi * (R72/R73)) + (-Voff * (R72/R67))
3	Vout = (-Vi * (R74/R75)) + (-Voff * (R74/R69))

Figure 26: D/A Gain Equations

2.3.2.5 D/A Output Trimming

The PC32 supports an output trim on each D/A output when used in the bipolar mode (no onboard trim is available for the unipolar mode). The trim method outlined below minimizes offset error, gain error, and bipolar zero error.

1. Write the value -32767 to the D/A and trigger a conversion. Adjust R5 (for DAC0, R6 for DAC1, R66 for DAC2 or R68 for DAC3) to give +10.000 volts output at the DB37 header. All voltages should be measured with a short (1") ground connection to analog ground on the DB37 connector.
2. Write the value 32767 to the D/A and trigger a conversion. Adjust R1 (for DAC0, R3 for DAC1, R70 for DAC2 or R71 for DAC3) to give -9.999 volts output.
3. Write the value 0 to the D/A and trigger a conversion. Adjust R5 (for DAC0, R6 for DAC1, R66 for DAC2 or R68 for DAC3) to give 0.000 volts out.

Please note that this trim procedure gives voltages which will be output from a standard PC32. Modifed output ranges will of course result in different output voltages.

2.3.2.6 D/A Converter Control Registers (Software Conversion Triggering)

The interface to the D/As allows flexibility in data loading and updating the outputs of the D/A converters. The D/A control registers are mapped into the IOSTROBE region of memory. All registers are write only. Since the D/A's are double buffered, you must update the D/A channels individually to generate the voltage output from loaded number.

Address (hex)	Function
814000	Load D/A 0 data latches
814800	Load D/A 1 data latches
815000	Load D/A 2 data latches
815800	Load D/A 3 data latches
816000	Update out voltage DAC 0
816800	Update out voltage DAC 1
817000	Update out voltage DAC 2
817800	Update out voltage DAC 3

Figure 27: DAC Register Memory Map

Note that on PC32 boards depopulated to just two analog channels, only D/A channels zero and two are available.

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2.3.2.7 D/A Hardware Conversion Triggering

The D/As may receive an update signal from either a memory mapped access, one of the two DSP timers, or an external source. The update signal causes the D/A to output an analog voltage representative of the currently latched data value. The update operation does not cause a data transmission to the D/A (data communications can only occur on a software-driven basis, by use of the memory-mapped D/A registers). Hardware conversion triggers can include timer outputs and external TTL strobe signals. The source of the update for each device is controlled by jumper JP3, JP4, JP10, JP11 for DAC 0 through 3 respectively.

JP3, JP4, JP10, JP11 Jumper Selection	Selected DAC Update Signal
1-2	DAC0 driven by TCLK0
3-4	DAC1 driven by TCLK1
5-6	DSP memory access

Figure 28: DAC Update Trigger Selection

External updating of the DACs is accomplished using the TCLK0 or TCLK1 pins on JP12. For this usage, configure these pins as inputs to the DSP and drive the pins with an active low, TTL signal which has a pulse width 50 nS or longer. Conversion occurs on the rising edge of the pulse. The internal timers may still be used in this configuration since the actual TCLK0..1 pins may be decoupled from the internal timer. The selection of the update trigger source depends on your application. For audio applications, it is usually best to use a timer driven conversion clock since this results in the lowest phase jitter and timing irregularities which compromise the performance from a dynamic point of view. For other applications, like servo control, it may be more convenient to use the D/A as a memory-mapped peripheral. Either way, DMA may be used to load the D/A's to reduce the processor involvement.

2.3.2.8 Analog Power Supplies

The analog subsection uses a DC-DC converter and several linear supplies to provide clean analog power for the A/D's and D/A's. These power supplies are available for use by external hardware via the DB37 external connector. Current draw from these supplies is limited, however, to the amounts listed in the following table.

Supply (referenced to AGND)	Maximum External Current Limit
+AV (= +15V)	30 mA
-AV (= -15V)	30 mA

Figure 29: DC-DC converter power limits.

DVCC (pin 17 on the DB37 connector) is available at significantly higher current ratings. This supply is the ISA bus logic +5V and as such is noisy and not recommended for powering sensitive, high quality analog circuitry. DVCC, however, could be made to supply power to an external DC-DC converter which would in turn provide significantly cleaner power to external analog circuitry.

The DC-DC converter used on the PC32 is short-circuit protected and can survive indefinite short-circuit to ground from either output. Shorting +15 to -15 should be avoided as this can destroy the converter if left unchecked for several minutes.

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2.4 Processor Interrupts

The PC32 provides the option to generate interrupts to the onboard TMS320C32 processor from a number of on- and off-board sources. These user-selectable connections are made via jumper header JP17. Possible sources for these interrupts and their signal requirements are listed below.

2.4.1 Interrupt Combinations

The following table lists the possible interrupt sources. Descriptions of each interrupt type and specific signal requirements are given following the table. The user should make use of this table when planning the overall system design so as to avoid interrupt conflicts and configuration problems.

Interrupt	Source	JP17 Setting
EI1	ADC 0/1 pair not busy	1-3
EI1	external digital clock	8-10
EI1	PC interrupt 0 to DSP	1-2
EI2	ADC 0/1 pair not busy	3-5
EI2	ADC 2/3 pair not busy	5-7
EI2	external digital clock	10-12
EI2	**PC interrupt 1 to DSP**	**11-12**
EI3	**PC interrupt 0 to DSP**	**2-4**
EI3	ADC 0/1 pair not busy	3-4
EI3	PC interrupt 1 to DSP	9-11
EI3	external digital clock	9-10
EI3	ADC 2/3 pair not busy	7-9

Figure 30: Interrupt sources selection jumper.

Factory default jumpers shown in **bold**

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2.4.2 Interrupt Source Signal Descriptions

The following section gives descriptions of each interrupt, its source connection, and any signal requirements which must be met by external equipment. In all cases, external interrupt and time source inputs should be low-going TTL pulses. The C32 DSP may be configured as either edge sensitive or level sensitive input to the DSP. The default setup in boot.asm is edge sensitive. Edge sensitivity tends to be the easiest to work with and typically eliminates the possibility of multiple interrupt triggerings from ill-conditioned interrupt sources. To recognize a single interrupt from a level sensitive source, the pulse must be less than 2 H clocks wide, or less than 100 nS for a 40 MHz system.

1. EI0, EI1, EI2, and EI3: These are the processor interrupt input pins. These pins can be driven by either an offboard TTL source or by the sources listed in the table above. These pins can be used to signal an outside event requiring the PC32's attention, to invoke either an interrupt routine or initiate a DMA transfer.
2. PC_INT0: This is an output from the Host PC initiated by strobing low bit 4 in the PC32 Host control register.
3. PC_INT0: This is an output from the Host PC initiated by strobing low bit 4 in the PC32 Host control register.
4. External Digital Input: This is an interrupt indicating new data has been placed into the external digital port.
5. ADC 0/1 not busy : This signal indicates that a conversion is complete for the A/D pair 0/1.
6. ADC 2/3 not busy : This signal indicates that a conversion is complete for the A/D pair 2/3

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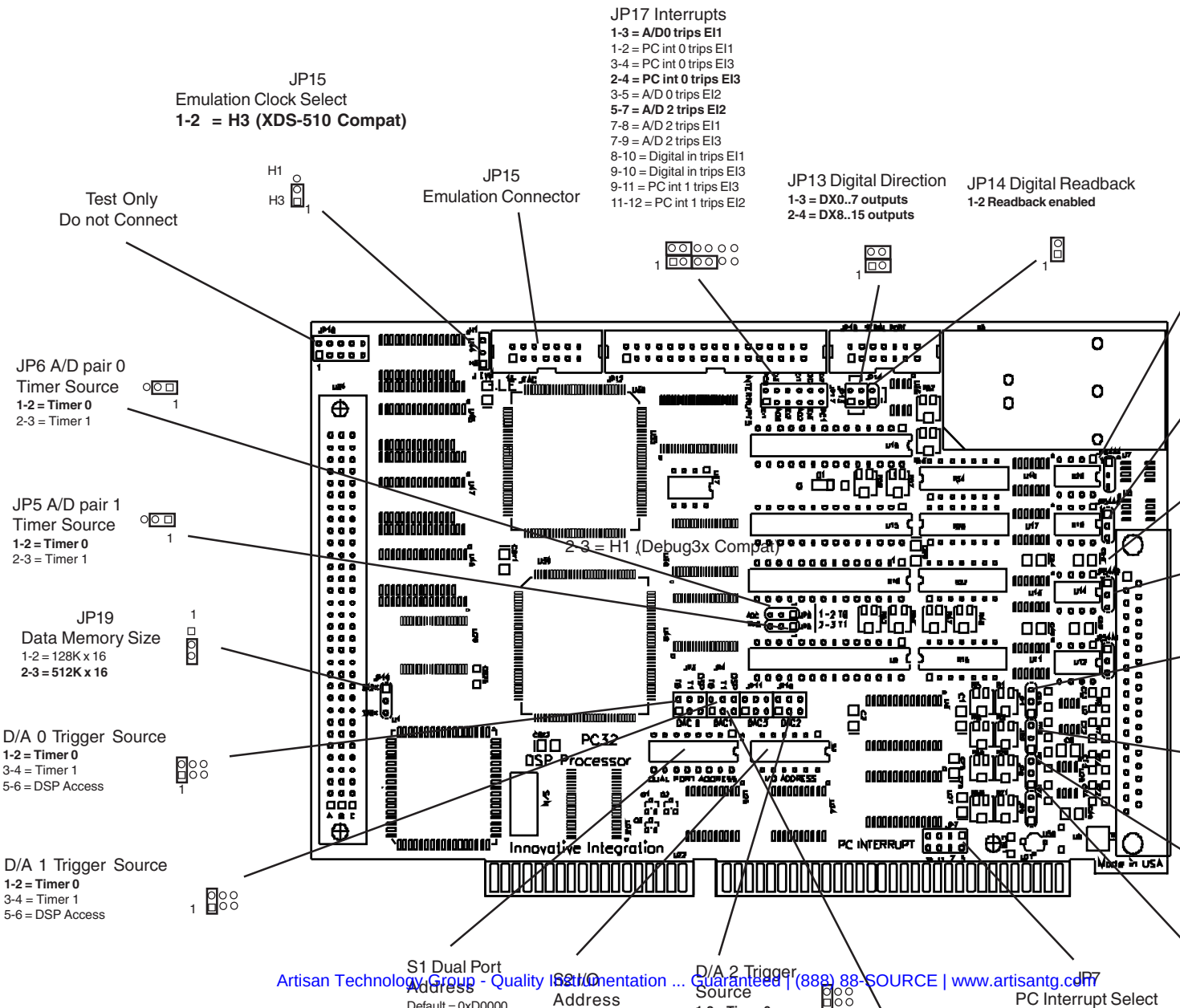
3. Appendices

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3.1 Factory Jumper Settings

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PC32 Factory Jumper Settings



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3.2 PC32 Connector Pinouts

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The analog I/O connector provides access to the A/D inputs, D/A outputs and selected interrupt inputs.

Connector type: DB37
# of pins: 37
Mating connector: AMP 747321-1

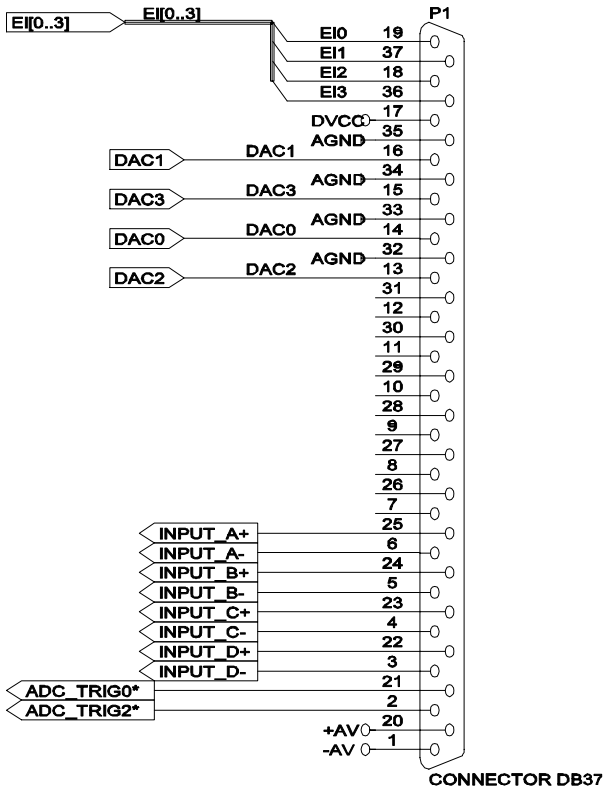


Figure 31: Analog I/O connector.

Signal Name	Function
INPUT_x+	Analog positive input signals channels A..D.
INPUT_x-	Analog negative input signals channels A..D
DAC0..3	Analog output signals
ADC_TRIG0*	External A/D conversion strobe input for A/Ds 0/1.
ADC_TRIG2*	External A/D conversion strobe input for A/Ds 2/3
EI0..3	External Interrupt inputs
VCC	+5Vdc (analog power supply)
AGND	Analog ground
+AV	+15Vdc (analog power supply)
-AV	-15Vdc (analog power supply)

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The two digital I/O header provides access to the parallel I/O ports and the PC32 counter/timer complement, plus selected interrupt input pins.

Connector type: .100” header
# of pins: 34, in two rows
Mating connector: AMP 746285-8

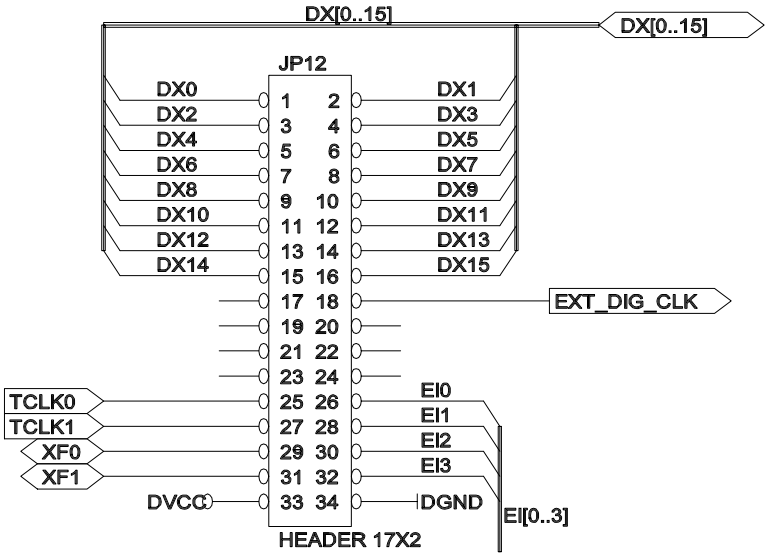


Figure 32: JP15 digital I/O connector.

Signal Name	Function
DX0..15	Digital I/O pins
Ext_Dig_clk	Clock input for latching digital bits into PC32 digital port
TCLK0..1	DSP counter/timer pins
XF0..1	DSP general purpose I/O pins
EI0..3	External Interrupt pins
DVCC	+5Vdc (digital 5V from PC supply)
DGND	Digital ground (to PC supply)

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The memory expansion header provides access to all important TMS320C32 bus signals to be used by peripheral daughter cards.

Connector type: DIN 96 Female
# of pins: 96 in three rows
Mating connector: AMP 650908-5

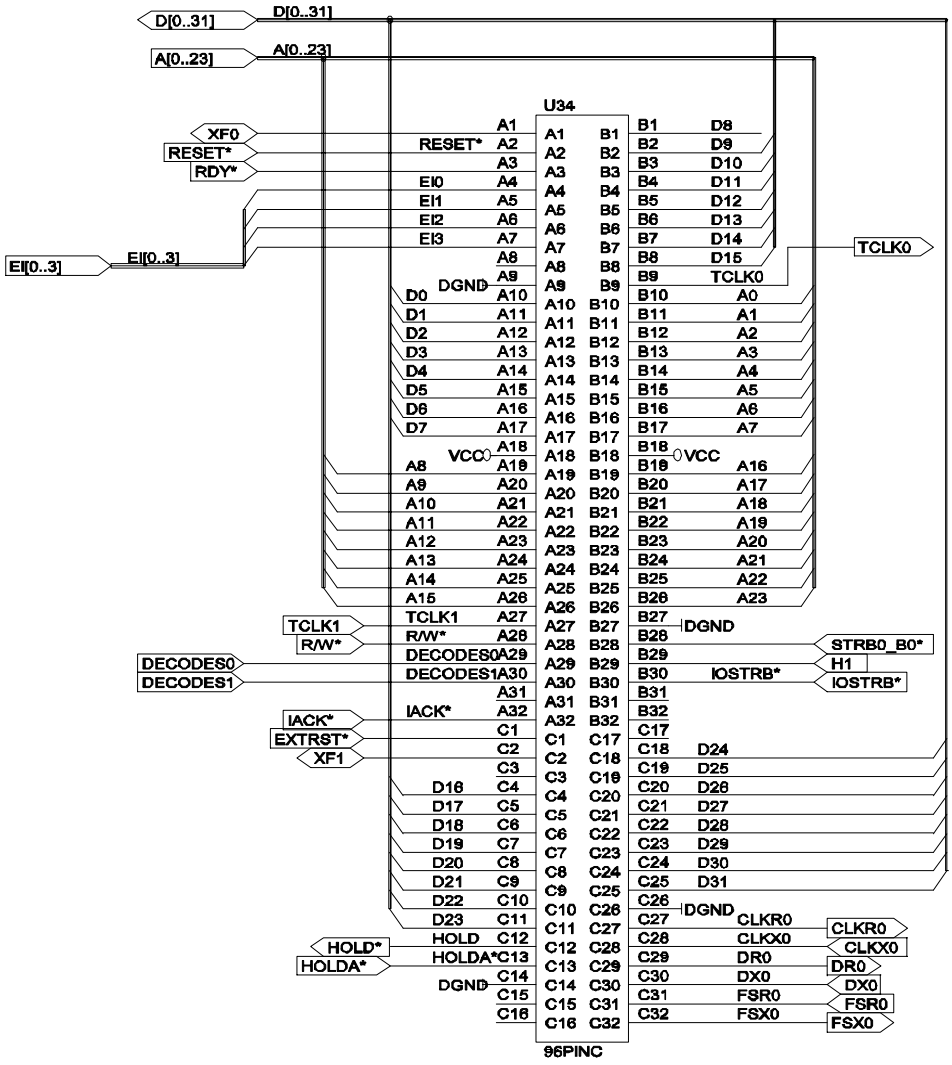


Figure 33: Memory expansion connector

Signal Name	Function
D[0..31]	‘C32 bidirectional data bus, unbuffered.
A[0..31]	‘C32 address bus, unbuffered.
R/W*	‘C32 read/write signal.
EI[0..3]	‘C32 interrupt inputs
H1	‘C32 processor clock (ICLK rate / 2).
RDY*	'
IOSTROBE*	‘C32 IO memory region active
STRB0_B0*	‘C32 external bus memory region 0 active strobe.
IACK*	‘C32 interrupt acknowledge signal.
WAIT[0..2]	PC32 external wait-state inputs.
HOLD*	‘C32 hold request input.
HOLDA*	‘C32 hold acknowledge output.
TCLK[0..1]	‘C32 counter/timer I/O pins.
DECODES[0..1]	Uncommitted strobes for user peripherals.
CLKR0	‘C32 sync serial port receive data clock
CLKX0	‘C32 sync serial port transmit data clock
DR0	‘C32 sync serial port receive data
DX0	‘C32 sync serial port transmit data
FSR0	‘C32 sync serial port frame sync receive
EXT_FSX0	‘C32 sync serial port frame sync transmit
RESET*	PC32 reset, active low
RAM_CS*	PC32 onboard SRAM chip select, active low.
VCC	+5Vdc (digital 5V from PC supply)
DGND	Digital ground (to PC supply)
AGND	Analog ground (to DC-DC converter)

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The DSP synchronous serial port connector provides access to the serial port on the DSP for connection to external devices and other PC32 cards.

Connector type: .100” header

# of pins: 14, in two rows

Mating connector: AMP 746285-2

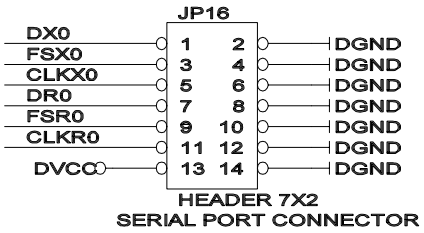


Figure 34: 'C32 Synchronous Serial Port Connector

Signal Name	Function
DXO	Data transmit from C32
DRO	Data receive into C32
FSX0	Frame sync for transmit
FSR0	Frame sync for receive
CLKX0	Clock for transmit
CLKR0	Clock for receive
DVCC	+5Vdc digital supply
DGND	Digital ground

3.3 Device Data Sheets

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Low Cost, Low Power Instrumentation Amplifier

AD620

FEATURES
EASY TO USE
Gain Set with One External Resistor (Gain Range 1 to 1000)
Wide Power Supply Range (±2.3 V to ±18 V)
Higher Performance than Three Op Amp IA Designs
Available in 8-Pin DIP and SOIC Packaging
Low Power, 1.3 mA max Supply Current

EXCELLENT DC PERFORMANCE ("A GRADE")
125 μV max, Input Offset Voltage (50 μV max "B" Grade)
1 μV/°C max, Input Offset Drift
2.0 nA max, Input Bias Current
93 dB min Common-Mode Rejection Ratio (G = 10)

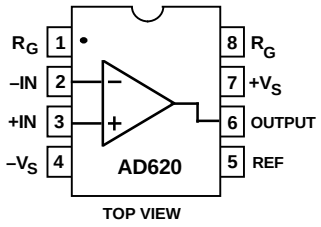
LOW NOISE
9 nV/√Hz, @ 1 kHz, Input Voltage Noise
0.28 μV p-p Noise (0.1 Hz to 10 Hz)

EXCELLENT AC SPECIFICATIONS
120 kHz Bandwidth (G = 100)
15 μs Settling Time to 0.01%

APPLICATIONS
Weigh Scales
ECG and Medical Instrumentation
Transducer Interface
Data Acquisition Systems
Industrial Process Controls
Battery Powered and Portable Equipment

CONNECTION DIAGRAM

8-Pin Plastic Mini-DIP (N), Cerdip (Q) and SOIC (R) Packages



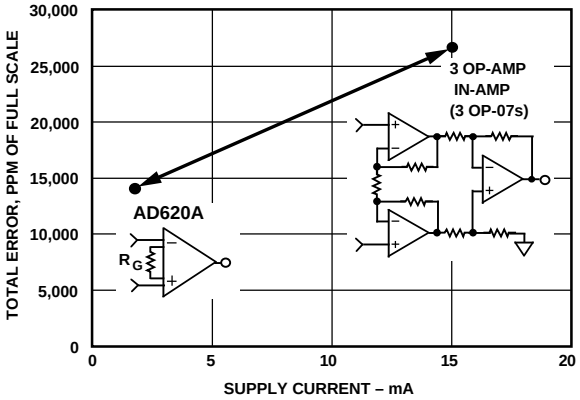
TOP VIEW

PRODUCT DESCRIPTION

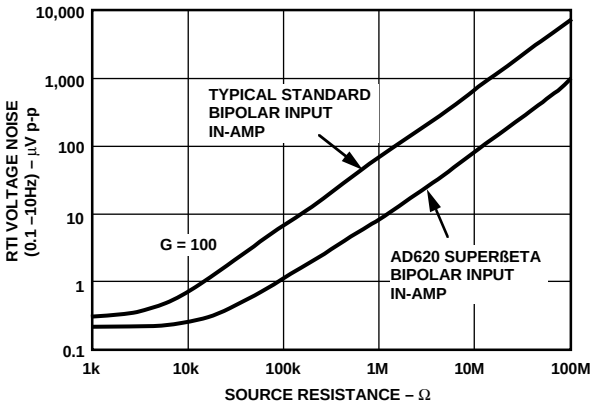
The AD620 is a low cost, high accuracy instrumentation amplifier which requires only one external resistor to set gains of 1 to 1000. Furthermore, the AD620 features 8-pin SOIC and DIP packaging that is smaller than discrete designs, and offers lower power (only 1.3 mA max supply current), making it a good fit for battery powered, portable (or remote) applications.

The AD620, with its high accuracy of 40 ppm maximum nonlinearity, low offset voltage of 50 μV max and offset drift of 0.6 μV/°C max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias current, and low power of the AD620 make it well suited for medical applications such as ECG and noninvasive blood pressure monitors.

The low input bias current of 1.0 nA max is made possible with the use of Superβeta processing in the input stage. The AD620 works well as a preamplifier due to its low input voltage noise of 9 nV/√Hz at 1 kHz, 0.28 μV p-p in the 0.1 Hz to 10 Hz band, 0.1 pA/√Hz input current noise. Also, the AD620 is well suited for multiplexed applications with its settling time of 15 μs to 0.01% and its cost is low enough to enable designs with one in amp per channel.



Three Op Amp IA Designs vs. AD620



Total Voltage Noise vs. Source Resistance

REV. D

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AD620—SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[2]	V_{OUT} = ±10 V										
G = 1			0.03	0.10		0.01	0.02		0.03	0.10	%
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = –10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature	Gain <1000[2]			–50			–50			–50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
Over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
Over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	$–V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	$–V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	$–V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.1		$+V_S$ – 1.4	$–V_S$ + 2.3		$+V_S$ – 1.4	V
Common-Mode Rejection Ratio DC to 60 Hz with I kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G= 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G= 100		110	130		120	130		110	130		dB
G= 1000		110	130		120	130		110	130		dB
OUTPUT											
Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	$–V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.4		$+V_S$ – 1.3	$–V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to +18 V	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	$–V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 1.6		$+V_S$ – 1.5	$–V_S$ + 2.3		$+V_S$ – 1.5	V
Short Current Circuit			±18			±18			±18		mA

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Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		µs
G = 1000			150			150			150		µs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	µV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	µV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ –1.6	V_S + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance		–40 to +85			–40 to +85			–55 to +125			°C

NOTES
[1]Does not include effects of external resistor R_G.
[2]One input grounded. G = 1.
[3]This is defined as the same supply range which is used to specify PSR.
[4]See Analog Devices military data sheet for 883B tested specifications.

Specifications subject to change without notice.

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ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Internal Power Dissipation[2] . . . . . 650 mW
Input Voltage (Common Mode) . . . . . $\pm V_S$
Differential Input Voltage . . . . . ±25 V
Output Short Circuit Duration . . . . . Indefinite
Storage Temperature Range (Q) . . . . . –65°C to +150°C
Storage Temperature Range (N, R) . . . . . –65°C to +125°C
Operating Temperature Range
AD620 (A, B) . . . . . –40°C to +85°C
AD620 (S) . . . . . –55°C to +125°C
Lead Temperature Range
(Soldering 10 seconds) . . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Specification is for device in free air:
8-Pin Plastic Package: θ_{JA} = 95°C/Watt
8-Pin Cerdip Package: θ_{JA} = 110°C/Watt
8-Pin SOIC Package: θ_{JA} = 155°C/Watt

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD620AN	–40°C to +85°C	N-8
AD620BN	–40°C to +85°C	N-8
AD620AR	–40°C to +85°C	R-8
AD620BR	–40°C to +85°C	R-8
AD620A Chips	–40°C to +85°C	Die Form
AD620SQ/883B	–55°C to +125°C	Q-8

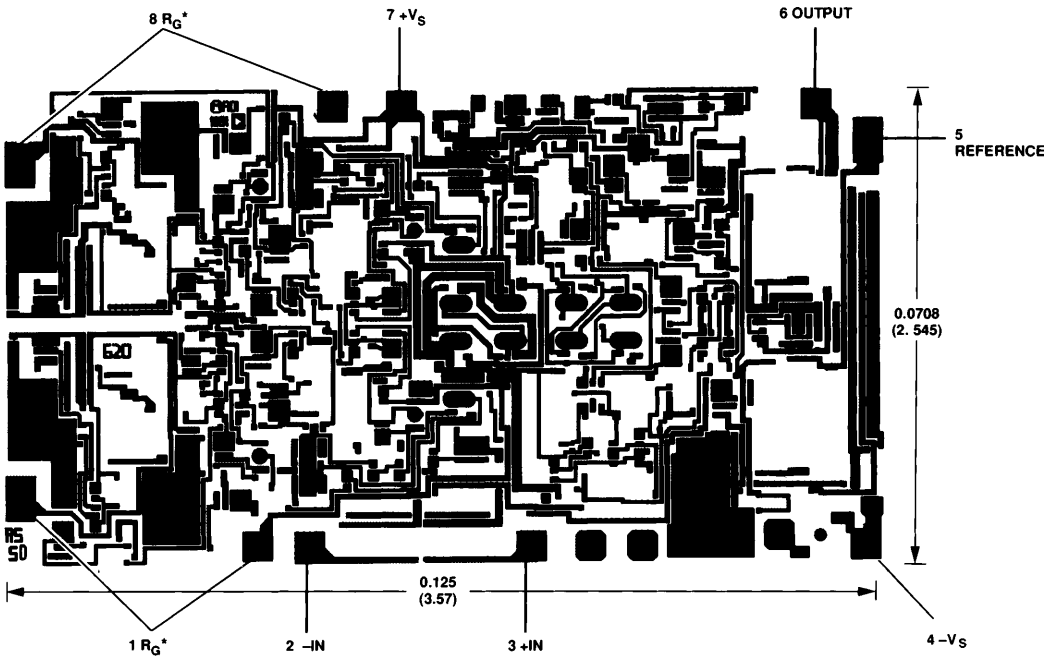
*N = Plastic DIP; Q = Cerdip; R = SOIC.

ESD SUSCEPTIBILITY

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 volts, which readily accumulate on the human body and on test equipment, can discharge without detection. Although the AD620 features proprietary ESD protection circuitry, permanent damage may still occur on these devices if they are subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid any performance degradation or loss of functionality.

METALIZATION PHOTOGRAPHY

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



*FOR CHIP APPLICATIONS: THE PADS 1R_G AND 8R_G MUST BE CONNECTED IN PARALLEL TO THE EXTERNAL GAIN REGISTER R_G. DO NOT CONNECT THEM IN SERIES TO R_G. FOR UNITY GAIN APPLICATIONS WHERE R_G IS NOT REQUIRED, THE PADS 1R_G MAY SIMPLY BE BONDED TOGETHER, AS WELL AS THE PADS 8R_G.

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Typical Characteristics (@ +25°C, V_S = ±15 V, R_L = 2 kΩ, unless otherwise noted)

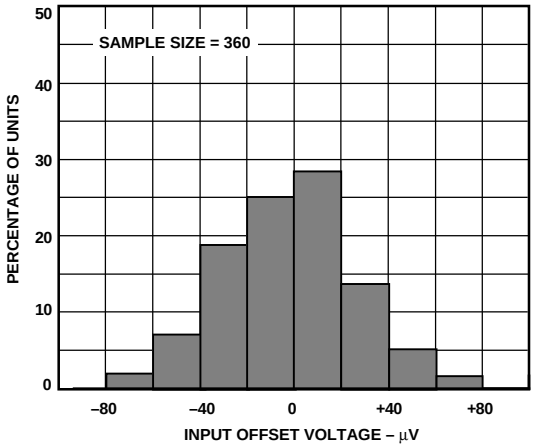


Figure 1. Typical Distribution of Input Offset Voltage

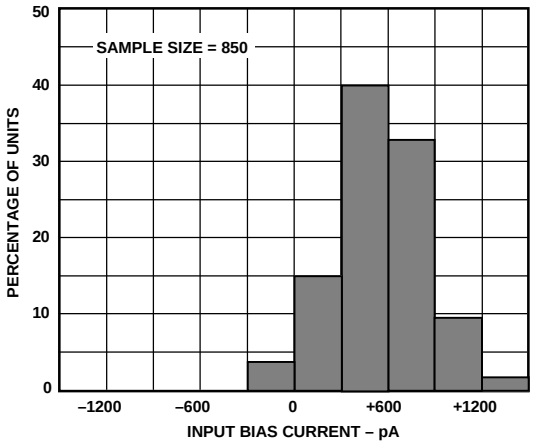


Figure 2. Typical Distribution of Input Bias Current

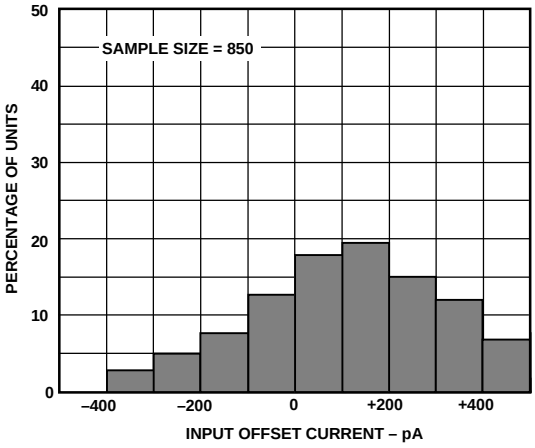


Figure 3. Typical Distribution of Input Offset Current

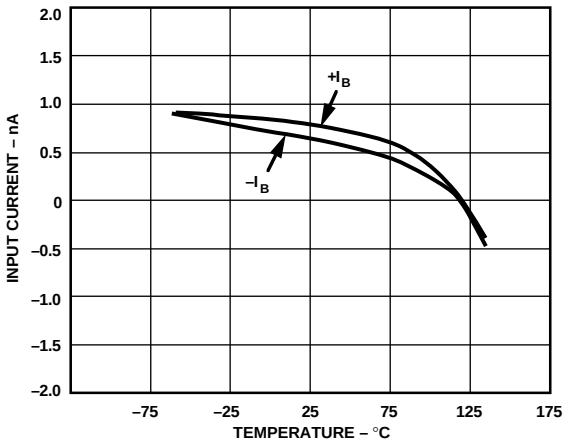


Figure 4. Input Bias Current vs. Temperature

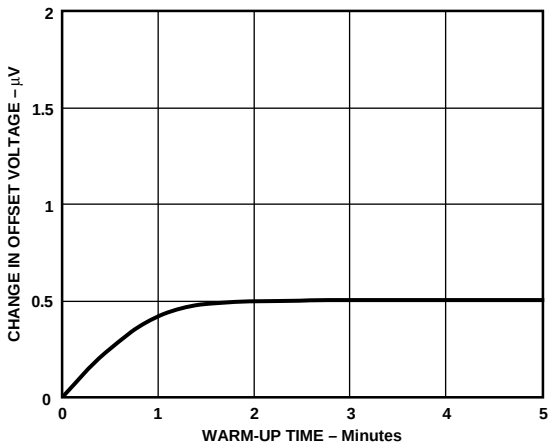


Figure 5. Change in Input Offset Voltage vs. Warm-Up Time

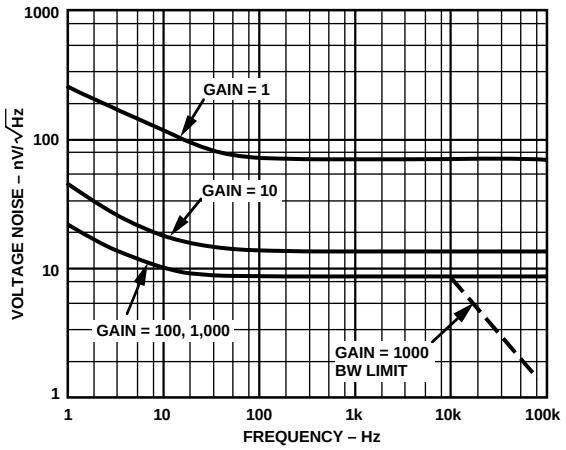


Figure 6. Voltage Noise Spectral Density vs. Frequency, (G = 1–1000)

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AD620–Typical Characteristics

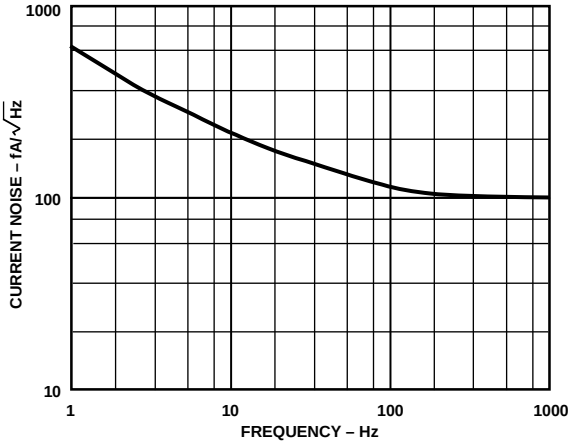


Figure 7. Current Noise Spectral Density vs. Frequency

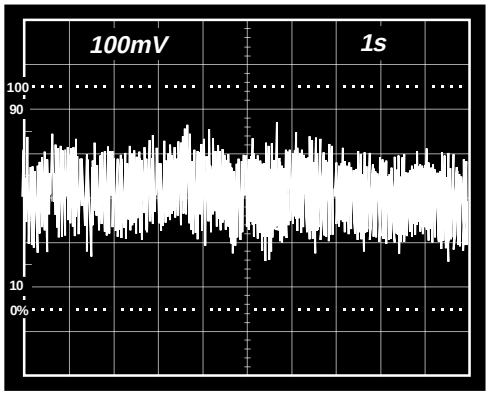


Figure 9. 0.1 Hz to 10 Hz Current Noise, 5 pA/Div

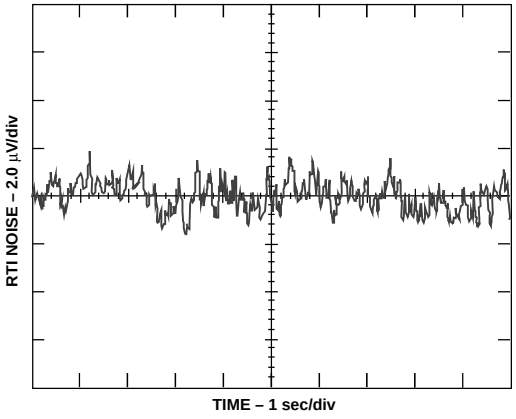


Figure 8a. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

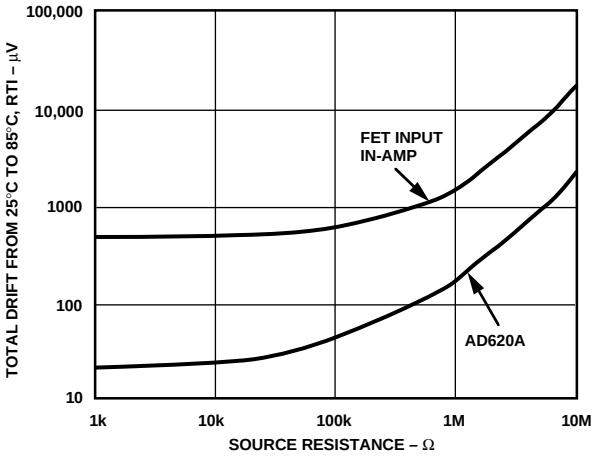


Figure 10. Total Drift vs. Source Resistance

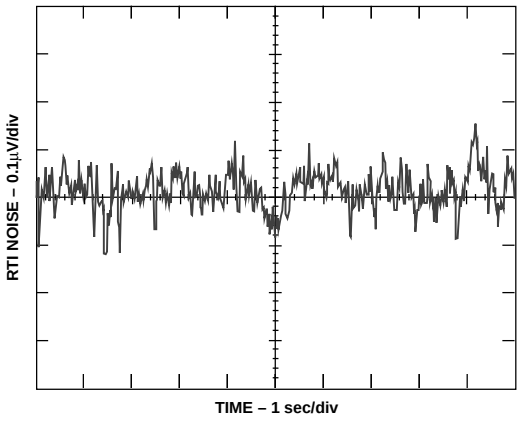


Figure 8b. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

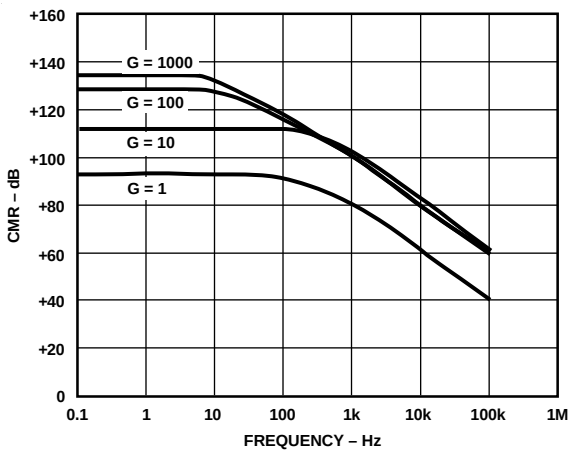


Figure 11. CMR vs. Frequency, RTI, Zero to 1 kΩ Source Imbalance

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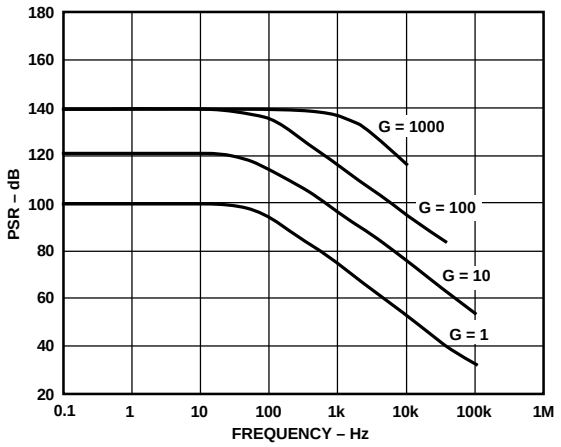


Figure 12. Positive PSR vs. Frequency, RTI (G = 1–1000)

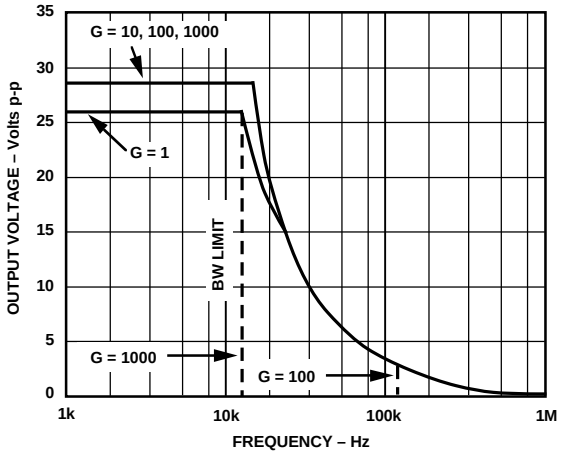


Figure 15. Large Signal Frequency Response

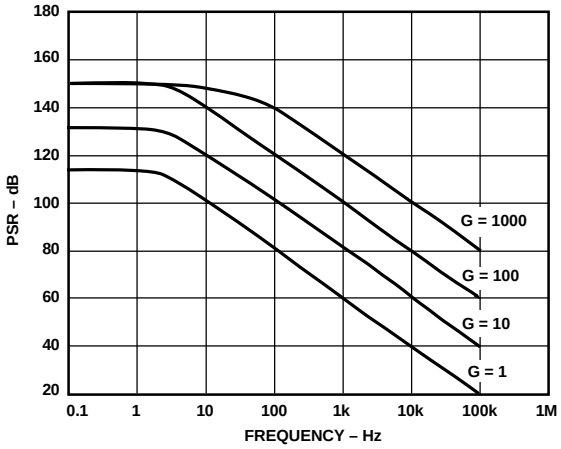


Figure 13. Negative PSR vs. Frequency, RTI (G = 1–1000)

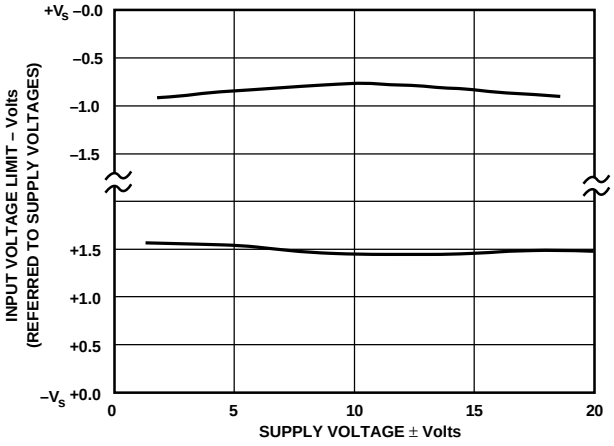


Figure 16. Input Voltage Range vs. Supply Voltage, G = 1

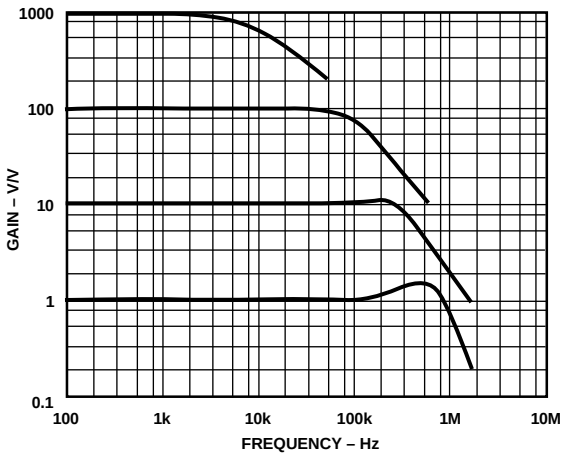


Figure 14. Gain vs. Frequency

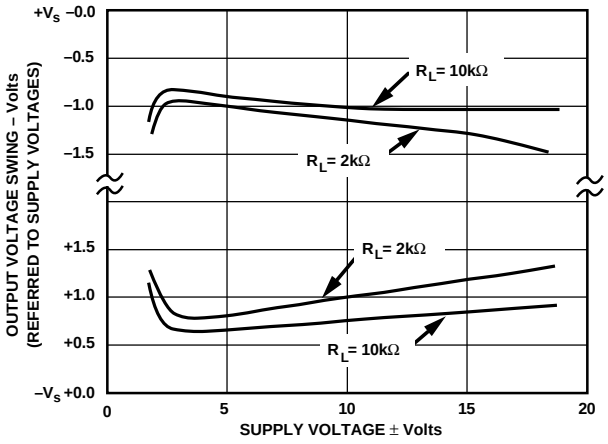


Figure 17. Output Voltage Swing vs. Supply Voltage, G = 10

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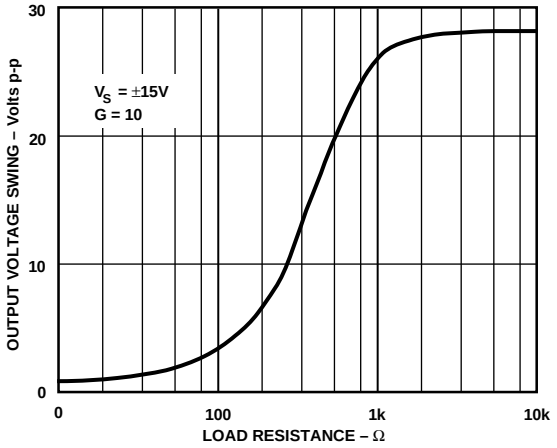


Figure 18. Output Voltage Swing vs. Load Resistance

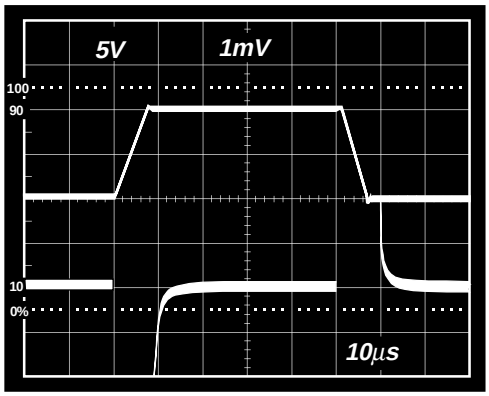


Figure 21. Large Signal Response and Settling Time, G = 10 (0.5 mV = 001%)

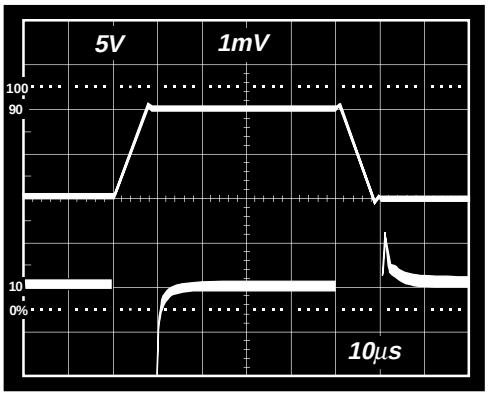


Figure 19. Large Signal Pulse Response and Settling Time G = 1 (0.5 mV = 0.01%)

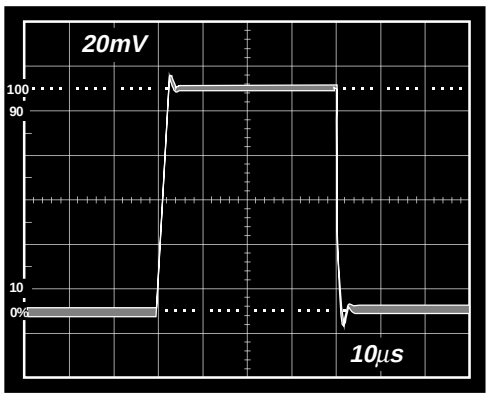


Figure 22. Small Signal Response, G = 10, R_L = 2 kΩ, C_L = 100 pF

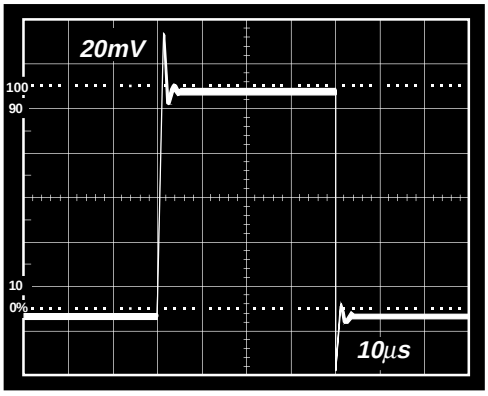


Figure 20. Small Signal Response, G = 1, R_L = 2 kΩ, C_L = 100 pF

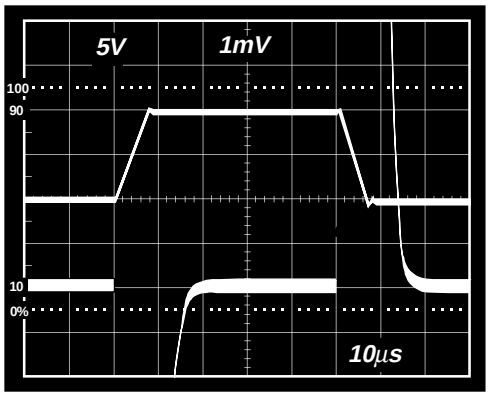


Figure 23. Large Signal Response and Settling Time, G = 100 (0.5 mV = 0.01%)

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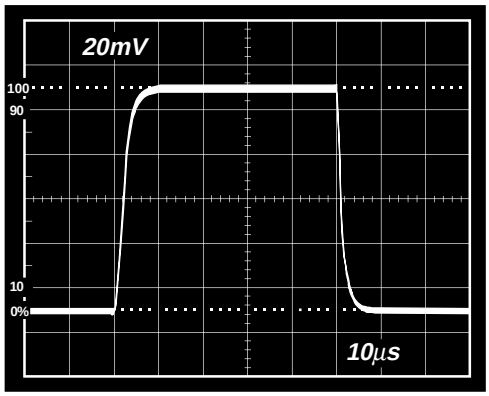


Figure 24. Small Signal Pulse Response, G = 100, R_L = 2 kΩ, CL = 100 pF

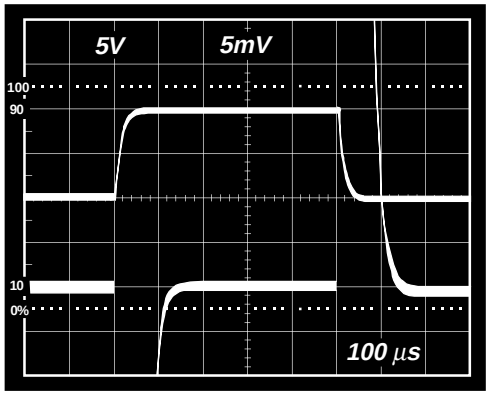


Figure 25. Large Signal Response and Settling Time, G = 1000 (0.5 mV = 0.01%)

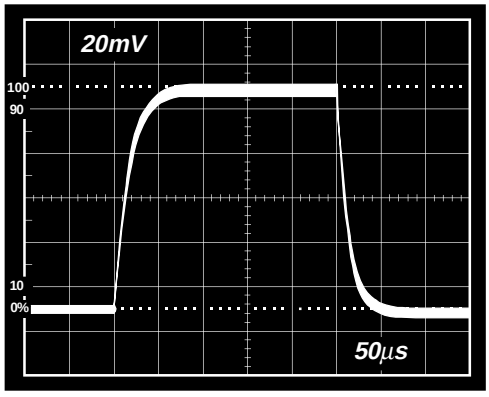


Figure 26. Small Signal Pulse Response, G = 1000, R_L = 2 kΩ, CL = 100 pF

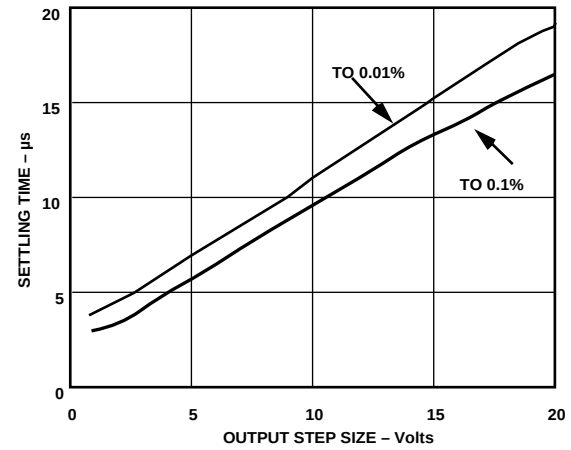


Figure 27. Settling Time vs. Step Size (G = 1)

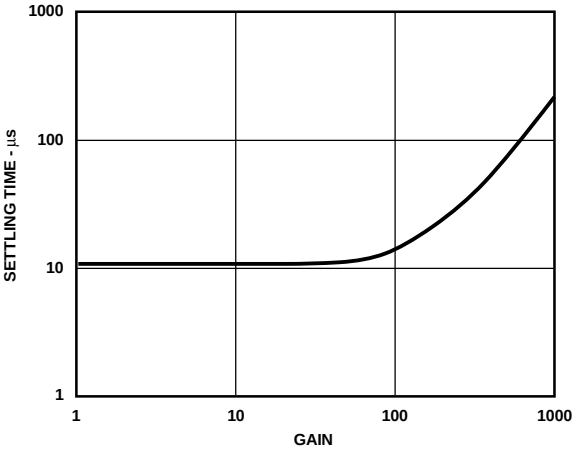


Figure 28. Settling Time to 0.01% vs. Gain, for a 10 V Step

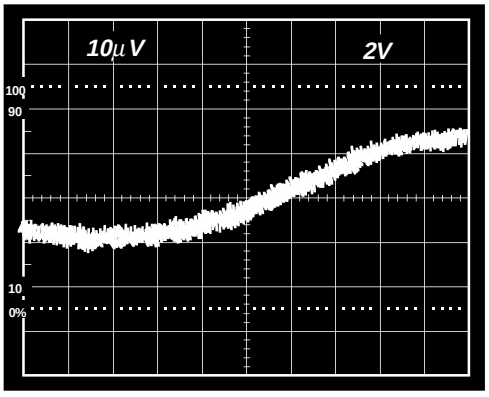


Figure 29a. Gain Nonlinearity, G = 1, R_L = 10 kΩ (10 µV = 1 ppm)

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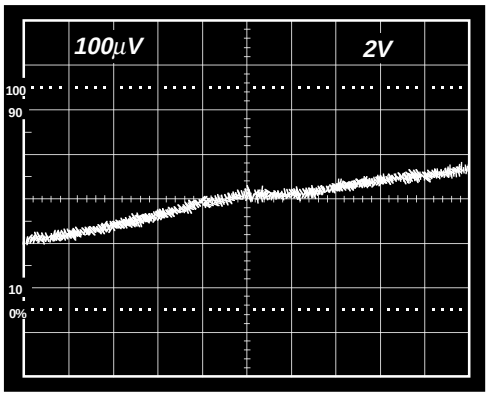


Figure 29b. Gain Nonlinearity, G = 100, R_L = 10 kΩ (100 μV = 10 ppm)

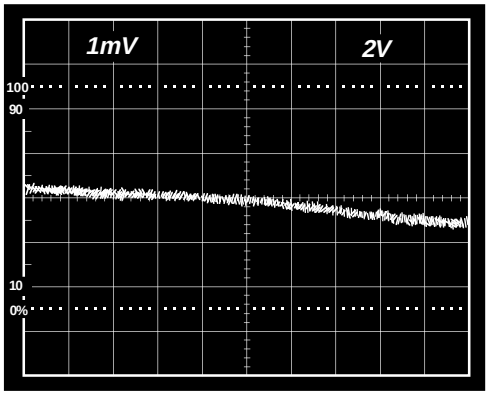


Figure 29c. Gain Nonlinearity, G = 1000, R_L = 10 kΩ (1 mV = 100 ppm)

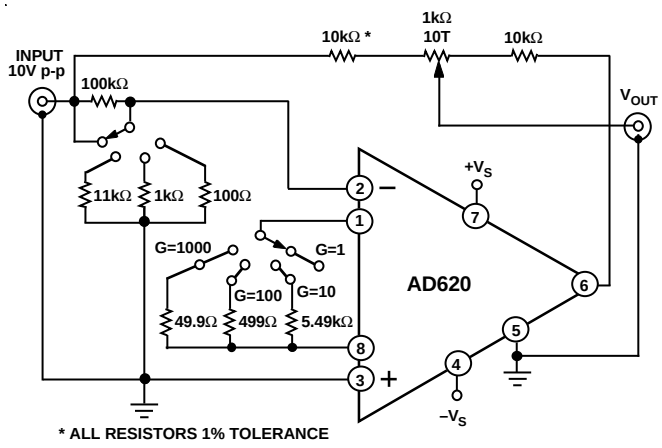


Figure 30. Settling Time Test Circuit

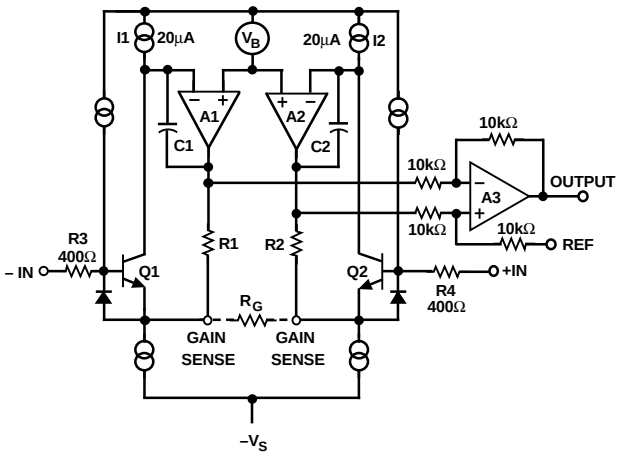


Figure 31. Simplified Schematic of AD620

THEORY OF OPERATION

The AD620 is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* (to 0.15% at G = 100) with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus insuring the high level of performance inherent in this circuit.

The input transistors Q1 and Q2 provide a single differential-pair bipolar input for high precision (Figure 31), yet offer 10× lower Input Bias Current thanks to Superβeta processing. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains constant collector current of the input devices Q1, Q2 thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by G = (R1 + R2)/R_G + 1. The unity-gain subtracter A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: (a) Open-loop gain is boosted for increasing programmed gain, thus reducing gain-related errors. (b) The gain-bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing frequency response. (c) The input voltage noise is reduced to a value of 9 nV/$\sqrt{\text{Hz}}$, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

The gain equation is then

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

so that

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

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Make vs. Buy: A Typical Bridge Application Error Budget

The AD620 offers improved performance over "homebrew" three op amp IA designs, along with smaller size, less components and 10× lower supply current. In the typical application, shown in Figure 32, a gain of 100 is required to amplify a bridge output of 20 mV full scale over the industrial temperature range of –40°C to +85°C. The error budget table below shows how to calculate the effect various error sources have on circuit accuracy.

Regardless of the system it is being used in, the AD620 provides greater accuracy, and at low power and price. In simple systems, absolute accuracy and drift errors are by far the most significant contributors to error. In more complex systems with an intelligent processor, an auto-gain/auto-zero cycle will remove all absolute accuracy and drift errors leaving only the resolution errors of gain nonlinearity and noise, thus allowing full 14-bit accuracy.

Note that for the homebrew circuit, the OP07 specifications for input voltage offset and noise have been multiplied by $\sqrt{2}$. This is because a three op amp type in amp has two op amps at its inputs, both contributing to the overall input error.

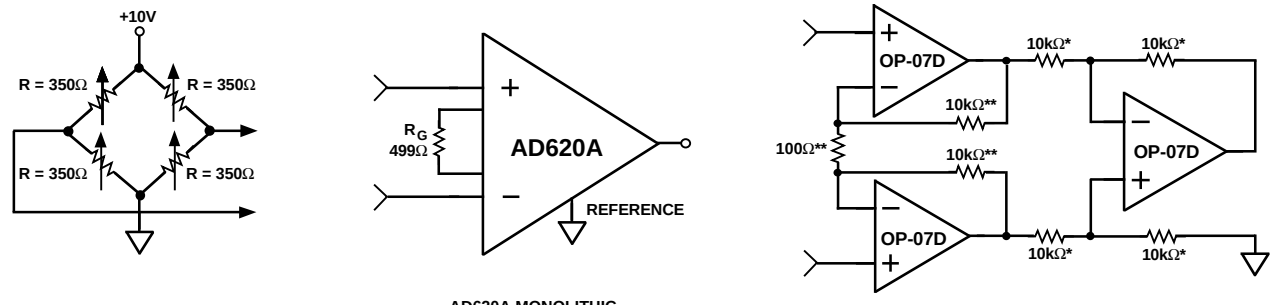


Figure 32. Make vs. Buy

Table I. Make vs. Buy Error Budget

Error Source	AD620 Circuit Calculation	"Homebrew" Circuit Calculation	Error, ppm of Full Scale AD620	Homebrew
ABSOLUTE ACCURACY at T_A = +25°C				
Input Offset Voltage, µV	125 µV/20 mV	(150 µV × $\sqrt{2}$)/20 mV	6,250	10,607
Output Offset Voltage, µV	1000 µV/100/20 mV	((150 µV × 2)/100)/20 mV	500	150
Input Offset Current, nA	2 nA × 350 Ω/20 mV	(6 nA × 350 Ω)/20 mV	18	53
CMR, dB	110 dB→3.16 ppm, × 5 V/20 mV	(0.02% Match × 5 V)/20 mV/100	791	500
		Total Absolute Error	7,558	11,310
DRIFT TO +85°C				
Gain Drift, ppm/°C	(50 ppm + 10 ppm) × 60°C	100 ppm/°C Track × 60°C	3,600	6,000
Input Offset Voltage Drift, µV/°C	1 µV/°C × 60°C/20 mV	(2.5 µV/°C × $\sqrt{2}$ × 60°C)/20 mV	3,000	10,607
Output Offset Voltage Drift, µV/°C	15 µV/°C × 60°C/100/20 mV	(2.5 µV/°C × 2 × 60°C)/100/20 mV	450	150
		Total Drift Error	7,050	16,757
RESOLUTION				
Gain Nonlinearity, ppm of Full Scale	40 ppm	40 ppm	40	40
Typ 0.1 Hz–10 Hz Voltage Noise, µV p-p	0.28 µV p-p/20 mV	(0.38 µV p-p × $\sqrt{2}$)/20 mV	14	27
		Total Resolution Error	54	67
		Grand Total Error	14,662	28,134

G = 100, V_S = ±15 V.

(All errors are min/max and referred to input.)

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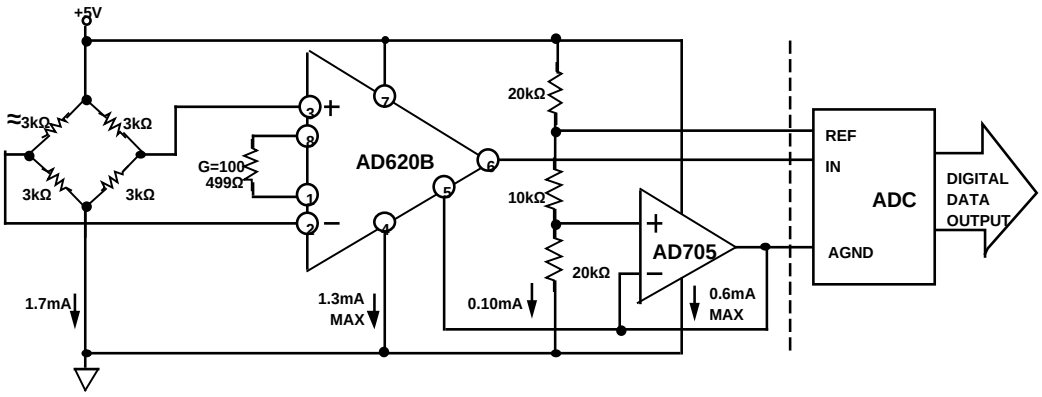


Figure 33. A Pressure Monitor Circuit which Operates on a +5 V Single Supply

Pressure Measurement

Although useful in many bridge applications such as weigh scales, the AD620 is especially suited for higher resistance pressure sensors powered at lower voltages where small size and low power become more significant.

Figure 33 shows a 3 kΩ pressure transducer bridge powered from +5 V. In such a circuit, the bridge consumes only 1.7 mA. Adding the AD620 and a buffered voltage divider allows the signal to be conditioned for only 3.8 mA of total supply current.

Small size and low cost make the AD620 especially attractive for voltage output pressure transducers. Since it delivers low noise and drift, it will also serve applications such as diagnostic non-invasive blood pressure measurement.

Medical ECG

The low current noise of the AD620 allows its use in ECG monitors (Figure 34) where high source resistances of 1 MΩ or higher are not uncommon. The AD620's low power, low supply voltage requirements, and space-saving 8-pin mini-DIP and SOIC package offerings make it an excellent choice for battery powered data recorders.

Furthermore, the low bias currents and low current noise coupled with the low voltage noise of the AD620 improve the dynamic range for better performance.

The value of capacitor C1 is chosen to maintain stability of the right leg drive loop. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

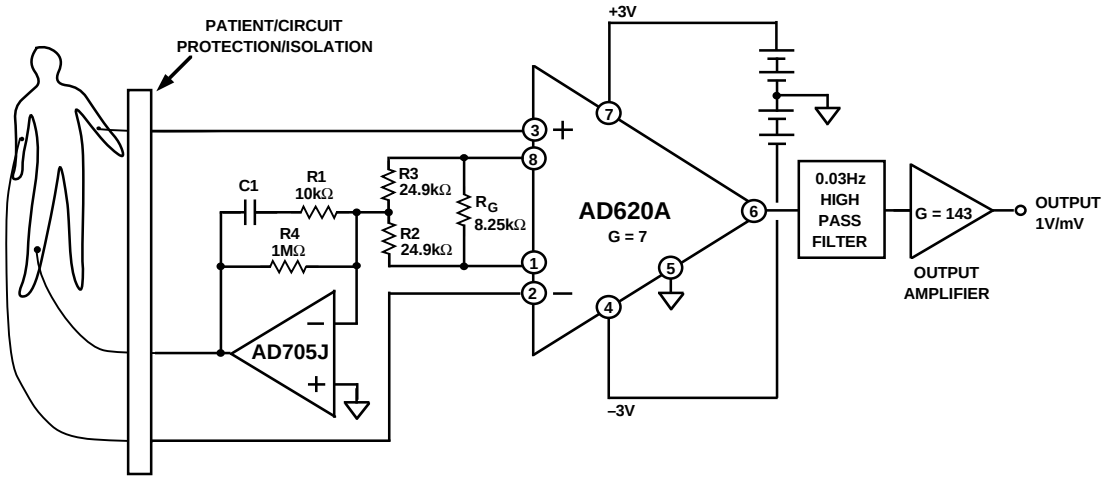


Figure 34. A Medical ECG Monitor Circuit

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Precision V-I Converter

The AD620 along with another op amp and two resistors make a precision current source (Figure 35). The op amp buffers the reference terminal to maintain good CMR. The output voltage V_X of the AD620 appears across R1 which converts it to a current. This current less only the input bias current of the op amp then flows out to the load.

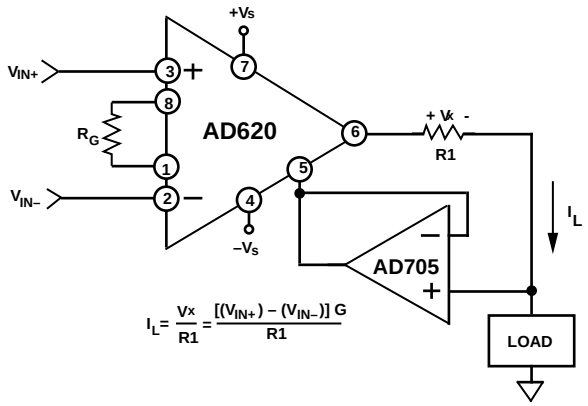


Figure 35. Precision Voltage-to-Current Converter (Operates on 1.8 mA, ±3 V)

GAIN SELECTION

The AD620's gain is resistor programmed by R_G: or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620 is designed to offer accurate gains using 0.1%–1% resistors. Table II shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain R_G can be calculated by using the formula:

$$R_G = \frac{49.4\ k\Omega}{G-1}$$

To minimize gain error avoid high parasitic resistance in series with R_G, and to minimize gain drift R_G should have a low TC—less than 10 ppm/°C for the best performance.

Table II. Required Values of Gain Resistors

1% Std Table Value of R_G, Ω	Calculated Gain	0.1% Std Table Value of R_G, Ω	Calculated Gain
49.9 k	1.990	49.3 k	2.002
12.4 k	4.984	12.4 k	4.984
5.49 k	9.998	5.49 k	9.998
2.61 k	19.93	2.61 k	19.93
1.00 k	50.40	1.01 k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003

INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620 are attributed to two sources, input and output errors. The output error is divided by G when referred to the input. In practice, the input errors dominate at high gains and the output errors dominate at low gains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error/G)

Total Error RTO = (input error × G) + output error

REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage, and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

INPUT PROTECTION

The AD620 features 400 Ω of series thin film resistance at its inputs, and will safely withstand input overloads of up to ±15 V or ±60 mA for several hours. This is true for all gains, and power on and off, which is particularly important since the signal source and amplifier may be powered separately. For longer time periods, the current should not exceed 6 mA ($I_{IN} \le V_{IN}/400\ \Omega$). For input overloads beyond the supplies, clamping the inputs to the supplies (using a low leakage diode such as an FD333) will reduce the required resistance, yielding lower noise.

RF INTERFERENCE

All instrumentation amplifiers can rectify out of band signals, and when amplifying small signals, these rectified voltages act as small dc offset errors. The AD620 allows direct access to the input transistor bases and emitters enabling the user to apply some first order filtering to unwanted RF signals (Figure 36), where RC ≈ 1/(2 πf) and where f ≥ the bandwidth of the AD620; C ≤ 150 pF. Matching the extraneous capacitance at Pins 1 and 8, and Pins 2 and 3 helps to maintain high CMR.

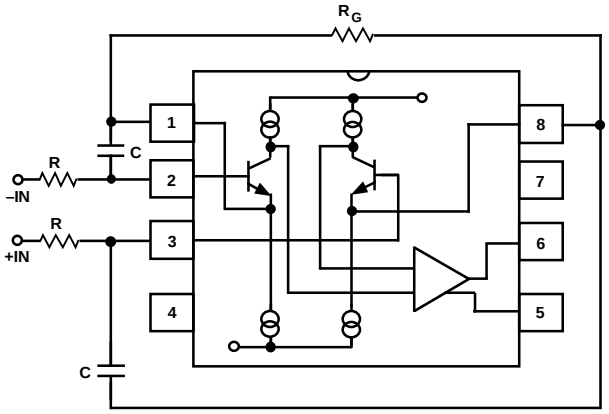


Figure 36. Circuit to Attenuate RF Interference

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COMMON-MODE REJECTION

Instrumentation amplifiers like the AD620 offer high CMR which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications shielded cables are used to minimize noise, and for best CMR over frequency the shield should be properly driven. Figures 37 and 38 show active data guards which are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

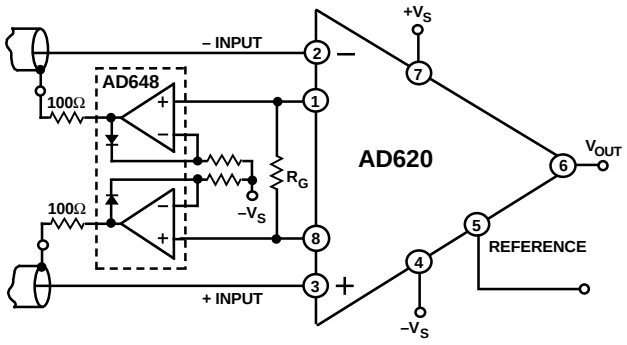


Figure 37. Differential Shield Driver

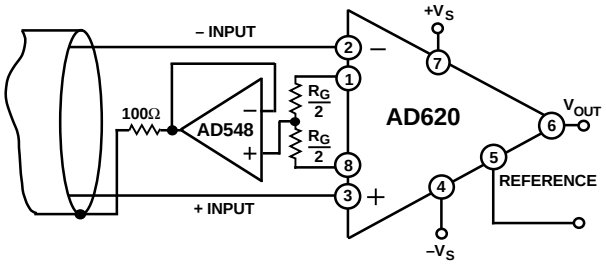


Figure 38. Common-Mode Shield Driver

GROUNDING

Since the AD620 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems by simply tying the REF pin to the appropriate "local ground."

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have separate analog and digital ground pins (Figure 39). It would be convenient to use a single ground line, however, current through ground wires and PC runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground. These ground returns must be tied together at some point, usually best at the ADC package as shown.

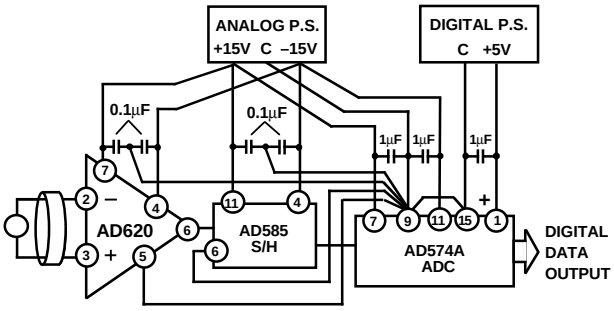


Figure 39. Basic Grounding Practice

GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path

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for these currents; therefore when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 40. Refer to the *Instrumentation Amplifier Application Guide* (free from Analog Devices) for more information regarding in amp applications.

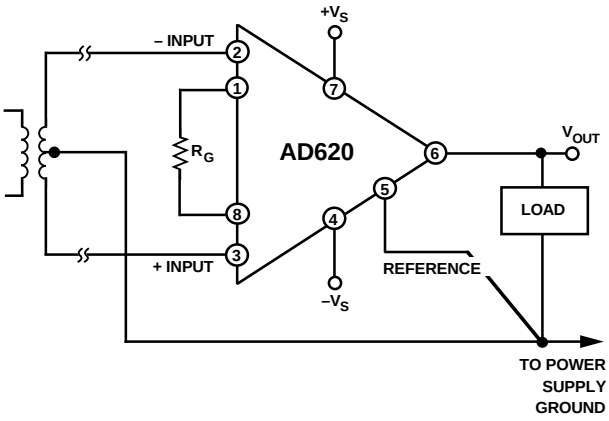


Figure 40a. Ground Returns for Bias Currents with Transformer Coupled Inputs

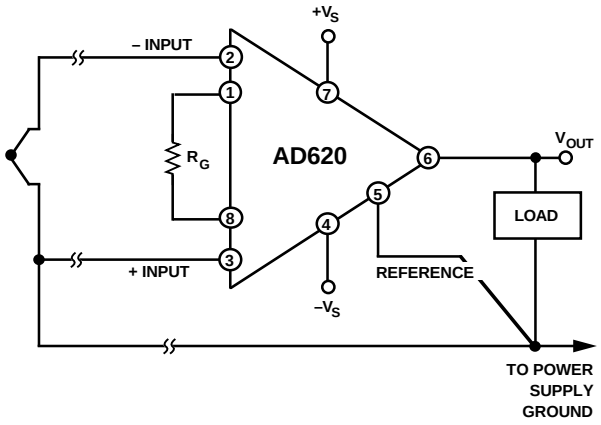


Figure 40b. Ground Returns for Bias Currents with Thermocouple Inputs

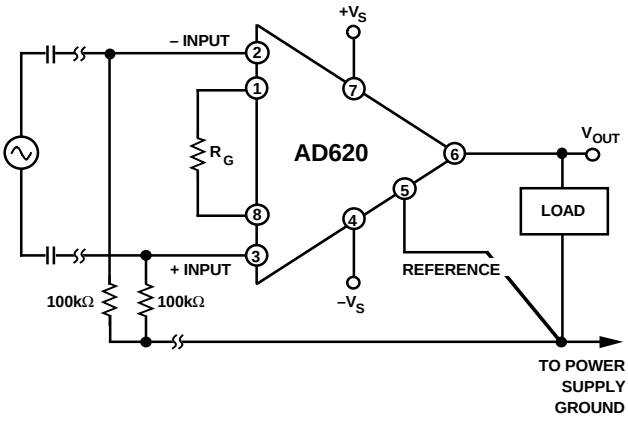


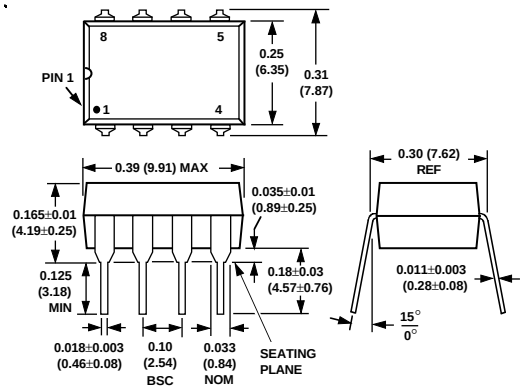
Figure 40c. Ground Returns for Bias Currents with AC Coupled Inputs

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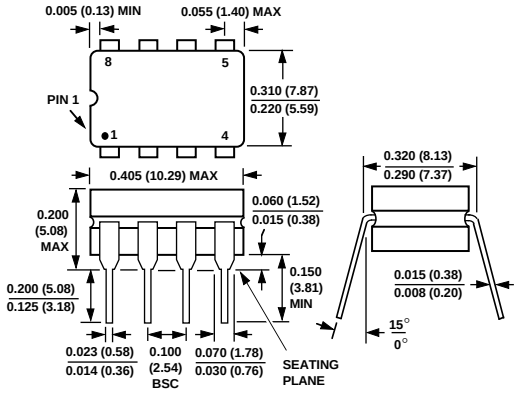
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

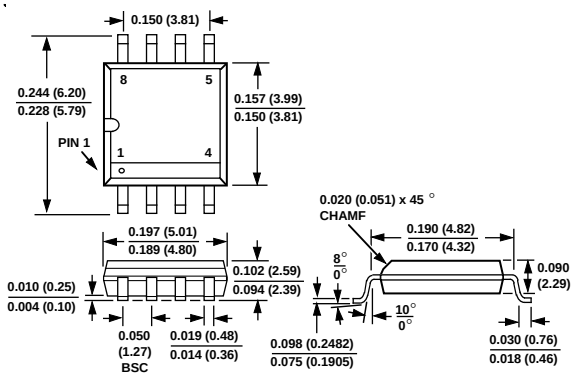
Plastic DIP (N-8) Package



Cerdip (Q-8) Package



SOIC (R-8) Package



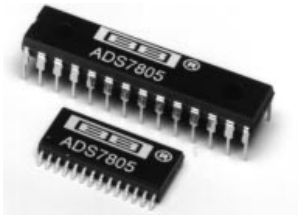
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ADS7805

DEMO BOARD AVAILABLE
See Appendix A

16-Bit 10μs Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

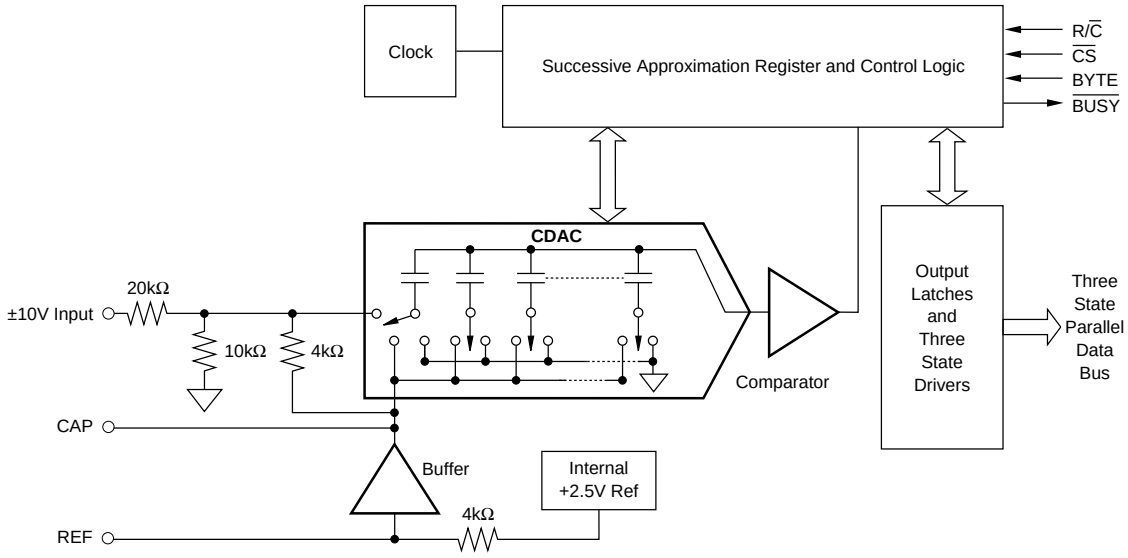
- **100kHz min SAMPLING RATE**
- **STANDARD ±10V INPUT RANGE**
- **86dB min SINAD WITH 20kHz INPUT**
- **±3.0 LSB max INL**
- **DNL: 16-bits "No Missing Codes"**
- **SINGLE +5V SUPPLY OPERATION**
- **PIN-COMPATIBLE WITH 12-BIT ADS7804**
- **USES INTERNAL OR EXTERNAL REFERENCE**
- **FULL PARALLEL DATA OUTPUT**
- **100mW max POWER DISSIPATION**
- **28-PIN 0.3" PLASTIC DIP AND SOIC**

DESCRIPTION

The ADS7805 is a complete 16-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, SAR A/D with S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7805 is specified at a 100kHz sampling rate, and guaranteed over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range, while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The 28-pin ADS7805 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –25°C to +85°C range.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT								
Voltage Ranges			±10V			*		V
Impedance			23			*		kΩ
Capacitance			35			*		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			10			*	µs
Throughput Rate		100			*			kHz
DC ACCURACY								
Integral Linearity Error				±4			±3	LSB[1]
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			*		LSB
Full Scale Error[3,4]				±0.5			±0.25	%
Full Scale Error Drift			±7			±5		ppm/°C
Full Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full Scale Error Drift	Ext. 2.5000V Ref		±2			*		ppm/°C
Bipolar Zero Error[3]				±10			*	mV
Bipolar Zero Error Drift			±2			*		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8			*	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 20kHz	90			94			dB[5]
Total Harmonic Distortion	f_{IN} = 20kHz			–90			–94	dB
Signal-to-(Noise+Distortion)	f_{IN} = 20kHz	83			86			dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 20kHz	83			86			dB
Full-Power Bandwidth[6]			250			*		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			*		ns
Transient Response	FS Step			2			*	µs
Overvoltage Recovery[7]			150			*		ns
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	*	*	*	V
Internal Reference Source Current (Must use external buffer.)			1			*		µA
Internal Reference Drift			8			*		ppm/°C
External Reference Voltage Range for Specified Linearity		2.3	2.5	2.7	*	*	*	V
External Reference Current Drain	Ext. 2.5000V Ref			100			*	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	*		*	V
V_{IH}		+2.0		V_D +0.3V	*		*	V
I_{IL}				±10			*	µA
I_{IH}				±10			*	µA
DIGITAL OUTPUTS								
Data Format				Parallel 16-bits				
Data Coding				Binary Two's Complement				
V_{OL}	I_{SINK} = 1.6mA			+0.4			*	V
V_{OH}	I_{SOURCE} = 500µA	+4			*			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			*	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			*	ns
Bus Relinquish Time				83			*	ns

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

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SPECIFICATIONS (CONT)

ELECTRICAL

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	*	*	*	V
V_{ANA}		+4.75	+5	+5.25	*	*	*	V
I_{DIG}			0.3			*		mA
I_{ANA}			16			*		mA
Power Dissipation	f_S = 100kHz			100			*	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	*		*	°C
Derated Performance		–55		+125	*		*	°C
Storage		–65		+150	*		*	°C
Thermal Resistance (θ_{JA})								
Plastic DIP			75			*		°C/W
SOIC			75			*		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7805, one LSB is 305µV. (2) Typical rms noise at worst case transitions and temperatures. (3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale ±10V input. (6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy. (7) Recovers to specified performance after 2 x FS input overvoltage.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN} ..... ±25V
CAP ..... $+V_{ANA}$ +0.3V to AGND2 –0.3V
REF ..... Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2 ..... ±0.3V
V_{ANA} 7V
V_{DIG} to V_{ANA} ..... +0.3V
V_{DIG} 7V
Digital Inputs ..... –0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature ..... +165°C
Internal Power Dissipation 825mW
Lead Temperature (soldering, 10s) ..... +300°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ADS7805P	Plastic DIP	246
ADS7805PB	Plastic DIP	246
ADS7805U	SOIC	217
ADS7805UB	SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ADS7805P	±4	83	–25°C to +85°C	Plastic DIP
ADS7805PB	±3	86	–25°C to +85°C	Plastic DIP
ADS7805U	±4	83	–25°C to +85°C	SOIC
ADS7805UB	±3	86	–25°C to +85°C	SOIC

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

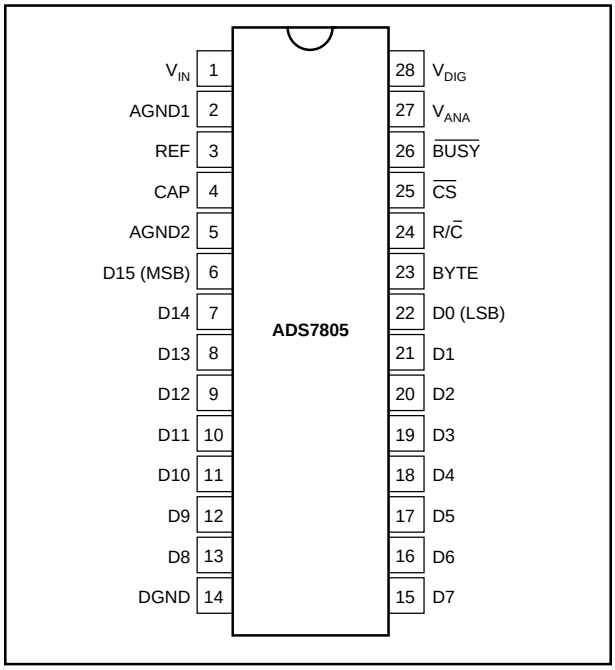
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. See Figure 7.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground.
6	D15 (MSB)	O	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground.
15	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	Data Bit 0. Lease Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a New Conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be ≤ V_{ANA}.

TABLE I. Pin Assignments.

PIN CONFIGURATION

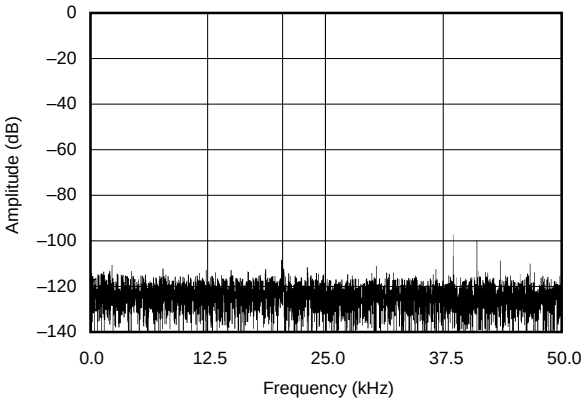


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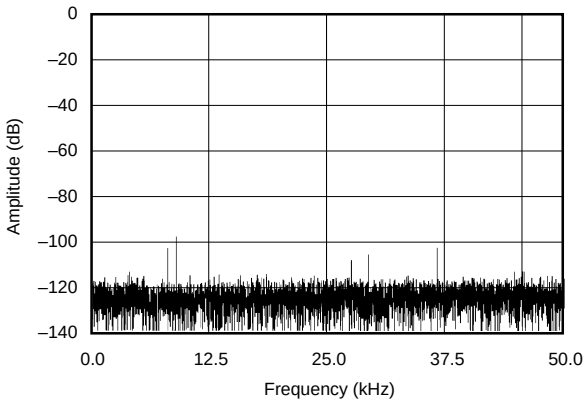
TYPICAL PERFORMANCE CURVES

T_A = +25°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 6b, unless otherwise specified.

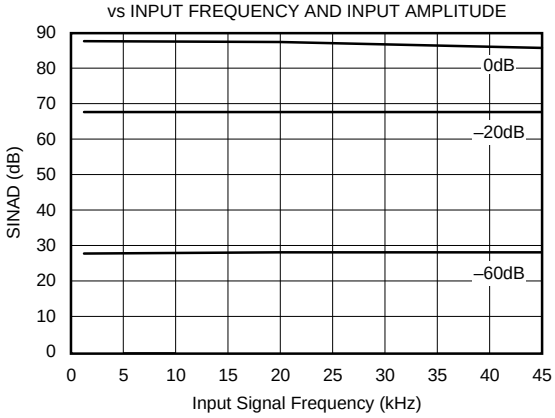
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 20kHz, 0dB)



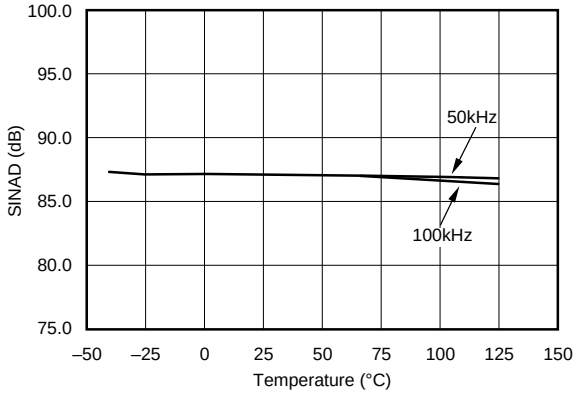
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 45kHz, 0dB)



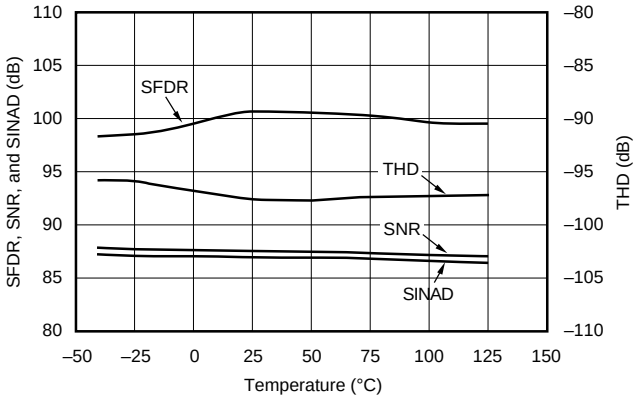
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE

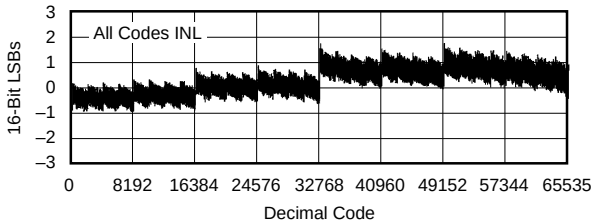


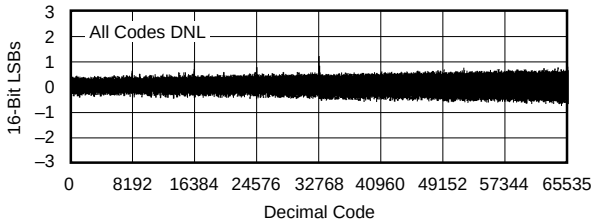
SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 20kHz, 0dB; f_S = 50kHz, 100kHz)



A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 20kHz, 0dB)



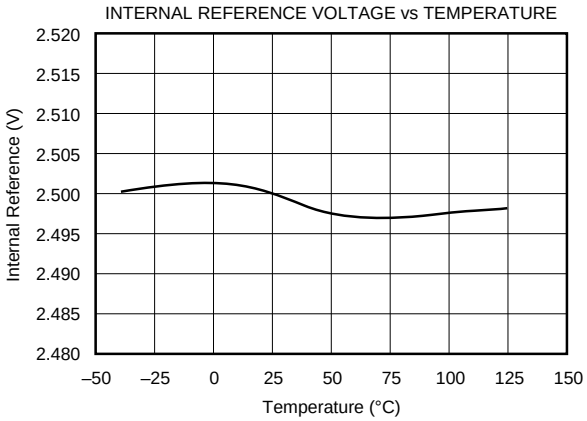


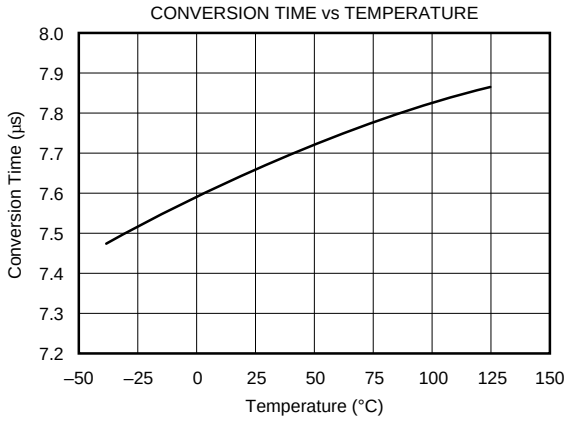


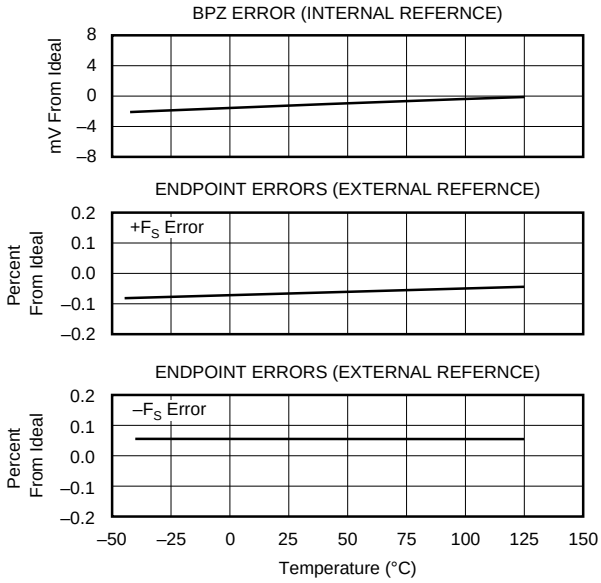
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TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 6b, unless otherwise specified.







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BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7805 with a full parallel data output. Taking R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns (7µs max) will initiate a conversion. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 25) and R/$\overline{C}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7805 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. $\overline{CS}$ and/or R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 3 through 5 for timing diagrams.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{CS}$ or R/$\overline{C}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output will become active whenever R/$\overline{C}$ goes HIGH. Refer to the **Reading Data** section.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{CS}$ and/or R/$\overline{C}$ must be HIGH when $\overline{BUSY}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 3 and 4 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".

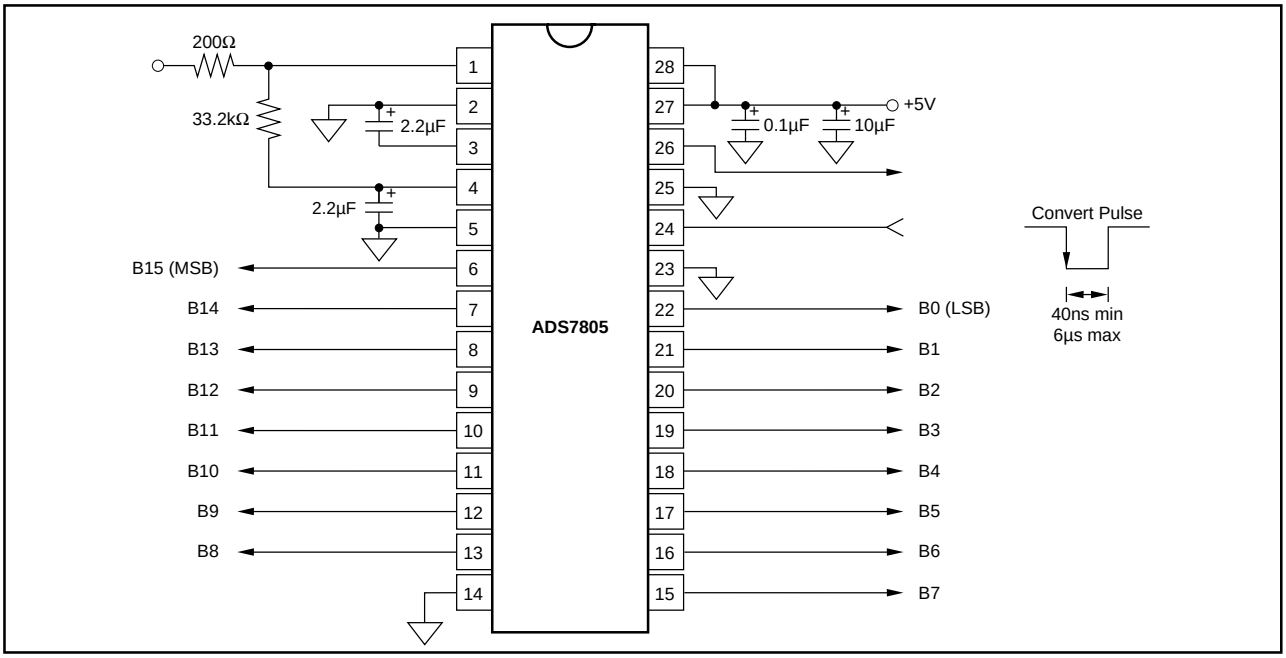


FIGURE 1. Basic Operation.

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READING DATA

The ADS7805 outputs full or byte-reading parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full Scale Range	±10V		
Least Significant Bit (LSB)	305µV		
+Full Scale (10V – 1LSB)	9.999695V	0111 1111 1111 1111	7FFF
Midscale	0V	0000 0000 0000 0000	0000
One LSB below Midscale	–305µV	1111 1111 1111 1111	FFFF
–Full Scale	–10V	1000 0000 0000 0000	8000

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D15-D0 (pin 6-13 and 15-22). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 and 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n-1' can be read and will be valid up to 7µs after the start of conversion 'n'. Do not attempt to read data from 7µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 and 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 3.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		7000	ns
t_2	Data Valid Delay after R/$\overline{C}$ LOW			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$ LOW			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after R/$\overline{C}$ LOW		7.4		µs
$t_7 + t_6$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

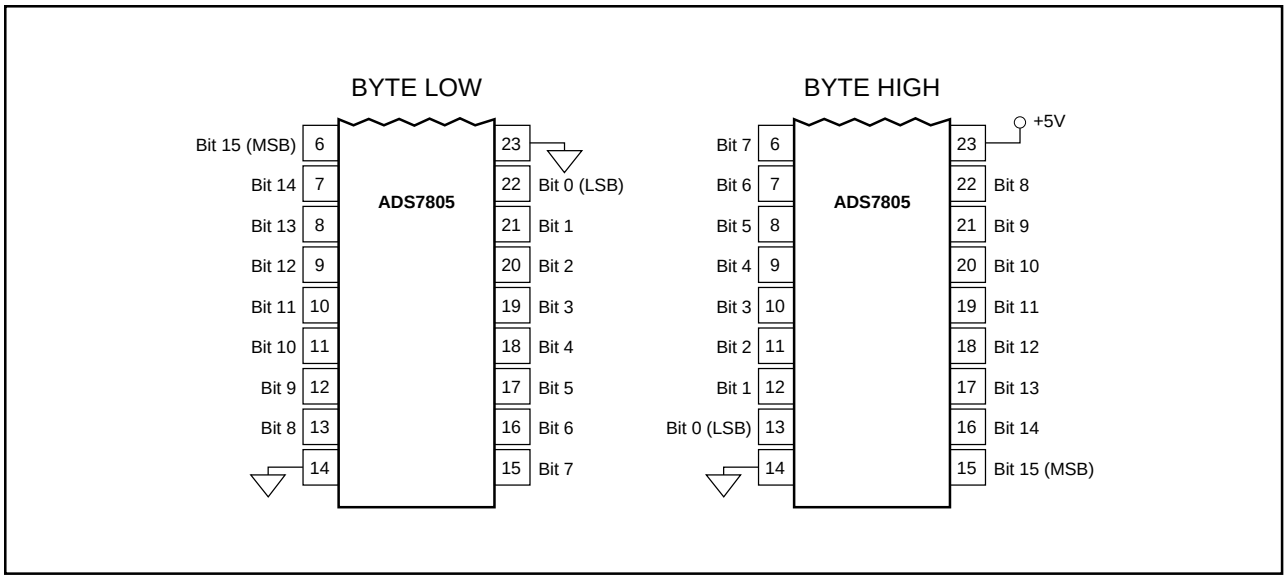


FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

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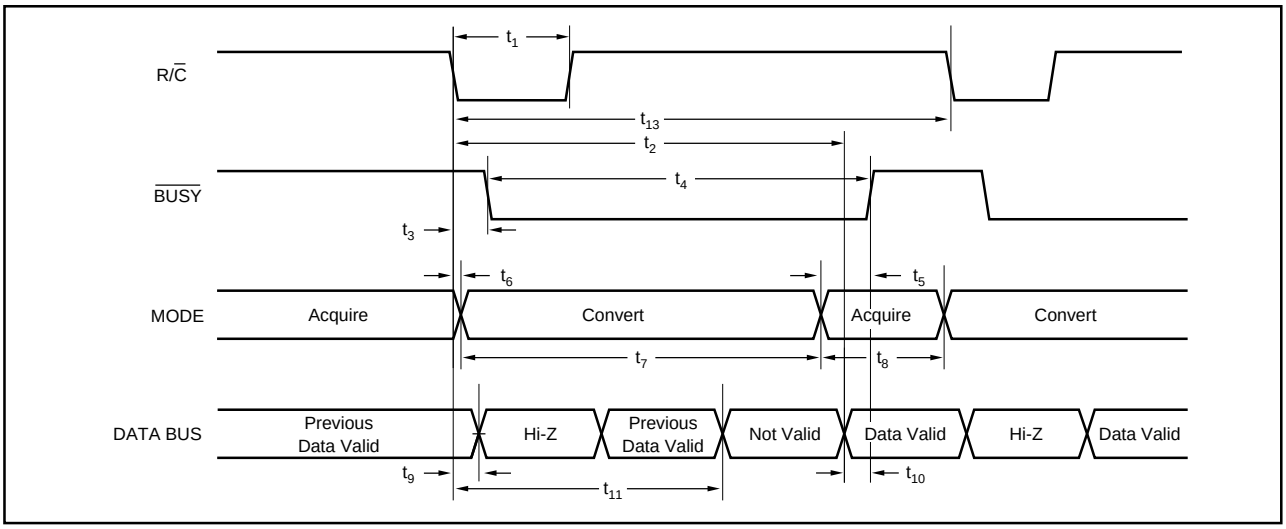


FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW.)

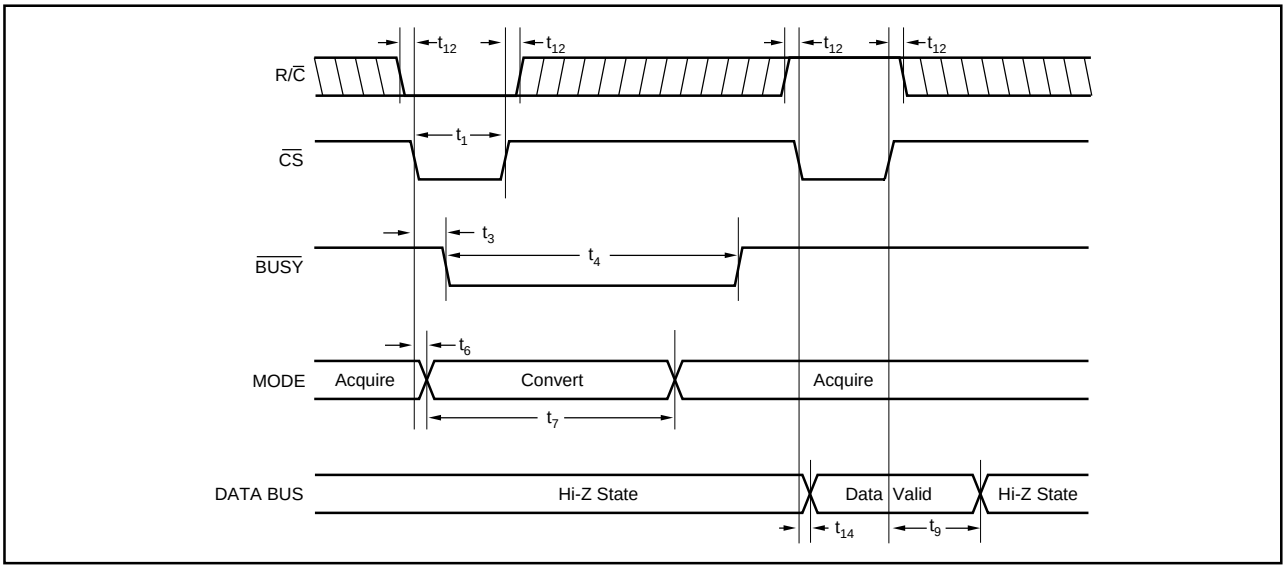


FIGURE 4. Using $\overline{CS}$ to Control Conversion and Read Timing.

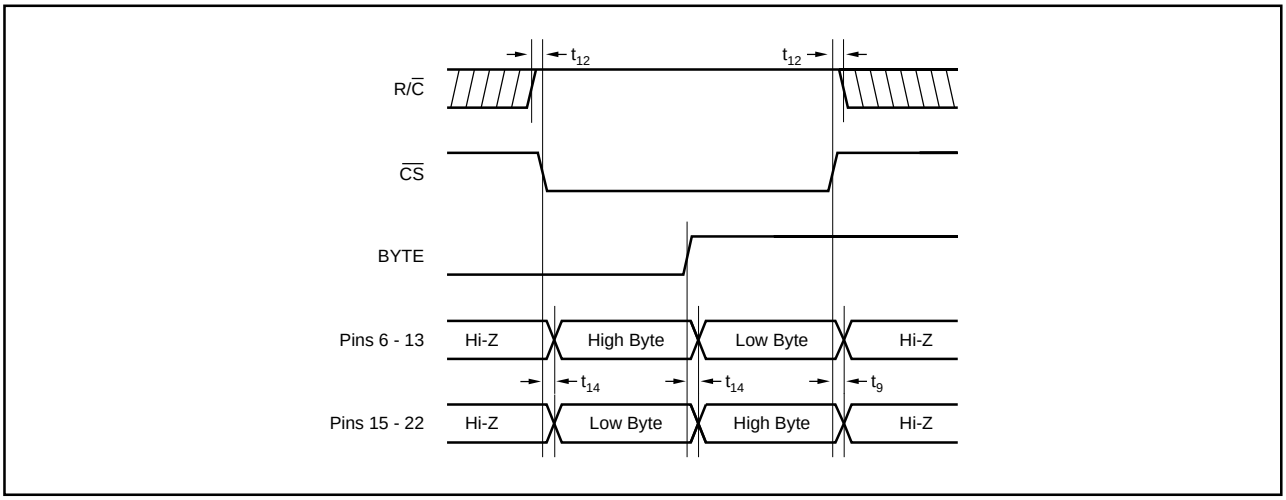


FIGURE 5. Using $\overline{CS}$ and BYTE to Control Data Bus.

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INPUT RANGES

The ADS7805 offers a standard ±10V input range. Figure 6 shows the necessary circuit connections for the ADS7805 with and without hardware trim. Offset and full scale error(1) specifications are tested and guaranteed with the fixed resistors shown in Figure 6b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The nominal input impedance of 23kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection guaranteed to at lease ±25V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

The ADS7805 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7805, install the proper resistors and potentiometers as shown in Figure 6a. The calibration range is ±15mV for the offset and ±60mV for the gain.

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7805 in software, no external resistors are required. See the **No Calibration** section for details on the effects of the external resistors. Refer to Table V for range of offset and gain errors with and without external resistors.

NO CALIBRATION

See Figure 6b for circuit connections. The external resistors shown in Figure 6b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer function of the ADS7805 will be bound by the shaded region seen in Figure 7 with a typical offset of –30mV and a typical gain error of –1.5%. Refer to Table V for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BP0	–10 < BPO < 10 –30 < BPO < 30	–50 < BPO < –15 –150 < BPO < –45	mV LSBs
Gain Error	–0.5 < error < 0.5	–2 < error < –1	% of FSR

TABLE V. Offset and Gain Errors With and Without External Resistors.

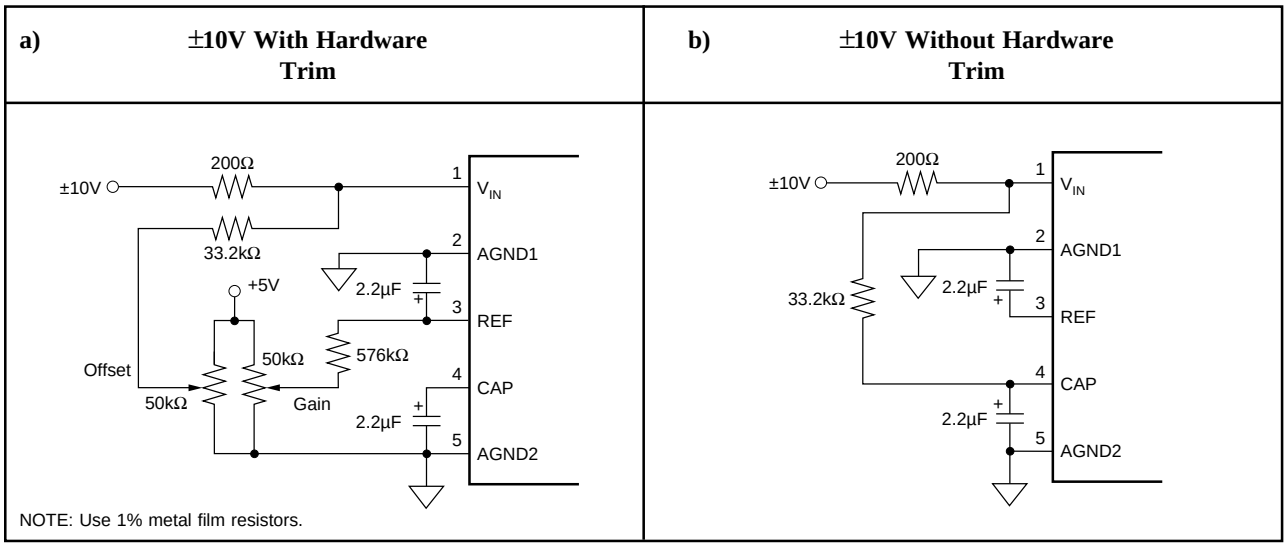


FIGURE 6. Circuit Diagram With and Without External Resistors.

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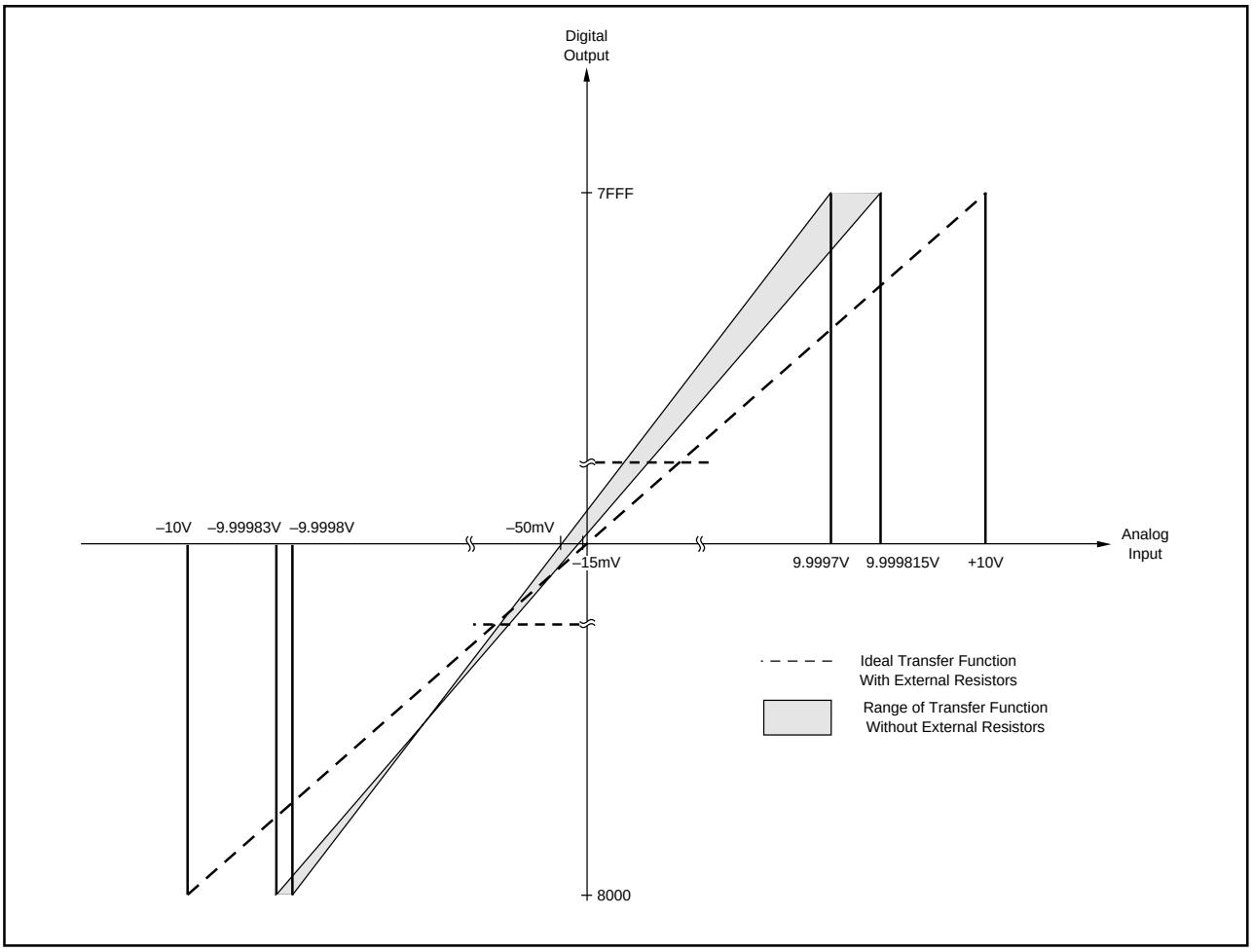


FIGURE 7. Full Scale Transfer Function.

REFERENCE

The ADS7805 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a DC load. DC loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7805. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

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LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7805 uses 90% of its power for the analog circuitry. The ADS7805 should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7805. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7805, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7805.

The resistive front end of the ADS7805 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

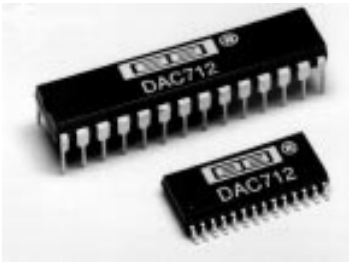
INTERMEDIATE LATCHES

The ADS7805 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus. Tri-state outputs can also be used when the A/D is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7805 has an internal LSB size of 38µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

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DAC712

16-BIT DIGITAL-TO-ANALOG CONVERTER WITH 16-BIT BUS INTERFACE

FEATURES

- HIGH-SPEED 16-BIT PARALLEL DOUBLE-BUFFERED INTERFACE
- VOLTAGE OUTPUT: ±10V
- 13-, 14-, AND 15-BIT LINEARITY GRADES
- 16-BIT MONOTONIC OVER TEMPERATURE (L GRADE)
- POWER DISSIPATION: 600mW max
- GAIN AND OFFSET ADJUST: Convenient for Auto-Cal D/A Converters
- 28-LEAD DIP AND SOIC PACKAGES

DESCRIPTION

DAC712 is a complete 16-bit resolution D/A converter with 16 bits of monotonicity over temperature.

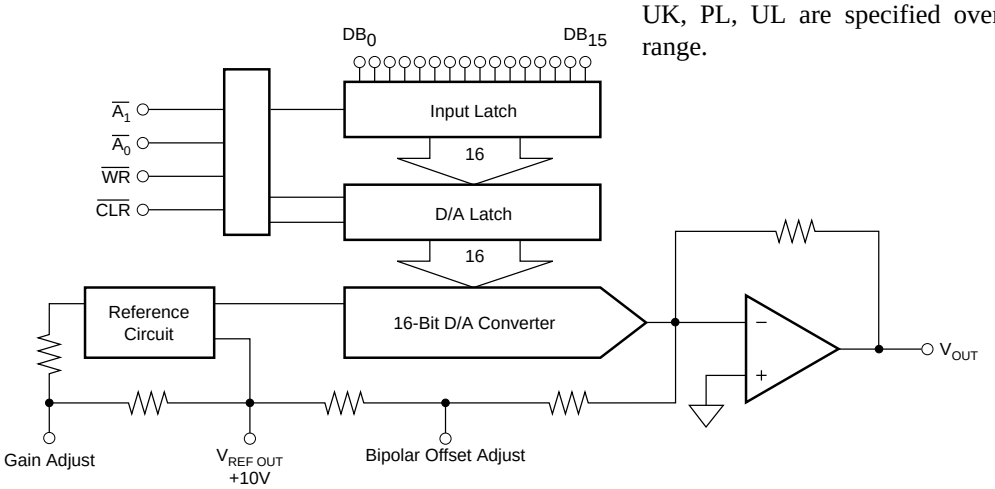
DAC712 has a precision +10V temperature compensated voltage reference, ±10V output amplifier and 16-bit port bus interface.

The digital interface is fast, 60ns minimum write pulse width, is double-buffered and has a CLEAR function that resets the analog output to bipolar zero.

GAIN and OFFSET adjustment inputs are arranged so that they can be easily trimmed by external D/A converters as well as by potentiometers.

DAC712 is available in two linearity error performance grades: ±4LSB and ±2LSB and three differential linearity grades: ±4LSB, ±2LSB, and ±1LSB. The DAC712 is specified at power supply voltages of ±12V and ±15V.

DAC712 is packaged in a 28-pin 0.3" wide plastic DIP and in a 28-lead wide-body plastic SOIC. The DAC712P, U, PB, UB, PC, UC are specified over the –40°C to +85°C temperature range and the DAC712PK, UK, PL, UL are specified over the 0°C to +70°C range.



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Printed in U.S.A. September, 1996

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SPECIFICATIONS

ELECTRICAL

At T_A = 25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = –12V and –15V, unless otherwise noted.

PARAMETER	DAC712P, U			DAC712PB, UB			DAC712PC, UC			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT										
RESOLUTION		16			*			*		Bits
DIGITAL INPUTS										
Input Code	Binary Two's Complement				*			*		
Logic Levels[1]										
V_{IH}	+2.0		$+V_{CC}$ – 1.4	*		*	*		*	V
V_{IL}	0		+0.8	*		*	*		*	V
I_{IH} (V_I = +2.7V)			±10			*			*	µA
I_{IL} (V_I = +0.4V)			±10			*			*	µA
TRANSFER CHARACTERISTICS										
ACCURACY										
Linearity Error			±4			±2			±2	LSB
T_{MIN} to T_{MAX}			±8			±4			±2	LSB
Differential Linearity Error			±4			±2			±1	LSB
T_{MIN} to T_{MAX}			±8			±4			±2	LSB
Monotonicity Over Temp	13			14			15			Bits
Gain Error[3]			±0.1			±0.1			*	%
T_{MIN} to T_{MAX}			±0.2			±0.15			*	%
Bipolar Zero Error[3]			±0.1			*			*	% FSR[2]
			±20			*			*	mV
T_{MIN} to T_{MAX}			±0.2			±0.15			*	% FSR
			±40			±30			*	mV
Power Supply Sensitivity Of Full Scale:			±0.003			*			*	% FSR/% V_{CC}
			±30			*			*	ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE										
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)[4]										
20V Output Step		6			*	10		*	*	µs
1 LSB Output Step[5]		4			*			*		µs
Output Slew Rate		10			*			*		V/µs
Total Harmonic Distortion + Noise										
0dB, 1001Hz, f_S = 100kHz		0.005			*			*		%
–20dB, 1001Hz, f_S = 100kHz		0.03			*			*		%
–60dB, 1001Hz, f_S = 100kHz		3.0			*			*		%
SINAD										
1001Hz, f_S = 100kHz		87			*			*		dB
Digital Feedthrough[5]		2			*			*		nV-s
Digital-to-Analog Glitch Impulse[5]		15			*			*		nV-s
Output Noise Voltage (Includes Reference)		120			*			*		nV/√Hz
ANALOG OUTPUT										
Output Voltage Range										
$+V_{CC}$, $-V_{CC}$ = ±11.4V	±10			*			*			V
Output Current	±5			*			*			mA
Output Impedance		0.1			*			*		Ω
Short Circuit to ACOM, Duration		Indefinite			*			*		
REFERENCE VOLTAGE										
Voltage	+9.975	+10.000	+10.025	*	*	*	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	*		*	V
Output Resistance		1			*			*		Ω
Source Current	2			*			*			mA
Short Circuit to ACOM, Duration		Indefinite			*			*		
POWER SUPPLY REQUIREMENTS										
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	*	*	*	V
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	*	*	*	V
Current (No Load, ±15V Supplies)										
$+V_{CC}$		13	15		*	*		*	*	mA
$-V_{CC}$		22	25		*	*		*	*	mA
Power Dissipation[6]		525	600		*	*		*	*	mW
TEMPERATURE RANGES										
Specification										
All Grades	–40		+85	*		*	*		*	°C
Storage	–60		+150	*		*	*		*	°C
Thermal Coefficient θ_{JA}										
DIP Package		75			*			*		°C/W
SOIC Package		75			*			*		°C/W

*Specifications are the same as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

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SPECIFICATIONS

ELECTRICAL

At T_A = +25°C, $+V_{CC}$ = +12V and +15V, $-V_{CC}$ = –12V and –15V, unless otherwise noted.

PARAMETER	DAC712PK, UK MIN	DAC712PK, UK TYP	DAC712PK, UK MAX	DAC712PL, UL MIN	DAC712PL, UL TYP	DAC712PL, UL MAX	UNITS
INPUT							
RESOLUTION		16			*		Bits
DIGITAL INPUTS							
Input Code		Binary Two's Complement			*		
Logic Levels[1]							
V_{IH}	+2.0		$+V_{CC}$ – 1.4	*		*	V
V_{IL}	0		+0.8	*		*	V
I_{IH} (V_I = +2.7V)			±10			*	µA
I_{IL} (V_I = +0.4V)			±10			*	µA
TRANSFER CHARACTERISTICS							
ACCURACY							
Linearity Error			±2			±2	LSB
T_{MIN} to T_{MAX}			±2			±2	LSB
Differential Linearity Error			±2			±1	LSB
T_{MIN} to T_{MAX}			±2			±1	LSB
Monotonicity Over Temp	15			16			Bits
Gain Error[3]			±0.1			*	%
T_{MIN} to T_{MAX}			±0.15			±0.02	%
Bipolar Zero Error[3]			±0.1			*	% FSR[2]
			±20			±0.15	mV
T_{MIN} to T_{MAX}			±0.15			±0.15	% FSR
			±30			±0.15	mV
Power Supply Sensitivity of Full Scale			±0.003			*	%FSR/% V_{CC}
			±30			*	ppm FSR/% V_{CC}
DYNAMIC PERFORMANCE							
Settling Time (to ±0.003%FSR, 5kΩ || 500pF Load)[4]							
20V Output Step		6	10		*	10	µs
1LSB Output Step[5]		4			*		µs
Output Slew Rate		10			*		V/µs
Total Harmonic Distortion + Noise							
0dB, 1001Hz, f_S = 100kHz		0.005			*		%
–20dB, 1001Hz, f_S = 100kHz		0.03			*		%
–60dB, 1001Hz, f_S = 100kHz		3.0			*		%
SINAD							
1001Hz, f_S = 100kHz		87			*		dB
Digital Feedthrough[5]		2			*		nV–s
Digital-to-Analog Glitch Impulse[5]		15			*		nV–s
Output Noise Voltage (includes reference)		120			*		nV/√Hz
ANALOG OUTPUT							
Output Voltage Range							
$+V_{CC}$, $-V_{CC}$ = ±11.4V	±10			*			V
Output Current	±5			*			mA
Output Impedance		0.1			*		Ω
Short Circuit to ACOM, Duration		Indefinite			*		
REFERENCE VOLTAGE							
Voltage	+9.975	+10.000	+10.025	*	*	*	V
T_{MIN} to T_{MAX}	+9.960		+10.040	*		*	V
Output Resistance		1			*		Ω
Source Current	2			*			mA
Short Circuit to ACOM, Duration		Indefinite			*		
POWER SUPPLY REQUIREMENTS							
Voltage: $+V_{CC}$	+11.4	+15	+16.5	*	*	*	V
$-V_{CC}$	–11.4	–15	–16.5	*	*	*	V
Current (No Load, ±15V Supplies)							
$+V_{CC}$		13	15		*	*	mA
$-V_{CC}$		22	25		*	*	mA
Power Dissipation[6]		525	600			*	mW
TEMPERATURE RANGES							
Specification							
All Grades	0		+70	*		*	°C
Storage	–60		+150	*		*	°C
Thermal Coefficient, θ_{JA}							
DIP Package		75			*		°C/W
SOIC Package		75			*		°C/W

*Same specification as grade to the left.

NOTES: (1) Digital inputs are TTL and +5V CMOS compatible over the specification temperature range. (2) FSR means Full Scale Range. For example, for a ±10V output, FSR = 20V. (3) Errors externally adjustable to zero. (4) Maximum represents the 3σ limit. Not 100% tested for this parameter. (5) For the worst case code changes: $FFFF_{HEX}$ to 0000_{HEX} and 0000_{HEX} to $FFFF_{HEX}$. These are Binary Two's Complement (BTC) codes. (6) Typical supply voltages times maximum currents.

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ABSOLUTE MAXIMUM RATINGS

$+V_{CC}$ to COMMON	0V, +17V
$-V_{CC}$ to COMMON	0V, –17V
$+V_{CC}$ to $-V_{CC}$	34V
Digital Inputs to COMMON	–1V to $+V_{CC}$ –0.7V
External Voltage Applied to BPO and Range Resistors	$\pm V_{CC}$
$V_{REF\ OUT}$	Indefinite Short to COMMON
V_{OUT}	Indefinite Short to COMMON
Power Dissipation	750mW
Storage Temperature	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PACKAGE INFORMATION

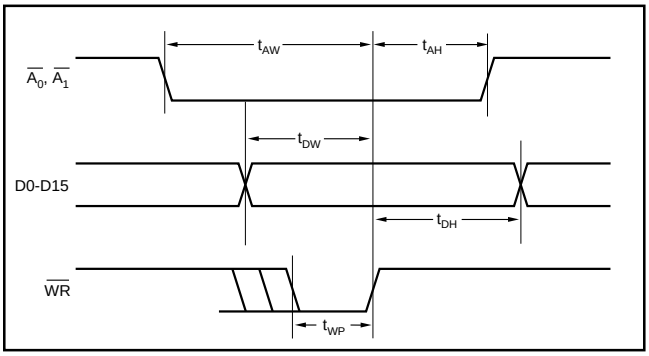
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
DAC712P	Plastic DIP	246
DAC712U	Plastic SOIC	217
DAC712PB	Plastic DIP	246
DAC712UB	Plastic SOIC	217
DAC712PK	Plastic DIP	246
DAC712UK	Plastic SOIC	217
DAC712PL	Plastic DIP	246
DAC712UL	Plastic SOIC	217
DAC712PC	Plastic DIP	246
DAC712UC	Plastic SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ORDERING INFORMATION

PRODUCT	TEMPERATURE RANGE	LINEARITY ERROR MAX at +25°C	DIFFERENTIAL LINEARITY ERROR MAX at +25°C
DAC712P	–40°C to +85°C	±4LSB	±4LSB
DAC712U	–40°C to +85°C	±4LSB	±4LSB
DAC712PB	–40°C to +85°C	±2LSB	±2LSB
DAC712UB	–40°C to +85°C	±2LSB	±2LSB
DAC712PK	0°C to +70°C	±2LSB	±2LSB
DAC712UK	0°C to +70°C	±2LSB	±2LSB
DAC712PL	0°C to +70°C	±2LSB	±1LSB
DAC712UL	0°C to +70°C	±2LSB	±1LSB
DAC712PC	–40°C to +85°C	±2LSB	±1LSB
DAC712UC	–40°C to +85°C	±2LSB	±1LSB

TIMING DIAGRAM



TIMING SPECIFICATIONS

T_A = –40°C to +85°C, $+V_{CC}$ = +12V or +15V, $-V_{CC}$ = –12V or –15V.

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{DW}	Data Valid to End of $\overline{WR}$	50		ns
t_{AW}	$\overline{A_0}$, $\overline{A_1}$ Valid to End of $\overline{WR}$	50		ns
t_{AH}	$\overline{A_0}$, $\overline{A_1}$ Hold after End of $\overline{WR}$	10		ns
t_{DH}	Data Hold after end of $\overline{WR}$	10		ns
t_{WP}(1)	Write Pulse Width	50		ns
t_{CP}	CLEAR Pulse Width	200		ns

NOTES: (1) For single-buffered operation, t_{WP} is 80ns min. Refer to page 10.

TRUTH TABLE

$\overline{A_0}$	$\overline{A_1}$	$\overline{WR}$	$\overline{CLR}$	DESCRIPTION
0	1	$1 \rightarrow 0 \rightarrow 1$	1	Load Input Latch
1	0	$1 \rightarrow 0 \rightarrow 1$	1	Load D/A Latch
1	1	$1 \rightarrow 0 \rightarrow 1$	1	No Change
0	0	0	1	Latches Transparent
X	X	1	1	No Change
X	X	X	0	Reset D/A Latch

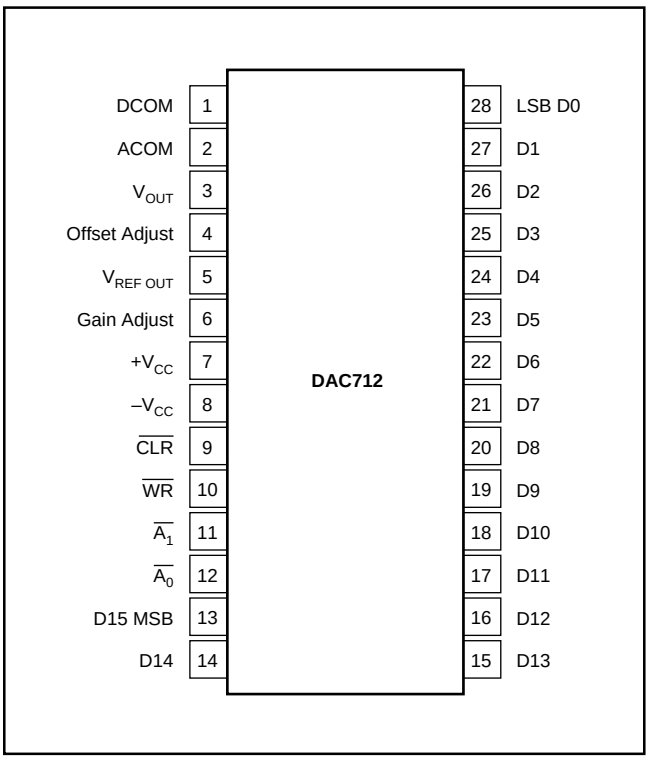
ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

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PIN CONFIGURATION



PIN DESCRIPTIONS

PIN	LABEL	DESCRIPTION
1	DCOM	Power Supply return for digital currents.
2	ACOM	Analog Supply Return.
3	V_{OUT}	±10V D/A Output.
4	Off Adj	Offset Adjust (Bipolar).
5	$V_{REF\ OUT}$	Voltage Reference Output.
6	Gain Adj	Gain Adjust.
7	$+V_{CC}$	+12V to +15V Supply.
8	$-V_{CC}$	–12V to –15V Supply.
9	$\overline{CLR}$	CLEAR. Sets D/A output to BIPOLAR ZERO (Active Low).
10	$\overline{WR}$	Write (Active Low).
11	$\overline{A_1}$	Enable for D/A latch (Active Low).
12	$\overline{A_0}$	Enable for Input latch (Active Low).
13	D15	Data Bit 15 (Most Significant Bit).
14	D14	Data Bit 14.
15	D13	Data Bit 13.
16	D12	Data Bit 12.
17	D11	Data Bit 11.
18	D10	Data Bit 10.
19	D9	Data Bit 9.
20	D8	Data Bit 8.
21	D7	Data Bit 7.
22	D6	Data Bit 6.
23	D5	Data Bit 5.
24	D4	Data Bit 4.
25	D3	Data Bit 3.
26	D2	Data Bit 2.
27	D1	Data Bit 1.
28	D0	Data Bit 0 (Least Significant Bit).

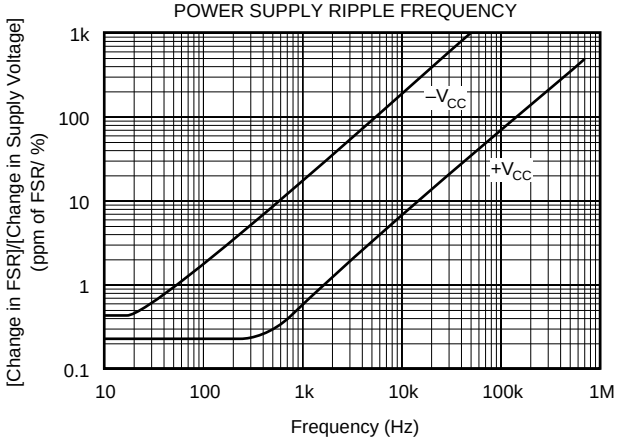
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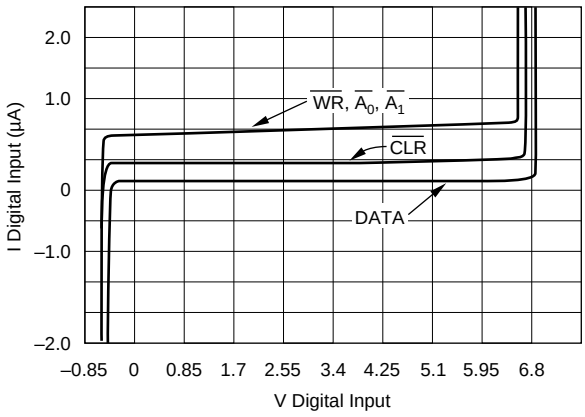
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_{CC} = ±15V, unless otherwise noted.

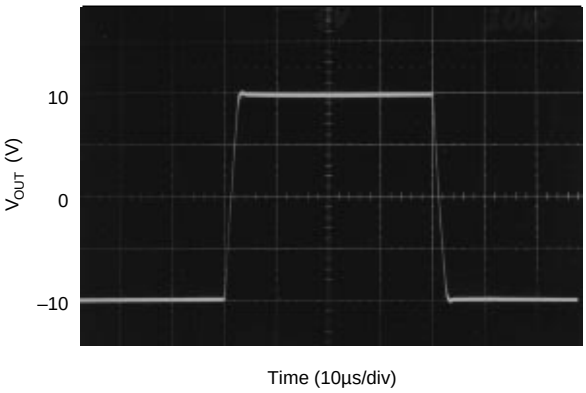
POWER SUPPLY REJECTION vs
POWER SUPPLY RIPPLE FREQUENCY



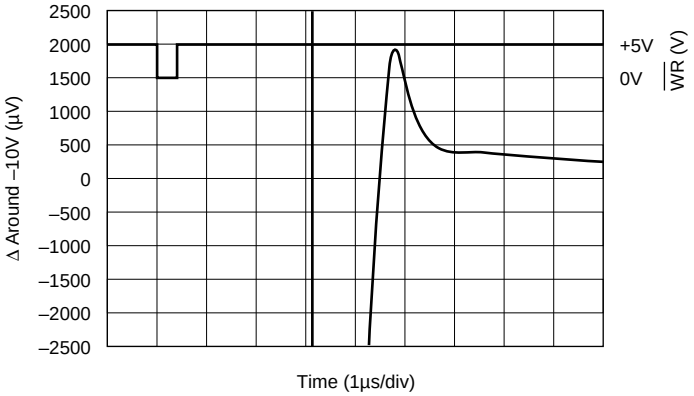
LOGIC vs V LEVEL



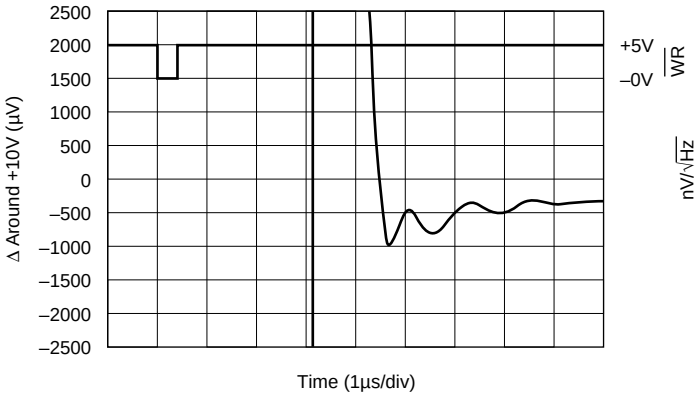
± FULL SCALE OUTPUT SWING



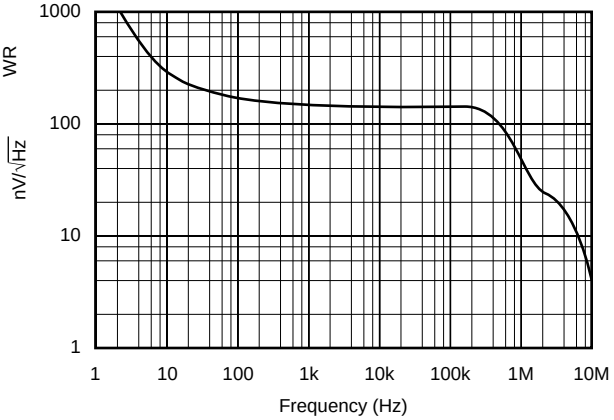
SETTLING TIME, +10V TO –10V



SETTLING TIME, –10V TO +10V



Spectral Noise Density



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DISCUSSION OF SPECIFICATIONS

LINEARITY ERROR

Linearity error is defined as the deviation of the analog output from a straight line drawn between the end points of the transfer characteristic.

DIFFERENTIAL LINEARITY ERROR

Differential linearity error (DLE) is the deviation from 1LSB of an output change from one adjacent state to the next. A DLE specification of ±1/2LSB means that the output step size can range from 1/2LSB to 3/2LSB when the digital input code changes from one code word to the adjacent code word. If the DLE is more positive than –1LSB, the D/A is said to be monotonic.

MONOTONICITY

A D/A converter is monotonic if the output either increases or remains the same for increasing digital input values. Monotonicity of DAC712 is guaranteed over the specification temperature range to 13, 14, 15, and 16 bits for performance grades DAC712P/U, DAC712PB/UB, DAC712PK/UK, and DAC712PL/UL respectively.

SETTLING TIME

Settling time is the total time (including slew time) for the D/A output to settle to within an error band around its final value after a change in input. Settling times are specified to within ±0.003% of Full Scale Range (FSR) for an output step change of 20V and 1LSB. The 1LSB change is measured at the Major Carry ($FFFF_{HEX}$ to 0000_{HEX}, and 0000_{HEX} to $FFFF_{HEX}$: BTC codes), the input transition at which worst-case settling time occurs.

TOTAL HARMONIC DISTORTION + NOISE

Total harmonic distortion + noise is defined as the ratio of the square root of the sum of the squares of the values of the harmonics and noise to the value of the fundamental frequency. It is expressed in % of the fundamental frequency amplitude at sampling rate f_S.

SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)

SINAD includes all the harmonic and outstanding spurious components in the definition of output noise power in addition to quantizing and internal random noise power. SINAD is expressed in dB at a specified input frequency and sampling rate, f_S.

DIGITAL-TO-ANALOG GLITCH IMPULSE

The amount of charge injected into the analog output from the digital inputs when the inputs change state. It is measured at half scale at the input codes where as many as possible switches change state—from $7FFF_{HEX}$ to 8000_{HEX}.

DIGITAL FEEDTHROUGH

When the A/D is not selected, high frequency logic activity on the digital inputs is coupled through the device and shows up as output noise. This noise is digital feedthrough.

OPERATION

DAC712 is a monolithic integrated-circuit 16-bit D/A converter complete with 16-bit D/A switches and ladder network, voltage reference, output amplifier and microprocessor bus interface.

INTERFACE LOGIC

DAC712 has double-buffered data latches. The input data latch holds a 16-bit data word before loading it into the second latch, the D/A latch. This double-buffered organization permits simultaneous update of several D/A converters. All digital control inputs are active low. Refer to block diagram of Figure 1.

All latches are level-triggered. Data present when the enable inputs are logic “0” will enter the latch. When the enable inputs return to logic “1”, the data is latched.

The $\overline{CLR}$ input resets both the input latch and the D/A latch to give a bipolar zero output.

LOGIC INPUT COMPATIBILITY

DAC712 digital inputs are TTL compatible (1.4V switching level) with low leakage, high impedance inputs. Thus the inputs are suitable for being driven by any type of 5V logic such as 5V CMOS logic. An equivalent circuit of a digital input is shown in Figure 2.

Data inputs will float to logic “0” and control inputs will float to logic “0” if left unconnected. It is recommended that any unused inputs be connected to DCOM to improve noise immunity.

Digital inputs remain high impedance when power is off.

INPUT CODING

DAC712 is designed to accept positive-true binary two’s complement (BTC) input codes which are compatible with bipolar analog output operation. For bipolar analog output configuration, a digital input of $7FFF_{HEX}$ gives a plus full scale output, 8000_{HEX} gives a minus full scale output, and 0000_{HEX} gives bipolar zero output.

INTERNAL REFERENCE

DAC712 contains a +10V reference.

The reference output may be used to drive external loads, sourcing up to 2mA. The load current should be constant, otherwise the gain and bipolar offset of the converter will vary.

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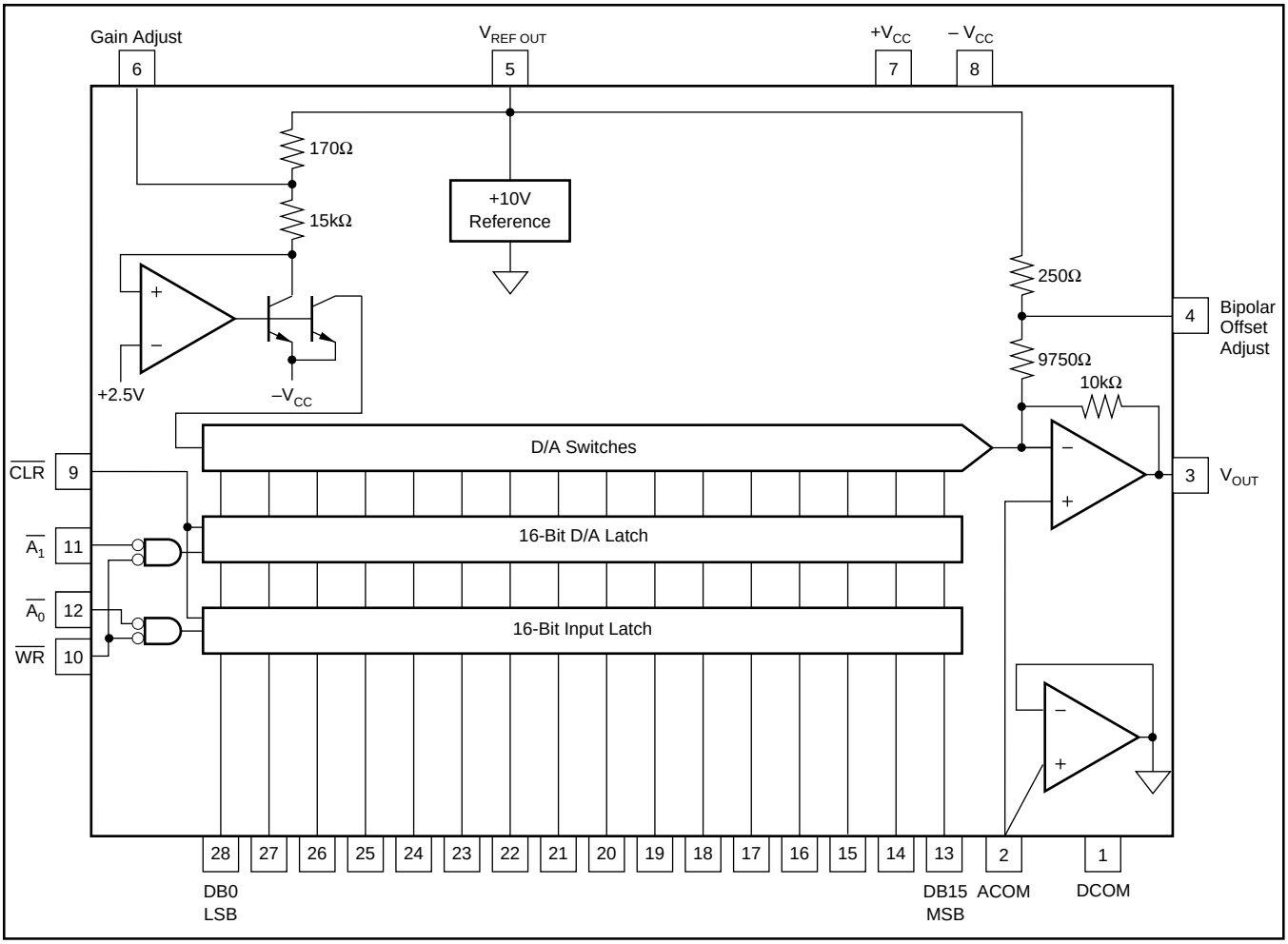


FIGURE 1. DAC712 Block Diagram.

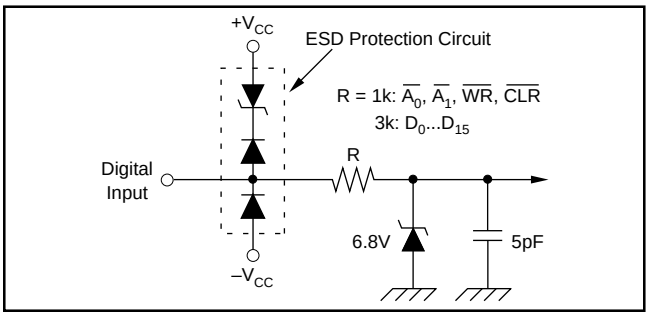


FIGURE 2. Equivalent Circuit of Digital Inputs.

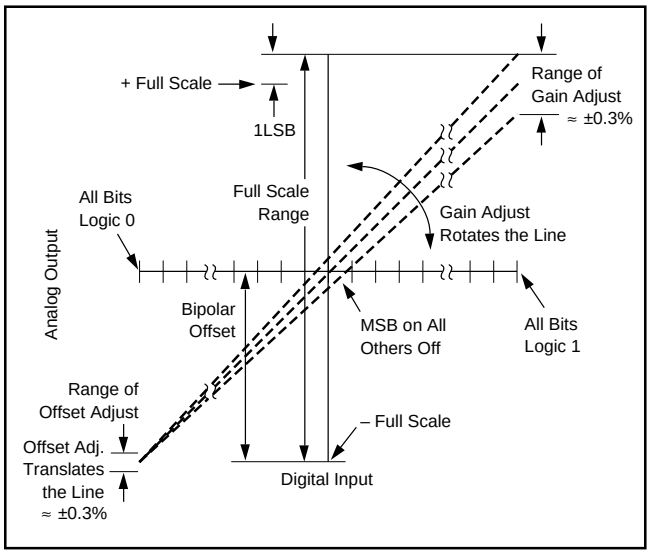


FIGURE 3. Relationship of Offset and Gain Adjustments.

OUTPUT VOLTAGE SWING

The output amplifier of DAC712 is committed to a ±10V output range. DAC712 will provide a ±10V output swing while operating on ±11.4V or higher voltage supplies.

GAIN AND OFFSET ADJUSTMENTS

Figure 3 illustrates the relationship of offset and gain adjustments for a bipolar connected D/A converter. Offset should be adjusted first to avoid interaction of adjustments. See Table I for calibration values and codes. These adjustments have a minimum range of ±0.3%.

Offset Adjustment

Apply the digital input code that produces the maximum negative output voltage and adjust the offset potentiometer or the offset adjust D/A converter for –10V.

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DAC712 CALIBRATION VALUES 1 LEAST SIGNIFICANT BIT = 305µV		
DIGITAL INPUT CODE BINARY TWO'S COMPLEMENT, BTC	ANALOG OUTPUT (V)	DESCRIPTION
$7FFF_H$	+9.999695	+ Full Scale –1LSB
4000_H	+5.000000	3/4 Scale
0001_H	+0.000305	BPZ + 1LSB
0000_H	0.000000	Bipolar Zero (BPZ)
$FFFF_H$	–0.000305	BPZ – 1LSB
$C000_H$	–5.000000	1/4 Scale
8000_H	–10.00000	Minus Full Scale

TABLE I. Digital Input and Analog Output Voltage Calibration Values.

Gain Adjustment

Apply the digital input that gives the maximum positive voltage output. Adjust the gain potentiometer or the gain adjust D/A converter for this positive full scale voltage.

INSTALLATION

GENERAL CONSIDERATIONS

Due to the high-accuracy of these D/A converters, system design problems such as grounding and contact resistance become very important. A 16-bit converter with a 20V full-scale range has a 1LSB value of 305µV. With a load current of 5mA, series wiring and connector resistance of only 60mΩ will cause a voltage drop of 300µV. To understand what this means in terms of a system layout, the resistivity of a typical 1 ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 5mA load, a 10 milli-inch wide printed circuit conductor 60 milli-inches long will result in a voltage drop of 150µV.

The analog output of DAC712 has an LSB size of 305µV (–96dB). The noise floor of the D/A must remain below this level in the frequency range of interest. The DAC712's noise spectral density (which includes the noise contributed by the internal reference,) is shown in the Typical Performance Curves section.

Wiring to high-resolution D/A converters should be routed to provide optimum isolation from sources of RFI and EMI. The key to elimination of RF radiation or pickup is small loop area. Signal leads and their return conductors should be kept close together such that they present a small capture cross-section for any external field. Wire-wrap construction is not recommended.

POWER SUPPLY AND REFERENCE CONNECTIONS

Power supply decoupling capacitors should be added as shown in Figure 4. Best performance occurs using a 1 to 10µF tantalum capacitor at $-V_{CC}$. Applications with less critical settling time may be able to use 0.01µF at $-V_{CC}$ as well as at $+V_{CC}$. The capacitors should be located close to the package.

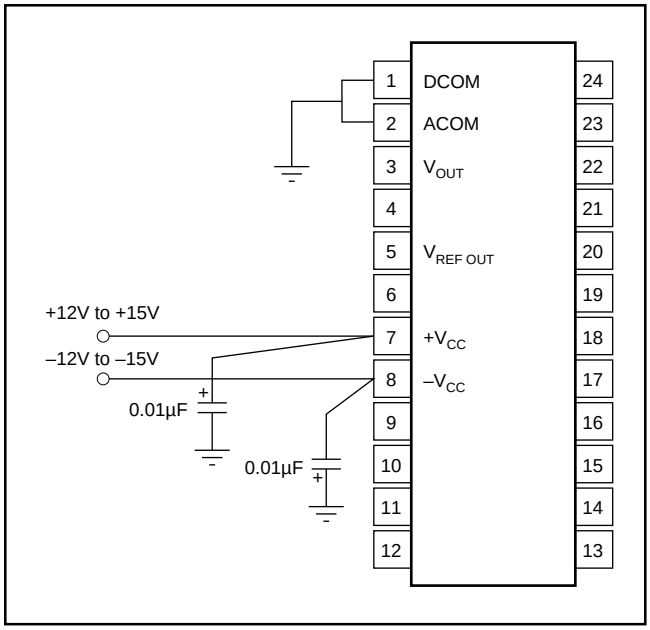


FIGURE 4. Power Supply Connections.

DAC712 has separate ANALOG COMMON and DIGITAL COMMON pins. The current through DCOM is mostly switching transients and are up to 1mA peak in amplitude. The current through ACOM is typically 5µA for all codes.

Use separate analog and digital ground planes with a single interconnection point to minimize ground loops. The analog pins are located adjacent to each other to help isolate analog from digital signals. Analog signals should be routed as far as possible from digital signals and should cross them at right angles. A solid analog ground plane around the D/A package, as well as under it in the vicinity of the analog and power supply pins, will isolate the D/A from switching currents. It is recommended that DCOM and ACOM be connected directly to the ground planes under the package.

If several DAC712s are used or if DAC712 shares supplies with other components, connecting the ACOM and DCOM lines to together once at the power supplies rather than at each chip may give better results.

LOAD CONNECTIONS

Since the reference point for V_{OUT} and $V_{REF\ OUT}$ is the ACOM pin, it is important to connect the D/A converter load directly to the ACOM pin. Refer to Figure 5.

Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance R_L is constant, R_1 simply introduces a gain error and can be removed by gain adjustment of the D/A or system-wide gain calibration. R_2 is part of R_L if the output voltage is sensed at ACOM.

In some applications it is impractical to return the load to the ACOM pin of the D/A converter. Sensing the output voltage at the SYSTEM GROUND point is reasonable, because

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there is no change in DAC712 ACOM current, provided that R_3 is a low-resistance ground plane or conductor. In this case you may wish to connect DCOM to SYSTEM GROUND as well.

GAIN AND OFFSET ADJUST

Connections Using Potentiometers

GAIN and OFFSET adjust pins provide for trim using external potentiometers. 15-turn potentiometers provide sufficient resolution. Range of adjustment of these trims is at least ±0.3% of Full Scale Range. Refer to Figure 6.

Using D/A Converters

The GAIN ADJUST and OFFSET ADJUST circuits of DAC712 have been arranged so that these points may be easily driven by external D/A converters. Refer to Figure 7. 12-bit D/A converters provide an OFFSET adjust resolution and a GAIN adjust resolution of 30µV to 50µV per LSB step.

Nominal values of GAIN and OFFSET occur when the D/A converters outputs are at approximately half scale, +5V.

OUTPUT VOLTAGE RANGE CONNECTIONS

The DAC712 output amplifier is connected internally for the ±10V bipolar (20V) output range. That is, the bipolar offset resistor is connected to an internal reference voltage and the 20V range resistor is connected internally to V_{OUT}. DAC712 cannot be connected by the user for unipolar operation.

DIGITAL INTERFACE

BUS INTERFACE

DAC712 has 16-bit double-buffered data bus interface with control lines for easy interface to interface to a 16-bit bus. The double-buffered feature permits update of several D/As simultaneously.

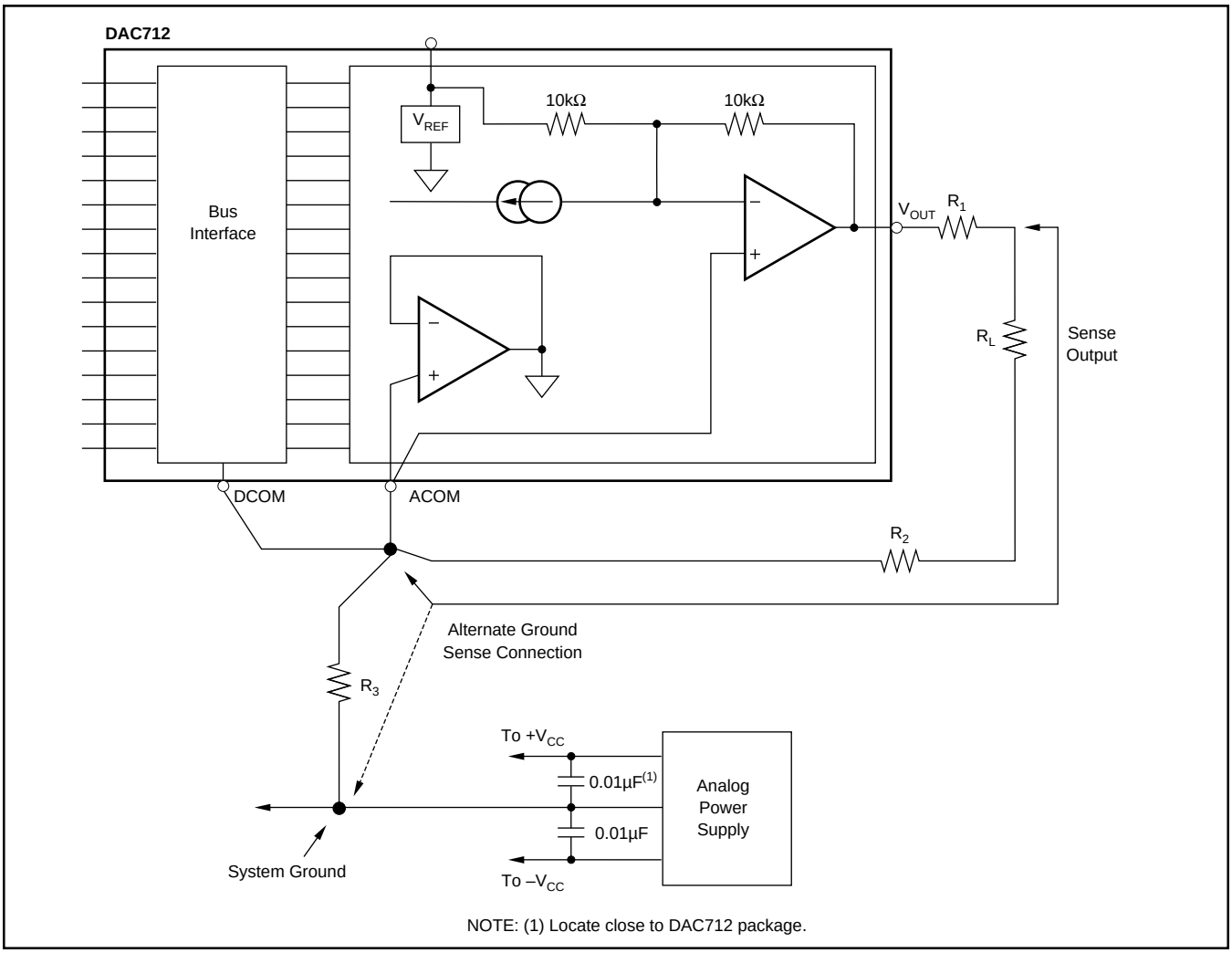


FIGURE 5. System Ground Considerations for High-Resolution D/A Converters.

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$\overline{A_0}$ is the enable control for the DATA INPUT LATCH. $\overline{A_1}$ is the enable for the D/A LATCH. $\overline{WR}$ is used to strobe data into latches enabled by $\overline{A_0}$, and $\overline{A_1}$. Refer to the block diagram of Figure 1 and to Timing Diagram on page 3.

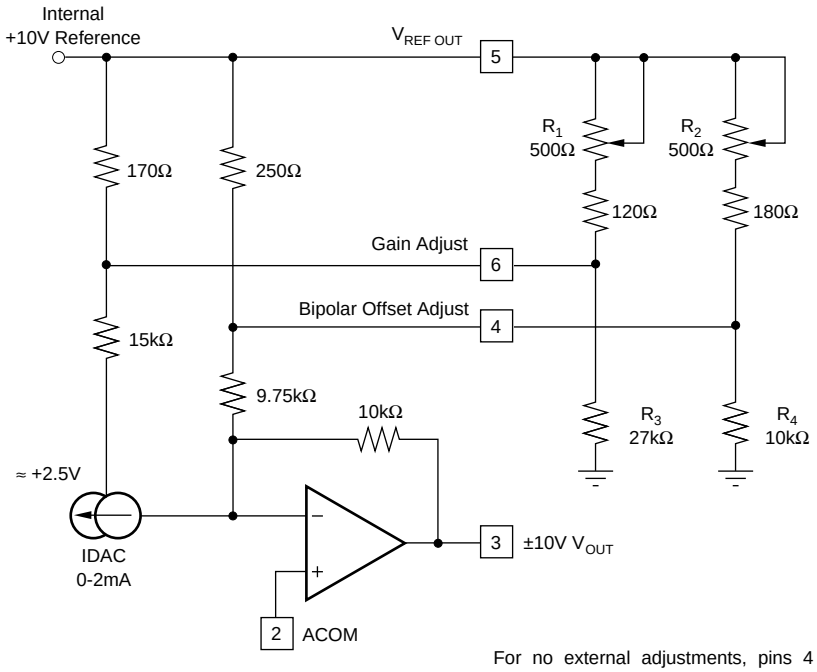
$\overline{CLR}$ sets the INPUT DATA LATCH to all zero and the D/A LATCH to a code that gives bipolar 0V at the D/A output.

SINGLE-BUFFERED OPERATION

To operate the DAC712 interface as a single-buffered latch, the DATA INPUT LATCH is permanently enabled by connecting $\overline{A_0}$ to DCOM. If $\overline{A_1}$ is not used to enable the D/A, it should be connected to DCOM also. For this mode of operation, the width of $\overline{WR}$ will need to be at least 80ns minimum to pass data through the DATA INPUT LATCH and into the D/A LATCH.

TRANSPARENT INTERFACE

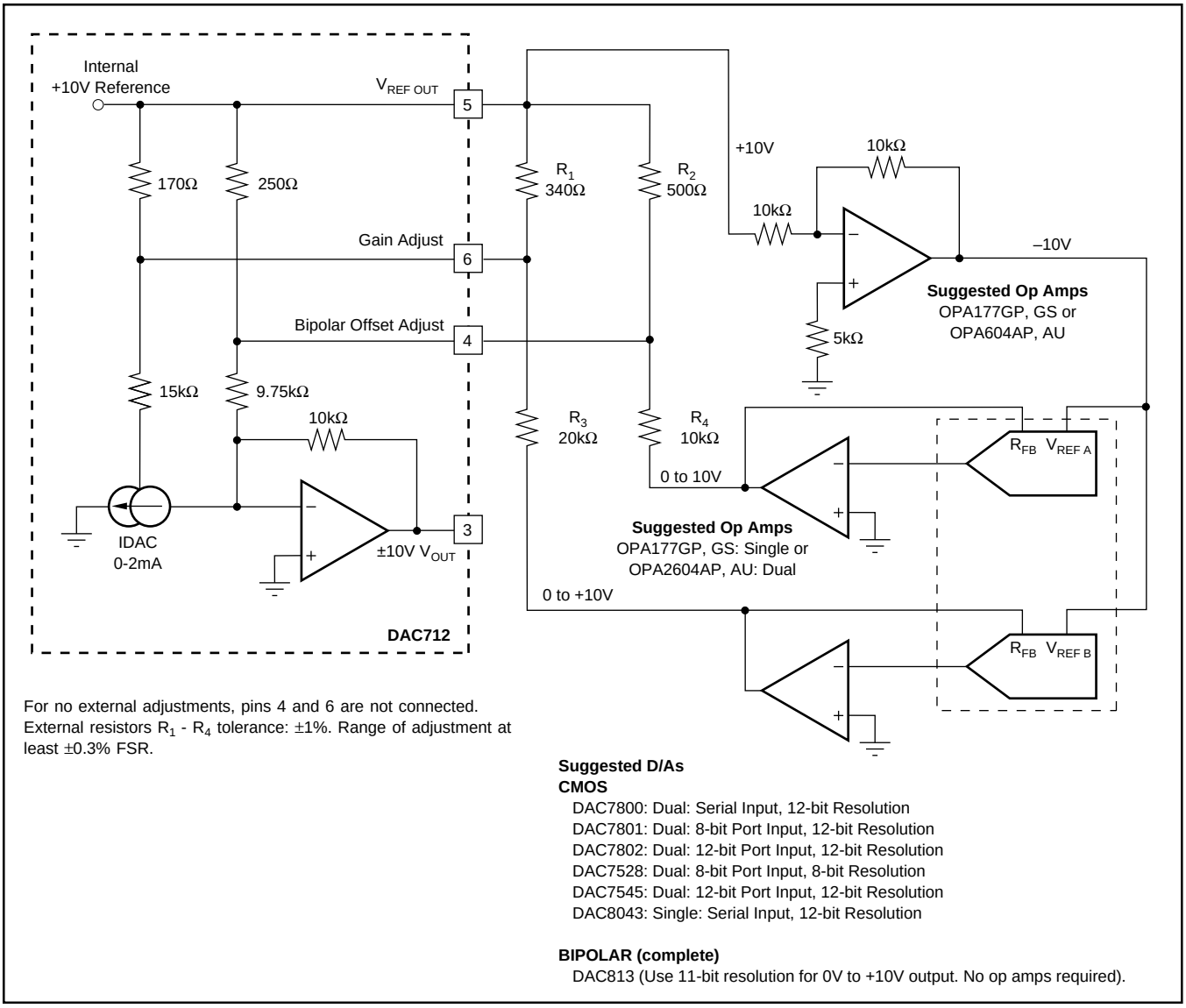
The digital interface of the DAC712 can be made transparent by asserting $\overline{A_0}$, $\overline{A_1}$, and $\overline{WR}$ LOW, and asserting $\overline{CLR}$ HIGH.



For no external adjustments, pins 4 and 6 are not connected. External resistors R_1 - R_4 are standard ±1% values. Range of adjustment at least ±0.3% FSR.

FIGURE 6. Manual Offset and Gain Adjust Circuits.

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For no external adjustments, pins 4 and 6 are not connected. External resistors R_1 - R_4 tolerance: ±1%. Range of adjustment at least ±0.3% FSR.

Suggested D/As

CMOS

DAC7800: Dual: Serial Input, 12-bit Resolution
DAC7801: Dual: 8-bit Port Input, 12-bit Resolution
DAC7802: Dual: 12-bit Port Input, 12-bit Resolution
DAC7528: Dual: 8-bit Port Input, 8-bit Resolution
DAC7545: Dual: 12-bit Port Input, 12-bit Resolution
DAC8043: Single: Serial Input, 12-bit Resolution

BIPOLAR (complete)

DAC813 (Use 11-bit resolution for 0V to +10V output. No op amps required).

FIGURE 7. Gain and Offset Adjustment Using D/A Converters.

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