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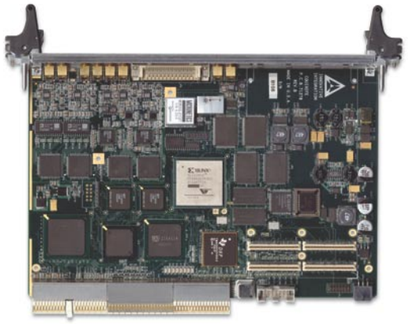
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Find the *Molex / Innovative Integration Quixote II* at our website: *Click HERE*

Quixote

High Speed DSP and FPGA card for digital radio, wireless test and development



RoHS 2002/95/EC Compliant

Quixote

Features

- 1 GHz TMS320C6416 DSP
- 32 MB SDRAM, 8 MB ZBT SBSRAM optional
- A/D: AD6645 14bit 105MSPS
- DAC: AD9764 14bit 105MSPS
- 64 bit CompactPCI
- PMC Site with Jn4 to FPGA
- 32-bit User DIO
- MATLAB and VHDL logic Development
- C/C++ DSP with DSP/BIOS RTOS

Applications

- Software Defined Radio
- Wireless IP Development & Hardware Testing
- Physical Layer Field Testing
- Ultra-Fast Flexible Data Acquisition
- Vector Signal Generation/Signal Identification
- RADAR
- Electronic Warfare

Hardware Options

- PCI to cPCI adapter
- Code Hammer Debugger
- 50 Ohm SMB to BNC Cable
- SyncLink/ClockLink Cable

Software Development Tools

- Pismo Toolset
- TI Code Composer Studio
- FrameWork Logic for VHDL/MATLAB

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MathWorks Partner

Ordering Information

Quixote I	80069-6
Quixote II	80069-7
Quixote III	80069-8

Overview

Quixote is a 64-bit cPCI 6U board that combines one Texas Instruments C6416 DSP with a two- or six- million-gate Xilinx Virtex-II FPGA, dual 105MSPS 14-bit analog input and output channels. A 64-bit 66MHz PCI interface and one PMC supports the addition of off-the shelf and custom PMC mezzanine boards.

A fast external digital interface is provided through connector JN4 of the PMC site, presenting 64 pins tied directly to the Virtex-II DIO, or alternatively configured as 31 pairs of LVDS signals. This interface provides a flexible and modular building block to implement any type of digital communication at 800MB/s. In addition, another 32-bit port is available for general purpose digital I/O.

Quixote is delivered in three different configurations. Quixote I is equipped with a "sealed" FPGA pre-loaded with turnkey firmware that gives user-friendly control of the analog I/O triggering to the DSP programmer. With Quixote I, no FPGA code development is required for the standard feature set.

Quixote II and Quixote III are the equivalent "open" platform for VHDL developers and ships with a 2 Million (XC2V2000) and 6 Million-gate (XC2V6000) VirtexII FPGA respectively.

DSP Processing Core

Quixote is powered by the new TMS320C6416 DSP from Texas Instruments, which uses the latest architecture of 32-bit fixed point DSP in the powerful C6000 series. Operating at 1GHz, the 6416 has processing power of 8000 MIPS. TI's highly parallel VelociTI architecture has multiple execution and math units that are optimized for signal processing applications. On-chip resources include eight highly independent functional units (6 ALUs and 2 Multipliers), an efficient memory structure consistent of 16 Kbytes of L1 data cache, 16 Kbytes of L1 program cache, 1 MByte of L2 Unified Mapped RAM/cache, hardware Viterbi and turbo decoder. The on-chip 32/33 PCI interface is interfaced to the host bus via a PCI bridge and tied to the Spartan II and PMC site.

There are two external memory interfaces: the 64-bit EMIF A is interfaced to the Virtex-II device and the SDRAM, while the 16-bit EMIF B is primarily used for the streaming PCI interface. The chip also has 2 multi-channel buffered synchronous serial port (McBSP) connected to the Virtex-II and capable of 100Mbps each.

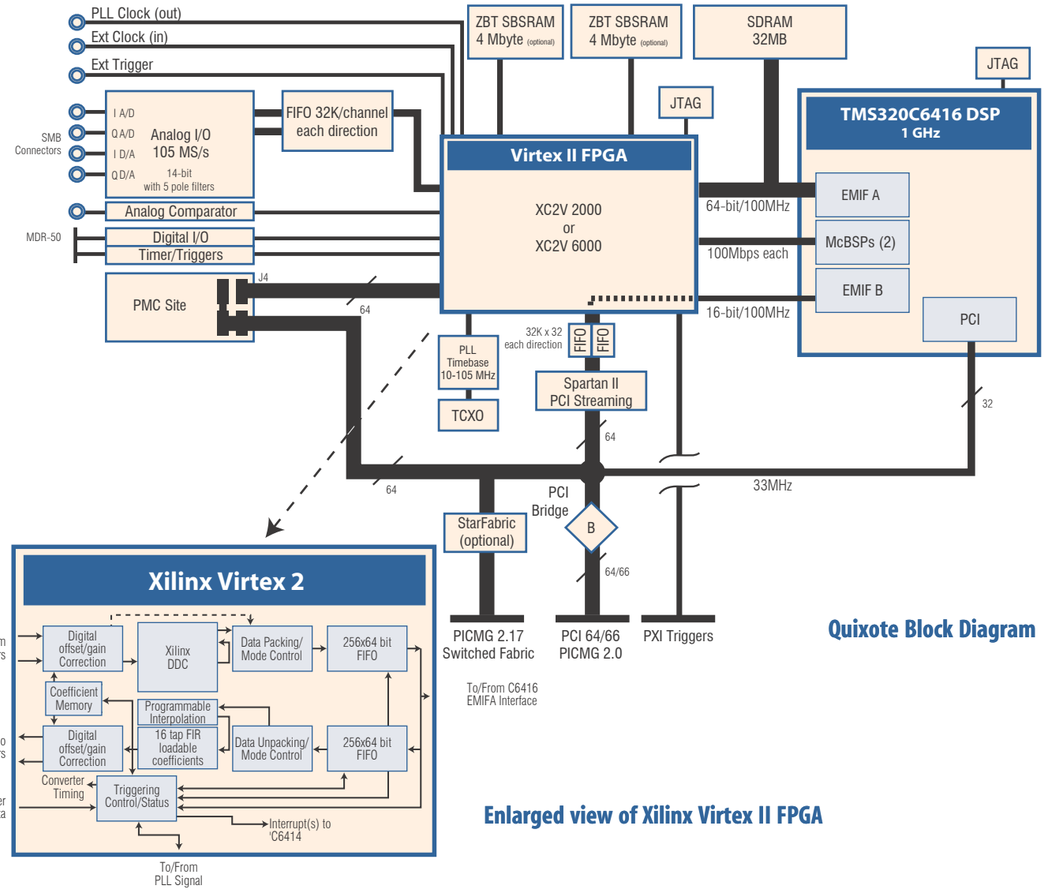
FPGA Core

Quixote utilizes a Xilinx Virtex 2 FPGA that directly connects to the DSP and I/O. There is up to 8MB of buffer for FPGA use.

- 2M or 6M gates
- Up to 8M SRAM memory
- Direct connection to A/D and DAC data streams
- Direct connection to DSP EMIFs A and B
- Direct connection to PMC J4
- Connection to 40 bits digital I/O

On-Board Memory

- 32MB DRAM on EMIFA running at 100MHz
- 4 or 8 MB SRAM for FPGA use



Quixote Block Diagram

Enlarged view of Xilinx Virtex II FPGA

Time Base and Trigger Mechanisms

The board supports a user-configurable timebase switch matrix, built in logic, that allows the user to select the input of any timebase from a choice of clock sources: on-chip and off-chip timers, VCO-based PLL, external clock, SyncLink/ClockLink.

The M/N + Pre-scalar PLL timebase uses a 5ppm 20MHz TCXO oscillator, delivering the best combination of low jitter and high-resolution clock pulse train. Output frequency range is 50-105MHz, with a 14.4MHz resolution.

The start/stop triggering methods can be configured for any of the following triggering methods:

- External trigger
- Analog threshold trigger
- Continuous streaming
- Framed acquisition (specified by either duration or sample count)
- Pre/post trigger sampling
- Re-trigger mode

In multi-card applications, any of these triggers can be shared between cards using the PXI triggers.

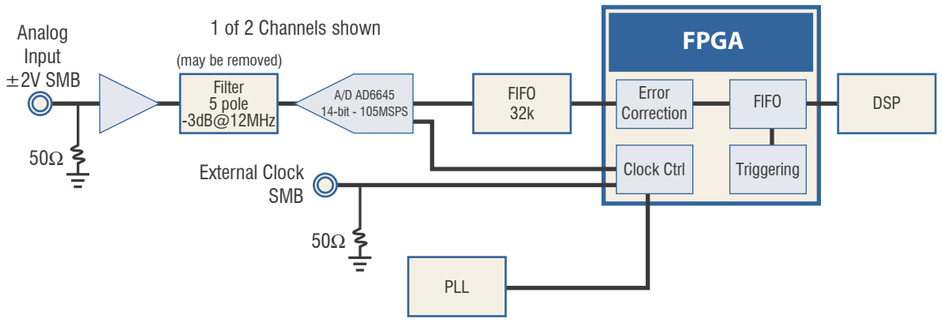
A real-time alert log in the firmware provides the user with a precision record of various events such as trigger times, data integrity monitoring and user-defined events. These features are all implemented in logic and can therefore be extended or customized to support new applications.

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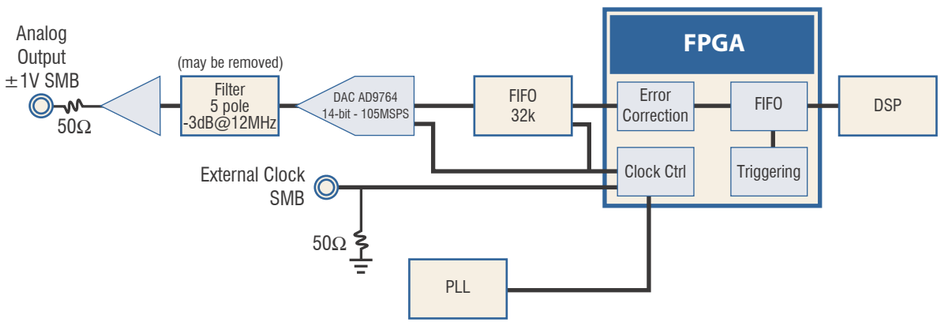
Innovative Integration
real time solutions

Analog Input



Dual Channel 14-bit, 105 MSPS A/D converters with filters and buffering directly connect to the FPGA

Analog Output



Dual Channel 14-bit, 105 MSPS D/A converters with filters and buffering directly connect to the FPGA

IEEE 1386 PMC Expansion Site

- Single width PMC site, 33MHz, 64-bit PCI interface
- J4 connection (64 signals) direct to FPGA

Quixote offers one 64bit/33MHz 3.3V PCI Mezzanine Card site (PMC) for a fast integration of off-the-shelf or custom daughter cards and support of a wide variety of peripherals like analog I/O, communication ports like FPDP or FPDP-II or custom I/O modules. This peripheral is mapped to be accessed by the DSP over the PCI bus (Jn1-Jn3), or by the FPGA using Jn4 as private data link. The PMC site 64-pin Jn4 connector is hooked straight to the Virtex-II digital I/O pins, offering an ultra high-speed, low latency, digital port for data movement as well as flexible configuration and synchronization signals. This port is capable of 800MB/s burst. The port can also be configured as 31 pairs of LVDS signaling at burst transfer rates close to 400MB/s. This can be used for adding high-speed serial interfaces where the mezzanine card handles data serializing/de-serializing and transmission protocols to external hardware.

Other System-Level Peripherals

- 32 bits Digital I/O
- PXI Triggers
- External sample clock and trigger
- PCI interface with 64-bit/33MHz

DSP Development Tools

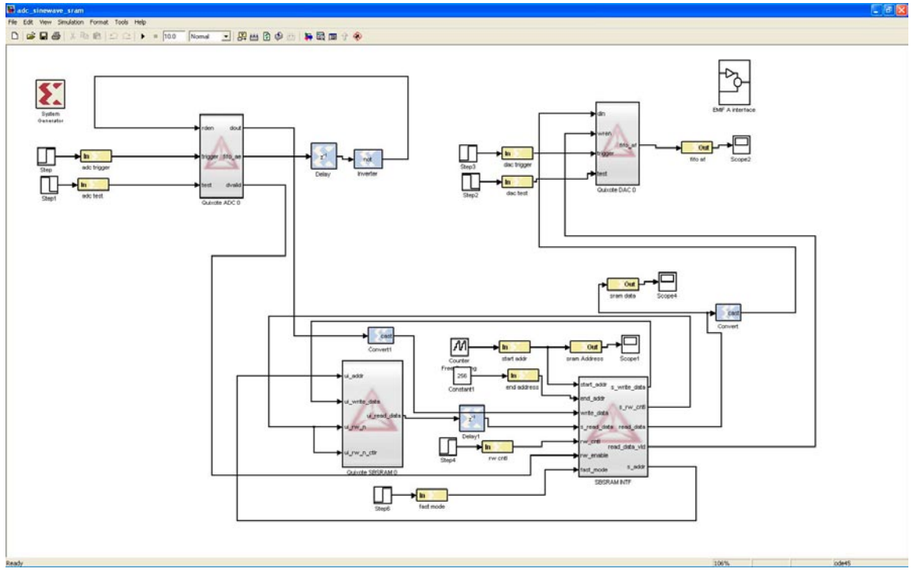
- TI Code Compser Studio required for DSP development
- C/C++ with Texas Instruments DSP/BIOS RTOS
- Pismo Toolset provides drivers examples and source code
- Malibu host support tools provide windows drivers, examples and support tools
- Visual C++/Borland C++

First time buyers of Quixote need to purchase the Quixote card, TI's Code Composer Studio DSP development environment, the JTAG debugger emulator and the Pismo Toolset for Quixote. The Pismo Toolset includes everything the developer will need to immediately begin code development for the 'C6416 DSP. From target-specific DSP and peripheral libraries in source code, single-command board-level functions to convenient utility applets allowing terminal emulation, download, execution and high-level debugging, it also provides a complete set of source code examples demonstrating full operation of all hardware resources. Pismo is fully supported from within Texas Instruments' Code Composer Studio. And of course, DSP/BIOS is supported with specific example project files and Bios device drivers. Drivers for the analog interface and other peripherals are provided for DSP/BIOS and PCI bus control support.

FPGA Logic Development

Logic development using VHDL and MATLAB is supported. The FrameWork Logic User's Guide fully describes the VHDL logic, which includes peripheral interfaces for all analog I/O and the DSP.

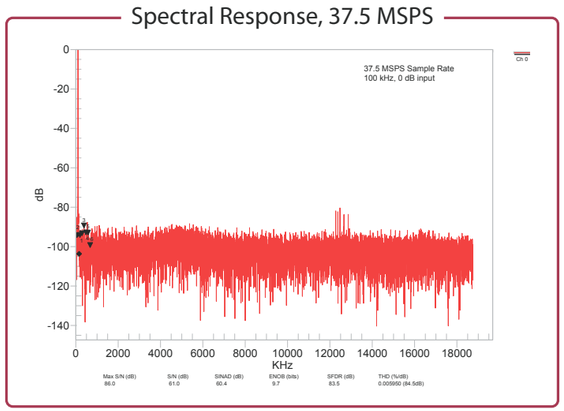
The board support package for MATLAB SimuLink and Xilinx System Generator provides a comprehensive development and simulation toolset for DSP development and testing.



Block sets for the Quixote include A/D, DAC, DSP and memory interfaces that provide full hardware access to MATLAB users.

OEM Configuration

Quixote can be configured to fit your specific requirements and provide the optimum mix of performance and features in cost sensitive volume applications. Contact Innovative Integration Sales department with your specific OEM needs.



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Digital Signal Processor

1GHz Texas Instruments TMS320C6416
32-bit fixed-point DSP
16 KB data L1 cache
16 KB program L1 cache
1Mbyte L2 cache
(3) 32-bit timers
64 EDMA channels

FPGA

Xilinx Virtex-II XC2V2000 or XC2V6000

Interface DSP/Virtex

EMIF A, 64 bit/100MHz interface
Mirrored EMIFB to PCI interface
(2 McBSP) Sync serial ports - 100Mbit/sec ea.

Memory

32 Mbytes of SDRAM; 8 Mbytes zero bus turnaround SBSRAM (Quixote II or III only)
32 MB flash EEPROM for FPGA configuration bitstream
512 Byte serial EEPROM for converter calibration coeff.

CompactPCI bus

64-bit/66 MHz
Local bus 33MHz Capable of 264/132Mbytes/sec respectively
DSP on local PCI bus
FIFO interface to DSP-100 MHz, 16-bit, EMIF B
(16) 32-bit bi-directional mailboxes

Digital I/O

40 bits I/O, 3.3V direct to FPGA
64bit I/O via PMC site Jn4 connector direct to FPGA

Timebase

PLL 14.4MHz resolution
Frequency Range: 25-105MHz
External clock input on SMB connector
PXI compatible
Synchronize with common triggers or clocks
5 PXI Triggers, 1 Star Trigger

A/D Channels

(2) 14-bit Analog Devices AD6645 converters
Sampling Rate: 30-105MHz
DC-coupled input
Digital gain/offset correction in logic

Input Range

±1V, single ended, 50 Ohm impedance

Input Filter

5 pole, analog low pass anti-alias filter (may be removed)
Standard config -3dB rolloff at 13.3MHz

D/A Channels

(2) 14-bit Analog Devices AD9764 converters
Sampling Rate: DC to 105MHz
Digital gain/offset correction in logic

Output Range

±1V Single ended, DC Coupled, 50 ohm impedance

Output Filter

5 pole analog smoothing filter (may be removed)
-3dB rolloff at 10.1MHz
Custom filters may be added

Triggering Modes

Continuous, single-shot, re-triggered modes
Software selectable start/stop triggers include software driven, external stop/start, number of points
Decimation

Connectors

PICMG 2.17 compliant cPCI interface (Q1 2005)
IEEE 1386 compliant PMC site, Jn1-Jn4 connectors
A/D and D/A - SMB connectors (4)
External Clock - SMB connector
External Interrupt - SMB connector
Analog Comparator Input - SMB connector
32-bit DIO, Timers, Start/Stop Triggers – MDR50 connector
DSP JTAG – 14-pin 0.1" shrouded male header
Virtex-II JTAG – 14-pin 2mm male header

Physical Size

6U CompactPCI card

Operating Environment

Forced air cooling required
Operating Temperature: 0°C - 55°C ambient, non-...
Designed to meet ETS 300 019-1.1 class 1.2, ETS 300 019-1.2 class 2.3, ETS 300 019-1.3 class 3.3

Power Requirements

+5V 1.9A; 3.3V 1.1A; ±12V 0.07A;
Total<15W

Development Languages

DSP

C/C++ with TI DSP/BIOS RTOS
Pismo toolset for DSP

FPGA

VHDL using Xilinx ISE and ModelSim
MATLAB using Xilinx System Generator

Host

Borland C++ Builder or Microsoft VC++

DSP Operating system

Texas Instruments DSP/BIOS II

Support PC OS

Windows2000/XP
Malibu host toolset for device drivers and applets

Host PC

Intel processor recommended for MMX library support

Software Selection Guide for Quixote

Software Package	Description	Usage/Requirements	Recommendations
Pismo Toolset	Peripheral libraries needed for developing code on this card. Includes host applications, target examples in source form demonstrating use of peripherals on the card, DSP-BIOS peripheral device driver.	Requires CCStudio*. Windows2000/XP compatible.	Includes Caliente DLL and Armada.
FrameWork VHDL	MATLAB and VHDL logic board support package	Requires Xilinx ISE and ModelSim for VHDL; MATLAB and Xilinx System Generator may also be used.	Recommended for experienced FPGA design developers who use Quixote for custom firmware development/implementation.
Caliente DLL	Dynamic link library (DLL) for the Quixote.	Requires ANSI-compliant C/C++ compiler. For example, Microsoft Visual C/C++ or Borland C++ Builder.	Required for interfacing Host side code to DSP.
CCStudio 'C6000	Integrated development environment (IDE) for Target side development/debugging from Texas Instruments.	Requires XDS-510 compatible JTAG emulator for debugging capabilities.	Required for all first time users. Recommend use with Innovative Integration plug-n-play PCI JTAG emulator.
Armada	Host side development package using a revolutionary integrated development environment (IDE). Allows user to build/debug sophisticated data acq apps fully using MS Windows graphical environment quickly with Innovative Integration's Visual Component Libraries (VCL) of MFC Classes.	Requires Borland C++ Builder* or Microsoft Visual C++.	Offers easiest interface while providing the most flexibility and performance. Ties into a plethora of 3rd party components.

*Contact Innovative Integration for current release version.

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