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Preliminary

MONARCH

PCI Frame Synchronizer / Telemetry Simulator with Reed-Solomon Encoder / Decoder

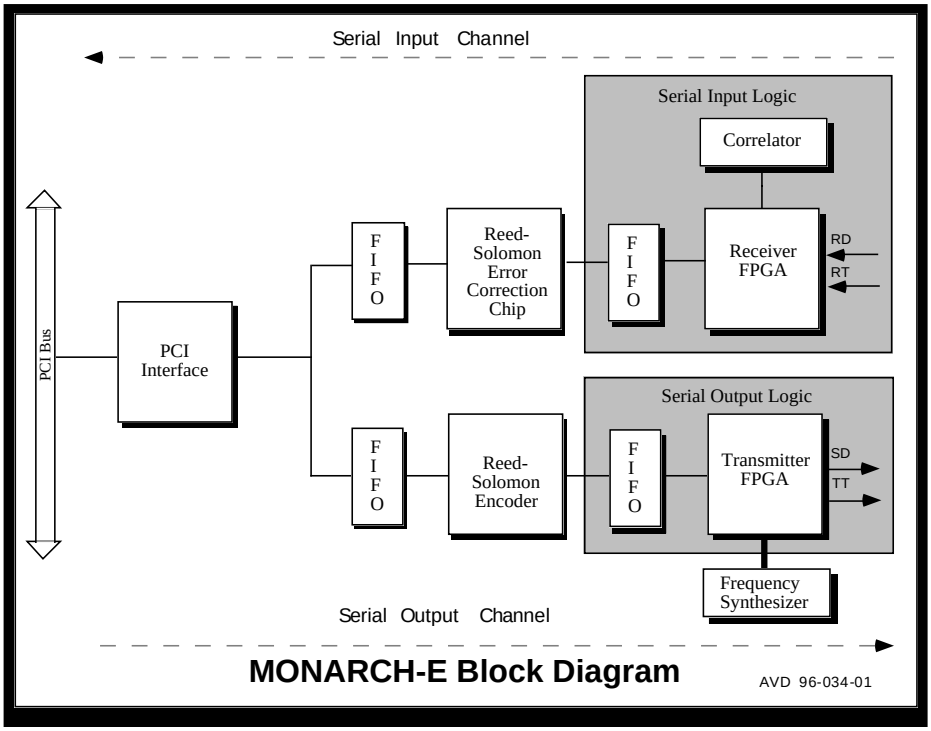
PCI-6100 / PCI-6200

Applications

- CCSDS/TDM Front-end processor
- High Speed PCM Frame Synchronization
- CCSDS / TDM Simulator
- Command Uplink

Features

- Supports both packetized and TDM telemetry, including CCSDS and IRIG formats
- Bidirectional synchronous serial I/O at up to 25 Mbps
- 32-bit PCI interface supports burst transfer rates of 133 MBps
- Serial input performs frame synchronization, derandomization, deinterleaving, Reed-Solomon decoding and outputs data to PCI bus
- Serial output reads data from PCI bus and performs CRC encoding, Reed-Solomon encoding, interleaving, sync marker insertion, pseudo-randomization, and convolutional encoding
- Programmable sync pattern, frame length, word size, and data code
- Onboard frequency synthesizer with output frequency from 100 Hz to 25 MHz
- TTL, RS422 or ECL clock and data I/O



Overview

The MONARCH Frame Synchronizer / PCM Simulator by Avtec Systems, Inc. is a PCI-based serial I/O card that supports both CCSDS (Conventional and Advanced Orbiting Systems) and time division multiplexed (TDM) data formats.

The MONARCH-E, an enhanced version of the MONARCH, provides a Reed-Solomon encoder /decoder to provide complete block error detection and correction for each of the CCSDS-recommended grades of service for Advanced Orbiting Systems.

The MONARCH/MONARCH-E input channel accepts serial data and clock from a bit synchronizer with Viterbi decoder and outputs frame data to the PCI bus. The input channel performs frame synchronization, derandomization, CRC error detection, deinterleaving, Reed-Solomon error detection and correction, time-tagging, and quality annotation. The input channel transfers annotated frame data to PC memory for further processing.

The MONARCH/MONARCH-E output channel reads frame data from PC memory via the PCI bus and outputs serial data and clock at up to 25 Mbps. The output channel performs Reed-Solomon encoding, interleaving, CRC encoding, sync marker insertion, pseudo-randomization, and convolutional encoding.

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Hardware

The MONARCH-E contains five functional components:

- Serial Input logic
- Reed-Solomon Error Correction chip
- PCI interface
- Reed-Solomon Encoder
- Serial Output Logic

Serial Input Logic

For CCSDS telemetry, the serial input logic synchronizes to channel access data units and formats them for input to the Reed-Solomon Decoder. For TDM telemetry, the serial input logic bypasses the Reed-Solomon Decoder and outputs frame data directly to the PCI interface. Programmable frame synchronizer parameters include: sync pattern and mask, error threshold, check frames, flywheel frames, frame length, word size, and bit slip window. The serial input logic automatically performs polarity correction based on the detected sync pattern polarity. The serial input logic also performs derandomization and CRC-16 VCDU error detection.

Reed-Solomon Error Correction (RSEC)

The RSEC chip is an LSI Logic ASIC that was designed by engineers at NASA's Goddard Space Flight Center. The RSEC chip accepts parallel data from the Serial Input Logic. It performs RS(255,223) VCDU error correction with interleaving depth from 1 to 8, RS(10,6) VCDU header error correction, and real-time quality generation and annotation. Shortened code blocks are also supported. The RSEC chip outputs corrected VCDUs with quality annotation to the PCI Interface.

PCI Interface

The PCI interface is based on the AMCC "Matchmaker" chip. It provides full PCI compatibility, including support for burst mode operation and peer-to-peer transfers with any PCI initiator/target. The PCI interface transfers frame data to/from the host processor's memory at up to 133 MBps.

Reed-Solomon Encoder

The Reed-Solomon encoder is implemented in a Field Programmable Gate Array. The encoder accepts parallel data from the PCI interface and performs RS(255,223) VCDU encoding with an interleave depth from 1 to 8 as well as RS(10,6) VCDU header encoding. Shortened code blocks are also supported. The RS encoder outputs interleaved code words to the Serial Output Logic.

Serial Output Logic

The serial output logic performs sync marker insertion, parallel to serial conversion, CRC encoding, pseudo-randomization, and convolution encoding at up to 25 Mbps. It contains a programmable frequency synthesizer with an output range from 100 Hz to 25 MHz.

Either a BNC or TRIAXIAL breakout cable is required for each board.

Ordering Guide

Part No.	Description
PCI-6100	MONARCH-E - PCI Frame Sync / Telemetry Simulator w/ Reed-Solomon Encoder/ Decoder
PCI-6200	MONARCH - PCI Frame Sync / Telemetry Simulator
CB-0100	BNC Breakout Cable for TTL signals
CB-0200	TRIAXIAL Breakout Cable for RS-422 signals

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Specifications

Serial Input/Output Options

- Data rates to 25 Mbps
- TTL signals
  - 50 Ohm termination
  - BNC connectors
- RS-422 signals
  - 120 Ohm termination
  - TRIAX connectors

Frame Synchronizer

- Programmable frame sync pattern up to 32 bits
- Programmable frame sync mask up to 32 bits
- Programmable error threshold for acceptable sync patterns up to 15 bit errors
- Adaptive sync strategy with 0 to 7 check frames and 0 to 7 flywheel frames
- Programmable bit slip window from 0 to ± 3
- Auto-polarity detection and correction
- Frame length up to 8192 words/frame
- Programmable word size from 4 to 16 bits

De-randomizer

- Exclusive OR received frame data following sync pattern with pseudo-random pattern given by
  $h(x) = x^8 + x^7 + x^5 + x^3 + 1$
- Shift register is initialized to all "ones" at the start of each frame

CRC Frame Error Control

- Compute frame error control field from received data using the polynomial $g(x) = x^{16} + x^{12} + x^5 + 1$
- Feed-back shift register is initialized to all "ones" at the start of each frame
- Programmable inclusion/exclusion of Attached Sync Marker

Reed-Solomon Error Correction

- CCSDS Reed-Solomon (255,223) error correction
- Support for shortened code blocks using "virtual" fill
- Interleave depth from 1 to 8
- CCSDS Reed-Solomon (10,6) header error correction
- Real-time quality generation and annotation for each VCDU

Telemetry Simulator

- Programmable sync marker insertion
- Programmable clock and data polarity
- Frame length up to 8192 words/frame
- Programmable word size from 4 to 16 bits
- Programmable output frequency from 100 Hz to 25 MHz

Convolutional Encoder

- Rate 1/2, constraint-length 7, convolutional code
- Connection vectors G1 = 1111001 and G2 = 1011011
- Programmable parity order and parity inversion

Pseudo-Randomizer

- Exclusive OR frame data following sync pattern with pseudo-random pattern given by
  $h(x) = x^8 + x^7 + x^5 + x^3 + 1$

- Shift register is initialized to all "ones" at the start of each frame

CRC Frame Error Control

- Compute frame error control field using the polynomial
  $g(x) = x^{16} + x^{12} + x^5 + 1$
- Feed-back shift register is initialized to all "ones" at the start of each frame
- Overlay computed CRC remainder into output frame
- Programmable inclusion/exclusion of Attached Sync Marker

Reed-Solomon Encoding

- CCSDS Reed-Solomon (255,223) encoding
- Support for shortened code blocks using "virtual" fill
- Interleave depth from 1 to 8
- CCSDS Reed-Solomon (10,6) header encoding

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